MP8008L

Fully Integrated, 802.3af/at-Compliant, PoE, PD Interface with a Peak-Current-Mode Flyback Controller

The Future of Analog IC Technology

DESCRIPTION

The MP8008L is an integrated, IEEE, 802.3af/at, PoE-compliant, powered device (PD), power supply converter. The MP8008L includes PD interface and a peak-current-mode flyback controller.

The PD interface has all the functions of IEEE 802.3af/at, including detection, 1-event and 2-event classification, 85mA inrush current limit, 840mA operation current limit, and a 100V hot-swap MOSFET.

The flyback pulse-width modulation (PWM) controller can drive an external MOSFET capable of handling more than 10A of current for high-power flyback PoE applications. Pulse-skip mode improves efficiency in light-load conditions. Other protection features include overload protection (OLP), short output, and over-voltage protection (OVP).

The MP8008L can support a front-end solution for PoE PD application with minimal external components and is available in a QFN-28 (4mmx5mm) package.

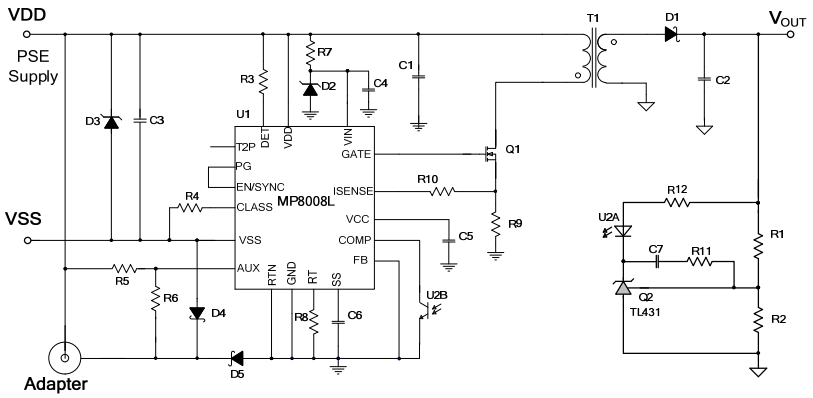
FEATURES

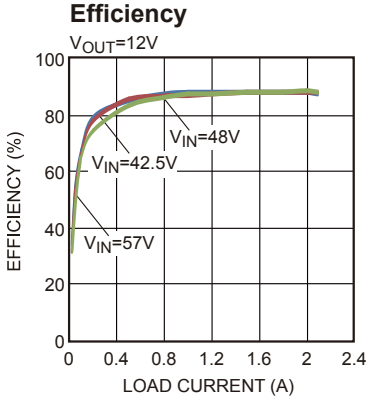
- Compatible with 802.3af/at Specifications
- 34V PD Power-On Rising UVLO
- 100V, 0.48Ω PD Integrated Pass Switch
- 85mA PD Inrush Current
- 840mA PD Operation Current Limit
- Auxiliary Adaptor O-Ring Power Supply
- PD Power Good and Type-2 PSE Indicator
- 12V, 1A, Flyback MOSFET Gate Driver
- Pulse-Skip Operation in Light Load
- Programmable Switching Frequency: 30kHz - 400kHz
- Frequency Synchronizing from 80kHz - 400kHz
- Cycle-by-Cycle Current Limit
- Overload Protection (OLP), Short-Circuit Protection (SCP), Over-Voltage Protection (OVP), and Thermal Protection
- Available in a QFN-28 (4mmx5mm) Package

APPLICATIONS

- IEEE 802.3af/at-Compliant Devices
- Security Cameras
- Video Telephones
- WLAN Access Points
- IoT Devices

TYPICAL APPLICATION





ORDERING INFORMATION

Part Number*	Package	Top Marking
MP8008LGV	QFN-28 (4mmx5mm)	*See Below*

*** FOR TAPE & REEL, ADD SUFFIX –Z (E.G. MP8008LGV–Z)**

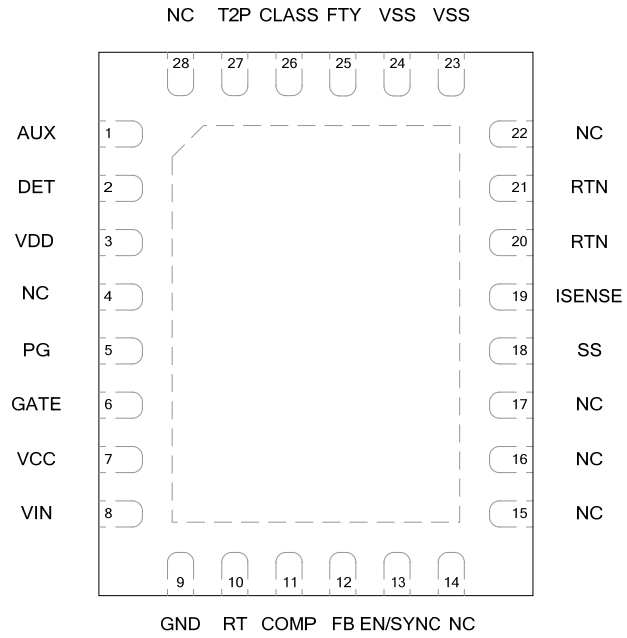
TOP MARKING

MPSYWW
M8008L
LLLLLL

MPS: MPS prefix
Y: Year code
WW: Week code
MP8008L: Part number
LLLLLL: Lot number

PACKAGE REFERENCE

TOP VIEW



QFN-28 (4mmx5mm)

ABSOLUTE MAXIMUM RATINGS (1)

Pin Voltage with Respect to VSS

VDD, RTN, DET, T2P, AUX, GND ..... -0.3V to +100V
CLASS, FTY ..... -0.3V to +6.5V

Pin Voltage with Respect to GND (2)

VDD ..... -0.3V to +100V
VIN ..... -0.3V to 40V
VCC, GATE ..... -0.3V to 15V
All other pins ..... -0.3V to 6V

Pin Voltage with Respect to VDD

AUX ..... -6.5V to +0.3V (3)

Pin Current

T2P sink current 10mA
AUX sink current ..... -5mA (3)
PG sink current 1mA (4)
EN/SYNC sink current 0.5mA (5)
Continuous power dissipation (T_A = +25°C) (6) 3.12W
Maximum operating frequency 500kHz
Junction temperature ..... 150°C
Lead temperature ..... 260°C
Storage temperature ..... -55°C to +150°C

Recommended Operating Conditions (7)

Supply voltage (VDD) ..... 0V to 57V
VIN voltage ..... 7V to 35V
Maximum T2P sink current 5mA
Maximum AUX sink current ..... -3mA (3)
Maximum PG sink current 0.6mA (4)
Maximum EN/SYNC sink current 0.4mA (5)
Operating junction temp. (T_J) ..... -40°C to +125°C

Thermal Resistance (8)

	θ_{JA}	θ_{JC}	
QFN-28 (4mmx5mm)	40	9	°C/W

NOTES:

1) Exceeding these ratings may damage the device.
2) GND must be connected to RTN.
3) When VDD to the adapter ground voltage is high, the AUX-VDD voltage may exceed -6.5V if the resistor divider is not appropriate. In this condition, the current should be limited by an external resistor. Refer to the Wall Power Adaptor Detection and Operation section on page 17 for more detail.
4) If PG is pulled higher than 6.5V externally, the pull-up current should be limited. Refer to the Power Good (PG) Indicator Signal section in on page 18 for more detail.
5) Refer to the Enable/SYNC Control section on page 20.
6) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
7) The device is not guaranteed to function outside of its operating conditions.
8) Measured on JESD51-7, 2-layer PCB.

ELECTRICAL CHARACTERISTICS

VDD, CLASS, DET, T2P, and RTN voltages are referred to VSS. All other pin voltages are referred to GND. GND and RTN are shorted together. VDD - VSS = 48V, VSS = 0V, V_{IN} = 18V, R_{DET} = 24.9kΩ, R_{CLASS} = 28.7Ω. T_J = -40°C to +125°C. Typical values are tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
PD Interface Section						
Detection (DET)						
Detection on	V_{DET-ON}	V_{DD} rising		1.9		V
Detection off	$V_{DET-OFF}$	V_{DD} rising		11		V
DET leakage current	I_{DET-LK}	V_{DET} = V_{DD} = 57V, measure I_{DET}		0.1	5	µA
Bias current		V_{DD} = 10.1V, float DET, not in mark event, measure I_{SUPPLY}			12	µA
Detection current	I_{DET}	V_{DD} = 2.5V, measure I_{SUPPLY}	96	99	102	µA
		V_{DD} = 10.1V, measure I_{SUPPLY}	395	410	425	µA
Classification (CLASS)						
Classification stability time				90		µs
V_{CLASS} output voltage	V_{CLASS}	13V < V_{DD} < 21V, 1mA < I_{CLASS} < 42mA	1.1	1.16	1.21	V
Classification current	I_{CLASS}	13V ≤ V_{VDD} ≤ 21V, guaranteed by V_{CLASS}				
		R_{CLASS} = 578Ω, 13V ≤ V_{DD} ≤ 21V	1.8	2	2.4	mA
		R_{CLASS} = 110Ω, 13V ≤ V_{DD} ≤ 21V	9.9	10.55	11.3	
		R_{CLASS} = 62Ω, 13V ≤ V_{DD} ≤ 21V	17.7	18.7	19.8	
		R_{CLASS} = 41.2Ω, 13V ≤ V_{DD} ≤ 21V	26.6	28.15	29.7	
		R_{CLASS} = 28.7Ω, 13V ≤ V_{DD} ≤ 21V	38.2	40.4	42.6	
Classification lower threshold	V_{CL-ON}	Class regulator turns on, V_{DD} rising	11.8	12.5	13	V
Classification upper threshold	V_{CL-OFF}	Class regulator turns off, V_{DD} rising	21	22	23	V
Classification hysteresis	V_{CL-H}	Low-side hysteresis		0.8		V
		High-side hysteresis		0.5		
Mark event reset threshold	V_{MARK-L}		4.5	5	5.5	V
Max mark event voltage	V_{MARK-H}		11	11.5	12	V
Mark event current	I_{MARK}		0.5	1.5	2	mA
Mark event resistance	R_{MARK}	2-point measure at 7V and 10V			12	kΩ
IC supply current during classification	$I_{IN-CLASS}$	V_{DD} = 17.5V, CLASS floating		220	300	µA
Class leakage current	$I_{LEAKAGE}$	V_{CLASS} = 0 V, V_{DD} = 57V			1	µA
PD UVLO						
VDD turn-on threshold	$V_{DD-VSS-R}$	V_{DD} rising	32	34	36	V
VDD turn-off threshold	$V_{DD-VSS-F}$	V_{DD} falling	29	31	33	V
VDD UVLO hysteresis	$V_{DD-VSS-HYS}$		2.6			V
IC supply current during operation	I_{IN}			450		µA

ELECTRICAL CHARACTERISTICS *(continued)*

VDD, CLASS, DET, T2P, and RTN voltages are referred to VSS. All other pin voltages are referred to GND. GND and RTN are shorted together. VDD - VSS = 48V, VSS = 0V, V_{IN} = 18V, R_{DET} = 24.9kΩ, R_{CLASS} = 28.7Ω. T_J = -40°C to +125°C. Typical values are tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Pass Device and Current Limit						
On resistance	R_{ON-RTN}	I_{RTN} = 600mA		0.48		Ω
LEAKAGE CURRENT	I_{RTN-LK}	V_{DD} = V_{RTN} = 57V		1	15	MA
CURRENT LIMIT	I_{LIMIT}	V_{RTN} = 1V	720	840	920	MA
INRUSH CURRENT LIMIT	I_{INRUSH}	V_{RTN} = 2V		85		MA
INRUSH CURRENT TERMINATION		V_{RTN} FALLING		1.2		V
INRUSH TO OPERATION MODE DELAY	T_{DELAY}		80	100		MS
CURRENT FOLDBACK THRESHOLD		V_{RTN} RISING		10		V
FOLDBACK DEGLITCH TIME		V_{RTN} RISING TO INRUSH CURRENT FOLDBACK		1		MS
T2P						
T2P OUTPUT LOW VOLTAGE		I_{T2P} = 2MA, RESPECT TO VSS		0.1	0.3	V
T2P OUTPUT HIGH LEAKAGE CURRENT		V_{T2P} = 48V			1	MA
AUX						
AUX HIGH THRESHOLD VOLTAGE (9)		RESPECT TO VDD			-2.3	V
AUX LOW THRESHOLD VOLTAGE (9)		RESPECT TO VDD	-0.6			V
AUX LEAKAGE CURRENT		V_{DD} - V_{AUX} = 6V			2	MA
POWER GOOD (PG)						
PG OUTPUT HIGH VOLTAGE		PG FLOATING		5.5		V
SOURCE CURRENT CAPABILITY		PG IS LOGIC HIGH, PULL DOWN PG TO 0V		30		MA
PG PULL-DOWN RESISTANCE		PG IS LOGIC LOW, PULL UP PG TO 1V		1000		KΩ
PD THERMAL SHUTDOWN						
THERMAL SHUTDOWN TEMPERATURE (10)	T_{PD-SD}			150		°C
THERMAL SHUTDOWN HYSTERESIS (10)	T_{PD-HYS}			20		°C

ELECTRICAL CHARACTERISTICS *(continued)*

VDD, CLASS, DET, T2P, and RTN voltages are referred to VSS. All other pin voltages are referred to GND. GND and RTN are shorted together. VDD - VSS = 48V, VSS = 0V, V_{IN} = 18V, R_{DET} = 24.9kΩ, R_{CLASS} = 28.7Ω. T_J = -40°C to +125°C. Typical values are tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Flyback Controller Section						
Controller Input Supply Management						
VCC UVLO threshold	$V_{CC-UVLO}$	Rising edge	3.9	4.17	4.44	V
VCC UVLO hysteresis	V_{CC-HYS}			350		mV
VCC regulation voltage	V_{CC}	Load = 0mA to 10mA	10.8	11.8	12.8	V
Shutdown current	I_S	V_{EN} = 0V, test supply from VIN to GND			1	μA
Quiescent current	I_Q	V_{FB} = 1.35V, test supply from VIN to GND		0.4	0.6	mA
Gate Driving Signal						
Gate driver impedance (sourcing)		I_{GATE} = -20mA		4.1		Ω
Gate driver impedance (sinking)		I_{GATE} = 20mA		2		Ω
Error Amplifier (EA)						
Error amplifier transconductance	G_{EA}	V_{FB} is ±50mV from FB threshold, V_{COMP} = 1.5V		0.56		mA/V
Maximum amplifier output current		Sourcing and sinking		75		μA
COMP high voltage		I_{SENSE} = 0V, V_{FB} = 1V		2.4		V
		I_{SENSE} = 1V, floating COMP				
Current Sense (ISENSE)						
Current comparator leading edge blanking (11)	T_{LEB}			214		ns
ISENSE limit	V_{LIMIT}	T_J = 25°C	163	185	206	mV
SCP limit (10)	V_{SCP}			350		mV
Current sense amplifier gain		$\Delta V_{COMP}/\Delta V_{ISENSE}$		2.7		V/V
ISENSE bias current	I_{SENSE}	T_J = 25°C		0.01	0.15	μA
PWM						
V_{COMP} (skipping mode) (10)		Pulse skipping mode operation threshold, V_{COMP}		0.95		V
Switching frequency	F_{SW}	RT = 6.81kΩ	308	337	363	kHz
		RT = 80.6kΩ	25	30	35	kHz
Minimum on time	T_{ON}			214	400	ns
Maximum duty cycle	D_{MAX}	RT = 6.81kΩ	93	95		%

ELECTRICAL CHARACTERISTICS *(continued)*

VDD, CLASS, DET, T2P and RTN voltages are referred to VSS. All other pin voltages are referred to GND. GND and RTN are shorted together. VDD - VSS = 48V, VSS = 0V, V_{IN} = 18V, R_{DET} = 24.9kΩ, R_{CLASS} = 28.7Ω. T_J = -40°C to +125°C. Typical values are tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Soft Start (SS) (12)						
Charge current	I_{SS}			54		µA
Discharge current during protection				1.66		µA
Overload detection discharge current				17.8		µA
Charged threshold voltage				3.65		V
Overload shutdown threshold voltage				3.27		V
Protection reset threshold voltage				0.2		V
Voltage Feedback Management						
Mode detection voltage (10)				185		mV
Mode detection current (10)				55		µA
Mode detection time (10)				50		µs
FB reference voltage	V_{FB}	T_J = 25°C	1.222	1.237	1.252	V
		T_J = -40°C to 125°C	1.211	1.237	1.258	V
FB bias current	I_{FB}	V_{FB} = 1.237V, T_J = 25°C		0.01	0.15	µA
OVP reference level	V_{OVP}		1.391	1.438	1.479	V
COMP pull-up resistor				14.4		kΩ
COMP pull-up voltage (10)				3.6		V
Enable Control (EN/SYNC)						
Enable rising threshold	$V_{EN-RISING}$	T_J = 25°C	1.463	1.628	1.793	V
Enable hysteresis	V_{EN-HYS}			540		mV
Enable turn-off delay	T_{TD-OFF}			20		µs
Enable input current	I_{EN}	V_{EN} = 3V		2.5	5	µA
Thermal Protection						
Thermal shutdown (10)	T_{SD}			160		°C
Thermal hysteresis (10)	T_{SD-HYS}			20		°C

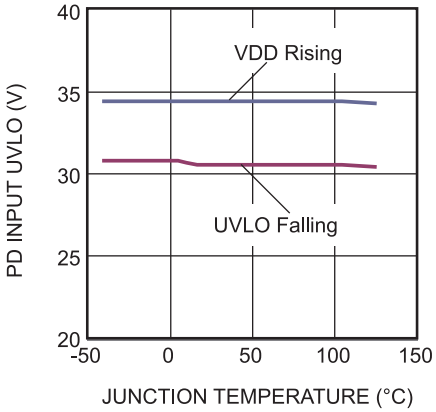
NOTES:

9) If VDD - AUX > 2.3V, the IC enables the adapter input. If VDD - AUX < 0.6V, the IC enables the PSE input. Refer to the Wall Power Adaptor Detection and Operation section on page 17 for AUX setting.
10) Guaranteed by characterization, not tested in production.
11) Same as the minimum on time.
12) Refer to the Soft Start (SS) section on page 19 for detail function of the discharge current and threshold voltage.

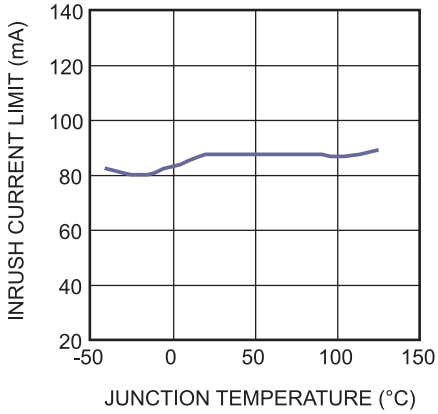
TYPICAL CHARACTERISTICS

V_{DD} - V_{SS} = 48V, V_{IN} = 18V, T_A = 25°C, unless otherwise noted.

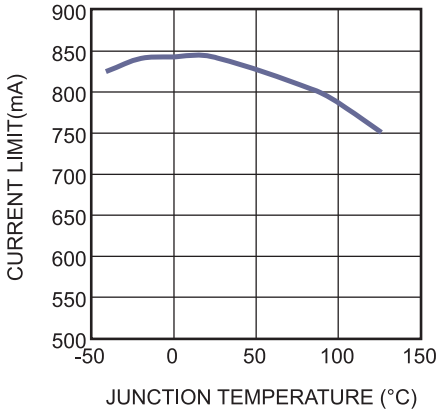
PD Input UVLO vs. Junction Temperature



PD Inrush Current Limit vs. Junction Temperature

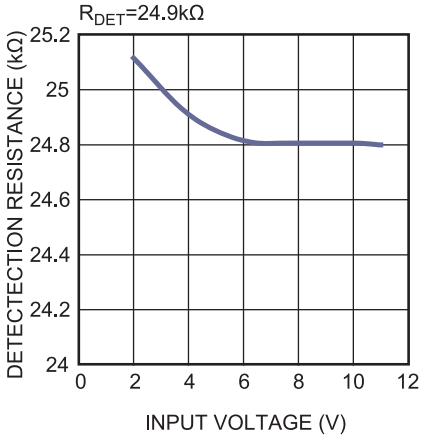


PD Current Limit vs. Junction Temperature

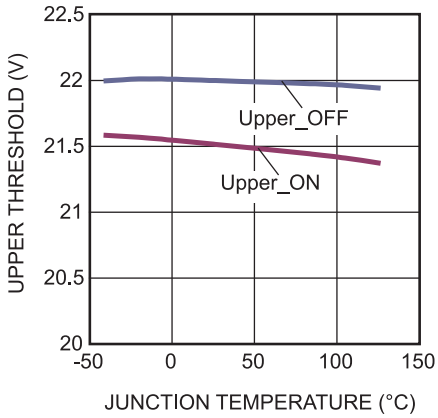


Detection Resistance vs. Input Voltage

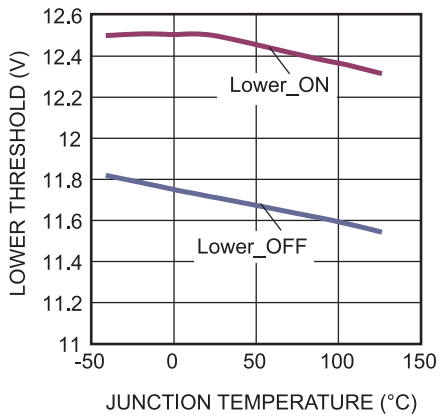
R_{DET}=24.9kΩ



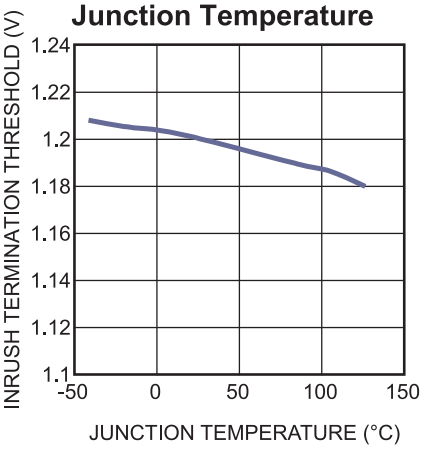
Class Upper Threshold vs. Junction Temperature



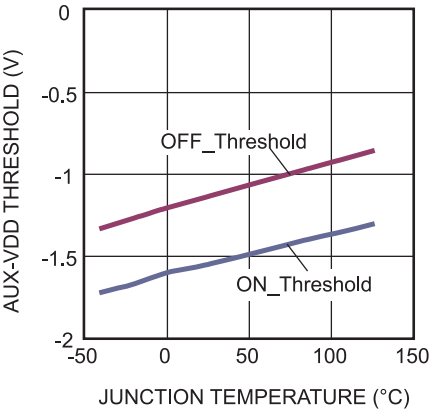
Class Lower Threshold vs. Junction Temperature



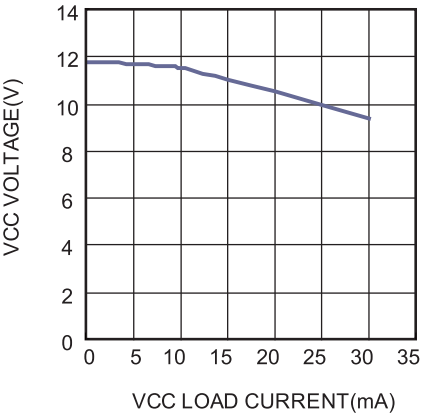
Inrush Current Termination Threshold vs. Junction Temperature



AUX-VDD Threshold vs. Junction Temperature



VCC Load Regulation

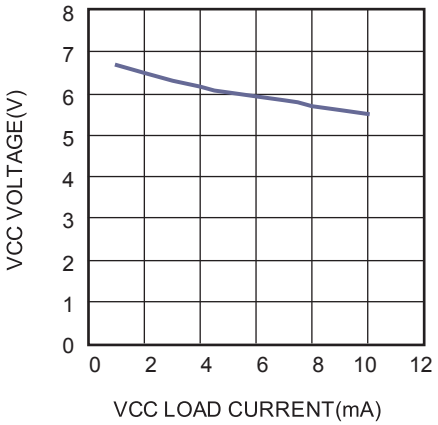


TYPICAL CHARACTERISTICS *(continued)*

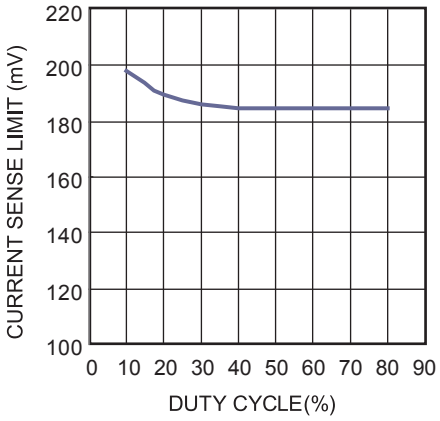
V_{DD} - V_{SS} = 48V, V_{IN} = 18V, T_A = 25°C, unless otherwise noted.

VCC Load Regulation

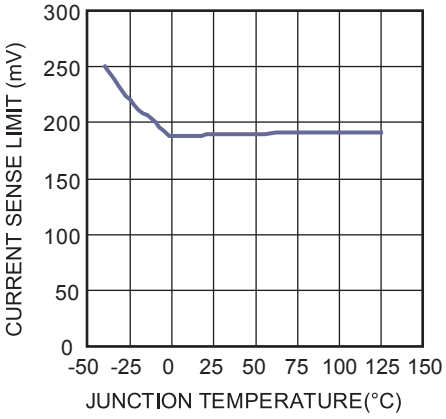
V_{IN}=7V



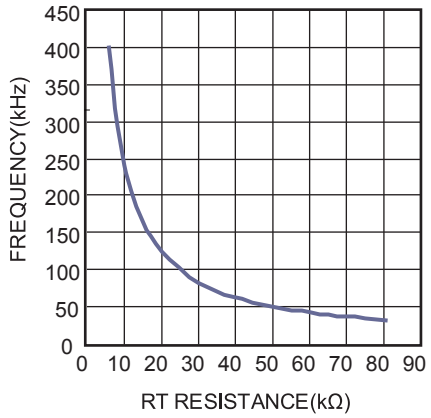
Flyback Controller Current Sense Limit vs. Duty Cycle



Flyback Controller Current Sense Limit vs. Junction Temperature

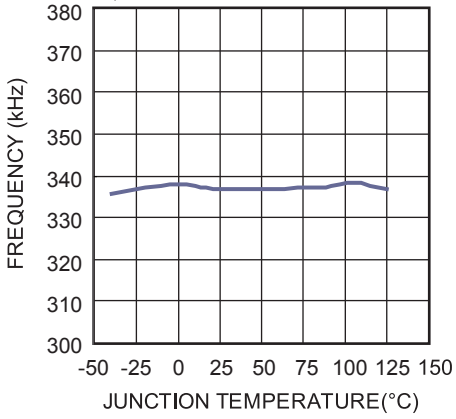


Frequency vs. RT Resistance



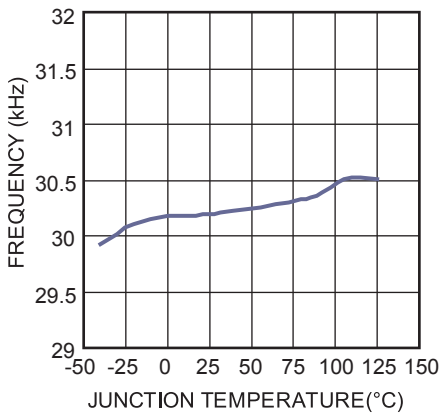
Frequency vs. Junction Temperature

R_T=6.81kΩ

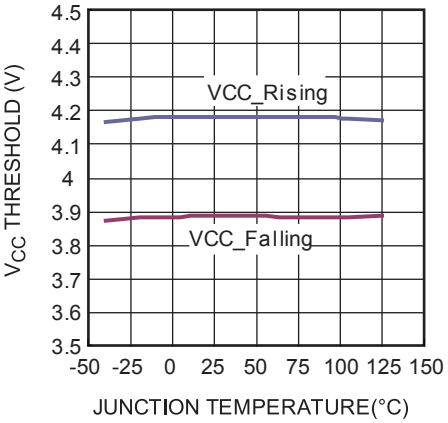


Frequency vs. Junction Temperature

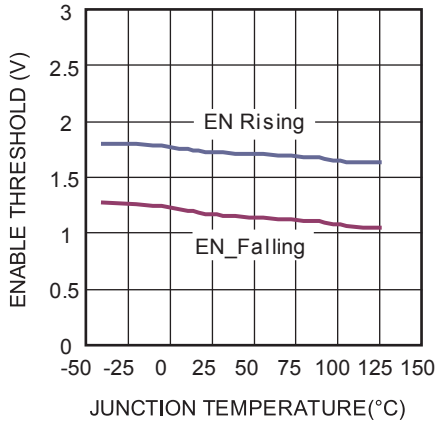
R_T=80.6kΩ



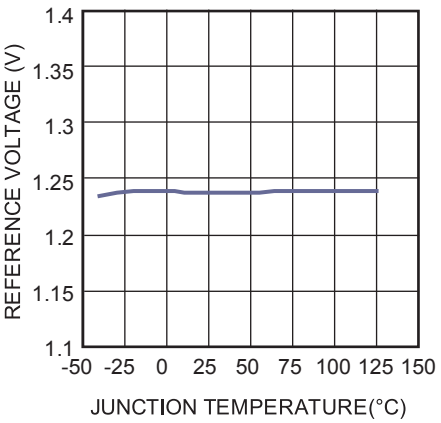
VCC UVLO vs. Junction Temperature



EN/SYNC UVLO vs. Junction Temperature



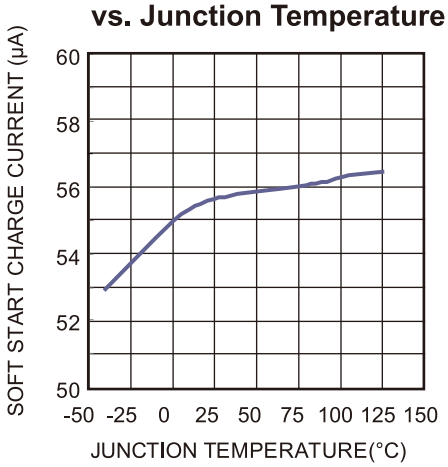
V_{REF} vs. Junction Temperature



TYPICAL CHARACTERISTICS *(continued)*

V_{DD} - V_{SS} = 48V, V_{IN} = 18V, T_A = 25°C, unless otherwise noted.

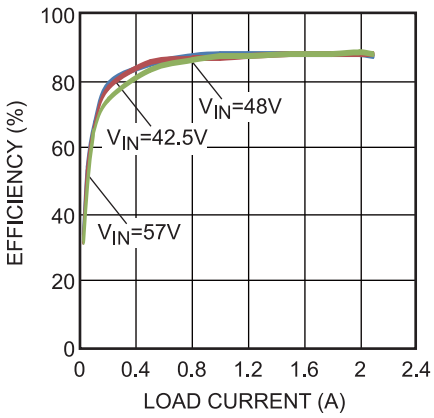
SS Charge Current vs. Junction Temperature



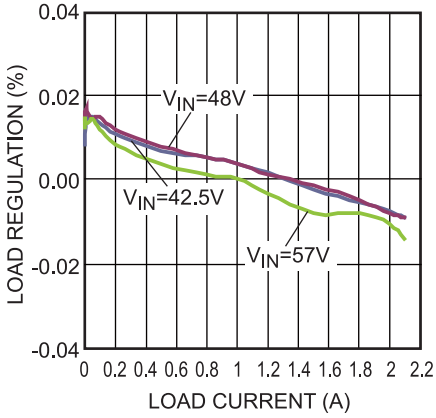
TYPICAL PERFORMANCE CHARACTERISTICS

V_{DD} - V_{SS} = 48V, V_{OUT} = 12V, I_{OUT} = 2.1A, T_A = 25°C, unless otherwise noted.

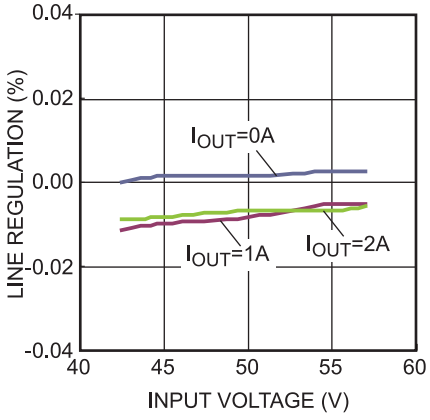
Efficiency



Load Regulation

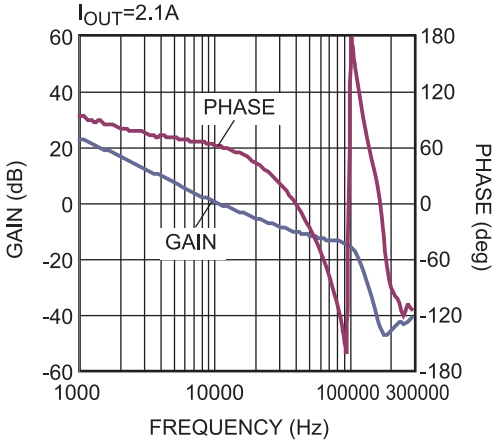


Line Regulation



Bode Plot vs. Frequency

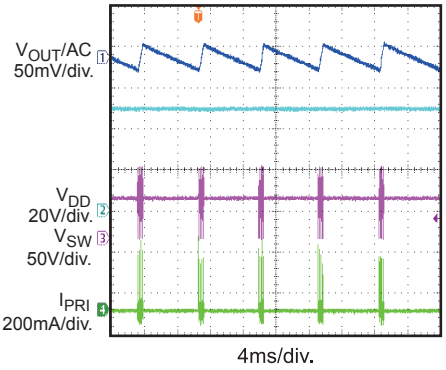
I_{OUT}=2.1A



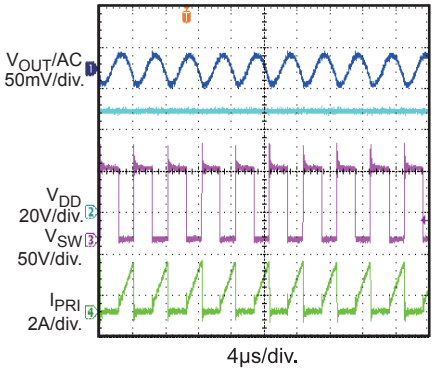
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{DD} - V_{SS} = 48V, V_{OUT} = 12V, I_{OUT} = 2.1A, T_A = 25°C, unless otherwise noted.

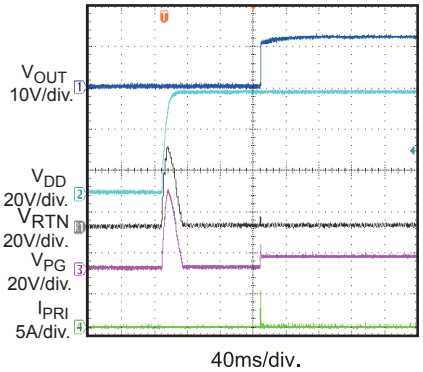
Steady State
I_{OUT} = 0A



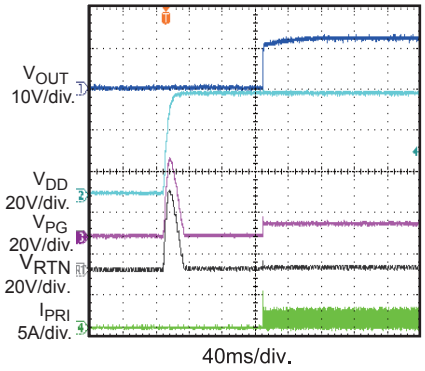
Steady State
I_{OUT} = 2.1A



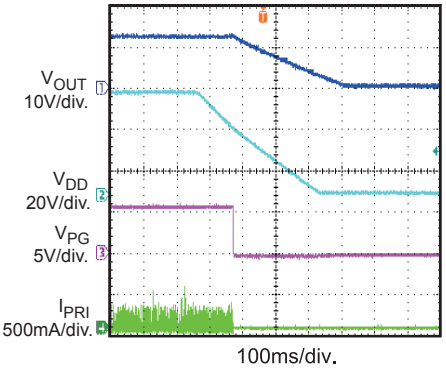
VDD Start-Up
I_{OUT} = 0A



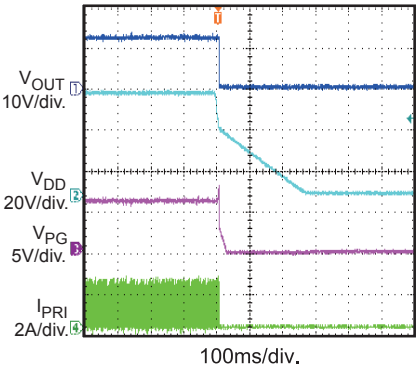
VDD Start-Up
I_{OUT} = 2.1A



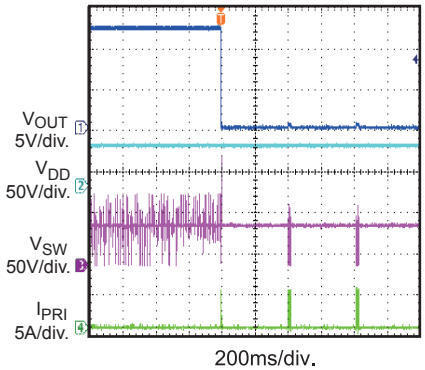
VDD Shutdown
I_{OUT} = 0A



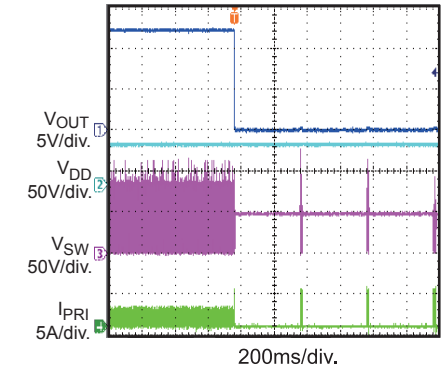
VDD Shutdown
I_{OUT} = 2.1A



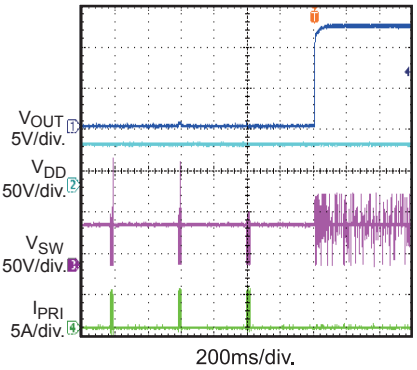
SCP Entry
I_{OUT} = 0A to Short



SCP Entry
I_{OUT} = 2.1A to Short



SCP Recovery
I_{OUT} = Short to 0A

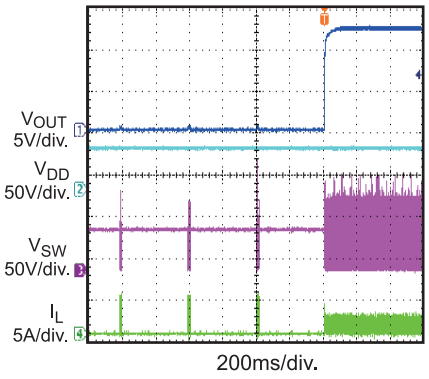


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{DD} - V_{SS}= 48V, V_{OUT} = 12V, I_{OUT} = 2.1A, T_A = 25°C, unless otherwise noted.

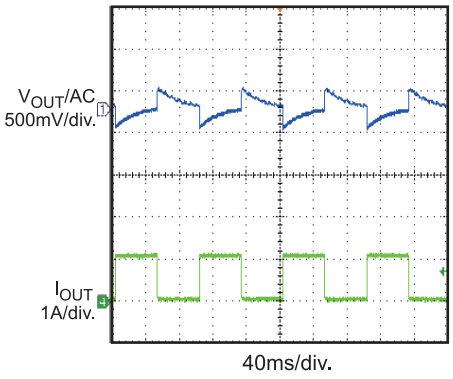
SCP Recovery

I_{OUT} = Short to 2.1A



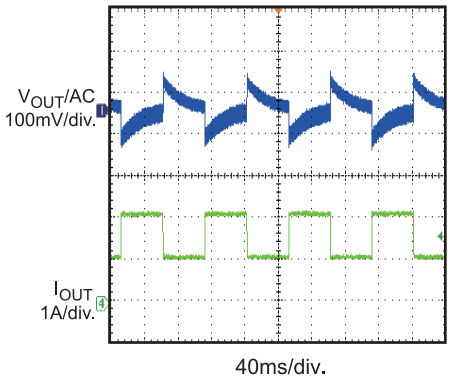
Load Transient

I_{OUT} = 0A to 1A, Iramp=25mA/µs



Load Transient

I_{OUT} = 1A to 2.1A, Iramp=25mA/µs



PIN FUNCTIONS

PIN#	Name	Description
1	AUX	**Auxiliary power input detector.** Use AUX for auxiliary power applications. Drive VDD - AUX above 2.3V to disable the hot-swap MOSFET and CLASS function and force T2P and PG active.
2	DET	**Detection.** Connect a 24.9kΩ resistor between VDD and DET for PoE detection.
3	VDD	**Positive power supply terminal from the PoE input power rail.**
4, 14 - 17, 22, 28	NC	**Not connected internally.** Connect NC to GND during layout.
5	PG	**PD supply power good indicator.** PG is pulled up by an internal current source when the PD output cap is fully charged. Connect PG to EN/SYNC for automatic flyback start-up.
6	GATE	**Gate driving signal.** GATE drives the external N-channel power MOSFET.
7	VCC	**Flyback controller for internal 12V regulator OUT pin.** VCC is powered through an internal LDO from VIN. Connect a capacitor between VCC and GND.
8	VIN	**Flyback controller input supply.** Connect a bypass capacitor from VIN to GND.
9	GND	**Power ground.** GND is a gate driver return.
10	RT	**Switching frequency set.** Connect a resistor from RT to GND to set the switching frequency (30kHz ~ 400kHz).
11	COMP	**Feedback for isolated flyback.** COMP is the error amplifier output for non-isolated solutions.
12	FB	**OVP monitor for isolated flyback.** FB is the feedback and OVP monitor for non-isolated solutions. Connect FB to GND if it is not being used in an isolated flyback.
13	EN/SYNC	**On/off control input.** Connect EN/SYNC to GND internally with a 1MΩ resistor. Apply an external clock higher than the RT-set frequency to EN/SYNC to synchronize the switching frequency.
18	SS	**Soft start.** Connect a capacitor between SS and GND to control the COMP voltage rising. SS determines both the soft-start time and hiccup protection delay.
19	ISENSE	**Current sense and application mode (isolated/non-isolated) setting.** During start-up, ISENSE outputs one current signal and senses the voltage for isolated or non-isolated mode setting detection. During normal operation, ISENSE senses the voltage across the sense resistor for current mode control, as well as cycle-by-cycle current limit, overload, and short-circuit protection.
20, 21	RTN	**Drain of PD hot-swap MOSFET.** Connect GND and the flyback power return to RTN.
23, 24	VSS	**Negative power supply terminal from PoE input power rail.**
25	FTY	**Factory use only.** FTY must be connected to VSS in application.
26	CLASS	**Classification.** Connect a resistor from CLASS to VSS to program the classification current.
27	T2P	**Type-2 PSE indicator.** T2P is an open-drain output. T2P pulled low to VSS indicates the presence of a Type-2 PSE or the presence of a wall adapter.

BLOCK DIAGRAM

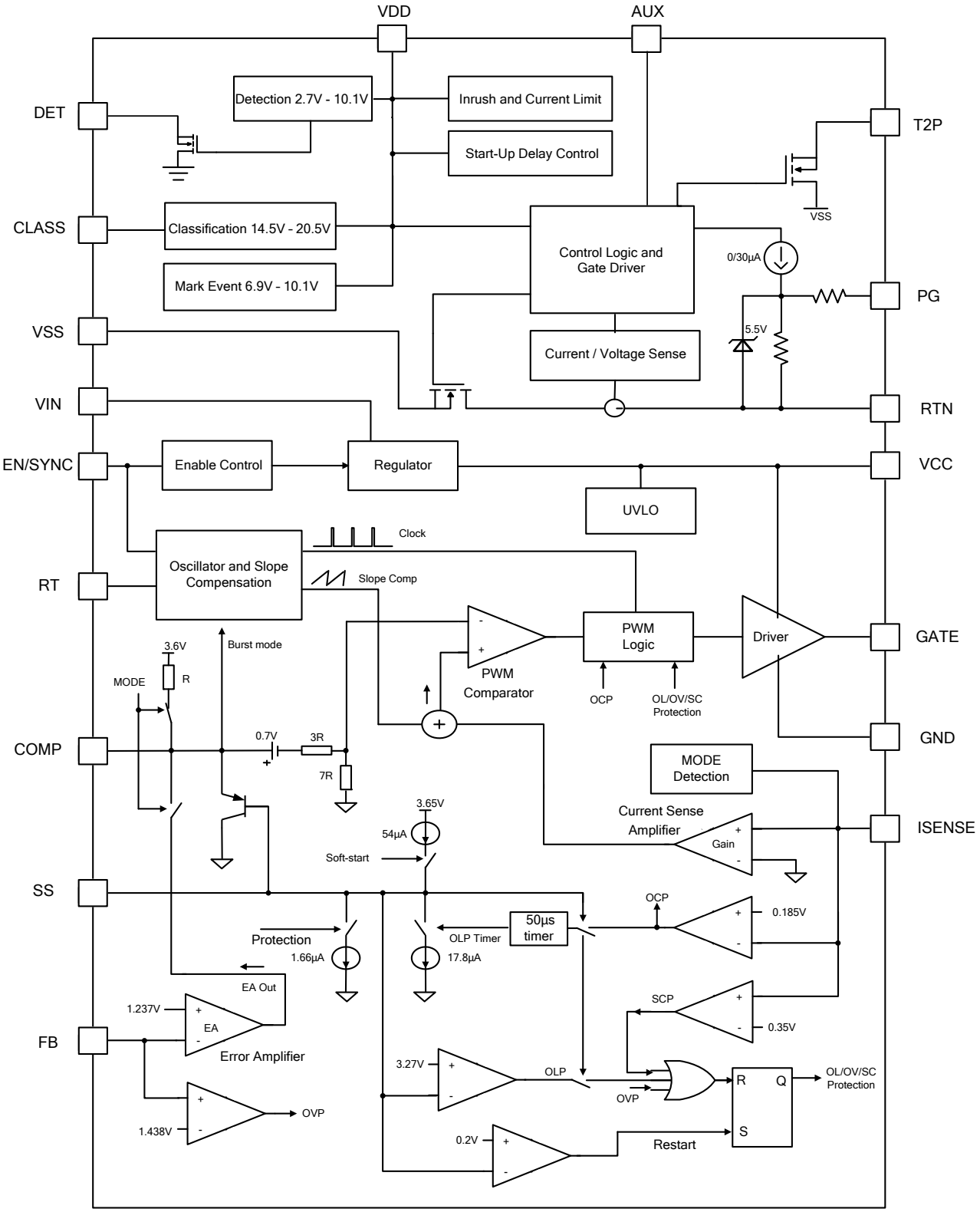


Figure 1: Functional Block Diagram

OPERATION

Compared with IEEE 802.3af, the IEEE 802.3at standard establishes a higher power allocation for Power over Ethernet (PoE) while maintaining backward compatibility with existing IEEE 802.3af systems. Power sourcing equipment (PSE) and power devices (PD) are distinguished as Type-1 (compliant with IEEE 802.3af power levels) or Type-2 (compliant with IEEE 802.3at power levels). The IEEE 802.3af/at standard establishes a method of communication between PD and PSE with detection, classification, and mark events.

The MP8008L is one integrated PoE solution with IEEE 802.3af/at PD interface and a peak-current-mode flyback controller. Along with the PSE, the MP8008L operates as a safety device to supply voltage only when the power sourcing equipment recognizes a unique and tightly specified resistance at the end of an unknown length of Ethernet cable. Once it is powered from the PSE, the MP8008L regulates the output voltage based on the application circuit setting. Figure 2 shows the typical PD interface power operation sequence.

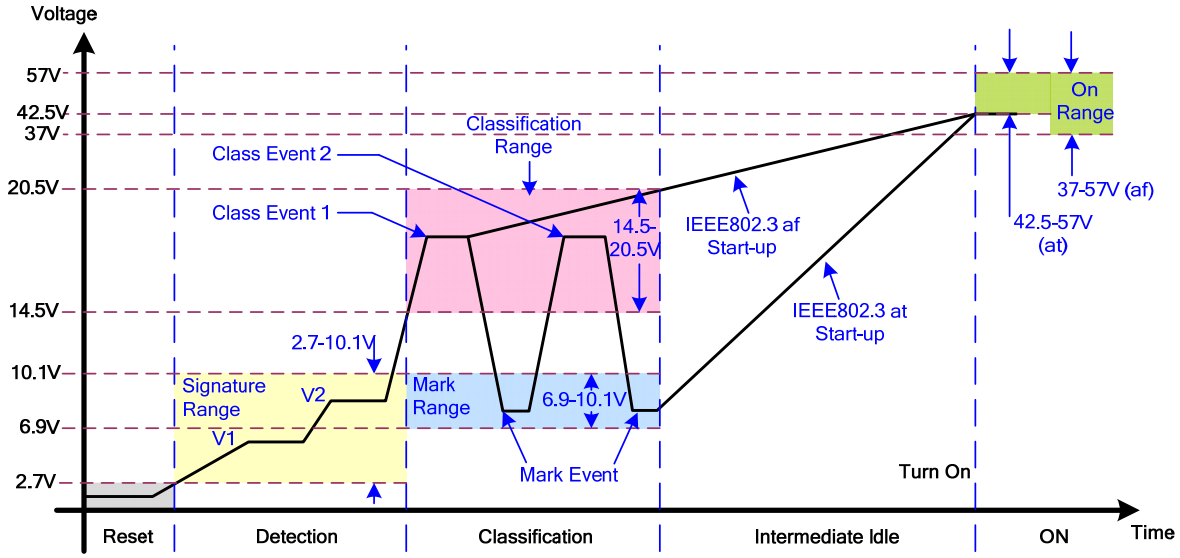


Figure 2: PD Interface Operation Description

Detection (DET)

R_{DET} connected between DET and VDD is presented as a load to the PSE in detection mode, where the PSE applies two "safe" voltages between 2.7V and 10.1V while measuring the change in current drawn to determine the load resistance. A 24.9kΩ (±1%) resistor between VDD and DET is recommended to present one correct signature. The valid signature resistance seen from the power interface (PI) is between 23.7kΩ and 26.3kΩ.

The detection resistance seen from the PI is the result of the input bridge resistance in series with VDD loading. The input bridge resistance is cancelled partially by the MP8008L's effective leakage resistance during detection.

Classification (CLASS)

Classification mode can specify the expected load range of the device under power to the PSE so that the PSE can distribute power intelligently to as many loads as possible within its maximum current capability. The classification mode is active between 14.5V and 20.5V. The MP8008L presents a current in classification mode (see Table 1).

Table 1: CLASS Resistor Selection

Class	Max Input Power to PD (W)	Classification Current (mA)	R_{CLASS} (Ω)
0	12.95	2	578
1	3.84	10.55	110
2	6.49	18.7	62
3	12.95	28.15	41.2
4	25.5	40.4	28.7

2-Event Classification

The MP8008L can be used as a Type-1 PD class 0-3 (as shown in Table 1). It also distinguishes class 4 with 2-event classification.

In 2-event classification, the Type-2 PSE reads the power classification twice. Figure 2 shows an example of a 2-event classification. The first classification event occurs when the PSE presents a voltage between 14.5V to 20.5V to the MP8008L, and the MP8008L presents a class-4 load current. The PSE then drops the input voltage into the mark voltage range of 6.9V to 10.1V, signaling the first mark event. The MP8008L presents a load current between 0.5mA to 2mA in the mark event voltage range.

The PSE repeats this sequence, signaling the second classification and second mark event. The PSE then applies power to the MP8008L, which charges up the DC/DC input capacitor (C_{BULK}, C1 in the schematic on page 1) with a controlled inrush current. When C_{BULK} is fully charged, T2P presents an active-low signal with respect to VSS after T_{DELAY}. The T2P output becomes inactive when the MP8008L input voltage (VDD) falls below the under-voltage lockout (UVLO) (see Figure 3).

PD Interface UVLO and Current Limit

When PD is powered by PSE and VDD is higher than the turn-on threshold, the hot-swap switch begins passing a limited current (I_{INRUSH}) to charge the downstream DC/DC converter's input capacitor (C_{BULK}). The start-up charging current is around 85mA.

If RTN drops below 1.2V, the hot-swap current limit changes to 840mA. After T_{DELAY} from the UVLO begins, the MP8008L asserts the PG signal and switches from start-up mode to running mode. If PG is connected to EN/SYNC, the PG signal rises high only after the hot-swap switch turns on completely, so PG enables the flyback through EN/SYNC. If VDD - VSS drops below the falling UVLO, the hot-swap MOSFET is disabled.

If the output current overloads on the internal pass MOSFET, the current limit works, and V_{RTN} - V_{SS} rises. If V_{RTN} rises above 10V for longer than 1ms or rises above 20V, the current limit reverts to the inrush value, and PG drops low at the same time.

Figure 3 shows the current limit and the PG and T2P work logic during start-up from the PSE power supply.

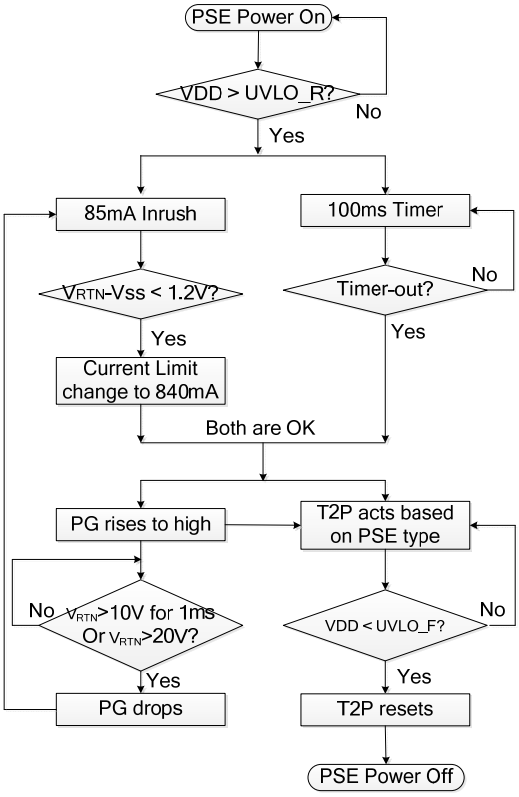


Figure 3: Start-Up Sequence

Wall Power Adaptor Detection and Operation

The MP8008L uses wall power adapter detection for applications where an auxiliary power source, such as a wall adapter, is used to power the device (see Figure 4). Once the input voltage (VDD - VSS) exceeds about 11.5V, the MP8008L enables wall adapter detection. The wall power adapter detection resistor divider is connected from VDD to the negative terminal of the adapter, and D_{ADP3} is added for a more accurate hysteresis. There is a -2.3V reference voltage from AUX to VDD for adapter detection. The adapter is detected when the AUX voltage triggers, as shown in Equation (1):

$$V_{DD} - V_{AUX} = (V_{ADP} - V_{DADP3}) \times \frac{R_{ADPUP}}{R_{ADPUP} + R_{ADPDOWN}} > 2.3V \quad (1)$$

Where V_{ADP} is the adapter voltage, V_{DADP3} is the Zener voltage, and R_{ADPUP} and $R_{ADPDOWN}$ are the AUX divider resistors from the adapter power.

If the applied adapter voltage is much higher than the design adapter voltage, the VDD - V_{AUX} voltage is high. If the applied voltage between VDD and AUX is higher than 6.5V, some current may flow out through AUX. Design the external resistor (R_{ADPUP}/$R_{ADPDOWN}$ or RT resistor from the resistor divider to AUX) to limit the AUX current. By assuming the VDD - AUX voltage is 6.5V for the calculation, the current out of AUX should be lower than 3mA via the external resistor limit.

To make the MP8008L work stably with adapter power, one Schottky diode (D_{APD1}, D4 on the schematic on page 1) is required between the negative terminal of the adapter and VSS. D_{APD2} (D5 on the schematic on page 1) is used to block reverse current between the adapter and PSE power source. When a wall adapter is detected, the internal MOSFET between RTN and VSS turns off, classification current is disabled, and T2P becomes active. The PG signal is active when the adapter power is detected, so that it can enable the downstream DC/DC converter, even if the input hot-swap MOSFET is disabled.

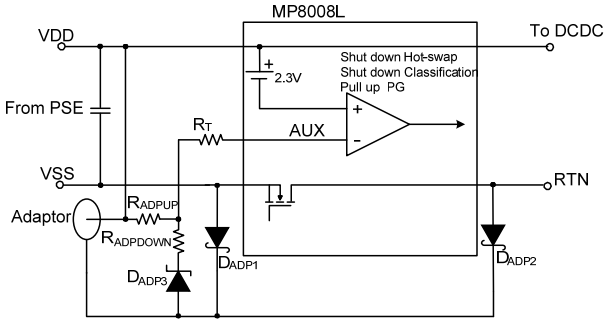


Figure 4: Adaptor Power Detection

Power Good (PG) Indicator

The PG signal is driven by the internal current source. After T_{DELAY} from the UVLO starts and RTN drops to 1.2V or a wall power adapter is detected, the PG signal is pulled high to indicate the power condition. Figure 3 shows the PG logic when powered from PSE. PG is high if the adapter is detected in any condition. Connect PG to EN/SYNC to set automatic start-up mode after power is applied.

Flyback Controller Operation

The MP8008L integrates a flyback controller, which uses a programmable frequency and peak-current-mode architecture to regulate the output voltage.

At the beginning of each cycle, the external N-channel MOSFET is turned on, forcing the current in the transformer to increase. The current through the MOSFET can be sensed. When the sum voltage of the amplified ISENSE signal and slope signal rises above the voltage set by COMP, the external MOSFET is turned off. The transformer current flows from the primary side to the secondary side, and then flows to the output capacitor through the output Schottky diode. The transformer current is controlled by the COMP voltage (V_{COMP}), which itself is controlled by the output voltage. Therefore, the output voltage controls the transformer current to satisfy the load. This current mode architecture improves transient response and control loop stability.

Pulse-Skip Mode (PSM)

In light-load conditions, the MP8008L goes into pulse-skip mode (PSM) to improve light-load efficiency. The pulse-skipping decision is based on the internal COMP voltage (VCOMP). If COMP is lower than the internal sleep threshold with a typical 0.95V value, a pause command is generated to block the turn-on clock pulse, so the power MOSFET is turned off immediately, saving gate driving and switching losses. This pause command also puts the entire chip into sleep mode, which consumes very low quiescent current to improve light-load efficiency further. The gate driver output remains low until VCOMP is higher than the sleep threshold, and then the pause signal is reset so the chip resumes normal pulse-width modulation (PWM) operation.

Internal VCC Regulator

VIN works with a 7 ~ 35V supply voltage. An internal regulator is applied to regulate the power at VCC to supply the internal circuitry of the controller and the gate driver. The regulator has a nominal output voltage of 12V at VCC and must be bypassed with a capacitor no less than 1μF.

When EN/SYNC is high, the capacitor at VCC is charged through VIN. VCC has its own UVLO protection. This UVLO's rising threshold is 4.17V with a hysteresis of 350mV.

When the voltage at VCC crosses the VCC UVLO, flyback is enabled, and all internal circuitry is powered by VCC. As the capacitor is charged, VCC increases until it reaches the 12V regulated voltage if VIN is sufficiently high.

When VIN is below 12V, VCC is lower than VIN due to an LDO drop. For normal operation, VIN should be higher than 7V. If VCC and VIN are connected together, the MP8008L's flyback converter can start up, even if VIN is 5V, but the max VCC value should be no higher than 13V. If both VIN and VCC are powered by an external source, VCC cannot be higher than VIN since there is one body diode from VCC to VIN.

Feedback Loop Setting

The MP8008L can feed back the output signal through either FB or COMP by a different setting on ISENSE.

For isolated flyback, the feedback signal from the optocoupler is amplified by the secondary circuitry. Connect the signal to COMP directly to make loop compensation easier by eliminating the primary-side amplifier. For non-isolated flyback, the MP8008L integrates one error amplifier, which can amplify the output error signal from FB. COMP needs one R-C network for compensation.

The different feedback loops can be set by different ISENSE connections. When the part is enabled, ISENSE outputs a 50μs current pulse with a typical 55μA value (see Figure 5). If the reflected voltage on ISENSE is higher than 185mV, the MP8008L disables the internal error amplifier between FB and COMP and pulls COMP up to a 3.6V source with a 14.4kΩ resistor. The feedback signal can be connected to COMP directly. If the detection voltage is lower than 185mV, the MP8008L enables the internal error amplifier and turns off the pull-up resistor. Then COMP is just one output pin of the error amplifier, and the feedback signal should be connected to FB.

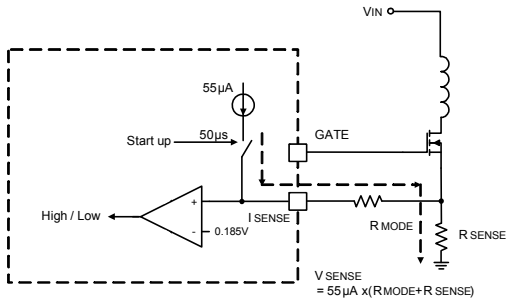


Figure 5: Feedback Mode Setting

Generally, it is recommended to place one 5 ~ 10kΩ resistor between ISENSE and the current sense resistor for feedback mode through COMP, and connect ISENSE to the current sense resistor directly for feedback mode through FB.

Soft Start (SS)

The MP8008L uses one external capacitor on SS to control V_{COMP} rising for a soft start. When the chip starts up, the capacitor on SS is charged by a 54μA current source at a slow pace set by the capacitance. When the SS voltage is lower than the external V_{COMP}, SS overrides the COMP signal, so the PWM comparator uses SS instead of COMP as the PWM turn-off reference. When SS is higher than V_{COMP}, COMP regains control, and the soft start finishes. Soft start can reduce voltage stresses and surge currents during start-up and prevent the converter output voltage from overshooting during start-up. Soft start occurs during the start-up time and protection recovery time after overload protection (OLP), short-circuit protection (SCP), and over-voltage protection (OVP). During normal condition, the SS voltage is clamped at 3.65V.

Programmable Oscillator

The MP8008L oscillating frequency is set by an external resistor from RT to ground. The value of RT can be estimated with Equation (2):

$$R_T = \frac{2.35 \times 10^3}{f_{SW}} \quad (2)$$

Where R_T is in kΩ, and f_{SW} is in kHz.

The frequency setting resistor value should not be too large when considering noise immunity. It is recommended to set the frequency within 30 - 400kHz.

Enable/SYNC Control

EN/SYNC is a digital control pin that turns the MP8008L flyback controller on and off. Drive EN/SYNC high to turn on the controller. Drive ENSYNC low to turn off the controller. An internal 1MΩ resistor from EN/SYNC to GND allows EN/SYNC to be floated to shut down the chip.

For external clock synchronization, connect a clock with a frequency higher than RT to set the frequency between 80 - 400kHz. The internal clock rising edge synchronizes with the external clock rising edge. Select an external clock pulse signal with a low-level width less than 10μs; otherwise, the MP8008L may treat this function as an EN/SYNC power off.

EN/SYNC and PG should be connected together so that the flyback controller starts up automatically once the PD enters an operation mode. If EN/SYNC is pulled high by an external power, then the EN/SYNC pull-up current should be limited to less than 0.4mA.

Current Sense and Over-Current Protection (OCP)

The current through the external MOSFET can be sensed through a sensing resistor used in series with the source terminal of the MOSFET. The sensed voltage on ISENSE is amplified and fed to the high-speed current comparator for current-mode control purposes. The current comparator takes this sensed voltage (pulse-slope compensation) as one of its inputs and compares the power switch current with V_{COMP}. When the amplified current signal is higher than V_{COMP}, the comparator output is low and turns off the power MOSFET.

If the voltage on ISENSE exceeds the current-limit threshold voltage with a typical value of 185mV, the PWM controller turns off the GATE output for that cycle until the internal oscillator starts the next cycle, and the current is sensed again. The MP8008L limits the current of the MOSFET cycle-by-cycle.

Overload Protection (OLP)

The peak current is limited cycle-by-cycle. If the load continues increasing after triggering over-current protection (OCP), the output voltage decreases, and the peak current triggers OCP during every cycle. The MP8008L sets the overload detection by monitoring the ISENSE voltage continuously.

Once the SS voltage is charged to 3.65V after start-up, OLP is enabled. If an OCP signal is detected, the soft-start charging current is disabled, and an over-current discharge source is enabled. The SS voltage drops with the rate of 17.8μA. At the same time, a 50μs one-shot timer is activated and remains active for 50μs after the OCP condition ends. The 17.8μA discharge source cannot be turned off until the one-shot timer becomes inactive. If the OCP condition is removed before at least 50μs prior to the SS capacitor discharging to 3.27V, the MP8008L resumes normal working condition, and the SS capacitor is re-charged to 3.65V with a 54μA rate.

If the SS capacitor is discharged to 3.27V, the MP8008L registers this as an overload condition and turns off the gate output until the next restart cycle. At the same time, the 17.8μA discharge current is disabled, and the 1.66μA overload discharge source is enabled. After the SS voltage is discharged to 0.2V, the PWM controller starts up again with a new soft-start cycle. This is called hiccup mode protection.

The OLP detection function is disabled after the SS voltage is discharged below 3.27V and is re-enabled after the SS voltage is recharged to 3.65V. OLP only occurs after the soft-start is completed.

Short-Circuit Protection (SCP)

When the output is shorted to ground, the MP8008L works in OCP mode, and the current is limited cycle-by-cycle. The MP8008L may run into OLP.

If the peak current cannot be limited by the 185mV ISENSE voltage every cycle due to the leading edge blanking (LEB) time, the current may run out of control, and the transformer may run into saturation. If the voltage on ISENSE reaches 0.35V, the MP8008L pulls GATE down and enters hiccup mode immediately by discharging the SS capacitor with a 1.66μA current. The MP8008L restarts if the SS voltage is discharged to 0.2V. If a short condition is still detected, the MP8008L enters SCP again immediately without having to wait for SS to

charge completely. This prevents damage during the soft start-up period. Once the short circuit is removed, the output voltage recovers only after the next restart cycle.

Over-Voltage Protection (OVP)

For isolated flyback application, the positive plateau of the auxiliary winding voltage is proportional to the output voltage. The MP8008L features OVP by using the auxiliary winding voltage instead of monitoring the output voltage directly. The auxiliary voltage can be monitored by FB through a resistor divider. Once the voltage is higher than the OVP reference voltage, the MP8008L turns off GATE and discharges the SS voltage with 1.66μA of current until the SS voltage is lower than 0.2V. The MP8008L then enters a new restart cycle.

If OVP is still detected, the MP8008L runs into OVP again without waiting for SS to charge completely. To prevent a mistrigger due to the oscillation of the leakage inductance and the parasitic capacitance, OVP sampling has an OVP blanking time (typically 500ns). For some oscillation conditions, an external filter is necessary to work with the 500ns LEB time.

For non-isolated solutions, the DC output voltage is applied to FB and can detect the OVP condition easily.

Thermal Shutdown

Thermal shutdown is implemented to prevent the chip from running away thermally. The MP8008L has a separated temperature monitor circuit for PD and flyback controllers. The flyback's thermal protection does not affect the PD interface, but the PD temperature protection turns off both the PD and flyback controller if EN/SYNC is connected to the PG signal. When the temperature is below its recovery threshold, thermal shutdown is removed, and the MP8008L is enabled.

APPLICATION INFORMATION

Detection Resistor

In detection mode, a resistor connected between DET and VDD is needed as a load to the PSE. The resistance is calculated as $\Delta V/\Delta I$, with an acceptable range of 23.7 - 26.3kΩ. Use a typical value of 24.9kΩ for the detection resistor.

Classification Resistor

To distribute power to as many loads as possible from PSE, a resistor between CLASS and VSS is used to classify the PD power level, which draws a fixed current set by the classification resistor. The supplied power to PD set by the classification resistor is shown in Table 1. The typical voltage on CLASS is 1.16V in the classification range and produces about 47mW power loss on the class resistor, even in a class 4 condition.

Protection TVS

To limit the input transient voltage within the absolute maximum ratings, a TVS across the rectified voltage (VDD - VSS) must be used. A SMAJ58A TVS or equivalent is recommended for general indoor applications. Outdoor transient levels or special applications require additional protection.

PD Input Capacitor

An input bypass capacitor of 0.05 - 0.12μF from VDD to VSS is needed for IEEE 802.3at/af standard specifications. Typically, a 0.1μF, 100V, ceramic capacitor is used.

Wall Power Adaptor Detection Circuit

When an auxiliary power source, such as a wall power adapter, is used to power the device, the resistor dividers R_{ADPUP}, $R_{ADPDOWN}$, and D_{ADP3} should be chosen to satisfy Equation (1) for correct wall power adaptor detection (see Figure 6).

R_{ADPUP} with a typical 3kΩ value is recommended to balance the power loss and D_{ADP1} and D_{ADP2} leakage current discharge.

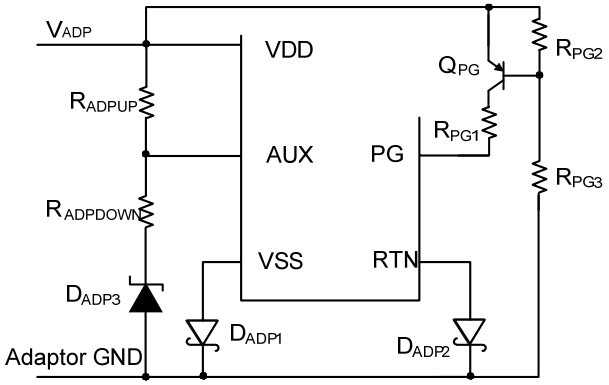


Figure 6: Wall Adaptor Detection Circuit

One small Schottky diode with a 100V voltage, such as BAT46W, is usually recommended for D_{ADP1}. The voltage rating of D_{ADP2} must also be 100V or higher, while the current rating must be higher than load current. A low voltage drop Schottky diode, such as STPS2H100, is recommended to reduce conduction power loss.

The MP8008L enables wall adapter detection at VDD = 11.5V. If an adapter power with a lower voltage rating (i.e.: 10V) is used to power the converter, an external PG pull-up resistor is necessary to enable the downstream DC/DC converter. Refer to Figure 6 and the following Power Good (PG) section for more detail.

Power Good (PG) Indicator Signal

The MP8008L integrates a power good (PG) indicator. PG is pulled high through an internal pull-up current source when the logic is high, so PG can connect with EN/SYNC to enable the flyback portion without any external pull-up circuit. PG disables the internal pull-up current, and PG is pulled low through an internal resistor when PG is in a logic low state.

If an adapter power lower than 11.5V is connected to supply the converter, the PG function is unable to work with such a low input. An external PG pull-up circuit is recommended (see Figure 6). Typically, Q_{PG} needs a V_{CE} voltage higher than 100V (i.e.: BSS63LT1). Choose R_{PG2} = 7.5kΩ and R_{PG3} = 100kΩ for a 12V adapter with some margin of adapter regulation. Choose R_{PG1} = 100kΩ to limit the PG sink current below 0.6mA when VDD is high.

T2P Indicator Connection

T2P is an active-low, open-drain output that indicates the presence of a Type-2 PSE or the presence of a wall adapter. An optocoupler is usually used as the interface from T2P to the circuitry on the output of the converter (see Figure 7). A high-gain optocoupler and a high-impedance receiver are recommended (i.e.: CMOS).

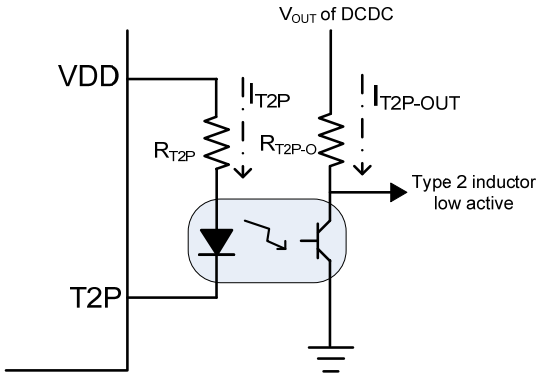


Figure 7: T2P Indicator Circuit

Considering the T2P sinking current (typically 2mA), the T2P output-low voltage (0.1V), and the diode forward voltage drop, choose R_{T2P} = 23.7kΩ to match the typical 48V input. Supposing V_{OUT} of the DC/DC part is 12V, choose R_{T2P-O} = 20kΩ based on the CRT, even if it varies with temperature, LED bias current, and aging.

If using an LED from VDD to T2P to indicate if Type-2 PSE is available, R_{T2P}'s resistance can be higher to match the LED's max current and reduce power loss.

Flyback Controller Power Supply Setting

VIN supports up to 35V of input voltage. For a typical PoE application, one external voltage regulator circuit is needed to clamp the 48V PoE input. After the flyback starts, VIN can be powered from the transformer auxiliary winding to save external high-voltage regulator power loss.

Output Voltage Setting

When the MP8008L works in isolated flyback mode, the output voltage cannot be set by FB. An additional external shunt regulator (i.e.: TL431) can be used to set V_{OUT}. Supposing that this regulator's reference voltage is 2.5V, and the expected output voltage is 12V, then the upper and lower resistor divider ratio is 3.8, the lower resistor is 49.9kΩ, and the upper resistor is 191kΩ. Typically, the upper resistor should be lower than 500kΩ to avoid noise injection.

Then TL431 generates an amplified signal, which is transferred to the MP8008L through an optocoupler (i.e.: PC817). Then V_{OUT} is regulated based on the feedback signal.

Selecting the Soft-Start Capacitor

The MP8008L ramps the external capacitor voltage on SS to control V_{COMP}, which determines the transformer primary-side peak current, resulting in a lower inrush current. The SS voltage can be calculated by Equation (3):

$$Vss = \frac{54\mu A}{C_{ss}} \times T_{ss} \quad (3)$$

More importantly, SS acts as a hiccup timer when OLP, SCP, or OVP occurs. Once protection occurs, a 1.66μA current discharges the SS capacitor for hiccup protection. Normally, a 0.22μF SS capacitor is sufficient for most applications.

Selecting the Input Capacitor

A DC/DC controller input capacitor is required to supply AC ripple current to the transformer while limiting noise at the input source. This controller acts as a voltage bulk between the PD and DC/DC converter. A large capacitance leads to longer PD charge time and higher cost. A lower capacitance leads to higher input voltage ripple and higher input current ripple. Typically, a 47 ~ 100μF electrolytic capacitor is recommended in parallel with a high-quality ceramic capacitor. The input voltage ripple can be estimated with Equation (4):

$$\Delta V_{IN} = I_{IN} \times \frac{V_{IN}}{F_{SW} \times C_{IN} \times (N \times V_{OUT} + V_{IN})} \quad (4)$$

Where ΔV_{IN} is the input voltage ripple, I_{IN} is the input current, F_{SW} is switching frequency, C_{IN} is the input capacitance, and N is the transformer ratio.

Selecting the Output Capacitor

The output capacitor maintains the DC output voltage and also affects system stability. For best results, use low ESR capacitors to minimize the output voltage ripple. Electrolytic capacitors are also sufficient, but must be used in parallel with a high-quality ceramic capacitor to filter high-frequency noise.

If the voltage ripple is too high, a π filter is needed. Choose the inductor to be between 0.1 ~ 0.47μH to achieve good V_{OUT} ripple and system stability.

Selecting the Transformer and ISENSE Resistor

A transformer is important in a flyback converter since it determines the duty cycle, peak current, efficiency, MOSFET, output diode rating, and so on. A good transformer should consider the winding ratio, primary-side inductance, saturation current, leakage inductance, current rating, and core selection.

The transformer winding ratio is very important since it determines the duty cycle. Calculate the duty with Equation (5):

$$D = \frac{NV_{OUT}}{NV_{OUT} + V_{IN}} \quad (5)$$

Where N is the transformer winding ratio, and D is the duty cycle. Typically, a max duty cycle of about 45% is recommended for most applications.

The primary-side inductance affects the input current ripple ratio factor. A high inductance results in a large transformer size and high cost. A low inductance results in high switching peak current and RMS current, which cause a decrease in efficiency. Choose a primary-side inductance to make the current ripple ratio factor around 30 ~ 50%. Estimate the primary-side inductance with Equation (6):

$$L_P = \frac{V_{IN} \times D^2}{2 \times n \times I_{IN} \times F_{SW}} \quad (6)$$

Where n is the current ripple ratio, I_{IN} is the input current, and L_P is the primary inductance. Calculate L_P based on the minimum input voltage condition.

The transformer should have a high saturation current to support the switching peak current; otherwise, the transformer inductance decreases sharply. The ISENSE resistor can be used to limit the switching peak current.

The energy stored in the leakage inductance cannot couple to the secondary side, causing a high spike when the MOSFET turns off. This decreases efficiency and increases MOSFET stress. Normally, the transformer leakage inductance can be controlled below 3% of the transformer inductance.

The current rating counts the max RMS current, which allows flow through each winding. The current density should be controlled; otherwise, it can cause a high resistive power loss.

After the transformer is chosen, determine the peak current. To avoid reaching the current limit, the voltage across the sensing resistor (R_{SENSE}) should be less than 80% of the worst-case current limit voltage (185mV). Calculate R_{SENSE} with Equation (7):

$$R_{SENSE} = \frac{0.8 \times 0.185}{I_{PEAK}} \quad (7)$$

RCD Snubber

The transformer leakage inductance causes spikes and excessive ringing on the MOSFET drain voltage waveform, and the RCD snubber circuit limits the MOSFET voltage spike (see Figure 8).

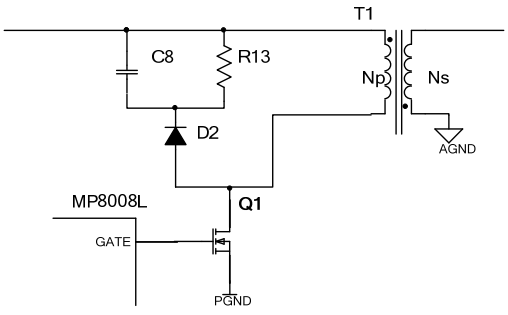


Figure 8: RCD Snubber

The power dissipation in the snubber circuit can be estimated with Equation (8):

$$P_{SN} = \frac{1}{2} \times L_K \times {I_{PEAK}}^2 \times F_{SW} \quad (8)$$

Where L_K is the leakage inductance, and I_{PEAK} is the peak switching current.

Since R13 consumes the leakage inductance power loss, R13 is selected with Equation (9):

$$R13 = \frac{V_{SN}^2}{P_{SN}} \quad (9)$$

Where V_{SN} is the expected snubber voltage on C8.

The snubber capacitor (C8) can be designed to achieve an appropriate voltage ripple on the snubber using Equation (10):

$$\Delta V_{SN} = \frac{V_{SN}}{R13 \times C8 \times F_{SW}} \quad (10)$$

Generally, a 15% ripple is acceptable.

Selecting the Power MOSFET

The MP8008L is capable of driving a wide variety of N-channel power MOSFETS. The critical parameters of selecting a MOSFET are maximum drain-to-source voltage ($V_{DS(MAX)}$), maximum current ($I_{D(MAX)}$), on resistance ($R_{DS(ON)}$), gate source charge (Q_{GS}) and gate drain charge (Q_{GD}), total gate charge (Q_G), and turn-on threshold (V_{TH}).

Ideally, the off-state voltage across the MOSFET is calculated with Equation (11):

$$V_{MOSFET} = V_{IN} + N \times V_{OUT} \quad (11)$$

Considering the voltage spike when it turns off, $V_{DS(MAX)}$ should be greater than 1.5 times the output voltage.

The maximum current through the power MOSFET occurs when the input voltage is at its minimum and the output power is at its maximum. The current rating of the MOSFET should be greater than 1.5 times I_{RMS}.

The on resistance of the MOSFET determines the conduction loss and should therefore be small.

Q_G is important for MOSFET selection since it determines the commutation time. A high Q_G leads to high switching loss. A low Q_G may cause a fast turn-on/-off speed, which determines the spike and kick.

The turn-on threshold voltage (V_{TH}) is also important. GATE is powered by VCC, so V_{TH} must be lower than VCC.

Selecting the Output Diode

The flyback output rectifier diode supplies current to the output capacitor when the primary side MOSFET is off. Use a Schottky diode to reduce losses due to the diode forward voltage and recovery time. The diode should be rated for a reverse voltage 1.5 times greater than the value calculated from Equation (12):

$$V_{DIODE} = \frac{V_{IN}}{N} + V_{OUT} \quad (12)$$

The average current rating must exceed the maximum expected load current, and the peak current rating must exceed the output winding peak current.

PCB Layout Guidelines

Efficient layout of the PoE front-end and high-frequency switching power supply is critical for stable operation. Poor layout may result in reduced performance, excessive EMI, resistive loss, and system instability. For best results, refer to Figure 9 and follow the guidelines below.

For the PD interface circuit:

All component placement must follow the power flow from RJ-45, Ethernet transformer, diode bridges, TVS to 0.1μF capacitor, and DC/DC converter input bulk capacitor. The spacing between VDD and VSS must comply with safety standards such as IEC60950.

1. Make all leads as short as possible with wide power traces.
2. Place the PD interface circuit ground planes referenced to VSS.
3. Place the switching converter ground planes referenced to RTN/GND.
4. Connect the exposed pad to GND.
   It cannot be connected to VSS.
5. Place the AUX divider resistor close to AUX if adapter power detection is enabled.
6. Place the diode (D4) close to VSS and RTN.

For the flyback circuit:

1. Keep the input loop between the input capacitor, transformer, MOSFET, current sense resistor, and GND plane as short as possible for minimal noise and ringing.
2. Keep the output loop between the rectifier diode, output capacitor, and transformer as short as possible.
3. Keep the clamp loop circuit between D6, C8, and the transformer as small as possible
4. Place the VCC capacitor close to VCC for the best decoupling.
5. Keep the feedback trace far away from noise sources such as the drain of the power MOSFET.
6. Use single-point connection between the power GND and signal GND.

For more detail information, refer to the flyback evaluation board datasheet.

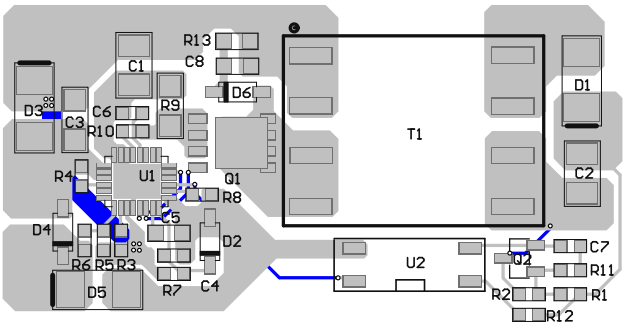


Figure 9: Recommended Layout

Design Example

Table 2 is a design example following the application guidelines for the following specifications.

Table 2: Flyback Design Example

V_{DD} - V_{SS}	37V - 57V (PoE supply)
R_{DET}	24.9kΩ
R_{CLASS}	28.7Ω (class 4)
$V_{ADAPTER}$ (13)	12V
V_{OUT}	12V
I_{OUT}	2.1A

The typical application circuit in Figure 10 shows the detailed application schematic and is the basis for the typical performance waveforms. Typically, the device is powered by PSE (V_{DD} - V_{SS} = 48V). For more detailed device applications, please refer to the related evaluation board datasheets.

NOTE:

13) When using a 12V adapter and the load is 2.1A, the board's temperature is high. It can be optimized by a larger PCB layout.

TYPICAL APPLICATION CIRCUIT

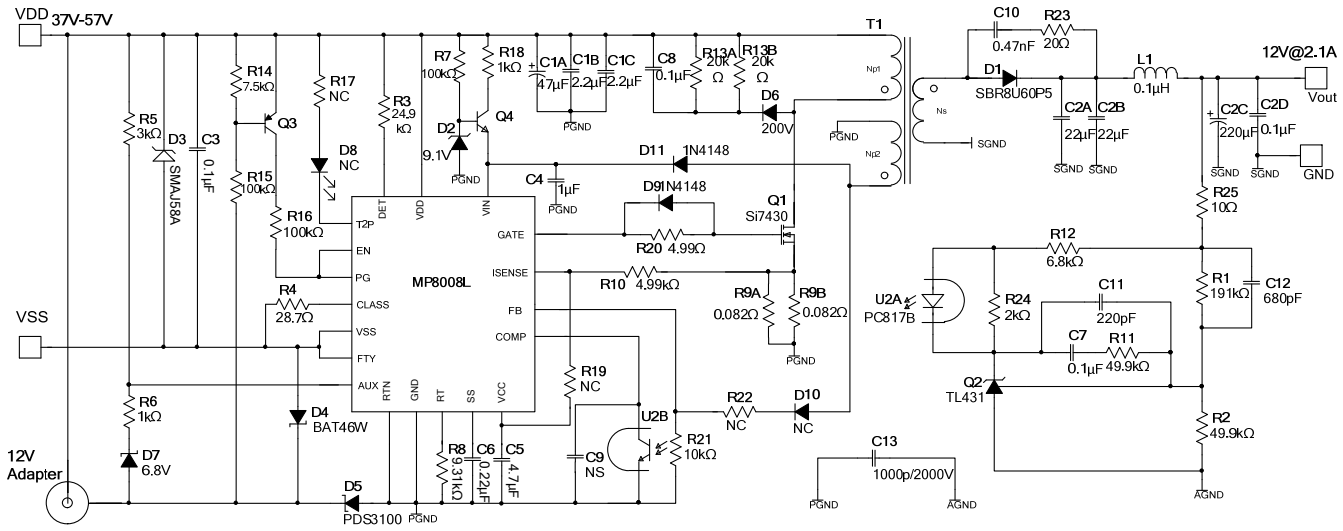
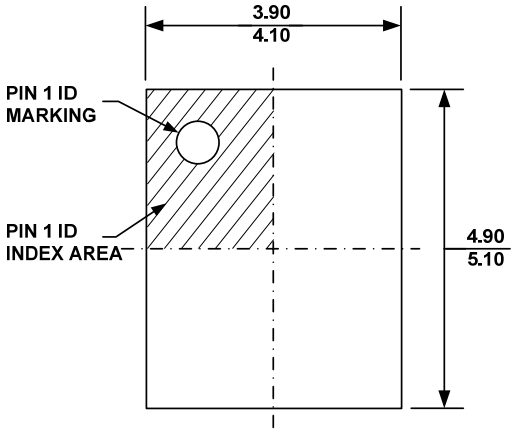


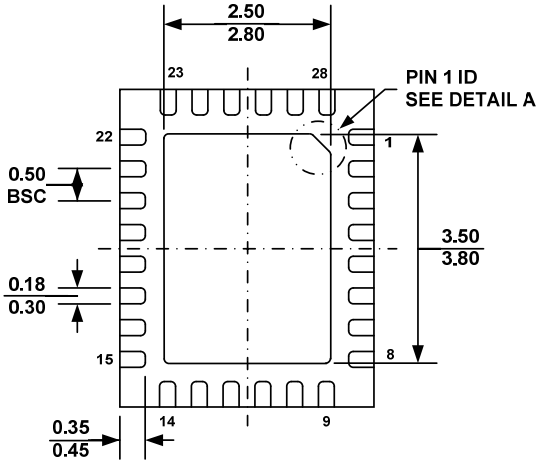
Figure 10: Typical Application Circuit, VDD = 37 - 57V PoE Input or 12V Adaptor, V_{OUT} = 12V @ 2.1A

PACKAGE INFORMATION

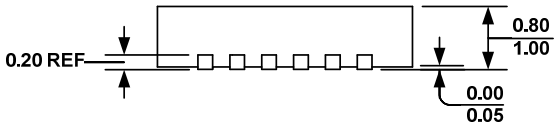
QFN-28 (4mmx5mm)



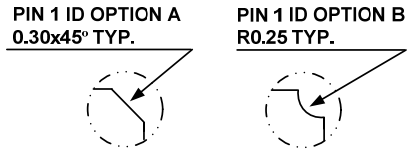
TOP VIEW



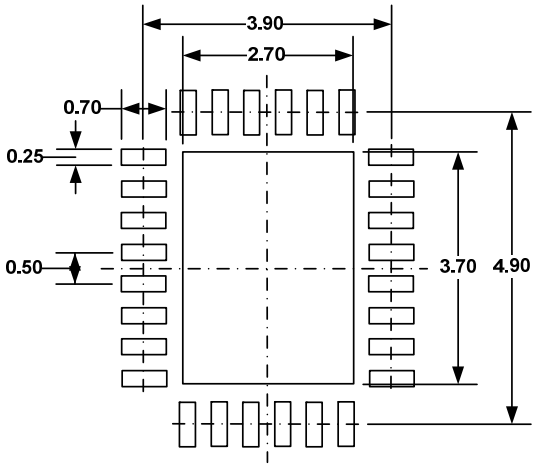
BOTTOM VIEW



SIDE VIEW



DETAIL A



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX.
4) DRAWING CONFORMS TO JEDEC MO-220, VARIATION VGHD-3.
5) DRAWING IS NOT TO SCALE.