

### DESCRIPTION

The MP6923 is a dual, fast turn-off, intelligent rectifier for synchronous rectification in LLC resonant converters.

The IC drives two N-channel MOSFETs and regulates their forward voltage drop to about 15mV. The IC turns off both MOSFETs before the switching current goes negative.

The MP6923 uses a light-load function to latch off the gate driver under light-load conditions, limiting the current to below 600µA.

The MP6923's fast turn-off enables both continuous conduction mode (CCM) and discontinuous conduction mode (DCM). An internal anti-bounce logic function ensures safe MOSFET operation.

The MP6923 requires a minimal number of readily available, standard, external components and is available in a SOIC14 package.

### FEATURES

- Works with Both Standard and Logic-Level MOSFETs
- Compatible with Energy Star's 0.5W Standby Requirements
- V<sub>DD</sub> Range from 8V to 24V
- 15mV VDS Regulation Function <sup>(1)</sup>
- Fast Turn-Off: Total Delay of 20ns
- Anti-Bounce Logic<sup>(1)</sup>
- Maximum Switching Frequency of 300kHz
- Light-Load Mode Function<sup>(1)</sup> with <600µA of Quiescent Current
- Supports CCM, CrCM, and DCM Operation
- Available in a SOIC14 Package

### APPLICATIONS

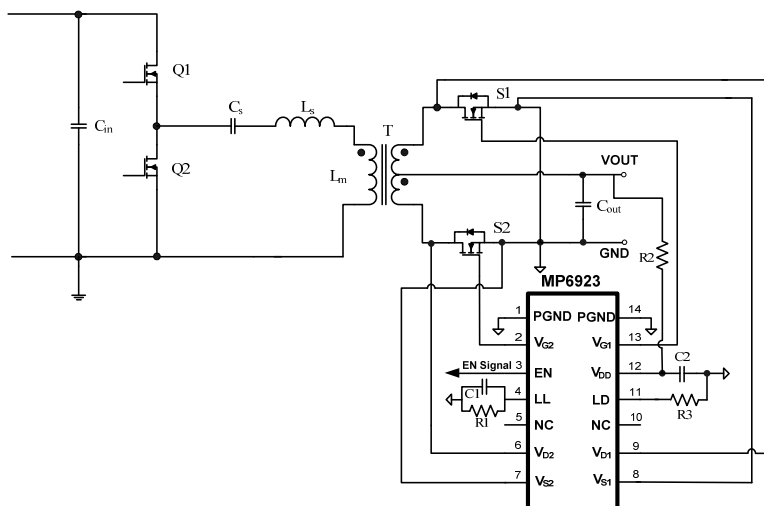
- AC/DC Adapters
- LCDs and PDP TVs
- Telecom SMPS

All MPS parts are lead-free, halogen-free, and adhere to the RoHS directive. For MPS green status, please visit MPS website under quality assurance. "MPS" and "The Future of Analog IC Technology" are registered trademarks of Monolithic Power Systems, Inc.

#### NOTE:

1) Related issued patent: US Patent US8,067,973; US8,400,790. CN Patent ZL201010504140.4; ZL200910059751.X. Other patents pending.

### TYPICAL APPLICATION



### ORDERING INFORMATION

Part Number*	Package	Top Marking
MP6923GS	SOIC14	See Below

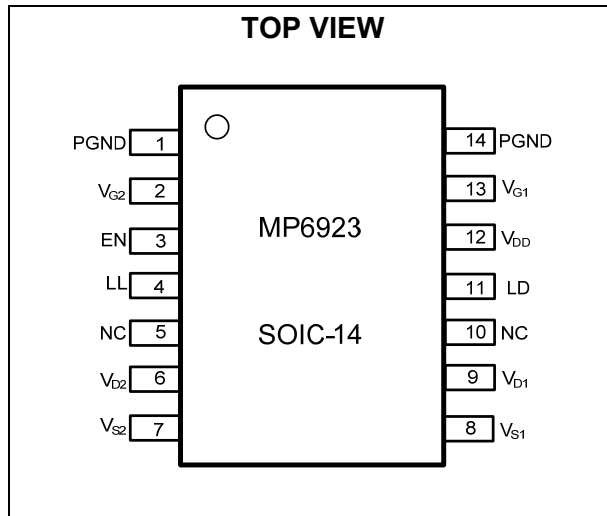
\*For Tape & Reel, add suffix -Z (e.g. MP6923GS-Z)

### TOP MARKING

**MPSYYWW**  
**MP6923**  
**LLLLLLLLL**

MPS: MPS prefix;  
 YY: year code;  
 WW: week code;  
 MP6923: part number;  
 LLLLLLLL: lot number;

### PACKAGE REFERENCE



**ABSOLUTE MAXIMUM RATINGS** <sup>(2)</sup>

$V_{DD}$ to $V_{S1}$ , $V_{S2}$ .....	-0.3V to +26V
PGND to $V_{S1}$ , $V_{S2}$ .....	-0.3V to +0.3V
$V_{G1}$ to $V_{S1}$ .....	-0.3V to $V_{DD}$
$V_{G2}$ to $V_{S2}$ .....	-0.3V to $V_{DD}$
$V_{D1}$ to $V_{S1}$ .....	-0.7V to +180V
$V_{D2}$ to $V_{S2}$ .....	-0.7V to +180V
LL, EN, LD to $V_{S1}$ , $V_{S2}$ .....	-0.3V to +6.5V
Maximum operating frequency.....	300kHz
Continuous power dissipation.....( $T_A = +25^\circ\text{C}$ ) <sup>(3)</sup>	1.5W
Junction temperature.....	150°C
Lead Temperature (solder).....	260°C
Storage temperature.....	-55°C to +150°C

**Recommended Operation Conditions** <sup>(4)</sup>

$V_{DD}$ to $V_{S1}$ , $V_{S2}$ .....	8V to 24V
Operating junction temp. ( $T_J$ )...	-40°C to +125°C

**Thermal Resistance** <sup>(5)</sup>

	$\theta_{JA}$	$\theta_{JC}$
SOIC14 .....	86	38

**NOTES:**

- 2) Exceeding these ratings may damage the device.
- 3)  $T_A = +25^\circ\text{C}$ . The maximum allowable power dissipation is a function of the maximum junction temperature  $T_J(\text{MAX})$ , the junction-to-ambient thermal resistance  $\theta_{JA}$ , and the ambient temperature  $T_A$ . The maximum allowable continuous power dissipation at any ambient temperature is calculated by  $P_D(\text{MAX}) = (T_J(\text{MAX}) - T_A) / \theta_{JA}$ . Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- 4) The device is not guaranteed to function outside of its operating conditions.
- 5) Measured on JESD51-7, 4-layer PCB, without heatsink.

## ELECTRICAL CHARACTERISTICS

$V_{DD} = 12V$ ,  $-40^{\circ}C \leq T_J \leq 125^{\circ}C$ , unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	
$V_{DD}$ voltage range			8		24	V	
$V_{DD}$ UVLO threshold		Rising	4.7	6.0	8.1	V	
		Hysteresis	0.3	1	1.5	V	
Operating current	$I_{CC}$	$C_{LOAD} = 5nF$ , $F_{SW} = 100kHz$	15	18	23	mA	
		$C_{LOAD} = 10nF$ , $F_{SW} = 100kHz$	24	27	31	mA	
Shutdown current		$V_{DD} = 20V$ , $EN = 0V$			600	$\mu A$	
Light-load mode current					600	$\mu A$	
Thermal shutdown <sup>(6)</sup>				150		$^{\circ}C$	
Thermal shutdown hysteresis <sup>(6)</sup>				30		$^{\circ}C$	
Enable shutdown threshold		Rising	1.1	1.5	2.0	V	
		Hysteresis		0.2	0.55	V	
Enable UVLO threshold		Rising	2.3	3	3.6	V	
		Hysteresis		0.2	0.55	V	
Internal pull-up current on EN				10	16	$\mu A$	
<b>Control Circuitry Section</b>							
$V_{S1,2} - V_{D1,2}$ forward voltage <sup>(6)</sup>	$V_{fwd}$		0	15	30	mV	
Turn-on delay	$T_{Don}$	$C_{LOAD} = 5nF$	$-20^{\circ}C \leq T_J \leq 125^{\circ}C$		150	200	ns
			$-40^{\circ}C \leq T_J < -20^{\circ}C$		250		
		$C_{LOAD} = 10nF$	$-20^{\circ}C \leq T_J \leq 125^{\circ}C$		250	300	ns
			$-40^{\circ}C \leq T_J < -20^{\circ}C$		350		
Input bias current on $V_{D1,2}$		$V_{D1,2} = 180V$			1.5	$\mu A$	
Minimum on time	$T_{MIN}$	$C_{LOAD} = 5nF$	100	500	1100	ns	
Minimum off time	$T_{OFF}$		0.6	1.5	2.6	$\mu s$	
Light-load enter delay	$T_{LL-Delay}$	$R_{LD} = 100k\Omega$	550	900	1100	$\mu s$	
Light-load enter pulse width	$T_{LL}$	$R_{LL} = 100k\Omega$	1.3	2.1	2.9	$\mu s$	
Light-load turn-on pulse width hysteresis	$T_{LL-H}$	$R_{LL} = 100k\Omega$		0.2		$\mu s$	
Light-load enter off period width	$T_{LL-OFF}$	$R_{LL} = 100k\Omega$	30	45	60	$\mu s$	
Light-load exit pulse width threshold ( $V_{D1,2} - V_{S1,2}$ )	$V_{LL-DS}$		-550	-300	-140	mV	
<b>Gate Driver Section</b>							
$V_{G1,2}$ (low)		$I_{LOAD} = 1mA$			0.1	V	
$V_{G1,2}$ (high)		$V_{DD} > 17V$	13	14.5	16.5	V	
		$V_{DD} < 17V$		$V_{DD} - 2.2$			
Turn-off threshold ( $V_{S1,2} - V_{D1,2}$ )			-35	-15	5	mV	
Turn-off propagation delay		$V_{D1,2} = V_{SS}$		20	55	ns	
Turn-off total delay	$T_{Doff}$	$V_{D1,2} = V_{SS}$ , $C_{LOAD} = 5nF$ , $R_{GATE} = 0\Omega$		50	75	ns	
		$V_{D1,2} = V_{SS}$ , $C_{LOAD} = 10nF$ , $R_{GATE} = 0\Omega$		50	75	ns	
Pull-down impedance				1	2	$\Omega$	
Pull-down current <sup>(6)</sup>		$3V < V_{G1,2} < 10V$		3		A	

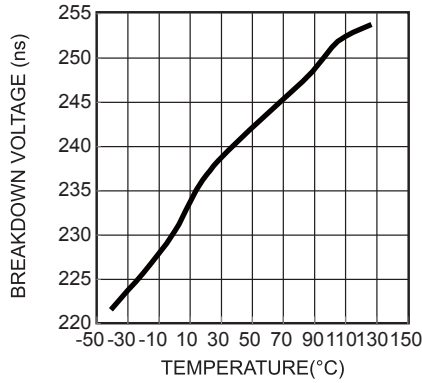
**NOTE:**

6) Guaranteed by design and characterization test.

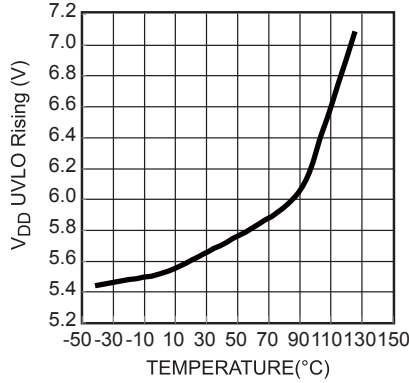
## TYPICAL PERFORMANCE CHARACTERISTICS

$V_{DD} = 12V$ , unless otherwise noted.

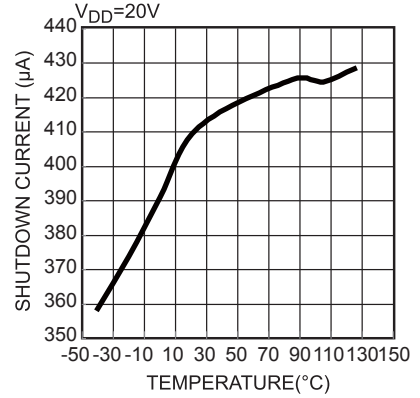
$V_{D1,2}$  Breakdown Voltage vs. Temperature



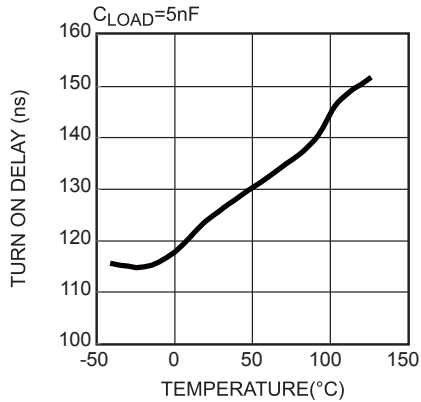
$V_{DD}$  UVLO Rising vs. Temperature



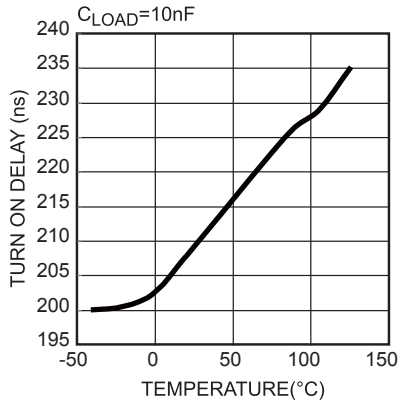
Shutdown Current vs. Temperature



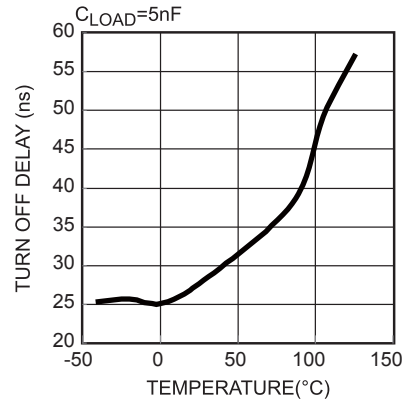
Turn-On Delay vs. Temperature



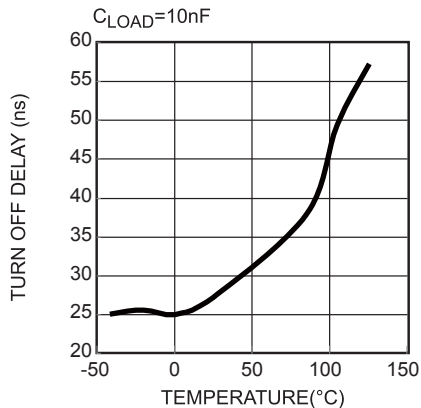
Turn-On Delay vs. Temperature



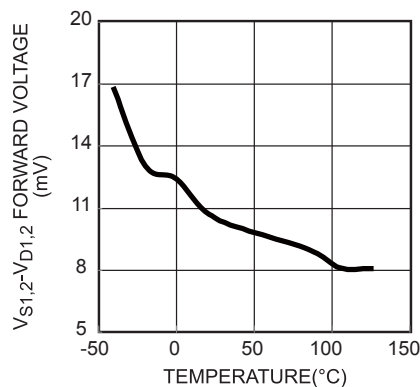
Turn-Off Delay vs. Temperature



Turn-Off Delay vs. Temperature



$V_{S1,2}-V_{D1,2}$  Forward Voltage vs. Temperature

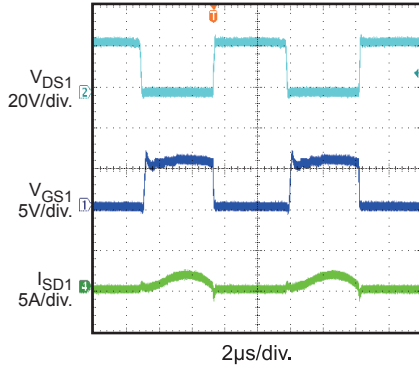


**TYPICAL PERFORMANCE CHARACTERISTICS** *(continued)*

$V_{DD} = 12V$ , unless otherwise noted.

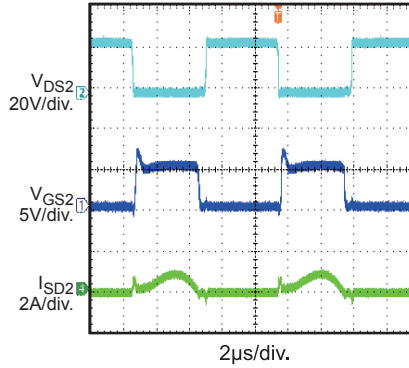
**Operation in 90W LLC Converter**

$V_{IN}=240VAC, V_{OUT}=12V, I_{OUT}=0.75A$



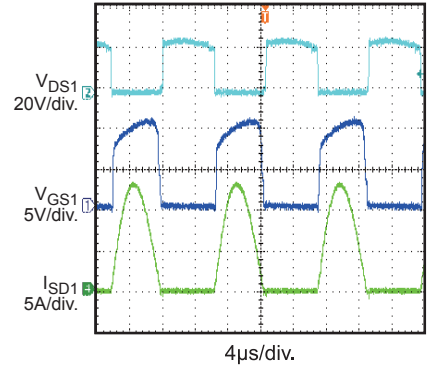
**Operation in 90W LLC Converter**

$V_{IN}=240VAC, V_{OUT}=12V, I_{OUT}=0.75A$



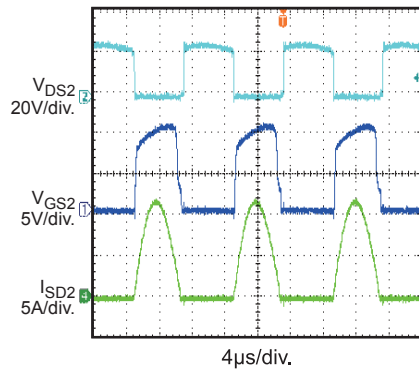
**Operation in 90W LLC Converter**

$V_{IN}=240VAC, V_{OUT}=12V, I_{OUT}=7.5A$



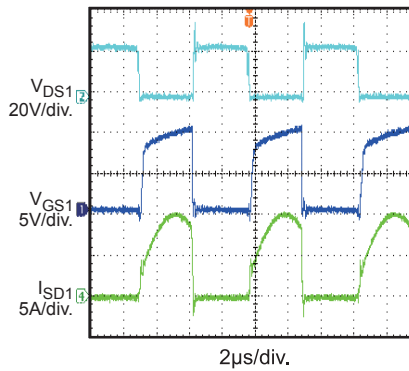
**Operation in 90W LLC Converter**

$V_{IN}=240VAC, V_{OUT}=12V, I_{OUT}=7.5A$



**Operation in 90W LLC Converter**

$V_{IN}=265VAC, V_{OUT}=12V, I_{OUT}=7.5A$



## PIN FUNCTIONS

Pin #	Name	Description
1, 14	PGND	<b>Power ground.</b> PGND is the power switch return.
2	V <sub>G2</sub>	<b>MOSFET 2 gate driver output.</b>
3	EN	<b>Enable.</b> EN enables the internal IC logic when the EN voltage exceeds the EN shutdown threshold. The gate driver remains latched until the EN voltage exceeds the EN UVLO threshold.
4	LL	<b>Light-load timing set.</b> Connect a resistor to LL to set the light-load timing.
5, 10	NC	<b>No connection.</b>
6	V <sub>D2</sub>	<b>MOSFET 2 drain voltage sense.</b>
7	V <sub>S2</sub>	<b>Source used as reference for V<sub>D2</sub>.</b>
8	V <sub>S1</sub>	<b>Source used as reference for V<sub>D1</sub>.</b>
9	V <sub>D1</sub>	<b>MOSFET 1 drain voltage sense.</b>
11	LD	<b>Light-load enter delay set.</b> Connect a resistor to LD to set the light-load enter delay.
12	V <sub>DD</sub>	<b>Supply voltage.</b>
13	V <sub>G1</sub>	<b>MOSFET 1 gate driver output.</b>

**BLOCK DIAGRAM**

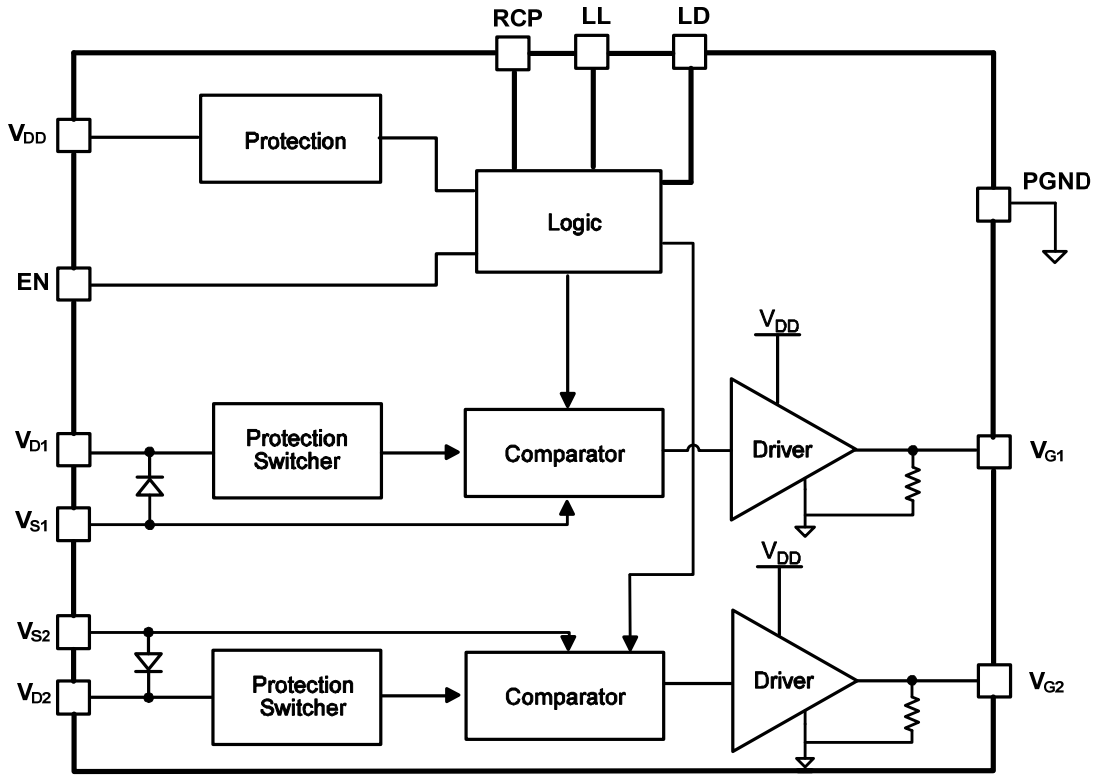


Figure 1: Functional Block Diagram



## OPERATION

The MP6923 operates in discontinuous conduction mode (DCM), continuous conduction mode (CCM), and critical conduction mode (CrCM). When operating in DCM or CrCM, the control circuitry controls the gate in forward mode and turns the gate off when the MOSFET current is low. In CCM, the control circuitry turns the gate off during very fast transients.

### Blanking

The control circuitry contains a blanking function to ensure that when the MOSFET turns on/off, the MOSFET remains on/off for about 1 $\mu$ s. This determines the minimum on time. During the turn-on blanking period, the turn-off threshold is not blanked completely but changes to about +50mV instead of +30mV. This ensures that the part can always turn off, even during the turn-on blanking period, although it does so more slowly. Avoid setting the synchronous period below 1 $\mu$ s in CCM in the LLC converter to eliminate shoot-through.

### VD Clamp

The MP6923 uses a high-voltage JFET at its input since V<sub>D1,2</sub> can rise as high as 180V. Connect a small resistor between V<sub>D1,2</sub> and the external MOSFET drain to avoid excessive currents when V<sub>G</sub> falls below -0.7V.

### Under-Voltage Lockout (UVLO)

When V<sub>DD</sub> falls below the UVLO threshold, the part enters sleep mode, and a 10k $\Omega$  resistor pulls V<sub>G</sub> down.

### Enable (EN)

When EN is pulled low, the MP6923 enters sleep mode.

### Thermal Shutdown

If the junction temperature of the IC exceeds 150°C, V<sub>G</sub> is pulled low, and the part stops switching. The part resumes normal operation after the junction temperature drops to 120°C.

### Turn-On Phase

V<sub>DS</sub> (V<sub>D</sub> - V<sub>SS</sub>) goes negative (<-500mV) when the switch current flows through the MOSFET's body diode. If V<sub>DS</sub> is much lower than the V<sub>fwd</sub> threshold of the control circuitry (-15mV), then

the MOSFET turns on after about 200ns of delay (see Figure 2).

Triggering the V<sub>fwd</sub> threshold (-15mV) causes the circuit to add a blanking time with a minimum on-time of 0.5 $\mu$ s. During this time, the turn-off threshold changes from +30mV to about +50mV. This blanking time avoids false triggering caused by ringing on the synchronous power switch.

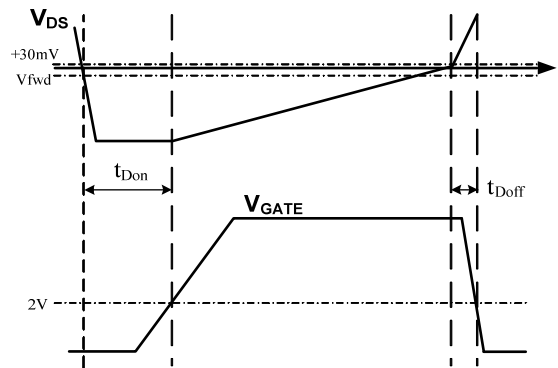


Figure 2: Turn-On and Turn-Off Delay

### Conducting Phase

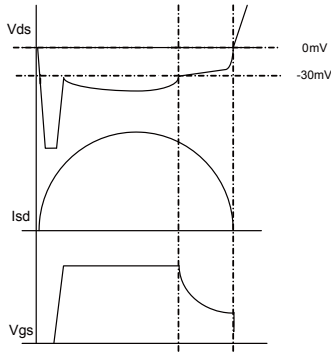
When the MOSFET turns on, V<sub>DS</sub> (-I<sub>SD</sub> × R<sub>DS(ON)</sub>) rises relative to the switch current (I<sub>SD</sub>) drop. When V<sub>DS</sub> rises above the V<sub>fwd</sub> threshold (-15mV), the control circuitry stops pulling the gate driver up, and the MOSFET driver voltage drops, increasing the MOSFET's R<sub>DS(ON)</sub>. This adjusts V<sub>DS</sub> (-I<sub>SD</sub> × R<sub>DS(ON)</sub>) to around -15mV, even when the switch current (I<sub>SD</sub>) is fairly small and can prevent the internal driver from triggering until the current through the MOSFET has almost dropped to zero.

### Turn-Off Phase

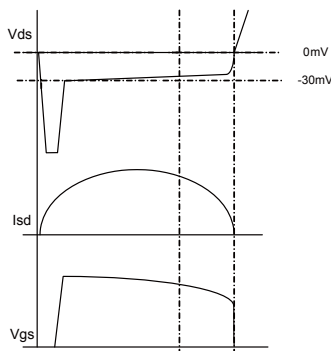
When V<sub>DS</sub> rises to trigger the turn-off threshold (30mV), the control circuitry pulls down the driver switch voltage after a turn-off delay (see Figure 2). Similarly, a 1.5 $\mu$ s blanking time occurs after the switch turns off, during which the MOSFET does not turn on to avoid false triggering.

Figure 3 shows the MP6923 operating in a heavy load. Initially, the high current saturates the driver voltage. After V<sub>DS</sub> rises above -15mV, the driver voltage decreases to adjust V<sub>DS</sub> to around -15mV.

Figure 4 shows the MP6923 operating in a light load. The low current prevents the driver voltage from saturating but decreases when the synchronous power switch turns on and adjusts V<sub>DS</sub>.



**Figure 3: Synchronous Rectification Operation at Heavy Load**



**Figure 4: Synchronous Rectification Operation at Light Load**

**Light-Load Latch-Off Function**

The gate driver of the MP6923 is latched to limit driver losses under light-load conditions to improve light-load efficiency.

**Normal Operation Latch-Off**

When the MOSFET’s switching cycle conducting period falls below 2.1μs (τ<sub>LL</sub>), the MP6923 enters light-load mode and latches off the MOSFET after a 900μs delay (light-load enter delay, τ<sub>LL-Delay</sub>). This delay time is programmable by connecting a resistor on LD, as shown in Equation (1):

$$t_{LL-Delay} = 900\mu s \cdot \frac{R_{LD}}{100k\Omega} \quad (1)$$

After entering light-load mode, the MP6923 monitors the MOSFET’s body diode conducting period by sensing V<sub>DS</sub>. When V<sub>DS</sub> exceeds

-300mV (V<sub>LL-DS</sub>), the MP6923 treats the MOSFET’s body diode conducting period as complete. If the MOSFET’s body diode conducting period exceeds 2.3μs (τ<sub>LL</sub> + τ<sub>LL-H</sub>), light-load mode ends, and the MOSFET unlatches to restart the synchronous rectification.

The MP6923 uses LL to adjust τ<sub>LL</sub> with an external resistor, as shown in Equation (2):

$$t_{LL} = 2.1\mu s \cdot \frac{R_{LL}}{100k\Omega} \quad (2)$$

**Latch-Off during Burst Operation**

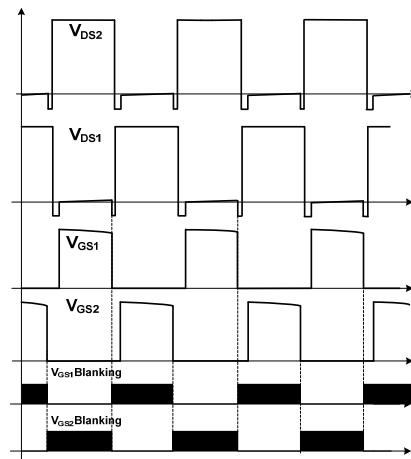
The IC also monitors the synchronous MOSFET off period. If the off period exceeds the light-load enter off period width (τ<sub>LL-OFF</sub>), the MP6923 enters light-load mode and latches off the gate driver.

The gate driver is unlatched when the drain-source voltage of the synchronous MOSFET (V<sub>DS</sub>) drops below V<sub>fwd</sub>.

**Anti-Bounce Logic**

The MP6923 has anti-bounce logic on both drivers, which helps protect the two-channel drivers from cross conduction.

Figure 5 shows the anti-bounce logic for the two-channel drivers. When channel 1 or 2 is turned off, this channel gate driver is blanked until channel 2 or 1 turns off.



**Figure 5: Anti-Bounce Logic of the Gate Drivers**

## APPLICATION INFORMATION

### Layout Considerations

Listed below are the main recommendations that should be taken into consideration when designing the PCB.

#### 1. Sensing for $V_D/V_S$

- Place the sensing connections ( $V_D/V_S$ ) as close to the MOSFET (drain/source) as possible.
- Keep the two channels' sensing loops separated.
- Keep the sensing loop as small as possible. (see Figure 6)
- See Figure 7 for a layout example of the MP6923 driving PowerPAK SO8 package MOSFETs with two separate, small, sensing loops.

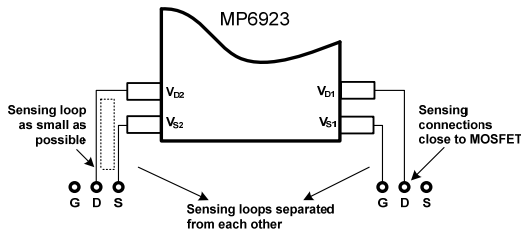


Figure 6: Sensing for  $V_D/V_S$

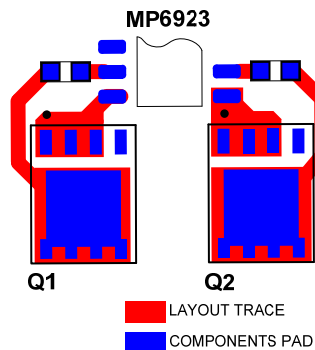


Figure 7: Layout Example for Sensing Loop

#### 2. $V_{DD}$ Decoupling Capacitor

- Place a decoupling capacitor from  $V_{DD}$  to PGND (no smaller than  $1\mu\text{F}$ ) as close to the IC as possible for adequate filtering.

#### 3. System Power Loop

- Keep the two channels' power loops separated to minimize their interaction, which may affect the voltage sensing of the IC (see Figure 8).

- Keep the power loop as small as possible to reduce parasitic inductance.
- See Figure 9 for a layout example of the power loop trace, which has a minimized loop length. The two channel power traces do not cross with each other.
- Place the driver's sensing loop trace (in Figure 7) away from the power loop trace (in Figure 9). The sensing loop trace and power loop trace can be put on different layers to keep them separate.
- Keep the driver IC out of the power loop; otherwise, the MOSFET voltage sensing may be affected.

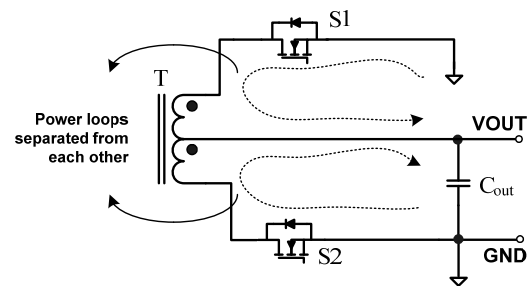


Figure 8: System Power Loop

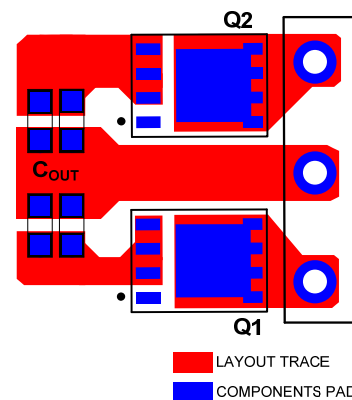


Figure 9: Layout Example for System Power Loop

### SR MOSFET Selection and Driver Ability

The power MOSFET selection is a trade-off between  $R_{DS(ON)}$  and  $Q_g$ . To achieve high efficiency, MOSFETs with a smaller  $R_{DS(ON)}$  are always preferred. Usually, the  $Q_g$  is larger with a smaller  $R_{DS(ON)}$ , making the turn-on/off speed lower and the power loss larger. For the MP6923, the  $V_{DS}$  is adjusted to about 15mV during the driving period. A MOSFET with an  $R_{DS(ON)}$  that is too small is not recommended. The gate driver may be kept at a fairly low level with an  $R_{DS(ON)}$  that is too small, even when the system load is high, making the advantage of the low  $R_{DS(ON)}$  inconspicuous.

Figure 10 shows the typical waveform of LLC on the secondary side. To achieve high usage of the MOSFET's  $R_{DS(ON)}$ , the MOSFET driver voltage is kept at a maximum level until the last 25% of the SR conduction period, as shown in Equation (3):

$$V_{DS} = -R_{ds(ON)} \cdot \frac{\sqrt{2}}{2} \cdot I_{peak} = -R_{ds(ON)} \cdot I_{OUT} = -15mV \quad (3)$$

Where  $V_{DS}$  is drain source voltage of the MOSFET, and -15mV is the  $V_{fwd}$  of the MP6923.

The MOSFET's  $R_{DS(ON)}$  is recommended to be no lower than  $15/I_{OUT}$  (mΩ). For example, in 10A applications, the  $R_{DS(ON)}$  of the MOSFET is recommended to be no lower than 1.5mΩ.

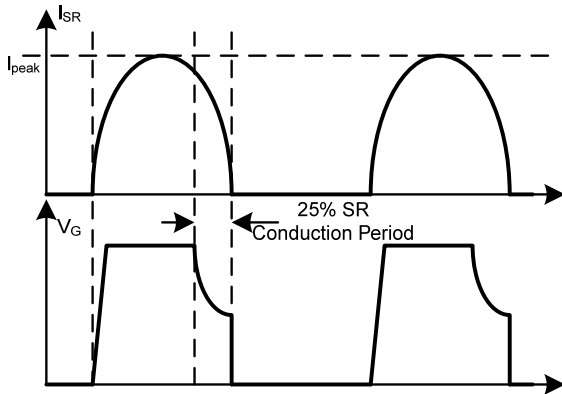


Figure 10: Synchronous Rectification Typical Waveform in LLC

The  $Q_g$  of the MOSFET affects the turn-on/off delay. Figure 2 indicates the turn-on delay ( $t_{Don}$ ) and turn-off delay ( $t_{Doff}$ ).  $T_{Don}$  is how long the body diode conducts before the MOSFET is turned on;  $T_{Doff}$  is how long the driver takes to turn off the MOSFET. With a higher turn-on delay, the body diode conduction duration of the MOSFET is longer, which brings down the total efficiency. A higher turn-off delay increases the risk for shoot-through in CCM operation.

Figure 11 and Figure 12 show the  $t_{Don}$  and  $t_{Doff}$  of the MP6923, according to different  $C_{load}$ s.

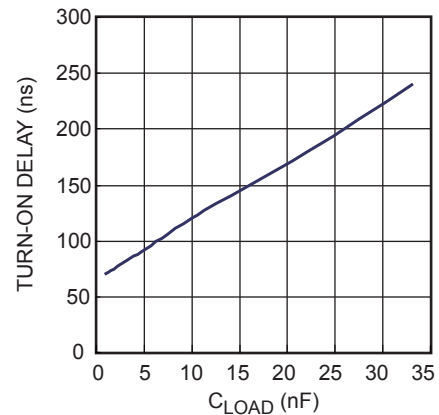


Figure 11: Turn-On Delay vs.  $C_{load}$

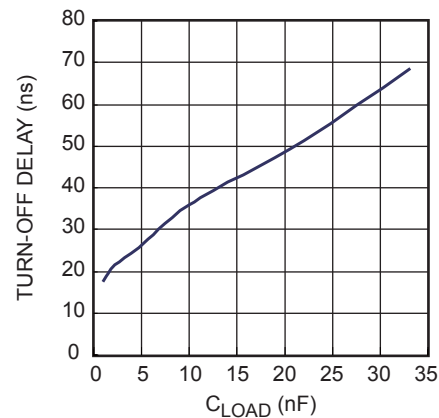
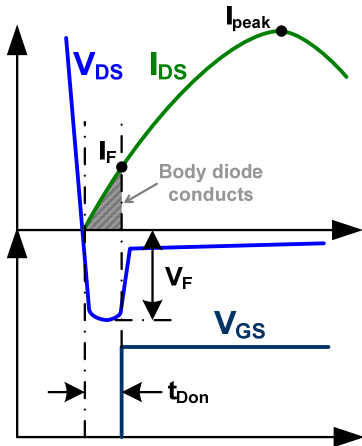


Figure 12: Turn-Off Delay vs.  $C_{load}$



**Figure 13: Turn-On Delay Effect on Efficiency**

Figure 13 shows how  $t_{Don}$  affects the system efficiency. During  $t_{Don}$ , the body diode of the SR MOSFET conducts, leading to a power loss, as shown in Equation (4):

$$P_{on} \approx \frac{V_F \cdot I_F}{2} \cdot 2f_s \cdot t_{Don} = V_F \cdot I_F \cdot f_s \cdot t_{Don} \quad (4)$$

Where the  $V_F$  is the body diode forward-voltage drop,  $I_F$  is the switching current when the turn-on delay ( $t_{Don}$ ) has ended, and  $f_s$  is the switching frequency.

Consider the switching current as a complete sine wave. The  $I_F$  can then be estimated with Equation (5):

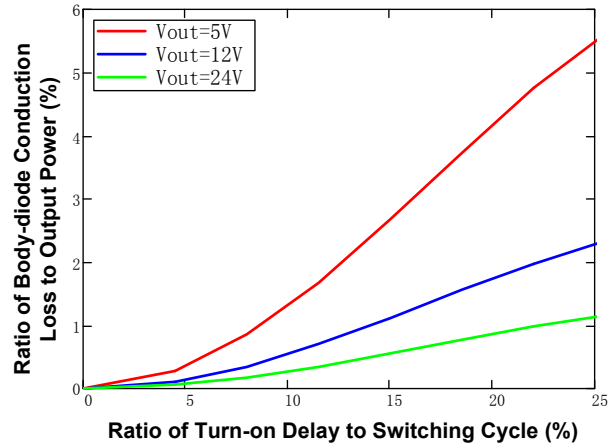
$$I_F = I_{peak} \cdot \sin(2 \cdot f_s \cdot t_{Don} \cdot \pi) \quad (5)$$

Where  $I_{peak}$  is the peak switching current through the MOSFET and can be calculated with Equation (6):

$$I_{peak} \approx \frac{\pi}{2} \cdot I_{out} \quad (6)$$

Where  $I_{out}$  is the system output current. Put Equation (5) and Equation (6) into Equation (4). The turn-on delay power loss through the SR MOSFET's body diode can then be calculated with Equation (7):

$$P_{on} = \frac{\pi}{2} \cdot I_{out} \cdot V_F \cdot f_s \cdot t_{Don} \cdot \sin(2 \cdot f_s \cdot t_{Don} \cdot \pi) \quad (7)$$



**Figure 14: Turn-On Delay vs. Power Loss**

Figure 14 shows how different turn-on delays affect the efficiency according to different output voltages. To keep the body diode conduction loss fairly low (below 0.5% of the output power), keep the turn-on delay below 5% of the switching cycle. For example, in a  $f_{sw} = 200\text{kHz}$  LLC system, the switching cycle is about  $5\mu\text{s}$ . Select a MOSFET to make  $t_{Don} < 250\text{ns}$ .

Turn-off delays ( $t_{Doff}$ ) are critical in some fast transient CCM applications. Choose a MOSFET to make the  $t_{Doff}$  below the CCM current transient duration. Otherwise, select a MOSFET with a lower  $Q_g$ , or add an external totem pole driver circuit to avoid shoot-through.

TYPICAL APPLICATION CIRCUIT

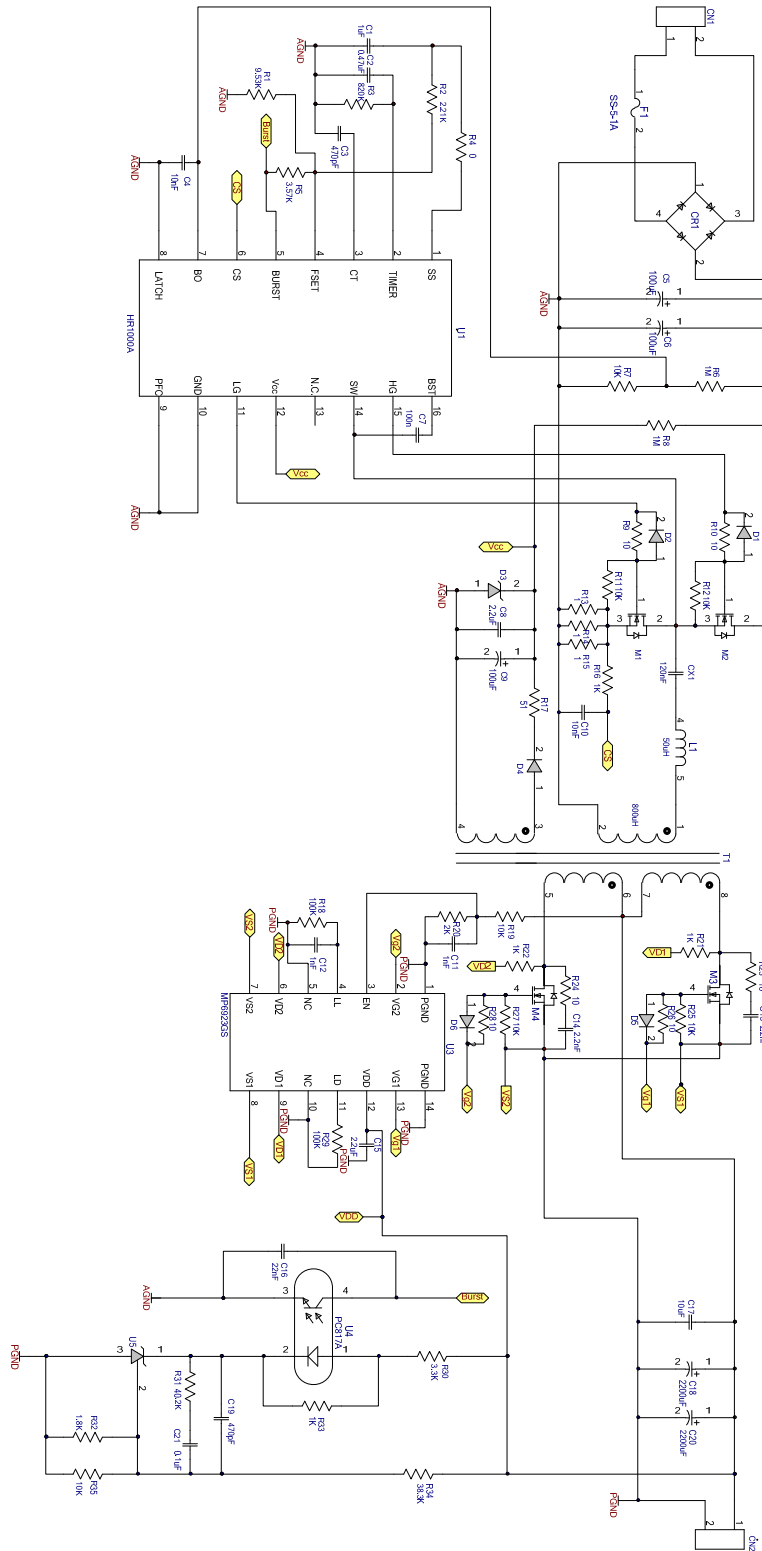
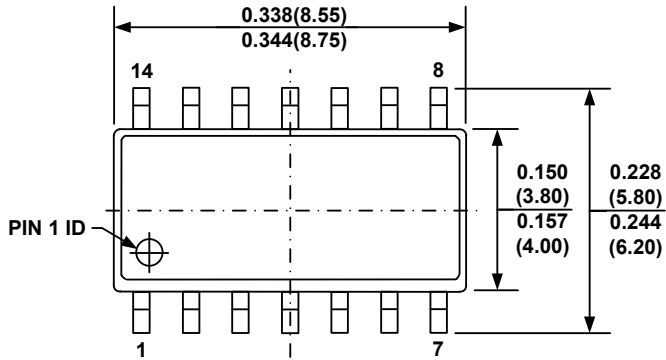


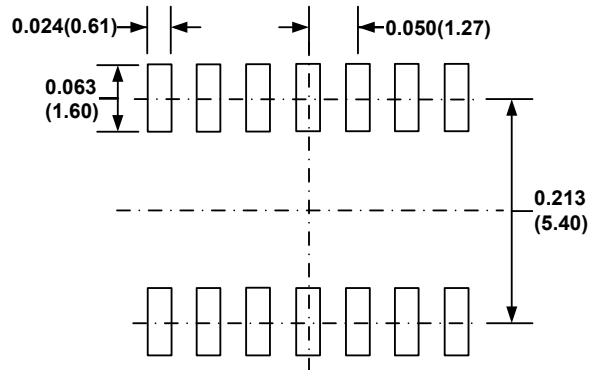
Figure 15: Synchronous Rectification in LLC with MP6923

## PACKAGE INFORMATION

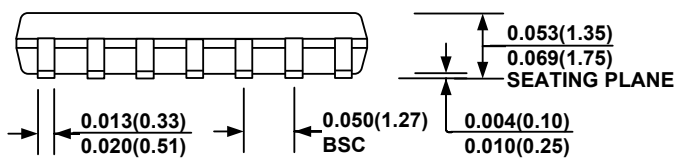
### SOIC14



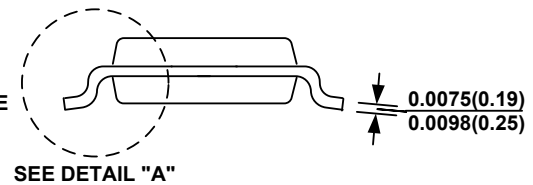
**TOP VIEW**



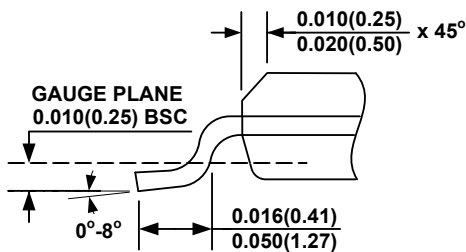
**RECOMMENDED LAND PATTERN**



**FRONT VIEW**



**SIDE VIEW**



**DETAIL "A"**

#### NOTE:

- 1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
- 2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
- 3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
- 4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
- 5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION AB.
- 6) DRAWING IS NOT TO SCALE.

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