MP6653B

35V/1.2A, Single-Phase BLDC Motor Driver with Integrated Hall Sensor and MOSFETs

DESCRIPTION

The MP6653B is a single-phase, brushless DC (BLDC) motor driver with integrated power MOSFETs and an embedded Hall sensor. It drives a single-phase BLDC motor with up to 1.2A of peak coil current. The wide input voltage (V_{IN}) ranges from 3.5V to 35V.

The MP6653B controls the motor speed through the pulse-width modulation (PWM) signal or the DC voltage on the PWM pin. The device features soft commutation, a configurable Hall offset angle, and speed curve configurations.

The rotating speed indicator or locked-rotor indicator (the FG/RD pin) can act as a rotating speed indicator (FG) based on an embedded Hall sensor's output, or locked-rotor indicator (RD) if locked-rotor protection is triggered.

Rich protections include input over-voltage protection (OVP), under-voltage lockout (UVLO), locked-rotor protection, over-current protection (OCP), and thermal shutdown protection.

The MP6653B is available in a TSOT23-6-SL package.

FEATURES

- 3.5V to 35V Operating Input Voltage (V_{IN}) Range
- On-Chip Hall Sensor
- Integrated High-Side MOSFET (HS-FET) and Low-Side MOSFET (LS-FET): 960mΩ
- Selectable Open-Loop or Closed-Loop Speed
- Curve Configurations
- Configurable Starting Duty Cycle
- Configurable Stop Duty Cycle
- Soft Commutation
- Configurable Soft Acceleration Time
- Configurable Hall Leading/Lag Angle
- Supports 50Hz to 100kHz Pulse-Width Modulation (PWM) Input Frequency or DC Input
- Automatic Reverse Current Block
- 24kHz PWM Output Frequency
- Configurable Current Limit
- Short-Circuit Protection (SCP)
- Over-Voltage Protection (OVP)
- Standby Mode
- Selectable FG or RD Output
- Available in a TSOT23-6-SL Package

APPLICATIONS

- Fans
- Cooling Fans
- General BLDC Motors

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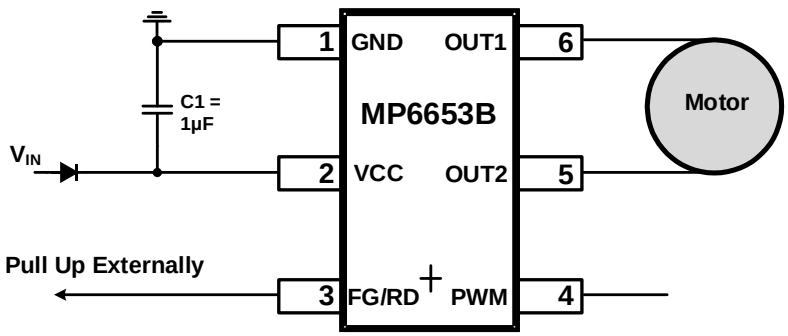
TYPICAL APPLICATION



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ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP6653BGJS-xxxx **	TSOT23-6-SL	*See Below*	1

* For Tape & Reel, add suffix -Z (e.g. MP6653BGJS-xxxx-Z).

** “xxxx” is the configuration code identifier. The four digits of the suffix (xxxx) can be a hexadecimal value between 0 and F. Work with an MPS FAE to create this unique number, even if ordering the default “0000” code.

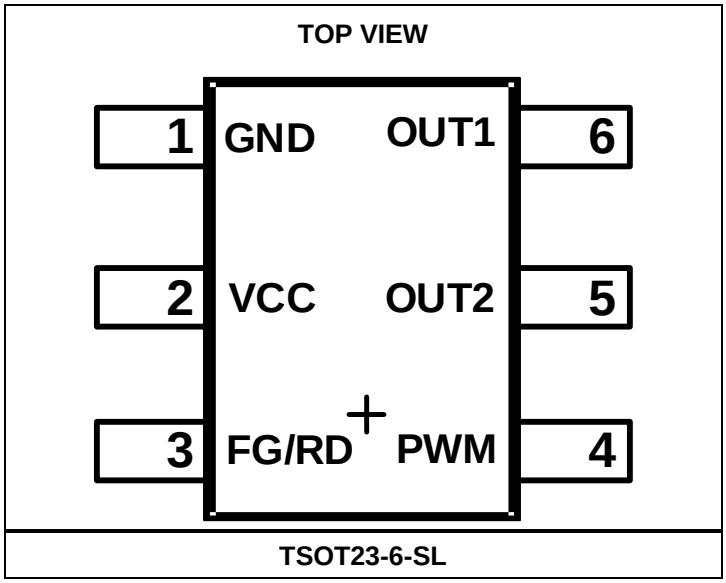
TOP MARKING (MP6653BGJS)

CHPY

LLL

CHP: Product code of MP6653BGJS
Y: Year code
LLL: Lot number

PACKAGE REFERENCE



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PIN FUNCTIONS

Pin #	Name	Description
1	GND	**Ground.**
2	VCC	**Input power supply.** The VCC pin must be locally bypassed.
3	FG/RD	**Speed (FG) or rotor deadlock (RD) indicator output.** The FG/RD pin is an open-drain output. Pull up FG/RD externally.
4	PWM	**Speed control PWM input.** The PWM pin supports a 50Hz to 100kHz PWM input frequency or a 0V to 3V DC input. Pull PWM high internally by 100kΩ.
5	OUT2	**Motor driver output 2.** The OUT2 pin is connected to the mid-point of the internal N-channel MOSFET half-bridge.
6	OUT1	**Motor driver output 1.** The OUT1 pin is connected to the mid-point of the internal N-channel MOSFET half-bridge.

ABSOLUTE MAXIMUM RATINGS (1)

V_{CC}, PWM, FG/RD .....-0.3V to +38V
OUT1/2 .....-0.3V to V_{CC} + 0.3V
Junction temperature (T_J) .....150°C
Lead temperature .....260°C
Continuous power dissipation (2)
TSOT23-6-SL 1.25W

ESD Ratings

Human body model (HBM) ..... ±2kV
Charged-device model (CDM)..... ....±2kV

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) .....3.5V to 35V
Operating junction temp (T_J).... -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

TSOT23-6-SL ..... 100 ..... 55... °C/W

Notes:

1) Absolute maximum ratings are rated under room temperature, unless otherwise noted. Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can produce an excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on a JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

V_{CC} = 24V, T_J = -40°C to 125°C, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
VCC voltage (V_{CC}) under-voltage lockout (UVLO) rising threshold	V_{UVLO_R}			3.1	3.4	V
V_{CC} UVLO hysteresis	V_{UVLO_HYS}			0.4		V
Operating supply current	I_{CC}	PWM = high		5	7	mA
Stand-by current	I_{STD}	PWM = low		130		μA
Pulse-width modulation (PWM) input high threshold	V_{PWM_H}		2.2			V
PWM input low threshold	V_{PWM_L}				0.8	V
DC input high threshold	V_{DC_H}		2.7	3	3.3	V
DC input low threshold	V_{DC_L}			130		mV
PWM internal pull-up resistance	R_{PWM}			100		kΩ
FG/RD output low level	V_{FG_L}	$I_{FG/RD}$ = 3mA		0.3	0.43	V
Switching frequency	f_{SW}	T_J = 25°C	23.28	24	24.72	kHz
High-side MOSFET (HS-FET) on resistance	R_{HS_ON}	I_{OUT} = 100mA		480		mΩ
Low-side MOSFET (LS-FET) on resistance	R_{LS_ON}	I_{OUT} = 100mA		480		mΩ
Cycle-by-cycle current limit	I_{OCP}	OCP_SEL = 1		1.2		A
Peak current limit	I_{LIM}			1.8		A
Zero-current detection (ZCD) threshold	I_{ZCD}		-5		+5	mA
Soft-on commutation angle	θ_{SON}	SON = 0x10		46.4		°
Soft-off commutation angle	θ_{SOFF}	SOFF = 0x10		46.4		°
Hall lead/lag angle	θ_{HAL}	HAL_ANG = 0xF		21.8		°
Locked-rotor detection time	t_{RD}			0.6		s
Locked-rotor retry time	t_{RE}	LOCK_SEL = 0		3.6		s
Over-voltage protection (OVP) threshold	V_{OVP_H}	OVP_DIS = 0, OVP_H = 1	28	31	34	V
	V_{OVP_L}	OVP_DIS = 0, OVP_H = 0	17	19	21	V
OVP hysteresis	V_{OVP_HYS}			2	3	V
Operating point	B_{OP}			1	2	mT
Release point	B_{RP}		-2	-1		mT
Thermal shutdown threshold	T_{ST}			170		°C
Thermal shutdown hysteresis	T_{ST_HYS}			25		°C

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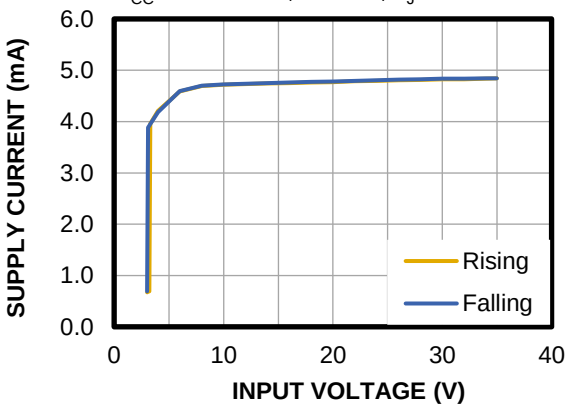
TYPICAL CHARACTERISTICS

V_{CC} = 24V, T_J = -40°C to +125°C, unless otherwise noted.

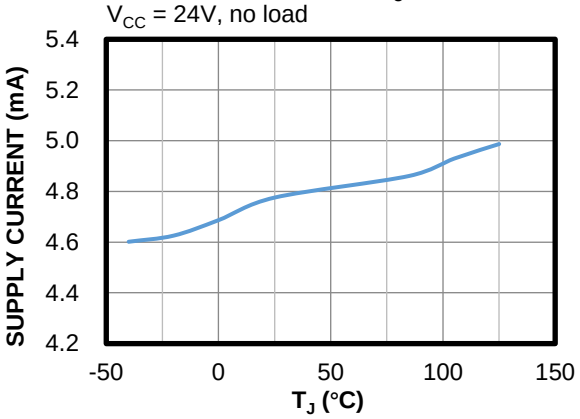
Supply Current vs. Input Voltage

V_{CC} = 3V to 35V, no load, T_J = 25°C

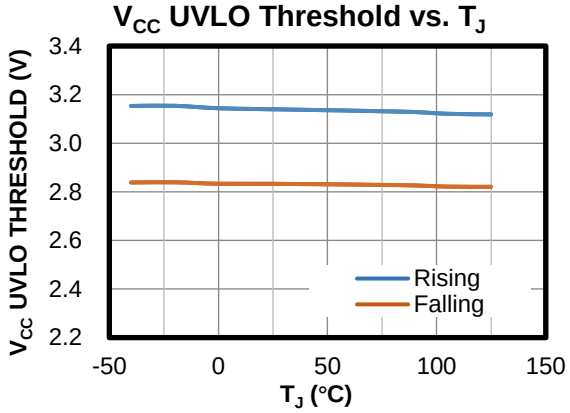


Supply Current vs. T_J

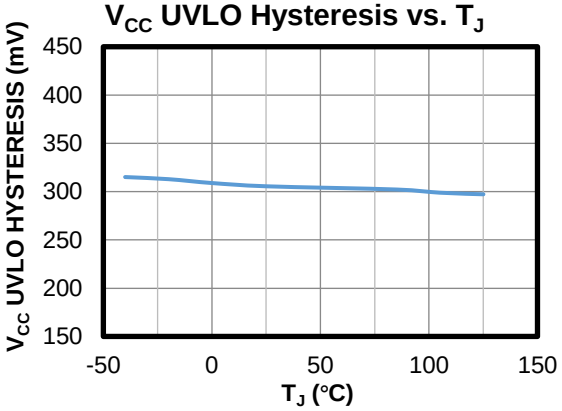
V_{CC} = 24V, no load



V_{CC} UVLO Threshold vs. T_J

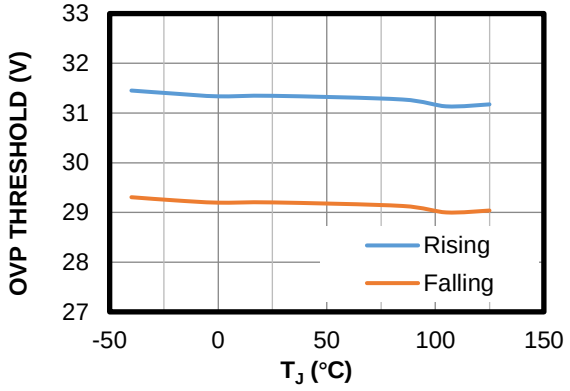


V_{CC} UVLO Hysteresis vs. T_J



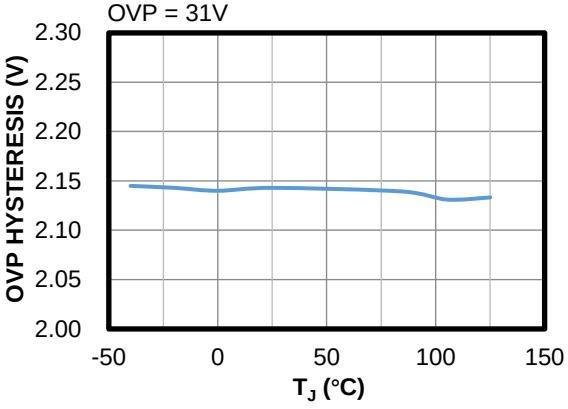
OVP Threshold vs. T_J

OVP = 31V



OVP Hysteresis vs. T_J

OVP = 31V



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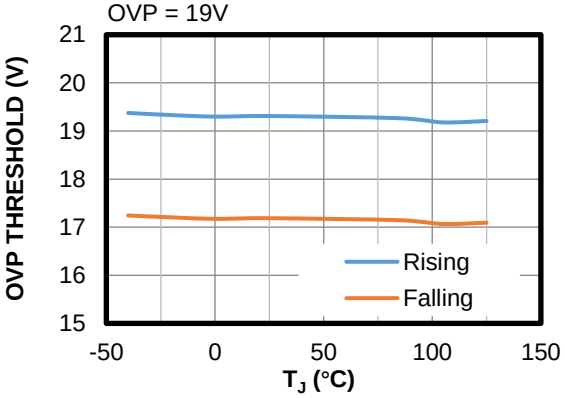
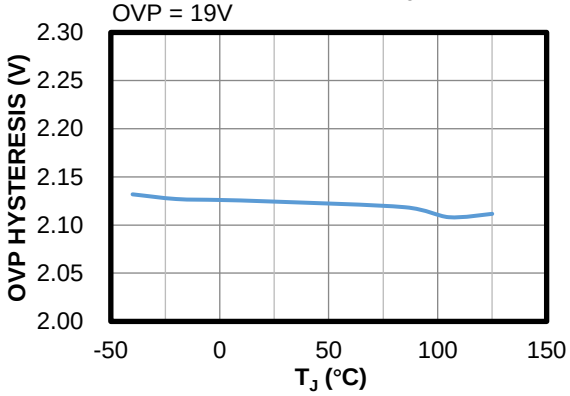
TYPICAL CHARACTERISTICS *(continued)*

V_{CC} = 24V, T_J = -40°C to +125°C, unless otherwise noted.

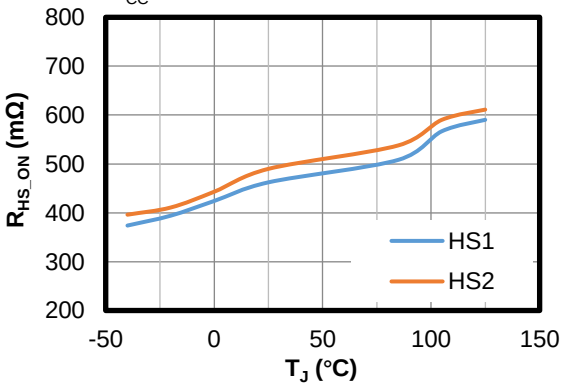
OVP Threshold vs. T_J



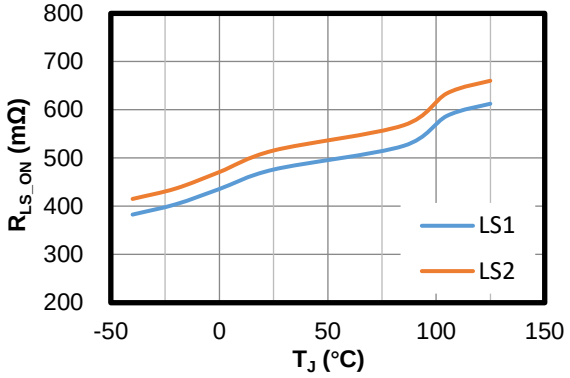
OVP Hysteresis vs. T_J



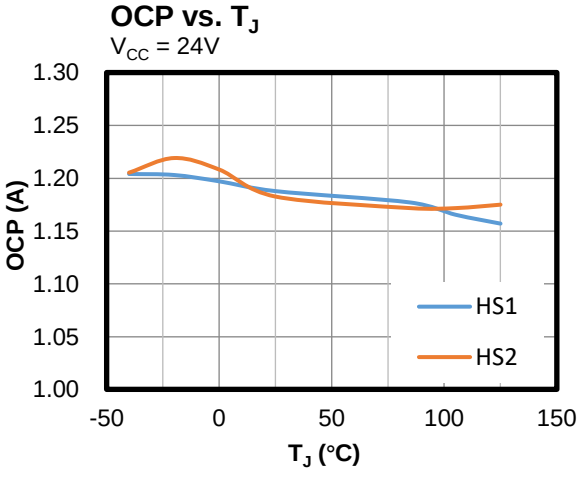
High-Side MOSFET On Resistance vs. T_J



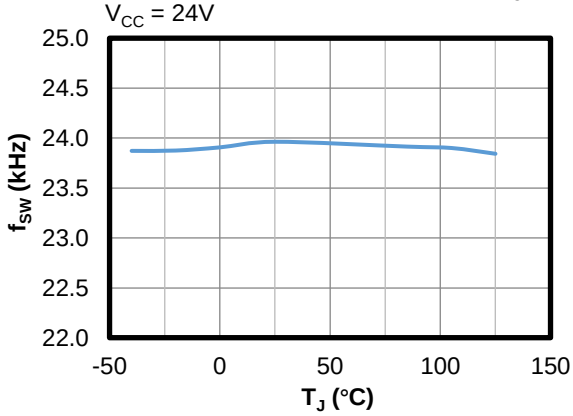
Low-Side MOSFET On Resistance vs. T_J



OCP vs. T_J



PWM Output Frequency vs. T_J



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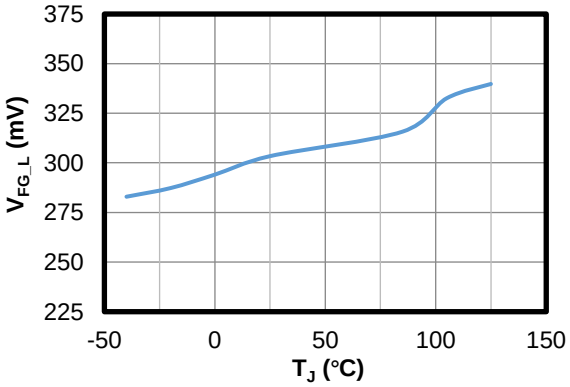
TYPICAL CHARACTERISTICS *(continued)*

V_{CC} = 24V, T_J = -40°C to +125°C, unless otherwise noted.

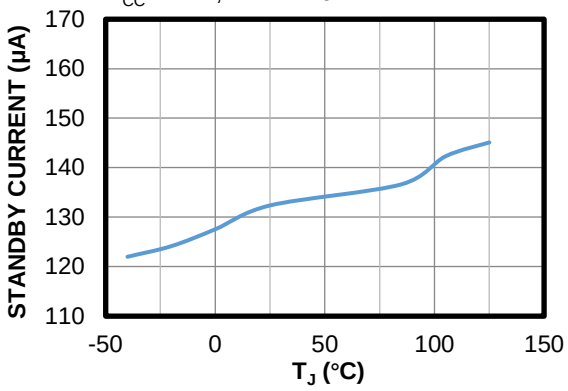
V_{FG_L} vs. T_J

V_{CC} = 24V, $I_{FG/RD}$ = 3mA



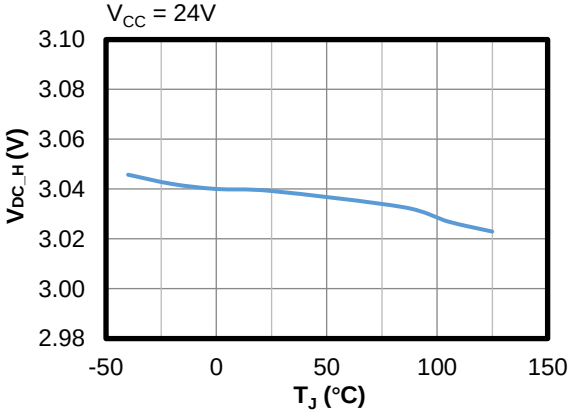
Standby Current vs. T_J

V_{CC} = 24V, PWM = low



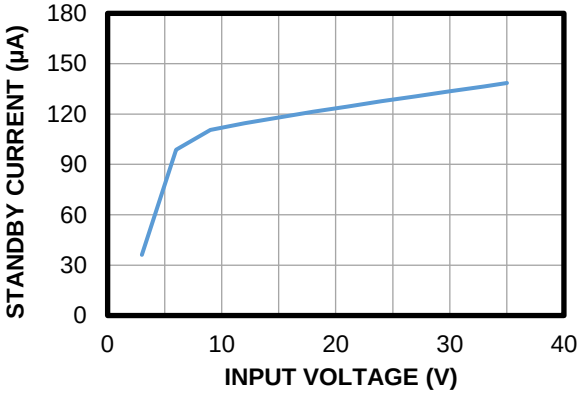
DC Input High Threshold Vs. T_J

V_{CC} = 24V



Standby Current vs. Input Voltage

V_{CC} = 3V to 35V, PWM = low, T_J = 25°C



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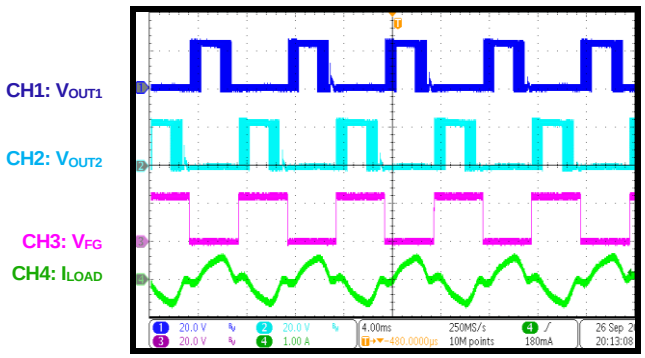
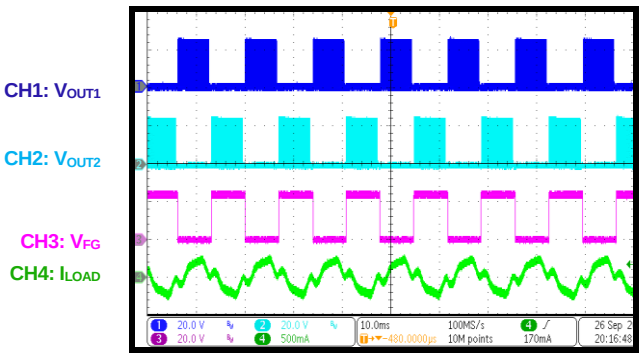
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 24V, 8038 axial fan, 250mA, 4000rpm, T_A = 25°C, unless otherwise noted.

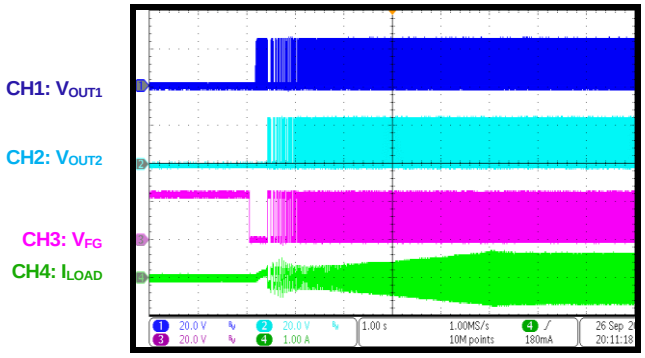
Steady State
PWM duty cycle = 100%



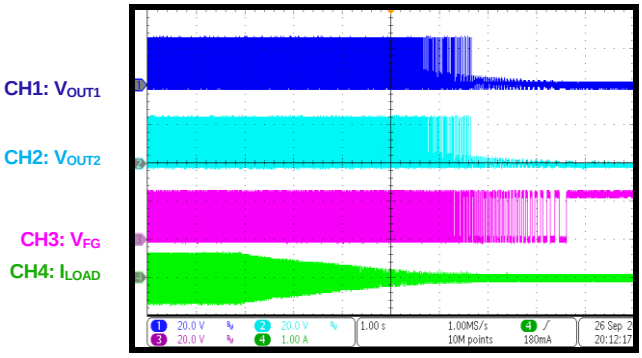
Steady State
PWM duty cycle = 50%



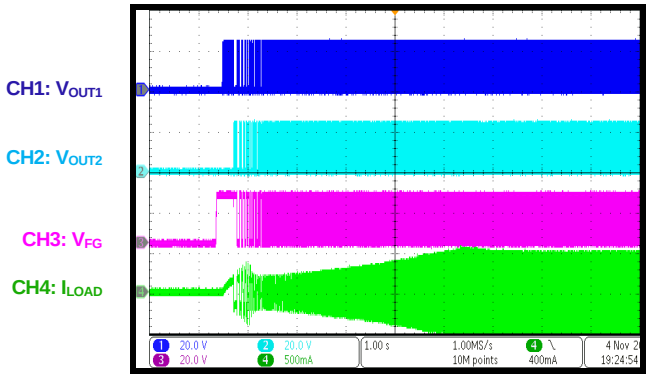
PWM On
PWM duty cycle = 0% to 100%



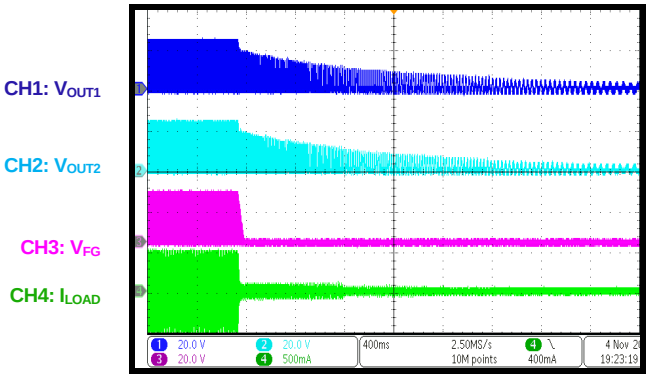
PWM Off
PWM duty cycle= 100% to 0%



Start-Up through VCC
VCC power plugged in



Shutdown through VCC
VCC power not plugged in



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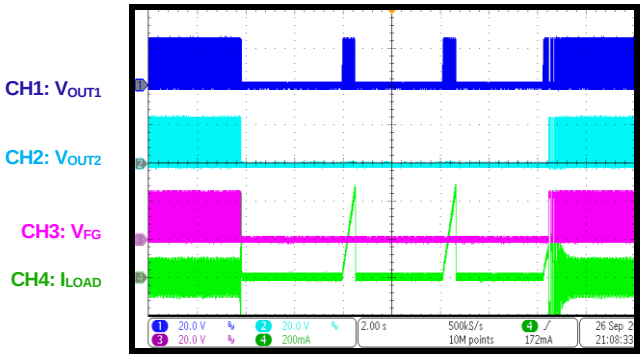
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 24V, 8038 axial fan, 250mA, 4000rpm, T_A = 25°C, unless otherwise noted.

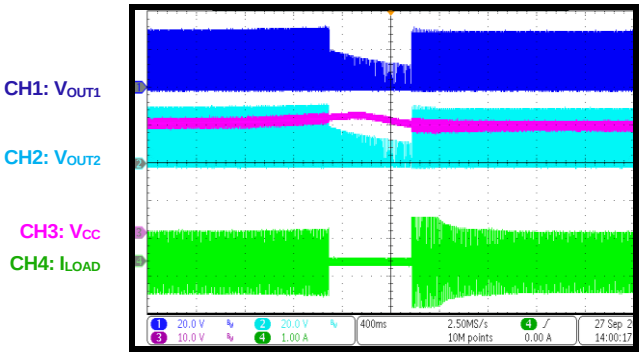
Locked-Rotor Protection

PWM duty cycle = 50%, locked rotor



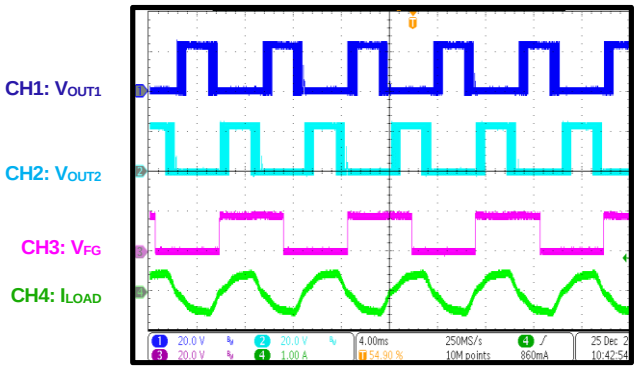
Over-Voltage Protection

VCC ramps up then ramps down,
OVP threshold = 31V



Steady State

2/3FG_EN = 1, PWM duty cycle = 100%



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FUNCTIONAL BLOCK DIAGRAM

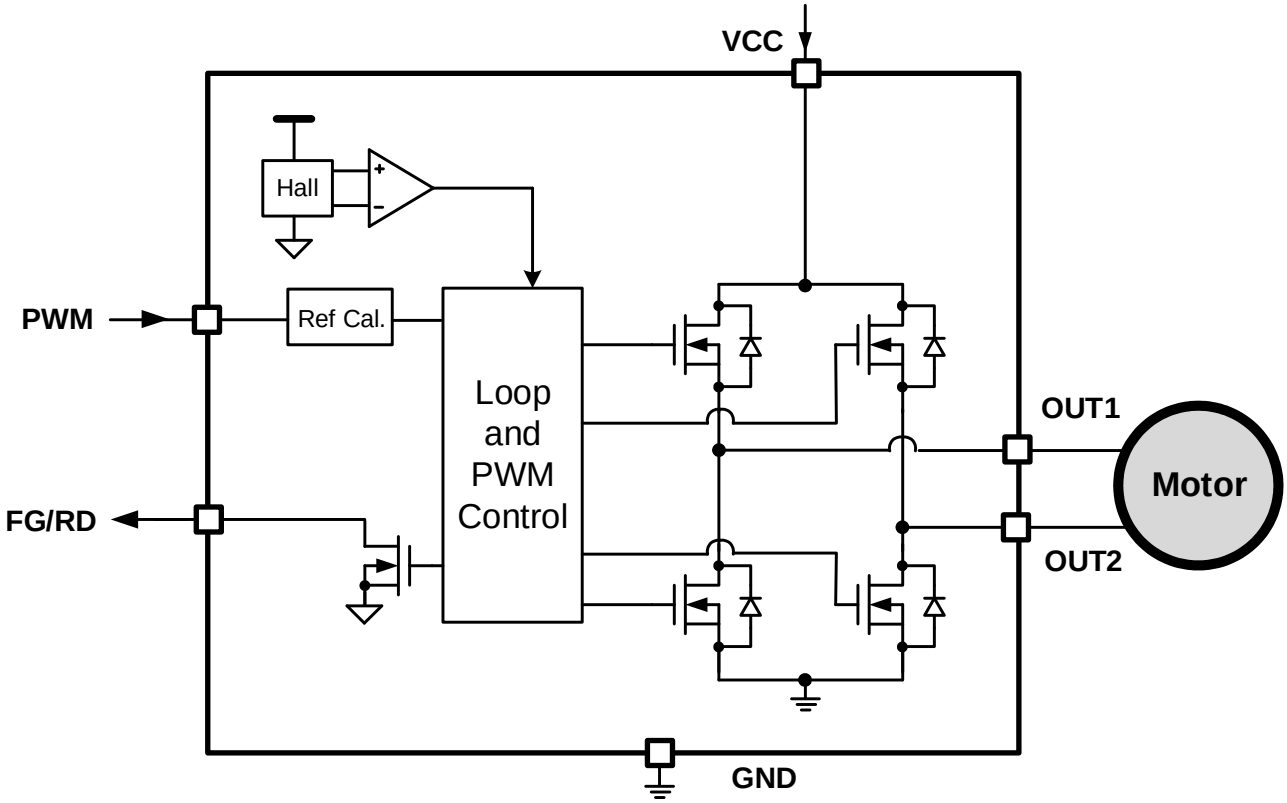

Figure 1: Functional Block Diagram

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OPERATION

The MP6653B is a single-phase brushless DC (BLDC) motor driver with integrated power MOSFETs and a Hall-effect sensor. The device controls the motor speed through the pulse-width modulation (PWM) signal or DC voltage on the PWM pin in either open-loop or closed-loop speed control. It features configurable soft on/off commutation. The Hall angle offset angle can be configured to flexibly optimize performance.

The MP6653B also provides rotational speed detection. The rotational speed detector (the FG/RD pin) is an open drain that outputs a high or low voltage relative to the internal Hall comparator's output.

Rich protection includes input over-voltage protection (OVP), under-voltage lockout (UVLO), locked-rotor protection, over-current protection (OCP), and thermal shutdown protection.

Speed Control

The PWM signal or DC voltage applied on the PWM pin controls the fan's rotating speed, as determined via the internal register bit (PWM_DC).

In PWM input mode, the input PWM duty cycle is detected, and the rotating speed is controlled by the input PWM duty cycle.

In DC input mode, the input DC voltage is converted to a PWM duty cycle that controls the rotating speed. There may be some shifts in the DC input threshold that affect the speed control accuracy in DC input mode.

By default, the PWM signal is selected. A wide 50Hz to 100kHz PWM frequency range is supported via the LOW_F bit.

- If LOW_F = 0, the PWM frequency ranges between 1kHz and 100kHz. The PWM signal's resolution is 163ns.
- If LOW_F = 1, the PWM frequency ranges between 50Hz and 2kHz. The PWM signal's resolution is 2.6μs.

The MP6653B provides open-loop and closed-loop speed control, as configured via the CLOSE bit.

In open-loop speed control, the output duty cycle of OUT1 and OUT2 are adjusted based on the input PWM duty cycle or input DC voltage on the PWM pin.

In closed-loop speed control, the input PWM duty cycle or input DC voltage is detected then converted to a reference speed. The motor's rotating speed is fed back to the control loop, and the output duty cycle is adjusted by the control loop to make the rotating speed equal to the reference speed.

Starting Duty Cycle

The D0[6:0] bits set the starting duty cycle. When the input duty cycle is below the starting duty cycle, there are two available responses, as selected via the SPD_ZERO bit:

- If SPD_ZERO = 0, OUT1/OUT2 maintains the minimum output duty cycle, or the fan maintains the minimum speed set via the S0[7:0] bits when the input duty cycle is below starting duty cycle.
- If SPD_ZERO = 1, there is no switching and the fan stops when the input duty cycle is below the starting duty cycle.

Figure 2 shows the minimum speed of the starting duty cycle.

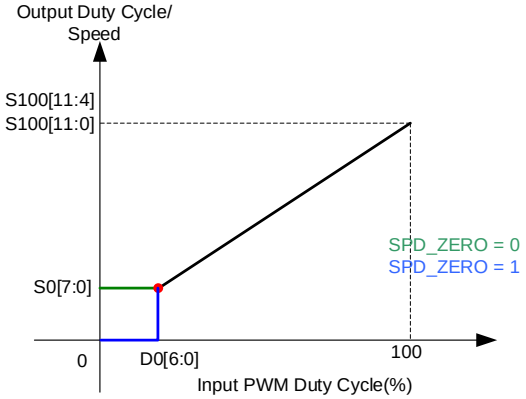

Figure 2: Minimum Speed with SPD_ZERO Setting

Stop Duty Cycle

The MP6653B stops the fan when the input PWM duty cycle exceeds the stop duty cycle (see Figure 3 on page 12).

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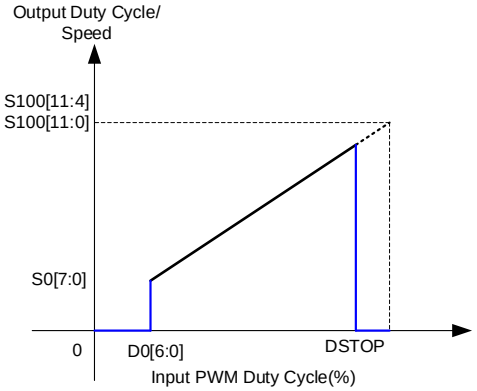

Figure 3: Stop at High Duty Cycle

The DSTOP[1:0] bits configure the stop duty cycle:

- If DSTOP[1:0] = 00, there are no stops.
- If DSTOP[1:0] = 01, the stop duty cycle is 100%.
- If DSTOP[1:0] = 10, the stop duty cycle is 95%.
- If DSTOP[1:0] = 11, the stop duty cycle is 90%.

OUT1/OUT2 Normal Operation

During steady-state operation, the MP6653B controls the H-bridge MOSFET's switching based on the internal Hall sensor's output to reduce speed variation and increase system efficiency (see Figure 4).

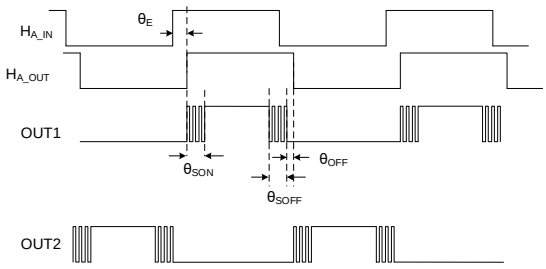

Figure 4: Operation with Hall Offset Angle

The operation sequence is based on the Hall signal coming from the embedded Hall sensor. H_{A_IN} is the original Hall from the embedded Hall. H_{A_OUT} is generated based on H_{A_IN} with a phase shift, and the shifted phase (θ_E) is configured via the HAL_ANG[3:0] bits.

If the H_{A_OUT} signal is high, OUT2 remains low constantly while OUT1 switches phases. If the H_{A_OUT} signal is low, OUT1 remains low constantly while OUT2 switches phases. The Hall offset angle is dependent on the following factors:

- The Hall offset angle is set via the HAL_ANG[3:0] bits.
- The Hall offset angle leading/lag direction is set via the HAL_FLAG bit.
- If HAL_ANG[3:0] = 0000, the Hall offset angle is 0.

Soft-On Commutation Section:

During soft-on commutation (denoted as θ_{SON} in Figure 4), the switching phase's output duty cycle gradually increases from 0 to the target duty cycle, and the other phase keeps the low-side MOSFETs (LS-FETs) on.

The SON[4:0] bits set the soft-on commutation angle, which is between 0° and 90°. Note that the high soft-on commutation angle leads to a lower rotation speed under the same conditions.

Soft-Off Commutation

During soft-off commutation (denoted as θ_{SOFF} in Figure 4), the switching phase's output duty cycle gradually decreases from the target duty cycle to 0, and the other phase keeps the LS-FETs on.

The SOFF[4:0] bits set the soft-off commutation angle, which ranges between 0° and 90°. Note that the larger soft-off commutation angle helps to eliminate the reverse current, but it also leads to a lower rotation speed under the same conditions.

Soft-On/Off Commutation Angle Linear Interpolation

The soft-on/off commutation angle can be set to linearly change when the output duty cycle varies. The SON[4:0] and SOFF[4:0] bits set the soft-on and soft-off commutation angle when the output duty cycle is 100%. The commutation angle linearly increases to 90° when the output duty cycle decreases to 0 (see Figure 5 on page 13).

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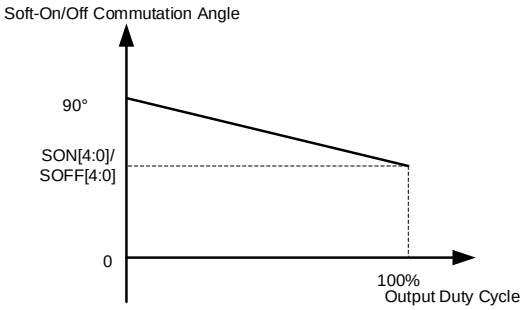

Figure 5 Soft-On/Off Commutation Angle Linear Interpolation

Curve Configurations

The MP6653B provides curve configurations. The input duty cycle and output duty cycle or speed can be configured depending on whether open-loop control or closed-loop control is selected.

There are four available configuration points, including the starting duty cycle (D0[6:0]) and 100% input duty cycle (see Figure 6).

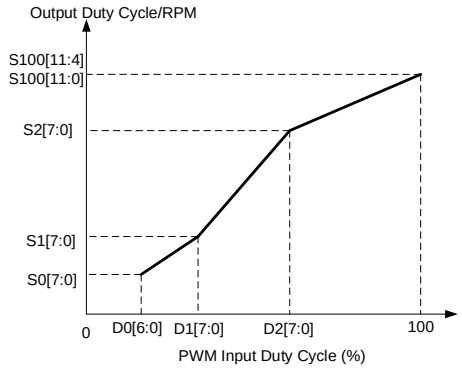

Figure 6: Curve Configuration

The starting duty cycle can be calculated with Equation (1):

$$\text{Starting Duty Cycle} = D0[6:0] / 255 \quad (1)$$

The input duty cycle is set via Dx[7:0] (where x = 1 or 2). The input duty cycle can be estimated with Equation (2):

$$\text{Input Duty Cycle} = Dx[7:0] / 255 \quad (2)$$

In open-loop speed control, the corresponding output duty cycle is set via Sx[7:0] (where x = 0, 1, 2, or 100). The output duty cycle can be calculated with Equation (3):

$$\text{Output Duty Cycle} = Sx[7:0] / 255 \quad (3)$$

In closed-loop speed control, S100[11:0] sets the maximum speed when the input duty cycle is 100%. In this scenario, the speed can be estimated with Equation (4):

$$\text{Speed (rpm)} = S100[11:0] \times 16 \quad (4)$$

When the electrical speed is set via Sx[7:0], then it can be calculated with Equation (5):

$$\text{Speed (rpm)} = Sx[7:0] / 255 \times S100[11:0] \times 16 \ (x = 0, 1, 2) \quad (5)$$

Standby Mode

The MP6653B is in standby mode if the VCC voltage (V_{CC}) exceeds its under-voltage lockout (UVLO) rising threshold and the PWM pin stays low. The MP6653B exits standby mode when the PWM input signal is high or power is recycled. Standby mode can be disabled via the STB_DIS bit.

Pre Start-Up

Once the input voltage (V_{IN}) exceeds the UVLO threshold or the input PWM duty exceeds the starting duty set via D0[6:0], the MP6653B first enters the pre start-up stage. The output duty cycle increases with a set slope by ignoring the final steady-state output duty cycle. After several Hall cycles, the MP6653B exits pre start-up and enters soft start (SS).

With different pre start-up timer configurations, the MP6653B can provide sufficient torque to spin up the motor.

Soft Start (SS)

After the pre start-up stage, SS is employed. The output duty cycle ramps up/down step-by-step following the TIME_SS[1:0] bits.

To reduce the input inrush current during start-up, several configurations are available to meet different application requirements. The dropping duty cycle can be configured to 1x or 2x that of TIME_SS[1:0].

Rotor Speed Indicator (FG) or Locked-Rotor Indicator (RD)

The speed indicator or locked-rotor indicator can be output on the FG/RD pin with different configurations.

The FGRD[2:0] bits set the FG/RD pin's output. In addition, a 2/3 x FG output can be configured via the 2/3FG_EN bit.

- If 2/3FG_EN = 0 and FGRD[2:0] = 000: 1x. The FG/RD pin outputs 1 pulse in every electrical cycle.

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- If 2/3FG_EN = 0 and FGRD[2:0] = 001: 1/2x. The FG/RD pin outputs 1 pulse in every 2 electrical cycles.
- If 2/3FG_EN = 0 and FGRD[2:0] = 010: 2x. The FG/RD pin outputs 2 pulses in every electrical cycle.
- If 2/3FG_EN = 0 and FGRD[2:0] = 011: The FG/RD pin outputs 1 pulse in every electrical cycle under normal operation and outputs an RD signal for locked-rotor protection. The RD signal output polarity is set via the RD_H_L bit.
- If 2/3FG_EN = 0 and FGRD[2:0] = 100: The FG/RD pin is set as the locked-rotor (RD) indicator. The RD signal output polarity is set via the RD_H_L bit.
- If 2/3FG_EN = 0 and FGRD[2:0] = 101: The FG/RD pin is set to be a fault indicator, and it outputs a signal if short-circuit protection (SCP), thermal shutdown (TSD), over-voltage protection (OVP), or RD is detected.
- If 2/3FG_EN = 0 and FGRD[2:0] = 110: The FG/RD pin is set as an external Hall signal input. The external Hall sensor replaces the internal Hall sensor for operation.
- If 2/3FG_EN = 1: The FG/RD pin outputs 2 pulses in 3 electrical cycles and ignores the FGRD[2:0] configuration.

Protection Circuits

The MP6653B is fully protected against over-voltage (OV), under-voltage (UV), over-current (OC), and over-temperature (OT) events.

Cycle-by-Cycle Current Limit (OCP)

During normal switching, if the current flowing through the high-side MOSFET (HS-FET) of the H-bridge exceeds the threshold set via the OCP_SEL bit after a blanking time, the HS-FET turns off. The HS-FET resumes switching in the next switching cycle. The OCP threshold can be set to 0.6A or 1.2A via the register.

Peak Current Limit (SCP)

If the current is not limited by the cycle-by-cycle limit, there is also a peak current limit. If the device reaches the peak current limit threshold (typically 1.8A), all MOSFETs turn off and resume operation after a locked retry time.

Thermal Shutdown (TSD)

The MP6653B integrates thermal monitoring. If the temperature exceeds 170°C, the MOSFETs of the switching half-bridge turn off. Once the die temperature has fallen to a safe level, operation automatically resumes.

Under-Voltage Lockout (UVLO)

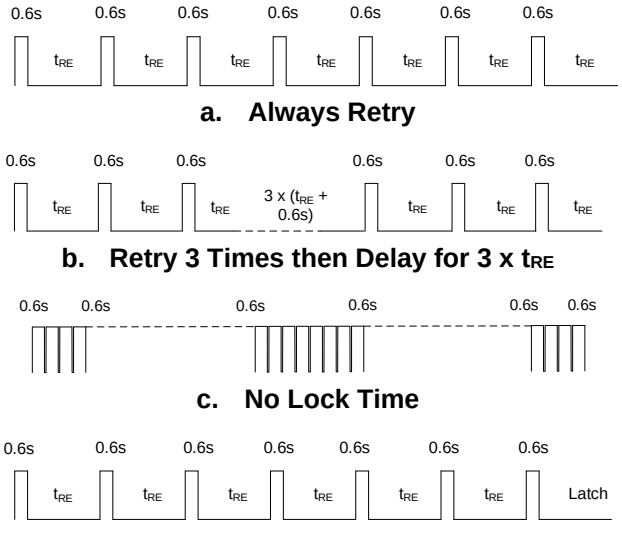
If V_{CC} falls below the UVLO falling threshold, all circuitry in the device is disabled and the internal logic is reset. Operation resumes when V_{CC} exceeds the UVLO rising threshold.

Locked-Rotor Protection (RD)

The internal Hall signal is detected to determine whether locked-rotor protection is triggered. If no Hall signal edge is detected during the 0.6s detection time, the locked-rotor protection is triggered, and the LS-FETs of the H-bridge are turn on. After a locked retry time set via the LOCK_SEL bit, the IC automatically retries starting up. This retry time can be set to 3.6s or 8.4s.

The MP6653B also supports no lock time or an option to retry several times; the lock-retry time can be set to a longer duration via the LOCK_BHV[1:0] configuration.

Figure 7 shows the protection options.



a. Always Retry

b. Retry 3 Times then Delay for 3 x t_{RE}

c. No Lock Time

d. Latch After 7 Retry Times

Figure 7: Lock Protection and Retry Time

The FG/RD pin releases only after 3 Hall signal edges are detected and the after locked-rotor condition is released.

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Over-Voltage Protection (OVP)

The MP6653B employs two OVP thresholds for different applications

If V_{CC} exceeds its OV threshold (19V/31V), the OUT1/2 output is disabled.

The device resumes normal operation when V_{CC} drops below the OVP threshold falling (17V/28V) and the Hall edge is detected in an OVP interval.

Fault Diagnostics

If a fault is triggered, the corresponding fault bit (OCP, SCP, TSD, OVP, and RD) is set, and all fault bits can be read. The fault bit can be reset after the fault bit is read.

Test Mode and Factory Mode

To configure the internal register, the MP6653B has a test mode. In this test mode, all internal registers can be read/written. After the design is finalized, the register value can be configured to the non-volatile memory (NVM).

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REGISTER MAP

Add	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
00h (OTP/REG)	S0[7:0]							
01h (OTP/REG)	S1[7:0]							
02h (OTP/REG)	S2[7:0]							
03h (OTP/REG)	S100[11:4]							
04h (OTP/REG)	D1[7:0]							
05h (OTP/REG)	D2[7:0]							
06h (OTP/REG)	RD_H_L	D0[6:0]						
07h (OTP/REG)	OVP_H	FAST_DN	PWM_POL	SON[4:0]				
08h (OTP/REG)	SINE	SPD_SEL[1:0]		SOFF[4:0]				
09h (OTP/REG)	WAIT_DIS	T_PRE[1:0]		HAL_FLAG	HAL_ANG[3:0]			
0Ah (OTP/REG)	RESERVED	INT_EN	RESERVED	LOCK_SEL	OCP_SEL	ASYNC	PWM_WAIT	TADV_EN
0Bh (OTP/REG)	OVP_DIS	TADV[1:0]		TIME_SS[1:0]		FGRD[2:0]		
0Ch (OTP/REG)	PWM_DC	CLOSE	LOW_F	LOCK_BHV[1:0]		SPD_ZERO	COA_SLOW	DN_SCALE
0Dh (OTP/REG)	KI[6:0]							ZCD_POS
0Eh (OTP/REG)	FIX_ST[1:0]		DSTOP[1:0]		S100[3:0]			
0Fh (OTP/REG)	RESERVED		FG_FIX	2/3FG_EN	STB_DIS	RD_ALL	ZCD_DIS	RESERVED
14h (REG)	OCP	SCP	OVP	TSD	RD	RESERVED		
15h (REG)	RESERVED	LOCK_ DIS	RESERVED					
16h (REG)	RESERVED	OTP_PAGE[1:0]		RESERVED				

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SPEED_CURVE_S0 (00h)

The SPEED_CURVE_S0 command configures the output duty cycle or speed when the input pulse-width modulation (PWM) duty cycle is set via D0[6:0].

Bits	Access	Bit Name	Default	Description
7:0	R/W	S0[7:0]	0x20	Sets the output duty cycle or speed when the input PWM duty cycle is set via D0[6:0]. In open-loop control, these bits set the output duty cycle when the input PWM duty cycle is set via D0[6:0]. The output duty cycle can be calculated with the following equation: Output Duty Cycle = S0[7:0] / 256 In closed-loop control, these bits set the speed reference when the input PWM duty cycle is set via D0[6:0]. The electrical speed can be calculated with the following equation: Speed (rpm) = S0[7:0] / 256 x S100[11:0] x 16

SPEED_CURVE_S1 (01h)

The SPEED_CURVE_S1 command configures the output duty cycle or speed when the input PWM duty cycle is set via D1[7:0].

Bits	Access	Bit Name	Default	Description
7:0	R/W	S1[7:0]	0x60	Sets the output duty cycle or speed when the input PWM duty cycle is set via D1[7:0]. In open-loop control, these bits set the output duty cycle when the input PWM duty cycle is set via D1[7:0]. The output duty cycle can be calculated with the following equation: Output Duty Cycle = S1[7:0] / 256 In closed-loop control, these bits set the speed reference when the input PWM duty cycle is set via D1[7:0]. The electrical speed can be calculated with the following equation: Speed (rpm) = S1[7:0] / 256 x S100[11:0] x 16

SPEED_CURVE_S2 (02h)

The SPEED_CURVE_S2 command configures the output duty cycle or speed when the input PWM duty cycle is set via D2[7:0].

Bits	Access	Bit Name	Default	Description
7:0	R/W	S2[7:0]	0xC0	Sets the output duty cycle or speed when the input PWM duty cycle is set via D2[7:0]. In open-loop control, these bits set the output duty cycle when the input PWM duty cycle is set via D2[7:0]. The output duty cycle can be calculated with the following equation: Output Duty Cycle = S2[7:0] / 256 In closed-loop control, these bits set the speed reference when the input PWM duty cycle is set via D2[7:0]. The electrical speed can be calculated with the following equation: Speed (rpm) = S2[7:0] / 256 x S100[11:0] x 16

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SPEED_CURVE_S100 (03h)

The SPEED_CURVE_S100 command configures the output duty cycle or speed when the input PWM duty cycle is 100%.

Bits	Access	Bit Name	Default	Description
7:0	R/W	S100[11:4]	0xFF	Sets the output duty cycle or the 8 most significant bits (MSB) for the speed when the input PWM duty cycle is 100%. Open-loop control sets the output duty cycle when the input PWM duty cycle is 100%. The output duty cycle can be calculated with the following equation: Output Duty Cycle = S100[11:4] / 256 Closed-loop control sets the maximum speed reference when the input PWM duty cycle is 100%. Combined with S100[3:0], the maximum electrical speed can be calculated with the following equation: Max Speed (rpm) = S100[11:0] × 16

SPEED_CURVE_D1 (04h)

The SPEED_CURVE_D1 command configures the input duty cycle 1 (D1).

Bits	Access	Bit Name	Default	Description
7:0	R/W	D1[7:0]	0x60	Sets the input duty cycle for curve configurations. The input PWM duty cycle can be calculated with the following equation: Input PWM Duty Cycle = D1[7:0] / 256

SPEED_CURVE_D2 (05h)

The SPEED_CURVE_D2 command configures the input duty cycle 2 (D2).

Bits	Access	Bit Name	Default	Description
7:0	R/W	D2[7:0]	0xC0	Sets the input duty cycle for curve configurations. The input PWM duty cycle can be calculated with the following equation: Input PWM Duty Cycle = D2[7:0] / 256

RD_D0 (06h)

The RD_D0 command sets the RD signal/fault signal (RD/FT) output polarity and the starting corner duty cycle.

Bits	Access	Bit Name	Default	Description
7	R/W	RD_H_L	0	Selects RD/FT output polarity. 0: The output is low if a protection is triggered (default) 1: The output is high if a protection is triggered
6:0	R/W	D0[6:0]	0x20	Sets the starting corner duty cycle for curve configuration. The starting corner PWM duty cycle can be calculated with the following equation: Starting Duty Cycle = D0[6:0] / 256

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CFR_1 (07h)

The CFR_1 command controls the function register 1, which sets the over-voltage protection (OVP) threshold, fast-off, input PWM polarity, and soft-on commutation angle.

Bits	Access	Bit Name	Default	Description
7	R/W	OVP_H	1	Selects the OVP threshold. 0: 19V 1: 31V (default)
6	R/W	FAST_DN	0	Enables fast-off. 0: Disables fast-off (default) 1: Enables fast-off when PWM is off. The IC quickly stops switching if the input duty cycle drops below the starting duty cycle
5	R/W	PWM_POL	0	Selects the input PWM polarity. 0: Positive duty cycle (default) 1: Negative duty cycle
4:0	R/W	SON[4:0]	0x10	Sets the soft-on commutation angle. 2.9° per step. 00000: 2.9° 00001: 5.8° 11111: 90° The soft-on commutation angle can be calculated with the following equation: Soft-On Angle = (SON[4:0] + 1) x 2.9°

SOFF_CLK (08h)

The SOFF_CLK command configures the soft-on and soft-off mode, digital clock, and soft-off commutation angle.

Bits	Access	Bit Name	Default	Description
7	R/W	SINE	0	Selects soft-on and soft-off mode. 0: Linear (default) 1: Sine
6:5	R/W	SPD_SEL[1:0]	00	Selects the digital clock. A higher frequency can result in a higher calculation resolution. However, it also leads to a higher minimum speed. The bits below indicate the supported minimum electrical speeds: 00: 200rpm (default electrical speed) 01: 800rpm 10: 1600rpm 11: 3200rpm
4:0	R/W	SOFF[4:0]	0x10	Sets the soft-off commutation angle. 2.9° per step. 00000: 2.9° 00001: 5.8° 11111: 90° The soft-off commutation angle can be calculated with the following equation: Soft-Off Angle = (SOFF[4:0] + 1) x 2.9°

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CFR_2 (09h)

The CFR_2 command controls function register 2, which sets the waiting function, pre start-up time, and Hall offset angle.

Bits	Access	Bit Name	Default	Description
7	R/W	WAIT_DIS	0	Disables the waiting function at start-up. 0: Enabled (default) 1: Disabled
6:5	R/W	T_PRE[1:0]	01	Selects the pre start-up time. 00: 21.33ms/step 01: 10.67ms/step (default) 10: 5.36ms/step 11: 2.73ms/step
4	R/W	HAL_FLAG	0	Sets the Hall offset angle lag/lead. 0: Lag (default) 1: Lead
3:0	R/W	HAL_ANG[3:0]	0000	Sets the Hall offset angle. 1.4° per step. 0000: 0° (default) 0001: 1.4° 1111: 21° The Hall offset angle can be calculated with the following equation: Hall Offset Angle = HAL_ANG[3:0] x 1.4°

CFR_3 (0Ah)

The CFR_3 command controls function register 3, which sets the soft-on and soft-off angle, lock-retry time, current limit, asynchronized rectification, waiting function, and advanced turn-off.

Bits	Access	Bit Name	Default	Description
7	R	RESERVED	0	Reserved.
6	R/W	INT_EN	0	Enables soft-on and soft-off commutation angle linear interpolation. 0: Disable the soft-on/soft-off commutation angle, which linearly increases to 90° when the duty cycle drops (default) 1: Enable the soft-on/soft-off commutation angle, which linearly increases to 90° when the duty cycle drops
5	R	RESERVED	1	Reserved.
4	R/W	LOCK_SEL	0	Sets the locked-rotor protection retry time. 0: 3.6s (default) 1: 8.4s
3	R/W	OCP_SEL	1	Sets the current limit threshold. 0: 0.6A 1: 1.2A (default)
2	R/W	ASYNC	0	Enables asynchronized rectification. 0: Disabled (default) 1: Enabled
1	R/W	PWM_WAIT	0	Enables the waiting function at PWM on start-up. 0: Disabled (default) 1: Enabled

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0	R/W	TADV_EN	1	Enables advanced turn-off. 0: Disables advanced turn-off 1: Enables advanced turn-off (default)

CFR_4 (0Bh)

The CFR_4 command controls function register 4, which sets over-voltage protection (OVP), advanced soft-off angle, soft-start time (t_{SS}), and the FG/RD pin.

Bits	Access	Bit Name	Default	Description
7	R/W	OVP_DIS	0	Enables OVP. 0: Enables OVP (default) 1: Disables OVP
6:5	R/W	TADV[1:0]	00	Selects the advanced off angle. 00: Automatic (default) 01: 5.6° 10: 11.2° 11: 22.5°
4:3	R/W	TIME_SS[1:0]	01	Selects t_{SS}, the time during which the output duty cycle transitions from 0% to 100%. 00: 2.73s 01: 5.46s (default) 10: 8.19s 11: 1.36s
2:0	R/W	FGRD[2:0]	000	Selects the FG/RD pin's function when 2/3FG_EN = 0. 000: 1 x FG (default) 001: 1/2 x FG 010: 2 x FG 011: FG + RD where the FG signal is the output during normal operation, and the RD signal is the output if locked-rotor protection is detected 100: RD where the RD signal polarity is set via the RD_H_L bit 101: FT where the fault signal is the output if a fault is detected, and the FT polarity is set via the RD_H_L bit 110: HALL_IN where the FG/RD pin is set as the external Hall input pin

CFR_5 (0Ch)

The CFR_5 command controls function register 5, which sets the PWM/DC input, closed-loop and open-loop speed control, PWM frequency, deadlock protection mode, coasting down threshold, zero-speed, and output duty cycle ramping down scale.

Bits	Access	Bit Name	Default	Description
7	R/W	PWM_DC	0	Selects the DC input or PWM input for the PWM/DC pin. 0: PWM input (default) 1: DC input
6	R/W	CLOSE	0	Enables closed-loop speed control. 0: Open-loop speed control (default) 1: Closed-loop speed control

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5	R/W	LOW_F	0	Selects the PWM input frequency mode. 0: The high frequency is selected between 1kHz and 100kHz (default) 1: The low frequency is selected between 50Hz and 2kHz
4:3	R/W	LOCK_BHV[1:0]	00	Selects deadlock protection mode. 00: Always retry (default) 01: Retries for 3 times, then the lock-retry time is t_{RE} + 3 x (t_{RE} + 0.6s) 10: No lock time 11: Retries for 7 times, then the device latches
2	R/W	SPD_ZERO	1	Enables zero speed. 0: Keep the minimum speed when the input duty cycle below the duty cycle set by D0[6:0] 1: Stop when the input duty cycle is below the duty cycle set via D0[6:0] (default)
1	R/W	COA_SLOW	0	Selects the coasting down speed threshold (electrical speed). The IC continues coasting until the fan rotation's coasting down speed drops below the speed threshold during start-up. 0: 1400rpm (default) 1: 700rpm
0	R/W	DN_SCALE	0	Selects the PWM output duty cycle ramping down scale as the output duty cycle drops from 100% to 0%. 0: 1 x TIME_SS[1:0] (default) 1: 2 x TIME_SS[1:0]

KI_ZCD (0Dh)

The KI_ZCD command sets the integral parameter for closed-loop speed control and the zero-current detection (ZCD) active angle position.

Bits	Access	Bit Name	Default	Description
7:1	R/W	KI[6:0]	0x10	Sets the integral parameter for closed-loop speed control.
0	R/W	ZCD_POS	0	Sets the ZCD active angle position. 0: ZCD is active once soft-on commutation ends (default) 1: ZCD is active after 90°

FIX_DSTOP_S100 (0Eh)

The FIX_DSTOP_S100 command sets the initial output duty cycle, stop input duty cycle, and maximum speed reference.

Bits	Access	Bit Name	Default	Description
7:6	R/W	FIX_ST[1:0]	00	Selects the initial output duty cycle at start-up. 00: The initial output duty cycle is 0% (default) 01: The initial output duty cycle is 12.5% 10: The initial output duty cycle is 25% 11: The initial output duty cycle is 50%
5:4	R/W	DSTOP[1:0]	00	Selects the stop input duty cycle. When the input PWM duty cycle is equal to or exceeds the selected stop input duty cycle, the IC stops switching. 00: Does not stop (default) 01: 100% 10: 95% 11: 90%

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3:0	R/W	S100[3:0]	0000	Sets the maximum speed reference when the input PWM duty cycle is 100% for closed-loop control. Combined with S100[11:4] (SPEED_CURVE_4 (03h), bits[7:0]), the maximum electrical speed can be calculated with the following equation: Max Speed (rpm) = S100[11:0] x 16

CFR_6 (0Fh)

The CFR_6 command controls function register 6, which sets the output of FG/RD pin, the standby mode and the zero-current detection (ZCD).

Bits	Access	Bit Name	Default	Description
7:6	R	RESERVED	00	Reserved.
5	R/W	FG_FIX	0	Enables FG signal is high when the IC is in pre-start stage or the IC stops switching. 0: Disabled(default) 1: Enabled
4	R/W	2/3FG_EN	0	Enables the 2/3 FG function. 0: The FG/RD pin's output depends on FGRD[2:0] (default) 1: The FG/RD pin outputs 2 pulses in three electrical cycle, ignoring the FGRD[2:0] configuration
3	R/W	STB_DIS	0	Disables standby mode. 0: Enables standby mode(default) 1: Disables standby mode
2	R/W	RD_ALL	0	Selects the cases where the FG/RD pin outputs an RD signal when FGRD[2:0] = 100. 0: FG/RD pin outputs RD signal when rotor dead lock(default) 1: FG/RD pin outputs RD signal when rotor dead lock or the fan stops because of the input PWM duty cycle or SCP.
1	R/W	ZCD_DIS	0	Disables zero-current detection. 0: Enables zero-current detection(default) 1: Disables zero-current detection
0	R	RESERVED	0	Reserved.

FAULT_BIT (14h)

The FAULT_BIT command indicates faults, including the cycle-by-cycle current limit (I_{OCP}), peak current limit (I_{LIMIT_PEAK}), input over-voltage (OV) conditions, thermal shutdown, and locked-rotor protection.

Bits	Access	Bit Name	Default	Description
7	R	OCP	0	Indicates an I_{OCP} fault. 0: I_{OCP} is not triggered 1: I_{OCP} is triggered
6	R	SCP	0	Indicates an I_{LIMIT_PEAK} fault. 0: I_{LIMIT_PEAK} is not triggered 1: I_{LIMIT_PEAK} is triggered
5	R	OVP	0	Indicates an input OV fault. 0: Input OVP is not triggered 1: Input OVP is triggered

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4	R	TSD	0	Indicates a thermal shutdown fault. 0: Thermal shutdown protection is not triggered 1: Thermal shutdown protection is triggered
3	R	RD	0	Indicates a locked-rotor fault. 0: Locked-rotor protection is not triggered 1: Locked-rotor protection is triggered
2:0	R	RESERVED	000	Reserved.

LOCK_DIS (15h)

The LOCK_DIS command enables locked-rotor protection.

Bits	Access	Bit Name	Default	Description
7	R	RESERVED	0	Reserved.
6	R/W	LOCK_DIS	0	Enables locked-rotor protection. 0: Enables locked-rotor protection 1: Disables locked-rotor protection
5:0	R	RESERVED	0x00	Reserved.

OTP_PAGE (16h)

The OTP_PAGE command indicates the one-time programmable (OTP) memory page.

Bits	Access	Bit Name	Default	Description
7	R	RESERVED	0	Reserved.
6:5	R	OTP_PAGE[1:0]	00	Indicates the OTP page. 00: No OTP page is configured 01: First OTP page is configured 10: Second OTP page is configured
4:0	R	RESERVED	0x00	Reserved.

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APPLICATION INFORMATION

Selecting the Input Capacitor

Place an input capacitor (C_{IN}) as close to the VCC and GND pins as possible to maintain a stable V_{IN} and reduce noise at the input. C_{IN} must have a low impedance at f_{SW}.

Ceramic capacitors with X7R dielectrics are recommended due to their low-ESR characteristics. The ceramic capacitance is dependent on the DC voltage rating. If the ceramic capacitor is biased to its DC voltage rating, then its capacitance drops below 50%.

Leave enough voltage rating margin when selecting the component. For most applications, a 1µF to 10µF ceramic capacitor is sufficient.

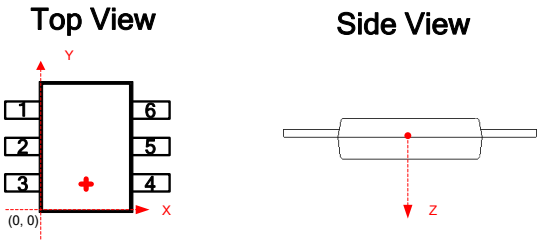
In some applications, an additional large, electrolytic capacitor may be required to absorb the motor's energy.

Selecting the Input Snubber

Due to the C_{IN} energy charge/discharge during phase commutation, the input current (I_{IN}) has switching cycle ringing. If necessary, place an RC snubber (a 2Ω resistor in series with a 1µF capacitor) in parallel with C_{IN}. This effectively prevents switching cycle ringing.

Hall Position

Figure 8 shows the embedded Hall sensor's cell location.



(X, Y, Z) = (800µm, 481µm, 80µm)

Figure 8: Hall Sensor Position

Selecting an Input Clamping Circuit

A voltage-clamping circuit may be required to prevent V_{IN} from being charged by the energy stored in the motor. Typically, a 15V SOD-123 Zener diode or TVS diode is sufficient for most 12V applications, and a 28V SOD-123 Zener diode or TVS diode is typically sufficient for most 24V applications. Higher clamping voltages can be used if a higher V_{IN} range is applied.

Selecting the Reverse Blocking Diode

To prevent damage if the fan experiences a reverse plug-in, or a reverse voltage applied on input terminal, a reverse blocking diode is required. The reverse blocking diode prevents the bus voltage from charging via the fan's reverse current.

The blocking diode's reverse voltage rating must exceed the maximum operating voltage under all conditions.

System-Level ESD

Some fan products must pass system-level ESD testing. System-level ESD follows the IEC61000-4-2 standard. There are differences between human body mode (HBM) ESD and system-level ESD (IEC 61000-4-2). Figure 9 shows the equivalent circuit of a HBM ESD circuit.

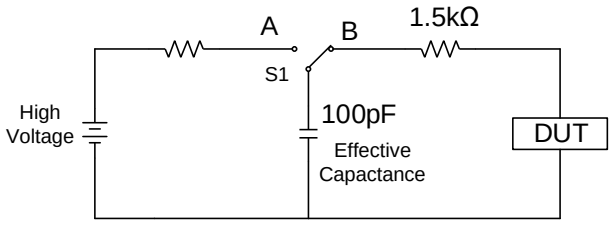


Figure 9: Equivalent Circuit of HBM ESD Circuit

Figure 10 shows the equivalent circuit of a system-level ESD circuit.

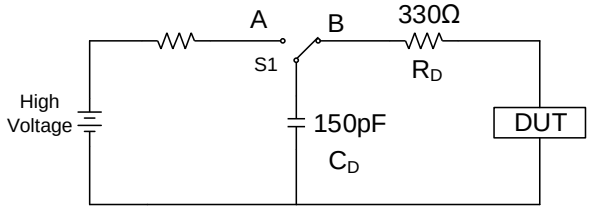


Figure 10: Equivalent Circuit of System Level ESD

Compared to the HBM ESD, the discharge capacitance in system-level ESD exceeds the HBM's effective capacitance, and the discharge resistance for system-level ESD is much smaller. Hence, the system level ESD discharging energy is much higher than HBM ESD.

If a high-level, system-level ESD is required, then an external circuit may be required to enhance the ESD capability (see Figure 11 on page 26).

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Figure 11 shows an external ESD-enhanced circuit using a Zener/ESD diode.

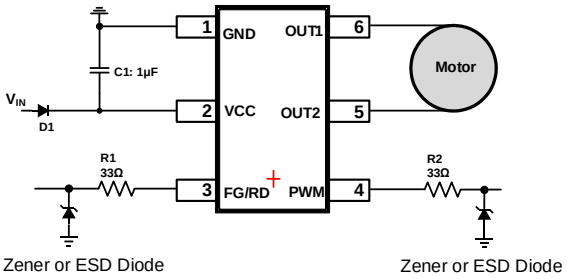

Figure 11: Enhanced ESD using a Zener Diode or ESD Diode

PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For the best results, refer to Figure 12 and follow the guidelines below:

1. To improve EMI performance, place a 0402 capacitor (C2 in Figure 13) as close to the VCC and GND pins as close.
2. Place the input capacitor (C1 in Figure 13) close the VCC and GND pins.

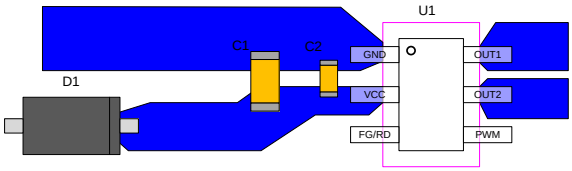

Figure 12: Recommended PCB Layout

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TYPICAL APPLICATION CIRCUITS

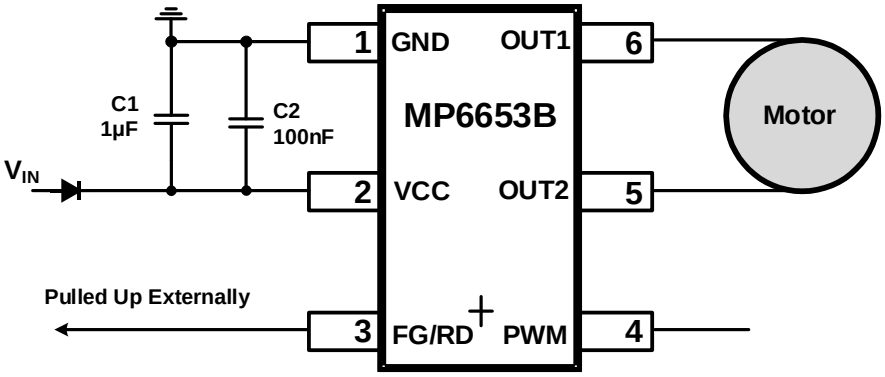

Figure 14: Typical Application Circuit

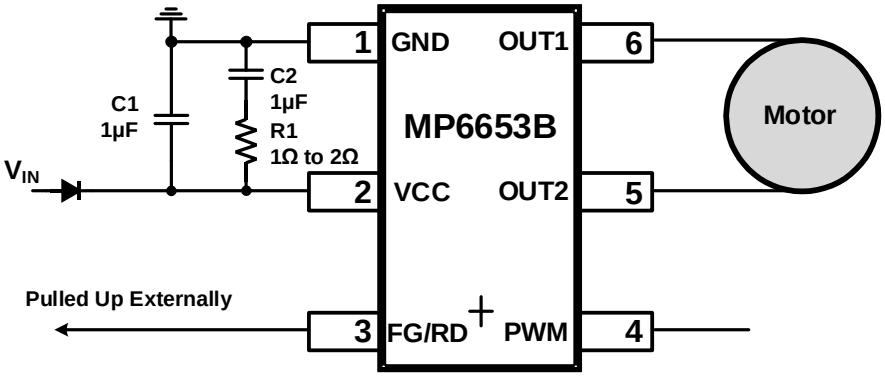

Figure 15: Typical Application Circuit with RC Snubber

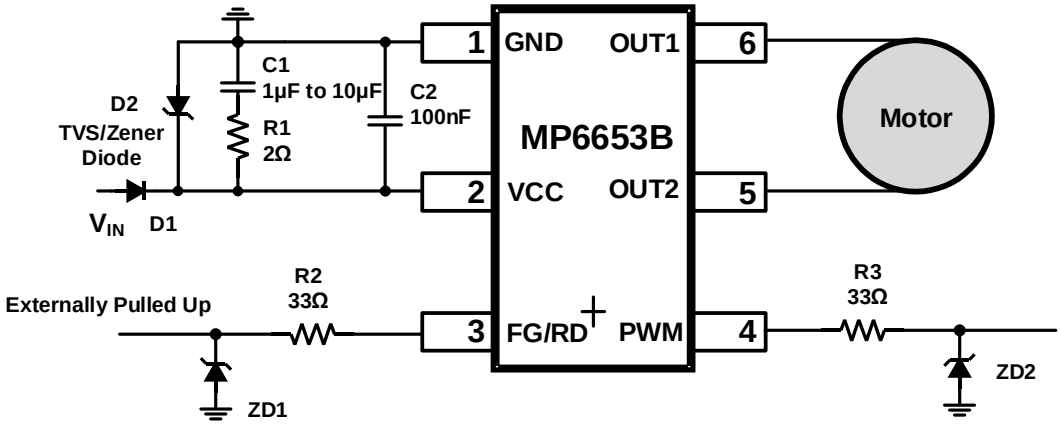

Figure 16: Typical Application Circuit with Voltage Clamping and Enhanced ESD

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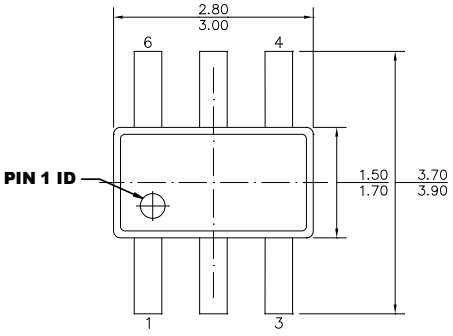
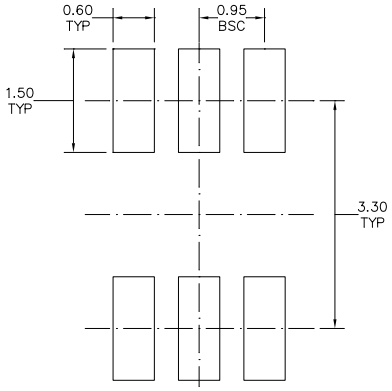
PACKAGE INFORMATION

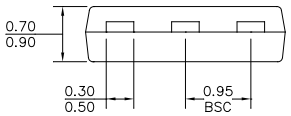
TSOT23-6-SL



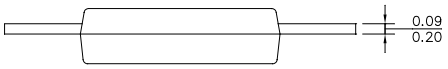
TOP VIEW



RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION, OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING REFERENCE IS JEDEC MO-193.
6) DRAWING IS NOT TO SCALE.

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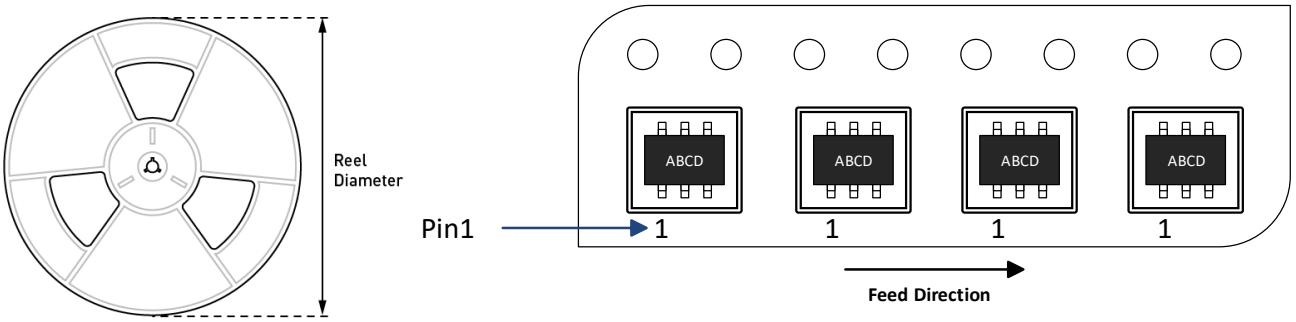
CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP6653BGJS-xxxx-Z	TSOT23-6-SL	5000	N/A	N/A	13in	12mm	8mm

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REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	12/10/2025	Initial Release	-

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