MP6611

32V 7A H-bridge DC Motor Driver

PRELIMINARY SPECIFICATIONS SUBJECT TO CHANGE

DESCRIPTION

The MP6611 is an H-bridge motor driver used for driving reversible motors, which can drive two solenoids or valves, one dc motor or one winding of a stepper motor or other Loads. The H-bridge consists of four N-channel power MOSFETs, and an internal charge pump generates needed gate-drive voltages.

The MP6611 operates on a motor power-supply voltage from 2.7V to 32V, which can supply an output current of up to 7A. Very low standby circuit current can be achieved when disable the device.

For the MP6611, control of the outputs is accomplished through the IN1/ENBL/PWM and IN2/DIR/EN pins, or by using the serial interface, or a combination of both. A mode pin is used to set the control modes like input signal logic (IN1/IN2, DIR/ENBL or independent PWM). A serial interface is used to set charge pump frequency, and slew rate, as well to read diagnostic registers. Internal safety and diagnostic features include open load detection, over-current protection, input over and under-voltage protection, thermal warning and thermal shutdown.

The MP6611 is available in a 20-pin, 4mmx4mm QFN package.

FEATURES

- 2.7V to 32V Operating Supply Voltage
- Internal Full H-Bridge Driver support 100% duty cycle
- Internal current-sensing and Programmable Cycle-by-cycle Current Regulation
- Low On Resistance (HS+LS: 40mΩ)
- Up to 7A Output Peak Current
- Serial Control interface
- MODE selection: set input PWM/DIR, IN1/IN2, Independent-PWM, Parallel
- 3.3V and 5V Compatible Logic Supply
- Controlled Slew Rate
- Programmable charge pump frequency
- Automatic Synchronous Rectification
- Low Iq SLEEP Mode and Brake mode
- Diagnostic Functions, including:
  - Open Load Detection
  - Over-Current Protection
  - Input Over- and Under-Voltage Protection
  - Over-Temperature Warning and Thermal Shutdown
  - Fault Indication Output
- Space-Saving 4mmx4mm QFN-20 Package

APPLICATIONS

- DC Brush Motor Drivers
- Solenoid Drivers
- Door Lock / Latch

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TYPICAL APPLICATION

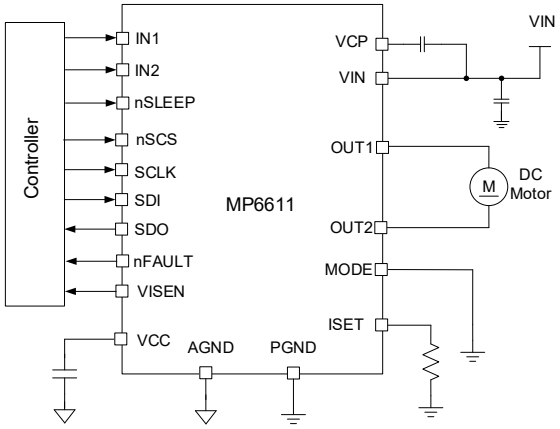

Figure 1: Full Bridge with IN1/IN2 Input

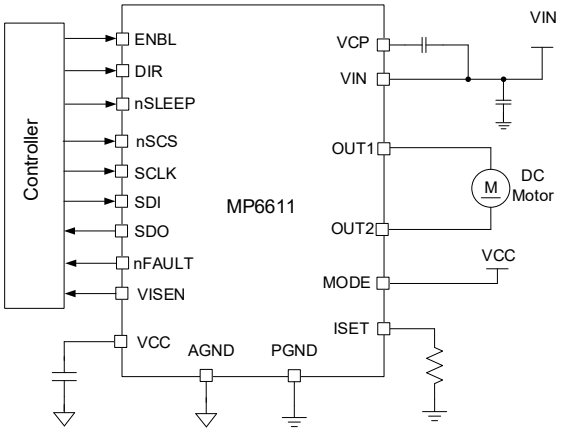

Figure 2: Full Bridge with DIR/ENBL Input

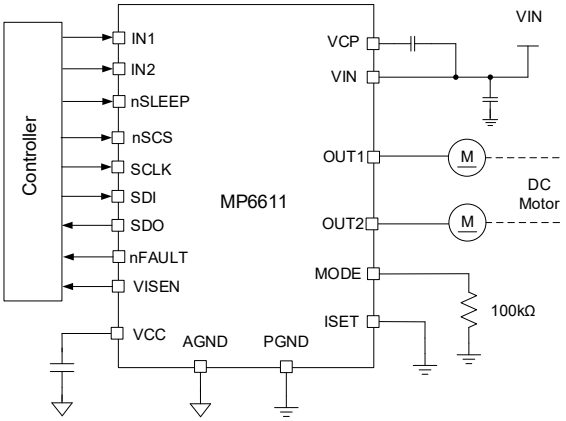

Figure 3: 2x Half Bridge with Independent PWM Input

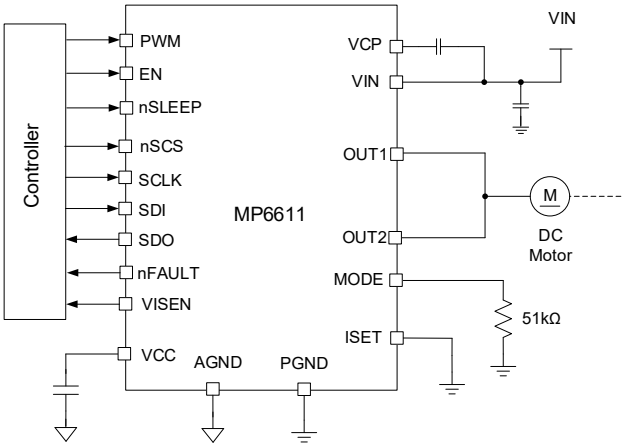

Figure 4: Parallel Half Bridge

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ORDERING INFORMATION

Part Number	Package	Top Marking	MSL Rating
MP6611GRE*	QFN-20 (4mm×4mm)	*See Below*	1

* For Tape & Reel, add suffix -Z (e.g. MP6611GRE-Z);

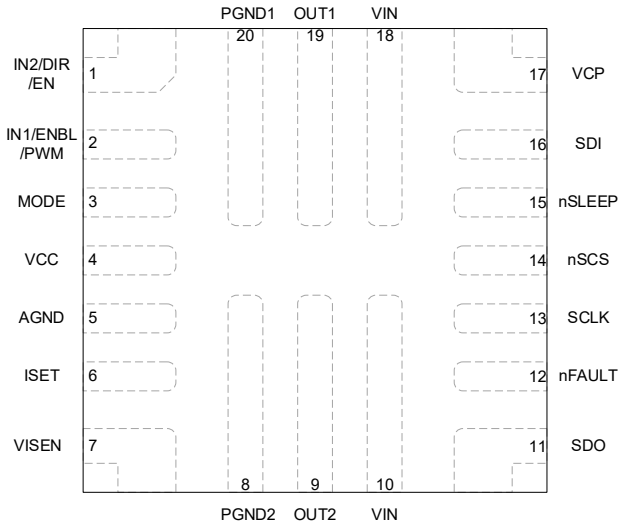
TOP MARKING

MPSYWW
MP6611
LLLLLL
E

MPS: MPS prefix
Y: Year code
WW: Week code
MP6611: First four digits of the part number
LLLLLL: Lot number
E: Wettable flank

PACKAGE REFERENCE

TOP VIEW



QFN-20 (4mmx4mm)

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PIN FUNCTIONS

Pin # MP6611	Pin Name			Description
1	IN2	-	-	**Input 2.** This pin has an internal pulldown resistor to GND. For details, see the Input Logic and Output configuration section.
	-	DIR	-	**Full-bridge phase input (motor direction).** This pin has an internal pulldown resistor to GND. For details, see the Input Logic and Output configuration section.
	-	-	EN	**Enable input for parallel half-bridge.** This pin has an internal pulldown resistor to GND. For details, see the Input Logic and Output configuration section.
2	IN1	-	-	**Input 1.** This pin has an internal pulldown resistor to GND. For details, see the Input Logic and Output configuration section.
	-	ENBL	-	**Full-bridge PWM input.** This pin has an internal pulldown resistor to GND. For details, see the Input Logic and Output configuration section.
	-	-	PWM	**PWM input for parallel half-bridge.** This pin has an internal pulldown resistor to GND. For details, see the Input Logic and Output configuration section.
3	MODE			**Input mode pin.** Sets the PH/EN, PWM, independent-PWM or parallel mode.
4	VCC			**3.3V LDO output for internal driver and logic.** Bypass this pin to AGND with a low-ESR ceramic capacitor. Do not connect external loads to this supply pin.
5	AGND			**Analog ground.** Reference ground for internal analog circuits. Appropriately connect to the reference ground of the external analog systems, and PGND.
6	ISET			**Current configuration resistor.** Connect a resistor to ground to set the current limit and VISEN output voltage. If the current limit is not desired, the ISET pin can be connected directly to ground.
7	VISEN			**Current sense output terminal.** The load current applied to the VISEN pin should be kept below 2mA, with no more than 500pF of capacitance.
8	PGND2			**Power ground2.** High-current return for the half-bridge 2. Connect PGND with large copper areas to the power supply returns. Connect this pin to the system ground.
20	PGND1			**Power ground1.** High-current return for the half-bridge 1. Connect PGND with large copper areas to the power supply returns. Connect this pin to the system ground.
9	OUT2			**Output terminal 2.** Connect OUT2 to the motor winding.
19	OUT1			**Output terminal 1.** Connect OUT1 to the motor winding.
10, 18	VIN			**Supply voltage pin.** Bypass each VIN pin to PGND with a low-ESR ceramic capacitor. And a bulk capacitor must be included on the VIN pin which is required to absorb the energy flowing from the motor or power supply and should be sized according to the application requirements.
11	SDO			**Serial data output.** Open-drain output, and must be pulled up by an external pull-up resistor.
12	nFAULT			**Fault indication pin.** The nFAULT pin is open-drain output requiring an external pullup resistor. This pin is pulled logic low when a fault is detected. The pin returns to Hi-Z state as the device resumes operation.
13	SCLK			**Serial clock.** Data is shifted on the rising edge of SCLK. SCLK has an internal pull-down resistor.
14	nSCS			**Serial chip selection input.** An active low on this pin enables the serial interface communication. nSCS is pulled up to nSLEEP internally.
15	nSLEEP			**Sleep mode input.** Logic high to enable device, logic low to enter low-power sleep mode. nSLEEP is pulled down via an internal resistor.

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PIN FUNCTIONS *(continued)*

Pin # MP6611	Pin Name	Description
16	SDI	**Serial data input.** SDI has an internal pull-down resistor.
17	VCP	**Charge pump output.** Connect a 1µF, 16V, X7R ceramic capacitor to VIN. Do not connect external loads to this supply pin.

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ABSOLUTE MAXIMUM RATINGS (1)

Input supply voltage (V_{IN}) ..... –0.3V to +39V
VCC (V_{CC}) ..... –0.3V to +5V
OUTx voltage ..... –0.7V to (V_{IN}+0.3)V
OUTx voltage (<100ns transient)
..... –2V to (V_{IN}+0.3)V
VCP ..... V_{IN} to V_{IN} +5V
MODE, VISEN, ISET ..... –0.3V to +5V
PGND ..... –0.3V to +0.3V
All other pins ..... –0.3V to +6V
Continuous power dissipation (T_A = +25°C) (2)
QFN-20 (4mm×4mm) 2.84W
Storage temperature ..... –65°C to +150°C
Junction temperature ..... 150°C
Lead temperature (solder) ..... 260°C

ESD Ratings

Human-body model (HBM) 2000V
Charged-device model (CDM) 750V

Recommended Operating Conditions (3)

Input supply voltage (V_{IN}) ..... 2.7V to 32V
Input supply voltage (V_{IN}) (4) ..... 2.7V to 28V
Operating junction temp (T_J) .... -40°C to +150°C

Thermal Metric (5)

θ_{JA} (Junction-to-ambient) ..... 37.8°C/W
θ_{JC_top} (Junction-to-case top) ..... 32.3°C/W
θ_{JC_bottom} (Junction-to-case bottom) ..... 1.8°C/W
θ_{JB} (Junction-to-board) ..... 2.4°C/W
Ψ_{JT} (Junction-to-top) ..... 1.4°C/W
Ψ_{JB} (Junction-to-board) ..... 2.5°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) -T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) For half bridge application, if load is connected to VIN, the recommended operating voltage is 2.7V to 28V.
5) According to JEDEC JESD51-2/-5/-7/-8/-14.

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ELECTRICAL CHARACTERISTICS

2.7V <= V_{IN} <= 32V, T_J = -40°C to 150°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Supply Voltage						
VIN operating range	V_{IN}		2.7		32	V
Turn-on threshold	V_{UVLO}	VIN rising edge	2.3	2.5	2.7	V
Turn-on hysteretic voltage	V_{UVLO_HYS}			0.2		V
VIN UV warning threshold	V_{UVW}		3.3	3.5	3.7	V
IC Supply						
Shutdown current	I_{IN_SD}	V_{IN} = 13.5V, T_J = 25°C, nSLEEP = low			1	µA
		V_{IN} = 13.5V, T_J = 150°C, nSLEEP = low			10	µA
Quiescent current	I_{IN_BRAKE}	V_{IN} = 13.5V, nSLEEP = High, Low Iq brake mode for MODE1 and MODE2		10	25	µA
Operation current		V_{IN} = 13.5V, nSLEEP = High, no load, 20kHz PWM		4		mA
VCC regulator voltage	V_{VCC}	V_{IN} > 3.6V, 10mA load	3	3.3	3.6	V
VCC regulator drop output voltage	V_{VCCD}	V_{IN} ≤ 3.6V, 10mA load		700		mV
IC SLEEP time	t_{SLEEP}	nSLEEP low to start device shutdown	100			µs
nSLEEP reset pulse	T_{RESET}	nSLEEP low to only clear fault registers	10		25	µs
IC start-up delay	T_{DELAY}	nSLEEP high or VIN > V_{UVLO} when nSLEEP = 1 to OUTx ready			1.5	ms
Low Iq brake mode entre time		IN1 = IN2 = H or ENBL = L	100	200	300	ms
IC Disable time	$t_{DISABLE}$	DIS transition from “0” to “1”	1	2	5	µs
Input Logic (IN1/ENBL/PWM, IN2/DIR/EN, SDI, SCLK)						
Input high voltage	V_{IH}		1.5			V
Input low voltage	V_{IL}				0.7	V
Input logic hysteresis	V_{I_HYS}			250		mV
Input high current	I_{IH}	V_{CC} = 3.3V	-20		20	µA
Input low current	I_{IL}	V_{CC} = 0V	-20		20	µA
Input pull-down resistance	R_{PD}	**I**N1/ENBL/PWM, IN2/DIR/EN, SDI		400		kΩ
		SCLK		100		kΩ
Propagation delay (ENBL/INx/PWM to OUTx = 50%)	T_{PD}	I_{OUT} = 1A, V_{IN} = 13.5V, SR = 000b		1.5		µs
		I_{OUT} = 1A, V_{IN} = 13.5V, SR = 001b		1		
		I_{OUT} = 1A, V_{IN} = 13.5V, SR = 010b		0.8		
		I_{OUT} = 1A, V_{IN} = 13.5V, SR = 011b		0.6		
		I_{OUT} = 1A, V_{IN} = 13.5V, SR = **100b***		0.48		
		I_{OUT} = 1A, V_{IN} = 13.5V, SR = 101b		0.36		
		I_{OUT} = 1A, V_{IN} = 13.5V, SR = 110b		0.25		
		I_{OUT} = 1A, V_{IN} = 13.5V, SR = 111b		0.2		
Input Logic (nSLEEP)						
Input high voltage	V_{IH}		1			V
Input low voltage	V_{IL}				0.4	V
Input logic hysteresis	V_{I_HYS}			130		mV

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ELECTRICAL CHARACTERISTICS *(continued)*

2.7V <= V_{IN} <= 32V, T_J = -40°C to 150°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Input pull-down resistance	R_{PU}			100		kΩ
Input Logic (nSCS)						
Input high voltage	V_{IH}		1.5			V
Input low voltage	V_{IL}				0.7	V
Input logic hysteresis	V_{I_HYS}			250		mV
Input pull-up resistance	R_{PU}			400		kΩ
nFault Output (Open-Drain Output)						
Output low voltage	V_{OL}	I_{nFault_OUT} = 5mA			0.4	V
Output high leakage current	I_{OH}	V_{nFault_OUT} = 3.3V	-1		1	μA
Power MOSFET						
Output on resistance	R_{HS}	I_{OUT} = 1A, T_A = 25°C,		20	25	mΩ
		I_{OUT} = 1A, T_J = -40 to 150°C			40	mΩ
	R_{LS}	I_{OUT} = 1A, T_A = 25°C,		20	25	mΩ
		I_{OUT} = 1A, T_J = -40 to 150°C			40	mΩ
Minimum on time	t_{MON}	I_{OUT} = 1A, SR = 000b, V_{IN} = 13.5V		2.2		μs
		I_{OUT} = 1A, SR = 111b, V_{IN} = 13.5V		1		
Output rise/fall time (OUTx 10% to 90% changing)	SR	I_{OUT} = 1A, V_{IN} = 13.5V, SR = 000b		5		V/μs
		I_{OUT} = 1A, V_{IN} = 13.5V, SR = 001b		9.6		
		I_{OUT} = 1A, V_{IN} = 13.5V, SR = 010b		13		
		I_{OUT} = 1A, V_{IN} = 13.5V, SR = 011b		19		
		I_{OUT} = 1A, V_{IN} = 13.5V, SR = 100b*		28		
		I_{OUT} = 1A, V_{IN} = 13.5V, SR = 101b		48		
		I_{OUT} = 1A, V_{IN} = 13.5V, SR = 110b		96		
		I_{OUT} = 1A, V_{IN} = 13.5V, SR = 111b		184		
Dead time (6)	t_{DEAD}			120		ns
Body diode forward voltage	V_{F_DIODE}	I_{OUT} = 1A		0.8		V
Switching Frequency						
Applied PWM frequency	F_{PWM}	CP_F = 00b			200	kHz
CHARGE PUMP (VCP)						
VCP operating voltage	V_{VCP}	with respect to VIN		VIN+ 3.3		V
Charge pump switching frequency	f_{CP}	VIN > V_{UVLO}; nSLEEP = 1; CP_F = 00b		3000		kHz
		VIN > V_{UVLO}; nSLEEP = 1; CP_F = 01b		1500		
		VIN > V_{UVLO}; nSLEEP = 1; CP_F = 10b		750		
		VIN > V_{UVLO}; nSLEEP = 1; CP_F = 11b		375		
Protection						
Over-current threshold	I_{OC}	OC_ADJ = 0b	8.5	11	13.5	A
		OC_ADJ = 1b	11.5	14.5	17.5	A

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ELECTRICAL CHARACTERISTICS *(continued)*

2.7V < V_{IN} < 32V, T_J = -40°C to 150°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
OCP retry time	t_{OCR}	OCR_T = 00b		10		ms
		OCR_T = 01b		4		
		OCR_T = 10b		1		
		OCR_T = 11b		0.5		
Over-Current Deglitch Time	t_{OCP_D}	OCD_T = 00b	0.8	1.2	1.4	µs
		OCD_T = 01b	0.5	0.65	0.8	
		OCD_T = 10b	1.7	2.3	2.9	
		OCD_T = 11b	3.5	4.5	5.5	
Input over-voltage threshold	V_{OVP}	OVP_M = 000b – 001b	35	37	38	V
		OVP_M = 010b – 100b	29	30	31	V
		OVP_M = 101b – 111b	21	22	23	V
Input over-voltage threshold Hysteresis	V_{OVP_HYS}			2		V
Open Load Current for standby mode	I_{OLS}		0.4	1.5	2.6	mA
Open load diagnostic delay time	t_{OL}	OLD_DLY = 0b		0.3		ms
		OLD_DLY = 1b		1.2		
Thermal shutdown	T_{SD}		150	170	190	°C
Thermal shutdown hysteresis	T_{SD_HY}			20		°C
Thermal Warning	T_{OTW}		120	140	160	°C
Thermal Warning hysteresis	T_{OTW_HY}			20		°C
Current Control						
ISET current	I_{ISET}	I_{OUT} > = 1A	95	100	105	µA/A
ISET current error	I_{ISET}	I_{OUT} >= 1A	-5		+5	%
		I_{OUT} < 1A	-5		+5	µA
Current trip voltage (rising)	$V_{ITRIP-R}$	At ISET pin	1.44	1.5	1.56	V
Current trip voltage (falling)	$V_{ITRIP-F}$	At ISET pin	1.15	1.2	1.25	V
Sense Delay Time (OUTx to VISEN) [6]	t_{SEN_D}	VISEN = 2V; SR = 000b		4.5		µs
		VISEN = 2V; SR = 111b		2.5		
Blanking time	t_{BLANK}	CLB_T = 00b	0.75	1	1.4	µs
		CLB_T = 01b	1.5	2	2.6	
		CLB_T = 10b	3	4	5	
		CLB_T = 11b	6	8	10	
Off time	t_{OFF}	OFF_T = 00b		20		µs
		OFF_T = 01b		40		
		OFF_T = 10b		60		
		OFF_T = 11b		80		
VISEN output						
Output voltage accuracy	ΔV_{VISEN}	V_{ISET} > 0.2V	-5		5	%

Note:

6) Not tested in production.

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TIMIMG CHARACTERISTICS (7)

V_{IN} = 13.5V, T_A = +25°C, unless otherwise noted.

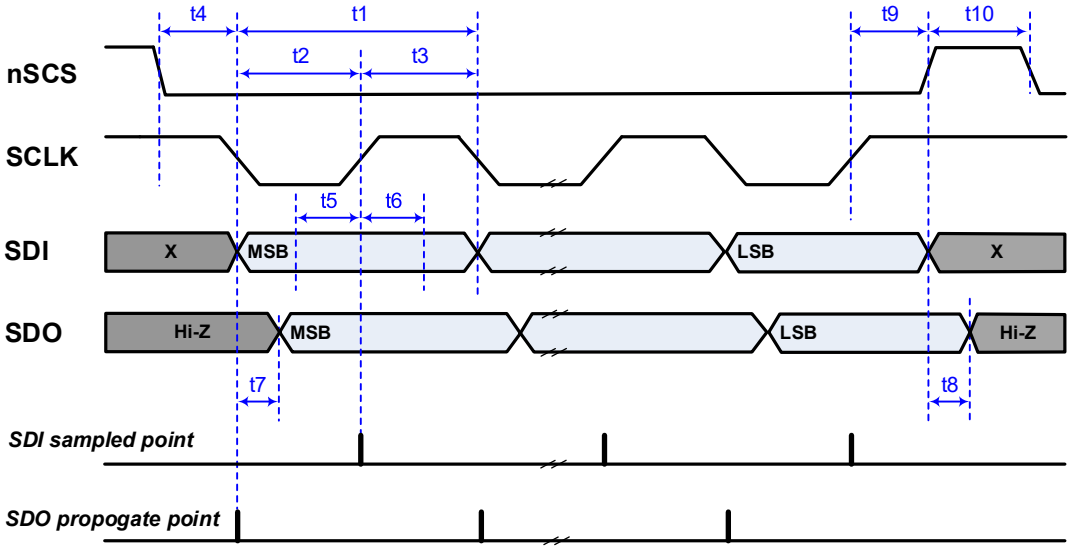

Figure 5: Serial Interface Timming Diagram

Parameter	Symbol	Condition	Min	Typ	Max	Units
SPI ready after startup	t_{READY}	V_{IN} > V_{UVLO}, nSLEEP = 1			1.5	ms
SCLK cycle time	t1		200			ns
SCLK frequency			0.1		5	MHz
SCLK low time	t2		100			ns
SCLK high time	t3		100			ns
SCLK rise/fall time	-				50	ns
nSCS input Setup time (nSCS low to SLCK falling)	t4		50			ns
SDI input data setup time (SDI valid to SCLK rising)	t5		50			ns
SDI input data hold time (SCLK rising to SDI valid)	t6		50			ns
SDO output data delay time (SCLK falling to SDO enable)	t7	C_L < 100pF, pull-up R = 1kΩ			40	ns
nSCS disable delay time (nSCS high to SDO high impedance)	t8				50	ns
nSCS input hold time	t9		40			ns
nSCS inactive time	t10		500			ns

Note:

7) Guaranteed by design.

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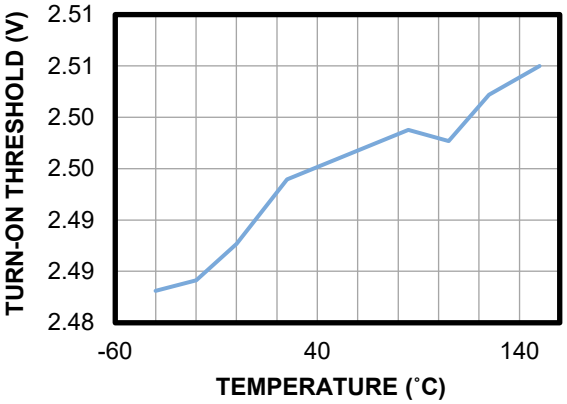
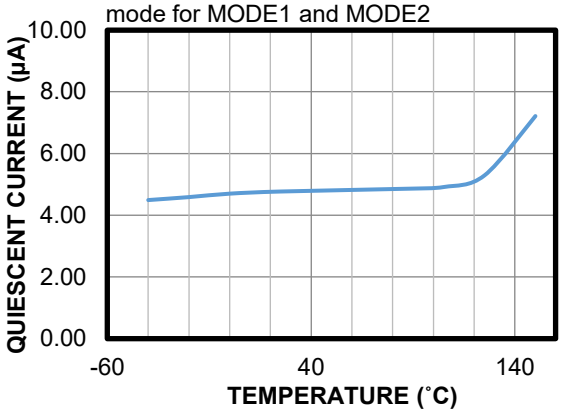
TYPICAL CHARACTERISTICS

Turn-on Threshold vs. Temperature



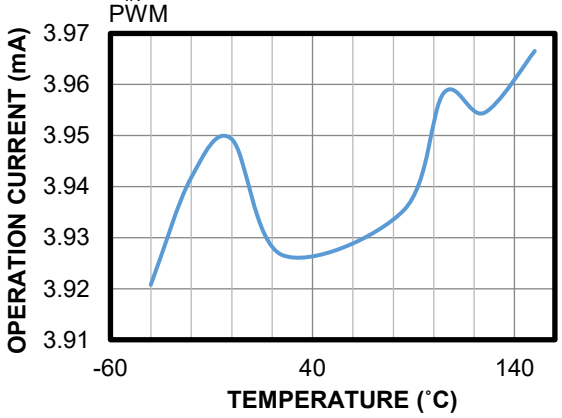
Quiescent Current vs. Temperature

V_{IN} = 13.5V, nSLEEP = H, Low Iq brake mode for MODE1 and MODE2



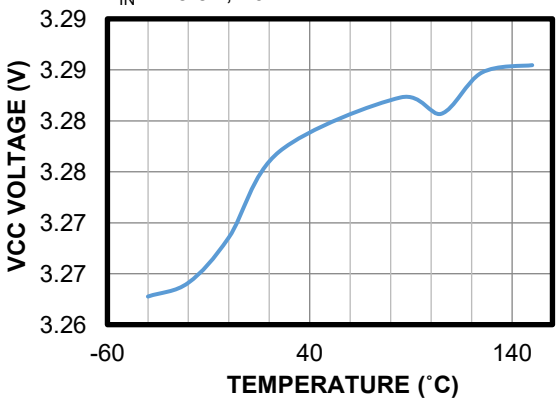
Operation Current vs. Temperature

V_{IN} = 13.5V, nSLEEP = H, no load, 20kHz PWM



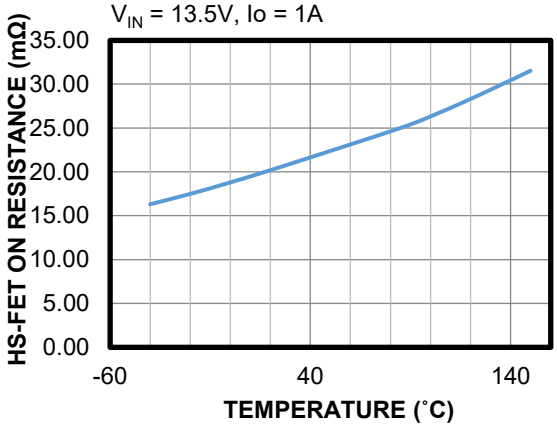
VCC Voltage vs. Temperature

V_{IN} = 13.5V, 10mA load



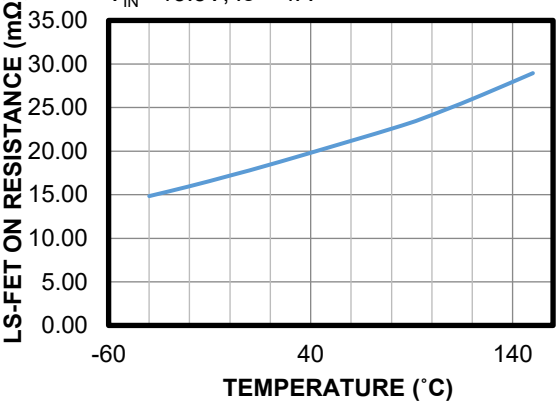
HS-FET On Resistance vs. Temperature

V_{IN} = 13.5V, Io = 1A



LS-FET On Resistance vs. Temperature

V_{IN} =13.5V, Io = 1A



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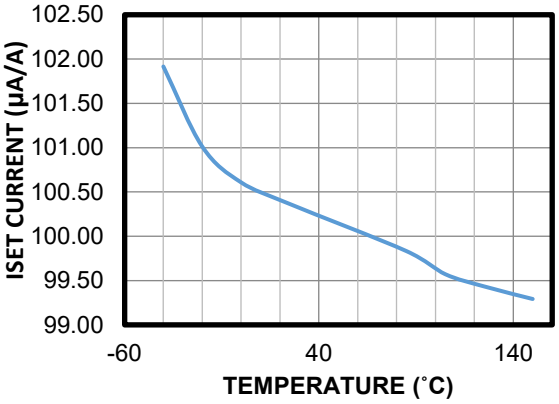
TYPICAL CHARACTERISTICS *(continued)*

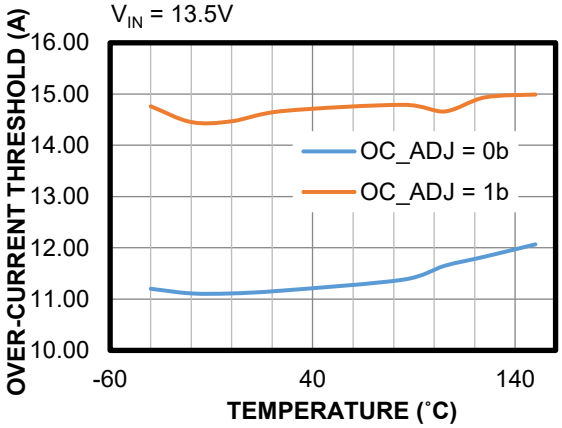
ISET Current vs. Temperature

I_{OUT} = 1A



Over-current threshold vs. Temperature

V_{IN} = 13.5V



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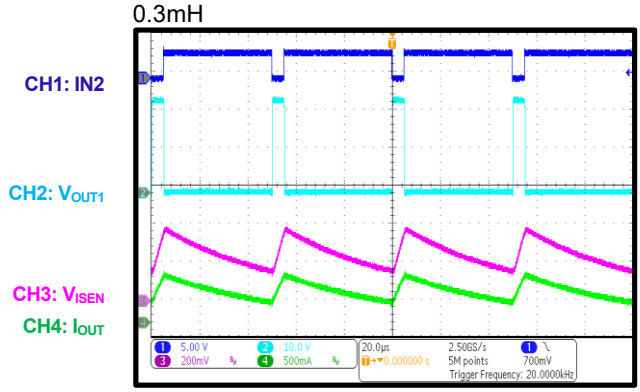
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 24V, T_A = 25°C, unless otherwise noted.

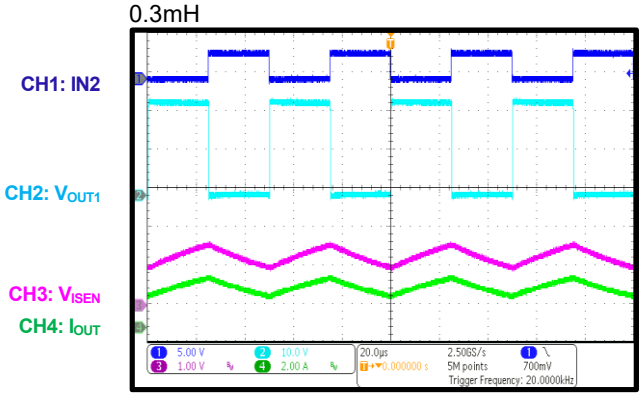
Full Bridge with IN1/IN2 input

IN1 = H, IN2 = PWM, duty = 10%, load = 5Ω + 0.3mH



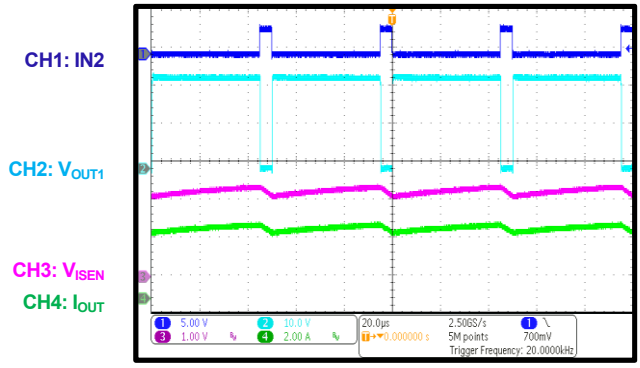
Full Bridge with IN1/IN2 input

IN1 = H, IN2 = PWM, duty = 50%, load = 5Ω + 0.3mH



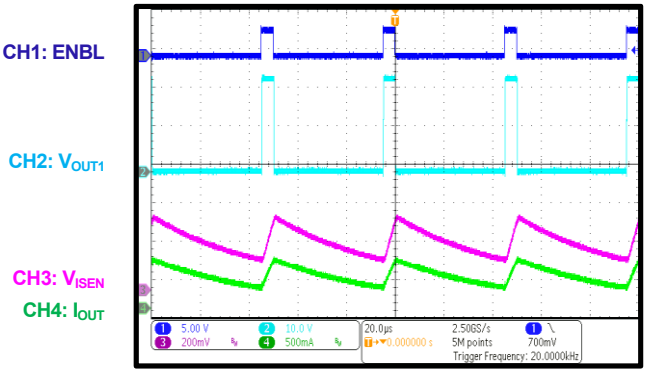
Full Bridge with IN1/IN2 input

IN1 = H, IN2 = PWM, duty = 90%, load = 5Ω + 0.3mH



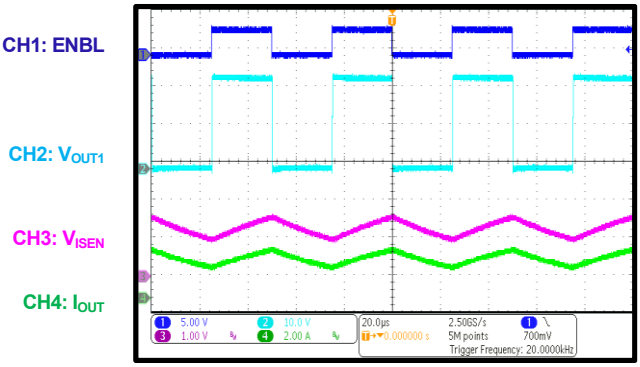
Full Bridge with DIR/ENBL input

ENBL = PWM, DIR = H, duty = 10%, load = 5Ω + 0.3mH



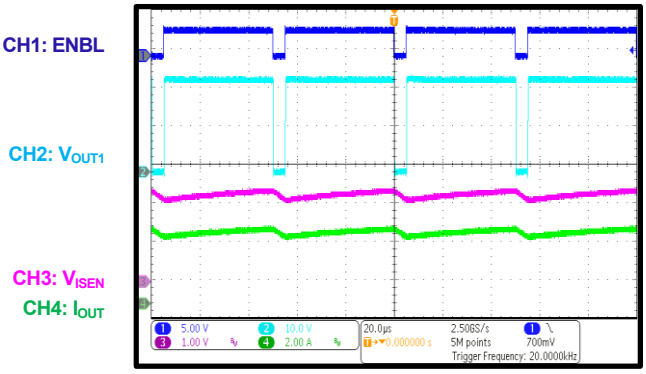
Full Bridge with DIR/ENBL input

ENBL = PWM, DIR = H, duty = 50%, load = 5Ω + 0.3mH



Full Bridge with DIR/ENBL input

ENBL = PWM, DIR = H, duty = 90%, load = 5Ω + 0.3mH



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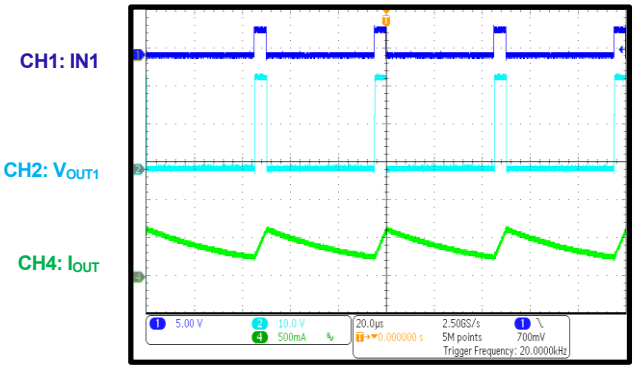
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 24V, T_A = 25°C, unless otherwise noted.

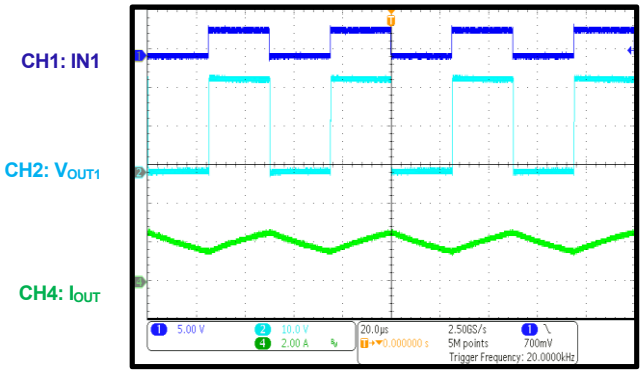
2x Half Bridge

IN1 = PWM, duty = 10%, load = 5Ω + 0.3mH connected to GND



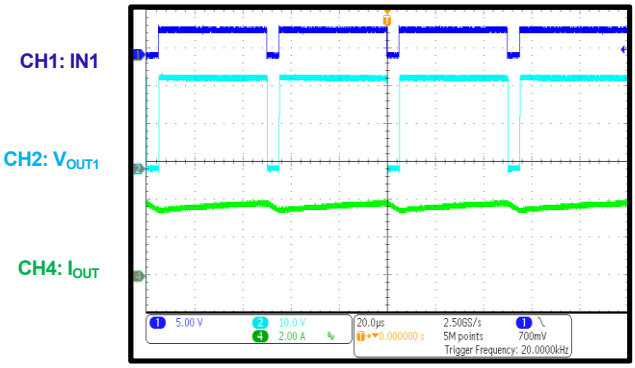
2x Half Bridge

IN1 = PWM, duty = 50%, load = 5Ω + 0.3mH connected to GND



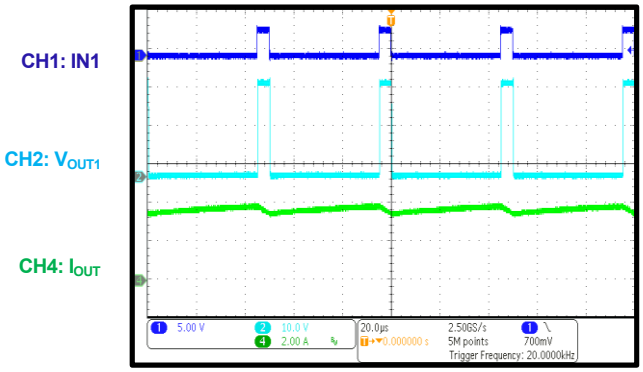
2x Half Bridge

IN1 = PWM, duty = 90%, load = 5Ω + 0.3mH connected to GND



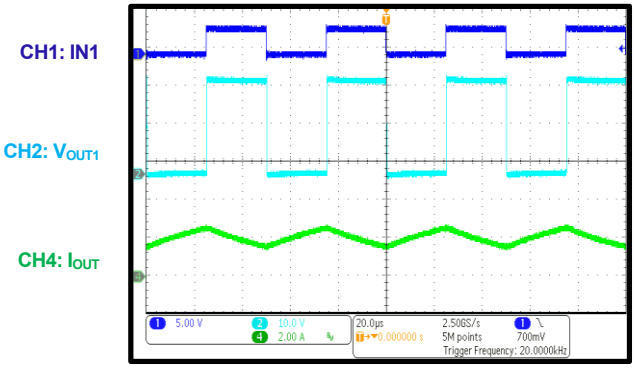
2x Half Bridge

IN1 = PWM, duty = 10%, load = 5Ω + 0.3mH connected to VIN



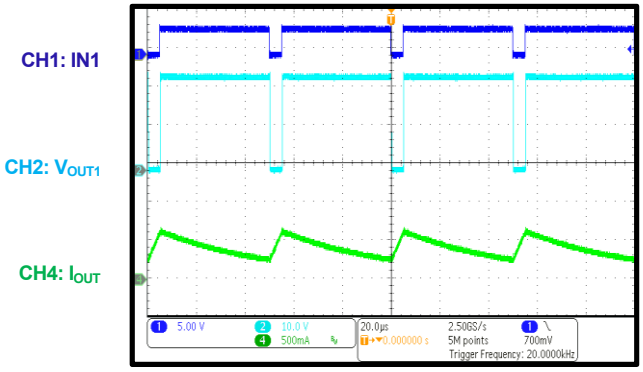
2x Half Bridge

IN1 = PWM, duty = 50%, load = 5Ω + 0.3mH connected to VIN



2x Half Bridge

IN1 = PWM, duty = 90%, load = 5Ω + 0.3mH connected to VIN



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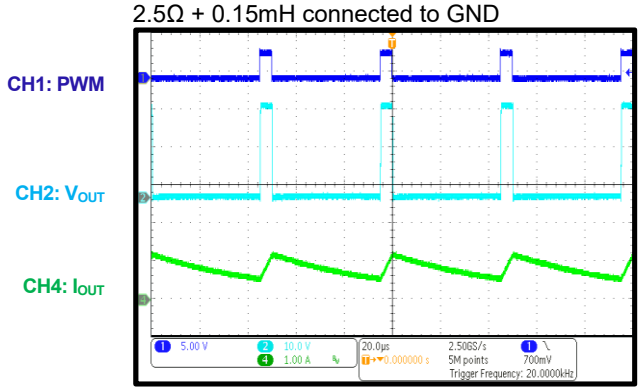
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 24V, T_A = 25°C, unless otherwise noted.

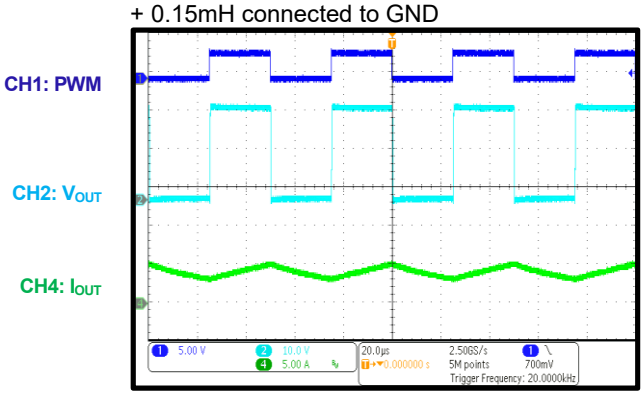
Parallel Half Bridge

EN = H, PWM = PWM, duty = 10%, load = 2.5Ω + 0.15mH connected to GND



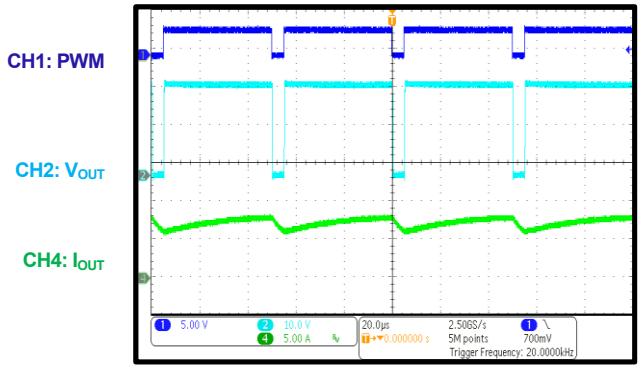
Parallel Half Bridge

EN = H, PWM = PWM, duty = 50%, load = 2.5Ω + 0.15mH connected to GND



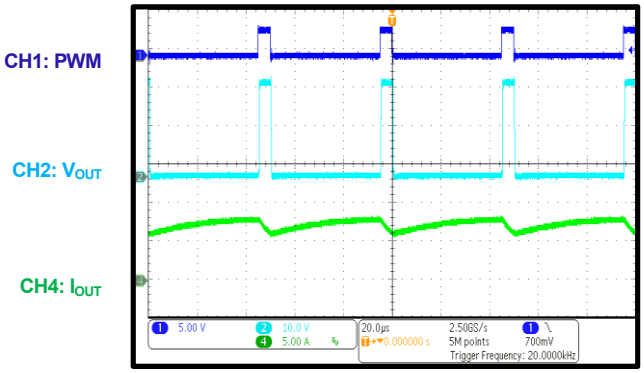
Parallel Half Bridge

EN = H, PWM = PWM, duty = 90%, load = 2.5Ω + 0.15mH connected to GND



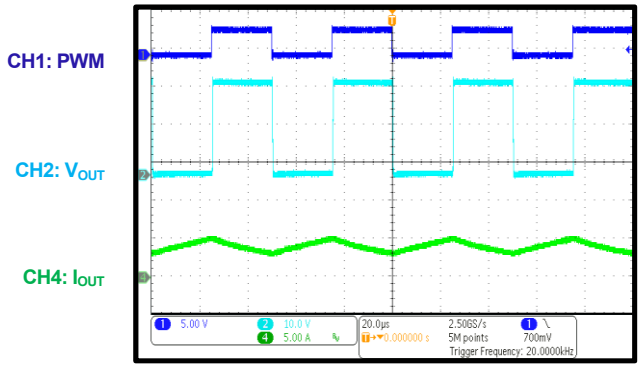
Parallel Half Bridge

EN = H, PWM = PWM, duty = 10%, load = 2.5Ω+0.15mH connected to VIN



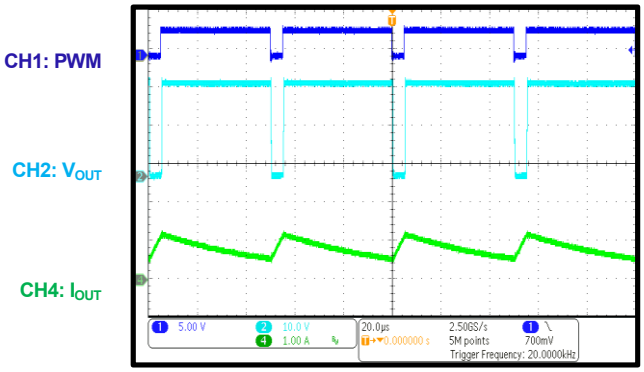
Parallel Half Bridge

EN = H, PWM = PWM, duty = 50%, load = 2.5Ω + 0.15mH connected to VIN



Parallel Half Bridge

EN = H, PWM = PWM, duty = 90%, load = 2.5Ω + 0.15mH connected to VIN



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FUNCTIONAL BLOCK DIAGRAM

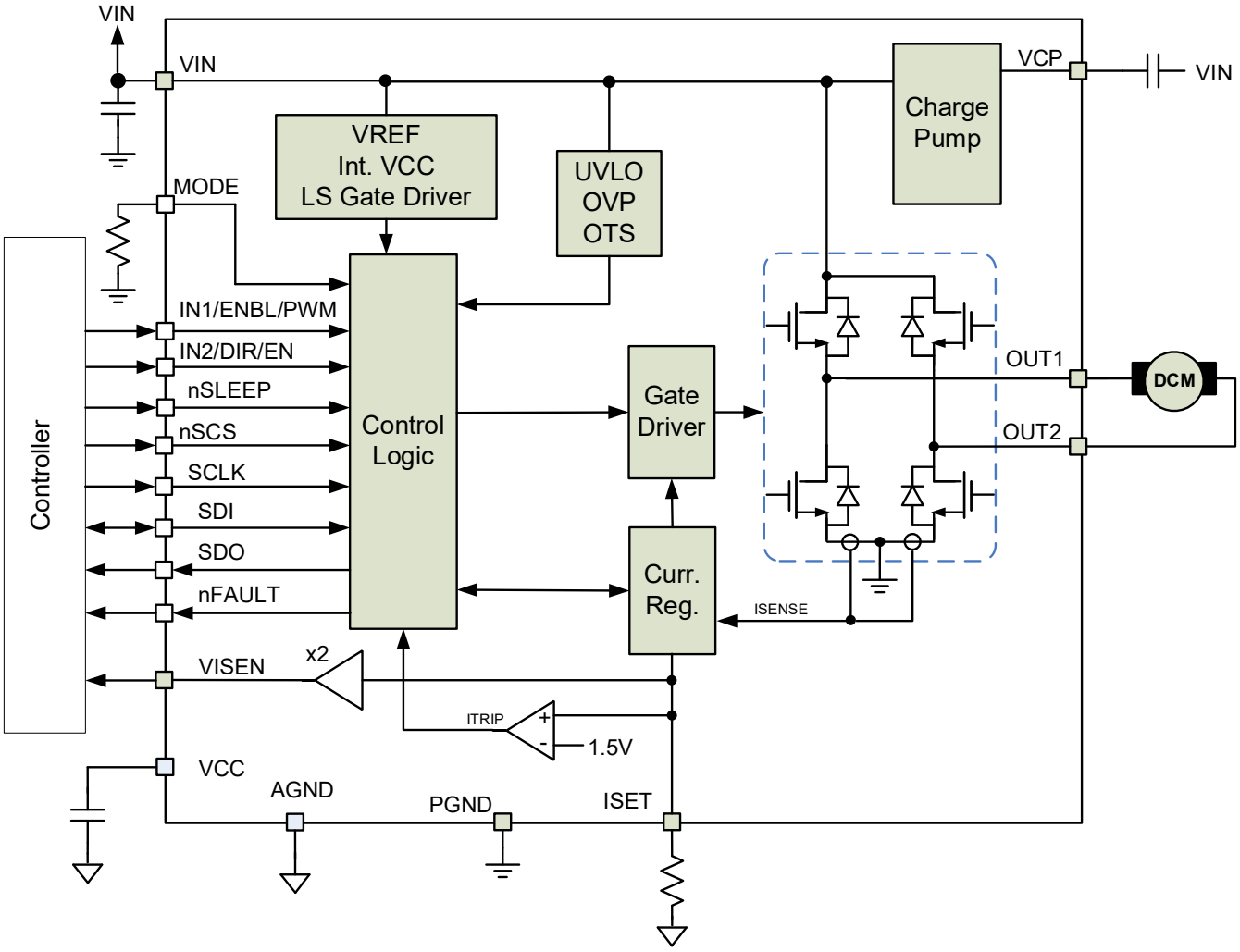

Figure 6: Functional Block Diagram

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OPERATION

The MP6611 is an H-bridge motor driver used for driving reversible motors, which can drive one dc motor or one winding of a stepper motor or other Loads. The H-bridge consists of four N-channel power MOSFETs, and an internal charge pump generates needed gate-drive voltages.

A serial (SPI) control interface is used to program device operation, as well as setup the slew rate, charge pump frequency, and read back the status of the device and access diagnostic information.

The MP6611 integrates internal current-sensing and programmable cycle by cycle current limit function.

Input Logic and Output Configuration

Four programmable input interface and configuration are available on the MP6611, which are selected by the MODE pin as below table:

Table 1: Mode Selection for Input/Output Configuration

MODE	Setup	Input interface	output configuration
1	Connect to GND (<10Ω)	IN1/IN2	full bridge
2	Connect to VCC (<10Ω)	DIR/ENBL	full bridge
3	100kΩ ± 10% to GND	IN1/IN2	2 x half bridges
4	51kΩ ± 10% to GND	PWM/EN	Parallel half bridge

The following tables show the input logic truth table for the different modes.

Table 2: Input Logic Truth Table for Mode 1

IN1	IN2	OUT1	OUT2	Function (DC Motor)
L	L	Z	Z	Coast
L	H	L	H	Reverse
H	L	H	L	Forward
H	H	L	L	Brake

Table 3: Input Logic Truth Table for Mode 2

ENBL	DIR	OUT1	OUT2	Function (DC Motor)
H	L	L	H	Reverse
H	H	H	L	Forward
L	x	L	L	Brake

Table 4: Input Logic Truth Table for Mode 3

INx	OUTx
L	L
H	H

Table 5: Input Logic Truth Table for Mode 4

EN	PWM	OUT
H	L	L
H	H	H
L	x	Z

Input Logic Control (SPI & input pins)

The MP6611 may be controlled either using the input pins IN1/ENBL/PWM and IN2/DIR/EN, by using writes to the SPI_IN1 and SPI_IN2 bits in the CTRL1 register via SPI, or a combination of both. When SPI_IN = 0b, outputs follow input pins only; when SPI_IN = 1b, outputs follow SPI registers or a combination of SPI and input pins. The enable function uses the level on the pin exclusive-or'ed with the state of corresponding register bits in the OUT register. This allows control to be done with either the SPI interface or pins. In addition, by programming the bit to '1', the input state is inverted. Refer to below table for the logic control combination of SPI and input pins.

Table 6: Logic Control Combination of SPI and Input Pins (when SPI_IN = 1b)

SPI SPI_IN1	Input PIN1 (IN1/ENBL/PWM)	Input Logic (IN1/ENBL/PWM)
0b	L	L
0b	H	H
1b	L	H
1b	H	L

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Table 7: Logic Control Combination of SPI and Input Pins (when SPI_IN = 1b)

SPI SPI_IN2	Input PIN2 (IN2/DIR/EN)	Input Logic (IN2/DIR/EN)
0b	L	L
0b	H	H
1b	L	H
1b	H	L

For control with SPI only, the input pins should be connected to ground.

nSLEEP Operation

Driving nSLEEP low puts the device into a low power sleep state. In this state, the H-bridge outputs are turned off, all related internal circuits including the gate drive charge pump are disabled, and all inputs are ignored. When waking up from sleep mode, some time (T_{DELAY}) needs to be passed before the outputs operate. All registers are reset after nSLEEP restart.

It is recommended to pull up nSLEEP after the input voltage (VIN) is ready.

nSLEEP Reset Pulse

The pre-controller can clear the device all fault flags and latched fault status by a nSLEEP reset pulse (nSLEEP low pulse between 10-25us), equivalent to the FLT, CLR command.

Brake Mode Operation

When BRAKE bit =1b as below table, the low Iq BRAKE mode is enabled, then the device will operate in low Iq brake mode when IN1=IN2=H or ENBL=L over 200ms for Mode 1/2, or device enters low Iq brake mode immediately for Mode 3, or set EN=H before set BRAKE=1b for Mode 4. This operates as described below:

Table 8: Low I_Q Brake Mode Setup

BRAKE	MODE	IN setup	OUT configuration
1b	1/2	IN1 = IN2 = H or ENB = L>0.2s	OUT1 = OUT2 = L
1b	3	Inx = H or L before set BRAKE = 1b	OUTx = INx
1b	4	EN = H, PWM = H or L before set BRAKE = 1b	OUT = PWM

In low Iq brake mode for Mode 1/2, only few internal circuit works to keep load brake, current sense and limit/regulation function are disabled, most diagnostic and protection functions are also disabled, only output short to Vin protection is retained, so part consumes very small current. In low Iq brake mode for Mode 3/4, charge pump works extra to prevent the requirement to turn on HS-FET.

Current Sensing

For mode 1 and mode 2, the current flowing in the two low-side MOSFETs is sensed with an internal current sensing circuit. A voltage that is proportional to the output current is sourced on the VISEN pin.

The VISEN output voltage scaling is set by a resistor connected between the ISET pin and ground. For 1A of output current, 100μA of current is sourced into the resistor connected to ISET. For example, if a 5kΩ resistor is connected between ISET and ground, the voltage on the ISET pin is 0.5V/A of output current and the output voltage on VISEN pin will be 1V/A of output current.

Current is sensed any time one of the low-side MOSFETs are turned on, including during slow decay mode (brake). But if device is in low Iq brake mode, the current sense function is disabled.

The load current applied to the VISEN pin should be kept below 2mA, with no more than 500pF of capacitance.

Current Regulation for Full Bridge

For mode 1 and mode 2, the current in the outputs is regulated using constant off-time PWM (pulse width modulation) control circuitry. This operates as described below:

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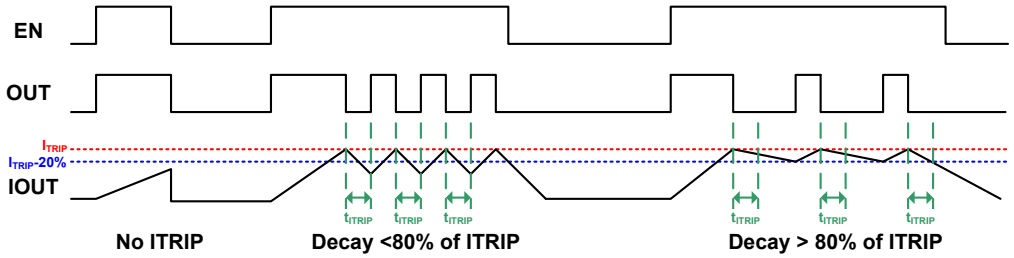

Figure 7: Current Regulation Operation

- Initially, a diagonal pair of MOSFETs turns on and drives current through the load.
- The current increases in the load, which is sensed by the internal current sense circuit.
- If the load current reaches the current trip voltage threshold ($V_{ITRIP-R}$), the H-bridge switches to slow decay mode, with the two low-side MOSFETs turned on.
- After a fixed off-time (t_{OFF}), if the load current drops to below 80% of the current trip voltage threshold, the diagonal pair of MOSFETs are re-enabled and the cycle repeats. If the current remains above 80%, the off time is extended until the current drops to 80% of the current trip voltage threshold.

The fixed off-time is determined by the setting of the OFF_T1:OFF_T0 bits in the CTRL5 register as follows:

Table 9: Fixed Off-Time Setting

OFF_T	Off Time t_{OFF}
00b (reset value)	20μS
01b	40μS
10b	60μS
11b	80μS

The current trip voltage threshold is reached when the ISET pin reaches 1.5V. As an example, with a 5kΩ resistor from ISET to ground, the ISET voltage is 0.5V/A of output current. So, when the current reaches 3A, the ISET pin voltage reaches 1.5V, and a current trip occurs.

For DC motors, current regulation is used to limit the start-up and stall current of the motor. Speed control is typically performed by providing an external PWM signal to the input pins.

If the current regulation feature is not needed, it can be disabled by connecting the ISET pin directly to ground.

If ILIMIT_M bit = 1b, after current regulation, the ILIMITx and FLT bits are set and the nFAULT pin is driven low. If ILIMIT_M bit = 0b, no fault report.

Cycle by Cycle Current Limit for Half-Bridge

For mode 3 and mode 4, the current in the each MOSFET is limited using constant off-time PWM (pulse width modulation) control circuitry. This operates as described below:

- Initially, a MOSFET of the half-bridge turns on (high-side MOSFET turn on with the load to GND, or low-side MOSFET turn on with the load to Vin) and drives current through the load.
- The current increases in the load, which is sensed by the internal current limit circuit.
- If the load current reaches the current limit voltage threshold (V_{ILIMIT}), the half-bridge switches to decay mode, with the other MOSFET of the half-bridge turned on.
- After a fixed off-time (t_{OFF}), the device resumes operation follow the input logic truth table and the cycle repeats. If after the t_{OFF} time has elapsed the current is still higher than the V_{ILIMIT} level, the device enforces another t_{OFF} time period of the same duration.

The current limit threshold is programmable as below table, which is related with over-current threshold.

It's necessary to set ILIMIT_LVL=11b to disable cycle by cycle current limit for full bridge applications in mode 1 and mode 2.

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Table 10: Current Limit Setting

ILIMIT_LVL	xx% of the over-current threshold
00b (reset value)	60%
01b	80%
10b	40%
11b	disabled

For DC motors, cycle by cycle current limit is used to limit the start-up and stall current of the motor. Speed control is typically performed by providing an external PWM signal to the input pins.

During current limit, the nFAULT pin is not activated unless the ILIMIT_M bit = 1b.

Deglitch Time and Blanking Time

There is often a current spike during the MOSFET turn-on, due to the body diode's reverse-recovery current or the shunt capacitance of the load. This current spike requires filtering to prevent the MOSFET from erroneously shutting down. The MP6611 has the internal programmable deglitch time for over-current protection and blanking time for current limit function. The blanking time T_{BLANK} blanks the output of the current sense comparator when the MOSFET turns on. This blanking time also sets the minimum on time for the MOSFET during current limit. For better current limit accuracy, it's suggested to set the blanking time larger than MOSFET rising/falling time.

The deglitch time is programmable by the OCD_T bits in the CTRL4 register according to the following table:

Table 11: OCP Deglitch Time Setting

OCD_T	OCP Deglitch time T_{OCP_D}
00b (reset value)	1μS
01b	0.5uS
10b	2μS
11b	4μS

The blanking time is programmable by the CLB_T bits in the CTRL4 register according to the following table:

Table 12: Current Regulation/Limit Blanking Time

CLB_T	Blanking time t_{BLANK}
00b (reset value)	1μS
01b	2uS
10b	4μS
11b	8μS

Slew Rate (SR) Control

To quickly reduce electromagnetic interference (EMI) generated by the output switching action, configurable slew rate control is integrated into the MP6611. The slew rate is programmable by the SR bits in the CTRL2 register according to the following table:

Table 13: Slew Rate Setting

SPI	Rising/Falling SR (V/μs)
000b	5
001b	9.6
010b	13
011b	19
100b (reset value)	28
101b	48
110b	96
111b	184

Charge Pump

An internal charge pump generates the gate drive for the HS-FETs. The charge pump frequency can be set to the four selections by the CP_F bits in the CTRL4 register according to the following table:

Table 14: Charge Pump Frequency Setting

CP_F	Charge Pump Frequency
00b (reset value)	3MHz
01b	1.5MHz
10b	750kHz
11b	375kHz

Diagnostic and Protection Functions

The MP6611 is fully protected against under-voltage, open-load, over-current, over-voltage and over-temperature events.

Over-Current Protection (OCP)

The MP6611 has internal short circuit protection. The currents in both the high-side and low-side MOSFETs are measured. If the current exceeds the over-current threshold (I_{OC}), all MOSFETs in

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the device are turned off for Mode 1/2/4, and over-current half-bridge is turned off for the Mode 3.

The over-current threshold and function is programmable by the OCP_M and OCP_LVL bits in the CTRL3 register according to the following table.

Table 15: Over-Current Protection Function

OCP_M	Protection function
00 (reset value)	Output Hi-Z, automatic retrying fault
01	Output Hi-Z, latched fault
10	report only but no action is taken
11	not reported and no action

Table 16: Over-Current Threshold

OCP_LVL	Min. OC Threshold
0 (reset value)	8.5A
1	11.5A

The OCP retry time is programmable by the OCR_T bits in the CTRL4 register according to the following table:

Table 17: OCP Retry Time Setting

OCR_T	OCP retry time T_{OCP}
00 (reset value)	10mS
01	4mS
10	1mS
11	0.5mS

Over-Temperature Warning

If the die temperature exceeds the thermal warning threshold T_{OTW}, the over-temperature warning is triggered. If the OTW_M =1b, then OTW and FLT bits in the FAULT register are set and the nFAULT pin is driven active low. All device functions remain operational. Once die temprature drops below T_{OTW} – T_{OTW_HY}, the nFAULT released. The FLT and OTW bits remain set until writing a ‘1’ to the OTW or FLT bit, or an nSLEEP reset pulse. If the OTW_M = 0b, then FLT bit and nFAULT pin no action when over-temperature warning.

Over-Temperature Shutdown

If the die temperature exceeds safe limits T_{SD}, all MOSFETs in the H-bridge are disabled. The TSD and FLT bits are set and the nFAULT pin is driven low.

If TSD_M = 0b, the nFAULTis released and the H-bridges are automatically re-enabled when the temperature drops below the T_{SD} - T_{SD_HY} threshold. The FLT and TSD bits remain set until writing a ‘1’ to the TSD or FLT bit, or an nSLEEP reset pulse.

If TSD_M = 1b, then this is a latched fault, the H-bridge and nFAULT are released until writing a ‘1’ to the TSD or FLT bit, or an nSLEEP reset pulse.

Table 18: Over-Temperature Shutdown Function

TSD_M	Protection function
0b (reset value)	Over-temperature condition causes an automatic recovery fault.
1b	Over-temperature condition causes a latched fault

VIN Under-Voltage Lockout (UVLO) and Under-Voltage Warning

If at any time the voltage on the VIN pin falls below the under-voltage lockout threshold voltage (UVLO), all the outputs (OUTx) are disabled. Operation resumes when VIN rises above the UVLO threshold.

If at any time the voltage on the VIN pin falls below the under-voltage warning threshold voltage (UVW), all device functions remain operational. If the UV_M =1b, then UVW and FLT bits in the FAULT register are set and the nFAULT pin is driven active low when under-voltage warning condition. The FLT and UVW bit remains set until it is cleared through writing a ‘1’ to UVW or FLT bit, or an nSLEEP reset pulse. If the UV_M = 0b, then UVW/FLT bit and nFAULT pin are no action when the voltage on the VIN pin falls below the under-voltage warning threshold voltage.

Over-Voltage Protection (OVP)

If the voltage on the VIN pin exceeds the input over-voltage threshold (V_{INOVP}), the device is disabled, the FLT and OVP bit in the FAULT register will be set, and the nFAULT pin will be driven low. Once VIN drops to a safe level, the MP6611 resumes normal operation, and nFAULT released. The FLT and OVP bit will remain set until writing a ‘1’ to the OVP or FLT bit, or an nSLEEP reset pulse.

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Table 19: Over-Voltage Protection Function

OVP_M	Protection function
000b (reset value)	37V OVP threshold, Over-voltage condition causes an automatic retrying fault
001b	37V OVP threshold, Over-voltage condition causes a latched fault
010b	30V OVP threshold, Over-voltage condition causes an automatic retrying fault
011b	30V OVP threshold, Over-voltage condition causes a latched fault
100b	30V OVP threshold, Over-voltage condition is report only but no action is taken
101b	22V OVP threshold, Over-voltage condition causes an automatic retrying fault
110b	22V OVP threshold, Over-voltage condition causes a latched fault
111b	22V OVP threshold, Over-voltage condition is report only but no action is taken

Charge Pump Under-Voltage Lockout (CPUV)

If at any time the voltage on the VCP pin falls below the $V_{VCP(UV)}$ voltage for the charge pump, all the outputs (OUTx) are disabled, and the nFAULT pin is driven low. The charge pump remains active during this condition. The FLT and CPUV bits are latched high in the SPI registers. Normal operation resumes (motor-driver operation and nFAULT released) when the VCP undervoltage condition is removed. The FLT and CPUV bit remains set until it is cleared through writing a '1' to the CPUV or FLT bit, or an nSLEEP reset pulse. This protection feature can be disabled by setting the CPUV_M bit high, then no CPUV fault reports, but all the outputs (OUTx) will be disabled until the VCP out of undervoltage condition (charged by internal charge pump).

Open Load Detection

If the motor is disconnected from the device, the MP6611 can detect the open load condition on the outputs, the OLD bit in the FAULT register will be set, and the nFAULT pin will be latched low. The fault clears until writing a '1' to the OLD bit or FLT bit, or an nSLEEP reset pulse, also clears when the device is power cycled or comes out of sleep mode. The OLD diagnostic delay time is programmable by the OLD_DLY bit set for different applications.

Table 20: OLD Diagnostic Delay Time Setting

OLD_DLY	OLD diagnostic delay time T_{OLD_DLY}
0 (reset value)	0.3mS
1	1.2mS

The open load detection works only in standby mode. OLD_STANDBY detects the presence of the motor prior to commutating the motor.

OLD_STANDBY Test

When device is in standby mode (DIS bit = 1b), OLD_STANDBY test is performed follow below steps:

1. Power up the device

2. Set DIS bit = "1".

3. Write "1" to the EN_OLDS bit to enable open load detection

4. Perform the OLD_STANDBY test. MP6611 will generate a sink or source current (around 1.5mA) to output to detect whether the load connection is ready (OUT1 and OUT2 take turns).

- If an open load (OL) is detected, the nFAULT pin is driven low, the FLT and OLD (OLDx) bits are latched high. Then the EN_OLDS bits will return to the default setting ("0").

– If an OL condition is not detected, the EN_OLDS bits will return to the default setting ("0") after the T_{OLD_DLY} time expires.

5. Set the DIS bit "0" to enable the device for normal operation.

The DIS bit must remain "1" for the entire duration of the OLD_STANDBY test. While the OLD_STANDBY test is running, if the DIS bit is issued to "0", the OLD_STANDBY test will be stopped to resume normal operation and no fault is reported. And the OLD_STANDBY test is not performed if the motor is energized.

Output short Detection in Mode1/2

In Mode1/2, the MP6611 can detect short condition on the outputs in standby mode.

If output short to VIN or GND, the OCP/SCP bit in the FAULT register will be set. The fault clears until writing a '1' to the OCP/SCP bit or FLT bit, or an nSLEEP reset pulse, also clears when the

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device is power cycled or comes out of sleep mode.

When device is in standby mode (DIS bit = 1b), output short detection test is performed follow below steps:

1. Power up the device

2. Set DIS bit = “1”.

3. Write “1” to the EN_OSD bit to enable output short detection

4. Perform the output short detection test. MP6611 will generate a sink or source current (around 1.5mA mA) to output to detect whether the output pins are shorted to VIN or GND (OUT1 and OUT2 take turns). The nFAULT pin will be latched low.

- If an output short condition is detected, the FLT and OCP/SCP bit are latched high. Then the EN_OSD bit will return to the default setting (“0”).

– If an output short condition is not detected, the EN_OSD bit will return to the default setting (“0”) after the T_{OLD_DLY} time expires.

5. Set the DIS bit “0” to enable the device for normal operation.

The DIS bit must remain “1” for the entire duration of the output short detection test. While the output short detection test is running, if the DIS bit is issued to “0”, the test will be stopped to resume normal operation and no fault register is reported. The nFAULT pin will be low until writing a ‘1’ to the FLT bit, or an nSLEEP reset pulse.

And the output short detection test is not performed if the motor is energized.

Fault Indication Output

The nFAULT pin should be clear once by writing a ‘1’ to the FLT bit, or an nSLEEP reset pulse, after MP6611 startup with VIN or nSLEEP.

The MP6611 provides an nFAULT pin that is driven active low if any of the protection circuits are activated, or if the output short detection test is performed.

These fault conditions include over-current (OC), over-temperature (OT), over-temperature warning (OTW), open load, under-voltage lockout (UVLO), under-voltage warning and over-voltage (OV). nFAULT is an open-drain output, and requires an external pull-up resistor.

Once all fault conditions removed and device operation resumed, nFAULT is pulled inactive high by the pull-up resistor.

The source of the fault can be determined by reading the FAULT register through the SPI interface.

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Table 21: Diagnostic and Fault Summary Table

Fault	Condition	Device Action	Recovery operation	Bits set	Bits cleared by	nFAULT flag
Overcurrent	$I_{OUT} > I_{OCP}$, OCP_M = 00b	All Outputs Hi-Z (Mode1/2/4) Half-bridge Hi-Z (Mode3)	Automatic retry after a certain recovery time	OCP/SCP, OCP_xx, FLT	Write '1' to OCP/SCP or write '1' to FLT bit	nFault = L, until $I_{OUT} < I_{OCP}$
	$I_{OUT} > I_{OCP}$, OCP_M = 01b		latched shutdown, until Write '1' to OCP/SCP or write '1' to FLT bit	OCP/SCP, OCP_xx, FLT		nFault = L, until OCP/SCP bit is cleared
	$I_{OUT} > I_{OCP}$, OCP_M = 10b	Unaffected	-	OCP/SCP, OCP_xx, FLT		nFault = H
	$I_{OUT} > I_{OCP}$, OCP_M = 11b	Unaffected	-	-		nFault = H
VIN Overvoltage	$V_{IN} > V_{OVP}$ OVP_M = 000b, 010b, 101b	All Outputs Hi-Z	Automatic recovery with $V_{IN} < V_{OVP}$	OVP, FLT	Write '1' to OVP or FLT bit	nFault = L, until $V_{IN} < V_{OVP}$
	$V_{IN} > V_{OVP}$ OVP_M = 001b, 011b, 110b	All Outputs Hi-Z	latched shutdown, until write '1' to OVP or FLT bit			nFault = L, until OVP bit is cleared
	$V_{IN} > V_{OVP}$ OVP_M = 100b, 111b	Unaffected	-			nFault = L, until $V_{IN} < V_{OVP}$
VIN Under-voltage Lockout	$V_{IN} < V_{UVLO}$	All Outputs Hi-Z	Automatic recovery $V_{IN} > V_{UVLO}$	-	-	When $V_{IN} > V_{UVLO}$, all register reset
VIN Under-voltage warning	$V_{IN} < V_{UVW}$, UV_M= 0b	Unaffected	-	-	-	nFault = H
	$V_{IN} < V_{UVW}$, UV_M= 1b			UVW, FLT	Write '1' to UVW or FLT bit	nFault = L, until $V_{IN} > V_{UVW}$
VCP Under-voltage	$V_{CP} < V_{CP_UVLO}$ DIS_CPUV=0b	All Outputs Hi-Z	Automatic recovery $V_{CP} > V_{CP_UVLO}$	CPUV, FLT	Write '1' to CPUV or FLT bit	nFault = L until $V_{CP} > V_{CP_UVLO}$
	$V_{CP} < V_{CP_UVLO}$ DIS_CPUV=1b	All Outputs Hi-Z	Automatic recovery $V_{CP} > V_{CP_UVLO}$	-	-	nFault = H

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Thermal Warning	$T_J > T_{OTW}$, OTW_M= 0b	Unaffected	-	-	-	nFault = H
	$T_J > T_{OTW}$, OTW_M= 1b			OTW, FLT	Write '1' to OTW or FLT bit	nFault = L, Until $T_J < T_{OTW} - T_{OTW_HY}$
Thermal Shutdown	$T_J > T_{SD}$, TSD_M= 0b	All Outputs Hi-Z	Automatic recovery with $T_J < T_{SD} - T_{SD_HY}$	TSD, FLT	Write '1' to TSD or FLT bit	nFault = L, Until $T_J < T_{SD} - T_{SD_HY}$
	$T_J > T_{SD}$, TSD_M= 1b	All Outputs Hi-Z	latched shutdown, until write '1' to TSD or FLT bit	TSD, FLT	Write '1' to TSD or FLT bit	nFault = L, Until TSD bit is cleared
OUT short to VIN or GND	OUTx > 1.4V for short to VIN test, OUTx < 0.8V, for short to GND test	All Outputs Hi-Z	latched shutdown, until write '1' to OCP/SCP or write '1' to FLT bit	OCP/SCP, FLT	Write '1' to OCP/SCP or write '1' to FLT bit	-
Open Load	Open load	Unaffected	-	OLD, FLT	Write '1' to OLD or FLT bit	nFault = L, Until OLD bit is cleared
Current regulation/limit	$I_{OUT} > I_{TRIP}$ or I_{LIMIT} ILIMIT_M = 0b	Decay mode	Automatic recovery	-	-	nFault = H
	$I_{OUT} > I_{TRIP}$ or I_{LIMIT} ILIMIT_M = 1b	Decay mode	Automatic recovery	ILIMIT1 or ILIMIT2, FLT	Write '1' to ILIMITx or FLT bit	nFault = L until off time finished or $I_{OUT} < 80\% \times I_{TRIP}$

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Serial (SPI) Control Interface

A serial interface is used to configure the control modes, as well as to read back the detailed diagnostics. Serial data is clocked in to the SDI pin by rising edges on the SCK pin, while the nSCS pin is held active low. SDO is driven while nSCS is active low, and high impedance when nSCS is inactive high. For a write command, the new data is written to the selected register on the rising edge of the nSCS input. The SPI interface uses a 16-bit serial data packet, include Header/Status/Address/Data bytes. SDI data composed of 5-bits register address, one read/write bit (“1” = write, “0” = read), and 8 data bits.

- Data on SDO from the device is propagated on the falling edge of SCLK, while data on SDI is captured by the device on the subsequent rising edge of SCLK.
- For SDI data, the third bit is a read/write bit. If clear (“0” = read), the data sent is ignored and register data is read out on the SDO pin. If set (“1” = write), the next 13 bits sent are latched into the selected register at the end of the transfer.
- The next five bits are the register address. They select both the source of data to be shifted out the SDO pin, as well as the destination of the new data being shifted in.
- The addressed register is updated on the rising edge of the nSCS input.
- While nSCS pin is driven low, a status byte (7-bits, S6:S0 bits) is clocked out before the 8-bit data, which are the FAULT flag reports. This allows a check of important status during every SPI transaction.The SCLK pin should be high when the nSCS pin transitions from high to low and from low to high.
- The nSCS pin should be pulled high for at least 500ns between words.
- The most significant bit (MSB) is shifted in and out first.
- When the nSCS pin is pulled high, any signals at the SCLK and SDI pins are ignored and the SDO pin is set Hi-Z.

SPI data transfers are performed as shown in the waveform below:

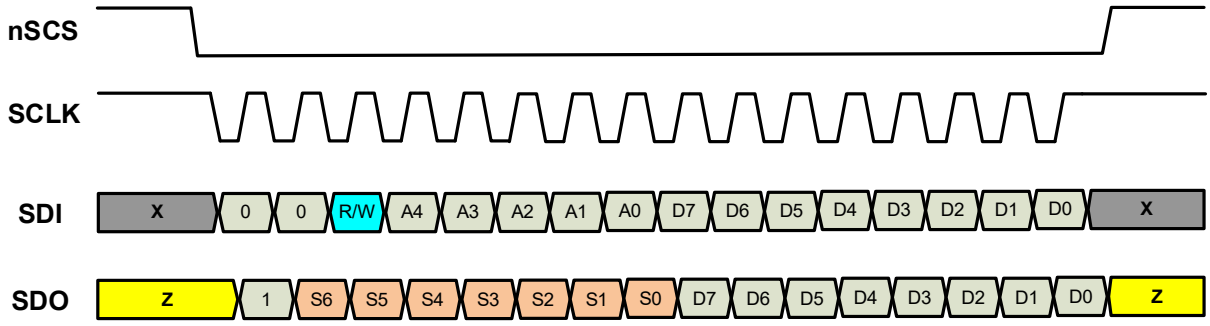

Figure 8: SPI Interface Timing

Daisy Chain

The device can be connected in a daisy chain configuration when multiple devices are communicating to the same MCU, for example three devices as below.

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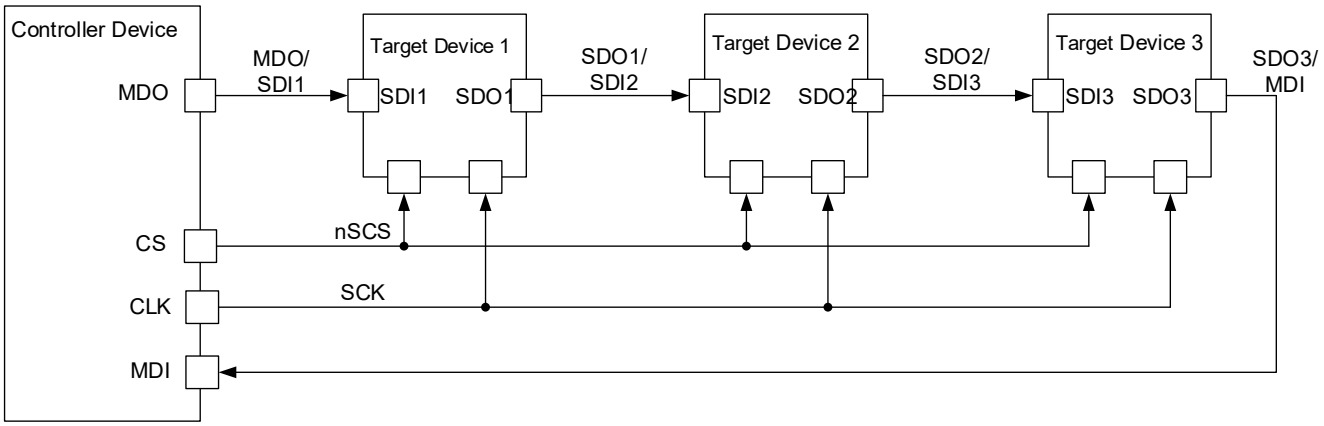

Figure 9: Three Devices Connected in Daisy Chain

There is the HDR header byte, which contain information of the number of devices connected in the chain, and a global clear fault command that will clear the fault registers of all the devices on the rising edge of the chip select (nSCS) signal. CLR bit is an auto-clear bit and will always read 0b, write 0b means “Faults not cleared”, write 1b means “Clear all faults”. Header values N4 through N0 are 5 bits dedicated to show the total number of the devices in the chain, so up to 31 devices can be connected in series for each daisy chain connection.

After the data has been transmitted through the chain, the MCU receives the data string in the following format, for example for 3-device configuration: 3 bytes of status (Sx), 1 byte of header (HDR), 3 bytes of output data (DOx). So for N-device configuration, the MCU will receive the data string: N bytes of status (Sx), 1 byte of header (HDR), N bytes of output data (DOx).

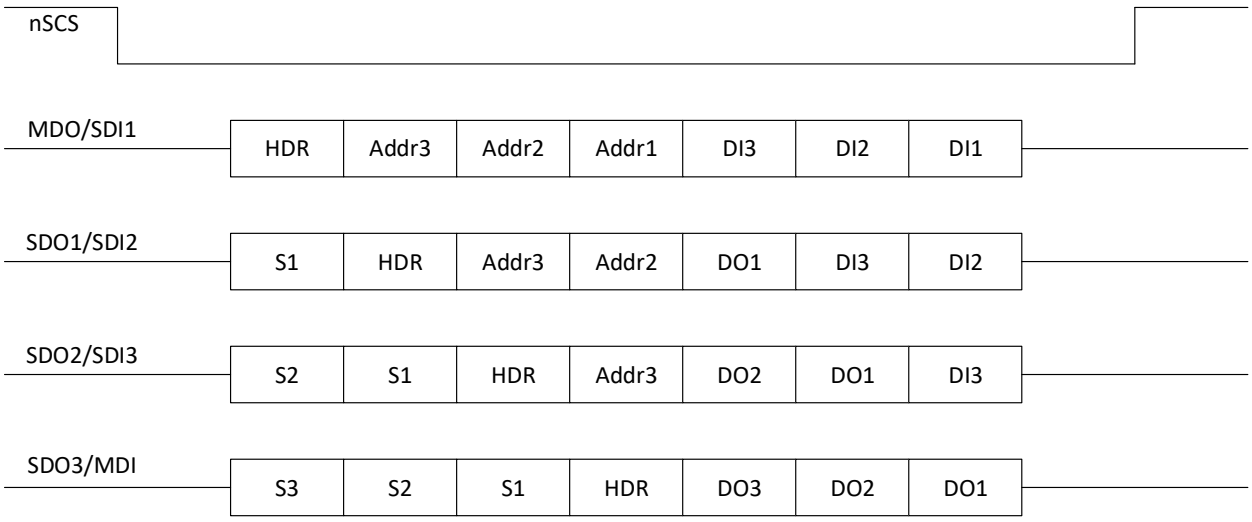

Figure 10: SPI Frame with Three Devices

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All bytes Descriptions:

	Symbol	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Header Bytes	HDR	0	1	CLR	N4	N3	N2	N1	N0
Status Byte	Sx	1	OTW	UVW	CPUV	OCP/SCP	TSD	OLD	OVP
Address Byte	Addrx	0	0	R/W	A4	A3	A2	A1	A0
Data Byte	DIx/DOx	D7	D6	D5	D4	D3	D2	D1	D0

Register Map Table

Address Byte	Register name	D7	D6	D5	D4	D3	D2	D1	D0
0x00	FAULT Status	FLT	OTW	UVW	CPUV	OCP/SCP	TSD	OLD	OVP
0x01	DIAG Status	OLD1	OLD2	ILIMIT1	ILIMIT2	OCP_H1	OCP_L1	OCP_H2	OCP_L2
0x02	CTRL1	DIS	DIS_OUT1	DIS_OUT2	EN_OLDS	EN_OLDA	SPI_IN	SPI_IN1	SPI_IN2
0x03	CTRL2	RSVD	EN_OSD	SR2	SR1	SR0	BRAKE	UV_M	CPUV_M
0x04	CTRL3	TSD_M	OTW_M	OCP_M1	OCP_M0	OCP_LVL	OVP_M2	OVP_M1	OVP_M0
0x05	CTRL4	OCD_T1	OCD_T0	OCR_T1	OCR_T0	CLB_T1	CLB_T0	CP_F1	CP_F0
0x06	CTRL5	OFF_T1	OFF_T0	OLD_DLY	ILIMIT_M	ILIMIT_LVL1	ILIMIT_LVL0	Load_OUT1	Load_OUT2

FAULT

Address: 0x00

The FAULT register is used for fault indication and fault clearing.

Bits	Access	Bit Name	Default	Description
7	R/W	FLT	0b	Global FAULT status register. Logical ‘OR’ of other fault bits. Compliments the nFAULT pin. Write a 1b to clear the all FAULT and DIAG Status bits.
6	R/W	OTW	0b	Indicates over-temperature warning
5	R/W	UVW	0b	Indicates under-voltage warning
4	R/W	CPUV	0b	Indicates charge-pump under-voltage fault condition
3	R/W	OCP/SCP	0b	Indicates an overcurrent condition
2	R/W	TSD	0b	Indicates an over-temperature shutdown
1	R/W	OLD	0b	Indicates an open-load detection
0	R/W	OVP	0b	Indicates an over-voltage fault condition

NOTE: Bits in the FAULT register are cleared by writing a ‘1’ to them – writing a ‘0’ has no effect.

DIAG Status

Address: 0x01

The DIAG register is used for fault indication and fault clearing.

Bits	Access	Bit Name	Default	Description
7	R	OLD1	0b	Indicates open-load detection on half bridge 1
6	R	OLD2	0b	Indicates open-load detection on half bridge 2
5	R/W	ILIMIT1	0b	Indicates the current regulation status of full bridge or the limit status of half bridge 1.
4	R/W	ILIMIT2	0b	Indicates the current limit status of half bridge 2.
3	R	OCP_H1	0b	Indicates overcurrent fault on the high-side FET of half bridge 1
2	R	OCP_L1	0b	Indicates overcurrent fault on the low-side FET of half bridge 1

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1	R	OCP_H2	0b	Indicates overcurrent fault on the high-side FET of half bridge 2
0	R	OCP_L2	0b	Indicates overcurrent fault on the low-side FET of half bridge 2

NOTE: Bits in the ILIMIT1/ILIMIT2 are cleared by writing a '1' to them – writing a '0' has no effect.

CTRL1

Address: 0x02

The CTRL1 register is used to enable or disable power stage, enable the open load diagnostic in standby mode, sets the input logic control.

Bits	Access	Bit Name	Default	Description
7	R/W	DIS	0b	Disable mode, the device power stage in Hi-Z 0b: all power stage enabled 1b: all power stage disabled (Hi-Z)
6	R/W	DIS_OUT1	0b	Disable mode, only in the Mode 3 (2 x half-bridges) 0b: Half bridge 1 enabled 1b: Half bridge 1 disabled (Hi-Z)
5	R/W	DIS_OUT2	0b	Disable mode, only in the Mode 3 (2 x half-bridges) 0b: Half bridge 2 enabled 1b: Half bridge 2 disabled (Hi-Z)
4	R/W	EN_OLDS	0b	0b: not in open load standby mode test 1b: run open load diagnostic in standby mode When open load test complete EN_OLDS returns to 0b (status check)
3	R/W	RSVD	0b	This bit must be default to 0b.
2	R/W	SPI_IN	0b	0b: Outputs follow input pins 1b: Outputs follow SPI registers or a combination of SPI and input pins.
1	R/W	SPI_IN1	0b	SPI input logic control, XOR'ed with the IN1/ENBL/PWM pin value (when SPI_IN = 1b).
0	R/W	SPI_IN2	0b	SPI input logic control, XOR'ed with the IN2/DIR/EN pin value (when SPI_IN = 1b).

CTRL2

Address: 0x03

The CTRL2 register is used to enable the output short detection in standby mode, sets the slew rate, enable or disable low Iq brake mode, as well as UVW, CPUV functions.

Bits	Access	Bit Name	Default	Description
7	R/W	RSVD	-	-
6	R/W	EN_OSD	0b	0b: not in output short detection test 1b: run output short detection test in standby mode When output short detection test is complete EN_OSD returns to 0b (status check)
5:3	R/W	SR	100b	000b: 5 V/μs 001b: 9.6 V/μs 010b: 13 V/μs 011b: 19 V/μs 100b: 28 V/μs 101b: 48 V/μs 110b: 96 V/μs 111b: 184 V/μs

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2	R/W	BRAKE	0b	Low Iq Brake mode enable. 0b: no active 1b: brake mode (two low-side MOSFETs turn on for full bridge mode; follow Low Iq Brake Mode Setup table for half bridge mode)
1	R/W	UV_M	0b	0b: UVW is not reported on nFAULT or the UVW/FLT bit 1b: UVW is reported on nFAULT and the UVW/FLT bit
0	R/W	CPUV_M	0b	0b: Charge pump under-voltage fault is reported on nFAULT and the CPUV/FLT bit. 1b: Charge pump under-voltage fault is not reported on nFAULT or the CPUV/FLT bit.

CTRL3

Address: 0x04

The CTRL3 register sets TSD, OTW, OCP, OVP functions.

Bits	Access	Bit Name	Default	Description
7	R/W	TSD_M	0b	0b: Over-temperature condition causes an automatic recovery fault 1b: Over-temperature condition causes a latched fault
6	R/W	OTW_M	0b	0b: OTW is not reported on nFAULT or the OTW/FLT bit. 1b: OTW is reported on nFAULT and the OTW/FLT bit.
5:4	R/W	OCP_M	00b	00b: Overcurrent condition causes an automatic retrying fault 01b: Overcurrent condition causes a latched fault 10b: Overcurrent condition is report on OCP/SCP, OCP_xx, FLT bit only but no action is taken 11b: Overcurrent condition is not reported and no action is taken
3	R/W	OCP_LVL	0b	0b: 11A 1b: 14.5A
2:0	R/W	OVP_M	000b	000b: 37V OVP threshold, Over-voltage condition causes an automatic retrying fault 001b: 37V OVP threshold, Over-voltage condition causes a latched fault 010b: 30V OVP threshold, Over-voltage condition causes an automatic retrying fault 011b: 30V OVP threshold, Over-voltage condition causes a latched fault 100b: 30V OVP threshold, Over-voltage condition is report only but no action is taken 101b: 22V OVP threshold, Over-voltage condition causes an automatic retrying fault 110b: 22V OVP threshold, Over-voltage condition causes a latched fault 111b: 22V OVP threshold, Over-voltage condition is report only but no action is taken

CTRL4

Address: 0x05

The CTRL4 register sets the OCP deglitch time, OCP retry time, current limit blanking time and charge pump frequency.

Bits	Access	Bit Name	Default	Description
7:6	R/W	OCD_T	00b	OCP Deglitch time setting
5:4	R/W	OCR_T	00b	OCP Retry time setting

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3:2	R/W	CLB_T	00b	Current limit blanking time setting
1:0	R/W	CP_F	00b	Charge Pump Frequency setting

CTRL5

Address: 0x06

The CTRL5 register sets the current limit functions, open load detection delay time, as well as the load information for Mode 3/4 (half-bridges mode)

Bits	Access	Bit Name	Default	Description
7:6	R/W	OFF_T	00b	Constant off time setting
5	R/W	OLD_DLY	0b	Open load detection delay time setting
4	R/W	ILIMIT_M	0b	0b: ITRIP/LIMIT is not reported on nFAULT or the ILIMITx /FLT bit. 1b: ITRIP/LIMIT is reported on nFAULT and the ILIMITx /FLT bit.
3:2	R/W	ILIMIT_LVL	00b	00b: current limit threshold is 60% of the over-current limit threshold 01b: current limit threshold is 80% of the over-current limit threshold 10b: current limit threshold is 40% of the over-current limit threshold 11b: current limit function disabled
1	R/W	Load_OUT1	0b	For Mode 3/4 (half-bridges mode), do need to provide the load information of the half-bridge. For mode 3, it's the load information of half-bridge1. For Mode 4 (mono half-bridge), Load_OUT1 and Load_OUT2 bit should be same. 0b: load connect from OUT to GND 1b: load connect from OUT to VIN
0	R/W	Load_OUT2	0b	For Mode 3/4 (half-bridges mode), do need to provide the load information of the half-bridge. For mode 3, it's the load information of half-bridge2. For Mode 4 (mono half-bridge), Load_OUT1 and Load_OUT2 bit should be same. 0b: load connect from OUT to GND 1b: load connect from OUT to VIN

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APPLICATION INFORMATION

Selecting the VCP and VCC External Capacitors

Table 22 lists the recommended external VCP and VCC capacitors.

Table 22: Recommended External VCP/VCC Capacitors

Charge Pump and VCC Capacitors	Min	Typ	Max	Units
VCP to VIN capacitance		1		µF
VCP to VIN capacitor voltage	10			V
VCC capacitance	4.7		10	µF
VCC capacitor voltage	10			V

PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For the best results, refer to Figure 5, and follow the guidelines below:

1. Place the supply bypass capacitors and charge pump capacitors as close to the IC as possible (ideally, place these capacitors on the same PCB layer between VIN and GND, VCC and GND, and VCP and VIN).
2. Supply bypass capacitors and charge pump capacitors can also be placed on the opposite side of the PCB directly under the IC. Use vias to make these connections.
3. Place as much copper on the long pads as possible.
4. Place large copper areas on the pads and on the same outer copper layer as the IC.
5. Place thermal vias inside the pad area to dissipate heat to the copper layers.
6. If via-in-pad construction is not possible, place multiple vias just outside the pad area.

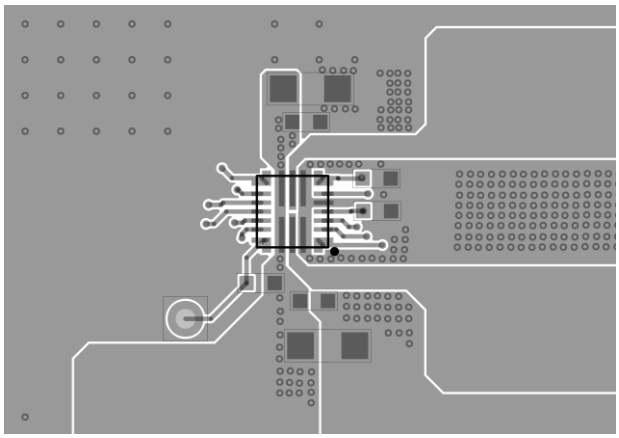

Figure 11: Recommended PCB Layout

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TYPICAL APPLICATION CIRCUITS

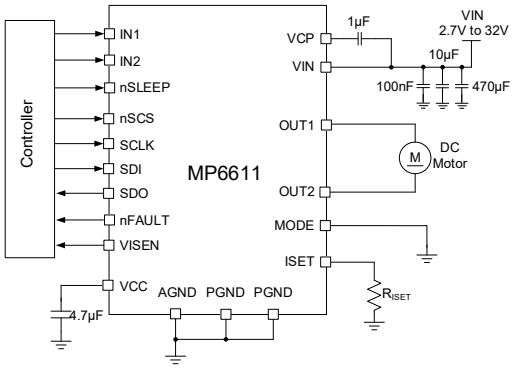

Figure 12: Full Bridge with IN1/IN2 Input

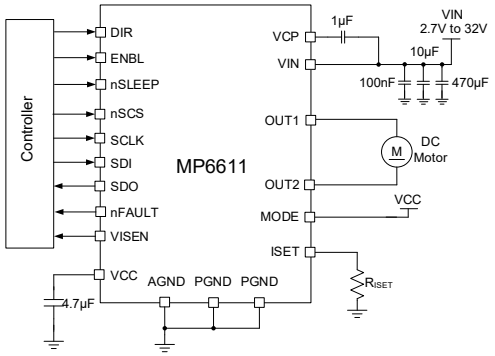

Figure 13: Full Bridge with DIR/ENBL Input

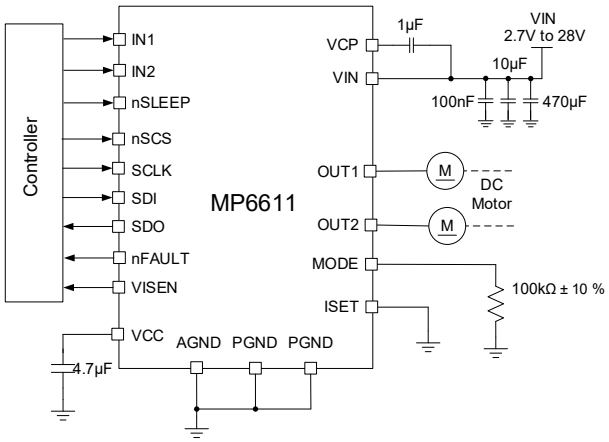

Figure 14: 2x Half Bridge with independent PWM Input(8)

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TYPICAL APPLICATION CIRCUITS *(continued)*

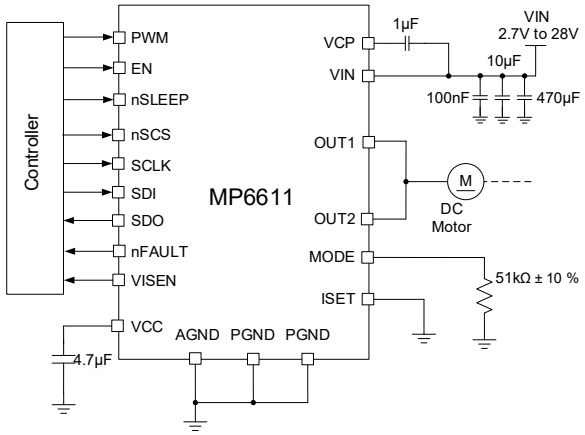

Figure 15: Parallel Half Bridge(8)

Note:

8) For half bridge application, if load is connected to VIN, the recommended operating voltage is 2.7V to 28V.

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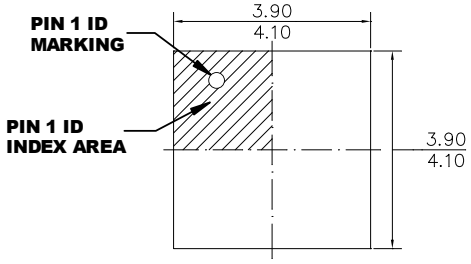
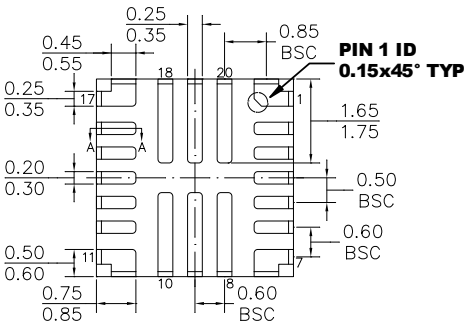
PACKAGE INFORMATION

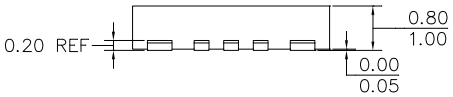
QFN-20 (4mmx4mm)



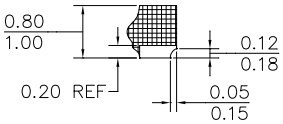
TOP VIEW



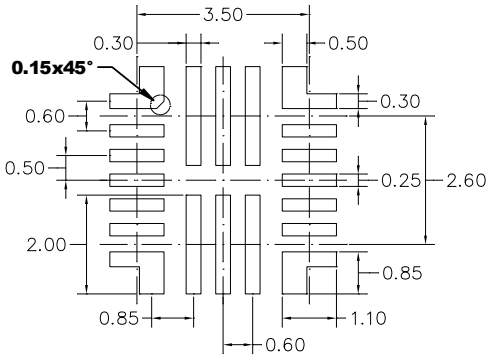
BOTTOM VIEW



SIDE VIEW



SECTION A-A



RECOMMENDED LAND PATTERN

NOTE:

1) THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

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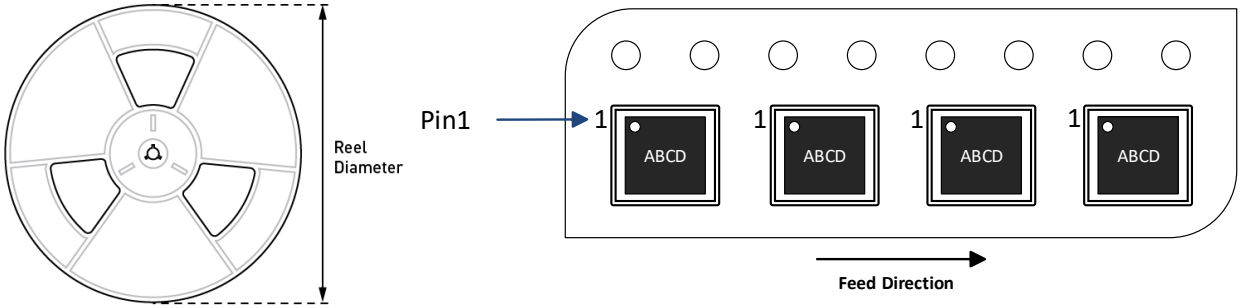
CARRIER INFORMATION



Part Number	Package Description	Quantity /Reel	Quantity /Tube	Quantity /Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP6611GRE-Z	QFN-20 (4mm×4mm)	5000	N/A	N/A	13 in.	12 mm	8 mm

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