MP5472

Fully Integrated, 12V, 6A, Dual-Output PMIC with I²C Interface and Flexible System Configurations

DESCRIPTION

The MP5472 is a complete power management IC (PMIC) that integrates two high-efficiency, step-down DC/DC converters, one adjustable-output low-dropout (LDO) regulator, and a flexible logic interface.

The integrated DC/DC converters provide constant-on-time (COT) control for fast transient response. The configurable 500kHz to 1.25MHz switching frequency (f_{SW}) minimizes the external inductor and capacitor size. Full protection features include under-voltage lockout (UVLO), over-current protection (OCP), under-voltage protection (UVP), and thermal shutdown.

The output voltage (V_{OUTx}) (where x = 1 or 2) can be adjusted via the I²C bus, or it can be preset by the multiple-time programmable (MTP) memory. The start-up/shutdown sequence can also be configured by the MTP, or it can be controlled online via the I²C.

The two rails can work in either independent mode or parallel mode, which can be configured. The current-sharing function is implemented in parallel mode.

The MP5472 requires a minimal number of external components, and it is available in a space-saving QFN-26 (4mmx4mm) package.

FEATURES

- Wide 3V to 16V Input Voltage (V_{IN}) Range
- Adaptive Constant-On-Time (COT) Control for Ultra-Fast Transient Response
- Two High-Efficiency Step-Down Converters
  - Buck 1: 12A DC/DC Converter, 15mΩ/5mΩ
  - Buck 2: 12A DC/DC Converter, 15mΩ/5mΩ
- Bucks 1/2 Support up to 12A of Continuous Current in Dual-Phase Mode
- One 500mA Low-Dropout (LDO) Regulator with Adjustable Output Voltage
- I²C-Configurable Reference Voltage (V_{REF}) with Slew Rate Control
- Configurable Switching Frequency (f_{SW}): 500kHz, 750kHz, 1MHz, 1.25MHz
- Accurate Output Voltage (V_{OUT}), Output Current (I_{OUT}), and Junction Temperature (T_J) Monitoring via the I²C
- Open-Drain Power Good (PG) Indication and General Status Interrupt
- Multiple-Time Programmable (MTP) Memory Soft Start/Soft Shutdown and Delay with MPS-Patented FLEX-Timer Sequence Control
- Selectable PFM/PWM Mode, Adjustable Frequency and Current Limit via the I²C
- Over-Current Protection (OCP), Under-Voltage Protection (UVP), Over-Voltage Protection (OVP), and Thermal Shutdown Protection
- Available in a QFN-26 (4mmx4mm) Package

MPL Optimized Performance with MPS Inductor MPL-4020 Series

APPLICATIONS

- Storage and Networking
- Enterprise Solid-State Drives (SSDs)
- General Enterprise Applications

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TYPICAL APPLICATIONS

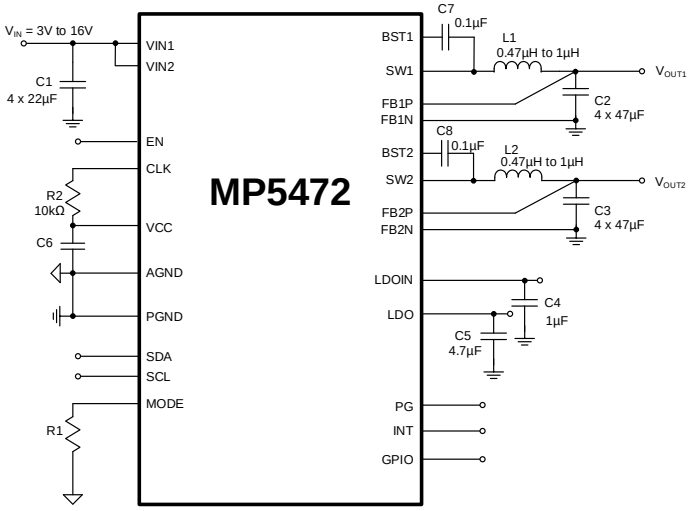
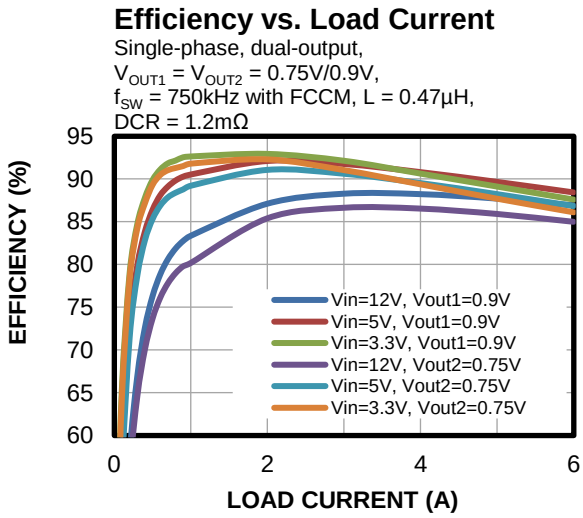


Figure 1: Typical Application (Single-Phase Mode)



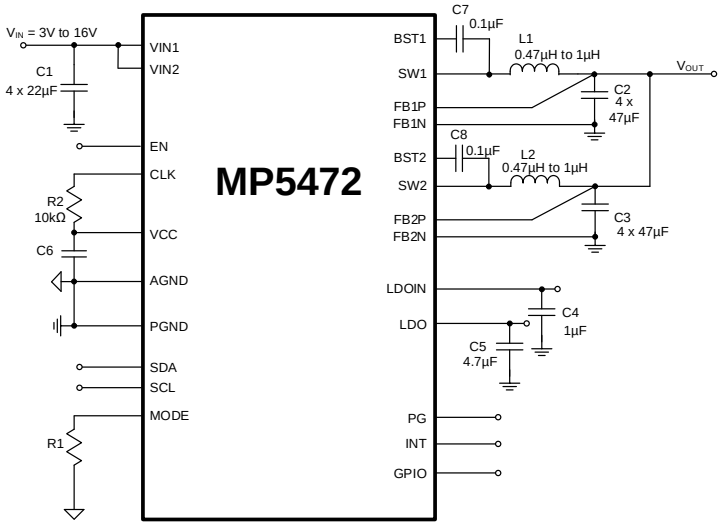


Figure 2: Typical Application (Dual-Phase Mode)

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ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP5472GR-xxxx**	QFN-26 (4mmx4mm)	*See Below*	1
MP5472GR-0000			

* For Tape & Reel, add suffix -Z (e.g. MP5472GR-xxxx-Z).

** "xxxx" is the configuration code identifier for the register setting stored in the MTP. The default number is "0000". The MP5472GR-0000 is the default version. Each "x" can be a hexadecimal value between 0 and F. Work with an MPS FAE to create this unique number, even if ordering the "0000" code.

TOP MARKING

MPSYWW
MP5472
LLLLLL

MPS: MPS prefix
Y: Year code
WW: Week code
MP5472: Part number
LLLLLL: Lot number

EVALUATION KIT (EVKT-MP5472)

EVKT-MP5472 kit contents:

#	Part Number	Item	Quantity
1	EVL5472-Q-00A	MP5472GR evaluation board	1
2	EVKT-USBI2C-02	Communication Interface Device USB to I²C/PMBus, included with product evaluation kit or can be purchased separately.	1
3	MP5472GR-0000	IC with default configuration, which can be used for MTP and MODE0~7 configurations	1
4	Virtual Bench Pro 4.0	Software to configure and monitor I²C digital parts and evaluation kits.	1

Order directly from MonolithicPower.com or our distributors.

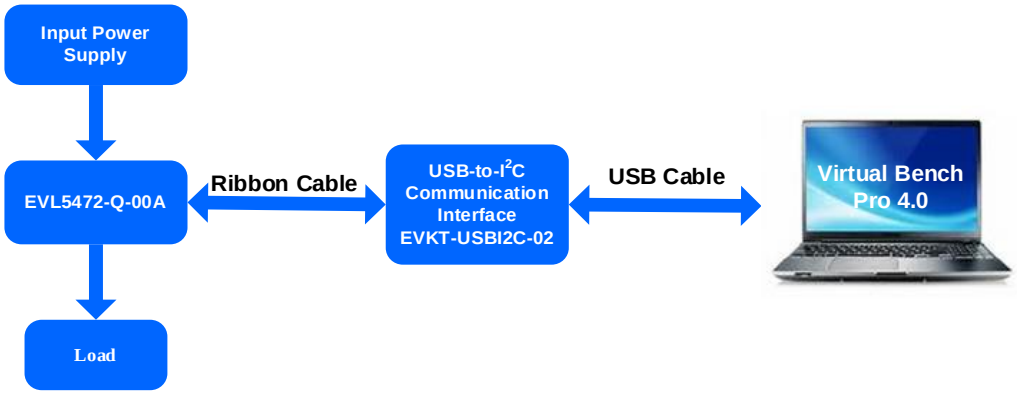

Figure 3: Evaluation Kit Set-Up

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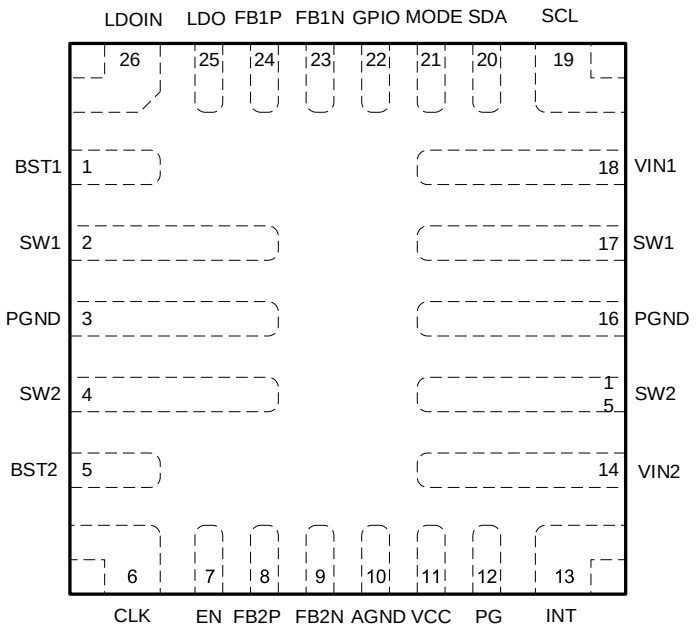
PACKAGE REFERENCE



QFN-26 (4mmx4mm)

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PIN FUNCTIONS

Pin #	Name	Description
1	BST1	**Buck 1 bootstrap.** Connect a capacitor between SW1 and BST1 to form a floating supply across buck converter 1's high-side switch driver.
2, 17	SW1	**Buck 1 switch output.** Connect SW1 using a wide PCB trace.
3, 16	PGND	**Power ground.** PGND requires special consideration during PCB layout. Connect PGND with copper traces and vias.
4, 15	SW2	**Buck 2 switch output.** Connect SW2 using a wide PCB trace.
5	BST2	**Buck 2 bootstrap.** Connect a capacitor between SW2 and BST2 to form a floating supply across buck converter 2's high-side switch driver.
6	CLK	**Clock pin for FLEX-Time Control.** CLK is an open-drain, bidirectional pin. Pull CLK up to the VCC voltage (V_{CC}) through a resistor (typically 10kΩ). For FLEX-Time Control, all CLK pins should be connected together and pulled up to the VCC pin via a resistor. See the FLEX-Time Sequence Control section on page 23 for more details.
7	EN	**Enable pin of the chip.** Drive EN high to turn on the chip. Drive EN low or float EN to turn off the chip. EN has an internal 2MΩ pull-down resistor connected to ground.
8	FB2P	**Positive feedback for buck 2's remote sense.**
9	FB2N	**Negative feedback for buck 2's remote sense.**
10	AGND	**Analog ground.** Connect AGND to the power ground pin.
11	VCC	**Internal 3.6V LDO output.** The driver of the FETs is powered from V_{CC}. Decouple VCC with a 1μF ceramic capacitor placed as close to VCC as possible. X7R- or X5R-grade dielectric ceramic capacitors are recommended due to their stable temperature characteristics.
12	PG	**Power good output, open drain.** Pull PG low when any enabled regulator (buck 1, buck 2, and the LDO) falls below the under-voltage (UV) threshold or exceeds the over-voltage (OV) threshold. Pull PG low when all regulators are disabled. PG is an input signal for the stop clock. If the PG voltage exceeds 2.3V, the CLK pin stops to generate a clock after finishing the clock number count.
13	INT	**General status interrupt.** INT is an open-drain output. The converter asserts INT low to communicate any one or more critical events to the host: power good (PG) indication, over-temperature warning (OTW), over-temperature (OT), over-current (OC), and UV. INT remains asserted until the appropriate registers are explicitly cleared or the converter is reset. When any status bit in Register 0x19 or 0x1A is changed to "1", and its corresponding MASK bit in 0x1B or 0x1C is set to "0", a low level is output on the INT pin.
14	VIN2	**Supply voltage of buck 2.** Ceramic capacitors are required to decouple the input rail. Connect VIN2 using a wide PCB trace. VIN1 and VIN2 must be connected to the same bus voltage.
18	VIN1	**Supply voltage of buck 1.** Ceramic capacitors are required to decouple the input rail. Connect VIN1 using a wide PCB trace. VIN1 and VIN2 must be connected to the same bus voltage.
19	SCL	**I²C bus clock.** SCL supports a 1.8V/3.3V bus voltage. If this pin is not used, pull it up to VCC.
20	SDA	**I²C bus data.** SDA supports a 1.8V/3.3V bus voltage. If this pin is not used, pull it up to VCC.
21	MODE	**MTP selection pin.** Connect a resistor to this pin to select the MTP configurations of certain features. See the MODE Pin Determined MTP Configuration section on page 22 for more details.
22	GPIO	**GPIO pin.** The GPIO pin can be configured into the start-up sequence with the regulators or an analog input for the analog-to-digital converter (ADC) circuit. Float this pin or connect it to ground if it is not used.
23	FB1N	**Negative feedback of buck 1 remote sense.**
24	FB1P	**Positive feedback of buck 1 remote sense.**
25	LDO	**Output of the 500mA LDO.**
26	LDOIN	**Input of the 500mA LDO.** The voltage of this pin should be below 3.6V.

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ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN1}, V_{IN2}) 18V
$V_{SW1(DC)}$, $V_{SW2(DC)}$.....-0.3V (-5V for < 10ns) to V_{IN} + 0.3V (+23V for <10ns)
V_{BST1}, V_{BST2}.....$V_{SW1/2}$ + 4V
EN .....-0.3V to +5V
All other pins .....-0.3V to +4V
Continuous power dissipation (T_A = 25°C) (2)
QFN-26 (4mmx4mm) 3.68W
Junction temperature (T_J) .....150°C
Lead temperature .....260°C
Storage temperature ..... -65°C to +150°C

Recommended Operating Conditions (3)

Supply voltage (V_{IN1}, V_{IN2}) .....3V to 16V
EN .....-0.3V to 4.8V
All other pins .....0.3V to 3.8V
Output voltage (V_{OUT}) .....-0.3V to 3.8V
Input and output voltage (LDO)..... 3.6V max
Output current (LDO) 500mA
Operating junction temp (T_J).... -40°C to +125°C

Thermal Resistance θ_{JA} θ_{JC}

QFN-26 (4mmx4mm)		
EVL5472 (4)	34	5.2 .. °C/W
JESD51-7 (5)	44	9 .... °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions. FB divider resistors are needed if V_{OUT} > 3.8V.
4) Measured on the EVL5472-Q-00A, a 4-layer PCB.
5) Measured on a JESD51-7, 4-layer PCB. The value of θ_{JA} given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_J = -40°C to +125°C, typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
VIN						
Input voltage (V_{IN}) under-voltage lockout (UVLO) rising threshold	V_{INUVLO_R}	Register 0x56, bits[1:0] configurable	2.6	2.75	2.9	V
V_{IN} UVLO hysteresis	V_{INUVLO_HYS}			150		mV
V_{IN} over-voltage (OV) rising threshold	V_{INOVLO_R}		16	18	20	V
VIN quiescent current	I_{Q_PFM}	PFM, no load		2.8	5	mA
Buck 1, Buck 2						
High-side (HS) switch on resistance	HSR_{ON}	For buck 1/2		15		mΩ
Low-side (LS) switch on resistance	LSR_{ON}	For buck 1/2		5		mΩ
Switch leakage	SW_{ILK1}	T_J = 25°C		0	1	μA
Minimum on time(6)	t_{ON_MIN1}			30		ns
Minimum off time(6)	t_{OFF_MIN1}			130		ns
Output voltage (V_{OUT}) accuracy	V_{FB1P}	All setting range, in FCCM	-1.5%	800	+1.5%	mV
V_{OUT} accuracy	V_{FB2P}	All setting range, in FCCM	-1.5%	800	+1.5%	mV
LS current limit (source)	I_{LS_VALLEY}	Registers 0x04, bits[4:2]; 0x09, bits[4:2] configurable		7.5		A
Negative current limit	I_{NOCP}	Forced PWM/OVP discharge	-6	-4.5	-3	A
Output discharge resistor	$R_{DISCHARGE}$			37		Ω
Under-Voltage (UV)/Over-Voltage (OV)						
Output UV threshold	V_{UVP_SW1}	Registers 0x05, bits[3:2]; 0x0A, bits[3:2] configurable	86%	90%	94%	V_{REF}
Output over-voltage protection (OVP) rising threshold	V_{OVP1_H}	Registers 0x05, bits[1:0]; 0x0A, bits[1:0] configurable	109%	113%	117%	V_{REF}
Output OVP recovery threshold	V_{OVP1_L}			110%		V_{REF}
Zero-current detection (ZCD)	I_{ZCD}	PFM mode		200		mA
Soft-Start Time						
Soft-start time	t_{START}	Registers 0x41, bits[6:4]; 0x48, bits[6:4] configurable	1.6	2	2.4	ms
Soft-stop time	t_{STOP}	Registers 0x41[3:2]; 0x48, bits[3:2] configurable		0.5		ms
Switching Frequency						
Default oscillation frequency	f_{SW}	Registers 0x02, bits[5:4]; 0x07 bit[5:4] configurable	800	1000	1200	kHz
Low-Dropout (LDO) Regulator						
LDOIN UVLO rising	V_{LDOIN_R}		2.4	2.6	2.8	V
LDOIN UVLO hysteresis	V_{LDOIN_HYS}			300		mV
Output voltage	V_{LDO}	Register 0x0C, configurable	-3%	1.8	+3%	V
LDO load capability	I_{LIM_LDO}		500			mA
LDO voltage regulation (6)	V_{LDO_RG}	LDOIN = 3.3V, LDO = 1.8V, load = 0mA to 500mA		1		%

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_J = -40°C to +125°C, typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Enable (EN)						
EN rising threshold	V_{EN_R}		1	1.2	1.4	V
EN falling threshold	V_{EN_F}		0.9	1	1.1	V
EN internal pull-down resistor			0.8	2	2.5	MΩ
MODE Detection						
MODE sourcing current	I_{MODE}		11.5	12.8	14.1	µA
MODE detection voltage upper threshold	V_{MODE_DT0}	MODE0 is detected if 0V < V_{MODE} < V_{MODE_DT0}			40	mV
	V_{MODE_DT1}	MODE1 is detected if V_{MODE_DT0} < V_{MODE} < V_{MODE_DT1}	80		120	mV
	V_{MODE_DT2}	MODE2 is detected if V_{MODE_DT1} < V_{MODE} < V_{MODE_DT2}	180		240	mV
	V_{MODE_DT3}	MODE3 is detected if V_{MODE_DT2} < V_{MODE} < V_{MODE_DT3}	320		460	mV
	V_{MODE_DT4}	MODE4 is detected if V_{MODE_DT3} < V_{MODE} < V_{MODE_DT4}	560		760	mV
	V_{MODE_DT5}	MODE5 is detected if V_{MODE_DT4} < V_{MODE} < V_{MODE_DT5}	860		1080	mV
	V_{MODE_DT6}	MODE6 is detected if V_{MODE_DT5} < V_{MODE} < V_{MODE_DT6}	1180		1400	mV
	V_{MODE_DT7}	MODE7 is detected if V_{MODE_DT6} < V_{MODE} < V_{CC}	1660			mV
Power Good (PG) and Interrupt (INT)						
PG output port sink current capability	V_{PG_SINK}	Sink 3mA			0.3	V
INT output port sink current capability	V_{INT_SINK}	Sink 3mA			0.3	V
PG UV rising	$V_{PG_UV_R}$	Registers 0x05, bit[5]; 0x0A, bit[5] configurable		95%		V_{REF}
PG UV falling	$V_{PG_UV_F}$			92.5%		V_{REF}
PG OV rising	$V_{PG_OV_R}$	Registers 0x05, bits[7:6]; 0x0A, bits[7:6] configurable		107.5%		V_{REF}
PG OV falling	$V_{PG_OV_F}$			105%		V_{REF}
VCC Regulator						
VCC voltage	V_{CC}	I_{CC} = 25mA	3.4	3.6	3.8	V
VCC voltage regulation	V_{CC_RG}	I_{CC} = 0mA to 25mA		1		%
Temperature Protection						
Thermal shutdown (7)	T_{OTP_R}	Register 0x0F, bits[7:5] configurable		155		°C
Thermal hysteresis (7)	T_{HYS}			20		°C
CLK						
CLK logic high	V_{CLK_IH}		1.4			V
CLK logic low	V_{CLK_IL}				0.4	V

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_J = -40°C to +125°C, typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
CLK output port sink current capability	V_{CLK_SINK}	Sink 3mA			0.3	V
General-Purpose Input/Output (GPIO)						
GPIO output port sink current capability	V_{GPIO_SINK}	Sink 3mA			0.3	V
I²C Interface Specifications (6)						
Input logic high	V_{IH}		1.4			V
Input logic low	V_{IL}				0.6	V
Output voltage logic low	V_{OUT_L}	Sink 4mA			0.4	V
SCL clock frequency	f_{SCL}				1	MHz
SCL high time	t_{HIGH}		60			ns
SCL low time	t_{LOW}		200			ns
Data set-up time	t_{SU_DAT}		10			ns
Data hold time	t_{HD_DAT}			70		ns
Set-up time for repeated start	t_{SU_STA}		160			ns
Hold time for repeated start	t_{HD_STA}		160			ns
Bus free time between a start and a stop command	t_{BUF}		160			ns
Set-up time for stop command	$t_{SU.STO}$		160			ns
SCL and SDA rising time	t_R		10		300	ns
SCL and SDA falling time	t_F		10		300	ns
Pulse width of suppressed spike	t_{SP}		0		50	ns
Capacitance bus for each bus line	C_B				400	pF

Notes:

6) Guarantee by engineering sample characterization.
7) Guaranteed by design.

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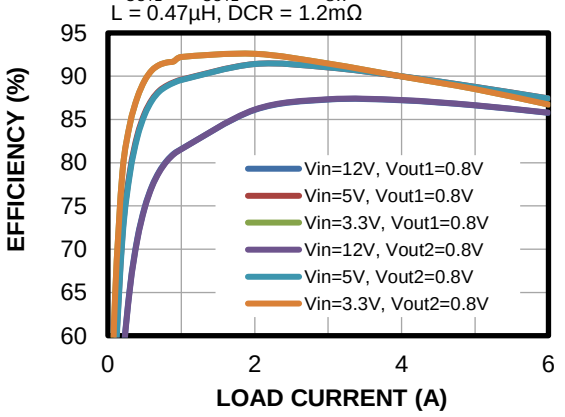
TYPICAL CHARACTERISTICS

V_{IN} = 12V, V_{OUT1} = V_{OUT2} = 0.8V, T_A = 25°C, unless otherwise noted.

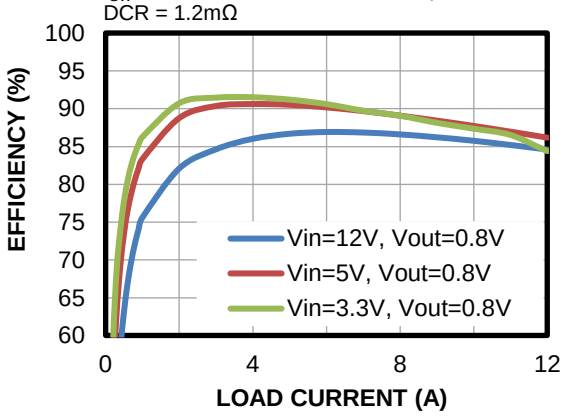
Efficiency vs. Load Current

Single-phase, dual-output,
V_{OUT1} = V_{OUT2} = 0.8V, f_{SW} = 750kHz with FCCM,
L = 0.47µH, DCR = 1.2mΩ



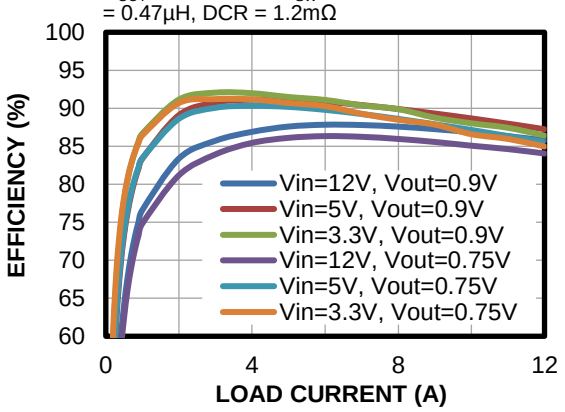
Efficiency vs. Load Current

Dual-phase, single-output, V_{OUT} = 0.8V,
f_{SW} = 750kHz with FCCM, L = 0.47µH,
DCR = 1.2mΩ

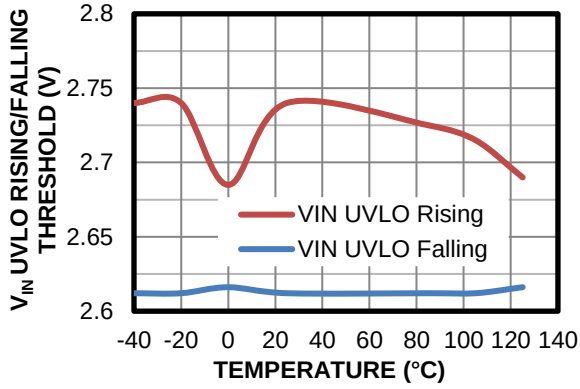


Efficiency vs. Load Current

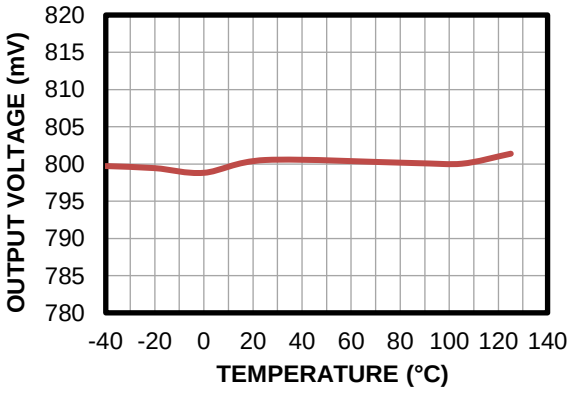
Dual-phase, single-output,
V_{OUT} = 0.75V/0.9V, f_{SW} = 750kHz with FCCM, L = 0.47µH, DCR = 1.2mΩ



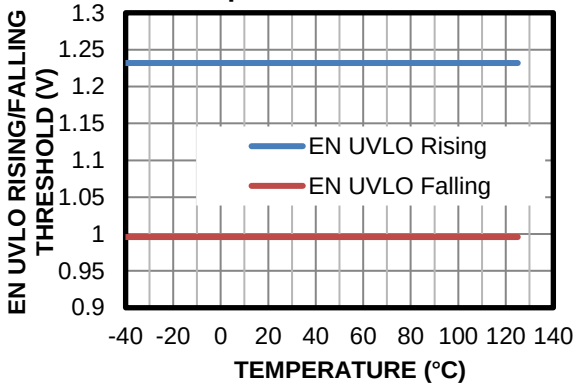
V_{IN} UVLO Rising/Falling vs. Temperature



Output Voltage vs. Temperature



EN UVLO Rising/Falling Threshold vs. Temperature



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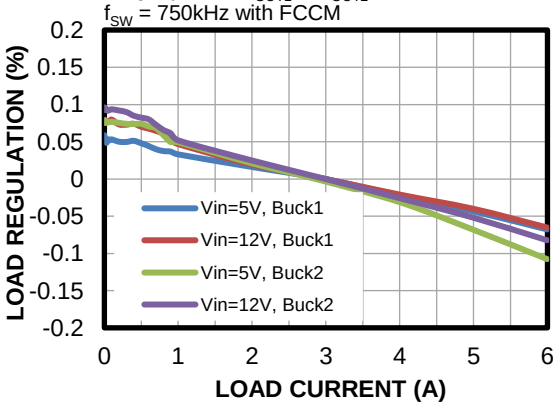
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT1} = V_{OUT2} = 0.8V, T_A = 25°C, unless otherwise noted.

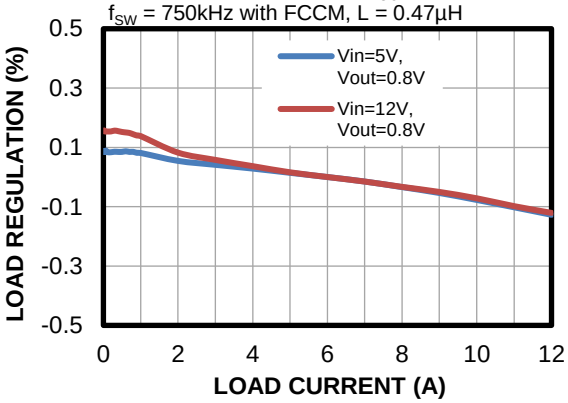
Load Regulation vs. Load Current

Single-phase, V_{OUT1} = V_{OUT2} = 0.8V, f_{SW} = 750kHz with FCCM



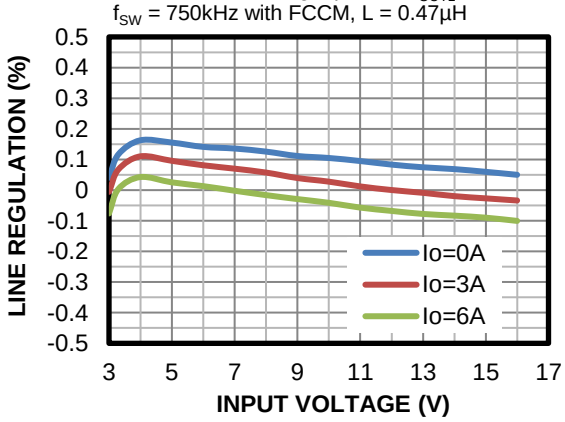
Load Regulation vs. Load Current

Dual-phase, single-output, V_{OUT} = 0.8V, f_{SW} = 750kHz with FCCM, L = 0.47µH



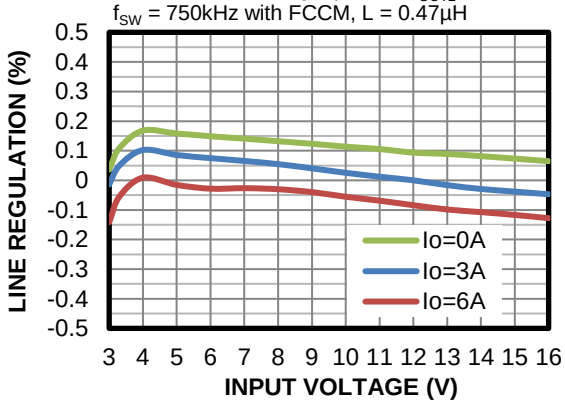
Line Regulation vs. Input Voltage

Buck 1 channel, single-phase, V_{OUT1} = 0.8V, f_{SW} = 750kHz with FCCM, L = 0.47µH



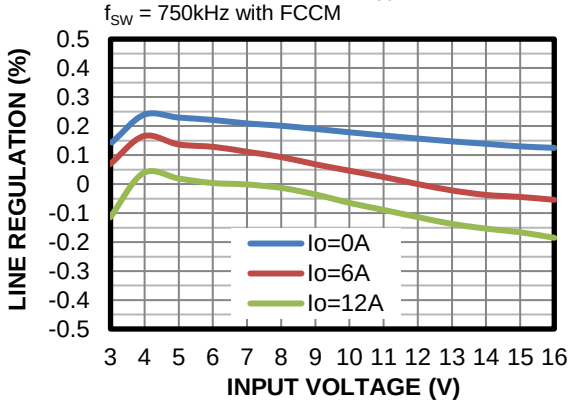
Line Regulation vs. Input Voltage

Buck 2 channel, single-phase, V_{OUT2} = 0.8V, f_{SW} = 750kHz with FCCM, L = 0.47µH



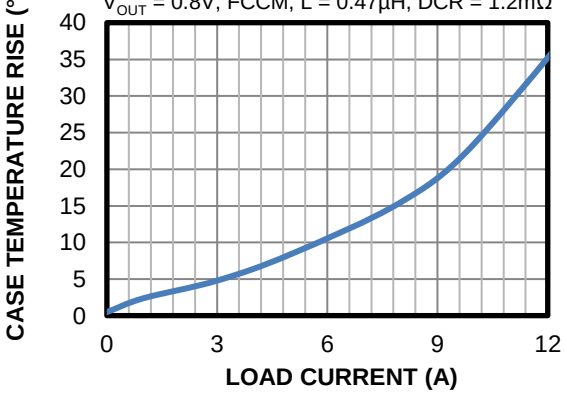
Line Regulation vs. Input Voltage

Dual-phase, single-output, V_{OUT} = 0.8V, f_{SW} = 750kHz with FCCM



Case Temperature Rise vs. Load Current

V_{IN} = 5V, dual-phase, single-output, V_{OUT} = 0.8V, FCCM, L = 0.47µH, DCR = 1.2mΩ



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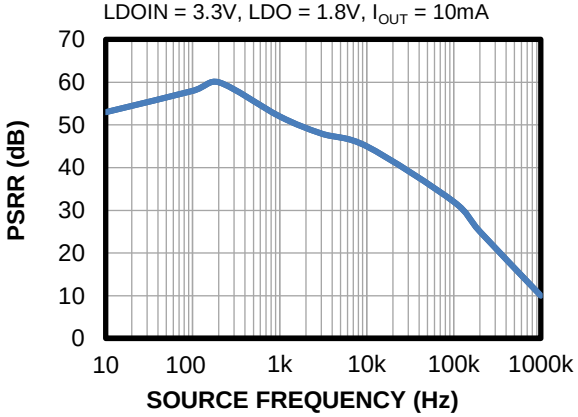
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT1} = V_{OUT2} = 0.8V, T_A = 25°C, unless otherwise noted.

PSRR vs. Source Frequency

LDOIN = 3.3V, LDO = 1.8V, I_{OUT} = 10mA



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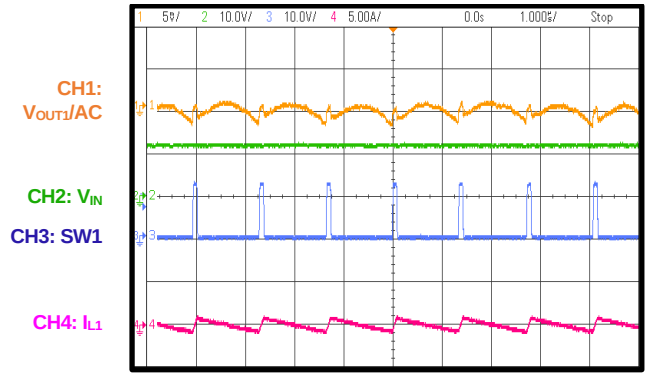
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT1} = V_{OUT2} = 0.8V, T_A = 25°C, unless otherwise noted.

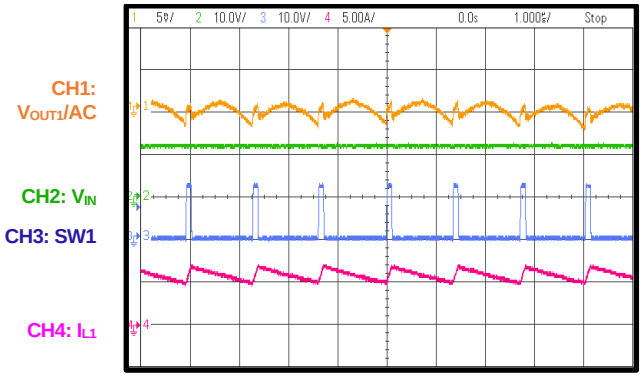
Steady State

Single-phase, V_{OUT1} = 0.8V, f_{SW} = 750kHz with FFCM, I_{OUTA} = 0A



Steady State

Single-phase, V_{OUT1} = 0.8V, f_{SW} = 750kHz with FCCM, I_{OUTA} = 6A



Steady State

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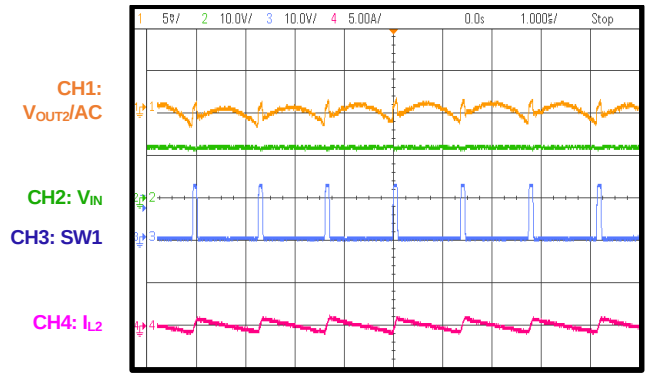
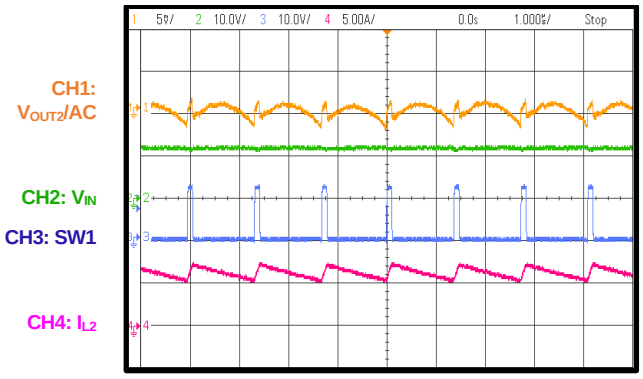


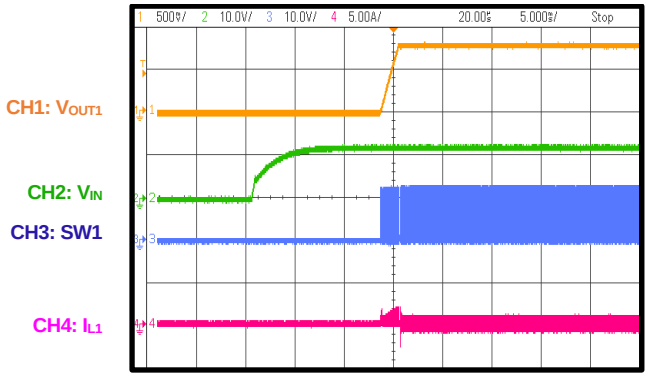
Steady State

Single-phase, V_{OUT2} = 0.8V, f_{SW} = 750kHz with FCCM, I_{OUTA} = 6A



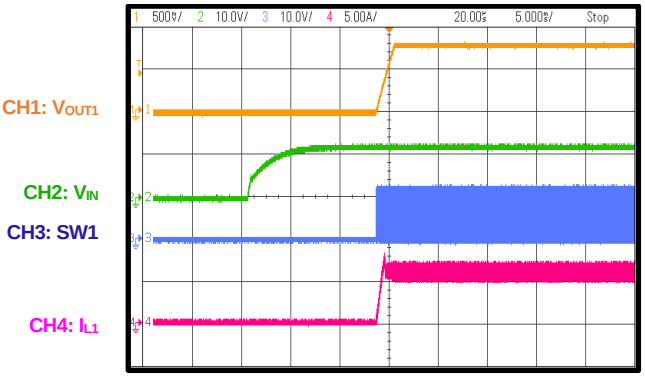
Power Start-Up

Single-phase, V_{OUT1} = 0.8V, I_{OUT1} = 0A



Power Start-Up

Single-phase, V_{OUT1} = 0.8V, I_{OUT1} = 6A



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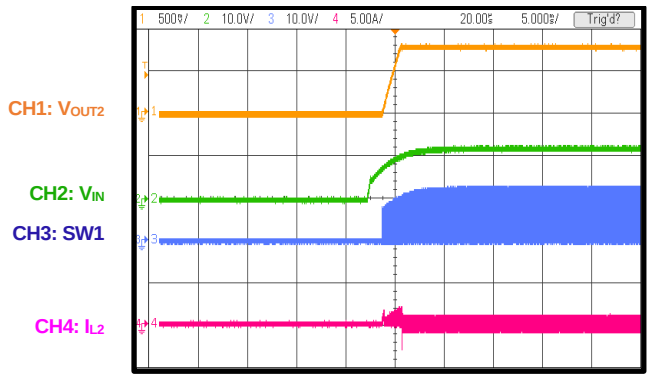
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT1} = V_{OUT2} = 0.8V, T_A = 25°C, unless otherwise noted.

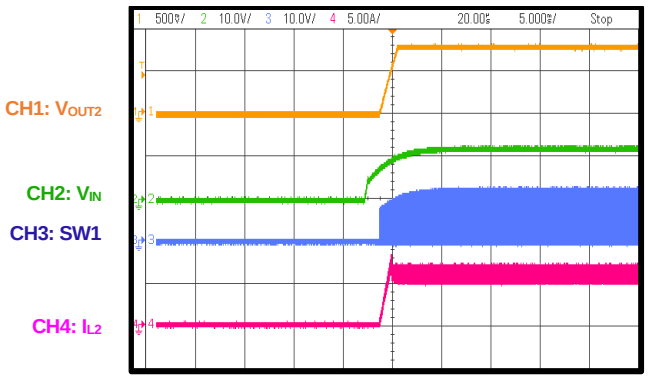
Power Start-Up

Single-phase, V_{OUT2} = 0.8V, I_{OUT1} = 0A



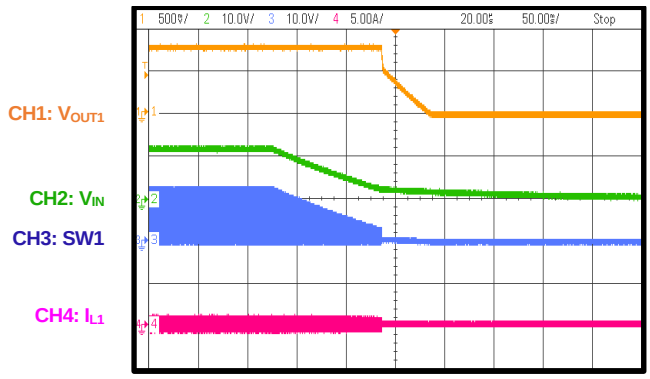
Power Start-Up

Single-phase, V_{OUT2} = 0.8V, I_{OUT1} = 6A



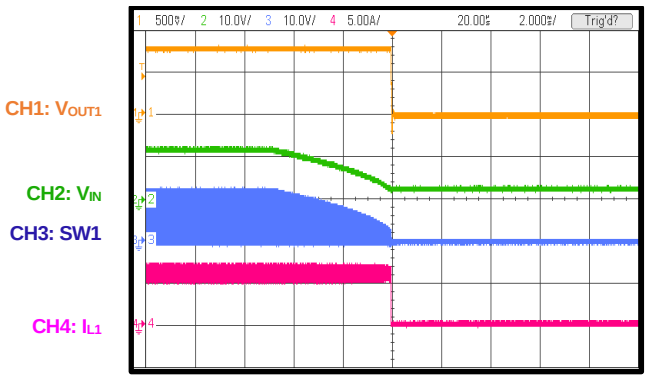
Power Shutdown

Single-phase, V_{OUT1} = 0.8V, I_{OUT1} = 0A



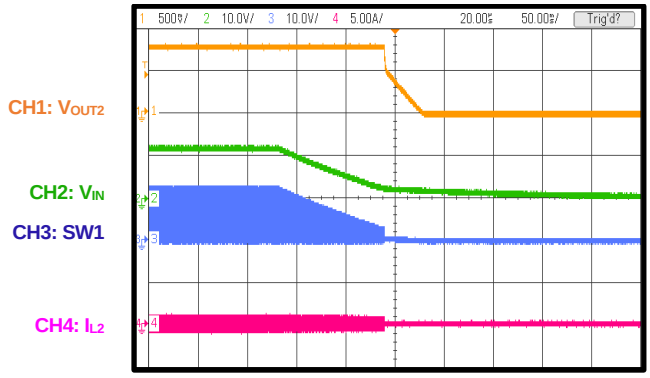
Power Shutdown

Single-phase, V_{OUT1} = 0.8V, I_{OUT1} = 6A



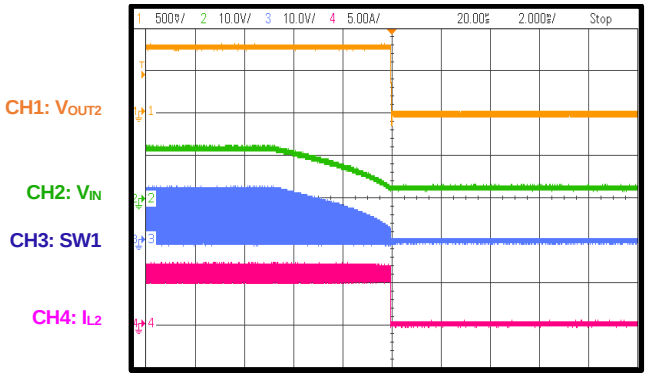
Power Shutdown

Single-phase, V_{OUT2} = 0.8V, I_{OUT1} = 0A



Power Shutdown

Single-phase, V_{OUT2} = 0.8V, I_{OUT1} = 6A



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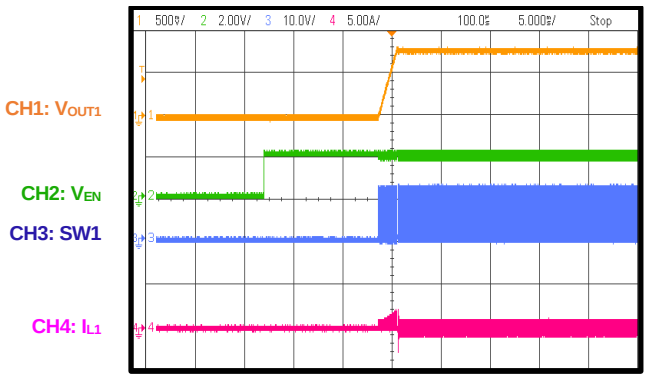
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT1} = V_{OUT2} = 0.8V, T_A = 25°C, unless otherwise noted.

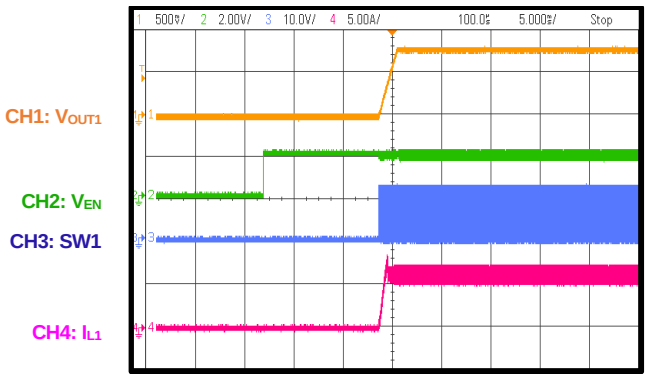
EN Start-Up

Single-phase, V_{OUT1} = 0.8V, I_{OUT1} = 0A



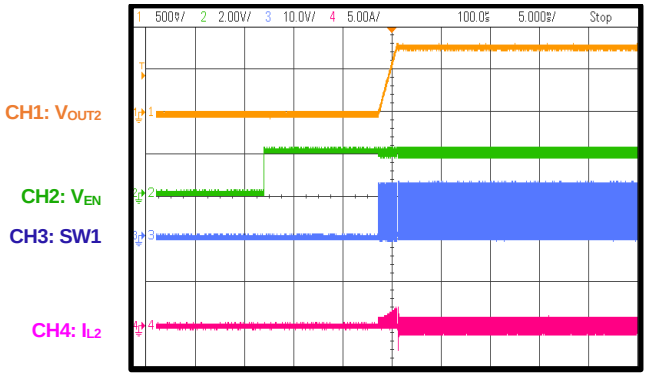
EN Start-Up

Single-phase, V_{OUT1} = 0.8V, I_{OUT1} = 6A



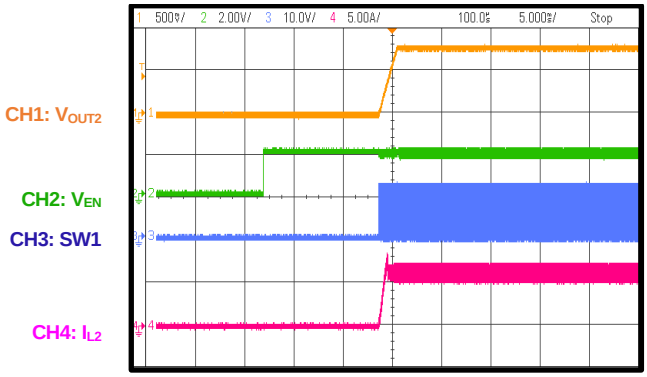
EN Start-Up

Single-phase, V_{OUT2} = 0.8V, I_{OUT1} = 0A



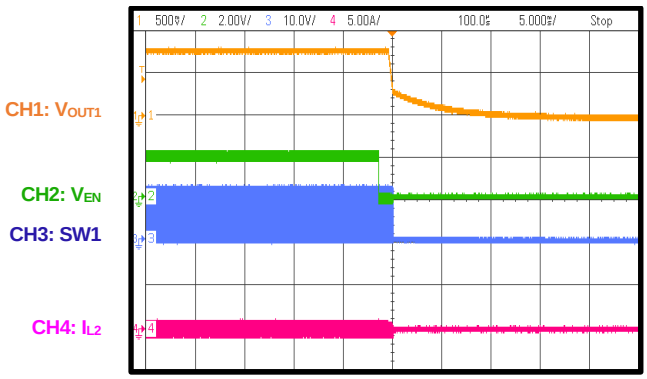
EN Start-Up

Single-phase, V_{OUT2} = 0.8V, I_{OUT1} = 6A



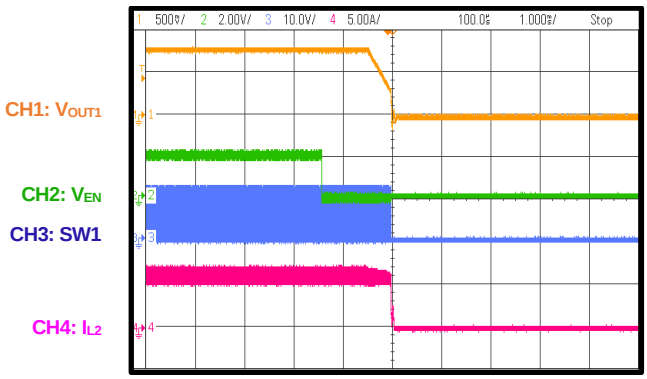
EN Shutdown

Single-phase, V_{OUT1} = 0.8V, I_{OUT1} = 0A



EN Shutdown

Single-phase, V_{OUT1} = 0.8V, I_{OUT1} = 6A



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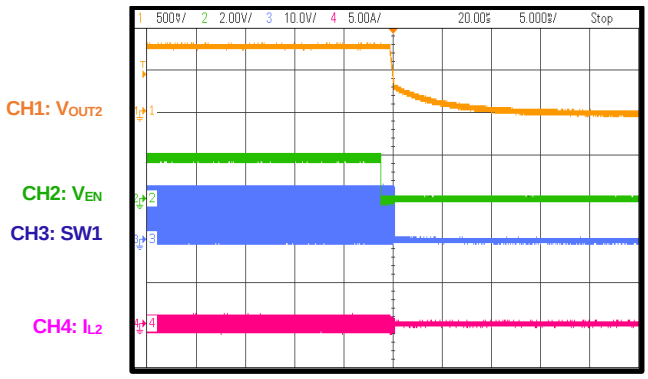
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT1} = V_{OUT2} = 0.8V, T_A = 25°C, unless otherwise noted.

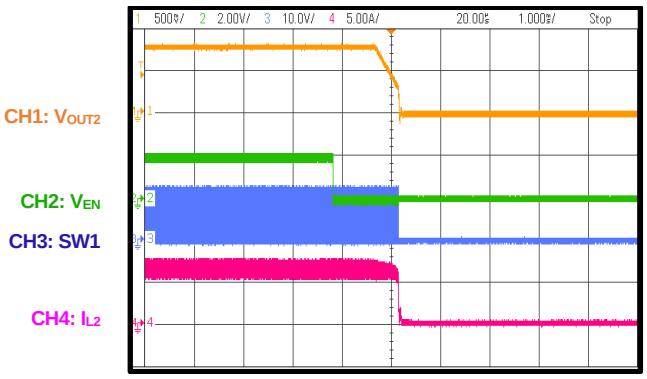
EN Shutdown

Single-phase, V_{OUT2} = 0.8V, I_{OUT1} = 0A



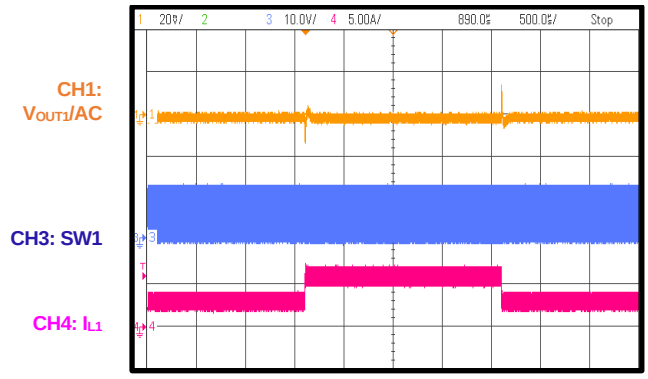
EN Shutdown

Single-phase, V_{OUT2} = 0.8V, I_{OUT1} = 6A



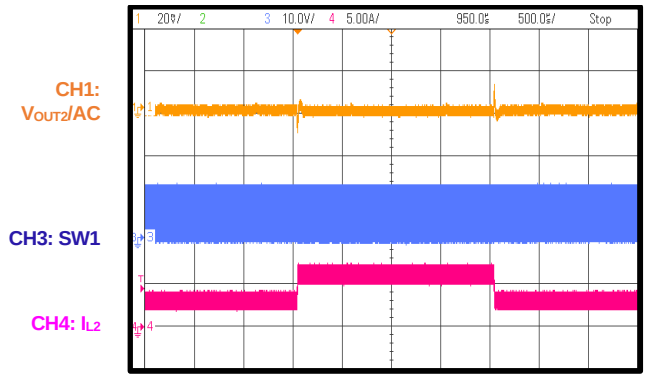
Load Transient

Single-phase, V_{OUT1} = 0.8V, I_{OUT} = 3 to 6A, slew rate = 1A/µs



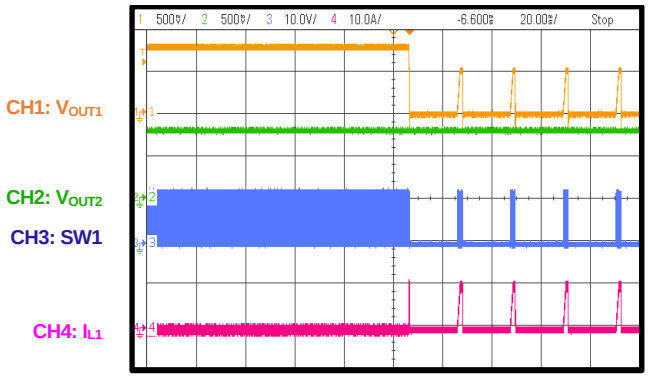
Load Transient

Single-phase, V_{OUT2} = 0.8V, I_{OUT} = 3 to 6A, slew rate = 1A/µs



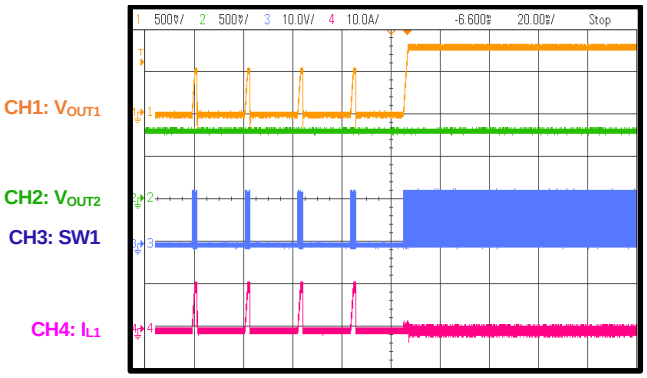
SCP Entry

Single-phase, V_{OUT1} = V_{OUT2} = 0.8V, V_{OUT1} short to GND



SCP Recovery

Single-phase, V_{OUT1} = V_{OUT2} = 0.8V, V_{OUT1} short to GND



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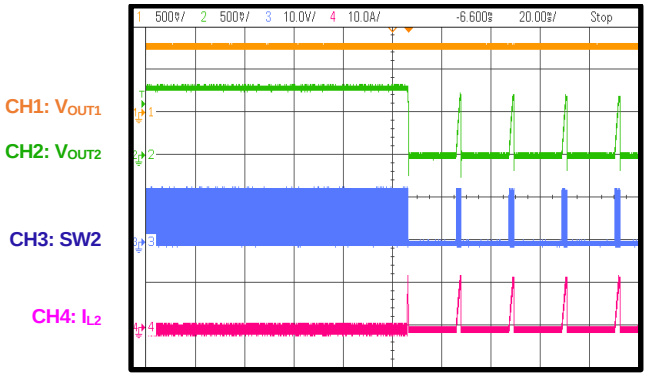
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT1} = V_{OUT2} = 0.8V, T_A = 25°C, unless otherwise noted.

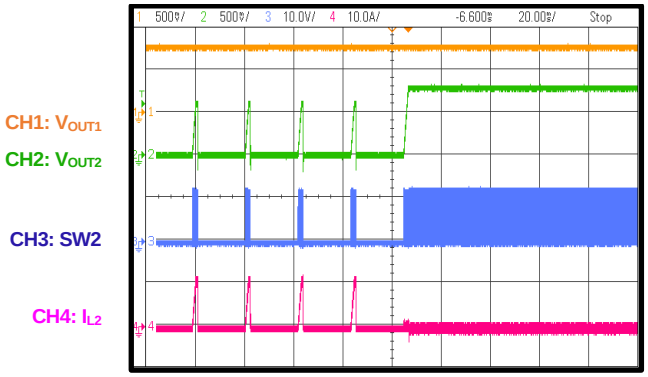
SCP Entry

Single-phase, V_{OUT1} = V_{OUT2} = 0.8V, V_{OUT2} short to GND



SCP Recovery

Single-phase, V_{OUT1} = V_{OUT2} = 0.8V, V_{OUT2} short to GND



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FUNCTIONAL BLOCK DIAGRAM

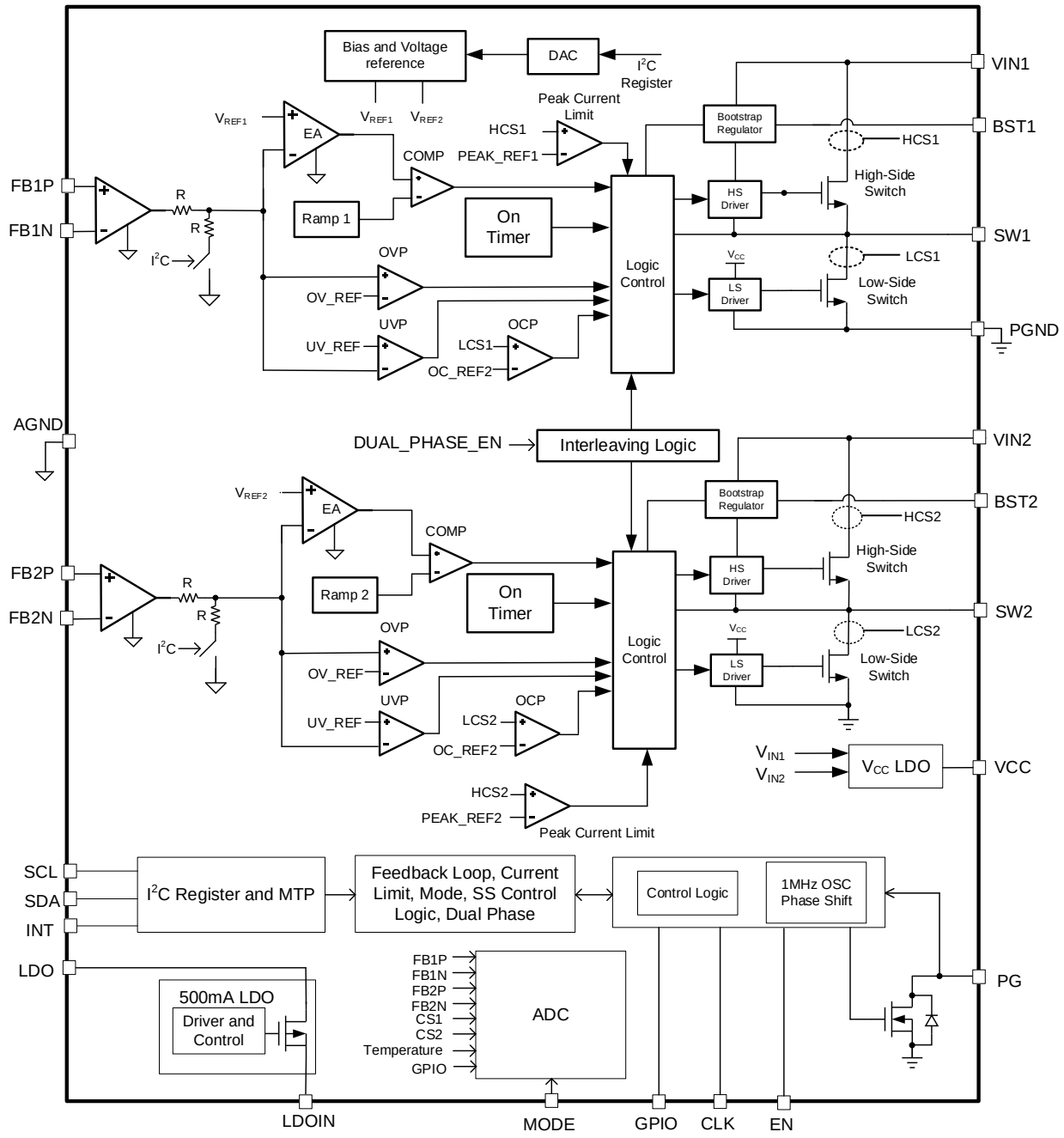

Figure 4: Functional Block Diagram

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OPERATION

High-Efficiency Buck Regulators

The MP5472 is dual-channel power module. Buck converter 1 (buck 1) and buck converter 2 (buck 2) are synchronous, step-down DC/DC converters with built-in soft start, compensation, and hiccup current-limit protection. Fixed-frequency constant-on-time (COT) control provides fast transient response.

VIN Power Supply

VIN1 is the power supply for buck 1, while VIN2 is the power supply for buck 2. It is recommended to connect VIN1 to VIN2 during application. When the input voltage (V_{INx}, where x = 1 or 2) exceeds the V_{INx} under-voltage lockout (UVLO) rising threshold, the corresponding buck starts up if all the other start-up conditions are met (V_{IN} and EN exceed their UVLO thresholds, and the power rails are enabled in the registers). The respective buck shuts down when V_{INx} falls below the V_{INx} UVLO falling threshold voltage.

Over-Temperature (OT) Warning and Thermal Shutdown

The MP5472 employs over-temperature (OT) warning and critical temperature shutdown. The MP5472 monitors the IC's junction temperature (T_J). If T_J exceeds the OT warning threshold set via register 0x0F, bits D[4:2], the MP5472 sets the warning status in register 0x19, bit D[1]. The MP5472 continues to operate as normal.

If the MPQ5472's temperature exceeds the thermal shutdown threshold set via register 0x0F, bits D[7:5], the MP5472 internally generates a disable command and disables buck 1, buck 2, and the 500mA low-dropout (LDO) regulator. In addition, the OT status in register 0x19, bit D[0] is set, and the PG output signal de-asserts at the same time.

Soft Start and Soft Shutdown

The MP5472 employs a soft-start and soft-shutdown mechanism to ensure that there is a smooth output during start-up and shutdown. When the part is enabled and the BST voltage reaches its rising threshold, the internal digital-to-analog converter (DAC) outputs a reference voltage (V_{REF}). The output voltage (V_{OUTx}, where x = 1 or 2) smoothly ramps up with the reference voltage. When the DAC output reaches the final voltage, it stops at that level. At this point, soft start is finished and the device enters steady-state operation.

When the part is disabled, the internal DAC output ramps down. V_{OUTx} smoothly ramps down with the reference voltage. When the DAC output reaches 300mV (if BUCK1_FB_HALF = 1 or BUCK2_FB_HALF = 1, the corresponding DAC output reaches 150mV), it stops at that level. At this point, soft shutdown is finished and the output gradually discharges to 0V via the FB1P- and FB2P-to-GND resistance.

The soft-start time and soft-shutdown time can be configured via registers 0x41 and 0x48.

Working Mode Selection

The MP5472 works with a fixed frequency under heavy-load conditions. When the load current decreases, the MP5472 can work in forced pulse-width modulation (PWM) mode and automatic pulse-frequency modulation (PFM)/PWM mode based on the frequency register setting.

Forced Pulse-Width Modulation (PWM) Operation

When the MP5472 works in forced PWM mode, the MP5472 enters continuous conduction mode (CCM), during which the high-side MOSFET (HS-FET) and low-side MOSFET (LS-FET) repeat on/off operation, even if the inductor current is zero or at a negative value. The switching frequency (f_{SW}) is fairly constant. Figure 5 shows the timing diagram during this operation.

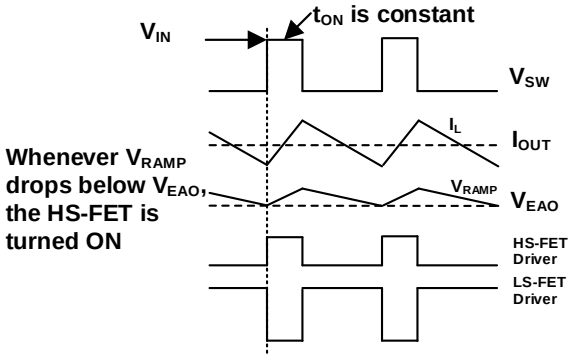

Figure 5: Forced PWM Operation

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Light-Load Operation

When the MP5472 works in auto PWM or auto PFM mode during light-load operation, the MP5472 reduces f_{SW} automatically to maintain high efficiency, and the inductor current drops almost to zero. The HS-FET turns on when V_{RAMP} is below V_{EAO}. The HS-FET turns off when the on-timer elapses and the inductor current exceeds its given threshold. When the inductor current reaches zero, the LS-FET driver goes into tri-state (Hi-Z) (see Figure 6). The output capacitors discharge slowly to GND through the LS-FET and the resistors (R1 and R2). This operation greatly improves device efficiency when the output current (I_{OUT}) is low.

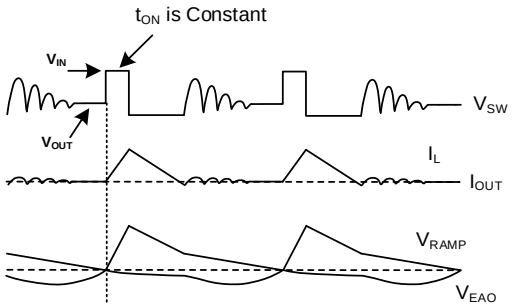

Figure 6: Light-Load Operation

VCC Regulator

A 3.6V internal regulator powers most of the internal circuitries. A 1µF decoupling capacitor is required to stabilize the regulator and reduce ripple. This regulator takes the VIN input and operates across the full V_{IN} range. After EN is pulled high and V_{IN} exceeds 3.6V, the output of the regulator is in full regulation. When V_{IN} is below 3.6V, the output voltage decreases and follows the input voltage. A 1µF ceramic capacitor is required for decoupling.

Over-Voltage Protection (OVP)

An output over-voltage protection (OVP) mechanism is implemented to limit the voltages on the MP5472's output regulators. The MP5472 actively monitors the output voltage (V_{OUTx}, where x = 1 or 2) on each enabled regulator.

The potential OV events for the MP5472 are listed below:

- Buck 1's output exceeds the threshold set via register 0x05, bits D[1:0].
- Buck 2's output exceeds the threshold set via register 0x0A, bits D[1:0].

The fault rail's output enters OVP discharge mode once the output voltage exceeds the set regulation voltage for longer than 2.5µs. In OVP discharge mode, the LS-FET turns on and stays on until its current drops to the negative current limit. This process discharges the output and keeps the output voltage within the normal range. If the OV condition still exists, the LS-FET turns on again after a fixed delay to repeat the discharge behavior. The device exits discharge mode when the feedback voltage (V_{FB}) drops to the reference voltage threshold.

Floating Driver and Bootstrap Charging

An external bootstrap capacitor powers the floating power MOSFET driver. This floating driver has its own UVLO protection with a rising threshold of 2.28V and a 250mV hysteresis. The bootstrap capacitor voltage is regulated by VIN internally through D1, M1, C4, L1, and C2 (see Figure 7). If V_{BST} - V_{SW} exceeds 3.5V, U1 regulates M1 to maintain a 3.5V BST voltage across C4.

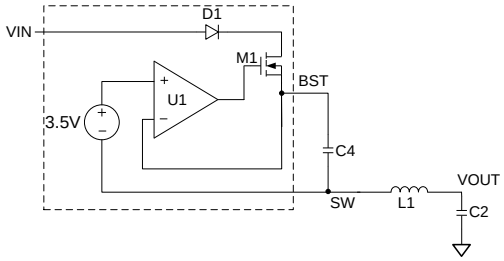

Figure 7: Internal BST Charging Circuit

Over-Current Protection (OCP) and Short-Circuit Protection (SCP)

The MP5472 has valley current limit control. When the LS-FET is on, the inductor current is monitored.

The potential over-current (OC) events for the MP5472 are listed below:

- Buck 1's inductor current exceeds the valley current limit threshold set via register 0x04, bits D[4:2].
- Buck 2's inductor current exceeds the valley current limit threshold set via register 0x09, bits D[4:2].

When the sensed inductor current exceeds the valley current limit threshold, the device enters over-current protection (OCP) mode. The HS-FET cannot turn on until the inductor current

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drops to the valley current limit. Meanwhile, the output voltage drops until it falls below the under-voltage (UV) threshold, which is typically 45% of the reference voltage.

Once UV and OC are both triggered, the MP5472 enters hiccup mode to periodically restart the related power rail. The hiccup duty cycle is very small to reduce power dissipation during short-circuit (SC) conditions. During OCP, the device tries to recover from the OC fault with hiccup mode. During this period, the chip disables the output power stage, discharges the soft-start capacitor, and then automatically tries to soft start again. If the OC condition still exists when soft start is finished, the device repeats this operation. OCP is a non-latch protection.

Active Voltage Position (AVP)

The MP5472 supports active voltage positioning (AVP) by setting the AVP_EN bit to 1 via the I²C. An internal current-sense circuit produces the droop current's (I_{DROOP}) current source, which is proportional to the internal sensing current. I_{DROOP} injects to the FB pin to produce the feedback voltage with a droop voltage. The actual output voltage (V_{OUT_AVP}) can be calculated with Equation (1):

$$V_{OUT_AVP}=V_{OUT}+AVPx_OFFSET - AVPx_GAIN\times I_{OUT}\times FB_FACTOR \quad (1)$$

Where V_{OUT} is the output voltage when the AVP function is disabled, and FB_FACTOR is a constant that is determined by BUCKx_FB_HALF in registers 0x44 and 0x4B (see Table 1). AVPx_GAIN and AVPx_OFFSET can be set via the I²C registers 0x1F and 0x20, respectively. These values can also be pre-configured to the MTP via registers 0x5C and 0x5D.

Table 1: FB_Factor Selection (8)

BUCKx_FB_HALF	FB_Factor
0	1
1	2

Note:

8) BUCKx_FB_HALF can be configured via the 0x44 and 0x4B MTP registers, bit[5]; as well as bits[7:6] of the following MODE registers: 0x72, 0x7D, 0x88, 0x93, 0x9E, 0xA9, 0xB4, 0xBF.

Power Good (PG) Signal

The PG pin indicates the statuses of V_{INx} and all enabled output regulators (VOUT1, VOUT2, and LDO). The MP5472 floats the PG pin (it is high) when V_{INx} is valid and all enabled output regulator's (VOUT1, VOUT2, LDO) tolerances are maintained, as configured via the appropriate registers.

When the output voltages of the power rails (V_{OUTx} and the LDO) are within the power good tolerance threshold, the internal power good bit (PGx) asserts (high). If the output voltages of the power rail (V_{OUTx} or LDO) are out of the power good tolerance thresholds, the internal power good bit (PGx) de-asserts (low).

The power good statuses of all the enabled power rails are used to determine whether the PG pin is high following "and" logic. If all the enabled rails have a high PG status, the PG pin is high. If one or more enabled rails have low PG status, or all the power rails are disabled, the PG pin is low.

PG also acts an input signal to stop the clock number. After PG pulls up and exceeds 2.3V, the master stops to generate the clock after the clock number count is complete.

Interleaving for Dual-Phase Operation

When interleaving mode is enabled (by setting register 0x54, bit D[7] = 1), buck 1 and buck 2 enter 2-phase interleaving operation, which is also known as dual-phase mode. The SET signal is triggered by comparing V_{FB} and the internal V_{REF}. When the SET signal goes high, only one phase's PWM output goes high; the next time the SET signal goes high, the next phase's PWM output goes high. This process accomplishes interleaving.

When buck 1 and buck 2 operate in dual-phase interleaving mode, it senses both phase currents and auto-tunes the buck's on time (t_{ON}) to balance the current. Figure 8 shows dual-phase, single-output operation.

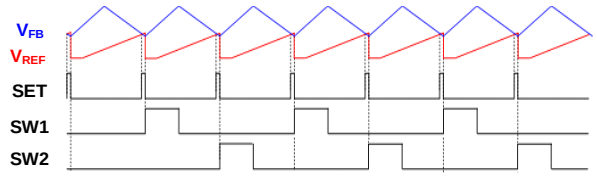

Figure 8: Bucks 1/2 Interleaving for Dual-Phase Operation

Analog-to-Digital Converter (ADC)

The MP5472 supports an ADC to monitor the input supply voltages, output voltages (for buck 1, buck 2, the LDO, and GPIO), and output

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voltage regulator current (for buck 1 and buck 2). Register 0x10, bit D[7] enables the ADC. Registers 0x12, 0x13, 0x14, 0x15, 0x16, 0x17, and 0x18 provide the actual measurements for V_{OUT1}, I_{OUT1}, V_{OUT2}, I_{OUT2}, LDO, GPIO, and V_{IN}, respectively.

MODE Pin Determined MTP Configuration

Some MTP configurations are determined by the resistor connected to the MODE pin. A 2% (or higher) accuracy is required for the MODE resistor to guarantee correct MODE configurations. Table 2 shows the configuration selections.

Table 2: Recommended MODE Determined MTP Configuration Map Selection

MODE Resistor	MODE Determined MTP Configuration
GND	MODE0, 0x70~0x7A
6.2kΩ	MODE1, 0x7B~0x85
13kΩ	MODE2, 0x86~0x90
27kΩ	MODE3, 0x91~0x9B
51kΩ	MODE4, 0x9C~0xA6
75kΩ	MODE5, 0xA7~0xB1
100kΩ	MODE6, 0xB2~0xBC
No connect or VCC	MODE7, 0xBD~0xC7

After start-up, if MODE_EN = 1, the MP5472 detects the MODE pin's resistor configuration, and selects the corresponding MODEx. Next, the MODEx MTP configurations are loaded into the corresponding MTP registers then the I²C registers (see Figure 9).

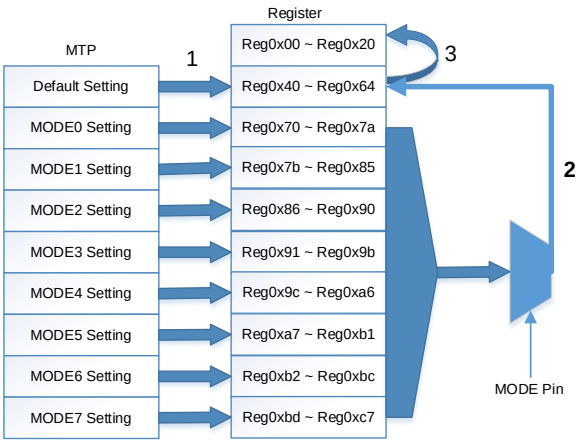

Figure 9: Mode Operation when MODE_EN = 1

The process is described in greater detail below:

Step 1: Copy the MTP data to the corresponding registers.

Step 2: Select one MODE according to the MODE pin voltage, and copy the MODE region registers' values to the MTP region registers (0x40~0x64).

Step 3: Copy the 0x40~0x64 values to corresponding I²C region register (0x00~0x20).

If MODE_EN = 0, the registers keep their original values, which are loaded into the I²C region registers (see Figure 10).

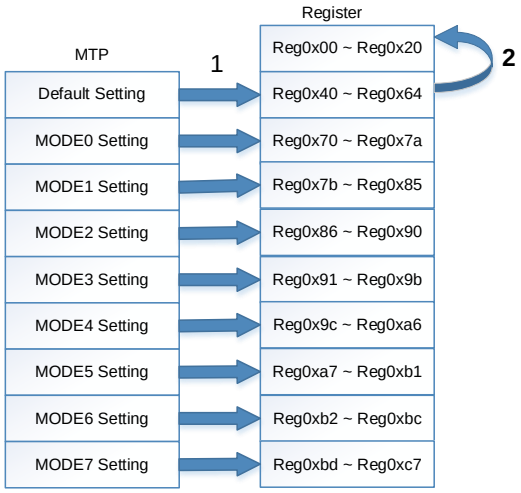

Figure 10: Mode Operation with MODE_EN = 0

The process is described in greater detail below:

Step 1: Copy the default setting in the MTP to the MTP region registers (0x40~0x64).

Step 2: Copy the MTP region registers' values to the corresponding I²C region registers.

Remote Voltage Sense

Remote voltage sense can be used to avoid the influence of cable voltage drop between the output cable and the load to accurately stabilize the load voltage. Connect the FBxP/FBxN pin to the output capacitor, and ensure that they are placed close to the load. Layout the FBxP/FBxN as a differential line.

Interrupt (INT)

The INT pin indicates the MP5472's status. INT is specified as an open-drain signal. Interrupts have an active low, latched signal. If any status bit in registers 0x19 or 0x1A is changed to 1, the INT pin outputs low.

The INT pin stays low until both of the following requirements are met:

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- The condition causing the interrupt no longer exists.
- The register is cleared through the I²C write-to-clear bit.

A status bit is latched to 1 if its related condition occurs. This bit stays latched to 1 until the clear bit is written to 1. If a status bit is cleared but the condition continues to persist, a new interrupt is generated (as if it is a new condition).

When the mask register bit is set to 1 (masked), the INT pin does not pull low, even though the corresponding status bit is triggered and set to 1.

FLEX-Timer Sequence Control

CLK-Based Power Sequence Control

This CLK based FLEX-Timer Sequence Control scheme uses “Master-Slave” structure.

The EN pins and CLK pins for all the PMICs are connected together for sequence control (see Figure 11). The CLK pins should be pulled up to any one of the VCCs via a resistor (typical 10kΩ).

One PMIC is configured as the master converter, which generates a clock signal output on the CLK pin (denoted as PMIC1 in Figure 11). The other converters are configured as the slave converters, which receive the clock signal input on the CLK pin. The start-up/shutdown sequence of all the power rails are synchronized by the clock signal.

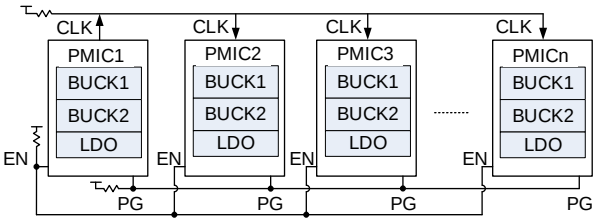

Figure 11: FLEX-Timer Sequence Control Connection

When the EN pin pulls high, the start-up sequence starts. The master PMIC starts generating the clock outputs, and the slave converters count the clock signal. For the relevant power rail in one master/slave converter, when the counted clock signal cycle reaches POWER_ON_DELAY (an internal non-volatile memory (NVM) register), the power rail turns on. When the master PMIC clock cycle reaches CLK_NUMBER (an NVM register in the master PMIC) and PG goes high (all enabled power rails finish their soft-start process and the PG pin is pulled high by an external resistor), the master converter stops the clock output, and the start-up sequence finishes. The master PMIC does not stop the clock outputs if the PG pin is floating or pulled down.

When the EN pin pulls low, the master converter’s CLK pin sends a set of 250kHz pulses (14 pulses) to inform the slaves that the shutdown sequence of all converters must begin.

The master converter starts generating the clock outputs. The slave converters count the clock signal. For the relevant power rail in one master/slave converter, when the counted clock signal cycle reaches POWER_OFF_DELAY (an internal NVM register), the power rail turns off. When the master converter clock cycle reaches CLK_NUMBER, the master converter stops the clock output, and the shutdown sequence finishes.

When there is only one MP5472, the CLK pin should be pulled high and CLK_MODE should be set to master converter.

Clock Pausing Function

For each master/slave PMIC, during the start-up/shutdown sequence, the following can occur:

- If CLK_PAUSE_EN = 1, the master/slave converter pulls the CLK pin down during the soft start/shutdown of any power rail(s). Figure 12 shows when CLK pauses during soft start. Figure 13 shows when CLK pauses during soft shutdown.

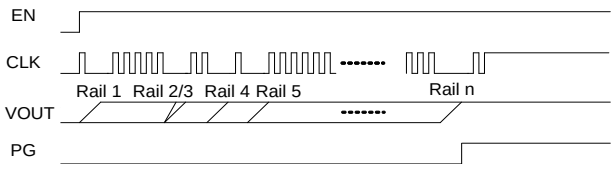

Figure 12: Soft Start when CLK Pulls Down (Pausing)

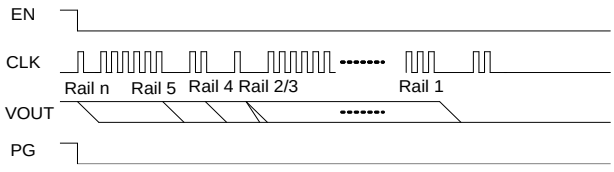

Figure 13: Soft Shutdown when CLK Pulls Down (Pausing)

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- If CLK_PAUSE_EN = 0, the master/slave converter does not pull the CLK pin down during the soft start/shutdown of any power rails. Figure 14 shows soft start when CLK does not pull down. Figure 15 shows soft shutdown when CLK does not pull down.

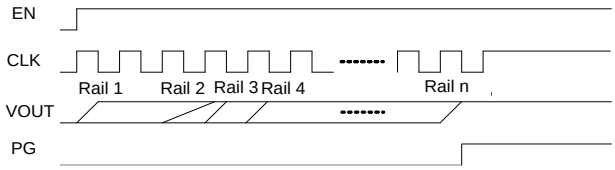

Figure 14: Soft Start when CLK Does Not Pull Down (Not Pausing)

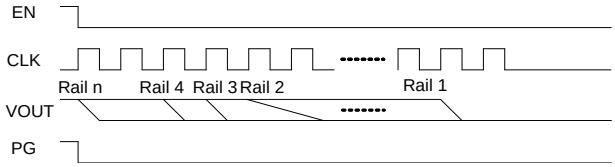

Figure 15: Soft Shutdown when CLK Does Not Pull Down (Not Pausing)

- If CLK_ON_ERROR_PAUSE_EN = 1, the master/slave PMIC pulls the CLK pin down if any error occurs during any power rail's soft start (see Figure 16).

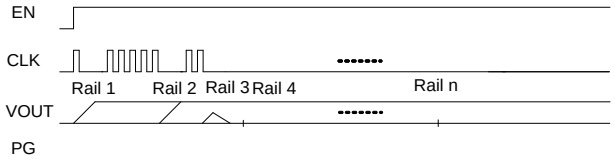

Figure 16: Soft Start during PMIC Error when CLK Pulls Down (CLK Pausing)

- If CLK_ON_ERROR_PAUSE_EN = 0, the master/slave PMIC does not pull the CLK pin down, even if any error occurs during the soft start of any power rails (see Figure 17). The function does not work when the buck converter protection mode is set to latch-off mode.

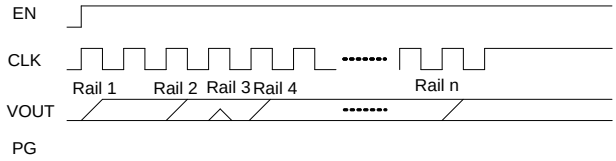

Figure 17: Soft Start during PMIC Error when CLK Does Not Pull Down (No CLK Pausing

For the clock pausing function, the master PMIC generates the clock signal and monitors the CLK pin's status. When the master PMIC generates a high clock (open-drain output) on the CLK pin but the CLK pin stays low, the CLK pin must be pulled low by one or more master/slave PMIC. The master PMIC pauses the clock signal output; it resumes the clock signal output once the CLK pin is released or detected high. If the CLK pin is not pulled low for clock pausing, the master PMIC should maintain the clock signal output until the start-up/shutdown sequence finishes.

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I²C INTERFACE

I²C Serial Interface Description

The I²C is a 2-wire, bidirectional, serial interface consisting of a data line (SDA) and a clock line (SCL). The lines are pulled to a bus voltage externally when they are idle. When connecting to the line, a master device generates the SCL signal and device address and arranges the communication sequence. The MP5472 interface is an I²C slave. The I²C interface adds flexibility to the power supply solution. The output voltage, transition slew rate, and other parameters can be controlled by the I²C interface instantaneously.

Data Validity

One clock pulse is generated for each data bit transferred. The data on the SDA line must be stable during the clock's high period. The high or low state of the data line can only change when the clock signal on the SCL line is low (see Figure 18).

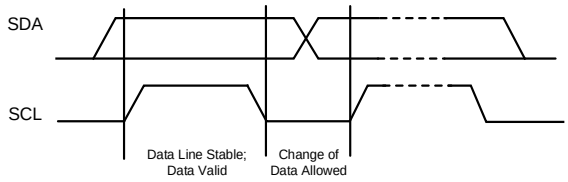

Figure 18: Bit Transfer on the I²C Bus

The start (S) and stop (P) commands are signaled by the master device, which signifies the beginning and the end of the I²C transfer. The start command is defined as the SDA signal transitioning from high to low while SCL is high. The stop command is defined as the SDA signal transitioning from low to high while SCL is high (see Figure 19).

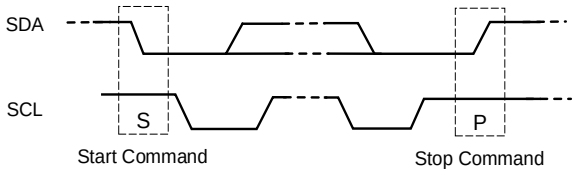

Figure 19: Start and Stop Commands

Start and stop commands are always generated by the master. The bus is busy after the start condition, and it is considered to be free again a minimum of 4.7µs after the stop command.

The bus remains busy if a repeated start (Sr) is generated instead of a stop command. The start and repeated start conditions are functionally identical.

Data Transfer

Every byte put on the SDA line must be 8 bits long. Each byte must be followed by an acknowledge (ACK) bit. The acknowledge-related clock pulse is generated by the master. The transmitter releases the SDA line (high) during the acknowledge clock pulse. The receiver must pull down the SDA line during the acknowledge clock pulse so that it remains stable low during the clock pulse's high period.

Figure 20 shows the data transfer format. After the start command, a slave address is sent. This address is 7 bits, followed by an 8th data direction bit (R/W). A 0 indicates a transmission (write), and a 1 indicates a request for data (read). A data transfer is always terminated by a stop command, which is generated by the master. If the master still wants to communicate on the bus, it can generate a repeated start command and address another slave without first generating a stop command.

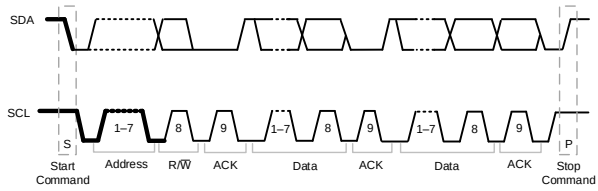

Figure 20: Complete Data Transfer

The MP5472 requires a start condition, a valid I²C address, a register address byte, and a data byte for a single data update. After receiving each byte, the MPQ5472 acknowledges by pulling the SDA line low during the high period of a single clock pulse. A valid I²C address selects the MP5472. The MP5472 performs an update on the falling edge of the least significant bit (LSB) byte.

Figure 21 on page 26 shows an I²C write example. Figure 22 on page 26 shows an I²C read example.

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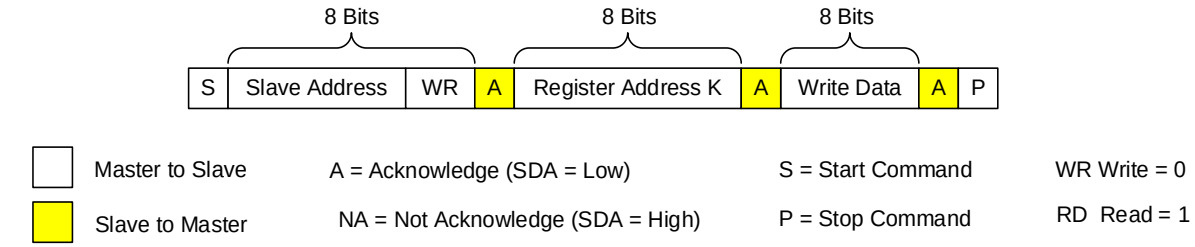

Figure 21: I²C Write Single Register Example

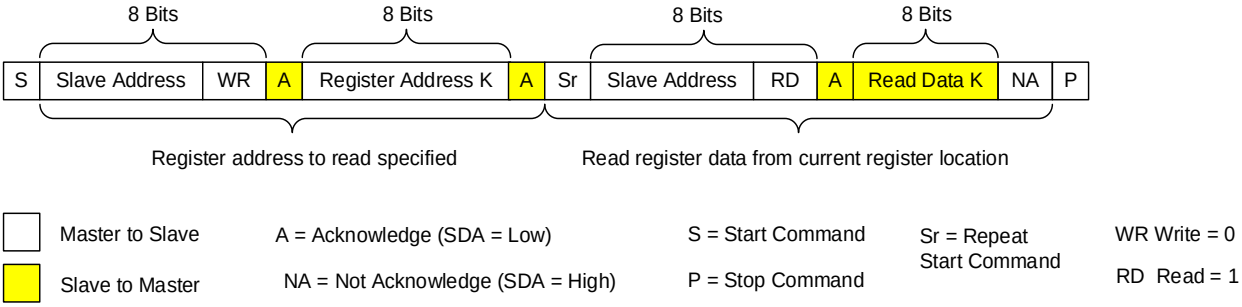

Figure 22: I²C Read Single Register Example

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REGISTER ATTRIBUTE DEFINITION

All volatile registers have base attributes (see Table 3).

Table 3: Register Base Attributes

Attribute	Abbreviation	Description
Read-Only	RO	This bit can be read by the host. Writes have no effect.
Read/Write	R/W	This bit can be read or written by the host.
Write-Only	W	This bit can only be written by the host. Reading from this bit returns 0.
Reserved	RV	This bit is reserved for future expansion and its value must not be modified by the host. The bit returns 0 when read. Writing to this bit has no effect.

Some register attributes can be further modified with attribute modifiers (see Table 4).

Table 4: Register Attribute Modifier

Attribute	Abbreviation	Description
Write 1 Only	1O	This bit can only be set (i.e. write 1) but not reset (i.e. write 0). Writing 0 to this bit has no effect.
Protected	P	This bit is protected by the password registers. This bit cannot be written to unless the password code has been written into the password register(s).
Persistent	E	This bit is persistent during the power cycle.

Table 5 goes into more detail on the register map regions.

Table 5: Register Map Breakdown

Register Range	Region	Description
0x00~0x3F	I²C Region	Volatile memory registers.
0x40~0x6F	MTP Region	NVM. These registers require a complete power cycle before they take effect. Changing these registers under normal operation is considered an illegal operation.
0x70~0xCF	MODE Region	NVM. These registers configure the default value for some registers in the MTP region.

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I²C REGISTER MAP DESCRIPTION (9) (10) (11) (12)

Add. (0X)	Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0
00	LOCK	R/W	RV							I2C_LOCK_EN
01	BUCK1_CTRL1	R/W	VOUT1_GO_BIT	RV					VOUT1_SLEW_RATE	
02	BUCK1_CTRL2	R/W	BUCK1_PWM/PFM		BUCK1_FSW		RV	VOUT1_SETTING_LOW		
03	BUCK1_CTRL3	R/W	VOUT1_SETTING_HIGH							
04	BUCK1_CTRL4	R/W	VOUT1_DISCHRG_EN	VOUT1_OVP_EN	RV	BUCK1_OC_TH			RV	
05	BUCK1_CTRL7	R/W	VOUT1_PG_VTH_HIGH		VOUT1_PG_VTH_LOW	RV	VOUT1_UV_VTH		VOUT1_OV_VTH	
06	BUCK2_CTRL1	R/W	VOUT2_GO_BIT	RV					VOUT2_SLEW_RATE	
07	BUCK2_CTRL2	R/W	BUCK2_PWM/PFM		BUCK2_FSW		RV	VOUT2_SETTING_LOW		
08	BUCK2_CTRL3	R/W	VOUT2_SETTING_HIGH							
09	BUCK2_CTRL4	R/W	VOUT2_DISCHRG_EN	VOUT2_OVP_EN	RV	BUCK2_OC_TH			RV	
0A	BUCK2_CTRL7	R/W	VOUT2_PG_VTH_HIGH		VOUT2_PG_VTH_LOW	RV	VOUT2_UV_VTH		VOUT2_OV_VTH	
0B	LDO_CTRL1	R/W	LDO_GO_BIT	RV			RV		LDO_DISCHRG	LDO_PG_VTH
0C	LDO_CTRL2	R/W	RV	LDO_SETTING						
0D	SYS_CTRL1	R/W	PMIC_EN	VOUT1_EN	VOUT2_EN	LDO_EN	RV		GPIO_CTRL	
0E	SYS_CTRL3	R/W	VIN_PG_VTH			MASK_PG	RV			
0F	SYS_CTRL4	R/W	OT_TH			OTW_TH			RV	
10	ADC_CTRL1	R/W	ADC_EN	RV					ADC_SAMPLE_FREQ	
11	TEMPERATURE	RO	TEMPERATURE			RV				
12	VOUT1_ADC	RO	VOUT1_ADC							
13	IOUT1_ADC	RO	IOUT1_ADC							
14	VOUT2_ADC	RO	VOUT2_ADC							
15	IOUT2_ADC	RO	IOUT2_ADC							
16	LDO_ADC	RO	LDO_ADC							
17	GPIO_ADC	RO	GPIO_ADC							
18	VIN_ADC	RO	VIN_ADC							
19	STATUS1	RO	VIN_PG	VOUT1_PG	VOUT2_PG	LDO_PG	RV		OTW	OT

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I²C REGISTER MAP DESCRIPTION *(continued)* (9) (10) (11) (12)

Add. (0X)	Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0
1A	STATUS2	RO	VIN_OV	VIN_UV	VOUT1_OV	VOUT2_OV	VOUT1_UV	VOUT2_UV	VOUT1_OC	VOUT2_OC
1B	MASK1	R/W	VIN_PG_MSK	VOUT1_PG_MSK	VOUT2_PG_MSK	LDO_PG_MSK	RV		OTW_MSK	OT_MSK
1C	MASK2	R/W	VIN_OV_MSK	VIN_UV_MSK	VOUT1_OV_MSK	VOUT2_OV_MSK	VOUT1_UV_MSK	VOUT2_UV_MSK	VOUT1_OC_MSK	VOUT2_OC_MSK
1D	CLEAR1	W1C	VIN_PG_CLEAR	VOUT1_PG_CLEAR	VOUT2_PG_CLEAR	LDO_PG_CLEAR	OTW_CLEAR	OT_CLEAR	RV	ALL_STATUS_CLEAR
1E	CLEAR2	W1C	VIN_OV_CLEAR	VIN_UV_CLEAR	VOUT1_OV_CLEAR	VOUT2_OV_CLEAR	VOUT1_UV_CLEAR	VOUT2_UV_CLEAR	VOUT1_OC_CLEAR	VOUT2_OC_CLEAR
1F	AVP_CTRL1	R/W	AVP1_EN	AVP1_GAIN		AVP1_OFFSET				
20	AVP_CTRL2	R/W	AVP2_EN	AVP2_GAIN		AVP2_OFFSET				

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MTP REGION REGISTER MAP (9) (10) (11) (12)

Add. (0X)	Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0
40	LOCK	R/W/P/E	MTP_REGION_ACCESS_PASSWORD							
41	BUCK1_CTRL1	R/W/P/E	RV	VOUT1_SOFT_START			VOUT1_SOFT_STOP		VOUT1_SLEW_RATE	
42	BUCK1_CTRL2	R/W/P/E	BUCK1_PWM/PFM		BUCK1_FSW		RV	VOUT1_SETTING_LOW		
43	BUCK1_CTRL3	R/W/P/E	VOUT1_SETTING_HIGH							
44	BUCK1_CTRL4	R/W/P/E	VOUT1_DISCHRG_EN	VOUT1_OVP_EN	BUCK1_FB_HALF	BUCK1_OC_TH			RV	
45	BUCK1_CTRL5	R/W/P/E	BUCK1_POWER_ON_DELAY							
46	BUCK1_CTRL6	R/W/P/E	BUCK1_POWER_OFF_DELAY							
47	BUCK1_CTRL7	R/W/P/E	VOUT1_PG_VTH_HIGH		VOUT1_PG_VTH_LOW	RV	VOUT1_UV_VTH		VOUT1_OV_VTH	
48	BUCK2_CTRL1	R/W/P/E	RV	VOUT2_SOFT_START			VOUT2_SOFT_STOP		VOUT2_SLEW_RATE	
49	BUCK2_CTRL2	R/W/P/E	BUCK2_PWM/PFM		BUCK2_FSW		RV	VOUT2_SETTING_LOW		
4A	BUCK2_CTRL3	R/W/P/E	VOUT2_SETTING_HIGH							
4B	BUCK2_CTRL4	R/W/P/E	VOUT2_DISCHRG_EN	VOUT2_OVP_EN	BUCK2_FB_HALF	BUCK2_OC_TH			RV	
4C	BUCK2_CTRL5	R/W/P/E	BUCK2_POWER_ON_DELAY							
4D	BUCK2_CTRL6	R/W/P/E	BUCK2_POWER_OFF_DELAY							
4E	BUCK2_CTRL7	R/W/P/E	VOUT2_PG_VTH_HIGH		VOUT2_PG_VTH_LOW	RV	VOUT2_UV_VTH		VOUT2_OV_VTH	
4F	LDO_CTRL1	R/W/P/E	RV	LDO_SOFT_START			RV		LDO_DISCHRG	LDO_PG_VTH
50	LDO_CTRL2	R/W/P/E	RV	LDO_SETTING						
51	LDO_CTRL3	R/W/P/E	LDO_POWER_ON_DELAY							
52	LDO_CTRL4	R/W/P/E	LDO_POWER_OFF_DELAY							
53	SYS_CTRL1	R/W/P/E	PMIC_EN	VOUT1_EN	VOUT2_EN	LDO_EN	RV		GPIO_CTRL	
54	SYS_CTRL2	R/W/P/E	SINGLE/DUAL	REV_CODE						
55	SYS_CTRL3	R/W/P/E	VIN_PG_VTH			MASK_PG	PG_DELAY_EN	VIN_OVP_EN	RV	HICCUP
56	SYS_CTRL4	R/W/P/E	OT_TH			OTW_TH			VIN_UV_SEL	
57	GPIO_CONFIG1	R/W/P/E	GPIO_POWER_ON_DELAY							
58	GPIO_CONFIG2	R/W/P/E	GPIO_POWER_OFF_DELAY							
59	ADC_CTRL2	R/W/P/E	ADC_EN	RV					ADC_SAMPLE_FREQ	
5A	MASK1	R/W/P/E	VIN_PG_MSK	VOUT1_PG_MSK	VOUT2_PG_MSK	LDO_PG_MSK	RV		OTW_MSK	OT_MSK

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MTP REGION REGISTER MAP *(continued)* (9) (10) (11) (12)

Add. (0X)	Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0
5B	MASK2	R/W/ P/E	VIN_OV_ MSK	VIN_ UV_MSK	VOUT1_ OV_MSK	VOUT2_ OV_MSK	VOUT1_ UV_MSK	VOUT2_ UV_MSK	VOUT1_ OC_MSK	VOUT2_ OC_MSK
5C	AVP_CT RL1	R/W/ P/E	AVP1_ EN	AVP1_GAIN		AVP1_OFFSET				
5D	AVP_CT RL2	R/W/ P/E	AVP2_ EN	AVP2_GAIN		AVP2_OFFSET				
5E	CLK_CT RL1	R/W/ P/E	CLK_ MODE	CLK_FREQUENCY			CLK_NUMBER			RV
5F	CLK_CT RL2	R/W/ P/E	RV					CLK_ PAUSE_EN	CLK_ON_ ERROR_ PAUSE_ EN	RV
60	I2C_CO NFIG	R/W/ P/E	MODE_ EN	I2C_ADDRESS						
61	MTP_CT RL1	R/W/ P/E	MTP_PASSWORD							
62	MTP_CT RL2	R/W/ P/E	RV						MTP_ RESTORE	MTP_ PROGRAM
63	RV	R/W/ P/E	RV							
64	ID2	R/W/ P/E	MTP_CODE							

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MODE REGION REGISTER MAP (9) (10) (11) (12)

Add. (0X)	R/W	D7	D6	D5	D4	D3	D2	D1	D0
70	R/W/ PE	MODE0_VOUT1_SETTING_HIGH							
71	R/W/ PE	MODE0_VOUT2_SETTING_HIGH							
72	R/W/ PE	MODE0_ BUCK1_FB_ HALF	MODE0_ BUCK2_FB_ HALF	MODE0_VOUT1_SETTING_LOW			MODE0_VOUT2_SETTING_LOW		
73	R/W/ PE	MODE0_CLK_ MODE	MODE0_ SINGLE/DUAL	RV		MODE0_BUCK1_ FSW		MODE0_BUCK2_FSW	
74	R/W/ PE	MODE0_BUCK1_POWER_ON_DELAY							
75	R/W/ PE	MODE0_BUCK2_POWER_ON_DELAY							
76	R/W/ PE	MODE0_VOUT1_SOFT_START_TIME			MODE0_VOUT2_SOFT_ START_TIME			MODE0_ LDO_EN	RV
77	R/W/ PE	MODE0_LDO_SOFT_START_TIME			MODE0_I2C_ADDRESS			MODE0_GPIO_CTRL	
78	R/W/ PE	MODE0_LDO_SETTING							
79	R/W/ PE	MODE0_LDO_POWER_ON_DELAY							
7A	R/W/ PE	MODE0_GPIO_POWER_ON_DELAY							
7B	R/W/ PE	MODE1_VOUT1_SETTING_HIGH							
7C	R/W/ PE	MODE1_VOUT2_SETTING_HIGH							
7D	R/W/ PE	MODE1_ BUCK1_FB_ HALF	MODE1_ BUCK2_FB_ HALF	MODE1_VOUT1_SETTING_LOW			MODE1_VOUT2_SETTING_LOW		
7E	R/W/ PE	MODE1_CLK_ MODE	MODE1_ SINGLE/DUAL	RV		MODE1_BUCK1_ FSW		MODE1_BUCK2_FSW	
7F	R/W/ PE	MODE1_BUCK1_POWER_ON_DELAY							
80	R/W/ PE	MODE1_BUCK2_POWER_ON_DELAY							
81	R/W/ PE	MODE1_VOUT1_SOFT_START_TIME			MODE1_VOUT2_SOFT_ START_TIME			MODE1_ LDO_EN	RV
82	R/W/ PE	MODE1_LDO_SOFT_START_TIME			MODE1_I2C_ADDRESS			MODE1_GPIO_CTRL	
83	R/W/ PE	MODE1_LDO_SETTING							
84	R/W/ PE	MODE1_LDO_POWER_ON_DELAY							
85	R/W/ PE	MODE1_GPIO_POWER_ON_DELAY							
86	R/W/ PE	MODE2_VOUT1_SETTING_HIGH							
87	R/W/ PE	MODE1_VOUT2_SETTING_HIGH							
88	R/W/ PE	MODE2_BUCK 1_FB_HALF	MODE2_BUCK 1_FB_HALF	MODE2_BUCK1_FB_HALF			MODE2_BUCK1_FB_HALF		
89	R/W/ PE	MODE2_CLK_ MODE	MODE2_CLK_ MODE	MODE2_CLK_MODE		MODE2_CLK_ MODE		MODE2_CLK_MODE	
8A	R/W/ PE	MODE2_BUCK1_POWER_ON_DELAY							
8B	R/W/ PE	MODE2_BUCK2_POWER_ON_DELAY							

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MODE REGION REGISTER MAP *(continued)* (9) (10) (11) (12)

Add. (0X)	R/W	D7	D6	D5	D4	D3	D2	D1	D0
8C	R/W/ PE	MODE2_VOUT1_SOFT_START_TIME			MODE2_VOUT2_SOFT_ START_TIME			MODE2_ LDO_EN	RV
8D	R/W/ PE	MODE2_LDO_SOFT_START_TIME			MODE2_I2C_ADDRESS			MODE2_GPIO_CTRL	
8E	R/W/ PE	MODE2_LDO_SETTING							
8F	R/W/ PE	MODE2_LDO_POWER_ON_DELAY							
90	R/W/ PE	MODE2_GPIO_POWER_ON_DELAY							
91	R/W/ PE	MODE3_VOUT1_SETTING_HIGH							
92	R/W/ PE	MODE3_VOUT2_SETTING_HIGH							
93	R/W/ PE	MODE3_ BUCK1_FB_ HALF	MODE3_ BUCK2_FB_ HALF	MODE3_VOUT1_SETTING_LOW			MODE3_VOUT2_SETTING_LOW		
94	R/W/ PE	MODE3_CLK_ MODE	MODE3_ SINGLE/DUAL	RV		MODE3_BUCK1_ FSW		MODE3_BUCK2_FSW	
95	R/W/ PE	MODE3_BUCK1_POWER_ON_DELAY							
96	R/W/ PE	MODE3_BUCK2_POWER_ON_DELAY							
97	R/W/ PE	MODE3_VOUT1_SOFT_START_TIME			MODE3_VOUT2_SOFT_ START_TIME			MODE3_ LDO_EN	RV
98	R/W/ PE	MODE3_LDO_SOFT_START_TIME			MODE3_I2C_ADDRESS			MODE3_GPIO_CTRL	
99	R/W/ PE	MODE3_LDO_SETTING							
9A	R/W/ PE	MODE3_LDO_POWER_ON_DELAY							
9B	R/W/ PE	MODE3_GPIO_POWER_ON_DELAY							
9C	R/W/ PE	MODE4_VOUT1_SETTING_HIGH							
9D	R/W/ PE	MODE4_VOUT2_SETTING_HIGH							
9E	R/W/ PE	MODE4_BUCK 1_FB_HALF	MODE4_BUCK 1_FB_HALF	MODE4_BUCK1_FB_HALF			MODE4_BUCK1_FB_HALF		
9F	R/W/ PE	MODE4_CLK_ MODE	MODE4_CLK_ MODE	MODE4_CLK_MODE		MODE4_CLK_ MODE		MODE4_CLK_MODE	
A0	R/W/ PE	MODE4_BUCK1_POWER_ON_DELAY							
A1	R/W/ PE	MODE4_BUCK2_POWER_ON_DELAY							
A2	R/W/ PE	MODE4_VOUT1_SOFT_START_TIME			MODE4_VOUT2_SOFT_ START_TIME			MODE4_ LDO_EN	RV
A3	R/W/ PE	MODE4_LDO_SOFT_START_TIME			MODE4_I2C_ADDRESS			MODE4_GPIO_CTRL	
A4	R/W/ PE	MODE4_LDO_SETTING							
A5	R/W/ PE	MODE4_LDO_POWER_ON_DELAY							
A6	R/W/ PE	MODE4_GPIO_POWER_ON_DELAY							
A7	R/W/ PE	MODE5_VOUT1_SETTING_HIGH							
A8	R/W/ PE	MODE5_VOUT2_SETTING_HIGH							

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MODE REGION REGISTER MAP *(continued)* (9) (10) (11) (12)

Add. (0X)	R/W	D7	D6	D5	D4	D3	D2	D1	D0
A9	R/W/PE	MODE5_BUCK1_FB_HALF	MODE5_BUCK2_FB_HALF	MODE5_VOUT1_SETTING_LOW			MODE5_VOUT2_SETTING_LOW		
AA	R/W/PE	MODE5_CLK_MODE	MODE5_SINGLE/DUAL	RV		MODE5_BUCK1_FSW		MODE5_BUCK2_FSW	
AB	R/W/PE	MODE5_BUCK1_POWER_ON_DELAY							
AC	R/W/PE	MODE5_BUCK2_POWER_ON_DELAY							
AD	R/W/PE	MODE5_VOUT1_SOFT_START_TIME			MODE5_VOUT2_SOFT_START_TIME			MODE5_LDO_EN	RV
AE	R/W/PE	MODE5_LDO_SOFT_START_TIME			MODE5_I2C_ADDRESS			MODE5_GPIO_CTRL	
AF	R/W/PE	MODE5_LDO_SETTING							
B0	R/W/PE	MODE5_LDO_POWER_ON_DELAY							
B1	R/W/PE	MODE5_GPIO_POWER_ON_DELAY							
B2	R/W/PE	MODE6_VOUT1_SETTING_HIGH							
B3	R/W/PE	MODE6_VOUT2_SETTING_HIGH							
B4	R/W/PE	MODE6_BUCK1_FB_HALF	MODE6_BUCK2_FB_HALF	MODE6_VOUT1_SETTING_LOW			MODE6_VOUT2_SETTING_LOW		
B5	R/W/PE	MODE6_CLK_MODE	MODE6_SINGLE/DUAL	RV		MODE6_BUCK1_FSW		MODE6_BUCK2_FSW	
B6	R/W/PE	MODE6_BUCK1_POWER_ON_DELAY							
B7	R/W/PE	MODE6_BUCK2_POWER_ON_DELAY							
B8	R/W/PE	MODE6_VOUT1_SOFT_START_TIME			MODE6_VOUT2_SOFT_START_TIME			MODE6_LDO_EN	RV
B9	R/W/PE	MODE6_LDO_SOFT_START_TIME			MODE6_I2C_ADDRESS			MODE6_GPIO_CTRL	
BA	R/W/PE	MODE6_LDO_SETTING							
BB	R/W/PE	MODE6_LDO_POWER_ON_DELAY							
BC	R/W/PE	MODE6_GPIO_POWER_ON_DELAY							
BD	R/W/PE	MODE7_VOUT1_SETTING_HIGH							
BE	R/W/PE	MODE7_VOUT2_SETTING_HIGH							
BF	R/W/PE	MODE7_BUCK1_FB_HALF	MODE7_BUCK1_FB_HALF	MODE7_BUCK1_FB_HALF			MODE7_BUCK1_FB_HALF		
C0	R/W/PE	MODE7_CLK_MODE	MODE7_CLK_MODE	MODE7_CLK_MODE		MODE7_CLK_MODE		MODE7_CLK_MODE	
C1	R/W/PE	MODE7_BUCK1_POWER_ON_DELAY							
C2	R/W/PE	MODE7_BUCK2_POWER_ON_DELAY							
C3	R/W/PE	MODE7_VOUT1_SOFT_START_TIME			MODE7_VOUT2_SOFT_START_TIME			MODE7_LDO_EN	RV
C4	R/W/PE	MODE7_LDO_SOFT_START_TIME			MODE7_I2C_ADDRESS			MODE7_GPIO_CTRL	

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MODE REGION REGISTER MAP *(continued)* (9) (10) (11) (12)

Add. (0X)	R/W	D7	D6	D5	D4	D3	D2	D1	D0
C5	R/W/ PE	MODE7_LDO_SETTING							
C6	R/W/ PE	MODE7_LDO_POWER_ON_DELAY							
C7	R/W/ PE	MODE7_GPIO_POWER_ON_DELAY							

Notes:

9) RO: Read only. This bit can be read. Writes have no effect.
10) R/W: Read/write. This bit can be read or written by the I²C master
11) RV: Reserved: This bit is reserved for future expansion and its value must not be modified.
12) W1C: Write “1” only. This bit can only be set (i.e. write “1”) but not reset (i.e. write “0”). Writing “0” has no effect.

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I²C REGISTER REGION DESCRIPTION

The I²C registers are volatile memories. These registers directly control converter operation.

LOCK (00h)

The LOCK command locks the writes for the I²C registers.

Bits	Access	Bit Name	Default	Description
D[0]	R/W	I2C_LOCK_EN	1'b 1	Enables locking writes for the I²C registers. I²C writing is ineffective when LOCK_EN = 1. 1'b 0: Disabled 1'b 1: Enabled

BUCK1_CTRL1 (01h)

The BUCK1_CTRL1 command controls buck converter 1 (buck 1).

Bits	Access	Bit Name	Default	Description
D[7]	R/W	VOUT1_GO_BIT	1'b 0	VOUT1_GO_BIT is a self-clearing bit. Make the new VOUT1_SETTING configuration, then set VOUT1_GO_BIT = 1 to start dynamic voltage scaling. When V_{OUT1} reaches the new voltage target, VOUT1_GO_BIT is automatically cleared. 1'b 0: Disable changing VOUT1_SETTING 1'b 1: Enable changing VOUT1_SETTING on the fly
D[6:2]	R/W	RV	5'b 0000 0	Reserved.
D[1:0]	R/W	VOUT1_SLEW_RATE	2'b 00	Sets the V_{OUT1} slew rate during dynamic voltage scaling (no external FB resistor divider). 2'b 00: 0.5mV/μs 2'b 01: 1mV/μs 2'b 10: 2mV/μs 2'b 11: 4mV/μs

BUCK1_CTRL2 (02h)

The BUCK1_CTRL2 command sets buck 1's mode and switching frequency.

Bits	Access	Bit Name	Default	Description
D[7:6]	RW	BUCK1_PFM/PWM	2'b 11	Selects buck 1's mode. 2'b 00, 01: Reserved 2'b 10: Constant-on-time (COT); discontinuous conduction mode (DCM) at light loads 2'b 11: COT; forced continuous current mode (FCCM)
D[5:4]	RW	BUCK1_FSW	2'b 10	Sets buck 1's switching frequency. 2'b 00: 500kHz 2'b 01: 750kHz 2'b 10: 1000kHz 2'b 11: 1250kHz
D[3]	RW	RV	1'b 0	Reserved.
D[2:0]	RW	VOUT1_SETTING_LOW	3'b 000 (Or MODE-Determined)	Works with VOUT1_SETTING_HIGH to set V_{OUT1}.

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BUCK1_CTRL3 (03h)

The BUCK1_CTRL3 command sets buck 1's output voltage (V_{OUT1}).

Bits	Access	Bit Name	Default	Description
D[7:0]	R/W	VOUT1_SETTING_HIGH	8'b 0110 0100 (Or MODE-Determined)	VOUT1_SETTING_HIGH works with VOUT1_SETTING_LOW. By adding these bits together, an 11-bit register controls V_{OUT1}. When BUCK1_FB_HALF = 0: If the bits value ≤ 001 0010 1100 (300d), the setting = 300mV. If 001 0010 1100 (300d) ≤ the bits value ≤ 111 1111 1111 (2047d), then the bits value is defined as equal to *X*, with the setting = *X*(mV). 1mV/step. When BUCK1_FB_HALF = 1: If the bits value ≤ 000 1001 0110 (150d), the setting = 300mV. If 000 1001 0110 (150d) ≤ the bits value ≤ 111 0110 1100 (1900d), then the bits value is defined as equal to *X*, with the setting = 2 x *X*(mV). 2mV/step. If the bits value ≥ 111 0110 1100 (1900d), the setting = 3800mV.

BUCK1_CTRL4 (04h)

The BUCK1_CTRL4 command sets buck 1's output passive discharge function, over-voltage protection (OVP) function, and valley current limit threshold.

Bits	Access	Bit Name	Default	Description
D[7]	R/W	VOUT1_DISCHRGE_EN	1'b 1	Enables buck 1's output passive discharge function. If the passive discharge function is enabled, when buck 1 is disabled, a discharging resistor is connected to the VOUT1_FB_P pin to discharge V_{OUT1} until it reaches 100mV. 1'b 0: Disabled 1'b 1: Enabled
D[6]	R/W	VOUT1_OVP_EN	1'b 1	Enables buck 1's output active OVP function. If output OVP is enabled, buck 1 actively turns on the LS-FET to discharge V_{OUT1}. See the Over-Voltage Protection (OVP) section on page 20 for more details. 1'b 0: Disabled 1'b 1: Enabled
D[5]	R/W	RV	1'b 0	Reserved.
D[4:2]	R/W	BUCK1_OC_TH	3'b 111	Sets buck 1's valley current limit threshold. 3'b 000: 4A 3'b 001: 4.5A 3'b 010: 5A 3'b 011: 5.5A 3'b 100: 6A 3'b 101: 6.5A 3'b 110: 7A 3'b 111: 7.5A
D[1:0]	R/W	RV	2'b 00	Reserved.

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BUCK1_CTRL7 (05h)

The BUCK1_CTRL7 command sets V_{OUT1}'s power good (PG), under-voltage (UV), and over-voltage (OV) thresholds.

Bits	Access	Bit Name	Default	Description
D[7:6]	R/W	VOUT1_PG_VTH_HIGH	2'b 01	Sets V_{OUT1}'s high-side voltage for the power good status (no external FB resistor divider). The hysteresis = 2.5%. 2'b 00: +5% from VOUT1_SETTING 2'b 01: +7.5% from VOUT1_SETTING 2'b 10: +10% from VOUT1_SETTING 2'b 11: Reserved
D[5]	R/W	VOUT1_PG_VTH_LOW	1'b 0	Sets V_{OUT1}'s low-side voltage for the power good status. The hysteresis = 2.5%. 1'b 0: -5% from VOUT1_SETTING 1'b 1: -7.5% from VOUT1_SETTING
D[4]	R/W	RV	1'b 0	Reserved.
D[3:2]	R//W	VOUT1_UV_VTH	2'b 00	Sets V_{OUT1}'s under-voltage (UV) status threshold. The hysteresis = 2.5%. 2'b 00: -10% from VOUT1_SETTING 2'b 01: -12.5% from VOUT1_SETTING 2'b 10: Reserved 2'b 11: Reserved
D[1:0]	R//W	VOUT1_OV_VTH	2'b 10	Sets V_{OUT1}'s over-voltage (OV) status threshold. The hysteresis = 2.5%. 2'b 00: +7.5% from VOUT1_SETTING 2'b 01: +10% from VOUT1_SETTING 2'b 10: +12.5% from VOUT1_SETTING 2'b 11: Reserved

BUCK2_CTRL1 (06h)

The BUCK2_CTRL1 command controls buck converter 2 (buck 2).

Bits	Access	Bit Name	Default	Description
D[7]	R/W	VOUT2_GO_BIT	1'b 0	VOUT2_GO_BIT is a self-clearing bit. Make the new VOUT2_SETTING configuration, then set VOUT2_GO_BIT = 1 to start dynamic voltage scaling. When V_{OUT2} reaches the new voltage target, VOUT2_GO_BIT is automatically cleared. 1'b 0: Disable changing VOUT2_SETTING 1'b 1: Enable changing VOUT2_SETTING on the fly
D[6:2]	R/W	RV	5'b 0000 0	Reserved.
D[1:0]	R/W	VOUT2_SLEW_RATE	2'b 00	Sets the V_{OUT2} slew rate during dynamic voltage scaling (no external FB resistor divider). 2'b 00: 0.5mV/μs 2'b 01: 1mV/μs 2'b 10: 2mV/μs 2'b 11: 4mV/μs

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BUCK2_CTRL2 (07h)

The BUCK2_CTRL2 command sets buck 2's mode and switching frequency.

Bits	Access	Bit Name	Default	Description
D[7:6]	RW	BUCK2_PFM/PWM	2'b 11	Selects buck 2's mode. 2'b 00, 01: Reserved 2'b 10: Constant-on-time (COT); discontinuous conduction mode (DCM) at light loads 2'b 11: COT; forced continuous current mode (FCCM)
D[5:4]	RW	BUCK2_FSW	2'b 10	Sets buck 2's switching frequency. 2'b 00: 500kHz 2'b 01: 750kHz 2'b 10: 1000kHz 2'b 11: 1250kHz
D[3]	RW	RESERVED	1'b 0	Reserved.
D[2:0]	RW	VOUT2_SETTING_ LOW	3'b 000 (Or MODE-Determined)	Works with VOUT2_SETTING_HIGH to set V_{OUT2}.

BUCK2_CTRL3 (08h)

The BUCK2_CTRL3 command sets buck 2's output voltage.

Bits	Access	Bit Name	Default	Description
D[7:0]	R/W	VOUT2_SETTING_ HIGH	8'b 0110 0100 (Or MODE-Determined)	VOUT2_SETTING_HIGH works with VOUT2_SETTING_LOW. By adding these bits together, an 11-bit register controls V_{OUT2}. When BUCK2_FB_HALF = 0: If the bits value ≤ 001 0010 1100 (300d), the setting = 300mV. If 001 0010 1100 (300d) ≤ the bits value ≤ 111 1111 1111 (2047d), then the bits value is defined as equal to *X*, with the setting = *X*(mV). 1mV/step. When BUCK2_FB_HALF = 1: If the bits value ≤ 000 1001 0110 (150d), the setting = 300mV. If 000 1001 0110 (150d) ≤ the bits value ≤ 111 0110 1100 (1900d), then the bits value is defined as equal to *X*, with the setting = 2 x *X*(mV). 2mV/step. If the bits value ≥ 111 0110 1100 (1900d), the setting = 3800mV.

BUCK2_CTRL4 (09h)

The BUCK2_CTRL4 command controls buck 2.

Bits	Access	Bit Name	Default	Description
D[7]	R/W	VOUT2_DISCHRGE_ EN	1'b 1	Enables buck 2's output passive discharge function. If the passive discharge function is enabled, when buck 2 is disabled, a discharging resistor is connected to the VOUT2_FB_P pin to discharge V_{OUT2} until it reaches 100mV. 1'b 0: Disabled 1'b 1: Enabled

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D[6]	R/W	VOUT2_OVP_EN	1'b 1	Enables buck 2's output active OVP function. If output OVP function is enabled, buck 2 actively turns on the LS-FET to discharge V_{OUT2}. See the Over-Voltage Protection (OVP) section on page 20 for more details. 1'b 0: Disabled 1'b 1: Enabled
D[5]	R/W	RV	1'b 0	Reserved.
D[4:2]	R/W	BUCK2_OC_TH	3'b 111	Sets buck 2's valley current limit threshold. 3'b 000: 4A 3'b 001: 4.5A 3'b 010: 5A 3'b 011: 5.5A 3'b 100: 6A 3'b 101: 6.5A 3'b 110: 7A 3'b 111: 7.5A
D[1:0]	R/W	RV	2'b 00	Reserved.

BUCK2_CTRL7 (0Ah)

The BUCK2_CTRL7 command sets V_{OUT2}'s power good (PG), under-voltage (UV), and over-voltage (OV) thresholds.

Bits	Access	Bit Name	Default	Description
D[7:6]	R/W	VOUT2_PG_VTH_HIGH	2'b 01	Sets V_{OUT2}'s high-side voltage for the power good status (no external FB resistor divider). The hysteresis = 2.5%. 2'b 00: +5% from VOUT2_SETTING 2'b 01: +7.5% from VOUT2_SETTING 2'b 10: +10% from VOUT2_SETTING 2'b 11: Reserved
D[5]	R/W	VOUT2_PG_VTH_LOW	1'b 0	Sets V_{OUT2}'s low-side voltage threshold for the power good status. The hysteresis = 2.5%. 1'b 0: -5% from VOUT2_SETTING 1'b 1: -7.5% from VOUT2_SETTING
D[4]	RW	RV	1'b 0	Reserved.
D[3:2]	R/W	VOUT2_UV_VTH	2'b 00	Sets V_{OUT2}'s under-voltage (UV) status threshold. The hysteresis = 2.5%. 2'b 00: -10% from VOUT2_SETTING 2'b 01: -12.5% from VOUT2_SETTING 2'b 10: Reserved 2'b 11: Reserved
D[1:0]	R/W	VOUT2_OV_VTH	2'b 10	Sets V_{OUT2}'s over-voltage (OV) status threshold. The hysteresis = 2.5%. 2'b 00: +7.5% from VOUT2_SETTING 2'b 01: +10% from VOUT2_SETTING 2'b 10: +12.5% from VOUT2_SETTING 2'b 11: Reserved

LDO_CTRL1 (0Bh)

The LDO_CTRL1 command controls the low-dropout (LDO) regulator.

Bits	Access	Bit Name	Default	Description
D[7]	R/W	LDO_GO_BIT	1'b 0	1'b 0: Disable changing LDO_SETTING on the fly 1'b 1: Enable changing LDO_SETTING on the fly

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D[6:2]	RV	RESERVED	5'b 0000 0	Reserved.
D[1]	R/W	LDO_DISCHG	1'b 1	1'b 0: Disable LDO discharge 1'b 1: Enable LDO discharge
D[0]	R/W	LDO_PG_VTH	1'b 0	Sets the LDO output threshold voltage for the power good status. The hysteresis = 5%. 1'b 0: -10% from LDO_SETTING 1'b 1: -15% from LDO_SETTING

LDO_CTRL2 (0Ch)

The LDO_CTRL2 command controls the LDO.

Bits	Access	Bit Name	Default	Description
D[7]	R/W	RV	1'b 0	Reserved.
D[6:0]	R/W	LDO_SETTING	7'b 011 1100 (Or MODE-determined)	Sets the LDO's output voltage. 30mV per LSB from 0.6V to 3.6V. All lower settings: Reserved 7'b 001 0100: 600mV 7'b 001 0101: 630mV … 7'b 111 1000: 3600mV All higher settings: Reserved

SYS_CTRL1 (0Dh)

The SYS_CTRL1 command enables the bucks, the LDO, and GPIO control.

Bits	Access	Bit Name	Default	Description
D[7]	R/W	CONVERTER_EN	1'b 1	1'b 0: Buck 1, buck 2, and the LDO are all disabled 1'b 1: Buck 1, buck 2, and the LDO are all enabled (must enable each regulator via I²C set-up)
D[6]	R/W	VOUT1_EN	1'b 1	1'b 0: Disable buck 1 1'b 1: Enable buck 1
D[5]	R/W	VOUT2_EN	1'b 1	1'b 0: Disable buck 2 1'b 1: Enable buck 2
D[4]	R/W	LDO_EN	1'b 0	1'b 0: Disable the LDO 1'b 1: Enable the LDO
D[3:2]	R/W	RV	2'b 00	Reserved
D[1:0]	R/W	GPIO_CTRL	2'b 10	Sets GPIO's open-drain output control. 2'b 00: The GPIO output is low 2'b 01: GPIO is an analog input for the ADC 2'b 10: GPIO is part of flex-time control and used as the external converter's enable signal. GPIO outputs as an EN signal for the external converter and its on/off sequence can be configured via the 0x57 and 0x58 registers 2'b 11: The GPIO output is floating/high

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SYS_CTRL3 (0Eh)

The SYS_CTRL3 command sets the V_{IN} rising threshold and controls the PG mask.

Bits	Access	Bit Name	Default	Description
D[7:5]	R/W	VIN_PG_VTH	3'b 110	Sets the V_{IN} rising threshold for VIN_PG. VIN_PG (0x19) is 0 (power good) even if V_{IN} < V_{IN} PG falling threshold after V_{IN} start-up. Then ramp up V_{IN} to be ≥ V_{IN} rising threshold. If V_{IN} triggers the V_{IN} PG falling threshold again, VIN_PG changes to 1 (power not good). The hysteresis = 0.5V. 3'b 000: 9.5V (same as 001) 3'b 001: 9.5V 3'b 010: 8.5V 3'b 011: 7.5V 3'b 100: 6.5V 3'b 101: 5.5V 3'b 110: 4.25V 3'b 111: Reserved
D[4]	R/W	MASK_PG	1'b 0	Masks the INT pin behavior. The STATUS register still indicates the PG status. 1'b 0: Not masked 1'b 1: Masked
D[3:0]	R/W	RV	4'b 0000	Reserved.

SYS_CTRL4 (0Fh)

The SYS_CTRL4 command sets the over-temperature (OT) threshold and OT warning threshold.

Bits	Access	Bit Name	Default	Description
D[7:5]	R/W	OT_TH	3'b 100	Sets the converter's temperature shutdown threshold. The hysteresis = 20°C. 3'b 000: 125°C 3'b 001: 135°C 3'b 010: 145°C 3'b 011: 155°C 3'b 100: 165°C 3'b 101: Reserved 3'b 110: Reserved 3'b 111: Reserved
D[4:2]	R/W	OTW_TH	3'b 101	Sets the OT warning threshold. The hysteresis = 20°C. 3'b 000: Reserved 3'b 001: 100°C 3'b 010: 110°C 3'b 011: 120°C 3'b 100: 130°C 3'b 101: 140°C 3'b 110: 150°C 3'b 111: Reserved
D[1:0]	R/W	RV	2'b 00	Reserved.

ADC_CTRL1 (10h)

The ADC_CTRL1 command controls the analog-to-digital converter (ADC).

Bits	Access	Bit Name	Default	Description
D[7]	R/W	ADC_EN	1'b 1	1'b 0: Disable the ADC 1'b 1: Enable the ADC
D[6:2]	R/W	RESERVED	5'b 00000	Reserved.

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D[1:0]	R/W	ADC_SAMPLE_ FREQ	2'b 01	Sets the frequency at which to refresh all the ADC channels. 2'b 00: 4kHz 2'b 01: 2kHz 2'b 10: 1kHz 2'b 11: 0.5kHz

TEMPERATURE (11h)

The TEMPERATURE command indicates the PMIC's temperature.

Bits	Access	Bit Name	Default	Description
D[7:5]	R/O	TEMPERATURE	3'b 000	Indicates the PMIC's temperature. 3'b 000: ≤80°C 3'b 001: 85°C 3'b 010: 95°C 3'b 011: 105°C 3'b 100: 115°C 3'b 101: 125°C 3'b 110: 135°C 3'b 111: ≥140°C
D[4:0]	R/W	RV	5'b 00000	Reserved.

VOUT1_ADC (12h)

The VOUT1_ADC command returns buck 1's output voltage (V_{OUT1}).

Bits	Access	Bit Name	Default	Description
D[7:0]	RO	VOUT1_ADC	8'b 0000 0000	Returns V_{OUT1}. 16mV/LSB. 8'b 0000 0000: Undefined 8'b 0000 0001: 16mV 8'b 0000 0010: 32mV … 8'b 1111 1110: 4080mV 8'b 1111 1111: 4096mV

IOUT1_ADC (13h)

The IOUT1_ADC command monitors buck 1's output current (I_{OUT1}).

Bits	Access	Bit Name	Default	Description
D[7:0]	RO	IOUT1_ADC	8'b 0000 0000	Returns I_{OUT1}. 50mA/LSB. All other encodings are reserved. 8'b 0000 0000: 0A 8'b 0000 0001: 0.05A 8'b 0000 0010: 0.1A … 8'b 1111 1110: 12.7A 8'b 1111 1111: 12.75A

VOUT2_ADC (14h)

The VOUT2_ADC command returns buck 2's output voltage (V_{OUT2}).

Bits	Access	Bit name	Default	Description
D[7:0]	RO	VOUT2_ADC	8'b 0000 0000	Returns V_{OUT2}. 16mV/LSB. 8'b 0000 0000: Undefined 8'b 0000 0001: 16mV 8'b 0000 0010: 32mV … 8'b 1111 1110: 4080mV 8'b 1111 1111: 4096mV

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IOUT2_ADC (15h)

The IOUT2_ADC command returns buck 2's output current (I_{OUT2}).

Bits	Access	Bit name	Default	Description
D[7:0]	RO	IOUT2_ADC	8'b 0000 0000	Returns I_{OUT2}. 50mA/LSB. All other encodings are reserved. 8'b 0000 0000: 0A 8'b 0000 0001: 0.05A 8'b 0000 0010: 0.1A … 8'b 1111 1110: 12.7A 8'b 1111 1111: 12.75A

LDO_ADC (16h)

Format: Direct

The LDO_ADC command returns the LDO's output voltage.

Bits	Access	Bit Name	Default	Description
D[7:0]	RO	LDO_ADC	8'b 0000 0000	Returns the LDO's output voltage. 16mV/LSB. 8'b 0000 0000: Undefined 8'b 0000 0001: 16mV 8'b 0000 0010: 32mV … 8'b 1111 1110: 4080mV 8'b 1111 1111: 4096mV

GPIO_ADC (17h)

The GPIO_ADC command monitors the GPIO voltage.

Bits	Access	Bit Name	Default	Description
D[7:0]	RO	GPIO_ADC	8'b 0000 0000	Returns the GPIO's voltage. 8mV/LSB. 8'b 0000 0000: 0mV 8'b 0000 0001 : 8mV … 8'b 1111 1111: 2040mV

VIN_ADC (18h)

The VIN_ADC command returns the input voltage (V_{IN}).

Bits	Access	Bit Name	Default	Description
D[7:0]	RO	VIN_ADC	8'b 0000 0000	Returns V_{IN}. 64mV/LSB. 8'b 0000 0000: 0mV 8'b 0000 0001: 64mV 8'b 0000 0010: 128mV … 8'b 1111 1111: 16320mV

STATUS1 (19h)

The STATUS1 command indicates the fault statuses for the following conditions: V_{IN} power good, $V_{OUT1/2}$ over-voltage (OV), LDO power good, and over-temperature warning and shutdown.

Bits	Access	Bit Name	Description
D[7]	RO	VIN_PG	Indicates V_{IN}'s power good status. 1'b 0: Power good 1'b 1: Power not good

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D[6]	RO	VOUT1_PG	Indicates V_{OUT1}'s OV fault status. 1'b 0: Normal start-up 1'b 1: A V_{OUT1} fault has occurred
D[5]	RO	VOUT2_PG	Indicates V_{OUT2}'s OV fault status. 1'b 0: Normal start-up 1'b 1: A V_{OUT2} fault has occurred
D[4]	RO	LDO_PG	Indicates the LDO's power good status. 1'b 0: Power good 1'b 1: Power not good
D[3:2]	RO	RV	Reserved.
D[1]	RO	OTW	Indicates the over-temperature (OT) warning status. 1'b 0: The temperature is below the warning threshold 1'b 1: The temperature exceeds the warning threshold
D[0]	RO	OT	Indicates the temperature shutdown status. 1'b 0: No temperature shutdown has occurred 1'b 1: Temperature shutdown has occurred

STATUS2 (1Ah)

The STATUS2 command indicates the fault statuses for the following conditions: V_{IN} over-voltage (OV), V_{IN} under-voltage (UV), $V_{OUT1/2}$ OV, $V_{OUT1/2}$ UV, and output current limit warning.

Bits	Access	Bit Name	Description
D[7]	RO	VIN_OV	Indicates the V_{IN} OV status. 1'b 0: No OV condition 1'b 1: There is an OV condition
D[6]	RO	VIN_UV	Indicates the V_{IN} UV status. 1'b 0: No UV condition 1'b 1: There is an UV condition
D[5]	RO	VOUT1_OV	Indicates the V_{OUT1} OV status. 1'b 0: No OV condition 1'b 1: There is an OV condition
D[4]	RO	VOUT2_OV	Indicates the V_{OUT2} OV status. 1'b 0: No OV condition 1'b 1: There is an OV condition
D[3]	RO	VOUT1_UV	Indicates the V_{OUT1} UV status. 1'b 0: No UV condition 1'b 1: There is an UV condition
D[2]	RO	VOUT2_UV	Indicates the V_{OUT2} UV status. 1'b 0: No UV condition 1'b 1: There is an UV condition
D[1]	RO	VOUT1_OC	Indicates buck 1's output current limit warning status. 1'b 0: No current-limit event has occurred 1'b 1: A current-limit event has occurred
D[0]	RO	VOUT2_OC	Indicates buck 2's output current limit warning status. 1'b 0: No current-limit event has occurred 1'b 1: A current-limit event has occurred

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MASK1 (1Bh)

The MASK1 command masks the INT pin's behavior for the following condition: V_{IN} power good, $V_{OUT1/2}$ power good, LDO power good, over-temperature warning and over-temperature shutdown. The STATUS register still indicates each event.

Bits	Access	Bit Name	Default	Description
D[7]	RW	VIN_PG_MSK	1'b 0	1'b 0: Do not mask 1'b 1: Mask
D[6]	RW	VOUT1_PG_MSK	1'b 0	1'b 0: Do not mask 1'b 1: Mask
D[5]	RW	VOUT2_PG_MSK	1'b 0	1'b 0: Do not mask 1'b 1: Mask
D[4]	RW	LDO_PG_MSK	1'b 0	1'b 0: Do not mask 1'b 1: Mask
D[3:2]	RW	RV	2'b 00	Reserved.
D[1]	RW	OTW_MSK	1'b 0	1'b 0: Do not mask 1'b 1: Mask
D[0]	RW	OT_MSK	1'b 0	1'b 0: Do not mask 1'b 1: Mask

MASK2 (1Ch)

The MASK2 command masks the INT pin's behavior for the following conditions: V_{IN} over-voltage (OV), V_{IN} under-voltage (UV), $V_{OUT1/2}$ OV, $V_{OUT1/2}$ UV, and $I_{OUT1/2}$ over-current (OC). The STATUS register still indicates each event.

Bits	Access	Bit Name	Default	Description
D[7]	RW	VIN_OV_MSK	1'b 0	1'b 0: Do not mask 1'b 1: Mask
D[6]	RW	VIN_UV_MSK	1'b 0	1'b 0: Do not mask 1'b 1: Mask
D[5]	RW	VOUT1_OV_MSK	1'b 0	1'b 0: Do not mask 1'b 1: Mask
D[4]	RW	VOUT2_OV_MSK	1'b 0	1'b 0: Do not mask 1'b 1: Mask
D[3]	RW	VOUT1_UV_MSK	1'b 0	1'b 0: Do not mask 1'b 1: Mask
D[2]	RW	VOUT2_UV_MSK	1'b 0	1'b 0: Do not mask 1'b 1: Mask
D[1]	RW	VOUT1_OC_MSK	1'b 0	1'b 0: Do not mask 1'b 1: Mask
D[0]	RW	VOUT2_OC_MSK	1'b 0	1'b 0: Do not mask 1'b 1: Mask

CLEAR1 (1Dh)

The CLEAR1 command clears the corresponding fault bits that have been set.

Bits	Access	Bit Name	Default	Description
D[7]	W1C	VIN_PG_CLEAR	1'b 0	Clears the V_{IN} power good status. 1'b 1: Clear the status

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D[6]	W1C	VOUT1_FAULT_CLEAR	1'b 0	Clears the V_{OUT1} power good status. 1'b 1: Clear the status
D[5]	W1C	VOUT2_FAULT_CLEAR	1'b 0	Clears the V_{OUT2} power good status. 1'b 1: Clear the status
D[4]	W1C	LDO_FAULT_CLEAR	1'b 0	Clears the LDO power good status. 1'b 1: Clear the status
D[3]	W1C	OTW_CLEAR	1'b 0	Clears the over-temperature (OT) warning status. 1'b 1: Clear the status
D[2]	W1C	OT_CLEAR	1'b 0	Clears the OT status. 1'b 1: Clear the status
D[1]	W1C	RV	1'b 0	Reserved
D[0]	W1C	ALL_STATUS_CLEAR	1'b 0	1'b 1: Clears all the status bits

CLEAR2 (1Eh)

The CLEAR2 command clears the corresponding fault bits that have been set.

Bits	Access	Bit Name	Default	Description
D[7]	W1C	VIN_OV_CLEAR	1'b 0	Clears the V_{IN} over-voltage (OV) status. 1'b 1: Clear the status
D[6]	W1C	VIN_UV_CLEAR	1'b 0	Clears the V_{IN} under-voltage (UV) status. 1'b 1: Clear the status
D[5]	W1C	VOUT1_OV_CLEAR	1'b 0	Clears the V_{OUT1} OV status. 1'b 1: Clear the status
D[4]	W1C	VOUT2_OV_CLEAR	1'b 0	Clears the V_{OUT2} OV status. 1'b 1: Clear the status
D[3]	W1C	VOUT1_UV_CLEAR	1'b 0	Clears the V_{OUT1} UV status. 1'b 1: Clear the status
D[2]	W1C	VOUT2_UV_CLEAR	1'b 0	Clears the V_{OUT2} UV status. 1'b 1: Clear the status
D[1]	W1C	VOUT1_OC_CLEAR	1'b 0	Clears buck 1's output current limit warning status. 1'b 1: Clear the status
D[0]	W1C	VOUT2_OC_CLEAR	1'b 0	Clear buck 2's output current limit warning status. 1'b 1: Clear the status

AVP_CTRL1 (1Fh)

The AVP_CTRL1 command enables the AVP function for buck 1.

Bits	Access	Bit Name	Default	Description
D[7]	R/W	AVP1_EN	1'b 0	Enables buck 1's AVP function. 1'b 0: Disabled 1'b 1: Enabled

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D[6:5]	R/W	AVP1_GAIN	2'b 00	Sets the AVP gain. 2'b 00: 3mV/A 2'b 01: 5.5mV/A 2'b 10: Reserved 2'b 11: Reserved
D[4:0]	R/W	AVP1_OFFSET	5'b 0000 1	Sets the DC offset voltage for the output voltage command value when AVP is enabled. This offset ranges between -30mV and +30mV. 2mV/step. AVP1_OFFSET is valid after setting AVP1_EN = 1 and GO_BIT = 1 when changing it on fly. 5'b x 0000: 0mV 5'b 0 0001: 2mV … 5'b 0 1111: 30mV 5'b 1 0001: -2mV … 5'b 1 1111: -30mV

AVP_CTRL2 (20h)

This AVP_CTRL2 command enables the AVP function for buck 2.

Bits	Access	Bit Name	Default	Description
D[7]	R/W	AVP2_EN	1'b 0	Enables buck 2's AVP function. In dual-phase, single-output mode, this function is invalid. 1'b 0: Disabled 1'b 1: Enabled
D[6:5]	R/W	AVP2_GAIN	2'b 00	Sets the AVP gain. In dual-phase, single-output mode, this function is invalid. 2'b 00: 3mV/A 2'b 01: 5.5mV/A 2'b 10: Reserved 2'b 11: Reserved
D[4:0]	R/W	AVP2_OFFSET	5'b 0000 1	Sets the DC offset voltage for the output voltage command value when AVP is enabled. This offset ranges between -30mV and +30mV. 2mV/step. AVP2_OFFSET is valid after setting AVP2_EN = 1 and GO_BIT = 1 when changing it on fly. 5'b x 0000: 0mV 5'b 0 0001: 2mV … 5'b 0 1111: 30mV 5'b 1 0001: -2mV … 5'b 1 1111: -30mV

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MTP REGISTER REGION

The MTP registers are non-volatile memories. Most of the MTP registers are related to the registers from the I²C. The MTP registers do not directly control the converter's operation. During start-up through VIN, the settings are copied from the MTP registers to the I²C registers.

LOCK (40h)

The LOCK command requires the correct password to be written to the register to access the MTP register region and MODE register region.

Bits	Access	Bit Name	Default	Description
D[7:0]	R/W	MTP_REGION_ ACCESS_ PASSWORD	8'b 0000 0000	The correct password must be used to access the MTP register region and MODE register region. Contact an MPS FAE for the password.

BUCK1_CTRL1 (41h)

The BUCK1_CTRL1 command sets the default settings for BUCK1_CTRL1 (01h). The only bits that have direct control of converter operation are VOUT1_SOFT_START and VOUT1_SOFT_STOP.

Bits	Access	Bit Name	Default	Description
D[7]	R/W	RV	1'b 0	Reserved.
D[6:4]	R/W	VOUT1_SOFT_ START	3'b 001 (Or MODE-Determined)	Sets buck 1's soft-start time after being enabled. The output is between 0% and 100% of V_{OUT1}. 3'b 000: 1ms 3'b 001: 2ms 3'b 010: 4ms 3'b 011: 6ms 3'b 100: 8ms 3'b 101: 10ms 3'b 110: 12ms 3'b 111: 14ms
D[3:2]	R/W	VOUT1_SOFT_STOP	2'b 00	Sets buck 1's soft-stop time after being enabled. The output is between 0% and 100% of V_{OUT1}. 2'b 00: 0.5ms 2'b 01: 1ms 2'b 10: 2ms 2'b 11: 4ms
D[1:0]	R/W	VOUT1_SLEW_RATE	2'b 00	Sets V_{OUT1}'s slew rate during dynamic voltage scaling (no external FB resistor divider). 2'b 00: 0.5mV/μs 2'b 01: 1mV/μs 2'b 10: 2mV/μs 2'b 11: 4mV/μs

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BUCK1_CTRL2 (42h)

The BUCK1_CTRL2 command sets the default setting for BUCK1_CTRL2 (02h). This command does not have direct control of converter operation. In dual-phase, single-output mode, BUCK2_FSW, BUCK2_PFM/PWM, and VOUT2 settings are masked; instead, these values are determined by buck 1's corresponding setting.

In single-phase, dual-output mode, it is recommended to set BUCK1_FSW and BUCK2_FSW to the same frequency.

Bits	Access	Bit Name	Default	Description
D[7:6]	RW	BUCK1_PFM/PWM	2'b 11	Selects buck 1's mode. 2'b 00, 01: Reserved 2'b 10: Constant-on-time (COT); discontinuous conduction mode (DCM) at light loads 2'b 11: COT; forced continuous current mode (FCCM)
D[5:4]	RW	BUCK1_FSW	2'b 10	Sets buck 1's switching frequency. 2'b 00: 500kHz 2'b 01: 750kHz 2'b 10: 1000kHz 2'b 11: 1250kHz
D[3]	RW	RV	1'b 0	Reserved.
D[2:0]	RW	VOUT1_SETTING_LOW	3'b 000 (Or MODE-Determined)	Works with VOUT1_SETTING_HIGH to set V_{OUT1}.

BUCK1_CTRL3 (43h)

The BUCK1_CTRL3 command sets the default setting for BUCK1_CTRL3 (03h). This command does not have direct control of converter operation.

Bits	Access	Bit Name	Default	Description
D[7:0]	R/W	VOUT1_SETTING_HIGH	8'b 0110 0100 (Or MODE-Determined)	VOUT1_SETTING_HIGH works with VOUT1_SETTING_LOW. By adding these bits together, an 11-bit register controls V_{OUT1}. When BUCK1_FB_HALF = 0: If the bits value ≤ 001 0010 1100 (300d), the setting = 300mV. If 001 0010 1100(300d) ≤ the bits value ≤ 111 1111 1111 (2047d), then the bits value is defined as equal to *X*, with the setting = *X*(mV). 1mV/step. When BUCK1_FB_HALF = 1: If the bits value ≤ 000 1001 0110 (150d), the setting = 300mV. If 000 1001 0110 (150d) ≤ the bits value ≤ 111 0110 1100 (1900d), then the bits value is defined as equal to *X*, with the setting = 2 x *X*(mV). 2mV/step. If the bits value ≥ 111 0110 1100 (1900d), the setting = 3800mV.

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BUCK1_CTRL4 (44h)

The BUCK1_CTRL4 command sets the default setting for BUCK1_CTRL4 (04h). This command does not have direct control of converter operation.

Bits	Access	Bit Name	Default	Description
D[7]	R/W	VOUT1_DISCHG_EN	1'b 1	Enables buck 1's output passive discharge function. If the passive discharge function is enabled, when buck 1 is disabled, a discharging resistor is connected to the VOUT1_FB_P pin to discharge V_{OUT1} until it reaches 100mV. 1'b 0: Disabled 1'b 1: Enabled
D[6]	R/W	VOUT1_OVP_EN	1'b 1	Enables buck 1's output active OVP function. If output OVP is enabled, buck 1 actively turns on the LS-FET to discharge V_{OUT1}. See the Over-Voltage Protection (OVP) section on page 20 for more details. 1'b 0: Disabled 1'b 1: Enabled
D[5]	R/W	BUCK1_FB_HALF	1'b 0	Enables buck 1's internal FB half divider. 1'b 0: There is no internal FB divider 1'b 1: The internal 1/2 divider for FB divider is enabled
D[4:2]	R/W	BUCK1_OC_TH	3'b 111	Sets buck 1's valley current limit threshold. 3'b 000: 4A 3'b 001: 4.5A 3'b 010: 5A 3'b 011: 5.5A 3'b 100: 6A 3'b 101: 6.5A 3'b 110: 7A 3'b 111: 7.5A
D[1:0]	R/W	RESERVED	2'b 00	Reserved.

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BUCK1_CTRL5 (45h)

The BUCK1_CTRL5 command sets buck 1's soft-start delay. It directly controls the converter.

Bits	Access	Bit Name	Default	Description
D[7:0]	R/W	BUCK1_POWER_ON_DELAY	8'b 0000 1100 (Or MODE-Determined)	Sets buck 1's soft-start delay via a number of CLK pulses. 8'b 0000 0000: 0 8'b 0000 0001: 1 8'b 0000 0010: 2 8'b 0000 0011: 3 …… 8'b 0110 0100: 100 8'b 0110 0101: 102 8'b 0110 0110: 104 ……. 8'b 1001 0110: 200 8'b 1001 0111: 204 8'b 1001 1000: 208 …… 8'b 1100 1000: 400 8'b 1100 1001: 408 8'b 1100 1010: 416 …… 8'b 1110 0001: 600 8'b 1110 0010: 616 8'b 1110 0011: 632 …… 8'b 1111 1010: 1000 8'b 1111 1011: 1024 8'b 1111 1100~1111 1111: Reserved

BUCK1_CTRL6 (46h)

The BUCK1_CTRL6 command sets buck 1's soft-shutdown delay. It directly controls the converter.

Bits	Access	Bit Name	Default	Description
D[7:0]	R/W	BUCK1_POWER_OFF_DELAY	8'b 0000 0000	Sets buck 1's soft-stop delay via a number of CLK pulses. 8'b 0000 0000: 0 8'b 0000 0001: 1 8'b 0000 0010: 2 8'b 0000 0011: 3 …… 8'b 0110 0100: 100 8'b 0110 0101: 102 8'b 0110 0110: 104 ……. 8'b 1001 0110: 200 8'b 1001 0111: 204 8'b 1001 1000: 208 …… 8'b 1100 1000: 400 8'b 1100 1001: 408 8'b 1100 1010: 416 …… 8'b 1110 0001: 600 8'b 1110 0010: 616 8'b 1110 0011: 632 …… 8'b 1111 1010: 1000 8'b 1111 1011: 1024 8'b 1111 1100~1111 1111: Reserved

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BUCK1_CTRL7 (47h)

The BUCK1_CTRL7 command sets the default setting for BUCK1_CTRL7 (05h). This command does not have direct control of converter operation.

Bits	Access	Bit Name	Default	Description
D[7:6]	R/W	VOUT1_PG_VTH_ HIGH	2'b 01	Sets V_{OUT1}'s high-side voltage for the power good status. The hysteresis = 2.5%. 2'b 00: +5% from VOUT1_SETTING 2'b 01: +7.5% from VOUT1_SETTING 2'b 10: +10% from VOUT1_SETTING 2'b 11: Reserved
D[5]	R/W	VOUT1_PG_VTH_ LOW	1'b 0	Sets V_{OUT1}'s low-side voltage threshold for the power good status. The hysteresis = 2.5%. 1'b 0: -5% from VOUT1_SETTING 1'b 1: -7.5% from VOUT1_SETTING
D[4]	R/W	RV	1'b 0	Reserved.
D[3:2]	R//W	VOUT1_UV_VTH	2'b 00	Sets V_{OUT1}'s under-voltage (UV) status threshold. The hysteresis = 2.5%. 2'b 00: -10% from VOUT1_SETTING 2'b 01: -12.5% from VOUT1_SETTING 2'b 10: Reserved 2'b 11: Reserved
D[1:0]	R//W	VOUT1_OV_VTH	2'b 10	Sets V_{OUT1}'s over-voltage (OV) status threshold. The hysteresis = 2.5%. 2'b 00: +7.5% from VOUT1_SETTING 2'b 01: +10% from VOUT1_SETTING 2'b 10:+12.5% from VOUT1_SETTING 2'b 11: Reserved

BUCK2_CTRL1 (48h)

The BUCK2_CTRL1 command sets the default setting for BUCK2_CTRL1 (06h). The only bits that have direct control of converter operation are VOUT2_SOFT_START and VOUT2_SOFT_STOP.

Bits	Access	Bit Name	Default	Description
D[7]	R/W	RV	1'b0	Reserved
D[6:4]	R/W	VOUT2_SOFT_ START	3'b 001 (Or MODE-Determined)	Sets buck 2's soft-start time after being enabled. The output is between 0% and 100% of V_{OUT2}. 3'b 000: 1ms 3'b 001: 2ms 3'b 010: 4ms 3'b 011: 6ms 3'b 100: 8ms 3'b 101: 10ms 3'b 110: 12ms 3'b 111: 14ms
D[3:2]	R/W	VOUT2_SOFT_STOP	2'b 00	Sets buck 2's soft-stop time after being enabled. The output is between 0% and 100% of V_{OUT2}. 2'b 00: 0.5ms 2'b 01: 1ms 2'b 10: 2ms 2'b 11: 4ms

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D[1:0]	R/W	VOUT2_SLEW_RATE	2'b 00	Sets V_{OUT2}'s slew rate during dynamic voltage scaling (no external FB resistor divider). 2'b 00: 0.5mV/μs 2'b 01: 1mV/μs 2'b 10: 2mV/μs 2'b 11: 4mV/μs

BUCK2_CTRL2 (49h)

The BUCK2_CTRL2 command sets the default settings for BUCK2_CTRL2 (07h). This command does not have direct control of converter operation. In dual-phase, single-output mode, the BUCK2_FSW, BUCK2_PFM/PWM, and VOUT2 settings are masked; instead, these values are determined by buck 1's corresponding setting.

In single-phase, dual-output mode, it is recommended to set BUCK1_FSW and BUCK2_FSW to the same frequency.

Bits	Access	Bit Name	Default	Description
D[7:6]	RW	BUCK2_PFM/PWM	2'b 11	Selects buck 2's mode. 2'b 00, 01: Reserved 2'b 10: Constant-on-time (COT); discontinuous conduction mode (DCM) 2'b 11: COT; forced continuous current mode (FCCM)
D[5:4]	RW	BUCK2_FSW	2'b 10	Sets buck 2's switching frequency. 2'b 00: 500kHz 2'b 01: 750kHz 2'b 10: 1000kHz 2'b 11: 1250kHz
D[3]	RW	RV	1'b 0	Reserved.
D[2:0]	RW	VOUT2_SETTING_LOW	3'b 000 (Or MODE-Determined)	Works with VOUT2_SETTING_HIGH to set V_{OUT2}.

BUCK2_CTRL3 (4Ah)

The BUCK2_CTRL3 command sets the default settings for BUCK2_CTRL3 (08h). This command does not have direct control of converter operation.

Bits	Access	Bit Name	Default	Description
D[7:0]	R/W	VOUT2_SETTING_HIGH	8'b 0110 0100 (Or MODE-Determined)	VOUT2_SETTING_HIGH works with VOUT2_SETTING_LOW. By adding these bits together, an 11-bit register controls V_{OUT2}. When BUCK2_FB_HALF (4Bh, bit[5]) = 0: If the bits value ⩽ 001 0010 1100 (300d), the setting = 300mV. If 001 0010 1100 (300d) ⩽ the bits value ⩽ 111 1111 1111 (2047d), then the bits value is defined as equal to *X*, with the setting = *X*(mV). 1mV/step. When BUCK2_FB_HALF (4Bh, bit[5]) = 1: If the bits value ⩽ 000 1001 0110 (150d), the setting = 300mV. If 000 1001 0110 (150d) ⩽ the bits value ⩽ 111 0110 1100 (1900d), then the bits value is defined as equal to *X*, with the setting = 2 x *X*(mV). 2mV/step. If the bits value ⩾ 111 0110 1100 (1900d), the setting = 3800mV.

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BUCK2_CTRL4 (4Bh)

The BUCK2_CTRL4 command sets the default setting for BUCK2_CTRL4 (09h). This command does not have direct control of converter operation.

Bits	Access	Bit Name	Default	Description
D[7]	R/W	VOUT2_DISCHG_EN	1'b 1	Enables buck 2's output passive discharge function. If the passive discharge function is enabled, when buck 2 is disabled, a discharging resistor is connected to the VOUT2_FB_P pin to discharge V_{OUT2} until it reaches 100mV. 1'b 0: Disabled 1'b 1: Enabled
D[6]	R/W	VOUT2_OVP_EN	1'b 1	Enables buck 2's output active OVP function. If output OVP is enabled, buck 2 actively turns on the LS-FET to discharge V_{OUT1}. See the Over-Voltage Protection (OVP) section on page 20 for more details. 1'b 0: Disabled 1'b 1: Enabled
D[5]	R/W	BUCK2_FB_HALF	1'b 0	Enables buck 2's internal FB 1/2 divider. 1'b 0: No internal FB divider 1'b 1: The internal 1/2 FB divider is enabled
D[4:2]	R/W	BUCK2_OC_TH	3'b 111	Sets buck 2's valley current limit threshold. 3'b 000: 4A 3'b 001: 4.5A 3'b 010: 5A 3'b 011: 5.5A 3'b 100: 6A 3'b 101: 6.5A 3'b 110: 7A 3'b 111: 7.5A
D[1:0]	R/W	RV	2'b 00	Reserved.

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BUCK2_CTRL5 (4Ch)

The BUCK2_CTRL5 command sets buck 2's soft-start delay by counting a set number of CLK pulses. This command does not have direct control of converter operation.

Bits	Access	Bit Name	Default	Description
D[7:0]	R/W	BUCK2_POWER_ON_DELAY	8'b 0000 1100 (Or MODE-Determined)	Sets buck 2's soft-start delay via CLK pulses. 8'b 0000 0000: 0 8'b 0000 0001: 1 8'b 0000 0010: 2 8'b 0000 0011: 3 …… 8'b 0110 0100: 100 8'b 0110 0101: 102 8'b 0110 0110: 104 ……. 8'b 1001 0110: 200 8'b 1001 0111: 204 8'b 1001 1000: 208 …… 8'b 1100 1000: 400 8'b 1100 1001: 408 8'b 1100 1010: 416 …… 8'b 1110 0001: 600 8'b 1110 0010: 616 8'b 1110 0011: 632 …… 8'b 1111 1010: 1000 8'b 1111 1011: 1024 8'b 1111 1100~1111 1111: Reserved

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BUCK2_CTRL6 (46h)

The BUCK2_CTRL6 command sets buck 2's soft-shutdown delay by counting a set number of CLK pulses. This command does not have direct control of converter operation.

Bits	Access	Bit Name	Default	Description
D[7:0]	R/W	BUCK2_POWER_OFF_DELAY	8'b 0000 0000	Sets buck 2's soft-stop delay via CLK pulses. 8'b 0000 0000: 0 8'b 0000 0001: 1 8'b 0000 0010: 2 8'b 0000 0011: 3 …… 8'b 0110 0100: 100 8'b 0110 0101: 102 8'b 0110 0110: 104 ……. 8'b 1001 0110: 200 8'b 1001 0111: 204 8'b 1001 1000: 208 …… 8'b 1100 1000: 400 8'b 1100 1001: 408 8'b 1100 1010: 416 …… 8'b 1110 0001: 600 8'b 1110 0010: 616 8'b 1110 0011: 632 …… 8'b 1111 1010: 1000 8'b 1111 1011: 1024 8'b 1111 1100~1111 1111: Reserved

BUCK2_CTRL7 (4Eh)

The BUCK2_CTRL7 command sets the default setting for BUCK2_CTRL7 (0Ah). This command does not have direct control of converter operation.

Bits	Access	Bit Name	Default	Description
D[7:6]	R/W	VOUT2_PG_VTH_HIGH	2'b 01	Sets V_{OUT2}'s high-side voltage for the power good status. The hysteresis = 2.5%. 2'b 00: +5% from VOUT2_SETTING 2'b 01: +7.5% from VOUT2_SETTING 2'b 10: +10% from VOUT2_SETTING 2'b 11: Reserved
D[5]	R/W	VOUT2_PG_VTH_LOW	1'b 0	Sets V_{OUT2}'s low-side voltage threshold for the power good status. The hysteresis = 2.5%. 1'b 0: -5% from VOUT2_SETTING 1'b 1: -7.5% from VOUT2_SETTING
D[4]	R/W	RV	1'b 0	Reserved.
D[3:2]	R//W	VOUT2_UV_VTH	2'b 00	Sets V_{OUT2}'s under-voltage (UV) status threshold. The hysteresis = 2.5%. 2'b 00: -10% from VOUT2_SETTING 2'b 01: -12.5% from VOUT2_SETTING 2'b 10: Reserved 2'b 11: Reserved

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D[1:0]	R//W	VOUT2_OV_VTH	2'b 10	Sets V_{OUT2}'s over-voltage (OV) status threshold. The hysteresis = 2.5%. 2'b 00: +7.5% from VOUT2_SETTING 2'b 01: +10% from VOUT2_SETTING 2'b 10:+12.5% from VOUT2_SETTING 2'b 11: Reserved

LDO_CTRL1 (4Fh)

The LDO_CTRL1 command sets the default setting for LDO_CTRL1 (0Bh). The only bits that have direct control of converter operation are LDO_SOFT_START.

Bits	Access	Bit Name	Default	Description
D[7]	R/W	RV	1'b 0	Reserved
D[6:4]	R/W	LDO_SOFT_START	3'b 001 (Or MODE-Determined)	Sets the LDO soft-start time after being enabled. The output is between 0% and 100% of V_{OUT}. 3'b 000: 1ms 3'b 001: 2ms 3'b 010: 4ms 3'b 011: 6ms 3'b 100: 8ms 3'b 101: 10ms 3'b 110: 12ms 3'b 111: 14ms
D[3:2]	RV	RV	2'b 00	Reserved.
D[1]	R/W	LDO_DISCHG	1'b 1	0: Disable LDO discharge 1: Enable LDO discharge
D[0]	R/W	LDO_PG_VTH	1'b 0	Sets the LDO output threshold voltage for the power good status. The hysteresis = 5%. 0: -10% from LDO_SETTING 1: -15% from LDO_SETTING

LDO_CTRL2 (50h)

The LDO_CTRL2 command sets the default setting for LDO_CTRL2 (0Ch). It does not directly control the converter.

Bits	Access	Bit Name	Default	Description
D[7]	R/W	RV	1'b 0	Reserved.
D[6:0]	R/W	LDO_SETTING	7'b 011 1100 (Or MODE-Determined)	LDO output voltage setting: 30mV per LSB from 0.6V to 3.6V All lower setting: Reserved 7'b 001 0100: 600mV 7'b 001 0101: 630mV … 7'b 111 1000: 3600mV All higher setting: Reserved

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LDO_CTRL3 (51h)

The LDO_CTRL3 command sets the LDO's soft-start delay. It does not directly control the converter.

Bits	Access	Bit Name	Default	Description
D[7:0]	R/W	LDO_POWER_ON_DELAY	8'b 0000 1000 (Or MODE-Determined)	Sets the LDO's soft-start delay via CLK pulses. 8'b 0000 0000: 0 8'b 0000 0001: 1 8'b 0000 0010: 2 8'b 0000 0011: 3 …… 8'b 0110 0100: 100 8'b 0110 0101: 102 8'b 0110 0110: 104 ……. 8'b 1001 0110: 200 8'b 1001 0111: 204 8'b 1001 1000: 208 …… 8'b 1100 1000: 400 8'b 1100 1001: 408 8'b 1100 1010: 416 …… 8'b 1110 0001: 600 8'b 1110 0010: 616 8'b 1110 0011: 632 …… 8'b 1111 1010: 1000 8'b 1111 1011: 1024 8'b 1111 1100~1111 1111: Reserved

LDO_CTRL4 (52h)

The LDO_CTRL4 command sets the LDO's soft-shutdown delay. It does not directly control the converter.

Bits	Access	Bit Name	Default	Description
D[7:0]	R/W	LDO_POWER_OFF_DELAY	8'b 0000 0000	Sets the LDO's soft-stop delay via CLK pulses. 8'b 0000 0000: 0 8'b 0000 0001: 1 8'b 0000 0010: 2 8'b 0000 0011: 3 …… 8'b 0110 0100: 100 8'b 0110 0101: 102 8'b 0110 0110: 104 ……. 8'b 1001 0110: 200 8'b 1001 0111: 204 8'b 1001 1000: 208 …… 8'b 1100 1000: 400 8'b 1100 1001: 408 8'b 1100 1010: 416 …… 8'b 1110 0001: 600 8'b 1110 0010: 616 8'b 1110 0011: 632 …… 8'b 1111 1010: 1000 8'b 1111 1011: 1024 8'b 1111 1100~1111 1111: Reserved

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SYS_CTRL1 (53h)

The SYS_CTRL1 command sets the default setting for SYS_CTRL1 (0Dh). This command does not have direct control of converter operation.

Bits	Access	Bit Name	Default	Description
D[7]	R/W	CONVERTER_EN	1'b 1	1'b 0: Buck 1, buck 2, and the LDO are all disabled 1'b 1: Buck 1, buck 2, and the LDO are all enabled (must enable each regulator)
D[6]	R/W	VOUT1_EN	1'b 1	1'b 0: Disable buck 1 1'b 1: Enable buck 1
D[5]	R/W	VOUT2_EN	1'b 1	1'b 0: Disable buck 2 1'b 1: Enable buck 2
D[4]	R/W	LDO_EN	1'b 0	1'b 0: Disable LDO 1'b 1: Enable LDO
D[3:2]	R/W	RV	2'b 00	Reserved.
D[1:0]	R/W	GPIO_CTRL	2'b 10	Sets GPIO's open-drain output control. 2'b 00: The GPIO output is low 2'b 01: GPIO is an analog input for the ADC 2'b 10: GPIO can be used for flex-time control and is used as the external converter's enable signal. GPIO outputs as an EN signal for the external converter and its on/off sequence can be configured via the 0x57 and 0x58 registers 2'b 11: The GPIO output is floating/high

SYS_CTRL2 (54h)

The SYS_CTRL2 command sets buck 1 and buck 2's operation mode. It directly controls converter operation.

Bits	Access	Bit Name	Default	Description
D[7]	R/W	SINGLE/DUAL	1'b 1 (Or MODE-Determined)	Sets whether buck 1 and buck 2 operate in single-phase, dual-output mode or dual-phase, single-output output. 1'b 0: Single-phase, dual-output 1'b 1: Dual-phase, single-output
D[6:0]	R/W	RV	0000000	Reserved.

SYS_CTRL3 (55h)

The SYS_CTRL3 command sets the default settings for SYS_CTRL3 (0Eh). This command does not have direct control of converter operation.

Bits	Access	Bit Name	Default	Description
D[7:5]	R/W	VIN_PG_VTH	3'b 110	Sets the V_{IN} rising threshold for VIN_PG. VIN_PG (0x19) is 0 (power good) even if V_{IN} < V_{IN} PG falling threshold after V_{IN} start-up. Then ramp up V_{IN} to be ≥ V_{IN} rising threshold. If V_{IN} triggers the V_{IN} PG falling threshold again, VIN_PG changes to 1 (power not good). The hysteresis = 0.5V. 3'b 000: 9.5V (same as 001) 3'b 001: 9.5V 3'b 010: 8.5V 3'b 011: 7.5V 3'b 100: 6.5V 3'b 101: 5.5V 3'b 110: 4.25V 3'b 111: Reserved

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D[4]	R/W	MASK_PG	1'b 0	Masks the PG pin's output. 1'b 0: No mask 1'b 1: Masked
D[3:1]	R/W	RV	3'b 010	Reserved.
D[0]	R/W	PROTECT_MODE	1'b 1	Sets the protection mode for the buck converters. 1'b 0: Latch-off mode 1'b 1: Hiccup mode

SYS_CTRL4 (56h)

The SYS_CTRL4 command sets the over-temperature (OT) thresholds. This command has direct control of the converter operation.

Bits	Access	Bit Name	Default	Description
D[7:5]	R/W	OT_TH	3'b 011	Sets the converter's temperature shutdown threshold. The hysteresis = 20°C. 3'b 000: 125°C 3'b 001: 135°C 3'b 010: 145°C 3'b 011: 155°C 3'b 100: 165°C 3'b 101: Reserved 3'b 110: Reserved 3'b 111: Reserved
D[4:2]	R/W	OTW_TH	3'b 101	Sets the over-temperature (OT) warning threshold. The hysteresis = 20°C. 3'b 000: Reserved 3'b 001: 100°C 3'b 010: 110°C 3'b 011: 120°C 3'b 100: 130°C 3'b 101: 140°C 3'b 110: 150°C 3'b 111: Reserved
D[1:0]	R/W	VIN_UV_SEL	2'b 00	Sets the buck V_{IN} under-voltage lockout (UVLO) rising threshold. 2'b 00: The default value in the Electrical Characteristics section starting on page x 2'b 01: 2.9V 2'b 10: 4V 2'b 11: 6V

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GPIO_CONFIG (57h)

The GPIO_CONFIG command sets the GPIO power on delay. This command has direct control of the converter operation.

Bits	Access	Bit Name	Default	Description
D[7:0]	R/W	GPIO_POWER_ON_DELAY	8’b 0001 0100 (Or MODE-Determined)	If GPIO_CTL = 10, GPIO goes high when counting the selected number of CLK pulses. 8’b 0000 0000: 0 8’b 0000 0001: 1 8’b 0000 0010: 2 8’b 0000 0011: 3 …… 8’b 0110 0100: 100 8’b 0110 0101: 102 8’b 0110 0110: 104 ……. 8’b 1001 0110: 200 8’b 1001 0111: 204 8’b 1001 1000: 208 …… 8’b 1100 1000: 400 8’b 1100 1001: 408 8’b 1100 1010: 416 …… 8’b 1110 0001: 600 8’b 1110 0010: 616 8’b 1110 0011: 632 …… 8’b 1111 1010: 1000 8’b 1111 1011: 1024 8’b 1111 1100~1111 1111: Reserved

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GPIO_CONFIG (58h)

The GPIO_CONFIG command sets the GPIO power off delay. This command has direct control of the converter operation.

Bits	Access	Bit Name	Default	Description
D[7:0]	R/W	GPIO_POWER_OFF_DELAY	8’b 0000 0000 (Or MODE-Determined)	If GPIO_CTL = 10, GPIO goes low when counting the selected number of CLK pulses. 8’b 0000 0000: 0 8’b 0000 0001: 1 8’b 0000 0010: 2 8’b 0000 0011: 3 …… 8’b 0110 0100: 100 8’b 0110 0101: 102 8’b 0110 0110: 104 ……. 8’b 1001 0110: 200 8’b 1001 0111: 204 8’b 1001 1000: 208 …… 8’b 1100 1000: 400 8’b 1100 1001: 408 8’b 1100 1010: 416 …… 8’b 1110 0001: 600 8’b 1110 0010: 616 8’b 1110 0011: 632 …… 8’b 1111 1010: 1000 8’b 1111 1011: 1024 8’b 1111 1100~1111 1111: Reserved

MASK1 (5Ah)

The MASK1 command sets the default setting for MASK1 (1Bh). This command does not have direct control of converter operation. The MASK1 command masks the INT pin’s behavior. The STATUS register still indicates each event.

Bits	Access	Bit Name	Default	Description
D[7]	R/W	VIN_PG_MSK	1’b 0	1’b 0: Do not mask 1’b 1: Mask
D[6]	R/W	VOUT1_PG_MSK	1’b 0	1’b 0: Do not mask 1’b 1: Mask
D[5]	R/W	VOUT2_PG_MSK	1’b 0	1’b 0: Do not mask 1’b 1: Mask
D[4]	R/W	LDO_PG_MSK	1’b 0	1’b 0: Do not mask 1’b 1: Mask
D[3:2]	R/W	RV	2’b 00	Reserved.
D[1]	R/W	OTW_MSK	1’b 0	1’b 0: Do not mask 1’b 1: Mask
D[0]	R/W	OT_MSK	1’b 0	1’b 0: Do not mask 1’b 1: Mask

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MASK2 (5Bh)

The MASK2 command sets the default setting for MASK2 (1Ch). This command does not have direct control of converter operation. The MASK2 command masks the INT pin's behavior. The STATUS register still indicates each event.

Bits	Access	Bit Name	Default	Description
D[7]	R/W	VIN_OV_MSK	1'b 0	1'b 0: Do not mask 1'b 1: Mask
D[6]	R/W	VIN_UV_MSK	1'b 0	1'b 0: Do not mask 1'b 1: Mask
D[5]	R/W	VOUT1_OV_MSK	1'b 0	1'b 0: Do not mask 1'b 1: Mask
D[4]	R/W	VOUT2_OV_MSK	1'b 0	1'b 0: Do not mask 1'b 1: Mask
D[3]	R/W	VOUT1_UV_MSK	1'b 0	1'b 0: Do not mask 1'b 1: Mask
D[2]	R/W	VOUT2_UV_MSK	1'b 0	1'b 0: Do not mask 1'b 1: Mask
D[1]	R/W	VOUT1_OC_MSK	1'b 0	1'b 0: Do not mask 1'b 1: Mask
D[0]	R/W	VOUT2_OC_MSK	1'b 0	1'b 0: Do not mask 1'b 1: Mask

AVP_CTRL1 (5Ch)

The AVP_CTRL1 command sets the default setting for AVP_CTRL1 (1Fh). This command does not have direct control of converter operation.

Bits	Access	Bit Name	Default	Description
D[7]	R/W	AVP1_EN	1'b 0	Enables buck 1's AVP function. 1'b 0: Disabled 1'b 1: Enabled
D[6:5]	R/W	AVP1_GAIN	2'b 00	Sets the AVP gain. 2'b 00: 3mV/A 2'b 01: 5.5mV/A 2'b 10: Reserved 2'b 11: Reserved
D[4:0]	R/W	AVP1_OFFSET	5'b 0000 1	Sets the DC offset voltage for the output voltage command value when AVP is enabled. This offset ranges between -30mV and +30mV. 2mV/step. 5'b x 0000: 0mV 5'b 0 0001: 2mV … 5'b 0 1111: 30mV 5'b 1 0001: -2mV … 5'b 1 1111: -30mV

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AVP_CTRL1 (5Dh)

The AVP_CTRL1 command sets the default setting for AVP_CTRL2 (20h). This command does not have direct control of converter operation.

Bits	Access	Bit Name	Default	Description
D[7]	R/W	AVP2_EN	1'b 0	Enables buck 2's AVP function. 1'b 0: Disabled 1'b 1: Enabled
D[6:5]	R/W	AVP2_GAIN	2'b 00	Sets the AVP gain. 2'b 00: 3mV/A 2'b 01: 5.5mV/A 2'b 10: Reserved 2'b 11: Reserved
D[4:0]	R/W	AVP2_OFFSET	5'b 0000 1	Sets the DC offset voltage for the output voltage command value when AVP is enabled. This offset ranges between -30mV and +30mV. 2mV/step. 5'b x 0000: 0mV 5'b 0 0001: 2mV … 5'b 0 1111: 30mV 5'b 1 0001: -2mV … 5'b 1 1111: -30mV

CLK_CTRL1 (5Eh)

The CLK_CTRL1 command sets the master/slave configuration, CLK pin's frequency, and maximum clock output number. This command has direct control over converter operation.

Bits	Access	Bit Name	Default	Description
D[7]	R/W	CLK_MODE	1'b 1 (Or MODE-Determined)	Sets the master/slave configuration for the power sequence. 1'b 0: Slave converter 1'b 1: Master converter
D[6:4]	RW	CLK_FREQUENCY	3'b 011	Configures the CLK pin's clock frequency. 3'b 000: 100Hz 3'b 001: 200Hz 3'b 010: 500Hz 3'b 011: 1kHz 3'b 100: 2kHz 3'b 101: 5kHz 3'b 110: 10kHz 111: 20kHz

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D[3:1]	RW	CLK_NUMBER	3'b 100	Configures the CLK pin's maximum clock output number. If the PG pin is pulled up, and the maximum POWER_ON_DELAY or maximum POWER_ON_DELAY CLK number of the enabled power rails is below CLK_NUMBER, CLK outputs CLK_NUMBER clocks when EN is turning on/off. If the on/off delay CLK number exceeds CLK_NUMBER, CLK continues outputting clocks until the on/off sequence is complete. If the PG pin is floating or below 2.3V, CLK does not stop outputting clocks until EN turns off or V_{IN} < UVLO threshold. Enable/disable the power channel via the I²C; CLK stays high. 3'b 000: 8 3'b 001: 16 3'b 010: 32 3'b 011: 64 3'b 100: 128 3'b 101: 256 3'b 110: 512 3'b 111: 1024
D[0]	R/W	RV	1'b 0	Reserved.

CLK_CTRL2 (5Fh)

The CLK_CTRL2 command selects the CLK clock's output pausing feature. It has direct control over converter operation.

Bits	Access	Bit Name	Default	Description
D[7:3]	R/W	RV	5'b 0000 0	Reserved.
D[2]	RW	CLK_PAUSE_EN	1'b 1	Enables the pausing feature of the CLK clock's output. 1'b 0: Disabled. The converter does not pull the CLK pin low during soft start/soft shutdown 1'b 1: Enabled. The converter pulls the CLK pin low during soft start/shutdown
D[1]	RW	CLK_ON_ERROR_ PAUSE_EN	1'b 1	Enables the pausing feature if an error occurs during soft start. 1'b 0: Disabled. The converter does not pull the CLK pin low if an error occurs during soft start 1'b 1: Enabled. The converter pulls the CLK pin low if an error occurs during soft start
D[0]	R/W	RV	1'b 0	Reserved.

I2C_CONFIG (60h)

The I2C_CONFIG command enables MODE control and sets the I²C address. It has direct control over converter operation.

Bits	Access	Bit Name	Default	Description
D[7]	R/W	MODE_EN	1'b 1	Enables MODE control. 0: MODE is disabled. The MODE-determined MTP registers keep the original value as the default value 1: MODE is enabled. The MODE-determined MTP registers load the default value based on MODE selection
D[6:0]	R/W	I2C_ADDRESS	7'b 100 0000	Sets the I²C 7-bit address.

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MTP_CTRL1 (61h)

The MTP_CTRL1 command writes the MTP password.

Bits	Access	Bit Name	Default	Description
D[7:0]	WO	MTP_PASSWORD	-	Sets the password for MTP configuration.

MTP_CTRL2 (62h)

The MTP_CTRL2 command controls MTP configurations.

Bits	Access	Bit Name	Default	Description
D[7:2]	R/W	RV	6’b 0000 00	Reserved.
D[1]	R/W	MTP_RESTORE	1’b 0	Controls MTP restoration. Write “1” to this bit to restore all registers values to the MTP registers’ values.
D[0]	R/W	MTP_PROGRAM	1’b 0	Controls MTP programming. Write “1” to this bit to start MTP programming.

ID2 (64h)

The ID2 command sets the MTP suffix code. It does not control converter operation.

Bits	Access	Bit Name	Default	Description
D[7:0]	R/W	MTP_CODE	8’b 0000 0000	Sets the MTP suffix code. MPS defines this register.

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MODE REGION REGISTERS

When MODE_EN = 1, some of the MTP region registers load their default values from the MODE region registers, depending on the MODE pin's resistance.

For the following register settings, their configurations are copied from the corresponding registers in 0x70~0xC7. There are 8 sets of configuration settings listed in MODE0–MODE7 for each of the following bits (see Table 6). The MODE resistor determines which mode is selected (MODEx).

Table 6: Registers Selected According to MODE0~MODE7

Command Code (0x)	Command Name	Tape	D7	D6	D5	D4	D3	D2	D1	D0
41	BUCK1_ CTRL1	R/W	-	VOUT1_SOFT_START			-		-	
42	BUCK1_ CTRL2	R/W	-	-	BUCK1_FSW		-	VOUT1_SETTING_LOW		
43	BUCK1_ CTRL3	R/W	VOUT1_SETTING_HIGH							
44	BUCK1_ CTRL4	R/W	-	-	BUCK1_ FB_ HALF	-	-	-	-	-
45	BUCK1_ CTRL5	R/W	BUCK1_POWER_ON_DELAY							
48	BUCK2_ CTRL1	R/W	-	VOUT2_SOFT_START			-		-	
49	BUCK2_ CTRL2	R/W	-	-	BUCK2_FSW		-	VOUT2_SETTING_LOW		
4A	BUCK2_ CTRL3	R/W	VOUT2_SETTING_HIGH							
4B	BUCK2_ CTRL4	R/W	-		BUCK2_ FB_ HALF	-	-	-	-	-
4C	BUCK2_ CTRL5	R/W	BUCK2_POWER_ON_DELAY							
4F	LDO_ CTRL1	R/W		LDO_SOFT_START			-		-	-
50	LDO_ CTRL2	R/W	-	LDO_SETTING						
51	LDO_ CTRL3	R/W	LDO_POWER_ON_DELAY							
53	SYS_ CTRL1	R/W	-	-	-	LDO_ EN	-	-	GPIO_CTRL	
54	SYS_ CTRL3	R/W	SINGLE/ DUAL	-		-	-		-	
57	GPIO_ CONFIG	R/W	GPIO_POWER_ON_DELAY							
5E	CLK_ CTRL1	R/W	CLK_ MODE	-			-			-
60	I2C_ CONFIG	R/W	-	I2C_ADDRESS						

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MODE REGION REGISTER DESCRIPTION (13)

Bit Name	Description
MODEx_VOUT1_SETTING	Sets the default value for VOUT1_SETTING_HIGH (BUCK1_CTRL3 (43h), bits D[7:0]) and VOUT1_SETTING_LOW (BUCK1_CTRL2 (42h), bits D[2:0]).
MODEx_VOUT2_SETTING	Sets the default value for VOUT2_SETTING_HIGH (BUCK2_CTRL3 (4Ah), bits D[7:0]) and VOUT2_SETTING_LOW (BUCK2_CTRL2 (49h), bits D[2:0]).
MODEx_BUCK1_FB_HALF	Sets the default value for BUCK1_FB_HALF (BUCK1_CTRL4 (44h), bit D[5]).
MODEx_BUCK2_FB_HALF	Sets the default value for BUCK2_FB_HALF (BUCK2_CTRL4 (4Bh), bit D[5]).
MODEx_BUCK1_FSW	Sets the default value for BUCK1_FSW (BUCK1_CTRL2 (42h), bits D[5:4]).
MODEx_BUCK2_FSW	Sets the default value for BUCK2_FSW (BUCK2_CTRL2 (49h), bits D[5:4]).
MODEx_CLK_MODE	Sets the default value for CLK_MODE (CLK_CTRL1 (5Eh), bit D[7]).
MODEx_SINGLE/DUAL	Sets the default value for SINGLE/DUAL (SYS_CTRL2 (54h), bit D[7]).
MODEx_BUCK1_POWER_ON_DELAY	Sets the default value for BUCK1_POWER_ON_DELAY (BUCK1_CTRL5 (45h), bits D[7:0]).
MODEx_BUCK2_POWER_ON_DELAY	Sets the default value for BUCK2_POWER_ON_DELAY (BUCK2_CTRL5 (4Ch), bits D[7:0]).
MODEx_VOUT1_SOFT_START_TIME	Sets the default value for VOUT1_SOFT_START (BUCK1_CTRL1 (41h), bits D[6:4]).
MODEx_VOUT2_SOFT_START_TIME	Sets the default value for VOUT2_SOFT_START (BUCK2_CTRL1 (48h), bits D[6:4]).
MODEx_LDO_EN	Sets the default value for LDO_EN (SYS_CTRL1 (53h), bit D[4]).
MODEx_LDO_SOFT_START_TIME	Sets the default value for LDO_SOFT_START (LDO_CTRL1 (4Fh), bits D[6:4]).
MODEx_I2C_ADDRESS	Sets the default value for the last three digits of I2C_ADDRESS (I2C_CONFIG (60h), bits D[2:0]).
MODEx_GPIO_CTRL	Sets the default value for GPIO_CTRL (SYS_CTRL1 (53h), bits D[1:0]).
MODEx_LDO_SETTING	Sets the default value for LDO_SETTING (LDO_CTRL2 (50h), bits D[6:0]).
MODEx_LDO_POWER_ON_DELAY	Sets the default value for LDO_POWER_ON_DELAY (LDO_CTRL3 (51h), bits D[7:0]).
MODEx_GPIO_POWER_ON_DELAY	Sets the default value for GPIO_POWER_ON_DELAY (GPIO_CONFIG (57h), bits D[7:0]).

Note:

13) MODEx represents MODE0–MODE7.

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MODE-DETERMINED MTP DEFAULT VALUES

MODE0, MODE resistor = 0Ω. Read the MODEx region's register default values from the MP5472GR-0000 via the I²C.

Bit Name	Command Code	Bits	Default Code	Default Value	Range/Values	Min Value	Max Value	Resolution/ LSB	Unit
MODE0_ VOUT1_ SETTING	0x70, 0x72	D[7:0], D[5:3]	011001 00, 000	800	300mV to 2047mV (BUCK1_FB_HALF = 0) or 300mV to 3800mV (BUCK1_FB_HALF = 1)	300	2047/ 3800	1 (BUCK1_FB_HALF = 0) / 2 (BUCK1_FB_HALF = 1)	mV
MODE0_ VOUT2_ SETTING	0x71, 0x72	D[7:0], D[2:0]	011001 00, 000	800	300mV to 2047mV (BUCK1_FB_HALF = 0) or 300mV to 3800mV (BUCK1_FB_HALF = 1)	300	2047/ 3800	1 (BUCK2_FB_HALF = 0) / 2(BUCK2_FB_HALF = 1)	mV
MODE0_ BUCK1_ FB_HALF	0x72	D[7]	0	FB voltage	FB voltage, 1/2 FB voltage	-	-	-	-
MODE0_ BUCK2_ FB_HALF	0x72	D[6]	0	FB voltage	FB voltage, 1/2 FB voltage	-	-	-	-
MODE0_ BUCK1_ FSW	0x73	D[3:2]	10	1000	500 to 1250	500	1250	250	kHz
MODE0_ BUCK2_ FSW	0x73	D[1:0]	10	1000	500 to 1250	500	1250	250	kHz
RESERVED	0x73	D[5:4]	00	N/A	-	-	-	-	-
MODE0_ CLK_ MODE	0x73	D[7]	1	Master converter	Slave converter, Master converter	-	-	-	-
MODE0_ SINGLE/ DUAL	0x73	D[6]	1	Dual-phase, single-output	Single-phase, dual-output; dual-phase, single-output	-	-	-	-
MODE0_ BUCK1_ POWER_ ON_ DELAY	0x74	D[7:0]	000011 00	Soft start when counting 12 CLK pulses	0 to 1024	0	1024	1/2/4/8/16/24	-
MODE0_ BUCK2_ POWER_ ON_ DELAY	0x75	D[7:0]	000011 00	Soft start when counting 12 CLK pulses	0 to 1024	0	1024	1/2/4/8/16/24	-
MODE0_ VOUT1_ SOFT_ START_ TIME	0x76	D[7:5]	001	2	1, 2, 4, 6, 8, 10, 12, 14	1	14	-	ms
MODE0_ VOUT2_ SOFT_ START_ TIME	0x76	D[4:2]	001	2	1, 2, 4, 6, 8, 10, 12, 14	1	14	-	ms

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MODE-DETERMINED MTP DEFAULT VALUES *(continued)*

MODE0, MODE resistor = 0Ω. Read the MODEx region's register default values from the MP5472GR-0000 via the I²C.

Bit Name	Command Code	Bits	Default Code	Default Value	Range/Values	Min Value	Max Value	Resolution/ LSB	Unit
MODE0_ LDO_EN	0x76	D[1]	0	LDO disabled	LDO enabled	-	-	-	-
RESERVED	0x76	D[0]	0	N/A	-	-	-	-	-
MODE0_ LDO_ SOFT_ START_ TIME	0x77	D[7:5]	001	2	1, 2, 4, 6, 8, 10, 12, 14	1	14	-	ms
MODE0_ I2C_ ADDRESS	0x77	D[4:2]	000	000	0 to 7	000	111	-	-
MODE0_ GPIO_ CTRL	0x77	D[1:0]	10	GPIO is part of flex-time control and used as the external converter's enable signal	The GPIO output is low; reserved; GPIO is part of flex-time control and used as the external converter's enable signal; GPIO output is floating/high	-	-	-	-
MODE0_ LDO_ SETTING	0x78	D[7:0]	00111100	1800	600 (001 0100) to 3600 (001 0101)	600	3600	30	mV
MODE0_ LDO_ POWER_ ON_ DELAY	0x79	D[7:0]	00001000	Soft start when counting 8 CLK pulses	0 to 1024	0	1024	1/2/4/8/16/24	-
MODE0_ GPIO_ POWER_ ON_ DELAY	0x7A	D[7:0]	00010100	Soft start when counting 20 CLK pulses	0 to 1024	0	1024	1/2/4/8/16/24	-

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APPLICATION INFORMATION

Selecting the Inductor

MPL Optimized Performance with MPS Inductor MPL-4020 Series

Use an inductor with a DC current rating at least 25% percent higher than the maximum load current for most applications. For the highest efficiency, use an inductor with a DC resistance below 15mΩ. For most designs, the inductance can be estimated with Equation (2):

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}} \quad (2)$$

Where ΔI_L is the inductor ripple current.

Choose the inductor ripple current to be approximately 30% of the maximum load current. The maximum inductor peak current can be calculated with Equation (3):

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2} \quad (3)$$

Use a larger-value inductor to improve efficiency under light-load conditions below 100mA.

MPS inductors are optimized and tested for use with our complete line of integrated circuits.

Table 7 lists our power inductor recommendations. Select a part number based on your design requirements.

Table 7: Power Inductor Selection

Part Number	Inductor Value	Manufacturer
Select family series (MPL-AY, MPL-AT, MPL-AL, MPL-SE)	0.47µH to 2.2µH	MPS
MPL-AL4020-R47	0.47µH	MPS
MPL-AL5030-2R2	2.2µH	MPS

Visit MonolithicPower.com under Products > Inductors for more information.

Selecting the Input Capacitor

The step-down converter has a discontinuous input current, and requires a capacitor to supply the AC current to the converter while maintaining the DC input voltage. Use low-ESR capacitors for the best performance. For the best results, use ceramic capacitors with X5R or X7R dielectrics due to their low ESR and small temperature coefficients. For most applications, use a 22µF capacitor.

Since C1 absorbs the input switching current, it requires an adequate ripple current rating. The input capacitor's RMS current can be estimated with Equation (4):

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (4)$$

The worst-case condition occurs at $V_{IN} = 2 \times V_{OUT}$, calculated with Equation (5):

$$I_{C1} = \frac{I_{LOAD}}{2} \quad (5)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, add a small, high-quality ceramic capacitor (e.g. 0.1µF) placed as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide sufficient charge to prevent excessive voltage ripple at input. The input voltage ripple caused by the capacitance can be estimated with Equation (6):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_{SW} \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (6)$$

Selecting the Step-Down Converter's Output Capacitor

The step-down converter's output capacitor maintains the DC output voltage. Use ceramic, tantalum, or low-ESR electrolytic capacitors. For the best results, use low-ESR capacitors to keep the output voltage ripple low.

The output voltage ripple can be estimated with Equation (7):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_{SW} \times C2}\right) \quad (7)$$

Where L_1 is the inductor value and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

For ceramic capacitors, the capacitance dominates the impedance at the switching

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frequency and causes the majority of the output voltage ripple. For simplification, the output voltage ripple can be calculated with Equation (8):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^{2} \times L_1 \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (8)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output voltage ripple can be estimated with Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (9)$$

The characteristics of the output capacitor also affect the regulation stability.

PCB Layout Guidelines

The PCB layout is vital for stable operation. For the best results, refer to Figure 23 and follow the guidelines below:

1. Connect the input ground to the GND pin using the shortest and widest trace possible.
2. Connect the input capacitor to the VIN pin using the shortest and widest trace possible.
3. Ensure that all feedback connections are short and direct. Place the feedback resistors and compensation components as close to the chip as possible.
4. Route SW away from sensitive analog areas, such as FB.
5. Put VCC and LDO decoupling capacitors close to the VCC, LDO, and AGND pins.
6. Air flow is necessary for MP5472 heat dissipation. Keep open space around the MP5472's surface.

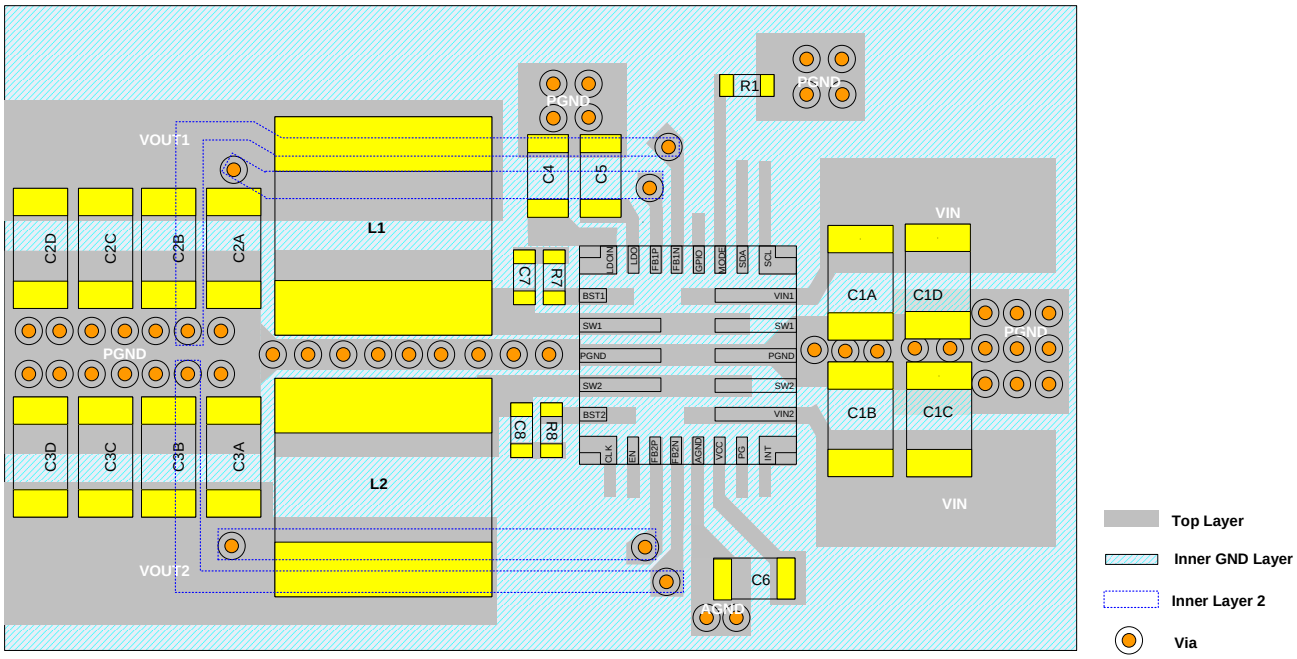

Figure 23: Recommended PCB Layout

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TYPICAL APPLICATION CIRCUITS

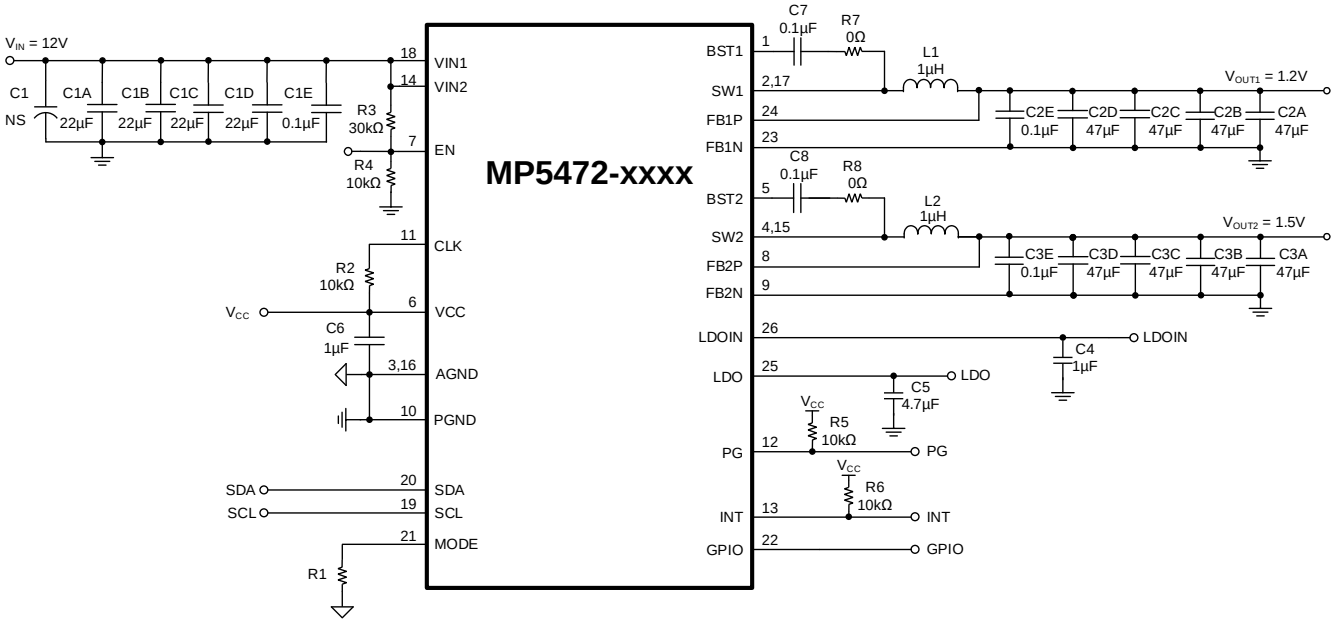

Figure 24: Typical Application Circuit (V_{IN} = 12V, V_{OUT1} = 1.2V/6A, V_{OUT2} = 1.5V/6A, Single-Phase, Dual-Output Mode)

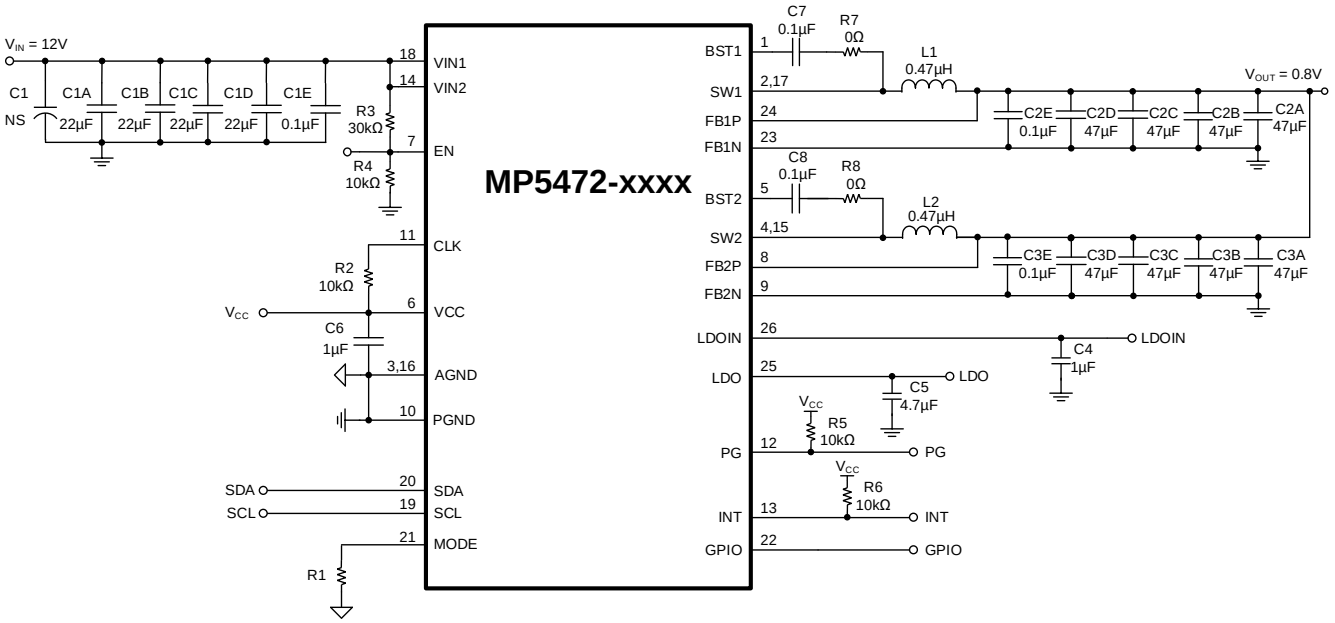

Figure 25: Typical Application Circuit (V_{IN} = 12V, V_{OUT} = 0.8V/12A, Dual-Phase, Single-Output Mode)

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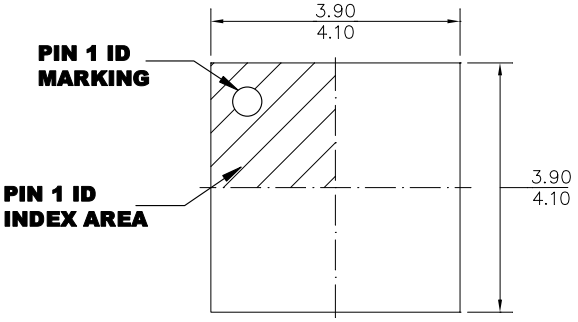
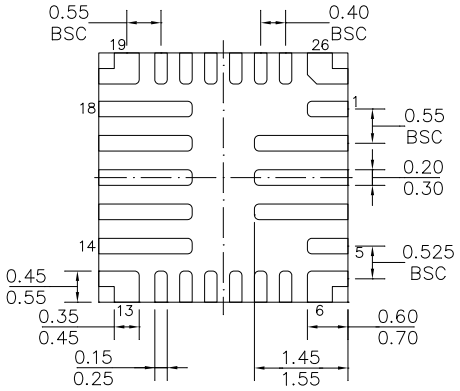
PACKAGE INFORMATION

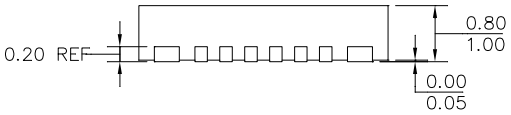
QFN-26 (4mmx4mm)



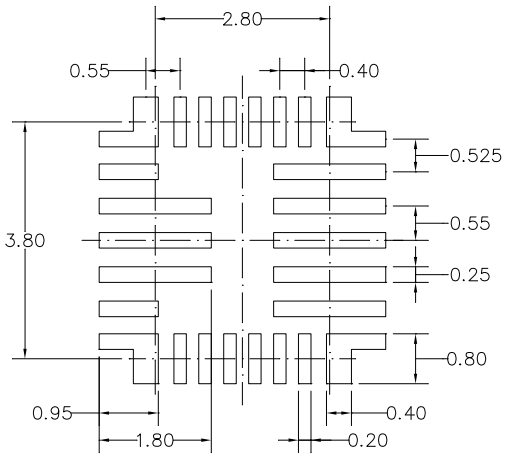
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-220.
4) DRAWING IS NOT TO SCALE.

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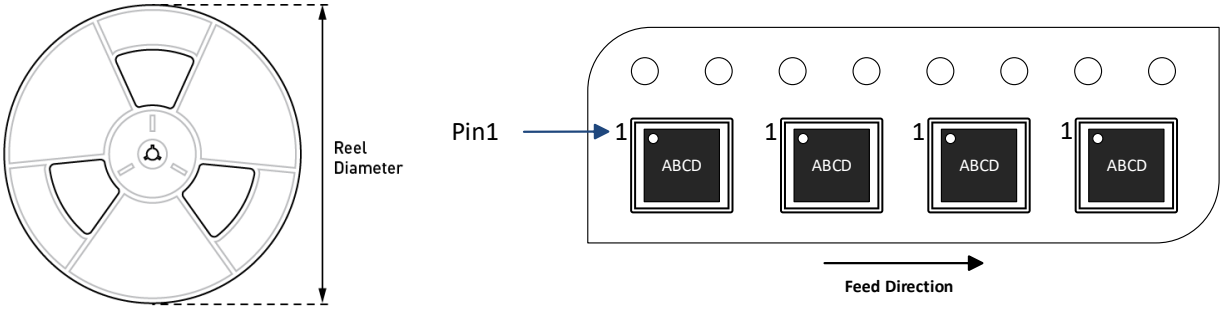
CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP5472GR-xxxx-Z	QFN-26 (4mmx4mm)	5000	N/A	N/A	13in	12mm	8mm

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REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	12/19/2024	Initial Release	-

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