MP5030

USB Charging Port Controller with Current Limit Switch, Supporting Type-C 5V and QC 3.0 Modes

The Future of Analog IC Technology

DESCRIPTION

The MP5030 integrates a USB current-limit switch and charging port identification circuit. The MP5030 achieves 3A of continuous output current over a wide input supply range.

The output of the USB switch is current-limit programmable. The MP5030 supports DCP schemes for battery charging specification (BC1.2), divider mode, 1.2V/1.2V mode, and quick charge specification (QC 3.0) without the need for external user interaction. The MP5030 also supports Type-C 5V @ 3A DFP mode.

The MP5030 provides linear line drop compensation.

Full protection features include hiccup current limiting, input over-voltage protection (OVP), and thermal shutdown.

The MP5030 requires a minimal number of readily available, standard, external components to complete the USB switch and charging mode auto-detection solution. The MP5030 is available in a QFN-10 (1.5mmx2mm) package.

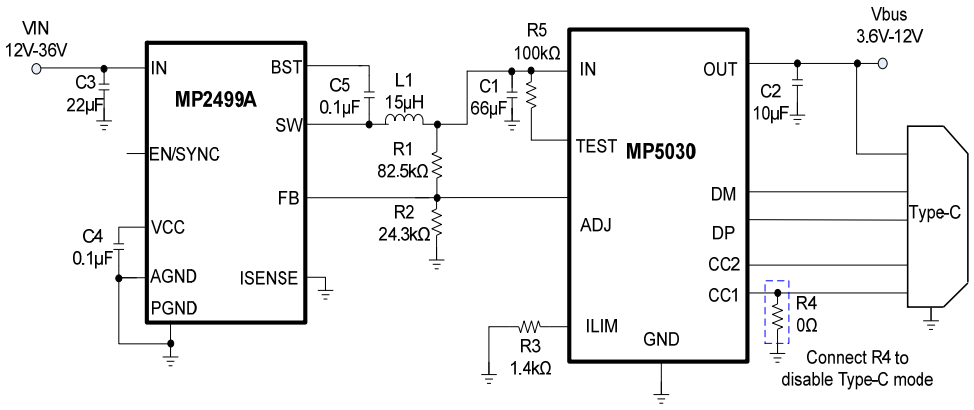
FEATURES

- Wide 3.6V to 14V Operating Input Voltage Range
- Supports QC 3.0 (3.6V - 12V_{OUT}) and DCP Schemes for BC 1.2, Divider Mode, 1.2V/1.2V Mode
- Supports Type-C 5V @ 3A DFP Mode
- Line Drop Compensation for 5V Output
- Programmable High-Accuracy Current Limit
- 32mΩ Low $R_{DS(ON)}$ Power MOSFET
- Input Discharge during High Voltage to Low Voltage Change
- Input Over-Voltage Shutdown Protection
- ±8kV HBM ESD Rating for USB DP/DM pins
- Compatible with Buck, Boost, and AC/DC Converters
- Available in a QFN-10 (1.5mmx2mm) Package

APPLICATIONS

- USB Power Supplies
- AC/DC Wall Adapters with USB Ports
- Automotive Cigarette Lighter Adapters
- Power Banks

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking
MP5030GQH	QFN-10 (1.5mmx2mm)	*See Below*

* For Tape & Reel, add suffix –Z (e.g. MP5030GQH–Z)

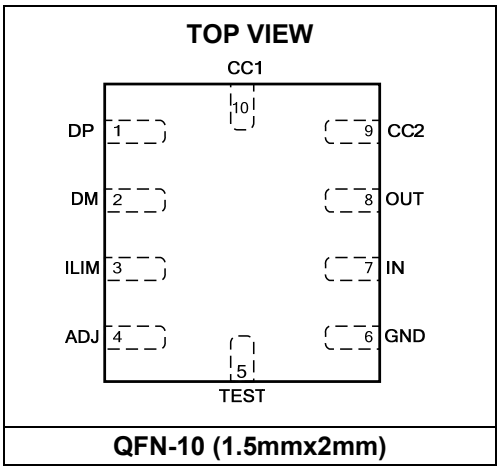
TOP MARKING

FE

LL

FE: Product code of MP5030GQH
LL: Lot number

PACKAGE REFERENCE



QFN-10 (1.5mmx2mm)

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}) ..... -0.3V to +16V
Output voltage (V_{OUT}) ..... -0.3V to +16V
All other pins ..... -0.3V to +6V
Junction temperature ..... 150°C
Lead temperature ..... 260°C
Continuous power dissipation (T_A = +25°C) (2) (5)
..... 2.23W

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) ..... 3.6V to 14V (4)
Output voltage (V_{OUT}) ..... follow with V_{IN}
Output current (I_{OUT}) ..... up to 3A
Operating junction temp. (T_J) ....-40°C to +125°C

Thermal Resistance	θ_{JA}	θ_{JC}	
QFN-10 (1.5mmx2mm)			
EV5030-QH-00C (5)	56	18	°C/W
JESD51-7 (6)	130	25	°C/W

NOTES:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) For lower V_{IN} applications, refer to the Operation section on page 10.
5) Measured on EV5030-QH-00C, 2-layer PCB, 58mmx32mm, 2Oz copper.
6) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 5V, T_J = -40°C to 125°C [7], typical value is tested at T_J = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
V_{IN} under-voltage lockout rising threshold	V_{IN_UVLO1}	ADJ starts to work	2.7	3.0	3.3	V
UVLO hysteresis	$V_{UVLOHYS1}$			880		mV
Second V_{IN} under-voltage lockout rising threshold	V_{IN_UVLO2}	Power MOSFET turn-on	3.7	3.9	4.1	V
Second UVLO hysteresis	$V_{UVLOHYS2}$			500		mV
Start-up delay	tdelay	From UVLO rising to V_{OUT} = 100mV	2	3	4	ms
Supply current	I_Q	V_{IN} = 5V, not including CC1/CC2 pull-up current		220	300	µA
USB Power MOSFET						
On resistance	R_{DSON}	V_{IN} = 5V, I_{OUT} = 0.5A, T_J = 25°C		32	40	mΩ
		V_{IN} = 5V, I_{OUT} = 0.5A, T_J = -40°C to 125°C		32	55	
Input discharge resistance	R_{DIS}	V_{IN_OVP} = 6V		72	105	Ω
Soft-start time	T_{SS}	V_{IN} = 5V, no load, V_{OUT} from 10% to 90%		290		µs
Current Limit Set						
USB current limit	I_{LIMIT}	R_{ILIM} = 1.4kΩ, V_{IN} = 5V, V_{OUT} starts to drop	3.13	3.35	3.57	A
Output Voltage Control						
Default V_{IN}	V_{IN_Def1}	I_{OUT} = 0A, T_J = 25°C	5.09	5.15	5.21	V
	V_{IN_Def2}	I_{OUT} = 0A, T_J = -40°C to 125°C	5.05	5.15	5.25	
9V_{IN} voltage	V_{IN_9}		8.82	9	9.18	V
12V_{IN} voltage	V_{IN_12}		11.76	12	12.24	V
V_{ADJ} sink current capability	I_{sink}	V_{FB} = 800mV	500			µA
Line drop compensation	$V_{IN\_5\_C}$	I_{OUT} = 2.4A, only 5V_{IN} active		150	200	mV
Protection						
V_{IN} OVP threshold	V_{OV_TH}	V_{IN} rising edge, V_{IN} = 5V	110	115	120	%
		V_{IN} rising edge, V_{IN} = 9V	110	115	120	
		V_{IN} rising edge, V_{IN} = 12V	110	115	120	
V_{IN} OVP recovery threshold	$V_{OV\_Recovery}$	Reset mode to 5V default	5.4	5.55	5.7	V
OVP deglitch time [8]	T_{OVP_DE}			10		µs
OCP on time of hiccup	T_{HIC_ON}	V_{OUT} < 3.5V		2		ms
OCP off time of hiccup	T_{HIC_OFF}			2		s
Shutdown temperature [8]	T_{STD}			150		°C
Hysteresis [8]	T_{HYS}			25		°C
BC 1.2 DCP Mode						
DP/DM short resistance	R_{DP/DM_Short}	V_{DP} = 0.8V, I_{DM} = 1mA			50	Ω
1.2V/1.2V Mode						
DP/DM output voltage	$V_{DP/DM\_1.2V}$		1.1	1.2	1.3	V
DP/DM output impedance	$R_{DP/DM\_1.2V}$		200	300	400	kΩ

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, T_J = -40°C to 125°C (7), typical value is tested at T_J = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Divider Mode						
DP/DM output voltage	$V_{DP/DM}$	V_{IN} = V_{OUT} = 5V	2.5	2.7	2.85	V
DP/DM output impendence	$R_{DP/DM}$		18	22	28	kΩ
Quick Charge 3.0 Mode						
Data detect voltage	V_{DAT_REF}		0.25	0.3	0.4	V
Output voltage select reference	V_{SEL_REF}		1.8	2.0	2.2	V
DP output impendence	R_{DP_QC}		250	350	450	kΩ
DM output impendence	R_{DM_QC}		15	20	25	kΩ
DM low glitch time (8)	T_{Glitch_DM}			10		ms
DP high glitch time	T_{Glitch_DP}		1000		1500	ms
Output voltage change glitch time	$T_{Glitch\_V\_Change}$		20	40	60	ms
Bus voltage step	$V_{BUS\_CONT\_STEP}$		150	200	250	mV
Time for V_{BUS} to discharge to 5V when DP < 0.6V (8)	T_{V_UNPLUG}				500	ms
USB Type-C 5V/3A Mode - CC1 and CC2						
CC1 voltage threshold to disable Type-C mode	V_{Rdis}	Pull CC1 to ground can enable V_{OUT} without $T_{CC\_debounce}$			20	mV
CC voltage to enable VCONN	V_{Ra}				0.75	V
CC voltage to enable V_{BUS}	V_{Rd}	Use 0.8V and 2.6V as threshold	0.85		2.45	V
CC detach threshold	V_{OPEN}	Use 2.6V as threshold	2.75			V
CC voltage at 5.1kΩ Rd	V_{CC_Rd}	CC pin pulled down by 5.1kΩ	1.31		2.04	V
CC voltage falling de-bounce timer	$T_{CC\_debounce}$	V_{BUS} enable deglitch	100	150	200	ms
CC voltage rising de-bounce timer	$T_{PD\_debounce}$	V_{BUS} disable deglitch	10	15	20	ms
VCONN output power	P_{VCONN}	VCONN comes from the MP5030 input with some series resistance	1			W

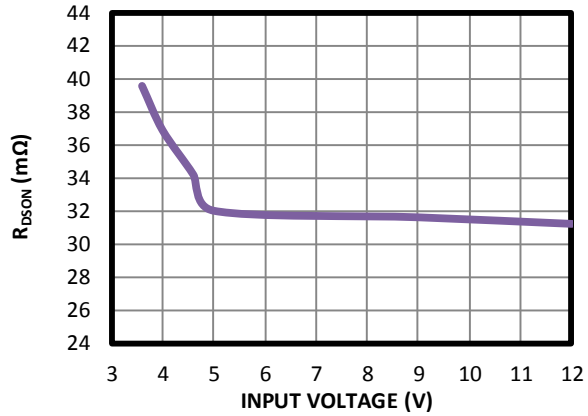
NOTES:

7) Guaranteed by over-temperature correlation, not tested in production.
8) Guaranteed by engineering sample characterization.

TYPICAL CHARACTERISTICS

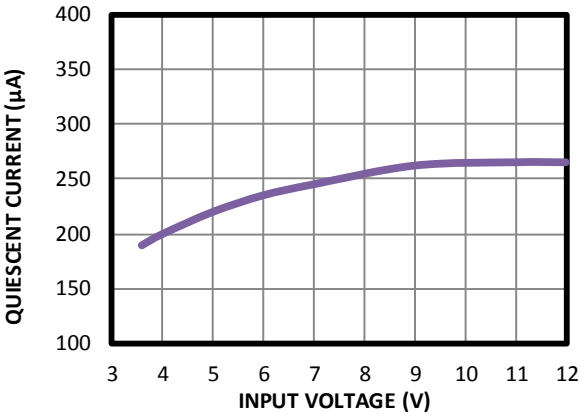
V_{IN} = 5V, V_{OUT} = 5V, R_{ILIM} = 1.4kΩ, T_A = 25°C, CC1 pulled down by 5.1kΩ resistor to ground, unless otherwise noted.

$R_{DS(ON)}$ vs. Input Voltage



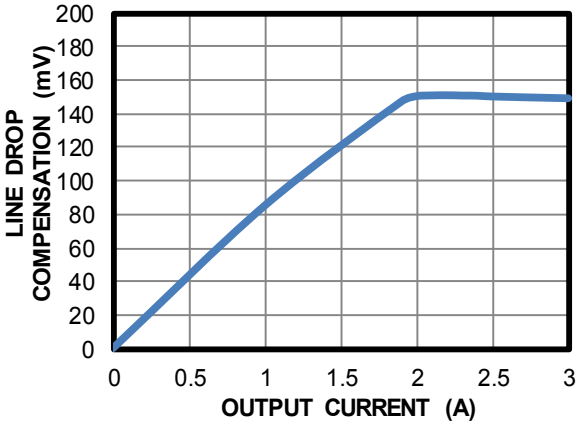
Quiescent Current vs. Input Voltage

V_{IN} = 5V, not including CC1/CC2 pull-up current

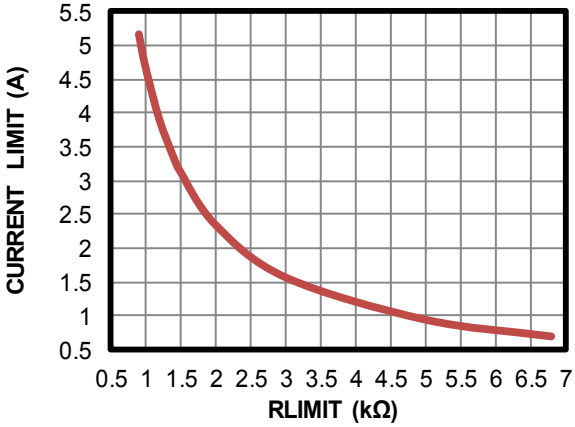


Line Drop Compensation

V_{IN} = 5V Only



Current Limit vs. R_{LIMIT}

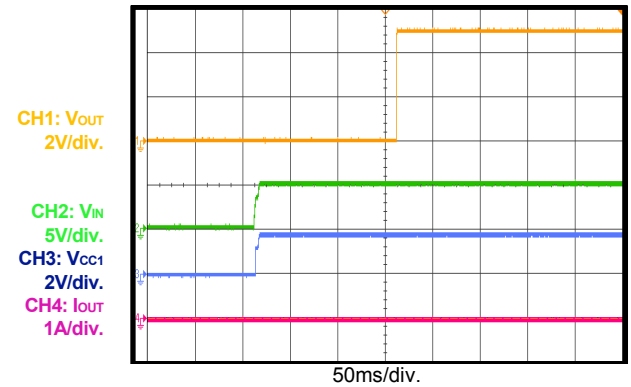


TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 5V, V_{OUT} = 5V, R_{ILIM} = 1.4kΩ, T_A = 25°C, CC1 pulled down by 5.1kΩ resistor to ground, unless otherwise noted.

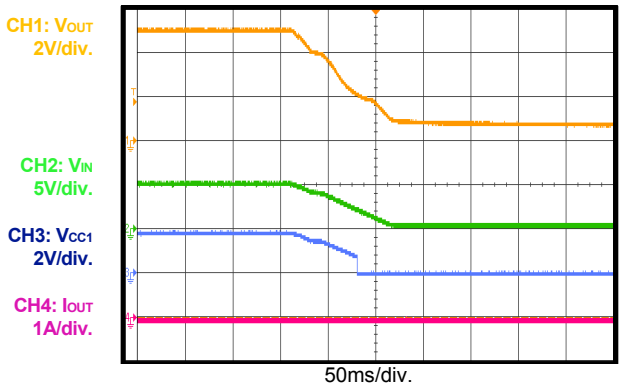
Start-Up through VIN

I_{OUT} = 0A



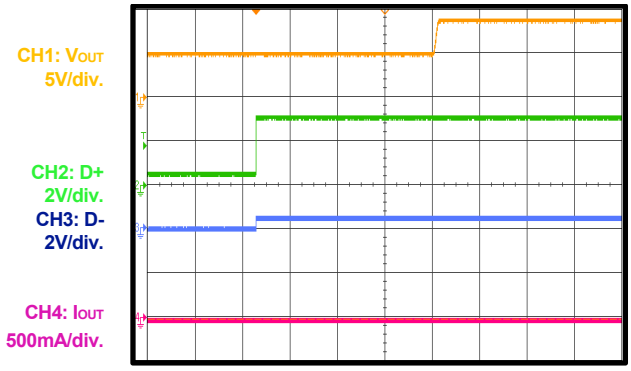
Shutdown through VIN

I_{OUT} = 0A



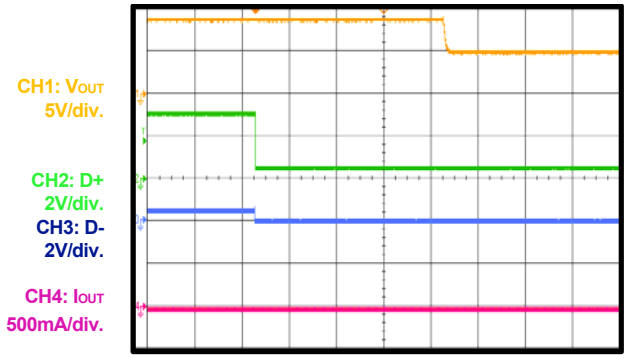
Mode Transition from 5V to 9V

I_{OUT} = 0A, from QC 2.0_5V to 9V



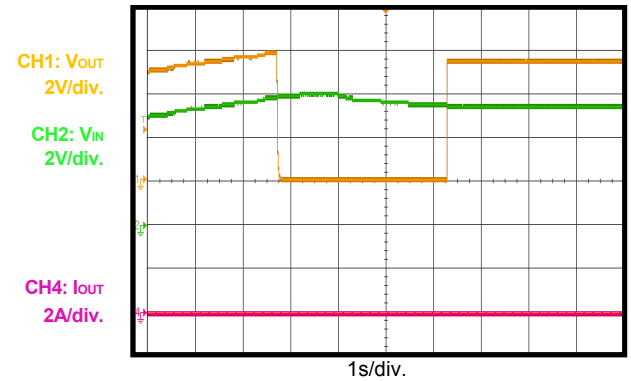
Mode Transition from 9V to 5V

I_{OUT} = 0A, from QC 2.0_9V to 5V



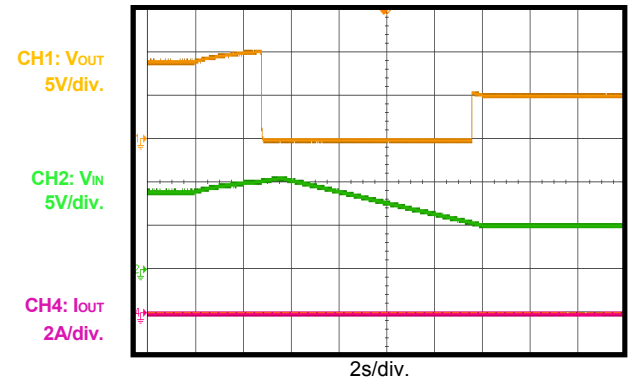
Input Over-Voltage Protection

QC 5V Mode, I_{OUT} = 0A



Input Over-Voltage Protection

QC 9V Mode, I_{OUT} = 0A

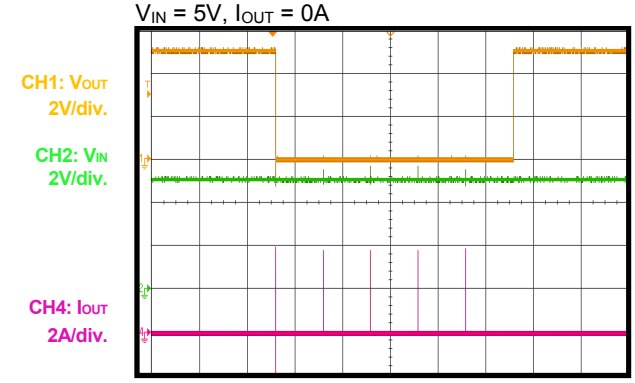


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 5V, R_{ILIM} = 1.4kΩ, T_A = 25°C, CC1 pulled down by 5.1kΩ resistor to ground, unless otherwise noted.

Short-Circuit Protection Entry and Recovery

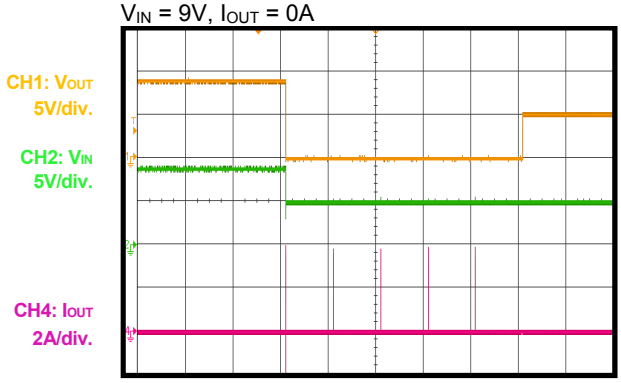
V_{IN} = 5V, I_{OUT} = 0A



2s/div.

Short-Circuit Protection Entry and Recovery

V_{IN} = 9V, I_{OUT} = 0A



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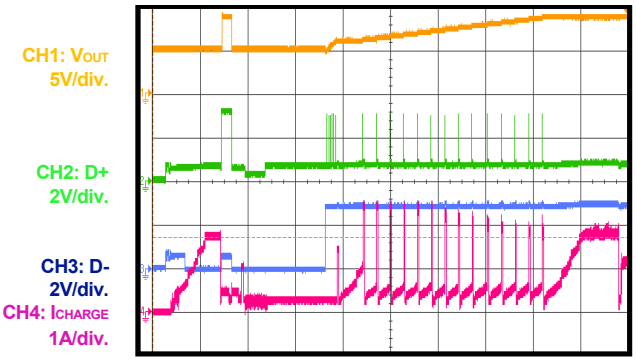
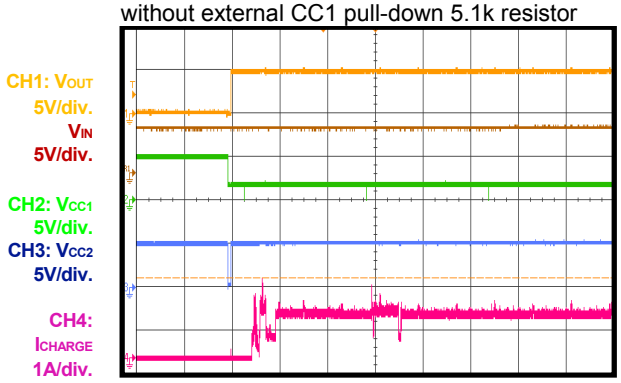
QC 3.0 Device Charging Test



2s/div.

Type-C Mode Test

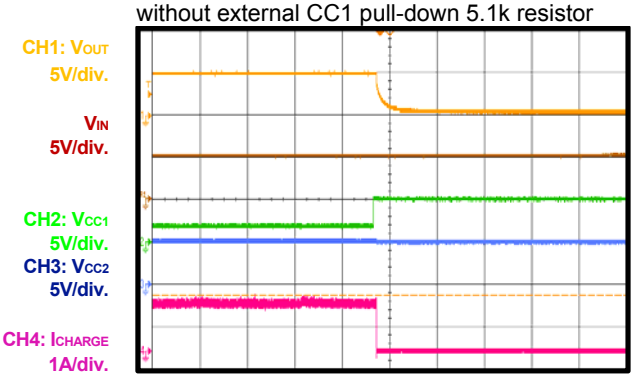
Type-C phone plug in,
without external CC1 pull-down 5.1k resistor



500ms/div.

Type-C Mode Test

Type-C phone plug out,
without external CC1 pull-down 5.1k resistor



200ms/div.

PIN FUNCTIONS

Package Pin #	Name	Description
1	DP	**D+ data line to USB connector.** DP is the input/output used for handshaking with portable devices.
2	DM	**D- data line to USB connector.** DM is the input/output used for handshaking with portable devices.
3	ILIM	**Set the current limit level.** Place a resistor between ILIM and GND to achieve a high-accuracy current limit.
4	ADJ	**Output voltage adjustment.** ADJ sinks a current from the upstream DC/DC converter's FB pin to ground to regulate the DC/DC converter's output voltage. ADJ also supports line drop compensation.
5	TEST	**Test pin.** Connect TEST to IN through a 100kΩ resistor. Do not float TEST.
6	GND	**Ground.**
7	IN	**Supply voltage.**
8	OUT	**Output of USB current limit switch.**
9	CC2	**Configuration channel.** CC1 and CC2 are used to detect connections and configure the interface across the USB Type-C cables and connectors. Once a connection is established, CC1 or CC2 is reassigned to provide power over the VCONN pin of the plug.
10	CC1	

BLOCK DIAGRAM

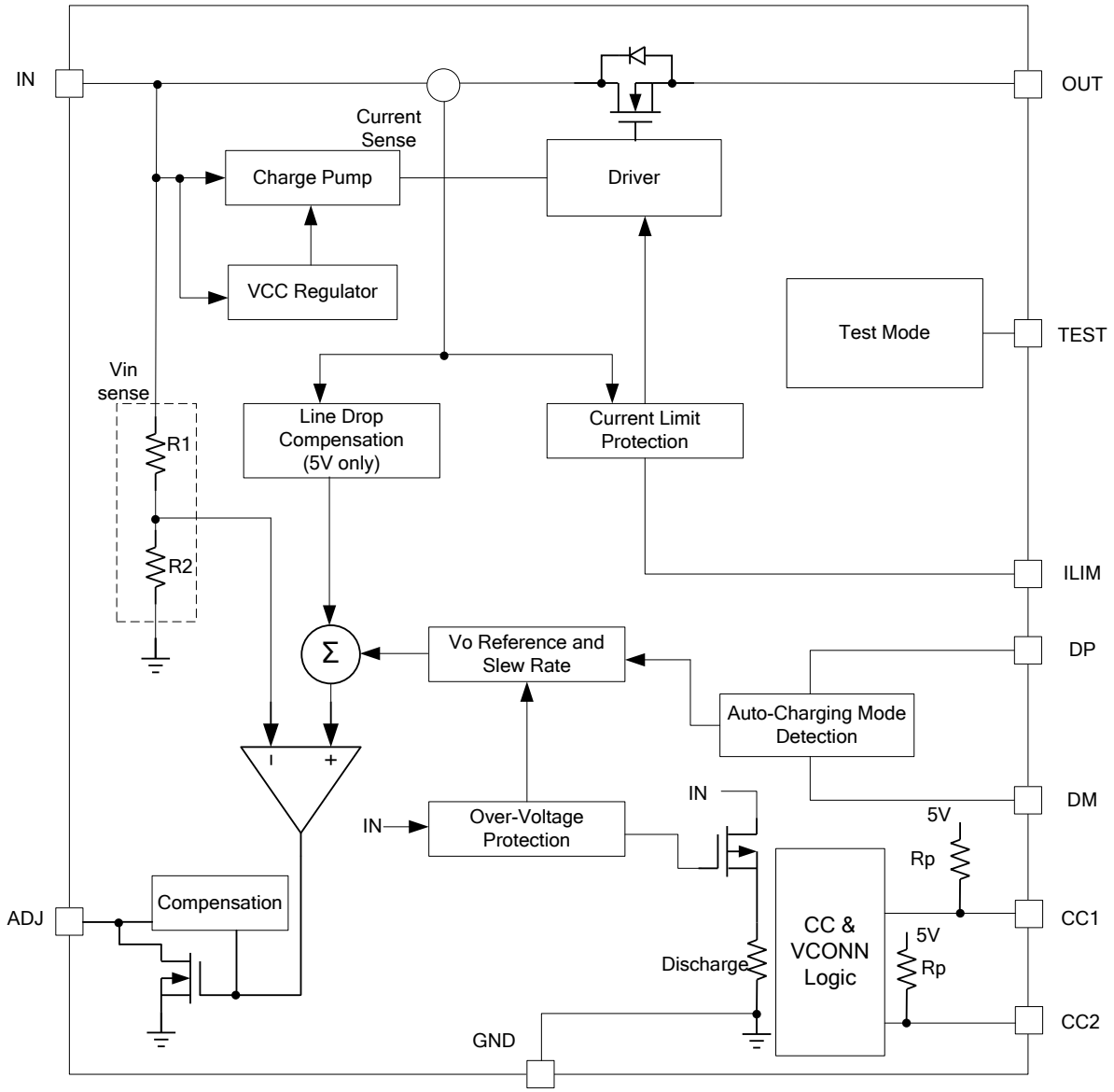


Figure 1: Functional Block Diagram

OPERATION

The MP5030 integrates a USB current-limit switch and charging port identification circuit. The MP5030 achieves 3A of continuous output current over a wide input supply range.

The output of the USB switch is current-limited with an adjustable current-limit threshold. The MP5030 supports the latest quick charge specification (QC 3.0) and is backwards-compatible with QC 2.0. The MP5030 also supports DCP schemes for battery charging specification (BC1.2), divider mode, and 1.2V/1.2V mode without the need for external user interaction.

The MP5030 also supports Type-C 5V @ 3A DFP mode. For Type-C applications, either CC1 or CC2 is pulled low by a 5.1kΩ resistor (Rd), and then V_{BUS} is enabled. For non-Type-C applications, short CC1 to ground, and V_{BUS} starts up directly after a 3ms delay.

The MP5030 provides line drop compensation for a 5V output. Fault condition protection includes hiccup current limiting, input over-voltage protection (OVP), and thermal shutdown.

Operation Supply Voltage

The MP5030 has a two-stage input voltage threshold. The first threshold is around 3V, and the second threshold is the under-voltage lockout (UVLO) of the power MOSFET. When V_{IN} is higher than the first threshold, the MP5030's ADJ block starts working and sinks a current to adjust the upstream regulator's output to an accurate 5.15V. Afterward, the MP5030 enters a fully working state.

Under Voltage Lockout (UVLO)

UVLO protects the chip from operating at an insufficient supply voltage. The MP5030's second UVLO comparator monitors the input voltage. Once the input voltage is higher than the second UVLO threshold, the power MOSFET starts to turn on with a controlled slew rate after a fixed delay.

Internal Soft Start (SS)

The internal soft-start prevents the output voltage from inrush current and overshooting during start-up.

QC Mode Voltage Transition - Class A

If the downstream device of the MP5030 supports the QC specification, the MP5030 can require an output voltage higher than 5V by DM and DP communication. If a higher USB bus voltage is required, ADJ must be used. ADJ is usually connected to the feedback pin of the upstream voltage converter. After the handshake, the MP5030 sinks a controlled current by ADJ gradually to adjust V_{OUT} to 9V/12V or another voltage 200mV step-by-step. Because of smart controller mode, only one ADJ pin can set to a different high voltage that meets QC specification. The output voltage transition is smooth and has no undershoot or overshoot (see Figure 2 and Table 1).

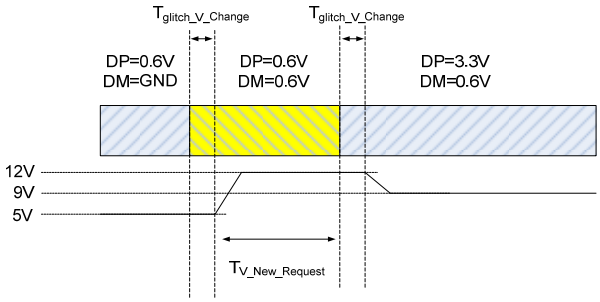


Figure 2: QC Mode Transition

Table 1: QC Mode Definition

Portable Device		USB Bus Voltage
DP	DM	
0.6V	0.6V	12V
3.3V	0.6V	9V
0.6V	3.3V	3.6V - 12V/200mV step according to QC 3.0
3.3V	3.3V	No action
0.6V	GND	5V

When downstream device is removed, the output voltage returns to the default 5V automatically. The input-to-ground discharge resistor helps expedite this procedure.

Line Drop Compensation

The MP5030 is capable of compensating for an output voltage drop, such as high impedance caused by a long trace, to maintain a fairly constant 5V load-side voltage. The line drop compensation is only active at 5V V_{IN} while it is disabled under QC 3.0 mode. Line drop compensation is achieved through ADJ. The MP5030 increases the input voltage by 150mV

at a 2.4A output current (see Figure 3).

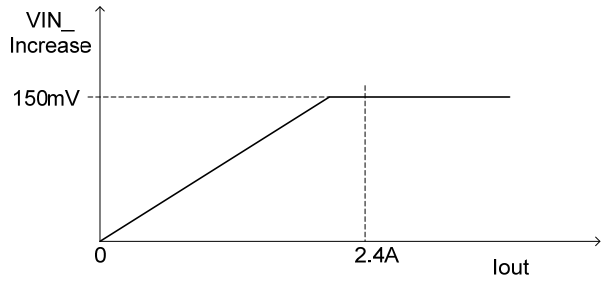


Figure 3: Line Drop Compensation

The ADJ voltage (V_{ADJ}) slowly sinks a controlled current. The line drop compensation amplitude increases linearly as the load current increases.

At no-load condition, if the input voltage is lower than the typical 5.15V, ADJ sinks a current to regulate the upstream regulator's output voltage to 5.15V. If the input voltage is higher than 5.15V, the MP5030 no longer regulates the input voltage.

Figure 4 shows the typical ADJ usage. The ADJ sink current capability is 500μA. The feedback current through R1 must be less than 500μA. Calculate R1 with Equation (1):

$$R1(k\Omega) > \frac{V_{OUT}(V) - V_{FB}(V)}{0.5} \quad (1)$$

Where V_{OUT} is the maximum output voltage that can be adjusted to.

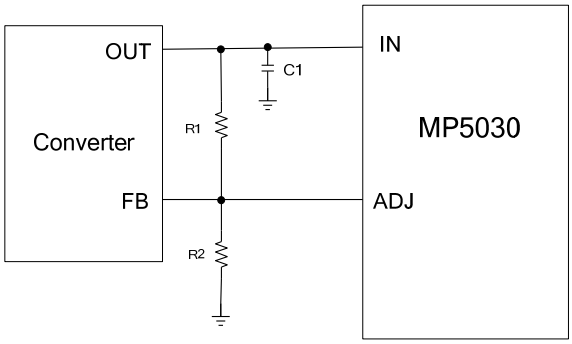


Figure 4: ADJ Configuration

Input Over-Voltage and Discharge

To protect the downstream device from an over-voltage condition, the MP5030 provides an input over-voltage protection (OVP) shutdown function. Since the MP5030 supports QC 3.0 protocol, it has a dynamic OVP threshold.

An accurate and fast comparator monitors the over-voltage condition of the input. If the input voltage rises above the threshold, the gate of the internal MOSFET is pulled low quickly, and the power MOSFET is shut down. Simultaneously, the input-to-ground discharge path is active. When the input voltage falls below the typical 5.55V, the MP5030 exits OVP mode.

The OVP shutdown function is blanked during the high-to-low voltage mode change period.

The input-to-ground discharge resistance is always active during the high-to-low voltage change mode period. The discharge path is turned off when FB is lower than 108% * V_{REF} (OV disappears) with 20ms of additional delay (see Figure 5).

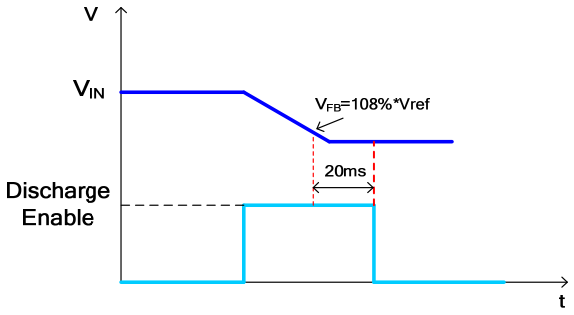


Figure 5: Input Discharge during High Voltage to Low Voltage Transition

QC mode is reset during the OVP rising edge.

Over-Current Protection (OCP)

The MP5030 provides a constant current limit. The current limit threshold is adjustable by an external resistor.

The current-limit threshold can be calculated with Equation (2):

$$I_{LIMIT}(A) = \frac{4.69\,V}{R_{LIMIT}(k\Omega)} \quad (2)$$

Once the device reaches its current limit threshold, the internal circuit regulates the gate voltage to hold the current in the power MOSFET constant.

If the over-current (OC) is triggered, and V_{OUT} < 3.5V lasts for 2ms, the MP5030 enters hiccup mode. If OC occurs but V_{OUT} is greater than 3.5V, the MP5030 works in constant current (CC) limit mode without hiccup. In this case, V_{OUT} drops while the output current increases slowly (see Figure 6).

In hiccup mode, the MP5030 turns off the power MOSFET. The hiccup signal resets QC mode to 5V. ADJ starts to change V_{IN} to 5V. Two seconds (hiccup off-timer) later, the MP5030 restarts to check the OC state. If the OC still remains, the MP5030 follows the previous operation. If the OC has been removed, the MP5030 recovers to normal operation in 5V mode.

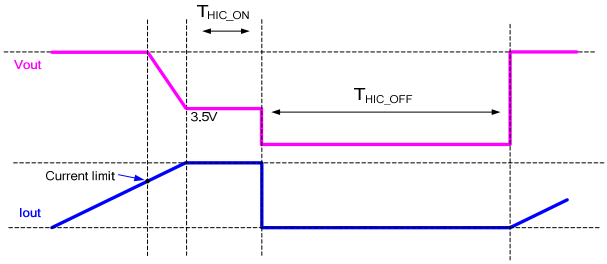


Figure 6: Over-Current Protection

Short-Circuit Protection (SCP)

If the load current increases rapidly due to a short circuit, the current may exceed the current-limit threshold greatly before the control loop can respond. If the current reaches an internal secondary current-limit level (about 6A), a fast turn-off circuit activates to turn off the power MOSFET. This limits the peak current through the switch to limit the input voltage drop. The fast-off response time typical value is 700ns. If the fast-off works, the power MOSFET remains off for 80μs. Afterward, the power MOSFET turns on again. If the part is still in a short-circuit condition, the MP5030 treats this as an over-current condition to enter hiccup mode or thermal shutdown. After the short-circuit condition is removed, the MP5030 recovers automatically.

Auto Detection

The MP5030 integrates a USB dedicated charging port auto-detect function, which recognizes most mainstream portable devices. It supports the following charging schemes:

- USB Battery Charging Specification BC1.2/ Chinese Telecommunications Industry Standard YD/T 1591-2009
- Divider mode
- 1.2V/1.2V mode
- Qualcomm quick charge mode 3.0 and 2.0
- Type-C 5V @ 3A DFP mode

USB Type-C Mode and VCONN

For USB Type-C solutions, two pins on the connector, CC1 and CC2, are used to establish and manage the source-to-sink connection. The general concept for setting up a valid connection between a source and sink is based on being able to detect terminations residing in the product being attached. To aid in defining the functional behavior of CC, a pull-up (Rp) and pull-down (Rd 5.1kΩ) termination model is used based on a pull-up resistor and pull-down resistor (see Figure 7).

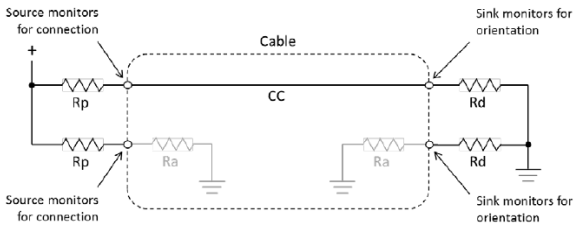


Figure 7: Current Source/Pull-Down CC Model

Initially, a source exposes independent Rp terminations on its CC1 and CC2 pins, and a sink exposes independent Rd terminations on its CC1 and CC2 pins. The source-to-sink combination of this circuit configuration represents a valid connection. To detect this, the source monitors CC1 and CC2 for a voltage lower than its unterminated voltage. The choice of Rp is a function of the pull-up termination voltage and the source's detection circuit. This indicates that either a sink, a powered cable, or a sink connected via a powered cable has been attached.

Prior to the application of VCONN, a powered cable exposes Ra (typically 1kΩ) on its VCONN pin. Ra represents the load on VCONN plus any resistive elements to ground. In some cable plugs, this might be a pure resistance, and in others, it may be simply the load.

The source must be able to differentiate between the presence of Rd and Ra to determine whether there is a sink attached and where to apply VCONN. The source is not required to source VCONN unless Ra is detected.

The Rp value of the MP5030 is 10kΩ, typically, which indicates that this is a 3A source port.

One special termination combination on the CC pins as seen by a source is defined for directly attached accessory mode: two Ra resistors pull down CC1 and CC2 for audio adapter accessory mode. In this case, the MP5030's V_{OUT} is disabled.

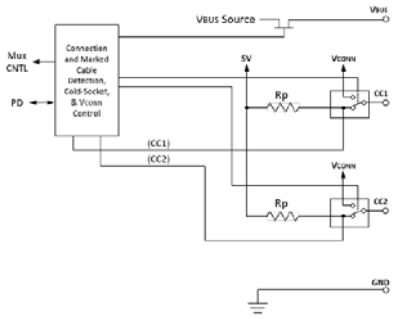


Figure 8: CC Pin Functional Block

A port that behaves as a source has the following functional characteristics:

1. The source uses a MOSFET to enable or disable power delivery across the V_{BUS}. Initially, the source has been disabled.
2. The source supplies pull-up resistors (Rp) on CC1 and CC2 and monitors both to detect a sink. The presence of an Rd pull-down resistor on either pin indicates that a sink is being attached.
3. The source uses the CC pin pull-down characteristic to detect and determine which CC pin is intended for supplying VCONN (when Ra is discovered).
4. Once a sink is detected, the source enables V_{BUS} and VCONN.
5. The source monitors the continued presence of Rd to detect a sink detachment. When a detach event is detected, the source is removed, the output is discharged by a 1kΩ resistor for 100ms, and the discharge path is disabled. Meanwhile, V_{BUS} and VCONN return to step 2.

Disable Type-C Mode, Direct VOUT Startup

If the CC1 voltage falls below 20mV, the MP5030 V_{OUT} starts up directly after a 3ms delay. Type-C mode is disabled, which means the CC attach and detach logic is disabled and V_{OUT} is always enabled.

To trigger this mode, it is recommended to short CC1 to ground.

Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the silicon die temperature exceeds 150°C, the entire chip shuts down. When the temperature falls below its lower threshold (typically 125°C), the chip is enabled again.

APPLICATION INFORMATION

Selecting the Input Capacitor

Use low ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. A 22µF ceramic capacitor is recommended for most applications.

The input capacitor must also consider pre-stage converter stability. The input capacitor of the MP5030 is the output capacitor of the converter. Ensure that the converter is stable with an additional output capacitor.

Selecting the Output Capacitor

Use low ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. A 10µF ceramic capacitor is recommended for most applications.

Selecting the ILIM Resistor

The current limit value can be set by the ILIM resistor. The programmable current limit can be calculated with Equation (2). The current limit threshold should be 10% higher than the maximum load current. For example, if the system's full load is 3A, set the current limit to 3.35A.

Selecting the V_{ADJ} Resistor

ADJ has a controlled current sink internally. Through ADJ, the line drop compensation and QC mode transition is achieved. The ADJ sink current capability is 500µA. It is recommended that the pre-side converter use a kΩ level feedback resistor. The current through the high-side feedback resistor should be less than 500µA. There is another V_{ADJ} configuration to limit the maximum output voltage (i.e.: to insert R5 between FB and ADJ). With R5, the maximum output voltage can be limited with Equation (3):

$$V_{OUT\_MAX}(V) = \frac{R_1 + R_2 // R_5}{R_2 // R_5} \times V_{FB}(V) \quad (3)$$

The required feedback resistor of R1 must be greater than 30kΩ (see Figure 9).

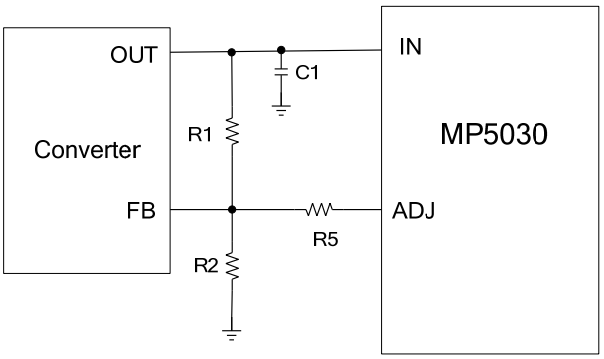


Figure 9: V_{ADJ}-Set Maximum V_{OUT}

Other Considerations

The upstream DC/DC converter must have a current-limit threshold higher than the MP5030's current limit.

ESD Protection for I/O Pins

Higher ESD levels should be considered for all USB I/O pins. The MP5030 features high ESD protection up to ±8kV human body model on DP, DM, and OUT, and ±6kV human body model on CC1 and CC2. The ESD structures can withstand high ESD both in normal operation and when the device is powered off. To further extend DP and DM's ESD level for covering complicated application environments, additional resistors and capacitors can be used (see Figure 10).

Similar R-C networks cannot be added on CC1 or CC2 since the CC line must be able to support 200mA of current and 300kHz of signaling. Additional ESD diodes can be added on the CC pins.

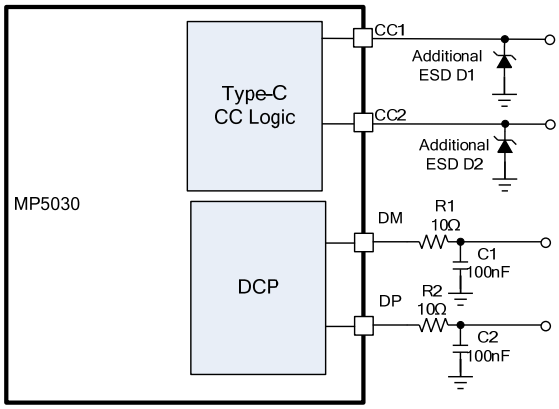


Figure 10: Recommended I/O Pins for ESD Enhancing

PCB Layout Guidelines

Efficient PCB layout is critical for stable operation and thermal dissipation. For best results, refer to Figure 11 and follow the guidelines below.

1. Use short, direct, and wide traces to connect the IC's IN/OUT pins.
2. Keep the ADJ trace to upstream converter's FB pin need as short as possible.
3. Route the trace as far from the switching node as possible to avoid noise injection.

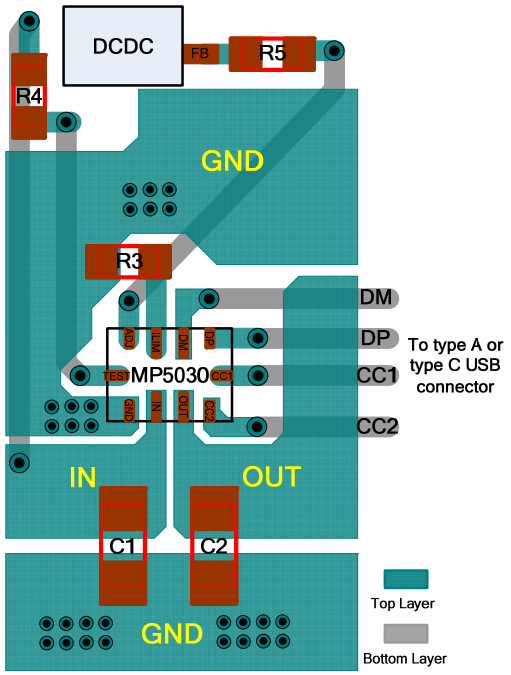


Figure 11: Recommended Layout

Design Example

Table 2 is a design example following the application guidelines for the given specifications:

Table 2: Design Example

V_{IN} (V)	3.6 - 12
Current Limit (A)	3.35

The detailed application schematic is shown in Figure 12 and Figure 13. The typical performance and circuit waveforms are shown in the Typical Performance Characteristics section. For more detailed device applications, please refer to the related evaluation board datasheet.

TYPICAL APPLICATION CIRCUITS

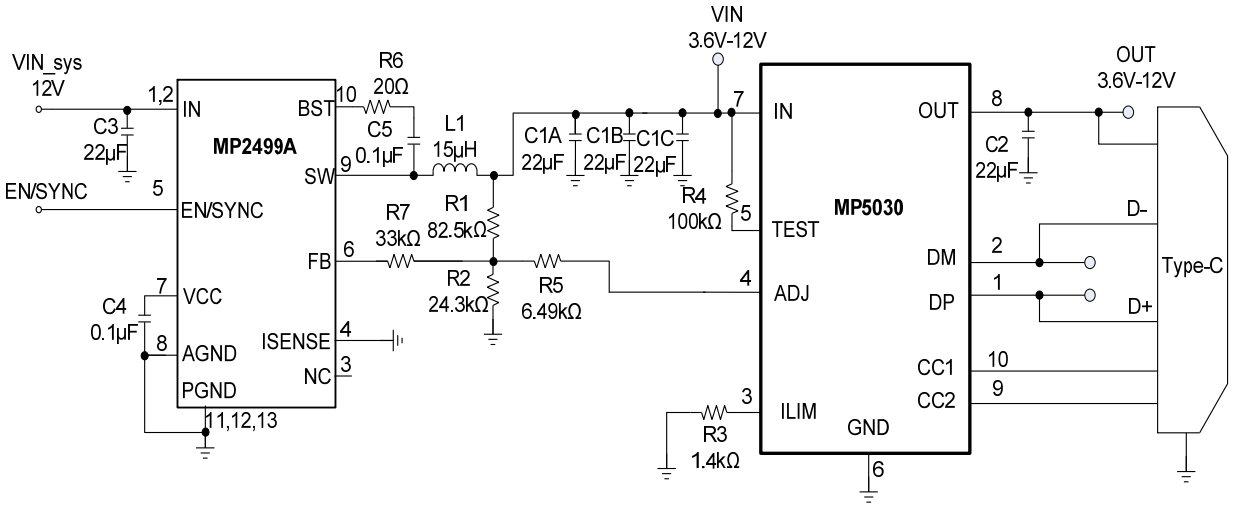


Figure 12: MP5030 + MP2499A for CLA Car Charger, Type-C Port w/ QC 3.0

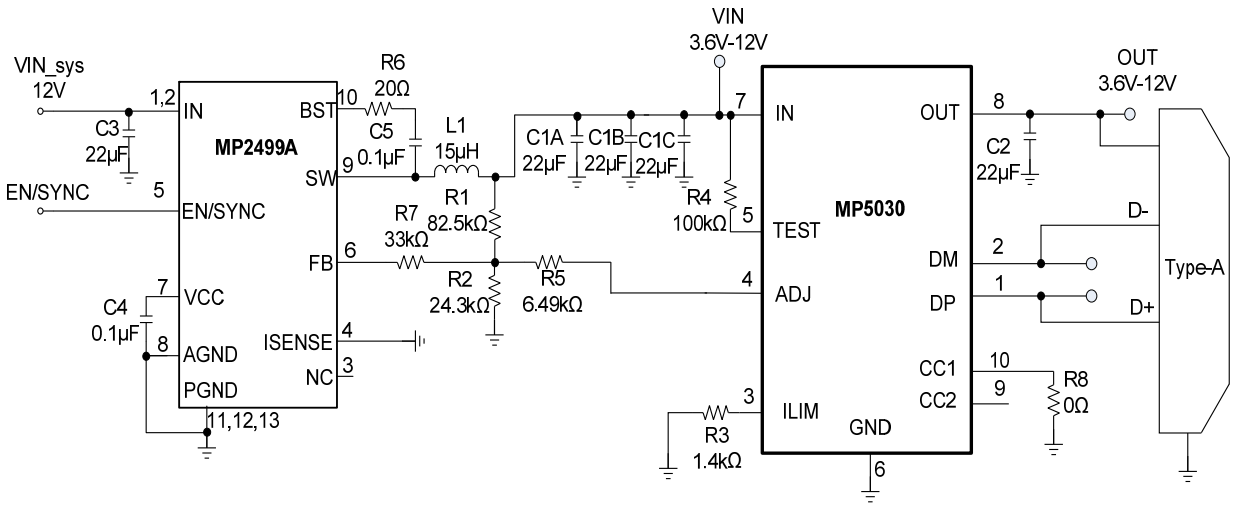
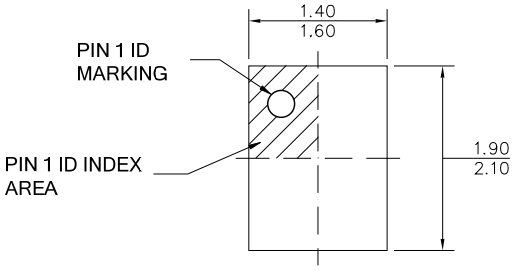


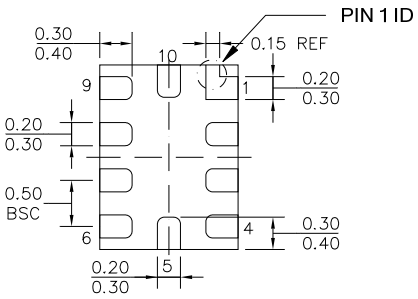
Figure 13: MP5030 + MP2499A for CLA Car Charger, Type-A Port w/ QC 3.0

PACKAGE INFORMATION

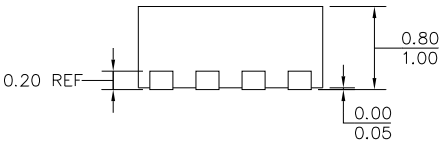
QFN-10(1.5mmx2mm)



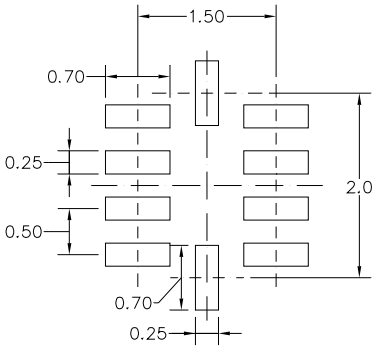
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-220.
4) DRAWING IS NOT TO SCALE.