

## DESCRIPTION

The MP2143H is a monolithic, step-down, switch-mode converter with internal power MOSFETs. It can achieve up to 3A continuous output current from a 2.5V to 5.5V input voltage with excellent load and line regulation. The output voltage can be regulated as low as 0.6V.

Constant-on-time control provides fast transient response and eases loop stabilization. Fault-condition protections include cycle-by-cycle current limiting and thermal shutdown.

The MP2143H is available in small QFN-10 package and requires only a minimal number of readily-available standard external components.

The MP2143H is ideal for a wide range of applications including high-performance DSPs, FPGAs, and portable instruments.

## FEATURES

- Wide 2.5V to 5.5V Operating Input Range
- Output Voltage as Low as 0.6V
- 100% Duty Cycle in Dropout
- Up to 3A Output Current
- 80mΩ and 40mΩ Internal Power MOSFET Switches
- Default 2.0MHz Switching Frequency
- EN and Power-Good for Power Sequencing
- Cycle-by-Cycle Over-Current Protection
- Auto Discharge at Power Off
- Short-Circuit Protect with Hiccup Mode
- Stable with Low-ESR Output Ceramic Capacitors
- Available in QFN-10 (2mmx3mm) Package

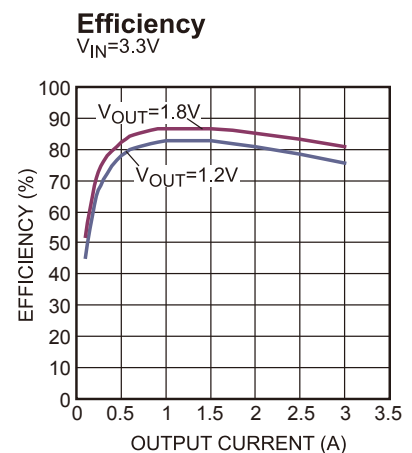
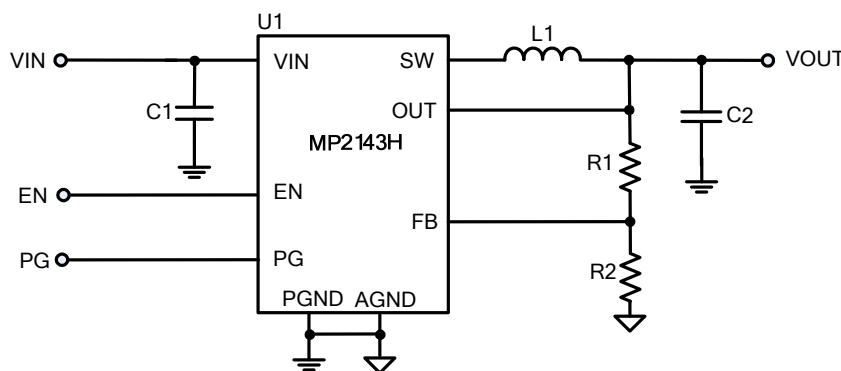
## APPLICATIONS

- Low Voltage I/O System Power
- Handheld/Battery-powered Systems
- Wireless/Networking Cards

All MPS parts are lead-free, halogen-free, and adhere to the RoHS directive. For MPS green status, please visit the MPS website under Quality Assurance.

"MPS" and "The Future of Analog IC Technology" are registered trademarks of Monolithic Power Systems, Inc.

## TYPICAL APPLICATION



### ORDERING INFORMATION

Part Number*	Package	Top Marking
MP2143HGD	QFN-10(2mmx3mm)	See Below

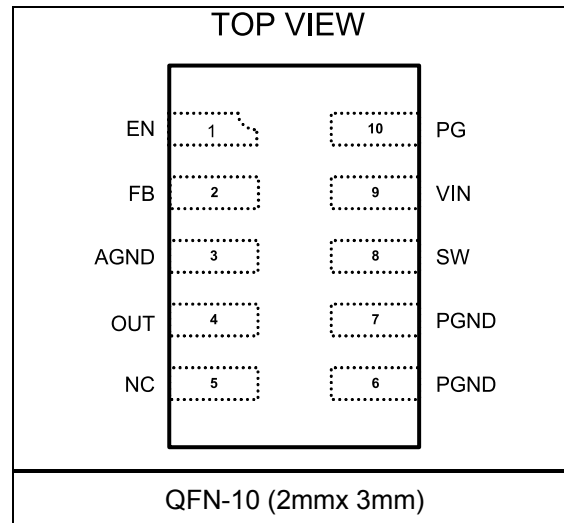
\* For Tape & Reel, add suffix –Z (e.g. MP2143HGD–Z).

### TOP MARKING

—  
**AMT**  
**YWW**  
**LLL**

AMT: product code of MP2143HGD;  
 Y: year code;  
 WW: week code;  
 LLL: lot number;

### PACKAGE REFERENCE



**ABSOLUTE MAXIMUM RATINGS** <sup>(1)</sup>

Supply Voltage $V_{IN}$ .....	6V
$V_{SW}$ .....	
-0.3V (-5V for <10ns) to $V_{IN}+0.3V$ (10V for <10ns)	
All Other Pins .....	-0.3V to +6 V
Junction Temperature .....	150°C
Lead Temperature .....	260°C
Continuous Power Dissipation ( $T_A = 25^\circ C$ ) <sup>(2)</sup>	
.....	1.9W
Storage Temperature.....	-65°C to +150°C

**Recommended Operating Conditions** <sup>(3)</sup>

Supply Voltage $V_{IN}$ .....	2.5V to 5.5V
Output Voltage $V_{OUT}$ .....	0.6V to $V_{IN} - 0.5V$
Operating Junction Temp. ( $T_J$ ). -40°C to +125°C	

<b>Thermal Resistance</b> <sup>(4)</sup>	$\theta_{JA}$	$\theta_{JC}$	
QFN-10 (2mmx3mm).....	65.....	13...	°C/W

**Notes:**

- 1) Exceeding these ratings may damage the device.
- 2) The maximum allowable power dissipation is a function of the maximum junction temperature  $T_J$  (MAX), the junction-to-ambient thermal resistance  $\theta_{JA}$ , and the ambient temperature  $T_A$ . The maximum allowable continuous power dissipation at any ambient temperature is calculated by  $P_D$  (MAX) =  $(T_J$  (MAX) -  $T_A$ ) /  $\theta_{JA}$ . Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- 3) The device is not guaranteed to function outside of its operating conditions.
- 4) Measured on JESD51-7, 4-layer PCB.

## ELECTRICAL CHARACTERISTICS

$V_{IN} = 5V$ ,  $T_J = -40^{\circ}C$  to  $125^{\circ}C$ , Typical value is tested at  $T_J = +25^{\circ}C$ . The limit over temperature is guaranteed by characterization, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Feedback Voltage	$V_{FB}$	$T_J = 25^{\circ}C$	591	600	609	mV
		$T_J = -40^{\circ}C$ to $85^{\circ}C$ <sup>(5)</sup>	588	600	612	
Feedback Current	$I_{FB}$	$V_{FB} = 0.63V$		10		nA
PFET Switch ON Resistance	$R_{DSON\_P}$			80		m $\Omega$
NFET Switch ON Resistance	$R_{DSON\_N}$			40		m $\Omega$
Switch Leakage		$V_{EN} = 0V$ , $V_{IN} = 5V$ , $V_{SW} = 0V$ and $5V$ , $T_J = 25^{\circ}C$		0.1	2	$\mu A$
PFET Current Limit		$T_J = 25^{\circ}C$	4.2	4.8		A
ON Time	$t_{ON}$	$V_{IN}=5V$ , $V_{OUT}=1.2V$		120		ns
		$V_{IN}=3.6V$ , $V_{OUT}=1.2V$		166		
Switching Frequency	$f_s$	$V_{IN}=3.3V$ , $V_{OUT}=1.2V$ , $T_J = 25^{\circ}C$	1800	2000		kHz
	$f_s$	$V_{IN}=3.3V$ , $V_{OUT} \geq 1.8V$ , $T_J = -40^{\circ}C$ to $125^{\circ}C$ <sup>(5)</sup>	1800		3000	
	$f_s$	$V_{IN}=5V$ , $V_{OUT} \geq 3.3V$ , $T_J = -40^{\circ}C$ to $125^{\circ}C$ <sup>(5)</sup>	1800		3000	
Minimum OFF Time	$t_{MIN-OFF}$			50		ns
Soft-Start Time	$t_{SS-ON}$	$V_{OUT}=1.2V$ , 10% to 90%		1.3		ms
Soft-Stop Time	$t_{SS-OFF}$	$V_{OUT}=1.2V$ , 90% to 10%		1		ms
Power-Good Upper Trip Threshold	$PG_H$	FB falling when PG turn to high voltage		110		%
Power-Good Upper Trip Hysteresis	$PG_{H\_Hys}$			5		%
Power-Good Lower Trip Threshold	$PG_L$	FB Rising when PG turn to high voltage		90		%
Power-Good Lower Trip Hysteresis	$PG_{L\_Hys}$			5		%
Power-Good Delay	$PG_D$			110		$\mu s$
Power-Good Sink Current Capability	$V_{PG-L}$	Sink 1mA			400	mV
Power-Good Logic High Voltage	$V_{PG-H}$	$V_{IN}=5V$ , $V_{FB}=0.6V$	4.9			V
Power-Good Internal Pull-Up Resistor	$R_{PG}$			500		k $\Omega$
Under-Voltage Lockout Threshold Rising			2.0	2.2	2.4	V
Under-Voltage Lockout Threshold Hysteresis				150		mV

## ELECTRICAL CHARACTERISTICS

$V_{IN} = 5V$ ,  $T_J = -40^{\circ}C$  to  $125^{\circ}C$ , Typical value is tested at  $T_J = +25^{\circ}C$ . The limit over temperature is guaranteed by characterization, unless otherwise noted.

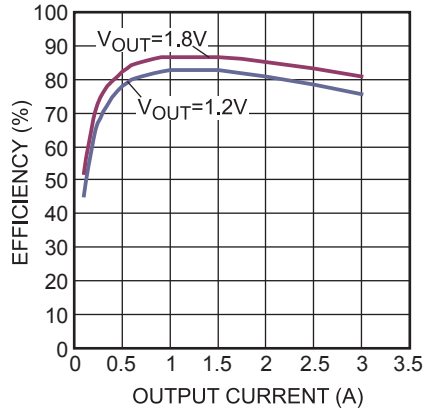
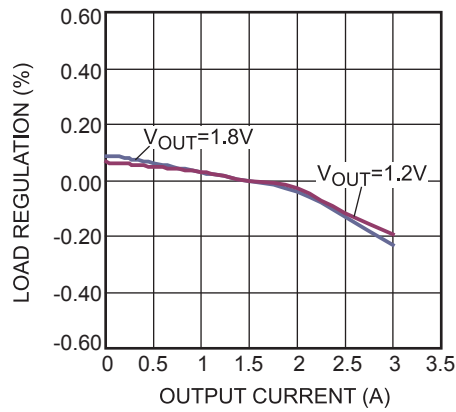
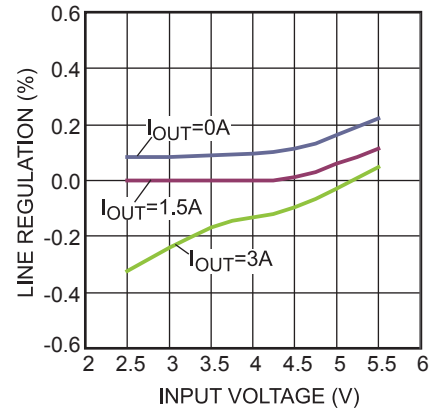
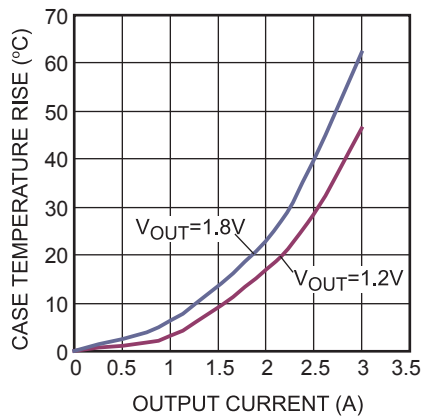
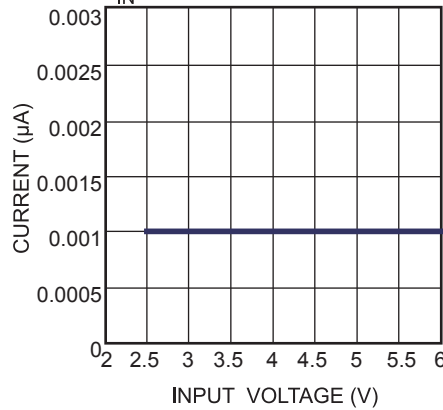
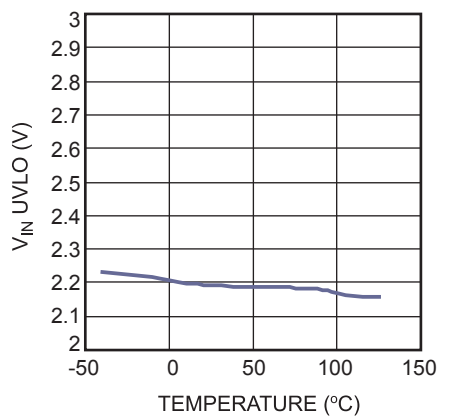
Parameter	Symbol	Condition	Min	Typ	Max	Units
EN Input Logic Low Voltage					0.4	V
EN Input Logic High Voltage			1.2			V
EN Input Current		$V_{EN}=2V$		2		$\mu A$
		$V_{EN}=0V$		0.1		$\mu A$
Supply Current (Shutdown)		$V_{EN}=0V$		0.1		$\mu A$
Thermal Shutdown <sup>(6)</sup>				170		$^{\circ}C$
Thermal Hysteresis <sup>(6)</sup>				30		$^{\circ}C$

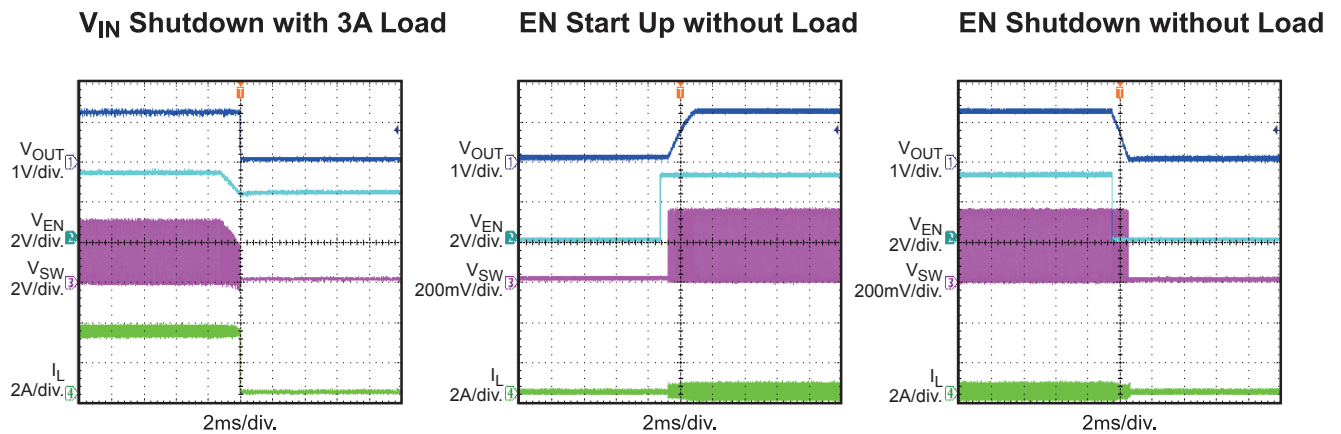
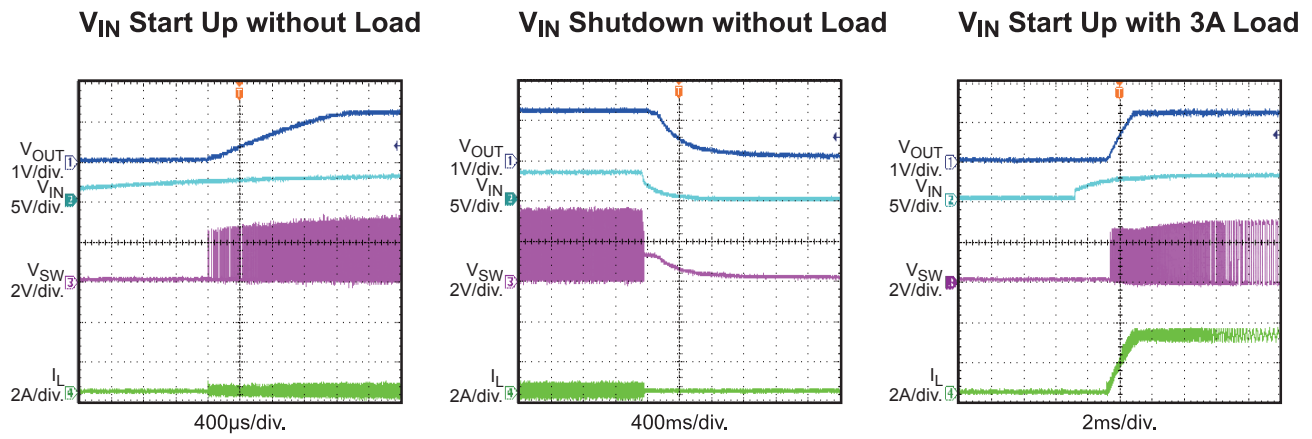
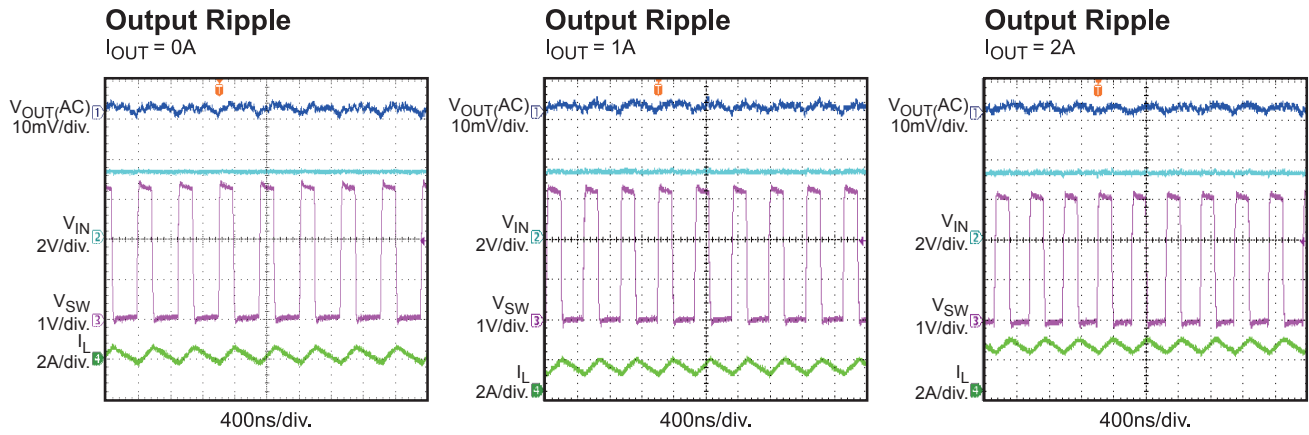
**Notes:**

- 5) Guaranteed by characterization, not production tested.
- 6) Design Guarantee, no production test.

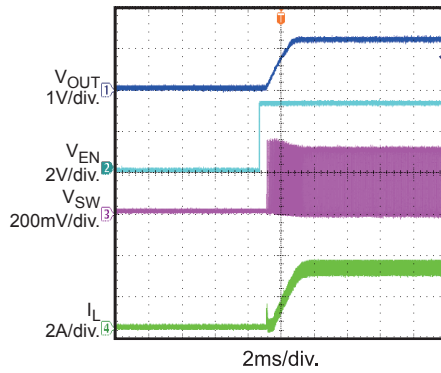
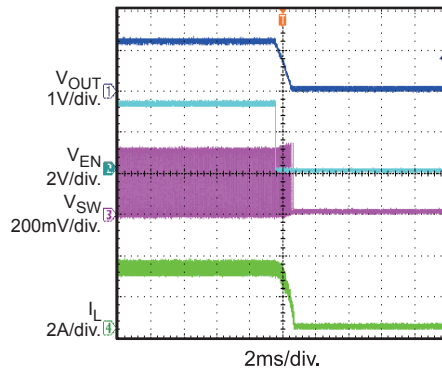
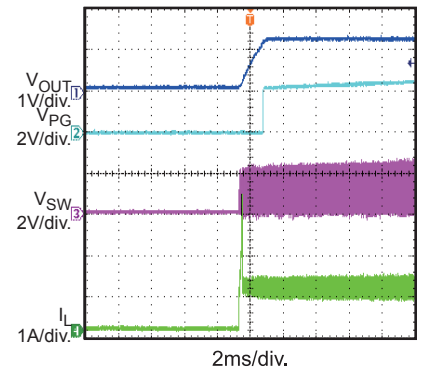
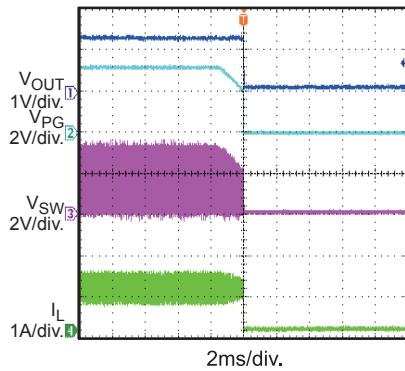
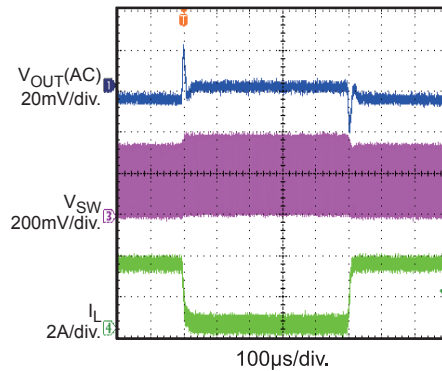
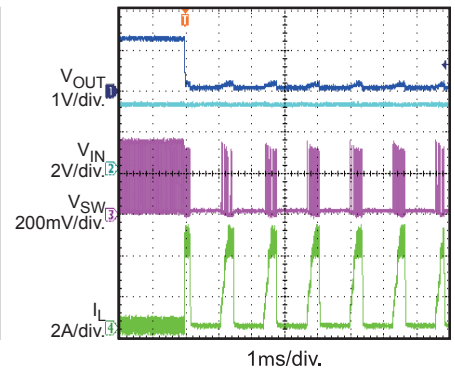
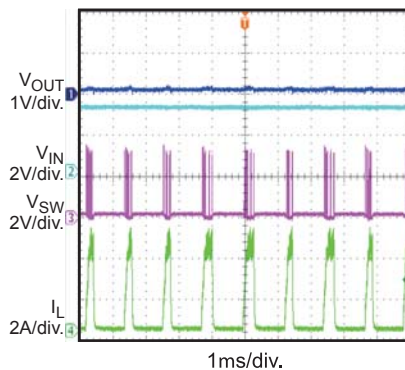
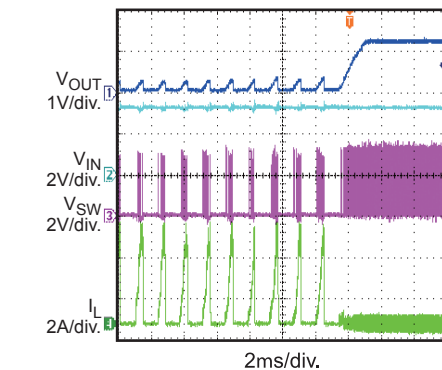
## TYPICAL PERFORMANCE CHARACTERISTICS

$V_{IN} = 5V$ ,  $V_{OUT} = 1.2V$ ,  $L = 0.47 \mu H$ ,  $C_{OUT} = 22 \mu F$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

**Efficiency**
 $V_{IN} = 3.3V$ 

**Load Regulation**
 $V_{IN} = 3.3V$ 

**Line Regulation**
 $V_{IN} = 3.3V$ 

**Case Temperature Rise**
 $V_{IN} = 3.3V$ 

**Shutdown Current vs. Input Voltage**
 $V_{IN} = 5V$ 

 **$V_{IN}$  UVLO vs. Temperature**


**TYPICAL PERFORMANCE CHARACTERISTICS (continued)**
 $V_{IN} = 3.3V$ ,  $V_{OUT} = 1.2V$ ,  $L = 0.47 \mu H$ ,  $C_{OUT} = 22 \mu F$ ,  $T_A = 25^\circ C$ , unless otherwise noted.


**TYPICAL PERFORMANCE CHARACTERISTICS (continued)**
 $V_{IN} = 3.3V$ ,  $V_{OUT} = 1.2V$ ,  $L = 0.47 \mu H$ ,  $C_{OUT} = 22 \mu F$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

**EN Start Up with 3A Load**

**EN Shutdown with 3A Load**

**VIN Start Up (PG) with 1A Load**

**VIN Shutdown (PG) with 1A Load**

**Load Transient Response**

**Short Circuit Entry**

**Short Circuit**

**Short Circuit Recovery**




## PIN FUNCTIONS

QFN-10 Pin #	Name	Description
1	EN	On/Off Control
2	FB	Feedback pin. Connect an external resistor divider from the output to AGND to set the output voltage.
3	AGND	Analog ground. Reference for the internal control circuit.
4	OUT	Input Sense. For output voltage feedback.
5	NC	Not Connected. It can be floated or connected to PGND for thermal.
6, 7	PGND	Power Ground
8	SW	Switch Output
9	VIN	Supply Voltage. The MP2143H operates from a 2.5V-to-5.5V unregulated input. C1 prevents large voltage spikes from appearing at the input.
10	PG	Power-Good Indicator. The pin output is an open drain that connects to VIN by an internal pull-up resistor. PG is pulled up to VIN when the FB voltage is within $\pm 10\%$ of the regulation level. If FB voltage is out of that regulation range, it is LOW.

### FUNCTIONAL BLOCK DIAGRAM

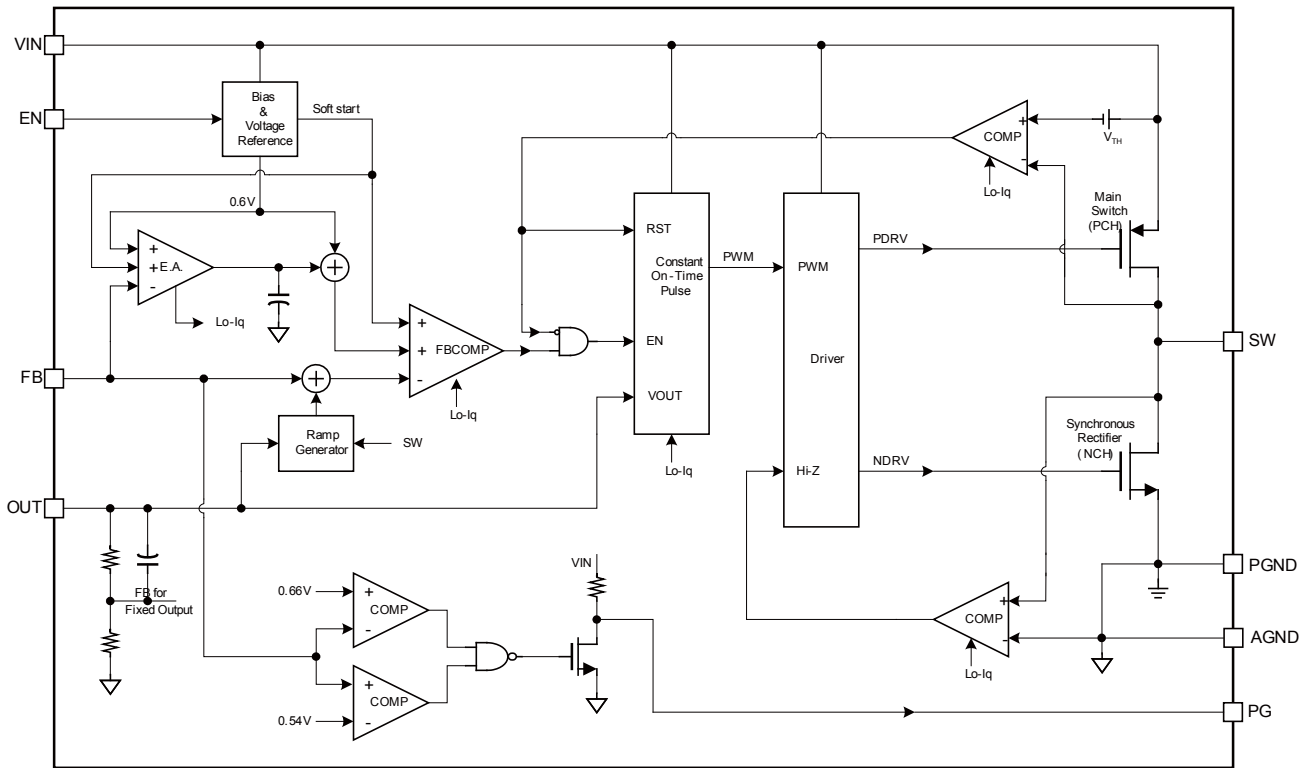


Figure 1: Functional Block Diagram

## OPERATION

The MP2143H uses constant-on-time control with input-voltage feed-forward to stabilize the switching frequency over its full input range. It can achieve up to 3A continuous output current from a 2.5V to 5.5V input voltage with excellent load and line regulation. The output voltage can be regulated as low as 0.6V.

### Constant-On-Time Control

When compared to fixed-frequency PWM control, constant on-time control offers a simpler control loop and faster transient response. By using input-voltage feed-forward, the MP2143H maintains a nearly constant switching frequency across the entire input and output voltage range. The switching pulse ON time can be estimated as:

$$T_{on} = V_{OUT}/V_{IN} \times 0.500\mu s$$

To prevent inductor current runaway during the load transient, the MP2143H has a fixed minimum OFF time of 50ns. However, this minimum OFF time limit does not affect the operation of the MP2143H in steady state in any way.

### Enable

When the input voltage exceeds the under-voltage lockout (UVLO) threshold—typically 2.2V—the MP2143H is enabled by pulling the EN pin above 1.2V. Leaving the EN pin floating or grounded will disable the MP2143H. There is an internal 1M $\Omega$  resistor from the EN pin to ground.

### Soft-Start/Stop

MP2143H has a built-in soft-start that ramps up the output voltage at a constant slew rate that avoids overshooting at startup. The soft-start time is typically about 1.3ms. When disabled, the MP2143H ramps down the internal reference voltage to allow the load to linearly discharge the output.

### Power Good Indicator

MP2143H has an open drain with 500k $\Omega$  pull-up resistor pin for power good (PG) indication. When the FB pin is within  $\pm 10\%$  of regulation voltage (0.6V), the PG pin is pulled up to  $V_{IN}$  by the internal resistor. If the FB pin voltage is outside the  $\pm 10\%$  window, the PG pin is pulled to ground by an internal MOSFET. The MOSFET has a maximum  $R_{dson}$  of less than 100 $\Omega$ .

### Current Limit

The MP2143H has a 4.8A current limit for the high side switch (HS-FET). When the HS-FET hits its current limit, the MP2143H enters hiccup mode until the current drops to prevent the inductor current from building and possibly damaging the components.

### Short Circuit and Recovery

The MP2143H also enters short-circuit protection (SCP) mode when it hits the current limit, and tries to recover from the short circuit by entering hiccup mode. In SCP, the MP2143H disables the output power stage, discharges a soft-start capacitor, and then enacts a soft-start procedure. If the short-circuit condition still holds after soft-start ends, the MP2143H repeats this operation until the short circuit ceases and output rises back to regulation level.

## APPLICATION INFORMATION

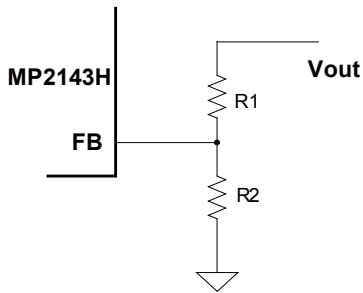
### COMPONENT SELECTION

#### Setting the Output Voltage

The external resistor divider sets the output voltage (see the Typical Application schematic on page 1). The feedback resistor R1 must account for both stability and dynamic response, and thus can not be too large or too small. Choose an R1 value between 120kΩ and 200kΩ. R2 is then given by:

$$R2 = \frac{R1}{\frac{V_{out}}{0.6} - 1}$$

The feedback circuit is shown as Figure 2.



**Figure 2: Feedback Network**

Table 1 lists the recommended resistors values for common output voltages.

**Table 1: Resistor Values for Common Output Voltages**

V <sub>OUT</sub> (V)	R1 (kΩ)	R2 (kΩ)
1.0	200(1%)	300(1%)
1.2	200(1%)	200(1%)
1.8	200(1%)	100(1%)
2.5	200(1%)	63.2(1%)
3.3	200(1%)	44.2(1%)

#### Selecting the Inductor

A 0.47μH to 1.5μH inductor is recommended for most applications. For highest efficiency, choose an inductor with a DC resistance less than 15mΩ. For most designs, the inductance value can be derived from the following equation.

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}}$$

Where ΔI<sub>L</sub> is the inductor ripple current.

Choose an inductor current to be approximately 30% of the maximum load current. The maximum inductor peak current is:

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2}$$

#### Selecting the Input Capacitor

The input current to the step-down converter is discontinuous, and requires a capacitor to supply the AC current to the step-down converter while maintaining the DC input voltage. Use low-ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR values and small temperature coefficients. For most applications, a 10μF capacitor is sufficient. For higher output voltage, use 47μF to improve system stability.

Since the input capacitor absorbs the input switching current it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated by:

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

The worse case condition occurs at V<sub>IN</sub> = 2V<sub>OUT</sub>, where:

$$I_{C1} = \frac{I_{LOAD}}{2}$$

For simplification, choose an input capacitor whose RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum or ceramic. When using electrolytic or tantalum capacitors, use a small high-quality ceramic capacitor (0.1μF), placed as close to the IC as possible. When using ceramic capacitors, make sure that they have enough capacitance to prevent excessive voltage ripple at input. The input voltage ripple caused by capacitance can be estimated by:

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_s \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

### Selecting the Output Capacitor

The output capacitor (C2) maintains the output DC voltage. Use ceramic capacitors. Low-ESR capacitors keep the output voltage ripple low. The output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_s \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_s \times C2}\right)$$

Where  $L_1$  is the inductor value and  $R_{ESR}$  is the equivalent series resistance of the output capacitor.

Using ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is mainly caused by the capacitance. For simplification, the output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_s^2 \times L_1 \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated as:

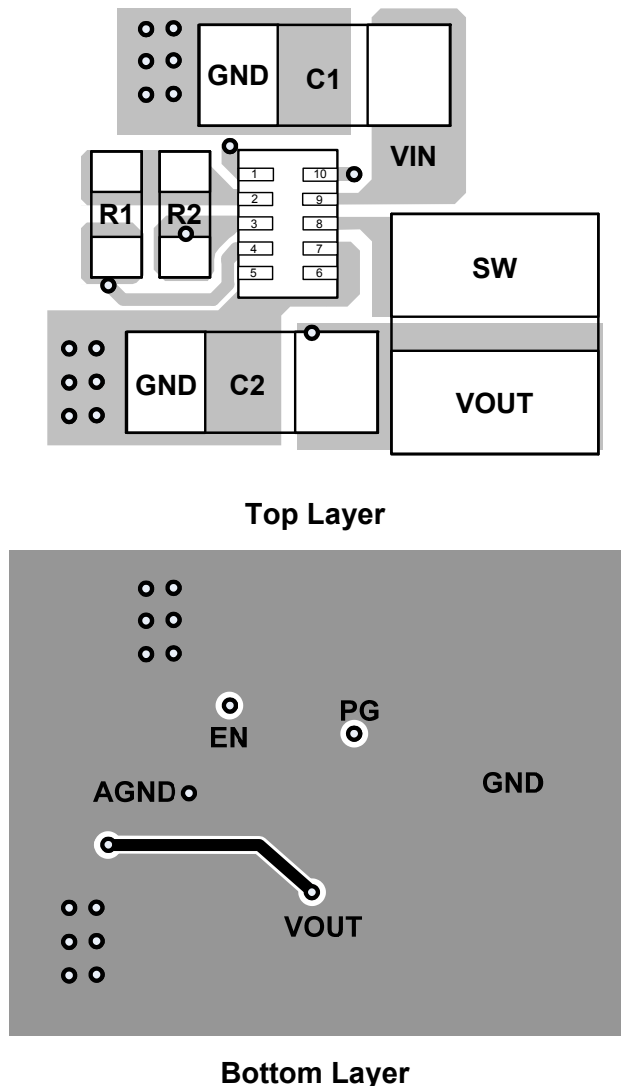
$$\Delta V_{OUT} = \frac{V_{OUT}}{f_s \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR}$$

The characteristics of the output capacitor also affect the stability of the regulation system.

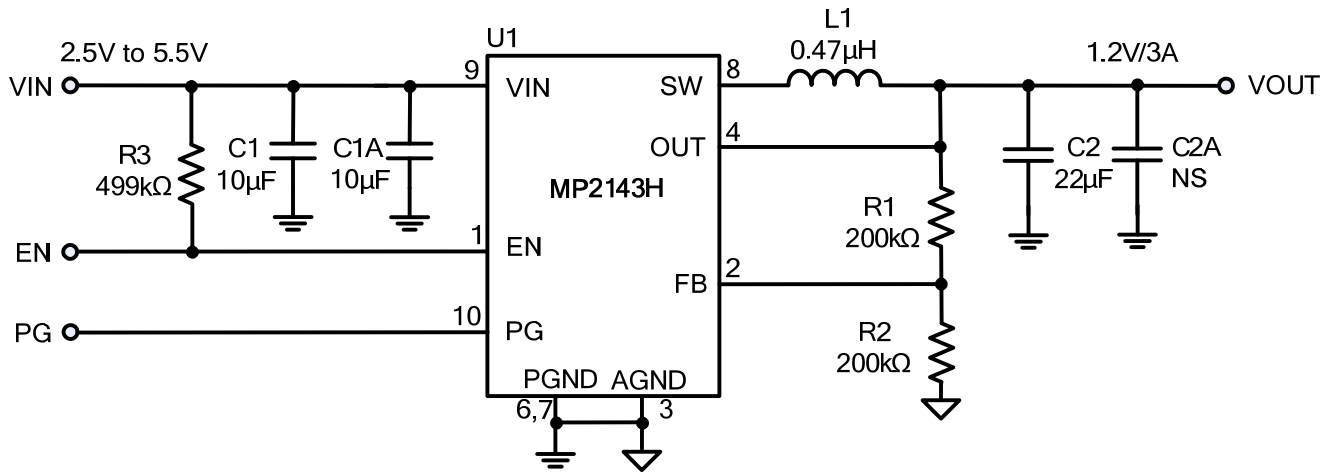
### PCB Recommendation of MP2143H

Proper layout of the switching power supplies is very important, and sometimes critical for proper operation. For high-frequency switching converters, poor layout could lead to poor line or load regulation and stability issues.

The high current paths (GND, VIN, and SW) should be placed very close to the device using short, direct, and wide traces. The input capacitor needs to be as close as possible to the VIN and GND pins. The external feedback resistors should be placed next to the FB pin. Keep the switching node SW short and away from the feedback network.

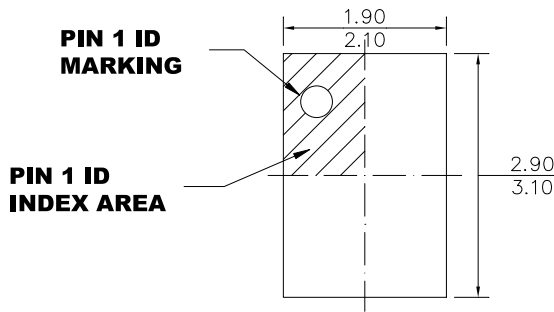


**Figure 3: Layout Recommendation**

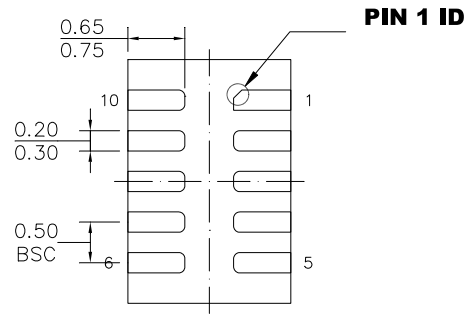
**TYPICAL APPLICATION CIRCUITS**

**Figure 4: MP2143H Typical Application Circuit**

## PACKAGE INFORMATION

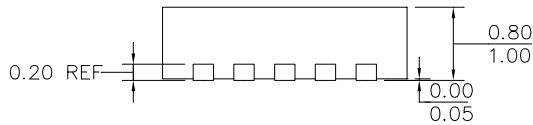
### QFN-10 (2mmx3mm)



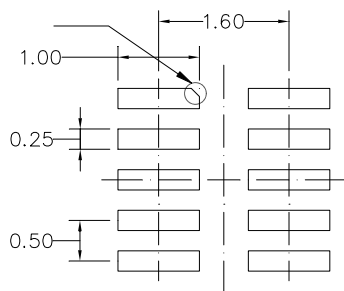
**TOP VIEW**



**BOTTOM VIEW**



**SIDE VIEW**



### **RECOMMENDED LAND PATTERN**

### **NOTE:**

- 1) ALL DIMENSIONS ARE IN MILLIMETERS.
- 2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
- 3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
- 4) JEDEC REFERENCE IS MO-220.
- 5) DRAWING IS NOT TO SCALE.

**NOTICE:** The information in this document is subject to change without notice. Please contact MPS for current specifications. Users should warrant and guarantee that third party Intellectual Property rights are not infringed upon when integrating MPS products into any application. MPS will not assume any legal responsibility for any said applications.