

#### DESCRIPTION

The MP18024 is a high-frequency, 100V, half-bridge, N-channel, power MOSFET driver. Its low-side and high-side driver channels are independently controlled and matched with less than 5ns in time delay. Under-voltage lockout on both high-side and low-side supplies force their outputs low in case of insufficient supply. The integrated bootstrap diode reduces external component count.

#### FEATURES

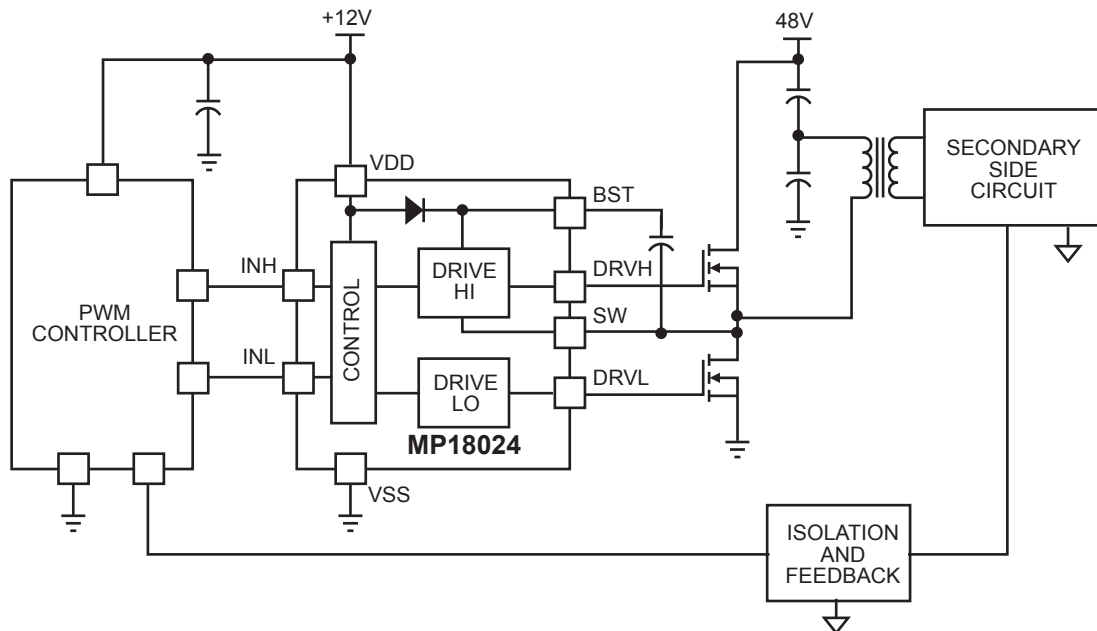
- Drives an N-Channel MOSFET Half Bridge
- 100V  $V_{BST}$  Voltage Range
- On-Chip Bootstrap Diode
- Typical Propagation Delay of 20ns
- Gate Drive Matching Of Less Than 5ns
- Drives A 2.2nf Load with 15nm Rise Time and 12ns Fall Time at 12v VDD
- TTL-Compatible Input
- Quiescent Current of Less Than 150 $\mu$ A
- UVLO for Both High Side and Low Side
- SOIC8E Package

#### APPLICATIONS

- Telecom Half-Bridge Power Supplies
- Avionics DC-DC Converters
- Two-Switch Forward Converters
- Active-Clamp Forward Converters

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#### TYPICAL APPLICATION

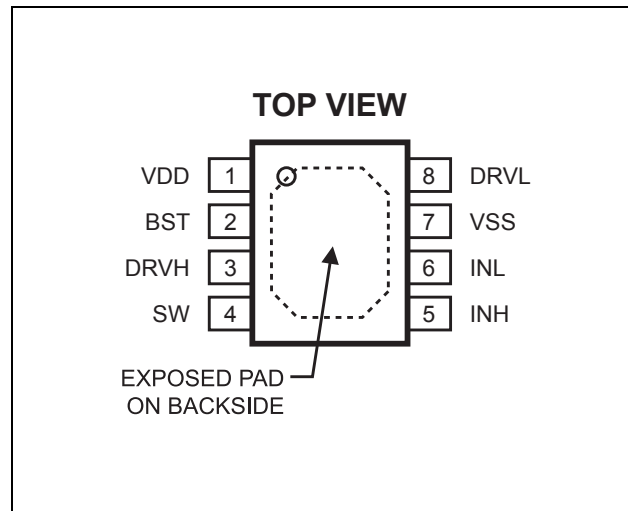


## ORDERING INFORMATION

Part Number*	Package	Top Marking
MP18024HN	SOIC8E	MP18024HN

\* For Tape & Reel, add suffix -Z (e.g. MP18024HN-Z);  
 For RoHS compliant packaging, add suffix -LF; (e.g. MP18024HN-LF-Z)

## PACKAGE REFERENCE



### ABSOLUTE MAXIMUM RATINGS <sup>(1)</sup>

Supply Voltage ( $V_{DD}$ )	-0.3V to +18V
SW Voltage ( $V_{SW}$ )	-5.0V to +105V
BST Voltage ( $V_{BST}$ )	-0.3V to +118V
BST to SW	-0.3V to +18V
DRVH to SW	-0.3V to (BST-SW) + 0.3V
DRVL to VSS	-0.3V to (VDD + 0.3V)
All Other Pins	-0.3V to (VDD + 0.3V)
Continuous Power Dissipation ( $T_A = 25^\circ\text{C}$ ) <sup>(2)</sup>	2.6W
Junction Temperature	150°C
Lead Temperature	260°C
Storage Temperature	-65°C to +150°C

### Recommended Operating Conditions <sup>(3)</sup>

Supply Voltage $V_{DD}$	9.0V to 16.0V
SW Voltage ( $V_{SW}$ )	-1.0V to 100V
SW Slew Rate	<50V/ns
Operating Junction Temp. ( $T_J$ )	-40°C to +125°C

<b>Thermal Resistance <sup>(4)</sup></b>	$\theta_{JA}$	$\theta_{JC}$
SOIC8E	48	10... °C/W

#### Notes:

- 1) Exceeding these ratings may damage the device.
- 2) The maximum allowable power dissipation is a function of the maximum junction temperature  $T_J(\text{MAX})$ , the junction-to-ambient thermal resistance  $\theta_{JA}$ , and the ambient temperature  $T_A$ . The maximum allowable continuous power dissipation at any ambient temperature is calculated by  $P_D(\text{MAX}) = (T_J(\text{MAX}) - T_A) / \theta_{JA}$ . Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- 3) The device is not guaranteed to function outside of its operating conditions.
- 4) Measured on JESD51-7, 4-layer PCB.

## ELECTRICAL CHARACTERISTICS

$V_{DD} = V_{BST} - V_{SW} = 12V$ ,  $V_{SS} = V_{SW} = 0V$ , No load at DRVH and DRVL,  $T_A = +25^\circ C$ , unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
<b>Supply Currents</b>						
VDD quiescent current	$I_{DDQ}$	INL = INH = 0		100	150	$\mu A$
VDD operating current	$I_{DDO}$	fsw = 500kHz		9		mA
Floating driver quiescent current	$I_{BSTQ}$	INL = INH = 0		60	90	$\mu A$
Floating driver operating current	$I_{BSTO}$	fsw = 500kHz		7.5		mA
Leakage current	$I_{LK}$	BST = SW = 100V		0.05	1	$\mu A$
<b>Inputs</b>						
INL/INH High				2	2.4	V
INL/INH Low			1	1.4		V
INL/INH internal pull-down resistance	$R_{IN}$			185		k $\Omega$
<b>Under Voltage Protection</b>						
VDD rising threshold	$V_{DDR}$		8.1	8.4	8.8	V
VDD hysteresis	$V_{DDH}$			0.5		V
(BST-SW) rising threshold	$V_{BSTR}$		6.9	7.3	7.7	V
(BST-SW) hysteresis	$V_{BSTH}$			0.55		V
<b>Bootstrap Diode</b>						
Bootstrap diode VF @ 100 $\mu A$	$V_{F1}$			0.5		V
Bootstrap diode VF @ 100mA	$V_{F2}$			0.95		V
Bootstrap diode dynamic R	$R_D$	@ 100mA		2		$\Omega$
<b>Low Side Gate Driver</b>						
Low level output voltage	$V_{OLL}$	$I_O = 100mA$		0.08		V
High level output voltage to rail	$V_{OHL}$	$I_O = -100mA$		0.23		V
Peak pull-up current	$I_{OHL}$	$V_{DRVL} = 0V, V_{DD} = 12V$		3		A
		$V_{DRVL} = 0V, V_{DD} = 16V$		4.7		A
Peak pull-down current	$I_{OLL}$	$V_{DRVL} = V_{DD} = 12V$		4.5		A
		$V_{DRVL} = V_{DD} = 16V$		6		A
<b>Floating Gate Driver</b>						
Low level output voltage	$V_{OLH}$	$I_O = 100mA$		0.08		V
High level output voltage to rail	$V_{OHH}$	$I_O = -100mA$		0.23		V
Peak pull-up current	$I_{OHH}$	$V_{DRVH} = 0V, V_{DD} = 12V$		2.6		A
		$V_{DRVH} = 0V, V_{DD} = 16V$		4		A
Peak pull-down current	$I_{OLH}$	$V_{DRVH} = V_{DD} = 12V$		4.5		A
		$V_{DRVH} = V_{DD} = 16V$		5.9		A

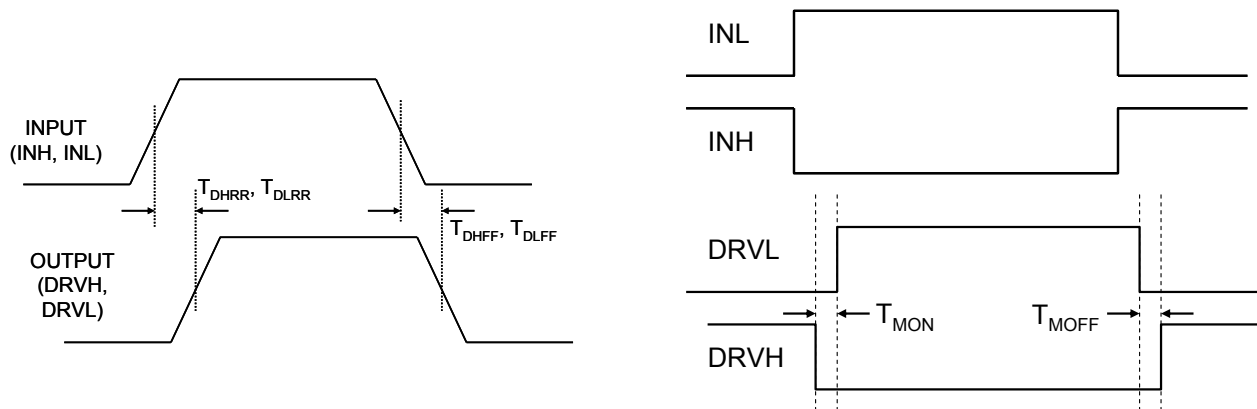
**ELECTRICAL CHARACTERISTICS** *(continued)*

$V_{DD} = V_{BST} - V_{SW} = 12V$ ,  $V_{SS} = V_{SW} = 0V$ , No load at DRVH and DRVL,  $T_A = 25^\circ C$ , unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
<b>Switching Spec. --- Low Side Gate Driver</b>						
Turn-off propagation delay INL falling to DRVL falling	$T_{DLFF}$			20		ns
Turn-on propagation delay INL rising to DRVL rising	$T_{DLRR}$			20		
DRVL rise time		$C_L = 2.2nF$		15		ns
DRVL fall time		$C_L = 2.2nF$		9		ns
<b>Switching Spec. --- Floating Gate Driver</b>						
Turn-off propagation delay INL falling to DRVH falling	$T_{DHFF}$			20		ns
Turn-on propagation delay INL rising to DRVH rising	$T_{DHRR}$			20		ns
DRVH rise time		$C_L = 2.2nF$		15		ns
DRVH fall time		$C_L = 2.2nF$		12		ns
<b>Switching Spec. --- Matching</b>						
Floating driver turn-off to low side drive turn-on	$T_{MON}$			1	5	ns
Low side driver turn-off to floating driver turn-on	$T_{MOFF}$			1	5	ns
Minimum input pulse width that changes the output	$T_{PW}$				50 <sup>(5)</sup>	ns
Bootstrap diode turn-on or turn- off time	$T_{BS}$			10 <sup>(5)</sup>		ns
Thermal shutdown				150		$^\circ C$
Thermal shutdown hysteresis				25		$^\circ C$

**Note:**

5) Guaranteed by design.

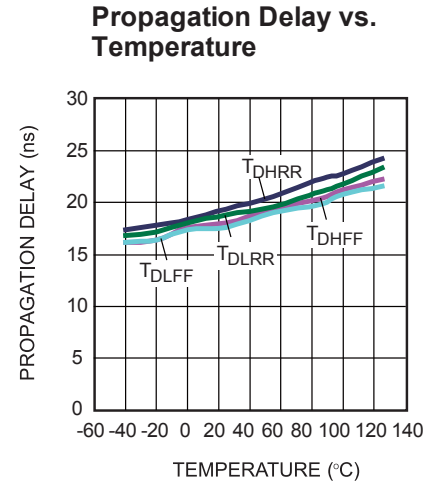
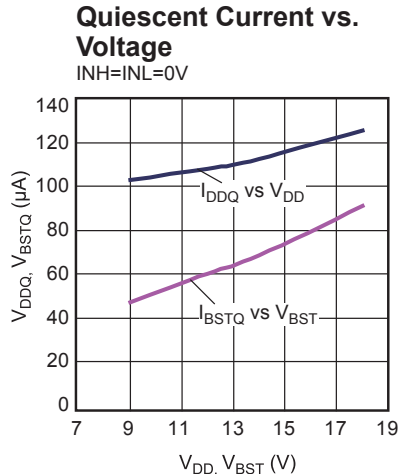
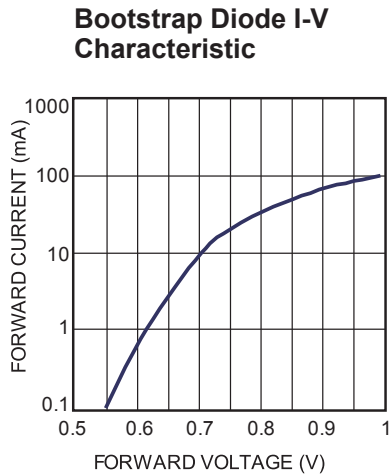
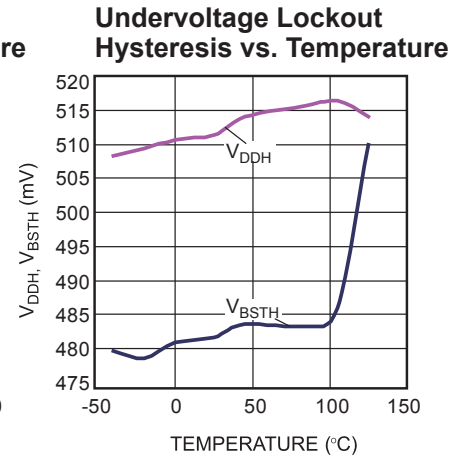
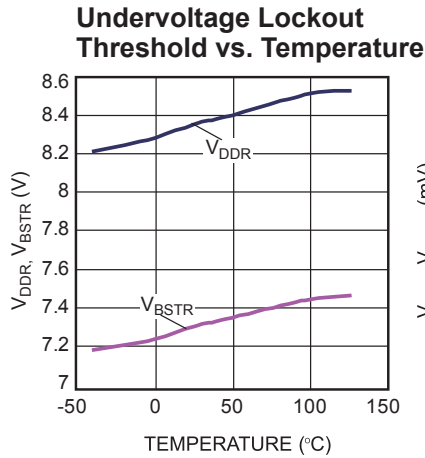
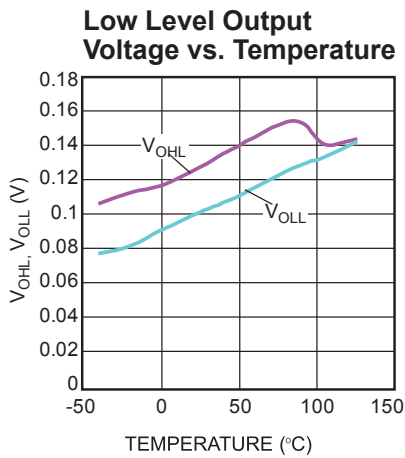
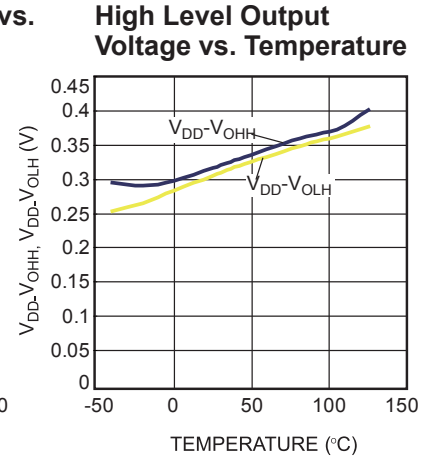
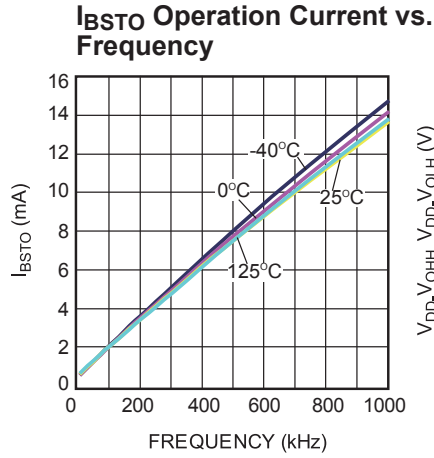
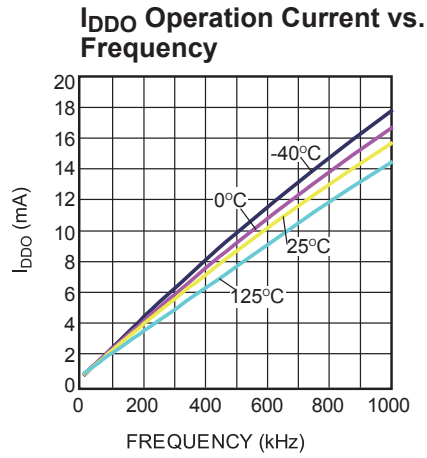

**Figure 1—Timing Diagram**

## PIN FUNCTIONS

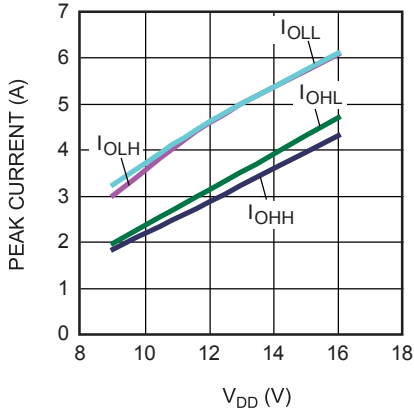
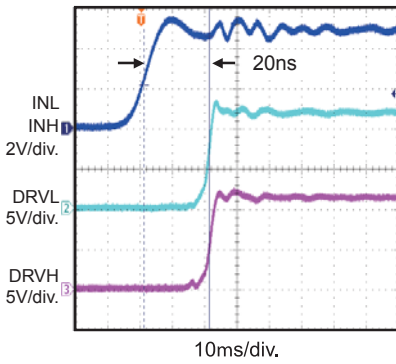
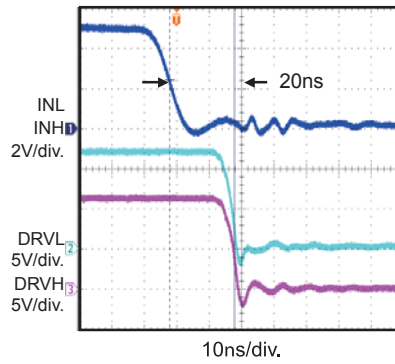
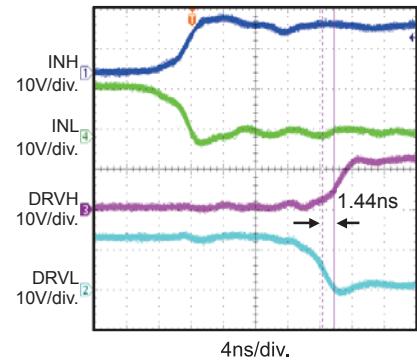
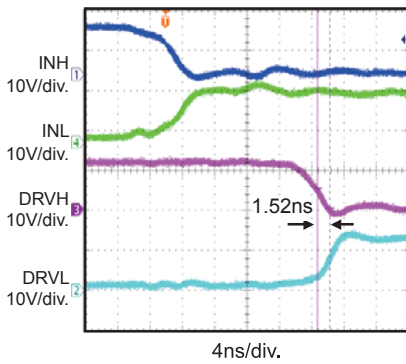
Pin #	Name	Description
1	VDD	Supply input. This pin supplies power to all the internal circuitry. Place a decoupling capacitor to ground close to this pin to ensure stable and clean supply.
2	BST	Bootstrap. This is the positive power supply for the internal floating high-side MOSFET driver. Connect a bypass capacitor between this pin and SW pin.
3	DRVH	Floating driver output.
4	SW	Switching node.
5	INH	Control signal input for the floating driver.
6	INL	Control signal input for the low side driver.
7	VSS, exposed pad	Chip ground. Connect exposed pad to VSS for proper thermal operation.
8	DRVL	Low side driver output.

## TYPICAL PERFORMANCE CHARACTERISTICS

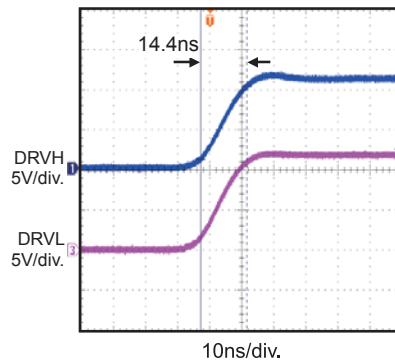
$V_{DD} = 12V$ ,  $V_{SS} = V_{SW} = 0V$ ,  $T_A = 25^\circ C$ , unless otherwise noted.



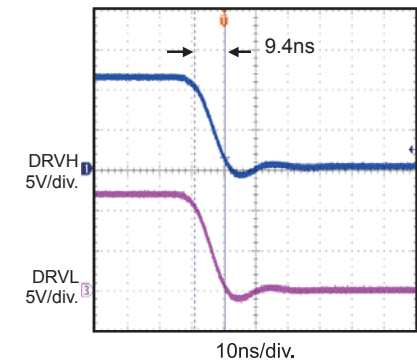
**TYPICAL PERFORMANCE CHARACTERISTICS (continued)**
 $V_{DD} = 12V, V_{SS} = V_{SW} = 0V, T_A = 25^\circ C$ , unless otherwise noted.

**Peak Current vs. V<sub>DD</sub> Voltage**

**Turn-on Propagation Delay**

**Turn-off Propagation Delay**

**Gate Drive Matching T<sub>MOFF</sub>**

**Gate Drive Matching T<sub>MON</sub>**

**Drive Rise Time**

2.2nF Load


**Drive Fall Time**

2.2nF Load



BLOCK DIAGRAM



Figure 2—Function Block Diagram



### APPLICATION

The input signals INH and INL can be controlled independently. If both INH and INL control the high-side MOSFET and low-side MOSFET of the same bridge, then users must avoid shoot through by

setting sufficient dead time between INH and INL low, and vice versa. See Figure 3 below. Dead time is defined as the time interval between INH low and INL low.

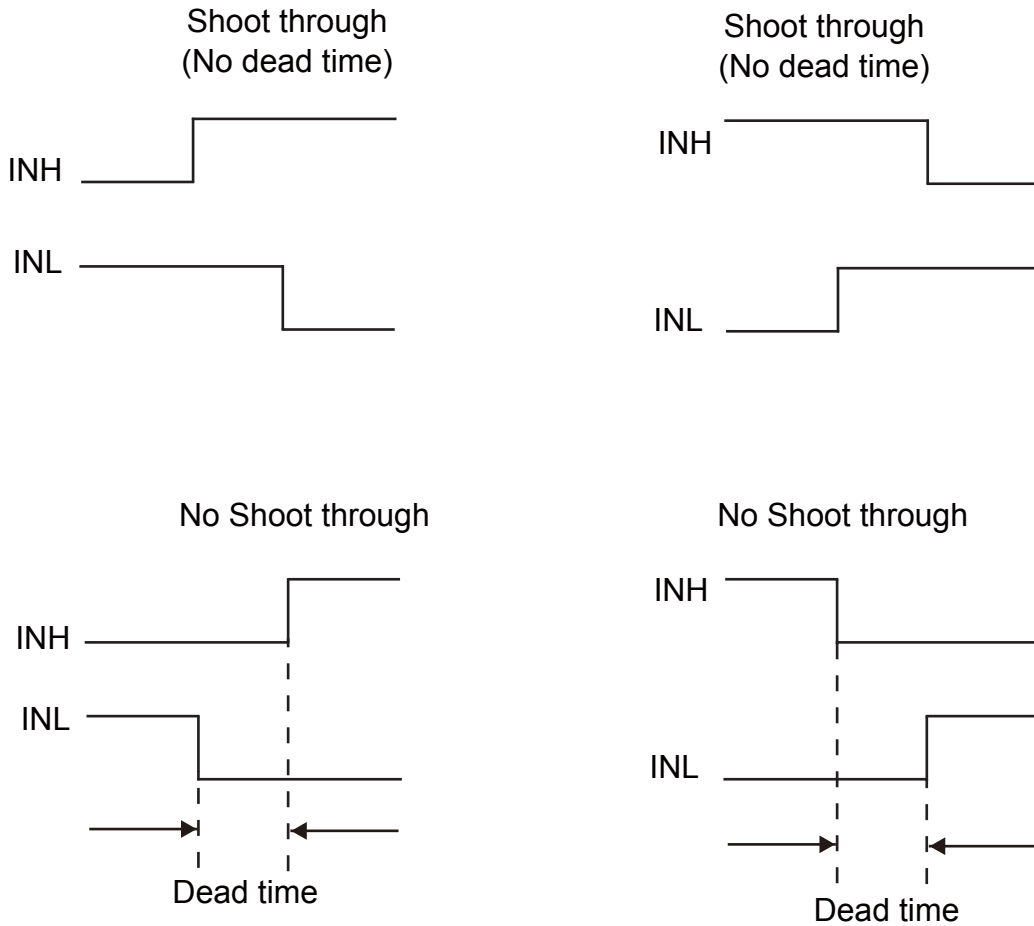


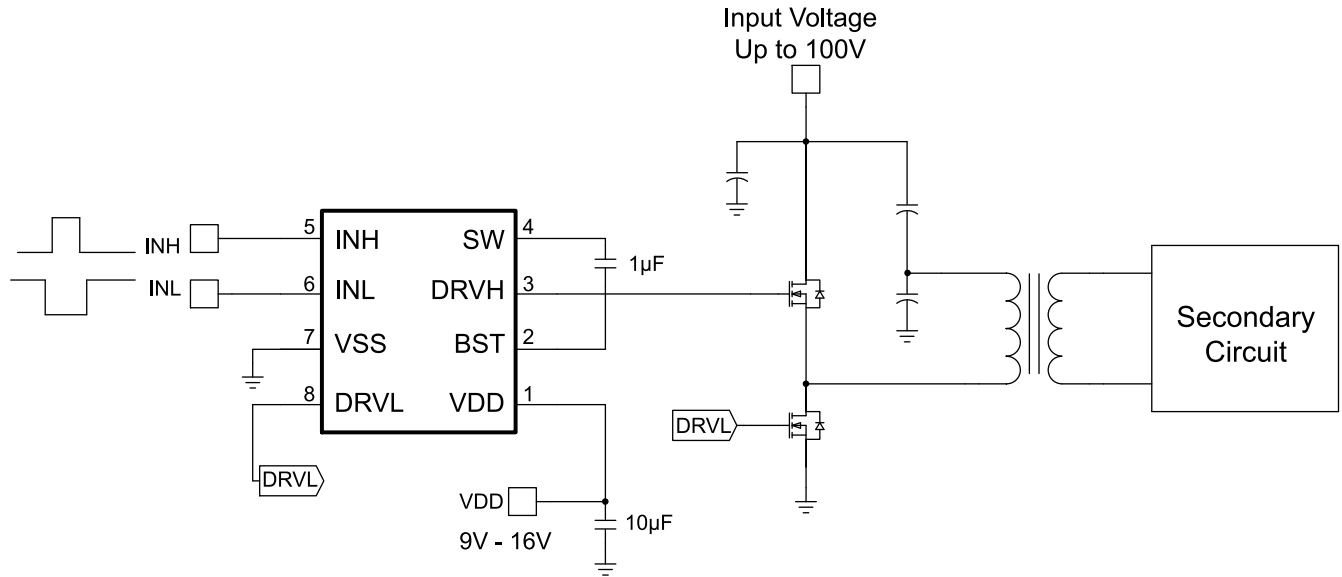
Figure 3—Shoot-Through Timing Diagram

## REFERENCE DESIGN CIRCUITS

### Half Bridge Converter

The MP18024 drives the MOSFETs with alternating signals (with dead time) in half-bridge converter topology. Therefore, from the PWM

controller drives INH and INL with alternating signals. The input voltage can go up to 100V.

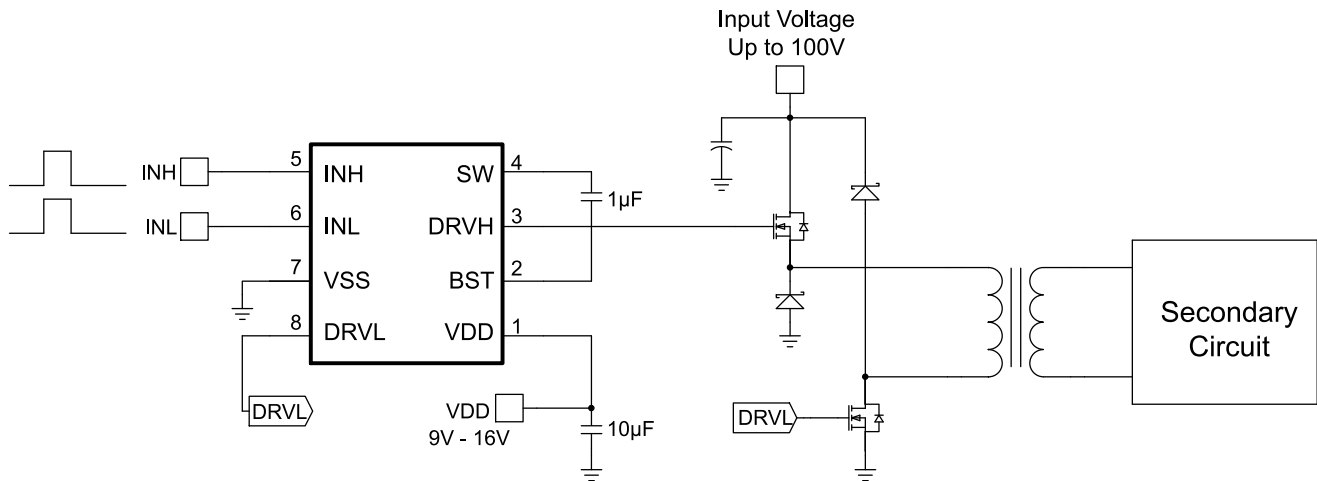


**Figure 4—Half Bridge Converter**

### Two-Switch Forward Converter

In two-switch forward converter topology, both MOSFETs are turned on and off simultaneously. The input signal (INH and INL) comes from a PWM controller that senses the output voltage (and output current during current-mode control).

The Schottky diodes clamp the reverse swing of the power transformer and must be rated for the input voltage. The input voltage can go up to 100V.

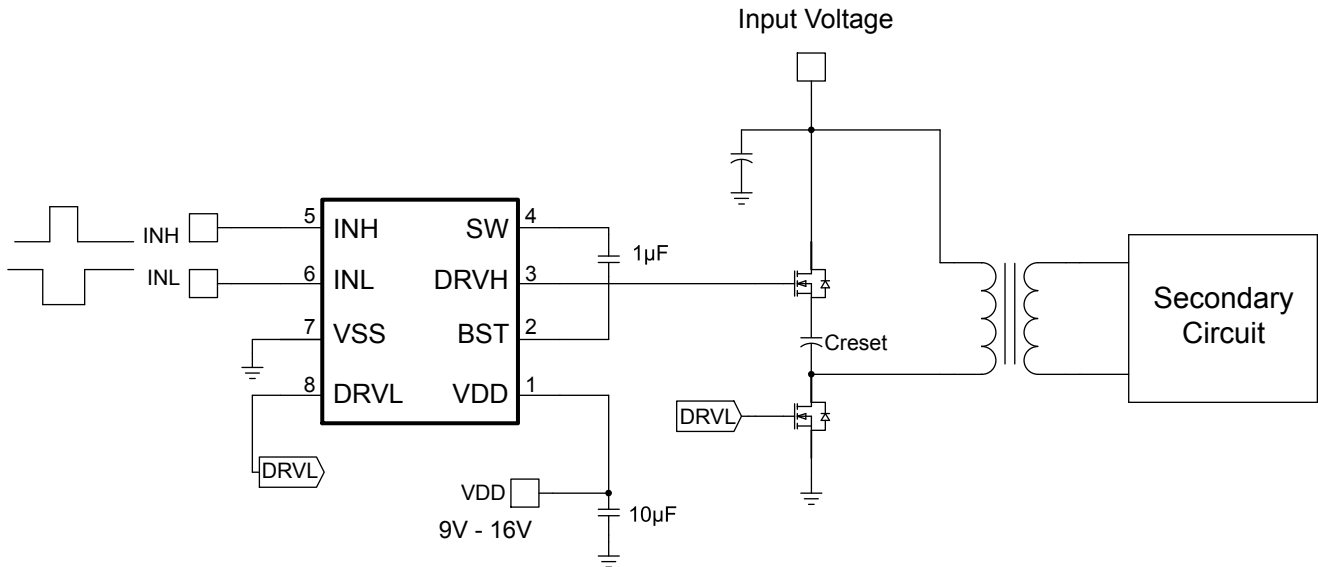


**Figure 5—Two-Switch Forward Converter**

### Active-Clamp Forward Converter

In active-clamp–forward converter topology, the MP18024 drives the MOSFETs with alternating signals. The high-side MOSFET, in conjunction with Creset, is used to reset the power transformer in a lossless manner.

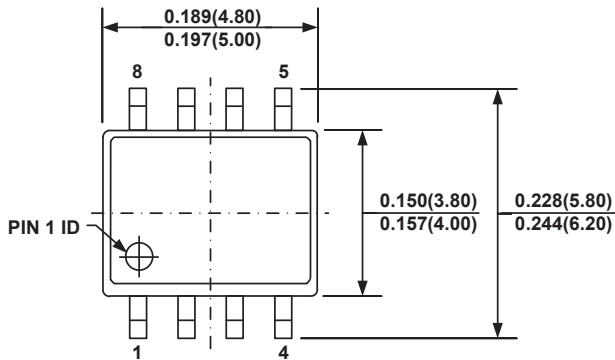
This topology lends itself well to run at duty cycles exceeding 50%. The device may not be able to run at 100V with this topology.



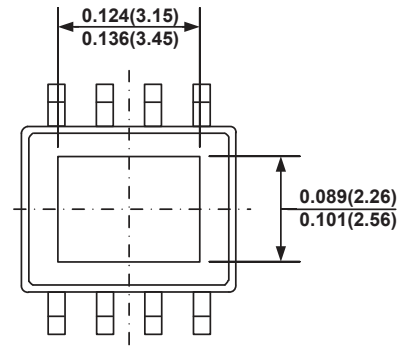
**Figure 6—Active-Clamp Forward Converter**

## PACKAGE INFORMATION

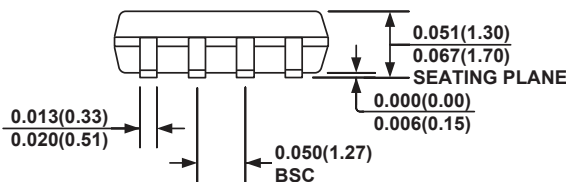
## SOIC8E



TOP VIEW

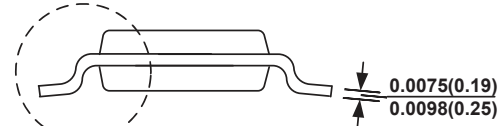


BOTTOM VIEW

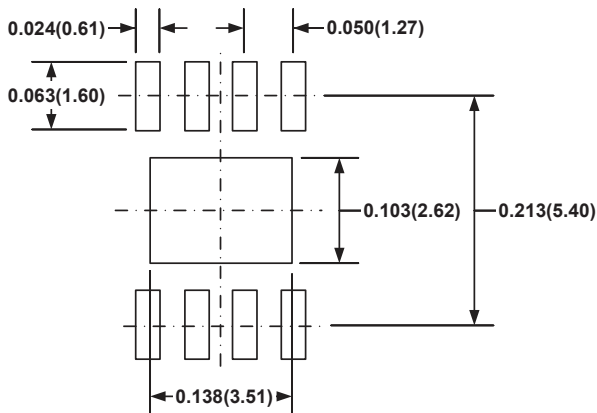


FRONT VIEW

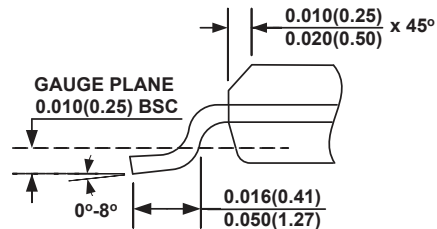
SEE DETAIL "A"



SIDE VIEW



RECOMMENDED LAND PATTERN



DETAIL "A"

## NOTE:

- 1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
- 2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
- 3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
- 4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
- 5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION BA.
- 6) DRAWING IS NOT TO SCALE.

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