MP1654N

16V, 4A, 1.1MHz, High-Efficiency, Synchronous Step-Down Converter in a SOT563 Package

DESCRIPTION

The MP1654N is a fully integrated, high-frequency, synchronous, rectified, step-down switch-mode converter with internal power MOSFETs. The device offers a very compact solution that achieves 4A of continuous output current (I_{OUT}), with excellent load and line regulation over a wide input voltage (V_{IN}) range. The MP1654N uses synchronous mode for higher efficiency across the I_{OUT} load range.

Constant-on-time (COT) control operation provides very fast transient response, easy loop design, and very tight output regulation.

Full protection features include short-circuit protection (SCP), over-current protection (OCP), under-voltage protection (UVP), and thermal shutdown.

The MP1654N requires a minimal number of readily available, standard external components, and is available in a space-saving SOT563 (1.6mmx1.6mm) package.

FEATURES

- Wide 4.5V to 16V Operating Input Voltage (V_{IN}) Range
- 4A Output Current (I_{OUT})
- 47mΩ/28mΩ Low On Resistance ($R_{DS(ON)}$) Internal Power MOSFETs
- 110μA Quiescent Current (I_Q)
- 0.6V to 8V Output Voltage (V_{OUT}) Range
- ±1% Feedback (FB) Accuracy at Room Temperature
- ±1.5% FB Accuracy at Full Temperature
- 1.1MHz Switching Frequency (f_{SW})
- Power-Save Mode for High Light Load Efficiency
- Excellent Load Transient Performance
- Pre-Biased Start-Up
- Enable (EN) Power Sequencing
- Over-Current Protection (OCP) with Hiccup Mode
- Thermal Shutdown
- Available in a SOT563 (1.6mmx1.6mm) Package

MPL Optimized Performance with MPS Inductor MPL-AL4020 and MPL-AL6050 Series

APPLICATIONS

- Flat-Panel Television and Monitors
- Digital Set-Top Boxes
- Security Cameras
- General-Purpose Power Supplies

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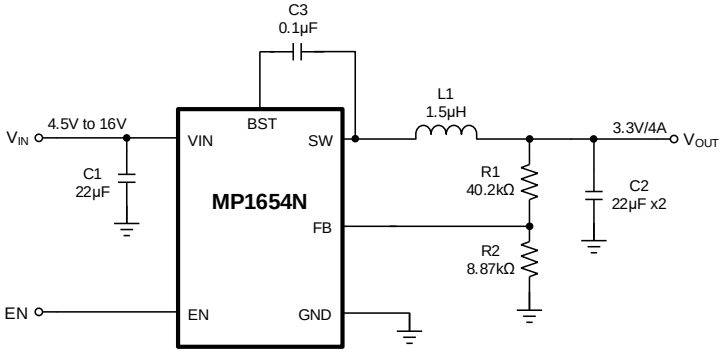
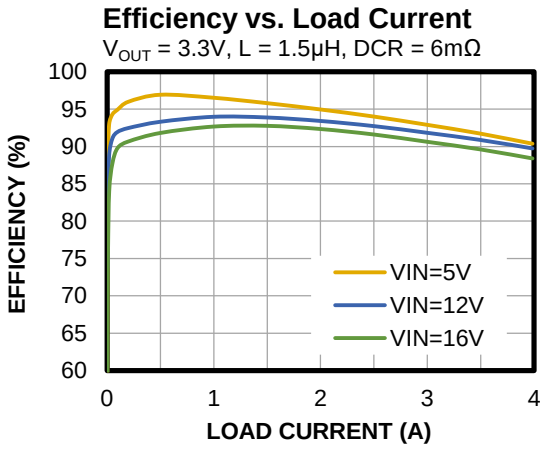
TYPICAL APPLICATION





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ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP1654NGTF	SOT563 (1.6mmx1.6mm)	*See Below*	1

* For Tape & Reel, add suffix -Z (e.g. MP1654NGTF-Z).

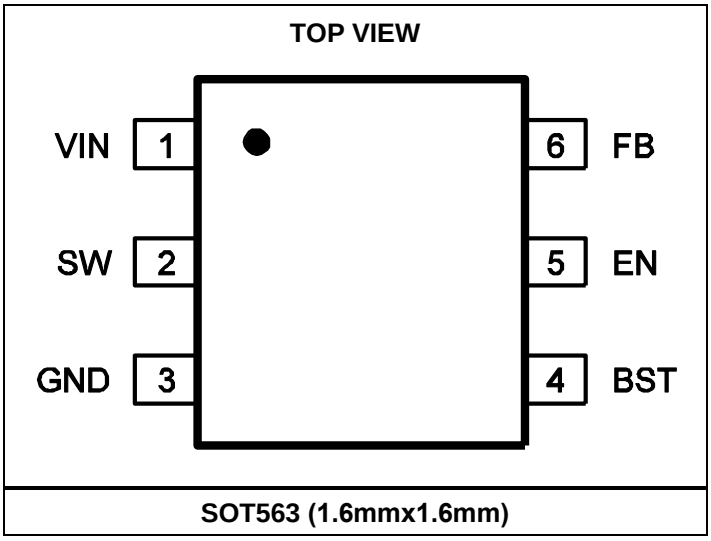
TOP MARKING

CEMY

LLL

CEM: Product code of MP1654NGTF
Y: Year code
LLL: Lot number

PACKAGE REFERENCE



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PIN FUNCTIONS

Pin #	Name	Description
1	VIN	**Supply voltage.** A capacitor is required to decouple the input rail. Connect the VIN pin using a wide PCB trace.
2	SW	**Switch output.** Connect the SW pin using a wide PCB trace.
3	GND	**System ground.** The GND pin is the reference ground of the regulated output voltage (V_{OUT}) and requires extra care during PCB layout. Connect GND using copper traces and vias.
4	BST	**Bootstrap.** Connect a 0.1µF to 1µF BST capacitor (C_{BST}) and a resistor between the SW and BST pins to form a floating supply across the high-side MOSFET (HS-FET) driver.
5	EN	**Enable.** Pull EN high to enable the chip. For automatic start-up, connect EN to VIN via a 100kΩ resistor.
6	FB	**Feedback.** To set V_{OUT}, connect the FB pin to the tap of an external resistor divider placed between the output and GND.

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}) .....-0.3V to +18V
SW voltage (V_{SW}) .....-0.3V (-4V for <10ns)
.....to V_{IN} + 0.3V (22V for <10ns)
BST voltage (V_{BST}) ..... V_{SW} + 4V
EN voltage (V_{EN}) .....-0.3V to +18V
All other pins .....-0.3V to +4V
Continuous power dissipation (T_A = 25°C) (2) (5)
SOT563 (1.6mmx1.6mm) 2W
Junction temperature (T_J) .....150°C
Lead temperature .....260°C
Storage temperature ..... -65°C to +150°C

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) .....4.5V to 16V
Output voltage (V_{OUT}).....
.....0.6V to V_{IN} x D_{MAX} or 8V max
Operating junction temp (T_J).... -40°C to +125°C

Thermal Resistance θ_{JA} θ_{JB}

SOT563 (1.6mmx1.6mm)
JEDEC (4).....130….33.5..°C/W
EVL1654N-TF-00A (5).....60……..°C/W

θ_{JC_TOP} θ_{JC_BOT}

JEDEC (4).....65.....17.4..°C/W

ψ_{JT}

JEDEC (4).....3.9...°C/W
EVL1654N-TF-00A (5).....4…°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation may generate an excessive die temperature, which can cause the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) The θ_{JA} value is only valid for comparison with other packages and cannot be used for design purposes. This value is based on a JEDEC51-7 board. They do not represent the performance obtained in an actual application.
5) Measured on the EVL1654N-TF-00A, a 2-layer, 2oz PCB (5cmx5cm). The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature in the real system, based on the following equation: $T_J = \psi_{JT} \times P_{LOSS} + T_{CASE_TOP}$, where P_{LOSS} is the entire loss of the IC in real application, and T_{CASE_TOP} is the case top temperature.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, V_{EN} = 2V, T_J = -40°C to +125°C, (6) typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Current						
Shutdown supply current	I_{SD}	V_{EN} = 0V			10	μA
Quiescent supply current	I_Q	V_{EN} = 2V, V_{FB} = 0.65V, no switching		110	200	μA
MOSFET						
High-side MOSFET (HS-FET) on resistance	$R_{DS(ON)_HS}$	V_{BST-SW} = 3.3V		47		mΩ
Low-side MOSFET (LS-FET) on resistance	$R_{DS(ON)_LS}$	V_{CC} = 3.3V		28		mΩ
Switch leakage	SW_{LKG}	V_{EN} = 0V, V_{SW} = 16V			10	μA
Current Limit and Zero-Current Detection (ZCD)						
Valley current limit	I_{LIMIT_VY}		4.3	5.5	6.9	A
Short hiccup duty cycle (7)	D_{HICCUP}			12.5		%
Zero-current detection (ZCD)	I_{ZCD}	V_{IN} = 12V, V_{OUT} = 3.3V, L = 1.5μH		150		mA
Switching Frequency and Minimum On/Off Times						
Switching frequency	f_{SW}	V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 2A, T_A = 25°C	1000	1100	1210	kHz
Minimum on time (7)	t_{ON_MIN}			45		ns
Minimum off time	t_{OFF_MIN}		80	115	150	ns
Reference and Soft Start (SS)						
Feedback voltage	V_{FB}	T_J = 25°C	594	600	606	mV
		T_J = -40°C to +125°C (6)	591	600	609	mV
Soft-start time	t_{SS}	V_{OUT} from 10% to 90%	0.5	1	1.6	ms
Enable (EN) and Under-Voltage Lockout (UVLO)						
EN rising threshold	V_{EN_RISING}		1.15	1.2	1.35	V
EN falling threshold	$V_{EN_FALLING}$		0.9	1	1.1	V
EN hysteresis	V_{EN_HYS}			200		mV
EN pull-down resistor	R_{EN}			1		MΩ
EN turn-on delay	$t_{EN_ON_DLY}$	From EN rising to the first switching		150		μs
V_{IN} under-voltage lockout (UVLO) rising threshold	$V_{IN_UVLO_RISING}$		4	4.25	4.5	V
V_{IN} UVLO falling threshold	$V_{IN_UVLO_FALLING}$		3.7	4	4.3	V
V_{IN} UVLO hysteresis	$V_{IN_UVLO_HYS}$			250		mV
Thermal Protection						
Thermal shutdown (7)	T_{SD}			155		°C
Thermal hysteresis (7)	T_{SD_HYS}			20		°C

Notes:

6) Over-temperature (OT) limits are guaranteed by design, characterization. and correlation. Not tested in production.
7) Derived by sample characterization, not tested in production.

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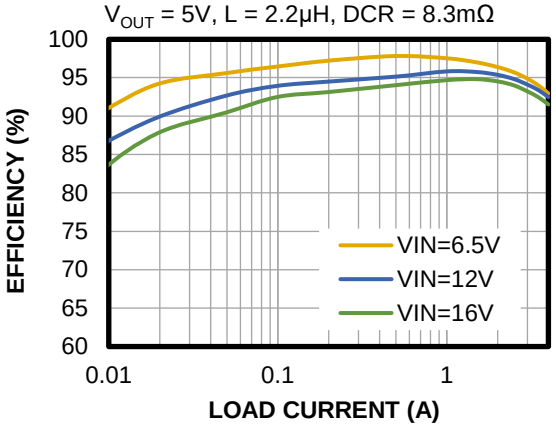
TYPICAL CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 3.3V, L = 1.5µH, T_A = 25°C, unless otherwise noted.

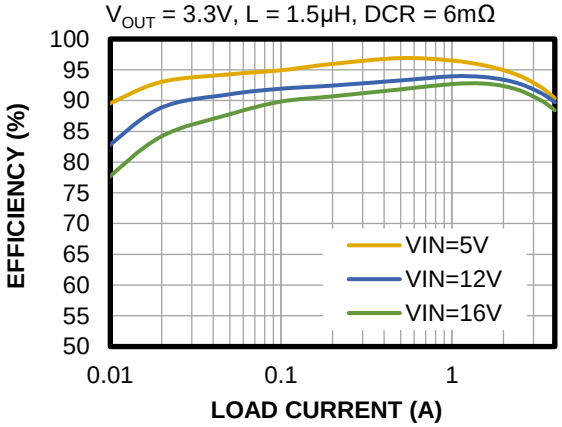
Efficiency vs. Load Current

V_{OUT} = 5V, L = 2.2µH, DCR = 8.3mΩ



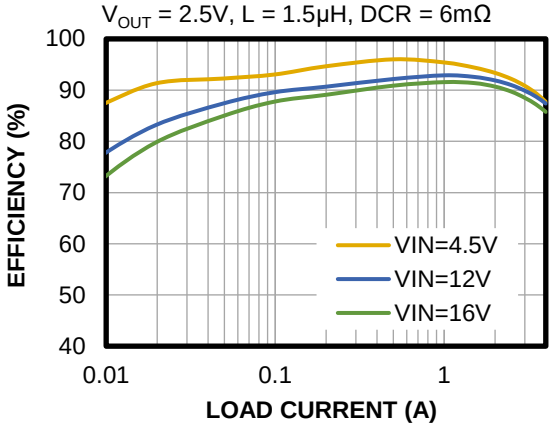
Efficiency vs. Load Current

V_{OUT} = 3.3V, L = 1.5µH, DCR = 6mΩ



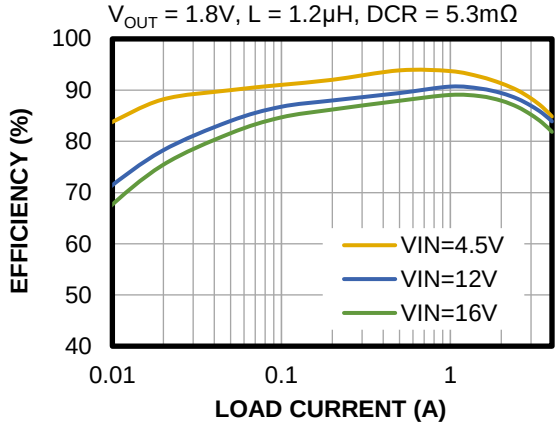
Efficiency vs. Load Current

V_{OUT} = 2.5V, L = 1.5µH, DCR = 6mΩ



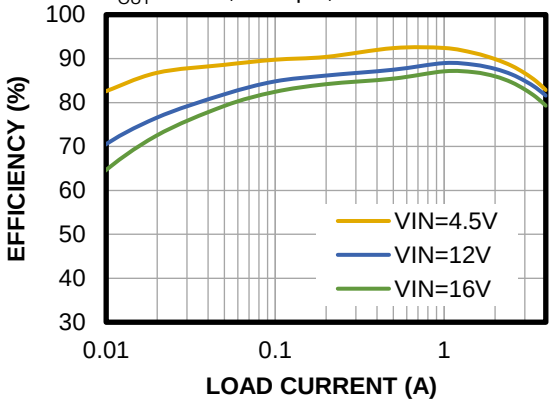
Efficiency vs. Load Current

V_{OUT} = 1.8V, L = 1.2µH, DCR = 5.3mΩ



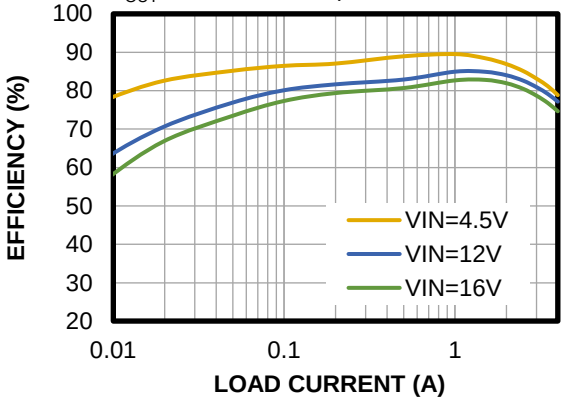
Efficiency vs. Load Current

V_{OUT} = 1.5V, L = 1µH, DCR = 4.3mΩ



Efficiency vs. Load Current

V_{OUT} = 1.2V, L = 0.68µH, DCR = 7.5mΩ



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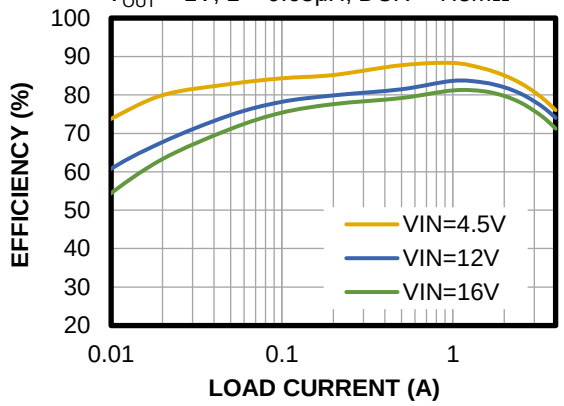
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 1.5µH, T_A = 25°C, unless otherwise noted.

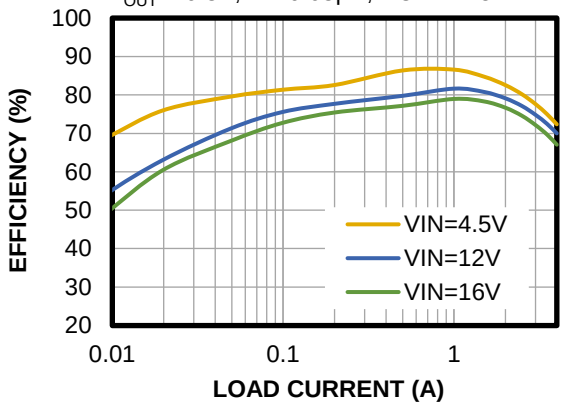
Efficiency vs. Load Current

V_{OUT} = 1V, L = 0.68µH, DCR = 7.5mΩ

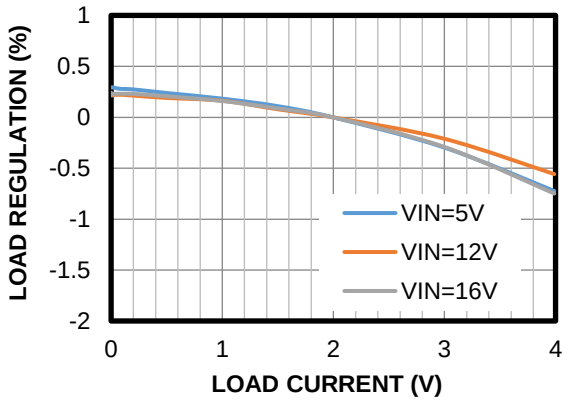


Efficiency vs. Load Current

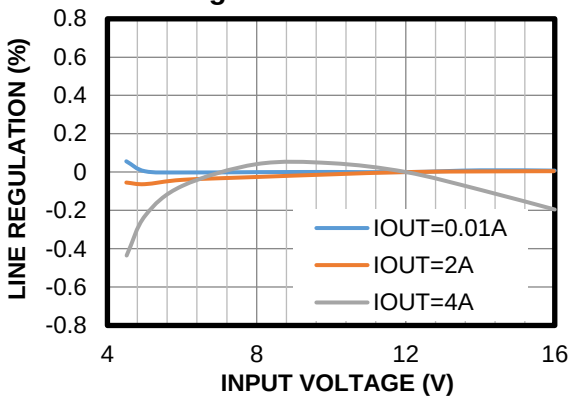
V_{OUT} = 0.8V, L = 0.68µH, DCR = 7.5mΩ



Load Regulation



Line Regulation



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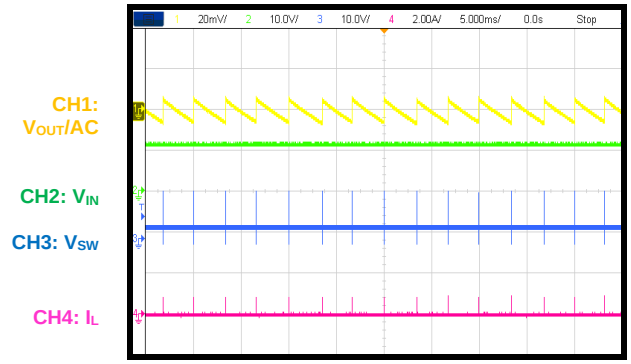
TYPICAL PERFORMANCE CHARACTERISTICS

Performance waveforms are tested on the evaluation board in the Design Example section on page 16. V_{IN} = 12V, V_{OUT} = 3.3V, L = 1.5µH, T_A = 25°C, unless otherwise noted.

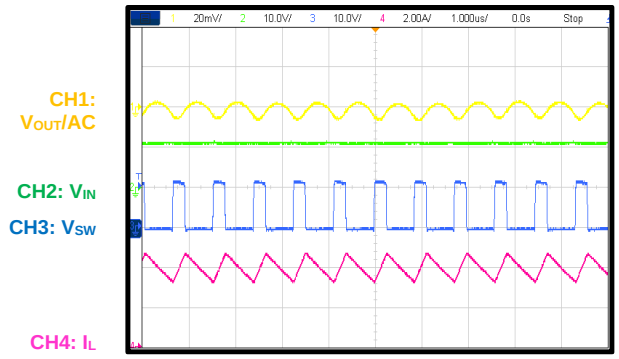
Output Ripple

I_{OUT} = 0A



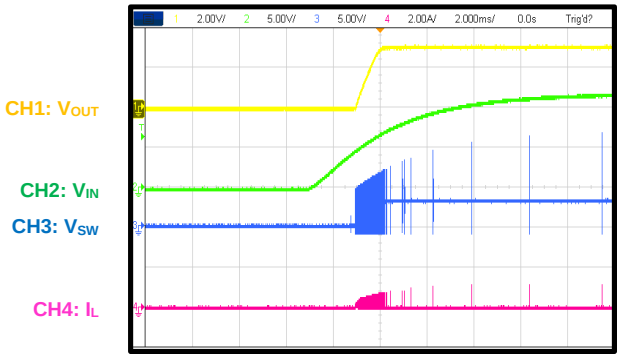
Output Ripple

I_{OUT} = 4A



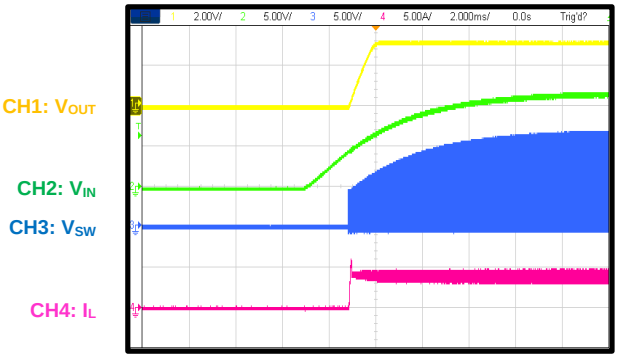
Start-Up through VIN

I_{OUT} = 0A



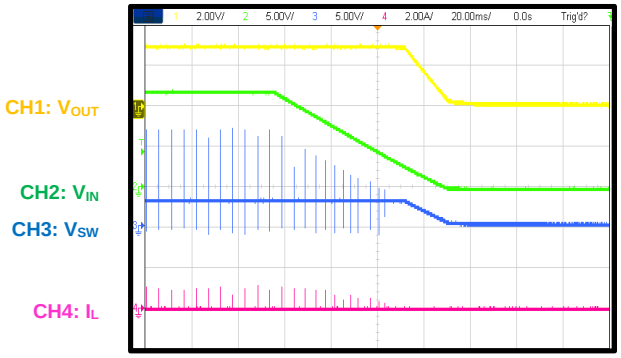
Start-Up through VIN

I_{OUT} = 4A



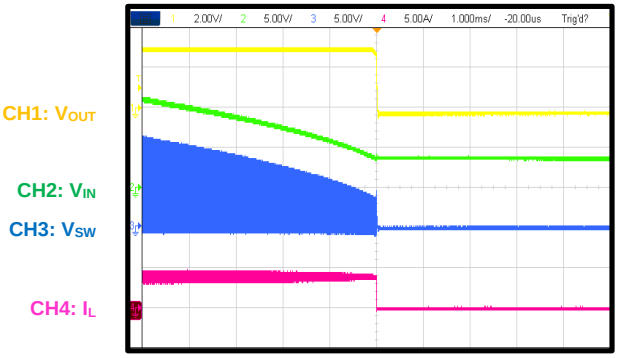
Shutdown through VIN

I_{OUT} = 0A



Shutdown through VIN

I_{OUT} = 4A



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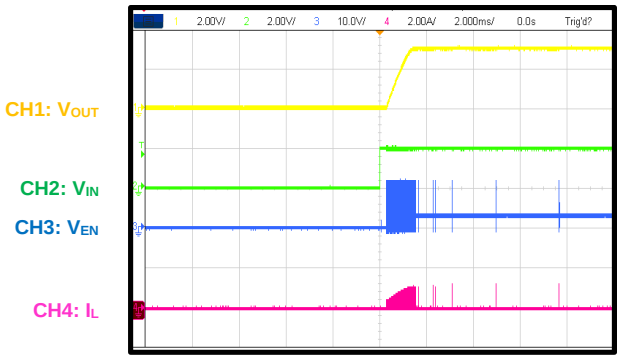
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board in the Design Example section on page 16. V_{IN} = 12V, V_{OUT} = 3.3V, L = 1.5µH, T_A = 25°C, unless otherwise noted.

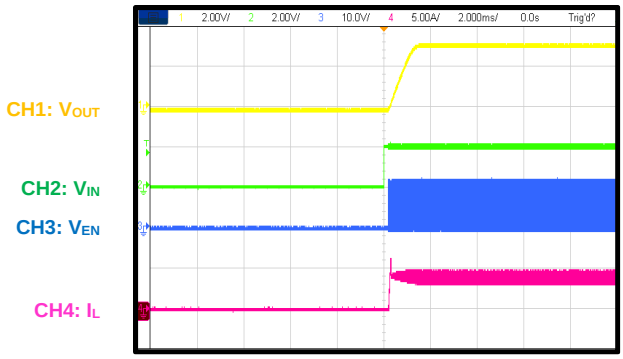
Start-Up through EN

I_{OUT} = 0A



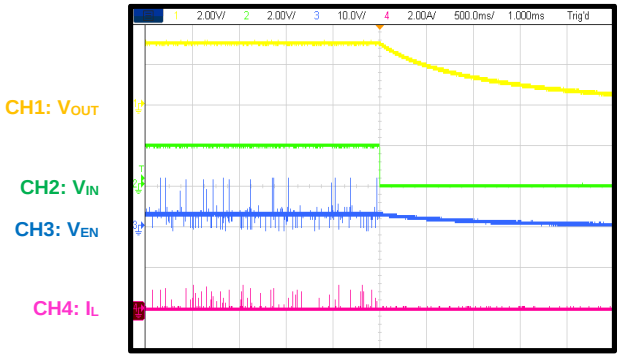
Start-Up through EN

I_{OUT} = 4A



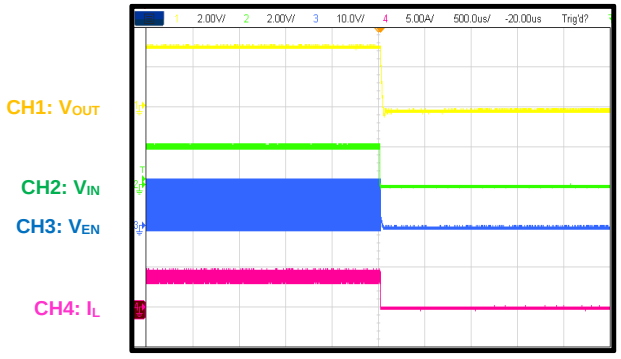
Shutdown through EN

I_{OUT} = 0A



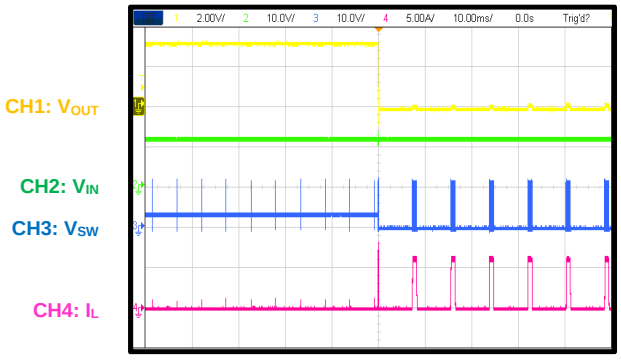
Shutdown through EN

I_{OUT} = 4A



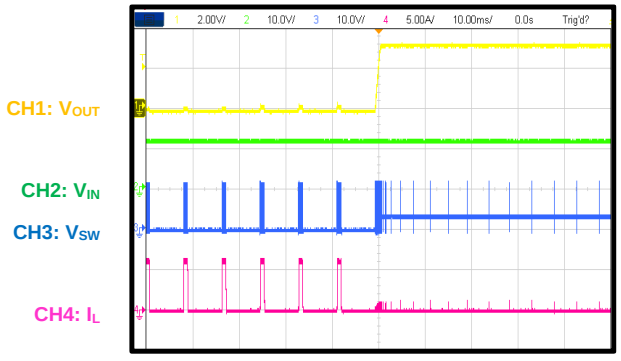
Short-Circuit Entry

I_{OUT} = 0A



Short-Circuit Recovery

I_{OUT} = 0A



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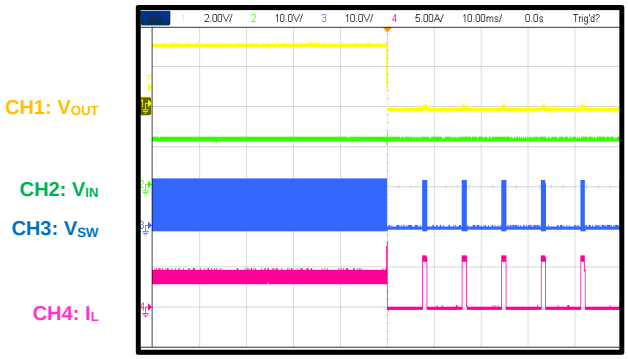
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board in the Design Example section on page 16. V_{IN} = 12V, V_{OUT} = 3.3V, L = 1.5µH, T_A = 25°C, unless otherwise noted.

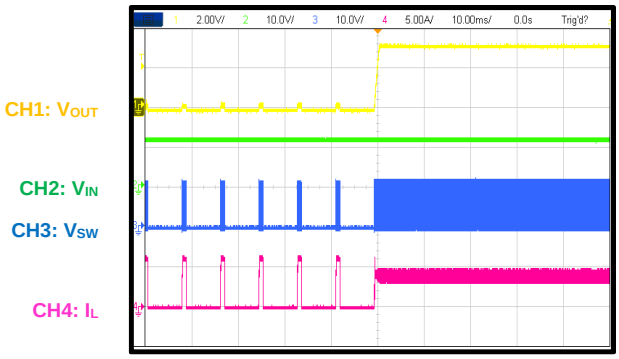
Short-Circuit Entry

I_{OUT} = 4A



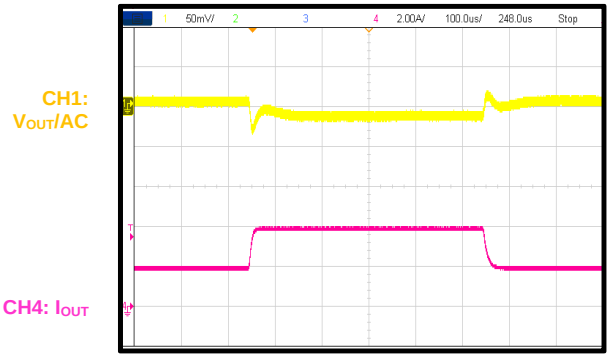
Short-Circuit Recovery

I_{OUT} = 4A



Load Transient Response

I_{OUT} = 2A to 4A, slew rate = 2.5A/µs with e-load



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FUNCTIONAL BLOCK DIAGRAM

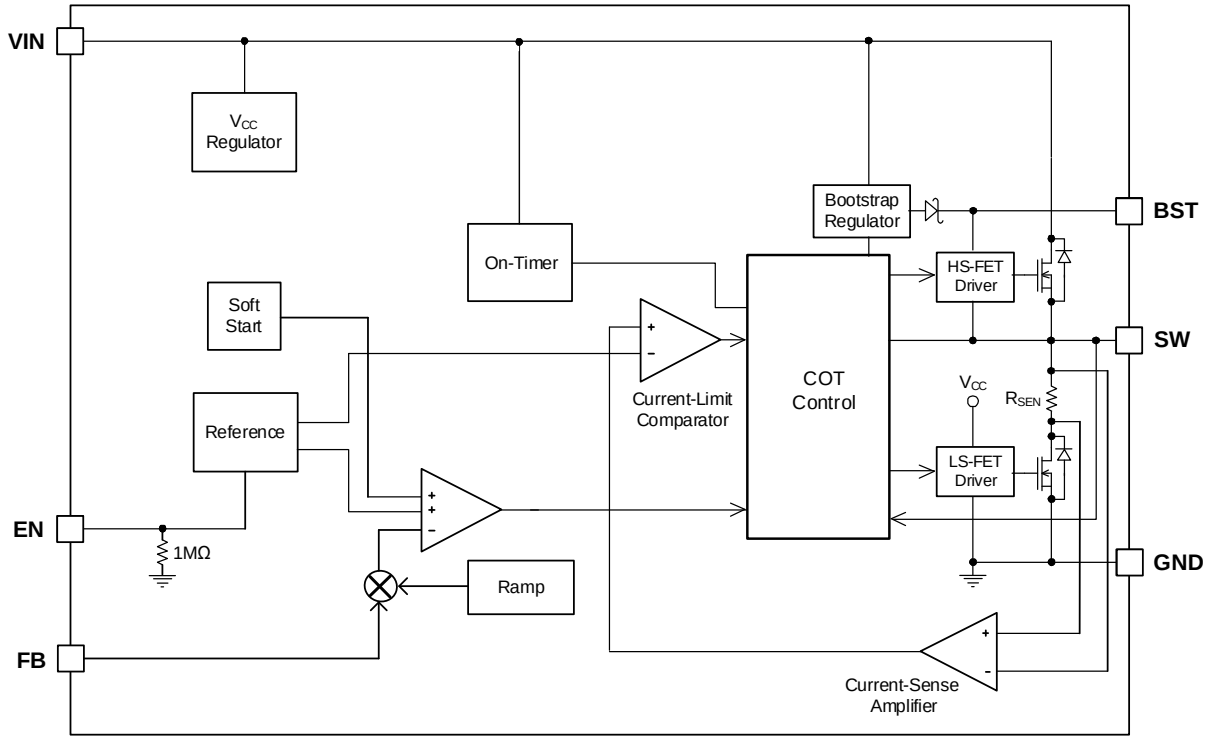

Figure 1: Functional Block Diagram

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OPERATION

Constant-On-Time (COT) Control

The MP1654N employs constant-on-time (COT) control to achieve a fast load transient response. Figure 2 shows the MP1654N's COT control stage.

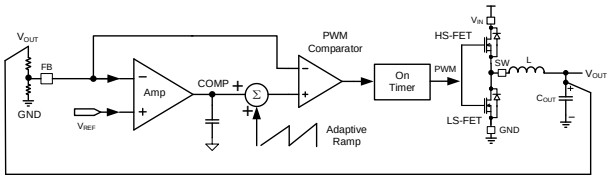

Figure 2: COT Control

The operational amplifier (op amp) corrects any error voltage between the FB pin and the reference voltage (V_{REF}). The MP1654N can use the op amp to provide excellent load regulation across the entire load range in either pulse-frequency modulation (PFM) mode or pulse-width modulation (PWM) mode.

The MP1654N provides internal ramp compensation to support a low-ESR multi-layer ceramic capacitor (MLCC) output capacitor (C_{OUT}) solution. The adaptive internal ramp is optimized to ensure that the MP1654N is stable across the entire operating input voltage (V_{IN}) and output voltage (V_{OUT}) ranges with a properly designed output LC filter.

Pulse-Width Modulation (PWM) Operation

Figure 3 shows how the pulse-width modulation (PWM) signal is generated. The op amp corrects any error between the FB voltage (V_{FB}) and V_{REF}, and generates a fairly smooth DC voltage (V_{COMP}).

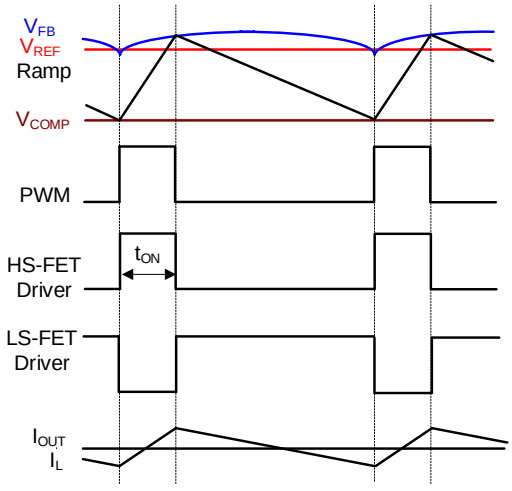

Figure 3: Heavy-Load Operation

The internal ramp is superimposed onto V_{COMP}, which is compared to the FB signal. If the FB signal drops below the superimposed V_{COMP}, then the integrated high-side MOSFET (HS-FET) turns on. The HS-FET remains on for a fixed turn-on time. The fixed on time is determined by V_{IN}, V_{OUT}, and the switching frequency (f_{SW}). After the on period elapses, the HS-FET turns off. It turns on again when V_{FB} drops below the superimposed V_{COMP}. By repeating this operation, the MP1654N regulates V_{OUT}.

To minimize conduction loss, the integrated low-side MOSFET (LS-FET) turns on when the HS-FET is off. A dead short occurs between the VIN and GND pins if the HS-FET and the LS-FET turn on at the same time. This is called shoot-through. To avoid shoot-through, a dead time (DT) is generated internally between the HS-FET off period and the LS-FET on period (and vice versa).

Continuous Conduction Mode (CCM)

Continuous conduction mode (CCM) occurs when the output current (I_{OUT}) is high, and the inductor current (I_L) always exceeds 0A (see Figure 3).

During CCM, f_{SW} is fairly constant. This means that the output voltage ripple (ΔV_{OUT}) remains almost constant across the entire load range.

Power-Save Mode

Under light-load conditions, the MP1654N works in power-save mode (also called PFM mode) to optimize efficiency. If the load decreases, then I_L decreases as well. Once I_L reaches 0A, the MP1654N transitions from CCM to power-save mode.

Figure 4 on page 13 shows power-save mode under light-load conditions. If V_{FB} drops below the superimposed V_{COMP}, then the HS-FET turns on for a fixed interval. When the HS-FET turns off, the LS-FET turns on until I_L reaches 0A. In power-save mode, V_{FB} does not reach the superimposed V_{COMP} when I_L approaches 0A. The LS-FET driver enters tri-state (Hi-Z) once I_L reaches 0A. Then the output capacitors discharge slowly to GND through the LS-FET. Under light-load conditions, the HS-FET does not turn on as frequently in power-save mode

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compared to forced continuous conduction mode (FCCM). As a result, efficiency in power-save mode compared to FCCM.

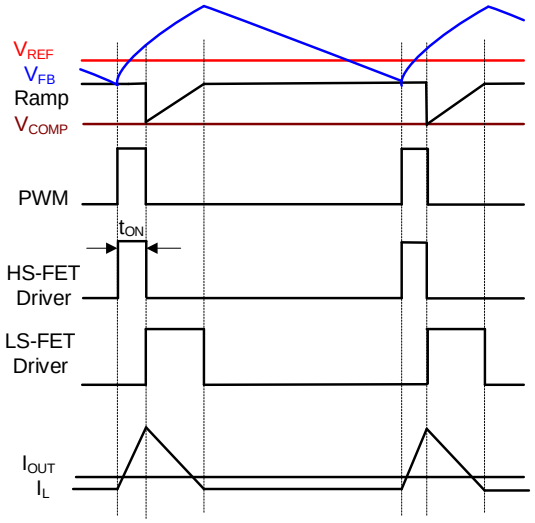

Figure 4: Power-Save Mode at Light Loads

As I_{OUT} increases from light loads, the HS-FET turns on more frequently, which increases f_{SW}. The critical level for I_{OUT} can be estimated with Equation (1):

$$I_{OUT} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times L \times f_{SW} \times V_{IN}} \quad (1)$$

The MP1654N enters CCM once I_{OUT} exceeds its critical level. Afterward, f_{SW} remains fairly constant across the I_{OUT} range.

Enable (EN) Control

EN is a digital control pin that turns the regulator on and off. Pull EN above its rising threshold (V_{EN_RISING}) to turn the regulator on. Pull EN below its falling threshold ($V_{EN_FALLING}$) to turn the regulator off. If EN is floated, the pin is pulled down to GND via an internal 1MΩ resistor. EN can be connected to V_{IN} via a 100kΩ resistor.

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The MP1654N's UVLO comparator monitors the internal regulator's output voltage (V_{CC}). The UVLO rising threshold ($V_{IN_UVLO_RISING}$) is about 4.25V, and the UVLO falling threshold is fixed at 4V.

Internal Soft Start (SS)

Soft start (SS) prevents the converter's V_{OUT} from overshooting during start-up. Once the chip starts up, the internal circuitry generates a soft-start voltage (V_{SS}) that ramps up from 0V to 1.2V. If V_{SS} is below V_{REF}, then V_{SS} overrides V_{REF}, meaning the error amplifier (EA) uses V_{SS} as the reference. If V_{SS} exceeds V_{REF}, then the EA uses V_{REF} as the reference.

Over-Current Protection (OCP) and Short-Circuit Protection (SCP)

The MP1654N provides valley-limit control. The LS-FET monitors the current flowing through the LS-FET. The HS-FET waits until the valley-current limit is removed before turning on again. Meanwhile, V_{OUT} drops until V_{FB} is below the under-voltage (UV) threshold (typically 40% of V_{REF}). If an UV fault is triggered, then the MP1654N enters hiccup mode to restart the part periodically.

During over-current protection (OCP), the device attempts to recover from the over-current (OC) fault with hiccup mode. This means that the chip disables the output power (P_{OUT}) stage, discharges SS, and attempts to soft start again automatically. If the OC condition remains after SS ends, the device repeats this operation cycle until the OC conditions disappears, then the output rises back to the regulation level.

Pre-Biased Start-Up

The MP1654N is designed for monotonic start-up into pre-biased loads. If the output is pre-biased to a certain voltage during start-up, then the IC disables switching for both the HS-FET and LS-FET until V_{SS} exceeds the sensed V_{OUT} at the FB pin. If the BST voltage (V_{BST}) is below its UVLO threshold during start-up, then the LS-FET turns on to allow V_{BST} to be charged through V_{IN}. The LS-FET turns on for very narrow pulses, meaning the drop in the pre-biased level is negligible. Once V_{SS} reaches the pre-biased voltage at the FB pin, the IC enters normal operation.

Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. If the silicon die temperature exceeds 155°C, then the entire chip shuts down.

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If the temperature falls below its lower threshold (typically 135°C), then the chip is enabled again.

Floating Driver and Bootstrap (BST) Charging

An external bootstrap (BST) capacitor (C_{BST}) powers the floating power MOSFET driver. This floating driver has its own UVLO protection. V_{IN} regulates the C_{SBT} voltage internally through D1, M1, R4, C4, the output inductor (L_{OUT}), and Co (see Figure 5). If the difference between V_{IN} and the SW voltage (V_{SW}) exceeds 3.3V, then U2 regulates M1 to maintain a 3.3V V_{BST} across C4. The BST resistor (R4) is recommended to be below 4.7Ω.

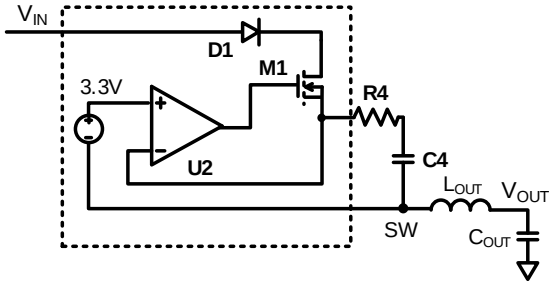

Figure 5: Internal Bootstrap Charger

Start-Up and Shutdown Circuits

If V_{IN} exceeds $V_{IN_UVLO_RISING}$ and the EN voltage (V_{EN}) exceeds its rising threshold (V_{EN_RISING}), then the chip starts up. The reference block starts first, generating a stable reference voltage and current, then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuits.

Three events can shut down the chip: low V_{EN}, low V_{IN}, and thermal shutdown. The shutdown procedure starts by initially blocking the signaling path to avoid any fault triggering. The internal supply rail is then pulled down.

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APPLICATION INFORMATION

Setting the Output Voltage

The external resistor divider sets the output voltage (V_{OUT}). Select a suitable value for R2 since a small R2 leads to considerable quiescent current (I_Q) loss, while a large R2 makes FB noise-sensitive. R2 is recommended be between 5kΩ and 100kΩ. Typically, set the current through R2 to be below 150μA, which achieves a good balance between system stability and no-load loss. R1 can then be calculated with Equation (2):

$$R1 = \frac{V_{OUT} - V_{REF}}{V_{REF}} \times R2 \quad (2)$$

Figure 6 shows the feedback circuit.

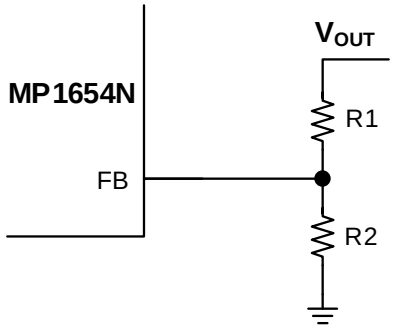

Figure 6: Feedback Network

Table 1 shows the recommended parameters for common output voltages.

Table 1: Parameter Selection for Common Output Voltages (C_{OUT} = 22μF x2) (8)

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	L (μH)
5	40.2	5.49	2.2
3.3	40.2	8.87	1.5
2.5	40.2	12.7	1.5
1.8	40.2	20	1.2
1.5	40.2	26.7	1
1.2	40.2	40.2	0.68
1	20.5	30.9	0.68
0.8	20.5	60.4	0.68

Note:

8) For the detailed design circuit, see the Typical Application Circuits section on page 18.

Selecting the Inductor

MPL **Optimized Performance with MPS Inductor MPL-AL4020 and MPL-AL6050 Series**

An inductor is required to supply constant current to the output load while being driven by the switched input voltage (V_{IN}). A larger-value inductor results in less ripple current and a lower output voltage ripple (ΔV_{OUT}), but also has a larger physical footprint, higher series resistance, and lower saturation current. A good rule for determining the inductance is to design the peak-to-peak ripple current in the inductor to be within the 30% to 60% range of the maximum output current. The inductance (L) can be calculated with Equation (3):

$$L = \frac{V_{OUT}}{f_{SW} \times \Delta I_L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (3)$$

Where ΔI_L is the peak-to-peak inductor ripple current.

The inductor should not saturate under the maximum inductor peak current. The peak inductor current (I_{LP}) can be calculated with Equation (4):

$$I_{LP} = I_{OUT} + \frac{V_{OUT}}{2 \times f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (4)$$

MPS inductors are optimized and tested for use with our complete line of integrated circuits.

Table 2 shows the recommended MPS power inductors, where the part number can be selected based on the design requirements.

Table 2: Power Inductor Selection

Part Number	Inductance	Manufacturer
MPL-AL4020 and MPL-AL6050	0.68μH to 2.2μH	MPS
MPL-AL4020-R68	0.68μH	MPS
MPL-AL6050-1R0	1μH	MPS
MPL-AL6050-1R2	1.2μH	MPS
MPL-AL6050-1R5	1.5μH	MPS
MPL-AL6050-2R2	2.2μH	MPS

For more information, visit the Inductors page on the MPS website.

Selecting the Input Capacitor

The step-down converter has a discontinuous input current (C_{IN}) and requires a capacitor to supply AC current to the converter while maintaining the DC input voltage. For the best results, use ceramic capacitors placed as close to VIN as possible. Capacitors with X5R and

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X7R ceramic dielectrics are recommended because they are fairly stable with temperature fluctuations.

The capacitors must also have a ripple current rating greater than the converter's maximum input ripple current. The input ripple current (I_{CIN}) can be estimated with Equation (5):

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (5)$$

The worst-case condition occurs at V_{IN} = 2 x V_{OUT}, which can be calculated with Equation (6):

$$I_{CIN} = \frac{I_{OUT}}{2} \quad (6)$$

For simplification, choose C_{IN} with an RMS current rating greater than half of the maximum load current.

C_{IN} determines the converter's input voltage ripple. If the system has an input voltage ripple requirement, then select C_{IN} to meet the specifications.

The input voltage ripple (ΔV_{IN}) can be estimated with Equation (7):

$$\Delta V_{IN} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (7)$$

The worst-case condition occurs at V_{IN} = 2 x V_{OUT}, which can be calculated with Equation (8):

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{f_{SW} \times C_{IN}} \quad (8)$$

Selecting the Output Capacitor

An output capacitor (C_{OUT}) is required to maintain the DC output voltage. Ceramic or POSCAP capacitors are recommended. ΔV_{OUT} can be estimated with Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}}) \quad (9)$$

For ceramic capacitors, the capacitance dominates the impedance at the switching frequency (f_{SW}). ΔV_{OUT} is caused mainly by the capacitance. For simplification, ΔV_{OUT} can be estimated with Equation (10):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^2 \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (10)$$

ΔV_{OUT} caused by the ESR is very small.

For POSCAP capacitors, the ESR dominates the impedance at f_{SW}. For simplification, ΔV_{OUT} can be estimated with Equation (11):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (11)$$

A larger C_{OUT} can achieve improved load transient response, but the maximum C_{OUT} must also be considered in the design application. If C_{OUT} is too high, then V_{OUT} cannot reach the design value during the soft-start time (t_{SS}) and fails to regulate. The maximum output capacitance (C_{OUT_MAX}) limit can be calculated with Equation (12):

$$C_{OUT_MAX} = (I_{LIM_AVG} - I_{OUT}) \times t_{SS} / V_{OUT} \quad (12)$$

Where I_{LIM_AVG} is the average start-up current during t_{SS}.

Design Example

Table 3 shows a design example where ceramic capacitors are applied.

Table 3: Design Example

V_{IN}	V_{OUT}	I_{OUT}
12V	3.3V	2A

Figure 9 on page 18 shows the detailed application schematic. See the Typical Performance Characteristics section on page 8 for the typical performance and waveforms. For more device applications, refer to the EVL1654N-TF-00A datasheet.

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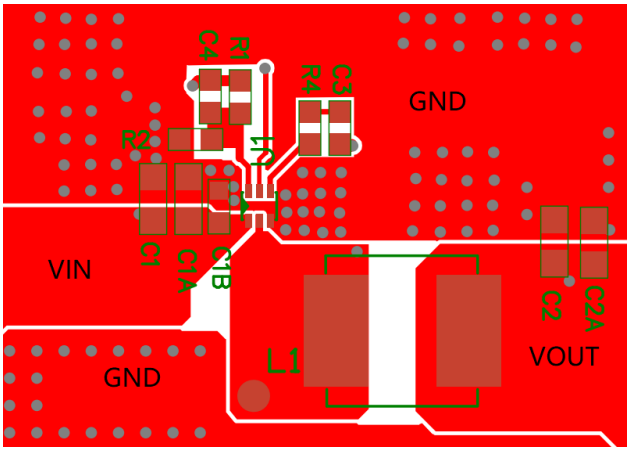
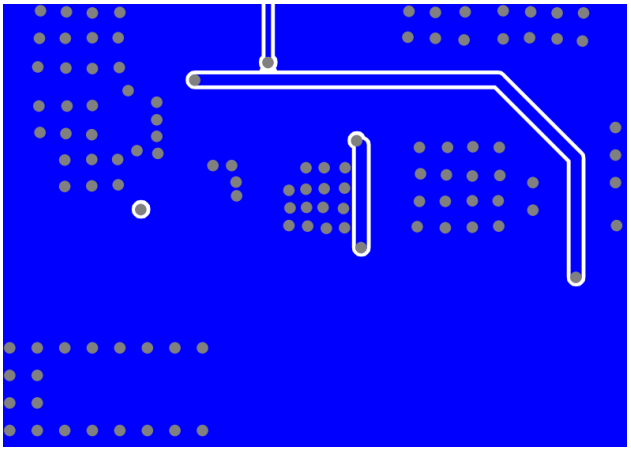
PCB Layout Guidelines

Efficient layout, particularly of the switching power supplies, is critical for stable operation. Poor layout design can result in poor line or load regulation as well as stability issues. For the best results, refer to Figure 7 and follow the guidelines below:

1. Place the high-current paths (GND, VIN, and SW) very close to the device using short, direct, and wide traces.
2. Place C_{IN} as close to VIN and GND as possible.
3. Place the external feedback resistors next to FB.
4. Keep the switching node (SW trace) short and away from the feedback network.
5. Place C_{BST} as close to BST and SW as possible.



Top Layer



Bottom Layer

Figure 7: Recommended PCB Layout

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TYPICAL APPLICATION CIRCUITS

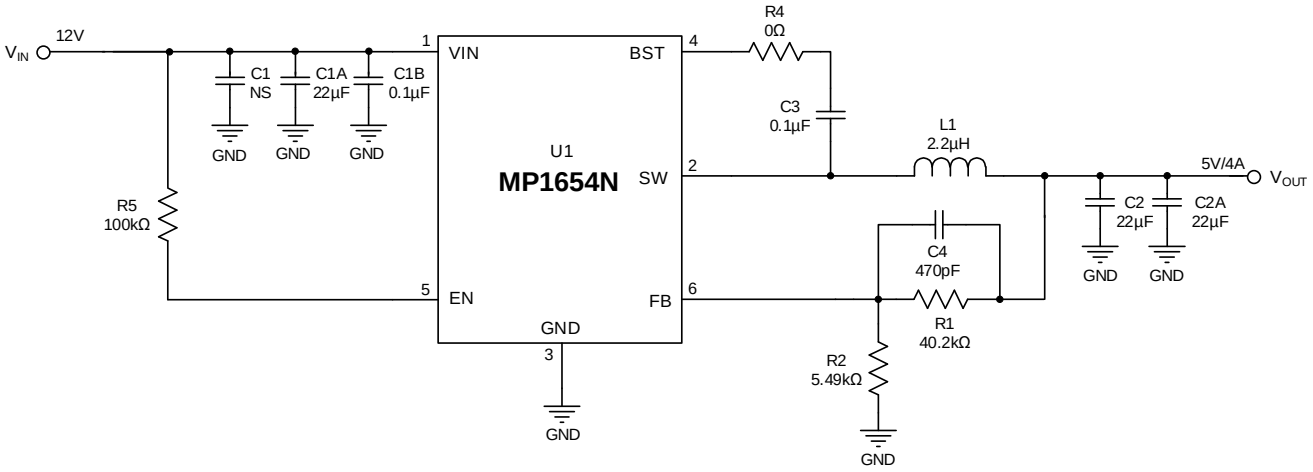

Figure 8: Typical Application Circuit (V_{IN} = 12V, V_{OUT} = 5V/4A)

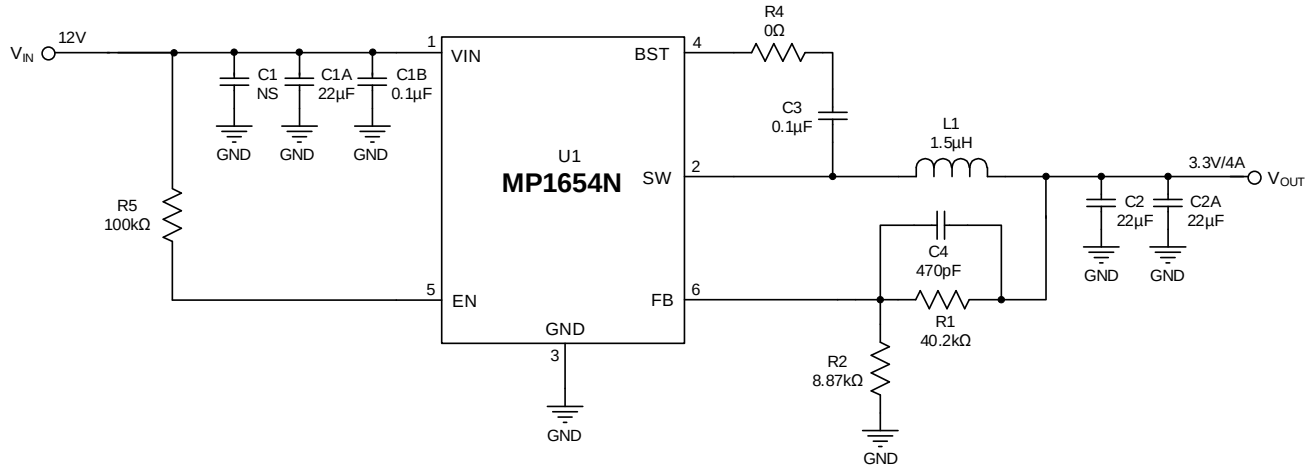

Figure 9: Typical Application Circuit (V_{IN} = 12V, V_{OUT} = 3.3V/4A)

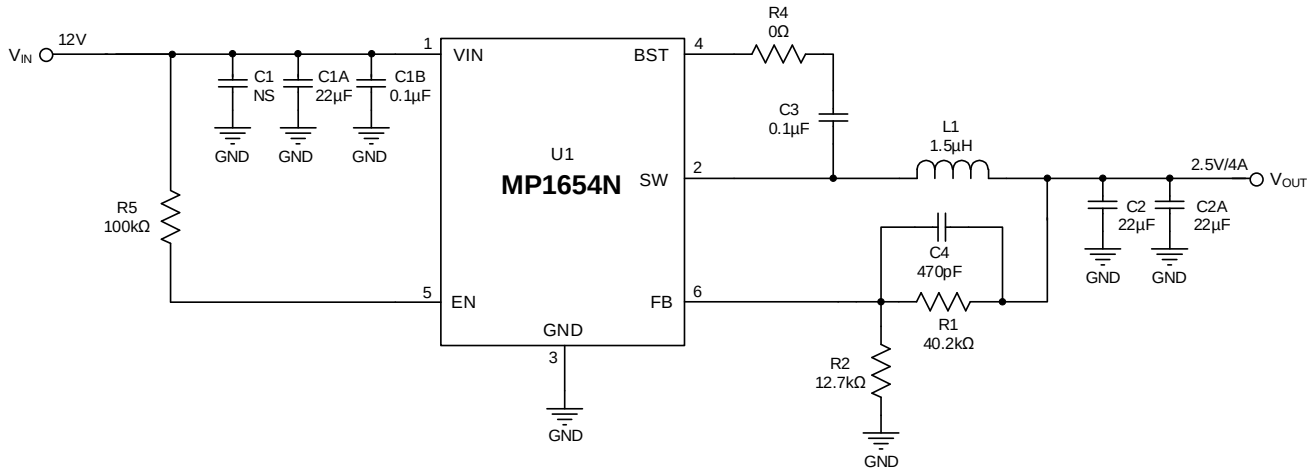

Figure 10: Typical Application Circuit (V_{IN} = 12V, V_{OUT} = 2.5V/4A)

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TYPICAL APPLICATION CIRCUITS *(continued)*

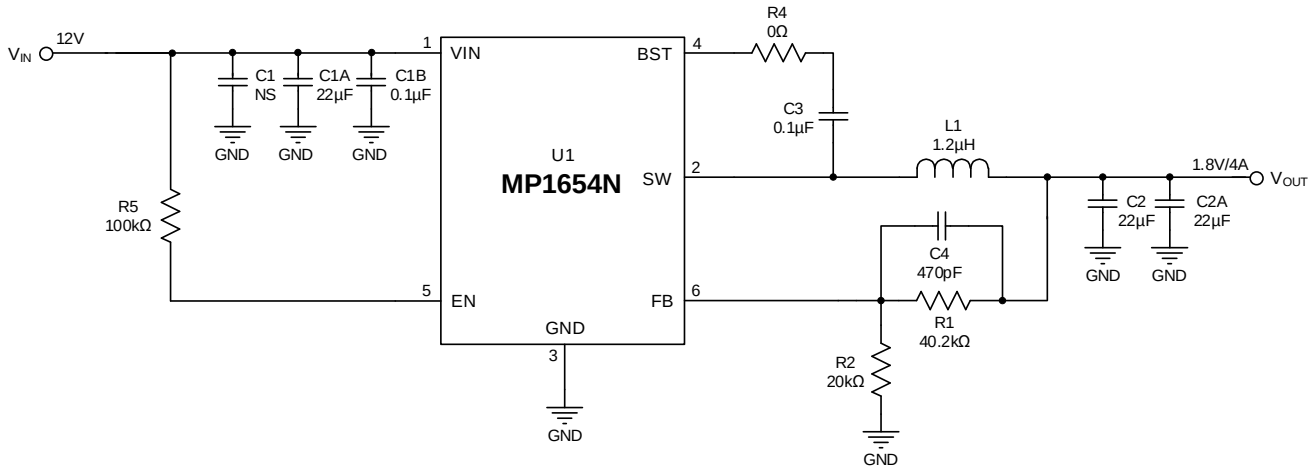

Figure 11: Typical Application Circuit (V_{IN} = 12V, V_{OUT} = 1.8V/4A)

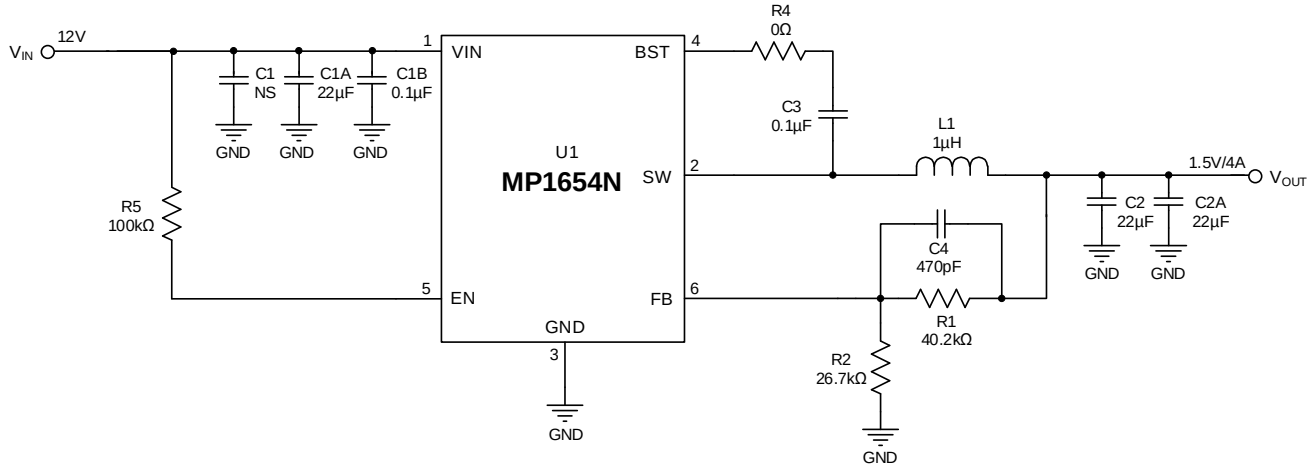

Figure 12: Typical Application Circuit (V_{IN} = 12V, V_{OUT} = 1.5V/4A)

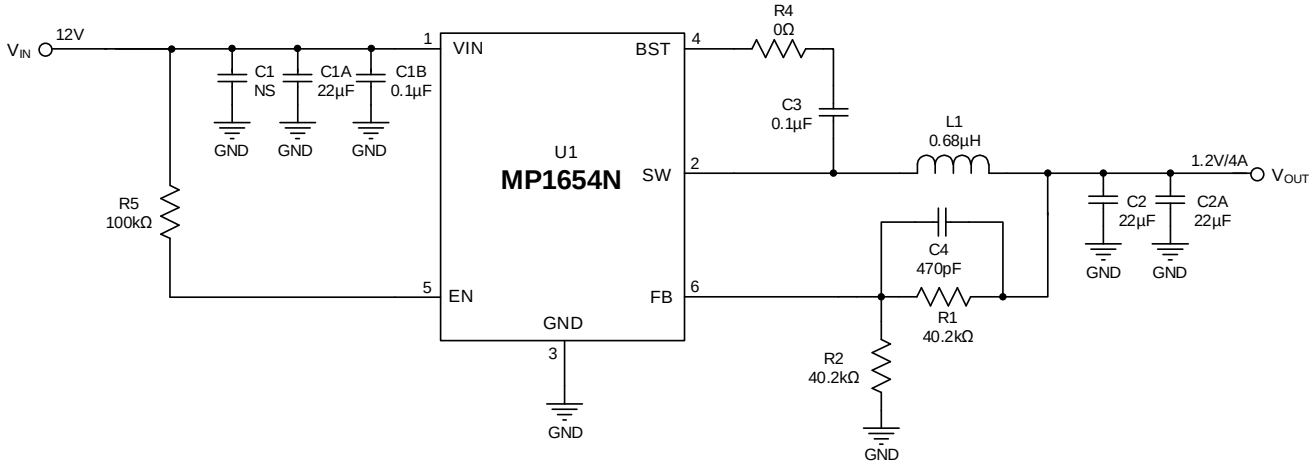

Figure 13: Typical Application Circuit (V_{IN} = 12V, V_{OUT} = 1.2V/4A)

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TYPICAL APPLICATION CIRCUITS *(continued)*

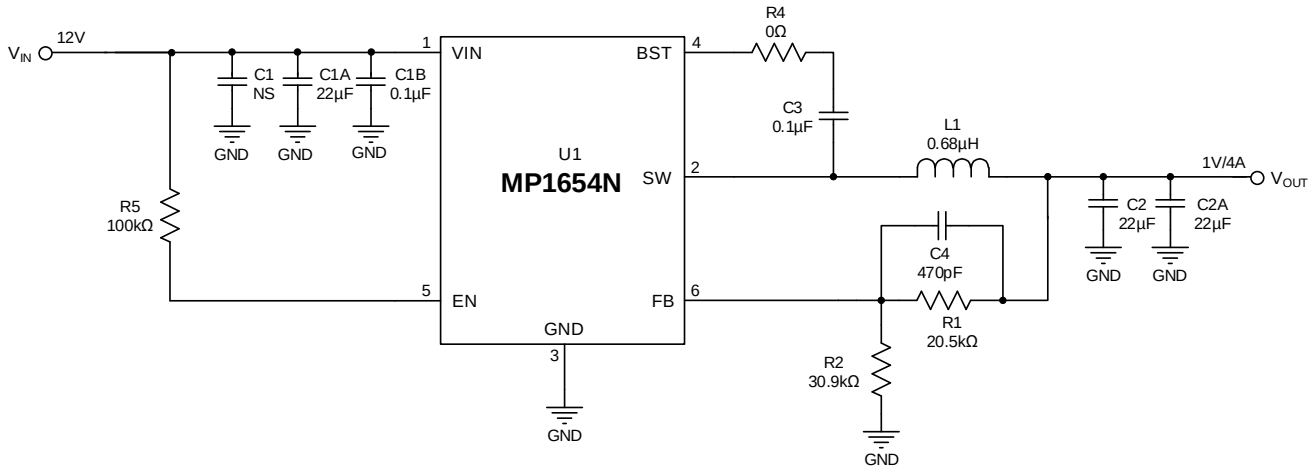

Figure 14: Typical Application Circuit (V_{IN} = 12V, V_{OUT} = 1V/4A)

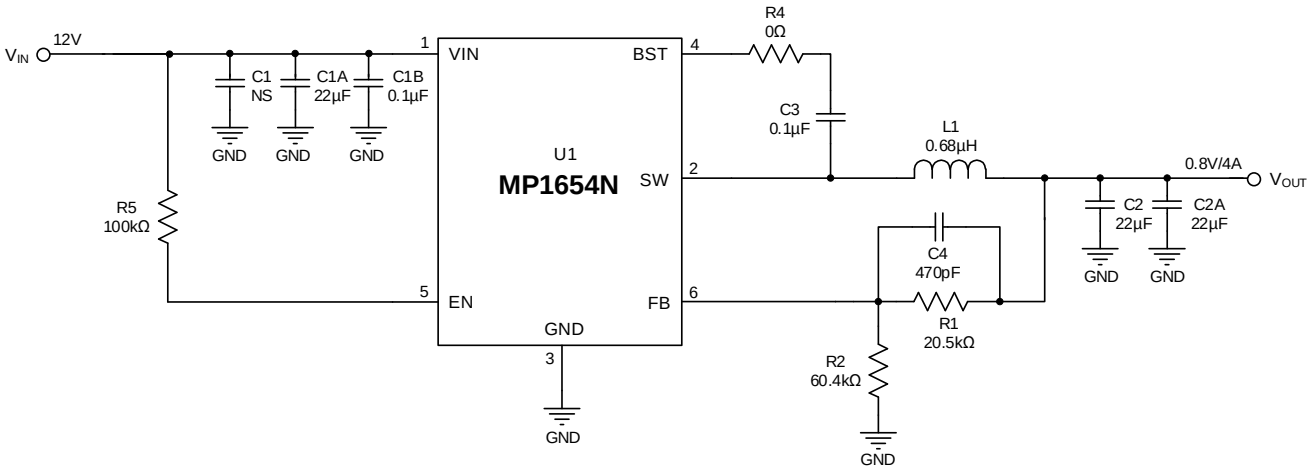

Figure 15: Typical Application Circuit (V_{IN} = 12V, V_{OUT} = 0.8V/4A)

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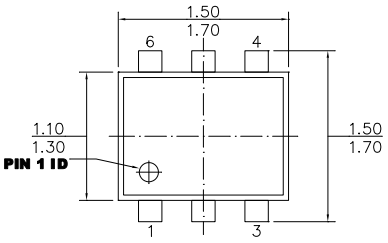
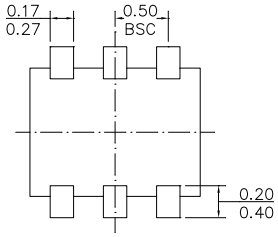
PACKAGE INFORMATION

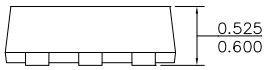
SOT563 (1.6mmx1.6mm)



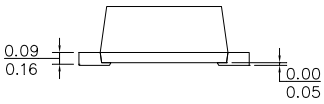
TOP VIEW



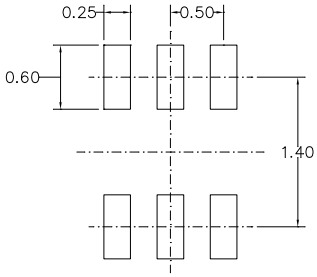
BOTTOM VIEW



FRONT VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING CONFORMS TO JEDEC MO-293, VARIATION UAAD.
6) DRAWING IS NOT TO SCALE.

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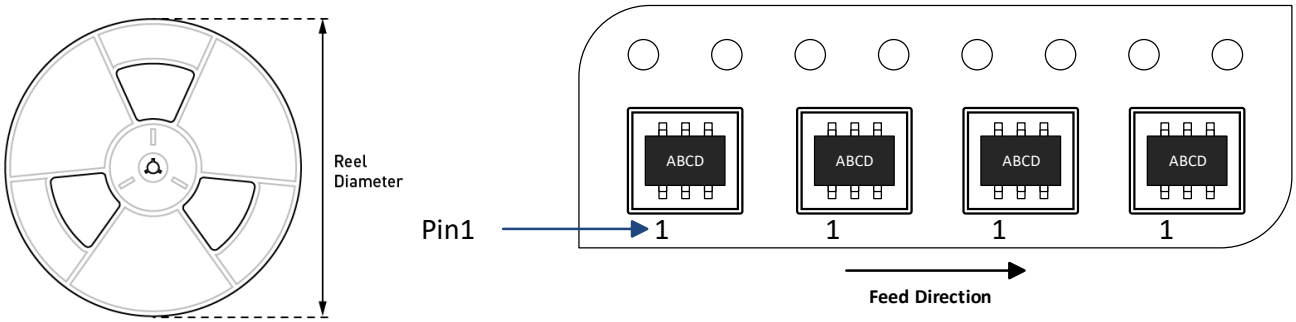
CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP1654NGTF-Z	SOT563 (1.6mmx 1.6mm)	5000	N/A	N/A	7in	8mm	4mm

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REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	8/12/2025	Initial Release	-

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