MEZS7-PDCharger-MP2761

425kHz, Bidirectional PD Charger Solution with Fully Integrated Buck-Boost Charger for 2S to 4S in Series Evaluation Board

DESCRIPTION

The MEZS7-PDCharger-MP2761 is a solution module for dual-role port (DRP) applications using the MP2761 and MPF52002.

The MP2761 is a 4V to 22V input voltage (V_{IN}) buck-boost charger IC designed for battery packs with 2 to 4 cells in series. It also supplies a wide voltage range (5V to 21V) of voltage at the IN pin in source mode, which is compliant with USB power delivery (PD). It also has an output current limit with a high resolution in source mode.

The MPF52002 is a highly integrated USB PD controller for DRP port, with a 32-bit ARM Cortex-M0 microcontroller unit (MCU). It supports automatic DRP toggling for DRP applications, and it is compliant with PD3.1 specifications. For source mode, the MPF52002 supports PD3.1, as well as BC1.2, Apple divider mode, Huawei FCP/SCP, and QC2.0/3.0.

The MEZS7-PDCharger-MP2761 contains a DRP USB Type-C port, supporting PD3.1 and BC1.2 protocols. When an adapter is inserted, the port acts as a sink port to charge the battery with a maximum 6A charge current. When a load is inserted, the port acts as a source port to power the USB VBUS from the battery.

PERFORMANCE SUMMARY (1)

Specifications are at T_A = 25°C, unless otherwise noted.

Parameters	Conditions	Default Value
Sink Mode		
Input voltage (V_{IN}) range		4V to 22V
Input current (I_{IN}) limit		Up to 5A
Battery charge regulation voltage (V_{BATT_REG}) (2)		8.4V
Fast charge current (2)	V_{IN} = 9V to 20V	3A
Charge typical efficiency	V_{IN} = 20V, V_{BATT} = 8V, I_{CC} = 3A	92.2%
Source Mode		
Battery voltage range		Up to 18.72V
Output voltage in source mode (V_{IN_SRC}) (3)		5V to 21V
Default PDO output (2)		5V/3A, 9V/3A, 15V/1.8A, 20V/1.35A, 5V to 5.9V/3A, 5V to 11V/3A, 5V to 16V/1.8A
Source mode typical efficiency	V_{BATT} = 8V, V_{IN_SRC} = 9V, I_{IN_SRC} = 2.6A	93.6%

Notes:

1) Refer to the MP2761 datasheet for details.
2) These items can be configured by the MPF52002 via the I^2C interface.
3) These items are configured by the MPF52002 automatically, according to the protocol.

MPL Optimized Performance with MPS Inductor MPL-AL5030 Series

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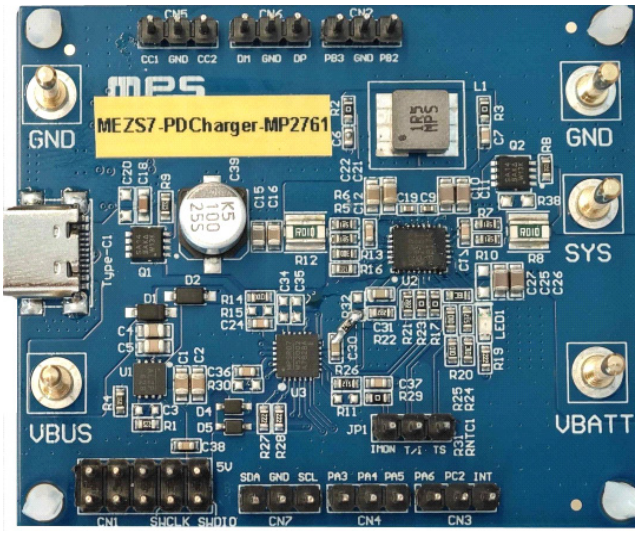
EVALUATION BOARD



LxWxH (6cmx5cmx2.1cm)

Board Number	MPS IC Number
MEZS7-PDCharger-MP2761	MPF52002GRE-0027
	MP2761GVT-0000

Table 1: Battery Cell Number and V_{SYS_MIN} Setting (4)

Cell Number	V_{SYS_MIN}	PB2	PB3
2-cell (default)	6.2V	1: Float or high	1: Float or high
3-cell	9V	0: Short to GND	1: Float or high
4-cell	12V	1: Float or high	0: Short to GND

Note:

4) Set PB2 and PB3 to configure the cell number and V_{SYS_MIN} before charging a real battery.

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QUICK START GUIDE

The MEZS7-PDCharger-MP2761 is a 2-cell to 4-cell series power delivery (PD) charger module using the MP2761 and MPF52002. It is a reference design for PD applications and includes a DRP USB Type-C port. The charge current is preset to 3A, and the charge-full voltage is preset to 8.4V for a 2-cell series Li-ion battery. In reverse source mode, the output is preset to 5V/3A or 27W PD. All the charging/discharging parameters are set by the MPF52002.

The user can download their own charge parameter settings to the MPF52002's volatile memory via the I^2C after start-up. The user can download these parameters to the MPF52002's non-volatile memory (NVM), which is not reset even if the part completely powers off.

Follow the steps below to prepare the battery and load connection for testing:

1. Connect the battery terminals to:
   a. Positive (+): VBATT
   b. Negative (-): GND

   If using a battery simulator, preset the battery voltage, then turn it off. Connect the battery simulator output terminals to:

   a. Positive (+): VBATT
   b. Negative (-): GND
2. Ensure the battery voltage is present (if using a battery simulator, turn the simulator on).
3. Connect the system load terminals to:
   a. Positive (+): SYS
   b. Negative (-): GND

Before adapter plug-in, ensure that the PB2 and PB3 settings are correct (see Table 1 on page 2). Otherwise, the system load and battery may be damaged.

Sink Mode

Connect the USB Type-C port to an adapter with a USB Type-C to Type-C or Type-A to Type-C cable. The MP2761's I_{IN_LIM} and the adapter's output voltage is set according to the negotiation result between the adapter and board. Then charger operation starts.

The default firmware of the MPF52002 on this evaluation board supports the following protocols in sink mode:

- PD3.1
- For a non-PD adapter, the bus voltage (V_{BUS}) is 5V. The default input current (I_{IN}) limit is 900mA. If there is a Rp on source CC termination, then I_{IN_LIM} can rise to 1.5A or 3A, according to the Rp value.

The MPF52002 automatically requests the maximum input power, according to the adapter's protocol.

The MPF52002 sends an I^2C command to the MP2761, and then the MP2761 charges the battery. For 2-cell applications, the default minimum system voltage (V_{SYS_MIN}) is 6.2V, and the default battery-full regulation voltage is 8.4V. The CC charge current limit is set to 3A by default.

If the input power is sufficiently high, the charge current is 3A by default. The real charge current may be limited by the input power limit if the input power is not sufficiently high. If the maximum adapter power is below the maximum charging power rating, the input current limit loop will adjust the charge current to avoid overloading the source/adapter.

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Figure 1 shows the set-up for sink mode.

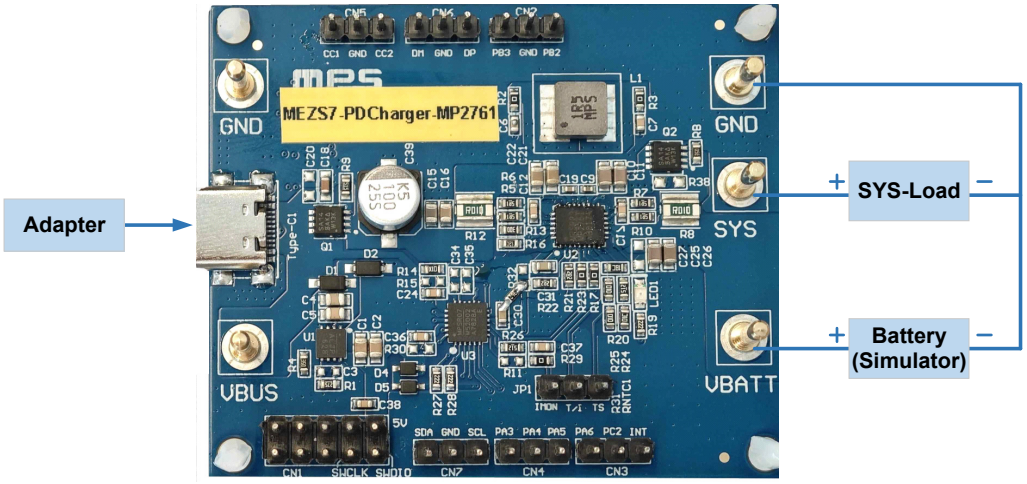

Figure 1: Sink Mode Set-Up

Source Mode

Connect the devices to the USB Type-C port with a USB Type-C to Type-C, Type-C to micro-B, or Type-C to lighting cable. Source mode can start automatically and provide the proper voltage to devices as requested.

The default firmware for the MPF52002 on this evaluation board supports the following protocols in source mode:

- PD3.1
- DCP
- Apple mode

VBUS should start up automatically at the default voltage set by the PD protocol sniffer or mobile device. The PD protocol sniffer can select different PDO outputs.

The default PD output power is 27W.The battery discharge current limit is 6.4A.

Figure 2 shows the set-up for source mode.

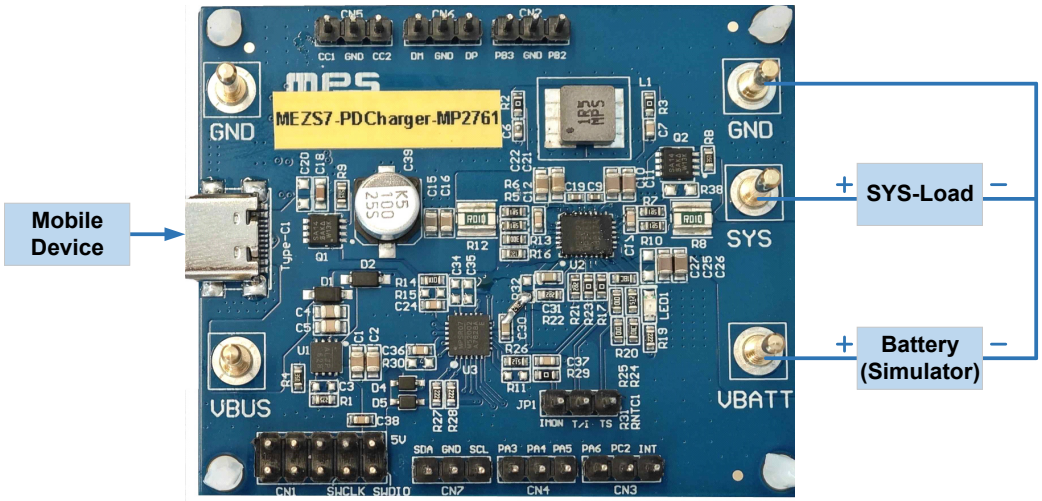

Figure 2: Source Mode Set-Up

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I²C Slave Function Description

The MP2761 and MPF52002 can be controlled or monitored via the I²C between the MPF52002 and I²C master (see Figure 3). The master should be connected to the MPF52002 through the I²C (PB6 and PB7) instead of the MP2761. The MPF52002 periodically reads the MP2761's charge parameters and alert status, then updates the information to the I²C slave registers. The master can also send certain I²C commands to the MP2761 through the MPF52002.

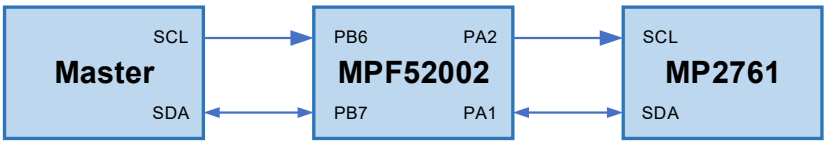

Figure 3: MPF52002 I²C Slave Diagram Block

Hardware Set-Up for I²C Connection

The MPF52002 enters a deep sleep status to save power when the device is only using a battery, and I²C function is disabled. Before starting I²C communication, there are two methods to make the MPF52002 and I²C slave function wake up, described below.

- Short PB1 (INT pin in CN3) to GND in only battery mode.
- A USB Type-C device or adapter is connected to the USB Type-C port.

After communication wakes up, connect the PC and this evaluation board with dongle (the EVKT-USBI2C-02 communication interface). The I²C's SCL should be connected on PB6, which has a SWDIO silkscreen print. The I²C's SDA should be connected on PB7, which has a SWCLK silkscreen print (see Figure 4).

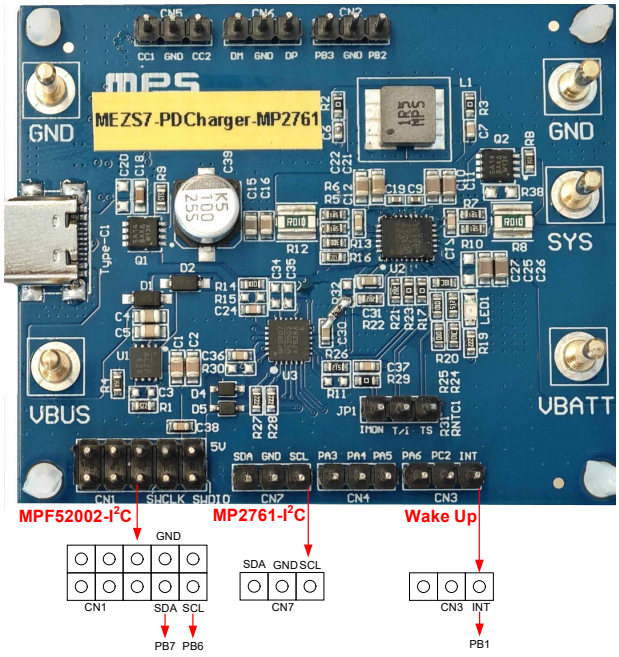

Figure 4: Hardware Connection for I²C Communication

Time Requirements for the I²C Master

- The master SCL clock frequency is 400kHz (fast mode), compliant with a 100kHz to 400kHz clock.
- Read or write 1 byte in every command. Does not support reading/writing multiple bytes.
- A 10ms (or longer) delay between two I²C commands is recommended.

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I²C SLAVE REGISTER MAP (5) (6)

Addr	Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0x00	MPF52002_CHIP_ID	R	MPF52002_CHIP_ID							
0x01	FIRMWARE_ID	R	FIRMWARE_REV							
0x02	PD_CONTROL	R/W	SEND_REQUEST	SEND_PR_SWAP	RESERVED		SEND_SCR_CAP	SEND_HDRST	RESERVED	ENABLE_CHARGER
0x03	PD_STATUS	R	RESERVED		CABLE_INFO		USB_ROLE_INFO		SOURCE_MODE	SINK_MODE
0x04	PD_FAULT_STATUS	R	RESERVED					OTP	OVP	OCP
0x05	PD_REQUEST_OBJ	R/W	RESERVED					REQUEST_OBJ		
0x06	REQUESTED_APDO_VOL	R/W	SNK request adapter's ADPO voltage (100mV/bit)							
0x07	SUFFIX_CODE_ID	R	Stores the suffix code (e.g. 0x17 means the suffix code is "0017").							
0x08	VBATT_PRE	R/W	RESERVED							CHARGER_VBATT_PRE
0x09	WARM_ACT	R/W	RESERVED						CHARGER_WARM_ACT	
0x0A	COOL_ACT	R/W	RESERVED						CHARGER_COOL_ACT	
0x0B	JEITA_VSET	R/W	RESERVED			CHARGER_JEITA_VSET				
0x0C	JEITA_ISET	R/W	RESERVED						CHARGER_JEITA_ISET	
0x0D	NTC_THRESHOLD	R/W	CHARGER_V_HOT		CHARGER_V_WARM		CHARGER_V_COOL		CHARGER_V_COLD	
0x11	ADC_EN	R/W	RESERVED							CHARGER_ADC_EN
0x12	CHARGE TIMER	R/W	RESERVED						CHARGER_CHARGE_TIMER	
0x15	CHARGER_BATT_CELL_NUMBER	R	RESERVED					CHARGER_BATT_CELL_NUMBER		
0x16	CHARGER_STATUS_0_H	R	CHARGER_STATUS_0 (Bits[15:8])							
0x17	CHARGER_STATUS_0_L	R	CHARGER_STATUS_0 (Bits[7:0])							
0x18	CHARGER_STATUS_1_H	R	CHARGER_STATUS_1 (Bits[15:8])							
0x19	CHARGER_STATUS_1_L	R	CHARGER_STATUS_1 (Bits[7:0])							
0x23	CHARGER_ADC_VIN_H	R	RESERVED						CHARGER_ADC_VIN (Bits[9:8])	
0x24	CHARGER_ADC_VIN_L	R	CHARGER_ADC_VIN (Bits[7:0])							
0x25	CHARGER_ADC_IIN_H	R	RESERVED						CHARGER_ADC_IIN (Bits[9:8])	
0X26	CHARGER_ADC_IIN_L	R	CHARGER_ADC_IIN (Bits[7:0])							
0x27	CHARGER_ADC_VBATT_H	R	RESERVED						CHARGER_ADC_VBATT (Bits[9:8])	
0X28	CHARGER_ADC_VBATT_L	R	CHARGER_ADC_VBATT (Bits[7:0])							
0x29	CHARGER_ADC_IBATT_H	R	RESERVED						CHARGER_ADC_IBATT (Bits[9:8])	
0x2A	CHARGER_ADC_IBATT_L	R	CHARGER_ADC_IBATT (Bits[7:0])							
0x2B	CHARGER_ADC_NTC_H	R	RESERVED						CHARGER_ADC_NTC (Bits[9:8])	
0x2C	CHARGER_ADC_NTC_L	R	CHARGER_ADC_NTC (Bits[7:0])							
0x2D	CHARGER_ADC_TS_H	R	RESERVED						CHARGER_ADC_TS (Bits[9:8])	
0x2E	CHARGER_ADC_TS_L	R	CHARGER_ADC_TS (Bits[7:0])							
0x2F	CHARGER_ADC_TJ_H	R	RESERVED						CHARGER_ADC_TJ (Bits[9:8])	
0x30	CHARGER_ADC_TJ_L	R	CHARGER_ADC_TJ (Bits[7:0])							
0x33	CHARGER_ADC_VIN_SRC_H	R	RESERVED						CHARGER_ADC_VIN_SRC (Bits[9:8])	
0x34	CHARGER_ADC_VIN_SRC_L	R	CHARGER_ADC_VIN_SRC (Bits[7:0])							
0x35	CHARGER_ADC_IIN_SRC_H	R	RESERVED						CHARGER_ADC_IIN_SRC (Bits[9:8])	
0x36	CHARGER_ADC_IIN_SRC	R	CHARGER_ADC_IIN_SRC (Bits[7:0])							
0x37	IIN_LIM	R/W	Input current limit in charge mode. 50mA/bit.							
0x38	ICHG_CLT1	R/W	Trickle-charge current set-up. 50mA/bit				Pre-charge current set-up. 100mA/bit.			
0x39	ICHG_CLT2	R/W	Terminal current set-up. 50mA/bit.				RESERVED			
0x3A	CC CHARGE	R/W	CC charge set-up. 50mA/bit.							
0x3B	VBAT_REG	R/W	RESERVED	Battery full voltage setting per cell, 3.4V offset, 10mV/bit. The total battery full voltage = BATT_NUMBER (0x15) x (3400mV+ 10mV x (0x3B)), 3.4V to 4.68V is available.						
0x40	CH1: PDO_EN	R/W	RESERVED		PDO7_EN	PDO6_EN	PDO5_EN	PDO4_EN	PDO3_EN	PDO2_EN
0x41	CH1: PDO_TYPE	R/W	RESERVED		PDO7_TYPE	PDO6_TYPE	PDO5_TYPE	PDO4_TYPE	PDO3_TYPE	PDO2_TYPE
0x42	CH1: PDO_V1	R	PDO1_VOLTAGE_SETTING							
0x43	CH1: PDO_I1	R/W	PDO1_CURRENT_SETTING							

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I²C SLAVE REGISTER MAP *(continued)* (5) (6)

Addr	Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0x44	CH1: PDO_V2_L	R/W	PDO2_VOLTAGE_SETTING_L							
0x45	CH1: PDO_V2_H	R/W	PDO2_VOLTAGE_SETTING_H							
0x46	CH1: PDO_I2	R/W	PDO2_CURRENT_SETTING							
0x47	CH1: PDO_V3_L	R/W	PDO3_VOLTAGE_SETTING_L							
0x48	CH1: PDO_V3_H	R/W	PDO3_VOLTAGE_SETTING_H							
0x49	CH1: PDO_I3	R/W	PDO3_CURRENT_SETTING							
0x4A	CH1: PDO_V4_L	R/W	PDO4_VOLTAGE_SETTING_L							
0x4B	CH1: PDO_V4_H	R/W	PDO4_VOLTAGE_SETTING_H							
0x4C	CH1: PDO_I4	R/W	PDO4_CURRENT_SETTING							
0x4D	CH1: PDO_V5_L	R/W	PDO5_VOLTAGE_SETTING_L							
0x4E	CH1: PDO_V5_H	R/W	PDO5_VOLTAGE_SETTING_H							
0x4F	CH1: PDO_I5	R/W	PDO5_CURRENT_SETTING							
0x50	CH1: PDO_V6_L	R/W	PDO6_VOLTAGE_SETTING_L							
0x51	CH1: PDO_V6_H	R/W	PDO6_VOLTAGE_SETTING_H							
0x52	CH1: PDO_I6	R/W	PDO6_CURRENT_SETTING							
0x53	CH1: PDO_V7_L	R/W	PDO7_VOLTAGE_SETTING_L							
0x54	CH1: PDO_V7_H	R/W	PDO7_VOLTAGE_SETTING_H							
0x55	CH1: PDO_I7	R/W	PDO7_CURRENT_SETTING							
0x60	ADAPTER_PDO_ NUMBER	R	RESERVED					OBJ_NUMBER		
0x61	ADAPTER_PDO_TYPE	R	RESERVED		PDO7_ TYPE	PDO6_ TYPE	PDO5_ TYPE	PDO4_ TYPE	PDO3_ TYPE	PDO2_ TYPE
0x62	ADAPTER_PDO_V1	R	ADAPTER_PDO1_VOLTAGE							
0x63	ADAPTER_PDO_I1	R	ADAPTER_PDO1_CURRENT							
0x64	ADAPTER_PDO_V2_L	R	ADAPTER_PDO2_VOLTAGE_L							
0x65	ADAPTER_PDO_V2_H	R	ADAPTER_PDO2_VOLTAGE_H							
0x66	ADAPTER_PDO_I2	R	ADAPTER_PDO2_CURRENT							
0x67	ADAPTER_PDO_V3_L	R	ADAPTER_PDO3_VOLTAGE_L							
0x68	ADAPTER_PDO_V3_H	R	ADAPTER_PDO3_VOLTAGE_H							
0x69	ADAPTER_PDO_I3	R	ADAPTER_PDO3_CURRENT							
0x6A	ADAPTER_PDO_V4_L	R	ADAPTER_PDO4_VOLTAGE_L							
0x6A	ADAPTER_PDO_V4_H	R	ADAPTER_PDO4_VOLTAGE_H							
0x6A	ADAPTER_PDO_I4	R	ADAPTER_PDO4_CURRENT							
0x6A	ADAPTER_PDO_V5_L	R	ADAPTER_PDO5_VOLTAGE_L							
0x6A	ADAPTER_PDO_V5_H	R	ADAPTER_PDO5_VOLTAGE_H							
0x6A	ADAPTER_PDO_I5	R	ADAPTER_PDO5_CURRENT							
0x70	ADAPTER_PDO_V6_L	R	ADAPTER_PDO6_VOLTAGE_L							
0x71	ADAPTER_PDO_V6_H	R	ADAPTER_PDO6_VOLTAGE_H							
0x72	ADAPTER_PDO_I6	R	ADAPTER_PDO6_CURRENT							
0x73	ADAPTER_PDO_V7_L	R	ADAPTER_PDO7_VOLTAGE_L							
0x74	ADAPTER_PDO_V7_H	R	ADAPTER_PDO7_VOLTAGE_H							
0x75	ADAPTER_PDO_I7	R	ADAPTER_PDO7_CURRENT							
0xf0	MTP_STATUS	R	RESERVED							MTP done flag.
0xf1	MTP_PASSWORD	R/W	Write ”0x05,” ”0xaa,” “0xbc,” or “0xbd” to start MTP operation. If an incorrect password is entered, MTP operation does not start.							
0xf2	CONFIGURED_MTP_ REG	R	RESERVED							Configured MTP_REG.
0xf3	RESTORE_DEFAULT_ CONFIG	R/W	RESERVED							Restores defaults.

Notes:

5) These registers are configurable. Contact an MPS FAE for more information.
6) The detailed register description is included in the MPF52002-0027 suffix code configuration table. Contact an MPS FAE to obtain the table.

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QUICK START GUIDE FOR THE MPF52002'S GUI

1. Obtain Virtual Bench Pro 4.0 from the MPS website.
2. Connect the GUI and evaluation board by following the steps in the Hardware Set-Up for I²C Connection section on page 5.
3. Open the VBP4.0 GUI, create a new project, and add the MPF52002-0027 (see Figure 5).

Figure 5: Start the MPF52002 GUI

To change the volatile memory data, modify the option on the GUI, then click "Write RAM" to make the modification valid on the MPF52002 (see Figure 6). The volatile memory data resets after the MPF52002 powers off. To prevent the data from being reset after shutdown, follow the steps in the MTP Operation section below.

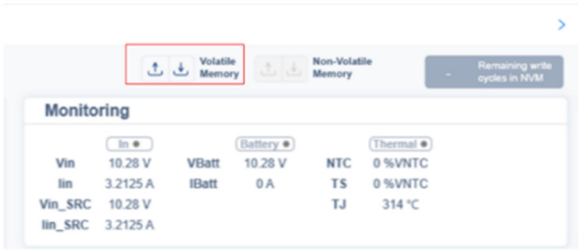

Figure 6: Valid Modification by Clicking "Write RAM"

MTP Operation

With mutilple-time-programmable (MTP) operation, the user can write another group of default settings for the MPF52002 into the NVM. The default register data is not reset after the MPF52002 resets.

Figure 7 on page 9 shows the options that support MTP operation.

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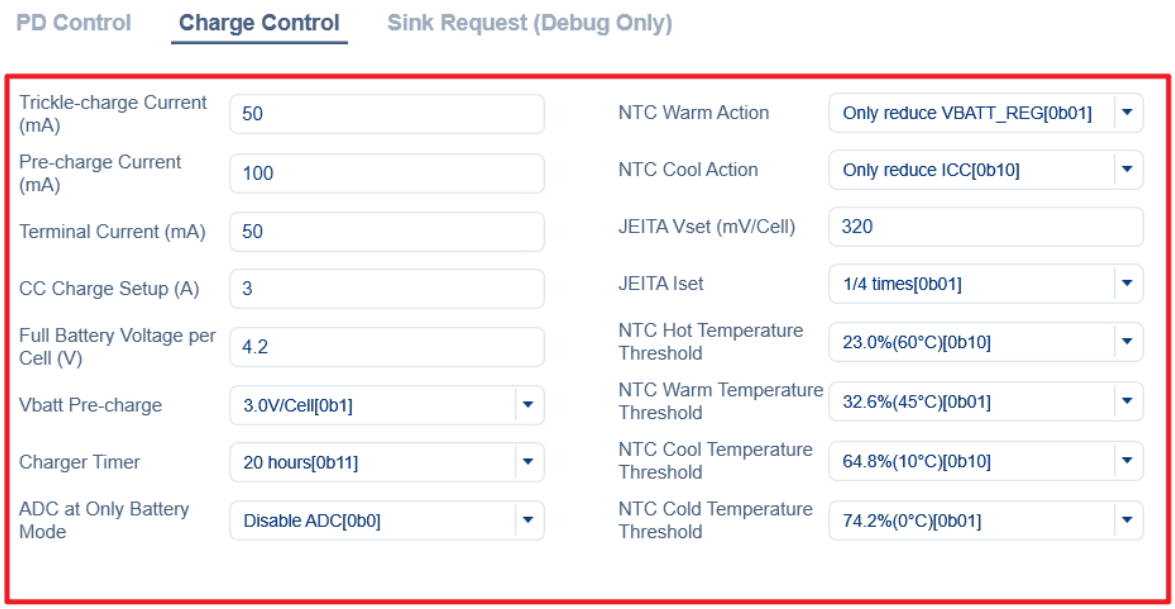

Figure 7: Charge Control (Supporting MTP Operation)

Follow the steps below for MTP operation:

1. Write the MTP's default register data to the volatile memory following the steps in the Quick Start Guide for the MPF52002's GUI section on page 9.
2. Write " 0x05", "0xaa", "0xbc", and "0xbd" to register 0xF1 one by one and wait for 10ms to load the MTP default register data from the RAM to flash. The user can also click "Write I²C Value to Flash" then wait 10ms (see Figure 8).

   Then MTP_STATUS (0xF0, bit[0]) shows "MTP DONE" (0xF0, bit[0] = 1'b1), which means that MTP operation is complete (see Figure 8). The MTP_STATUS register is reset after the power is reset. Writing 0xff to register 0xF0 can also clear the MTP_STATUS bit without resetting the power.

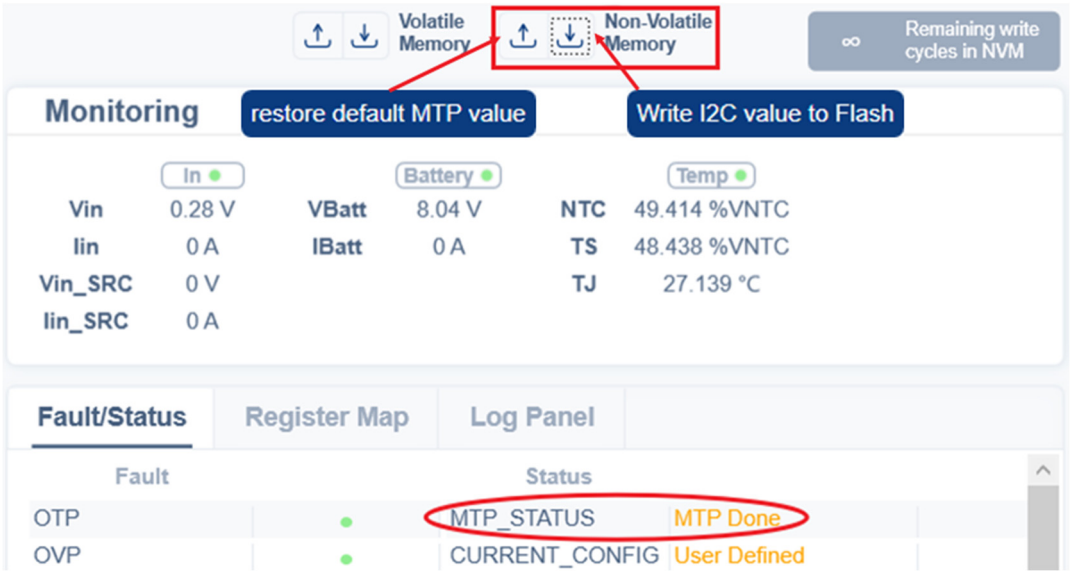

Figure 8: The MTP operation

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3. CURRENT_CONFIG (0xF2, bit[0]) shows which default setting is being used. If it says “User defined” (0xF2, bit[0] = 1’b1), then this means that the MPF52002 is using the user’s configuration; meanwhile, “Default” (0xF2, bit[0] = 1’b0) means that the MPF52002 is using the default setting created by MPS.
4. The data in the customer-defined MTP range can be cleared by writing 0xff to register 0xF3. Afterward, the MPF52002’s default setting is restored. The user can also click “restore default MTP value” then wait 10ms. (see Figure 8)
5. To erase data in the customer-defined MTP range, set the download function. Erase the full chip using a Jlink tool (or another SWD tool). After re-downloading the PD firmware, the old MTP values are cleared (see Figure 9).

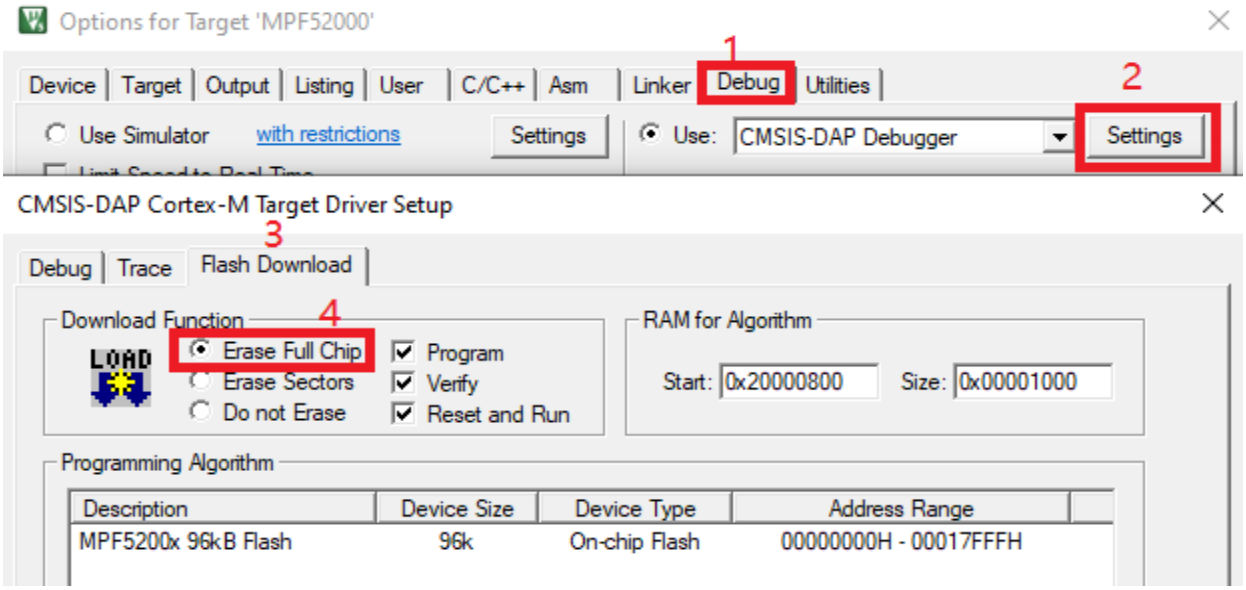

Figure 9: Erasing Data in the Customer-Defined MTP Range

Table 2 shows the MPF52002-0027’s general GPIO set-up.

Table 2: MPF52002-0027 General GPIO Set-Up

OTP Items	Value	Description
PA1_FUNCTION	I2C0_SDA	Connected to MP2761’s SDA pin.
PA2_FUNCTION	I2C0_SCL	Connected to MP2761’s SCL pin.
PA3_FUNCTION	BOOT0	Default boot pin.
PA4_FUNCTION	BOOT1	Default boot pin.
PA5_FUNCTION	USART_TX	TX for debugging.
PA6_FUNCTION	USART_RX	RX for debugging.
PB0_FUNCTION	PB0	Not used.
PB1_FUNCTION	PB1	Connected to the MP2761’s INT pin. Pull down to exit low-power mode.
PB2_FUNCTION	PB2	Cell number setting pin.
PB3_FUNCTION	PB3	Cell number setting pin.
PB6_FUNCTION	I2C1_SCL	SWDIO pin for SWD, and the SCL pin for the MPF52002 I²C.
PB7_FUNCTION	I2C1_SDA	SWCLK pin for SWD, and the SDA pin for the MPF52002 I²C.
PC2_FUNCTION	PC2	Not used.

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Firmware Update

The MPF52002's firmware does not need to be manually updated since the MPF52002 mounted on the MEZS7-PDCharge-MP2761 board already has suitable firmware. This section will describe how to further update the firmware.

The MPF52002 has a serial wire debug (SWD) port, which is on the evaluation board's CN1 connector (see Figure 10).

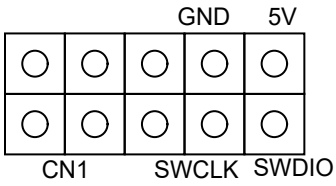

Figure 10: SWD Port on the MPF52002

Follow the steps below to download new firmware:

1. Pull PA3 down to GND.
2. Power on the MPF52002 with 8V on the VBATT pin.
3. Connect the SWD communication interface and download the firmware. The steps below describe an example while using Keil MDK to update the firmware:
   a. Obtain the MFP5200x series firmware update template from an MPS FAE.
   b. The folder MPF52000_PD_Downoad includes the PD firmware download templates (see Figure 11).

Figure 11: MPF52000_PD_Downoad Folder

   c. Ensure that the MPF5200x series pack has been installed. Find the "MPS.MPF5200x_DFP_1.0.0.pack" in the "…\MPF52000_PD_Download\Flash_Algorithm" folder (see Figure 12). Double-click the software pack for installation .

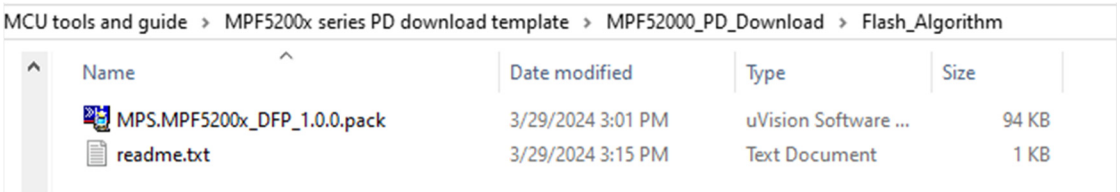

Figure 12: Installing the Software Pack

   d. Click "Options for Target..." > "Device". MPS devices should be on the list once the software pack is correctly installed. Select the "MPF52002" and click "OK" to select the device (see Figure 13 on page 12).

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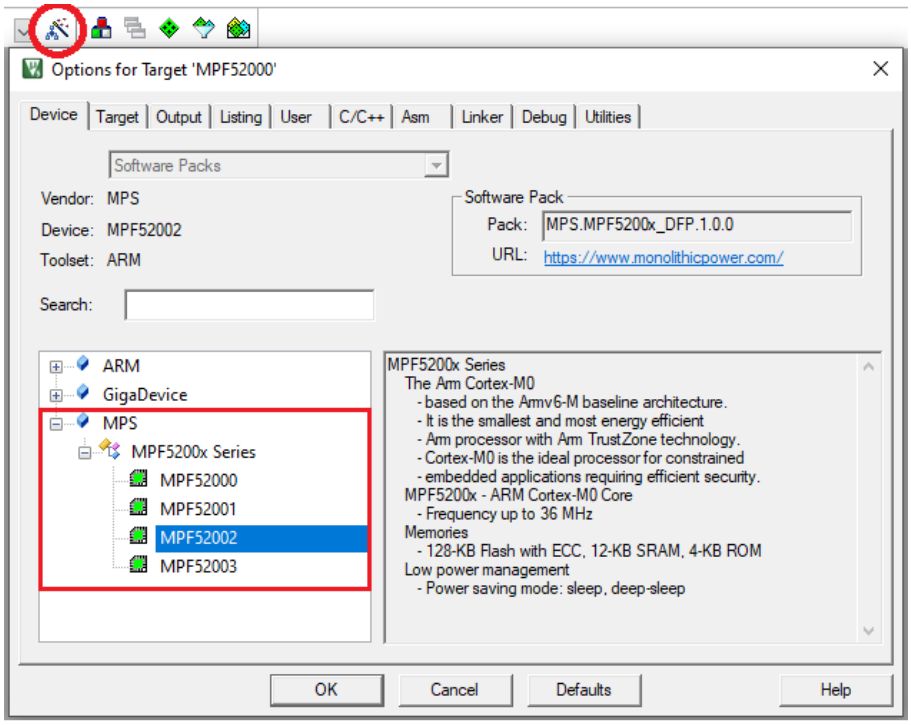

Figure 13: Selecting the MPF52002

e. Click “Options for Target…” > “Debug” > “Settings” > “Flash Download”. Ensure that the set-up is the same as below (see Figure 14).

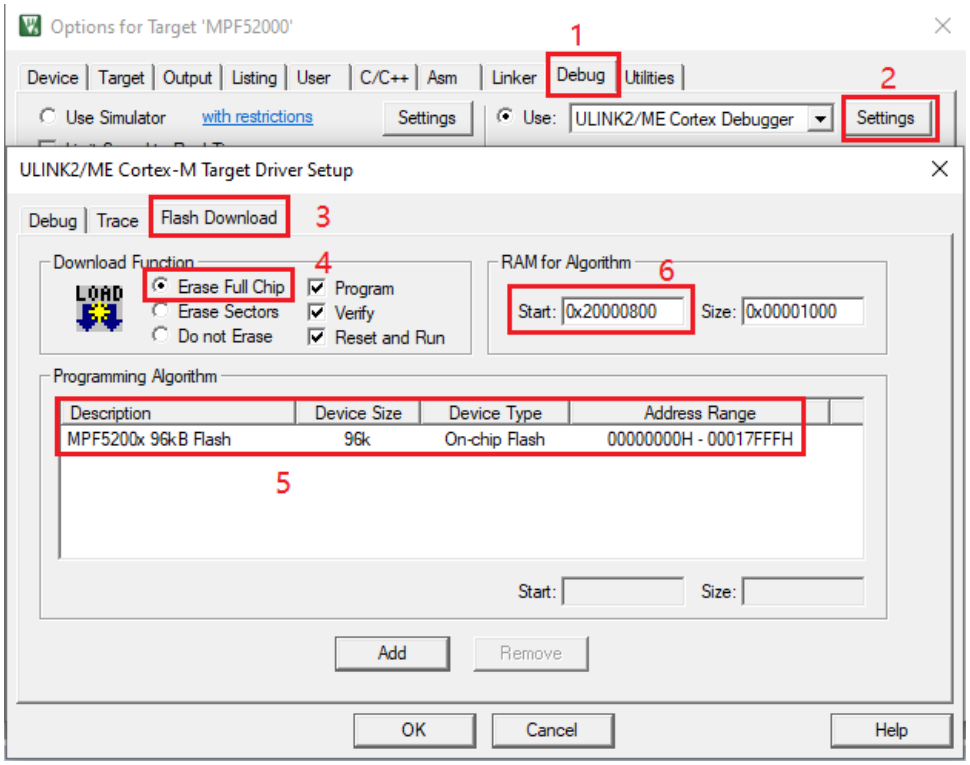

Figure 14: Set-Up

f. Copy the target firmware into the “Objects” folder, then open “MPF52002_Download.uvprojx” (see Figure 15 on page 13).

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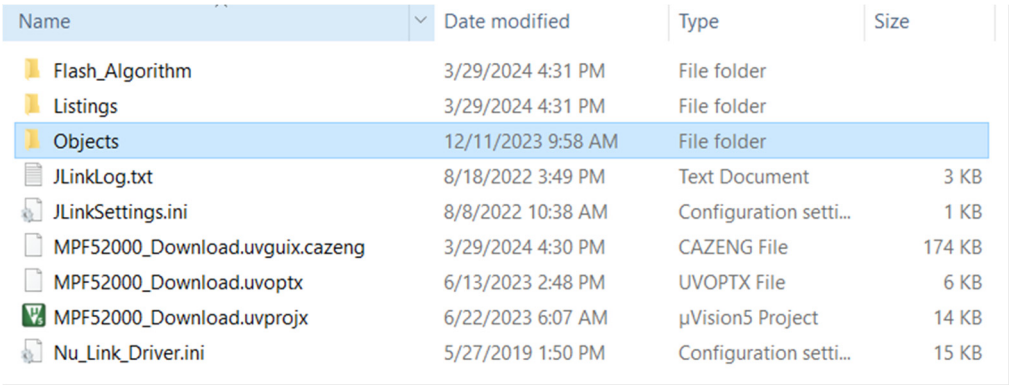

Figure 15: Copying Target Firmware

g. Copy the full name of the firmware (e.g. MPF52002GRE-0001-fr1003.axf) into “Options for Target...” > “Output” > “Name of Executable”, and then click “OK” (see Figure 16).

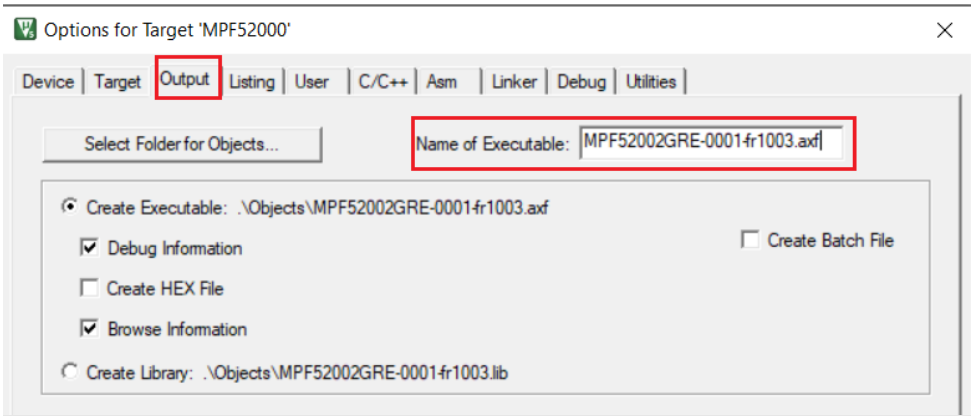

Figure 16: Copying the Full Name of the Firmware

h. Click the “Download” button, or press “F8” to download the firmware to MPF52002.

4. Remove the SWD communication interface and release PA3 after the firmware update is finished.
5. Cycle the power to load the new firmware.

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EVALUATION BOARD SCHEMATIC (7) (8)

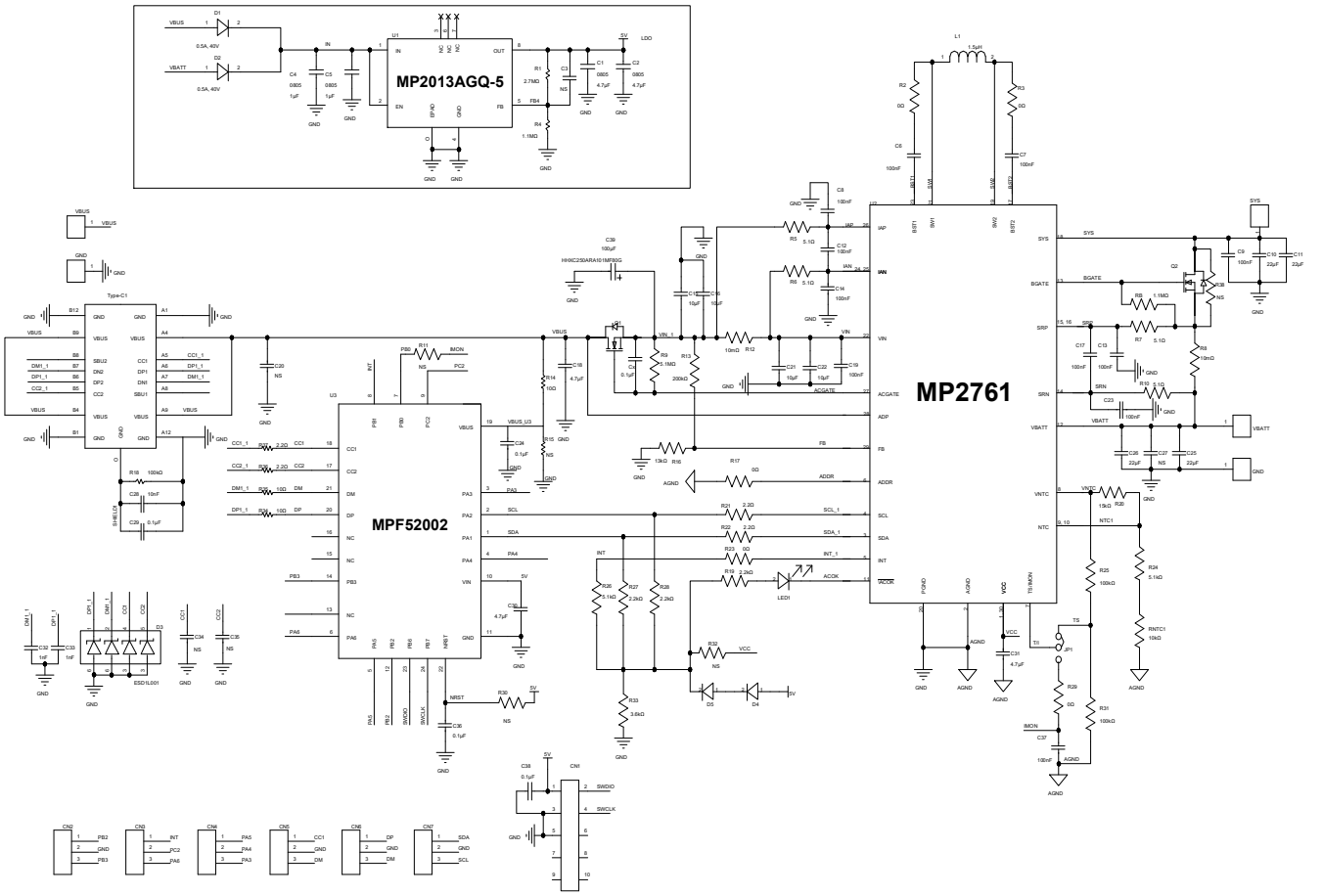

Figure 17: Evaluation Board Schematic

Notes:

7) A 0.1μF capacitor (Cx) can be paralleled with R9 to prevent an inrush current when ACGATE turns on the MOSFET (Q1).
8) PB6/7 can be used as a SWD interface. Pull down PA3 (Boot0) and restart the MPF52002 before downloading new firmware through the SWD interface (PB6/7). Remove the PB6/7 connection with the SWD communication interface and release PA3 after the firmware update is finished. Then re-power on to load the new firmware.

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MEZS7-PDCharger-MP2761 BILL OF MATERIALS

Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
2	C1, C2	4.7μF	Ceramic capacitor, 16V, X7R	0805	Murata	GCM21BR71C475KA73L
5	C3, C20, C27, C34, C35	NS				
2	C4, C5	1μF	Ceramic capacitor, 25V, X7R	0805	Wurth	885012207078
13	C6, C7, C8, C12, C13, C14, C17, C23, C24, C29, C36, C37, C38	100nF	Ceramic capacitor, 25V, X7R	0603	Wurth	885012206071
2	C9, C19	100nF	Ceramic capacitor, 25V, X7R	0402	Murata	GRM155R71E104KE14D
4	C10, C11, C25, C26	22μF	Ceramic capacitor, 25V, X5R	0805	Murata	GRM21BR61E226ME44L
4	C15, C16, C21, C22	10μF	Ceramic capacitor, 25V; X7S	0805	Murata	GRM21BC7E106KE11L
1	C18	4.7μF	Ceramic capacitor, 25V; X5R	0603	Murata	GRM188R61E475KE11D
1	C28	10nF	Ceramic capacitor, 25V, X7R	0603	TDK	C1608X7R1E103K
2	C30, C31	4.7μF	Ceramic capacitor, 16V, X5R	0603	Murata	GRM188R61C475KE11D
2	C32, C33	1nF	Ceramic capacitor, 25V, C0G	0603	Murata	GRM1885C1E102JA01D
1	C39	100μF	Hybrid, 25V, 20mΩ	SMD	Nippon Chemi-Con	HHXC250ARA101MF80G
1	R1	2.7MΩ	Film resistor, 1%	0603	Yageo	RC0603FR-132M7L
5	R2, R3, R17, R23, R29,	0Ω	Film resistor, 5%	0603	Yageo	RC0603JR-070RL
2	R4, RB	1.1MΩ	Film resistor, 1%	0603	Yageo	RC0603FR-071M1L
4	R5, R6, R7, R10	5.1Ω	Film resistor, 1%	0603	Yageo	RC0603FR-075R1L
2	R8, R12	10mΩ	Current-sensing resistor, 1%, long side, 1W	L1508	Film Tech	RL3720WT-R010-F
1	R9	5.1MΩ	Film resistor, 5%	0603	Yageo	RC0603FR-075M1L
5	R11, R15, R30, R32, R38	NS				
1	R13	200kΩ	Film resistor, 1%,	0603	Yageo	RC0603FR-07200KL
3	R14, R34, R35	10Ω	Film resistor, 1%	0603	Yageo	RC0603FR-0710RL
1	R16	13kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-0713KL
3	R18, R25, R31	100kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-07100KL
3	R19, R27, R28	2.2kΩ	Film resistor, 5%	0603	Liz	CR0603JA0222G
1	R20	15kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-0715KL
4	R21, R22, R36, R37	2.2Ω	Film resistor, 1%	0603	Yageo	RC0603FR-072R2L
2	R24, R26	5.1kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-075K1L

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MEZS7-PDCharger-MP2761 BILL OF MATERIALS *(continued)*

Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
1	R33	3.6kΩ	Film resistor, 5%	0603	Liz	CR0603JA0362G
1	RNTC1	10kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-0710KL
7	JP1, CN2, CN3, CN4, CN5, CN6, CN7	3-pin	3 pins, 1 row, 2.54mm	DIP	Wurth	61300311121
1	CN1	10-pin	5 pins, 2 rows, 2.54mm	DIP	Wurth	61301021121
1	TYPE_C1	16-pin	USB Type-C receptacle	SMD	Yuehu Electronic	PC-071603863-R
5	VBUS ,GND, VBAT, GND, VSYS	Φ2.0	Φ2.0 copper pin	DIP		
1	LED1	Red	LED	0805	Wurth	150080RS75000
2	D1, D2	I_R = 20μA	Schottky diode, 40V, 0.5A	SOD123	AUK	SDB0540
1	D3	5V	ESD diode	SOT-363	onsemi	ESD1L001
2	D4, D5	V_F = 0.4V at I_F = 1mA	60V,15mA	SOD-323	Diodes	SD101AWS
2	Q1, Q2	8.5mΩ	MOSFET	QFN (3.3mmx 3.3mm)	Vishay	SISA14DN-T1-GE3
1	L1	1.5μH	Inductor, 9.7mΩ, 9A	SMD	MPS	MPL-AL5030-1R5
1	U1	MP2013A-5	LDO	QFN-8 (3mmx 3mm)	MPS	MP2013AGQ-5
1	U2	MP2761	Charger	TQFN-30 (4mmx 5mm)	MPS	MP2761GVT-0000
1	U3	MPF52002	PD controller	QFN-24 (4mmx 4mm)	MPS	MPF52002-0027

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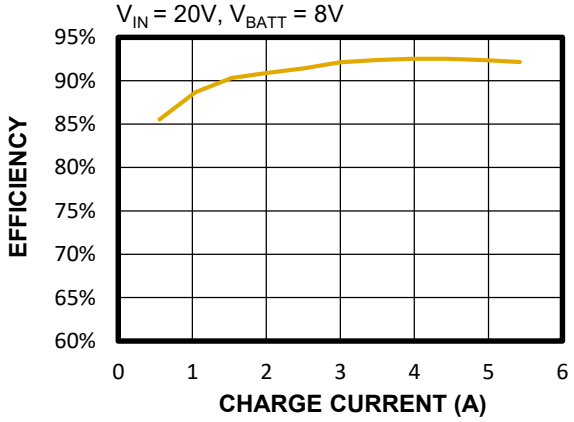
EVB TEST RESULTS

Performance curves and waveforms are tested on the evaluation board. V_{IN} = 20V, V_{BATT} = 8V, T_A = 25°C, default register data, unless otherwise noted.

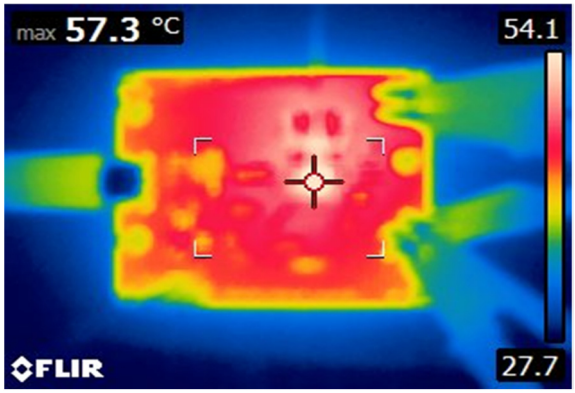
Efficiency vs. Charge Current

V_{IN} = 20V, V_{BATT} = 8V



Thermal Images

V_{IN} = 20V, V_{BATT} = 8V, I_{CHG} = 3A, T_A = 28°C,T_{CASE} = 57.3°C



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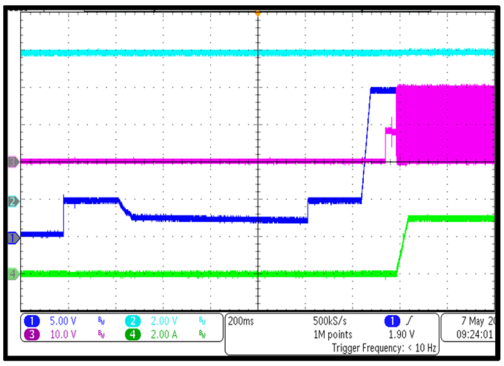
EVB TEST RESULTS *(continued)*

Performance curves and waveforms are tested on the evaluation board. Input power source is a PD adapter, V_{BATT} = 8V, T_A = 25°C, default register data, unless otherwise noted.

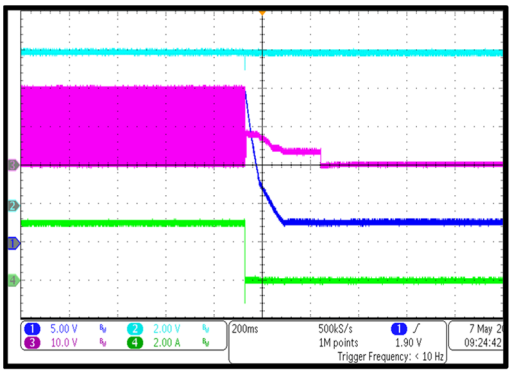
Plug PD Adapter

CH3: V_{SW}
CH2: V_{BATT}
CH1: V_{IN}
CH4: I_{BATT}



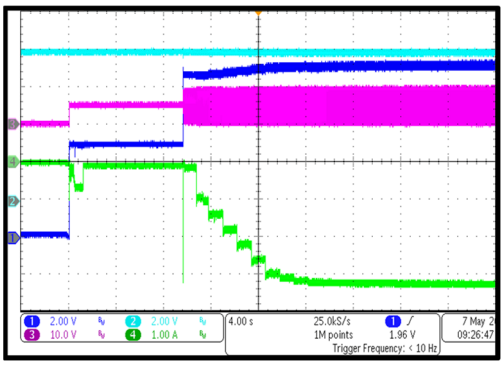
Unplug PD Adapter

CH3: V_{SW}
CH2: V_{BATT}
CH1: V_{IN}
CH4: I_{BATT}



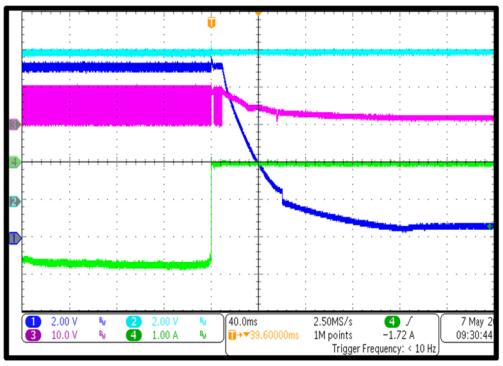
Plug PD Mobile Device

CH3: V_{SW}
CH4: I_{BATT}
CH2: V_{BATT}
CH1: V_{IN}



Unplug PD Mobile Device

CH3: V_{SW}
CH4: I_{BATT}
CH2: V_{BATT}
CH1: V_{IN}



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PCB LAYOUT

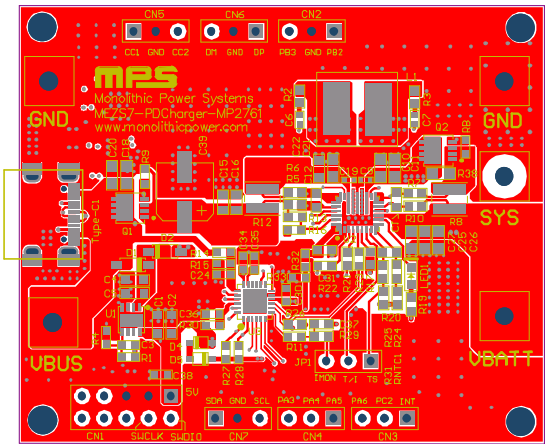

Figure 18: Top Layer

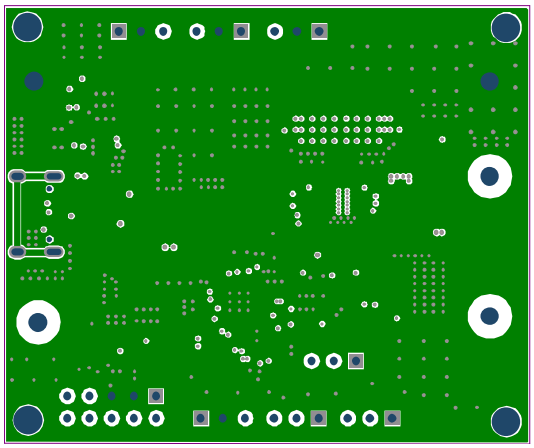

Figure 19: Mid-Layer 1

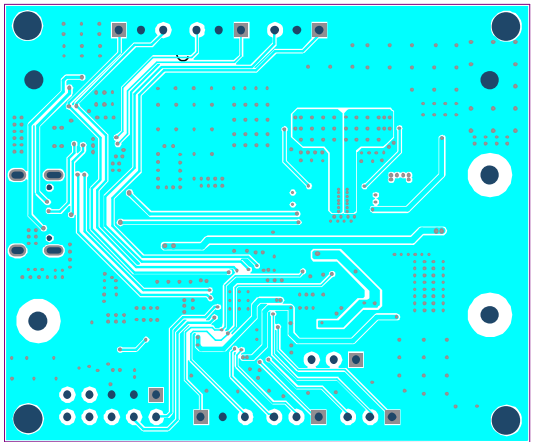

Figure 20: Mid-Layer 2

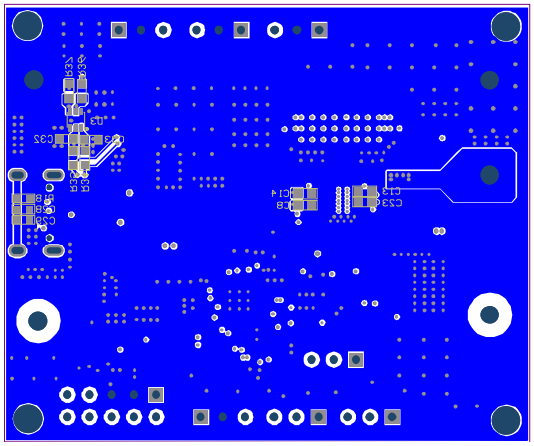

Figure 21: Bottom Layer

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REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	12/17/2024	Initial Release	-

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