MA600A

High-Accuracy, <0.6° (<0.1°) INL, High-Bandwidth, Configurable Digital Magnetic Angle Sensor

DESCRIPTION

The MA600A is a precision, high-bandwidth magnetic angle sensor that detects the absolute angular position of a permanent magnet, typically a diametrically magnetized cylinder on a rotating shaft. With an integrated precision tunnel magnetoresistance (TMR) sensor, the MA600A achieves high bandwidth and high accuracy (INL), making it an ideal solution for position control and robotics.

The MA600A supports a wide range of magnetic field strengths and mounting configurations: end-of-shaft (on-axis) and side-shaft (off-axis).

On-chip non-volatile memory (NVM) provides storage for configuration parameters, including the reference zero-angle position, ABZ, UVW, and pulse-width modulation (PWM) settings.

The MA600A is factory-calibrated to achieve an error (INL) below 0.6° across its operating temperature range. Furthermore, a final system calibration is available through a 32-point, user-configurable correction table. The resulting error (INL) after user calibration can be smaller than 0.1°.

Communication with the MA600A can be accomplished via the serial peripheral interface (SPI) and synchronous serial interface (SSI).

The MA600A supports a daisy-chain configuration. It allows for the sequential SPI angle readout of multiple sensors, which minimizes the number of I/O pins used by the controller device.

The MA600A is available in a small QFN-16 (3mmx3mm) package.

FEATURES

- <0.6° Error (INL)
- <0.1° Error (INL) after User Calibration with On-Chip 32-Point Lookup Table
- Configurable 12-Bit to 15-Bit Absolute Angle Encoder
- High Bandwidth (e.g. 12kHz at 12.5-Bit Resolution)
- No Latency
- Wide 10mT to 100mT Magnetic Field Range
- Serial Peripheral Interface (SPI) for Digital Angle Readout and Chip Configuration
- SPI Angle Readout in Daisy Chain Configuration Supported
- Synchronous Serial Interface (SSI) for Digital Angle Readout
- Incremental ABZ Quadrature Encoder Interface with Configurable Pulses per Turn (1 to 4096)
- Incremental UVW Encoder Output
- Pulse-Width Modulation (PWM) Absolute Output
- Multi-Turn or Speed Output Option
- 3.3V Supply
- 7.5mA Quiescent Current (I_{AVDD} + I_{DVDD})
- -40°C to +125°C Operating Temperature
- Available in a Small QFN-16 (3mmx3mm) Package

APPLICATIONS

- Robotics
- Multi-Turn Encoders
- Position Control
- Speed Control

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TYPICAL APPLICATION

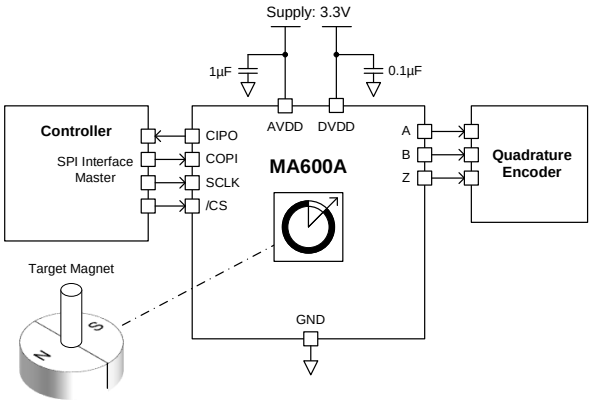

Table 1: Configurable Filter Window to Optimize Resolution vs. Bandwidth (BW)

Digital Filter Window FW	Noise-Free Resolution (Bits)	Latency Cancellation at Constant Speed	Bandwidth (kHz)
0	12.3	No	17
5 (default)	12.5	Yes	12
6	13	Yes	5.8
7	13.5	Yes	2.7
8	14	Yes	1.3
9	14.3	Yes	0.63
10	14.6	Yes	0.31
11	14.8	Yes	0.15
12	15	Yes	0.075

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ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MA600AGQE-0000	QFN-16 (3mmx3mm)	*See Below*	1
MA600AGQE-xxxx**			
TBMA600A-Q-LT	Test board	N/A	N/A
EVKT-MagAlpha-MagDiff	Evaluation kit	N/A	N/A

* For Tape & Reel, add suffix -Z (e.g. MA600AGQE-xxxx-Z).

** “xxxx” is the configuration code identifier for the register settings. The first four digits of the suffix (“xxxx”) can be a hexadecimal value between 0 and F. Work with an MPS FAE to create this unique number for the non-default function option. “0000” is the factory default code.

TOP MARKING

$\overline{\text{CLGY}}$
LLLL

CLG: MPS product code of MA600AGQE-xxxx
Y: Year code
LLLL: Lot number

EVALUATION KIT (EVKT-MAGALPHA-MAGDIFF)

EVKT-MagAlpha-MagDiff kit contents (items below cannot be ordered separately):

#	Part Number	Item	Quantity
1	EVKT-MA-RP-PICO-V2	MagAlpha and MagDiff evaluation board with MCU	1
2	Ribbon cable	8 conductors flat ribbon cable	2
3	USB cable	USB cable (A male to Micro-B male)	1
4	Online resources	Include GUI, Python library, and supplementary documents	-

Order directly from MonolithicPower.com or our distributors.

Figure 1: EVKT-MagAlpha-MagDiff Evaluation Kit Set-Up

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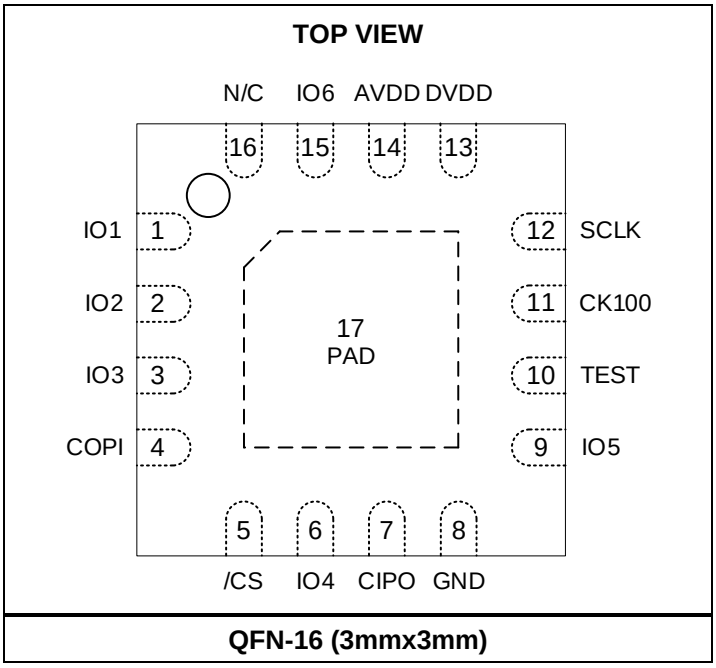
PACKAGE REFERENCE



QFN-16 (3mmx3mm)

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PIN FUNCTIONS

Pin #	Name	Description
1	IO1	**Digital input/output (I/O) 1.** The IO1 pin is bidirectional and configured as push-pull by default. (1) Float IO1 if it is not used.
2	IO2	**Digital I/O 2.** The IO2 pin is bidirectional and configured as push-pull by default. (1) Float IO2 if it is not used.
3	IO3	**Digital I/O 3.** The IO3 pin is bidirectional and configured as push-pull by default. (1) Float IO3 if it is not used.
4	COPI	**Serial peripheral interface (SPI) data in.** The COPI pin is pulled down internally. (2) Connect COPI to GND if it is not used.
5	/CS	**SPI chip selection.** The /CS pin is pulled up internally. (2) Connect /CS to DVDD if it is not used.
6	IO4	**Digital I/O 4.** The IO4 pin is bidirectional and configured as push-pull by default. (1) Float IO4 if it is not used.
7	CIPO	**SPI data out.** The CIPO pin is configured as push-pull when the SPI is active. CIPO is configured as pull-down when the SPI is idle. Float CIPO if it is not used.
8	GND	**Supply ground.**
9	IO5	**Digital I/O 5.** The IO5 pin is bidirectional and configured as push-pull by default. (1) Float IO5 if it is not used.
10	TEST	**Test.** Connect the TEST pin to GND.
11	CK100	**Clock output reference for speed calculation.** Float the CK100 pin if it is not used. The pin is internally pulled down to GND when the CK100 bit in the IF register is set to 0.
12	SCLK	**SPI clock.** The SCLK pin is pulled down internally. (2) Connect SCLK to GND if it is not used.
13	DVDD	**Digital supply 3.3V.** Bypass the DVDD pin to GND with a 0.1µF, low-ESR capacitor. See the Electrical Mounting and Power Supply Decoupling section on page 42 for details on the layout reference.
14	AVDD	**Analog supply 3.3V.** Bypass the AVDD pin to GND with a 1µF, low-ESR capacitor. See the Electrical Mounting and Power Supply Decoupling section on page 42 for details on the layout reference.
15	IO6	**Digital I/O 6.** The IO6 pin is bidirectional and configured as push-pull by default. (1) Float IO6 if it is not used.
16	NC	**Do not connect this pin.** This pin is internally pulled down to GND.
17	E-PAD	**E-pad.** No connection. Float the E-PAD pin.

Notes:

1) Can be configured as open drain with the OD615 and OD243 bits.
2) Can be configured to high impedance via the SPULLIN bit.

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ABSOLUTE MAXIMUM RATINGS (3)

Supply voltage (V_{AVDD}, V_{DVDD}) .....-0.5V to +4.6V
All other pins .....-0.5V to +6V
Continuous power dissipation (T_A = 25°C) (4)
..... 2W
Lead temperature.....260°C
Operating temperature..... -40°C to +125°C
Maximum magnetic field 200mT

ESD Ratings

Human body model (HBM) ..... ±2kV
Charged-device model (CDM).....±2kV

Recommended Operating Conditions (5)

V_{AVDD}, V_{DVDD} .....3V to 3.6V
Operating junction temp (T_J).....-40°C to +125°C

Thermal Resistance (6) θ_{JA} θ_{JC}

QFN-16 (3mmx3mm).....50 ..... 12... °C/W

Notes:

3) Exceeding these ratings may damage the device.
4) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can produce an excessive die temperature, which may cause the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
5) The device is not guaranteed to function outside of its operating conditions.
6) Measured on a JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

V_{AVDD} = V_{DVDD} = 3.3V, T_A = -40°C to +125°C, typical values at T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Power Supply						
Supply voltage	V_{AVDD}		3	3.3	3.6	V
	V_{DVDD}		3	3.3	3.6	V
VDD voltage (V_{DD}) under-voltage lockout (UVLO) threshold	V_{DD_UVLO}	V_{DD} rising, V_{AVDD} = V_{DVDD}			2.95	V
V_{DD} UVLO hysteresis	$V_{DD_UVLO_HYS}$	V_{AVDD} = V_{DVDD}	30			mV
Supply current	I_{AVDD} + I_{DVDD}	T_A = 25°C	5.5	7.5	9.5	mA
Supply current drift		T_A = -40°C to +125°C		0.006		mA/°C
Digital Input/Output (I/O)						
Input high voltage	V_{IH}		2.5		5.5	V
Input low voltage	V_{IL}		-0.3		+0.8	V
Pull-up resistor	R_{PU}	V_I = GND		80		kΩ
Pull-down resistor	R_{PD}	V_I = V_{DVDD}		30		kΩ
Push-Pull Option						
Output low voltage	V_{OL_PP}	I_{OL} = 12mA			0.4	V
Output high voltage	V_{OH_PP}	I_{OH} = 12mA	2.4			V
Rising edge slew rate	t_R	C_{LOAD} = 50pF		0.7		V/ns
Falling edge slew rate	t_F	C_{LOAD} = 50pF		0.7		V/ns
Open-Drain Option						
Output low voltage	V_{OL_OD}	I_{OL} = 12mA			0.4	V
Output high voltage (7)	V_{OH_OD}	Supplied by external pull-up resistor			5.5	V
Open-drain leakage current				100		nA

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GENERAL CHARACTERISTICS

V_{AVDD} = V_{DVDD} = 3.3V, 20mT < B < 80mT, T_A = -40°C to +125°C, typical values at T_A = 25°C and B = 45mT, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Operating temperature	T_{OP}		-40		+125	°C
Applied magnetic field	B	Optimal linearity	20		80	mT
		Functional	10		150	mT
Absolute Output (Serial)						
Resolution (7)		±3σ noise deviation	12		15	bit
Noise RMS (7)			0.002		0.015	deg
Refresh rate	$f_{REFRESH}$	T_A = 25°C	780	800	820	kHz
Oscillator drift		T_A = -40°C to +85°C		-30		ppm/°C
		T_A = 85°C to 125°C		-100		ppm/°C
Data output length				16		bit
Response Time						
Start-up time (7)		FW bits = 0, T_A = 25°C			250	µs
Front-end time constant	t_{FE}			5		µs
Digital propagation delay	t_{DP}			22		µs
Total latency (added time beyond refresh time) (7)	L	FW bits = 0		32		µs
		FW bits = 5 to 12	-0.5		0.5	µs
Cutoff frequency	f_{CUTOFF}	FW bits = 0		17		kHz
Accuracy						
Integral nonlinearity (7)	INL	T_A = 25°C, B = 45mT		0.2	0.6	deg
		After user calibration with on-chip 32-point lookup table, T_A = 25°C		0.06	0.1	deg
Differential nonlinearity (7)	DNL	T_A = 25°C, B = 45mT		2.8		%
Output Drift						
Temperature induced (7)		T_A = -40°C to +85°C		0.0015	0.0045	deg/°C
		T_A = 85°C to 125°C		0.005	0.02	deg/°C
Magnetic field induced (7)		T_A = 25°C		0.004	0.007	deg/mT
Voltage supply induced (7)		B = 45mT, T_A = 25°C		0.1	0.3	deg/V
Functional Test Mode						
Functional test accuracy				2		deg
Absolute Output (PWM)						
Pulse-width modulation (PWM) frequency	f_{PWM}	PWMF bit = 1, T_A = 25°C	243	250	257	Hz
		PWMF bit = 0, T_A = 25°C	0.975	1	1.025	kHz
PWM resolution				12		bit
Incremental Output (ABZ)						
ABZ update rate		T_A = 25°C	12	12.8		MHz
Edges per turn resolution		Configurable	4		16384	
Pulses per channel per turn	PPT + 1	Configurable	1		4096	
Differential nonlinearity	DNL			1.7		%
Overall ABZ jitter (3σ)		PPT bits = 511, speed = 1krpm		0.06		deg
		PPT bits = 2047, speed = 10krpm		0.02		deg

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GENERAL CHARACTERISTICS *(continued)*

V_{AVDD} = V_{DVDD} = 3.3V, 20mT < B < 80mT, T_A = -40°C to +125°C, typical values at T_A = 25°C and B = 45mT unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Incremental Output (UVW)						
Cycle per turn	NPP + 1	Configurable	1		8	
UVW jitter (3σ)		NPP bit = 0, speed = 5krpm		0.4		deg
Speed Output						
Speed scale	S_{SPEED}	f_{CK100} = 100kHz		5.722		rpm/LSB
CK100 clock frequency		T_A = 25°C	98	100	102	kHz

Note:

7) Guaranteed by design or characterization.

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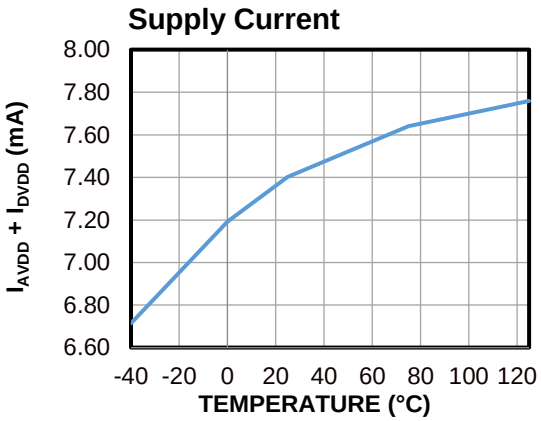
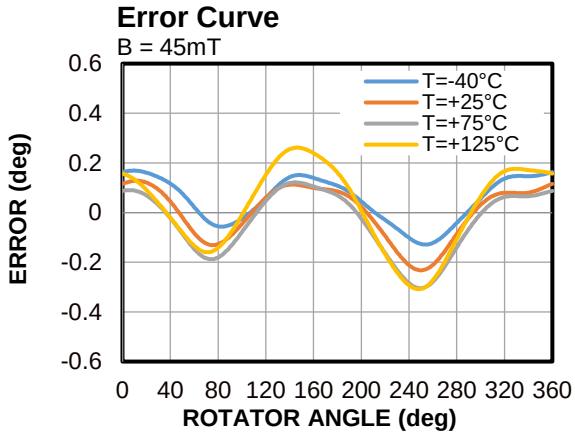
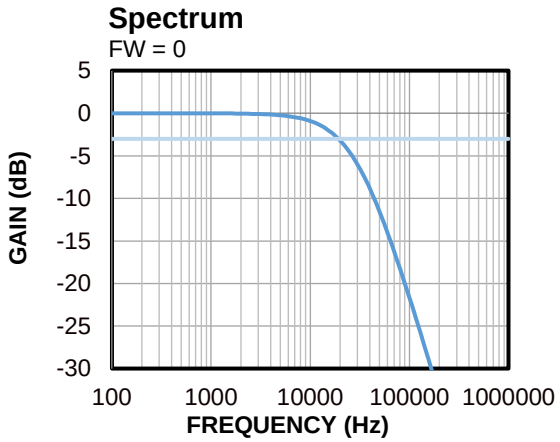
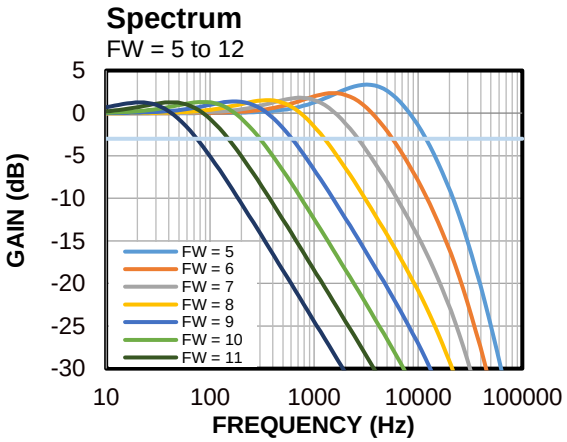
TYPICAL CHARACTERISTICS

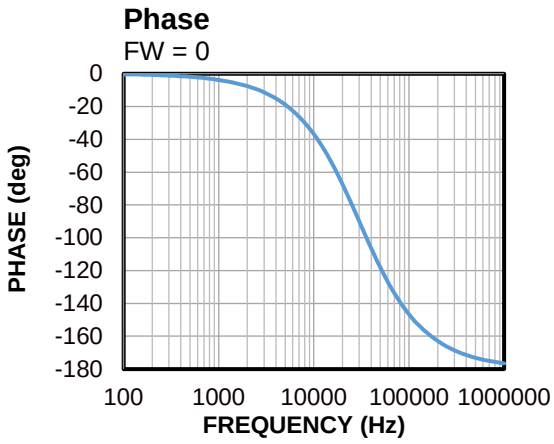
V_{AVDD} = V_{DVDD} = 3.3V, 20mT < B < 80mT, T_A = 25°C, unless otherwise noted.

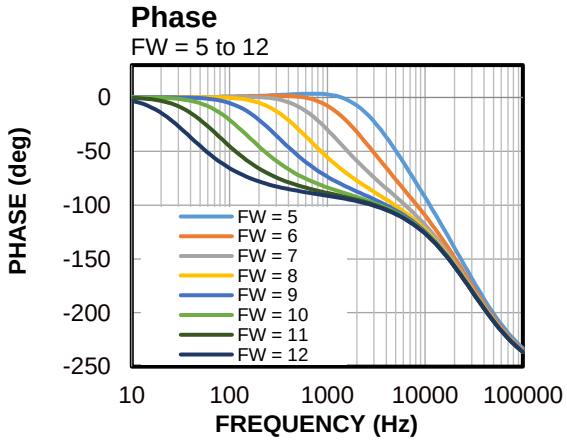












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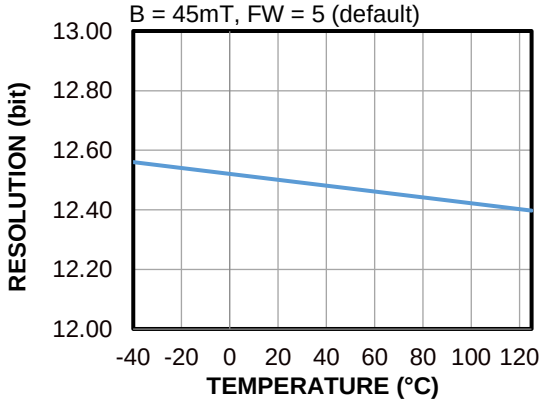
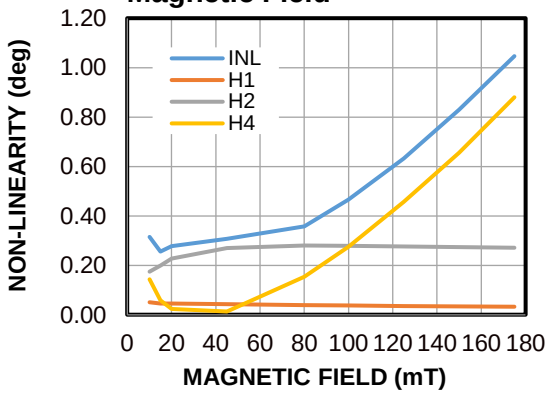
TYPICAL CHARACTERISTICS *(continued)*

V_{AVDD} = V_{DVDD} = 3.3V, 20mT < B < 80mT, T_A = 25°C, unless otherwise noted.

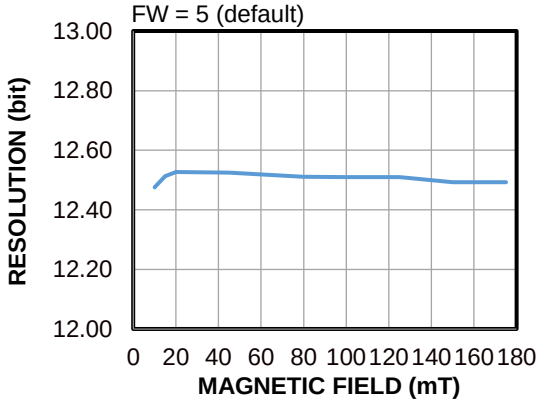
Resolution vs. Temperature (Over-Temperature)



INL and Harmonics vs. Magnetic Field (8)



Resolution vs. Magnetic Field



Note:

8) See the Appendix B: Definitions section on page 47 for the INL and harmonics definitions.

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FUNCTIONAL BLOCK DIAGRAM

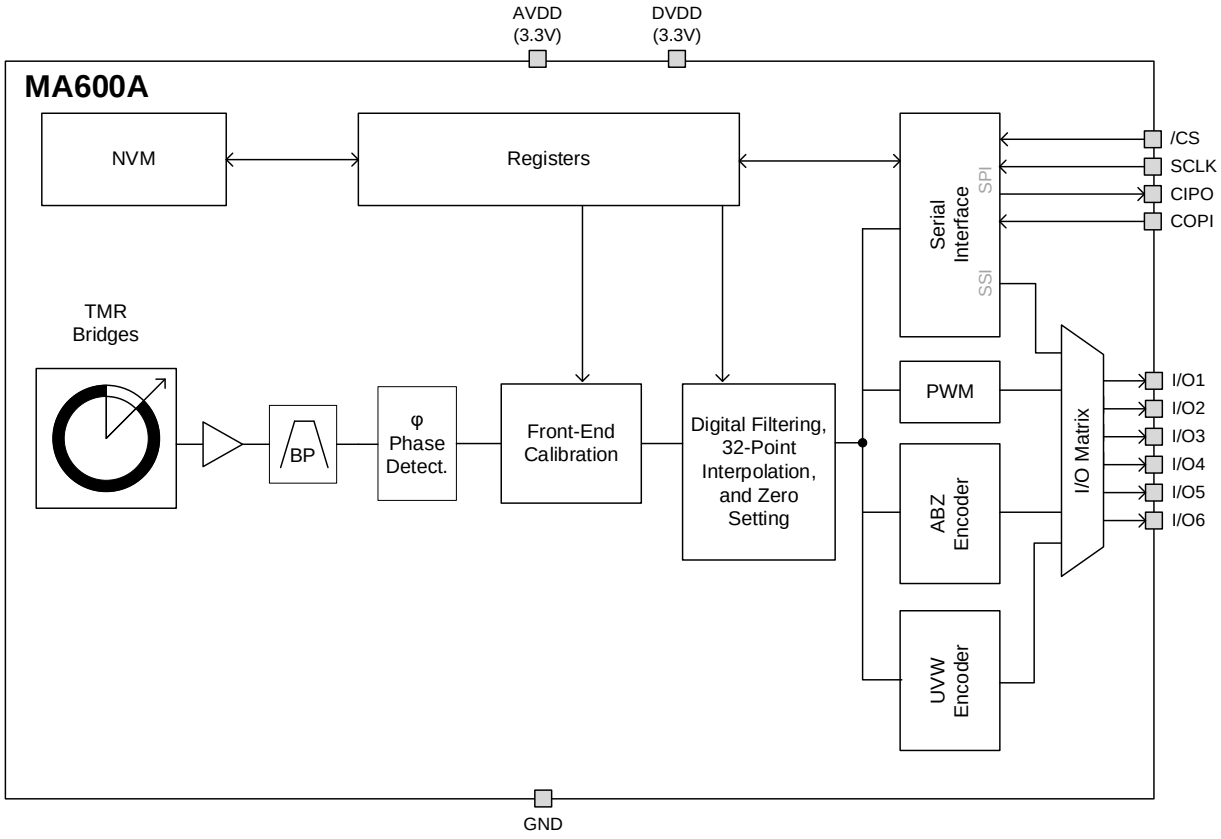

Figure 2: Functional Block Diagram

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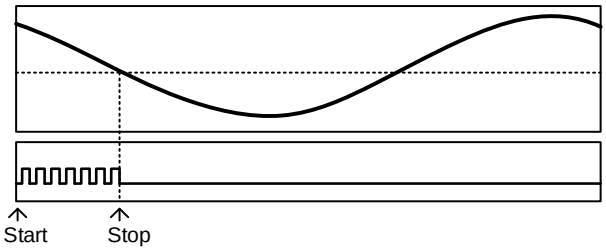
OPERATION

Sensor Front End

The magnetic field is detected with the tunneling magnetoresistance (TMR) bridges located in the center of the package. The angle is measured using the Spinaxis™ method, which directly digitizes the direction of the field without complex arctangent computation or feedback loop-based circuits (interpolators).

The Spinaxis™ method is based on phase detection, and this method generates a sinusoidal signal with a phase that represents the angle of the magnetic field. The angle is then obtained by a time-to-digital converter, which measures the time between the zero crossing of the sinusoidal signal and the edge of a constant waveform (see Figure 3). The time-to-digital is output from the front end to the digital conditioning block.



Top: Sine Waveform

Bottom: Clock for Time-to-Digital Converter

Figure 3: Phase Detection Method

The front-end output delivers a digital number that is proportional to the angle of the magnetic field (at a rate of 800kHz) in a straightforward and open-loop manner.

Sensor (Magnet Mounting)

The sensitive volume of the MA600A is confined to a region less than 400µm wide. This area contains multiple TMR bridges. The volume is located horizontally within 50µm of the center of the package. Vertically, the sensitive volume is centered at approximately 300µm under the surface. The sensor detects the angle of the magnetic field projected in a plane parallel to the package's upper surface. This means that the only relevant magnetic field is the in-plane component (X and Y components) within the sensitive volume (see Figure 4).

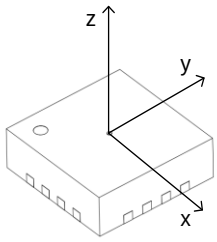


Figure 4: Space Coordinates (Field is Sensed on the XY Plane)

By default, when looking at the top of the package, the angle increases when the magnetic field rotates clockwise. Figure 5 shows the zero angle of a sensor that has not been configured, where the cross indicates the sensitive point. Both the rotation direction and the zero angle can be configured.

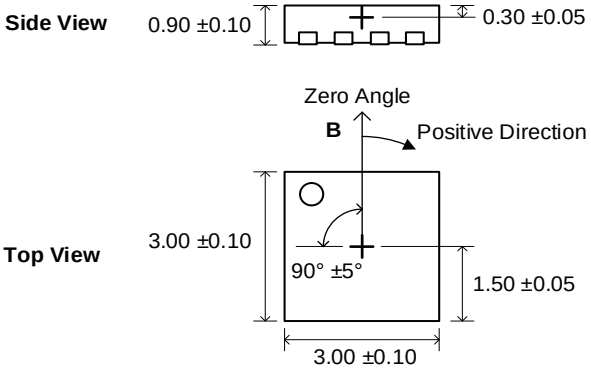


Figure 5: Detection Point and Default Positive Direction

This type of detection provides flexibility for the angular encoder design. The sensor requires the magnetic vector to remain within the sensor plane with an amplitude within the recommended operating range.

The most straightforward mounting method is to place the MA600A sensor on the rotation axis of a permanent magnet, such as a diametrically magnetized cylinder (see Figure 6 on page 14).

Consider a Neodymium alloy (N35) cylinder magnet with Ø5x2.5mm dimensions inserted into an aluminum shaft, with a 2mm air gap between the magnet and the sensor (surface of the package). For optimal linearity, the distance between the sensor's center and rotation axis should be smaller than 5% of the magnet's outer diameter.

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For more information about the sensor and magnet placement, refer to the related application note on the MPS website (Selecting the Right Magnet for the MagAlpha in End-of-Shaft Mounting).

Figure 6 shows end-of-shaft mounting.

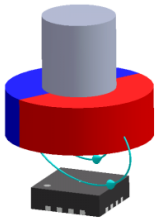

Figure 6: End-of-Shaft Mounting

If the end-of-shaft position is not available, the sensor can be positioned away from the rotation axis of a cylinder or ring magnet (see Figure 7).

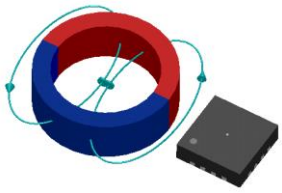

Figure 7: Side-Shaft Mounting

With side-shaft mounting, the magnetic field angle is no longer directly proportional to the mechanical angle. The MA600A can be adjusted to compensate for this effect, and to recover the linear relation between the mechanical angle and the sensor output. With multiple pole pair magnets, the MA600A indicates multiple rotations for each mechanical turn.

Serial Interface

The sensor supports the serial peripheral interface (SPI) for angle reading and register configuration. Alternatively, the synchronous serial interface (SSI) protocol can be used for angle reading. Configuration through the SSI is not supported.

Serial Peripheral Interface (SPI)

The SPI is a four-wire, synchronous, serial communication interface. The MA600A supports SPI mode 3 and mode 0. Table 2 shows the SPI specifications.

Table 2: SPI Specifications

	Mode 0	Mode 3
SCLK Idle State	Low	High
Data Capture	On the SCLK rising edge	
Data Transmission	On the SCLK falling edge	
/CS Idle State	High	
Data Order	MSB first	

The SPI mode (0 or 3) is detected automatically by the sensor and does not require additional action from the user. The maximum SPI clock frequency supported by the MA600A is 25MHz. There is no minimum clock rate. The real maximum data rates depend on the PCB layout quality and signal trace length.

Table 3 shows the standard SPI values.

Table 3: SPI Standard

	Mode 0	Mode 3
CPOL	0	1
CPHA	0	1
Data Order (DORD)	0 (MSB first)	

All commands to the MA600A (whether for writing or reading register content) must be transferred through the SPI's COPI pin. See the SPI Communication section on page 16 for more details.

Figure 8 on page 15 shows the SPI timing diagram for mode 3 and mode 0, where COPI stands for the controller output peripheral input, and CIPO stands for the controller input peripheral output. Figure 9 on page 15 shows the minimum idle time. Table 4 on page 16 shows the SPI timing.

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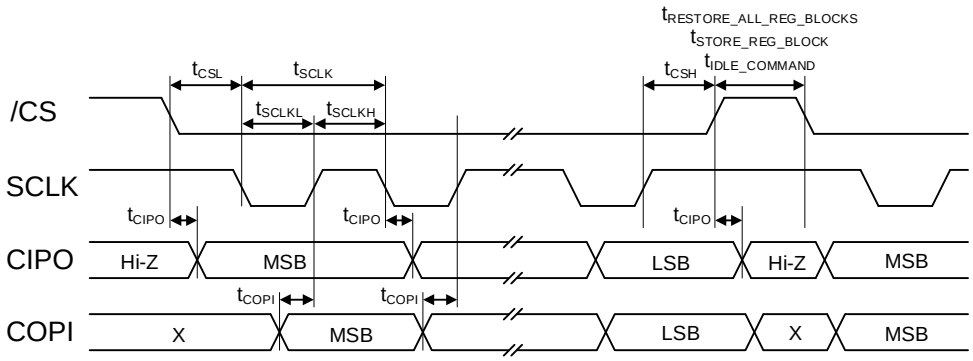
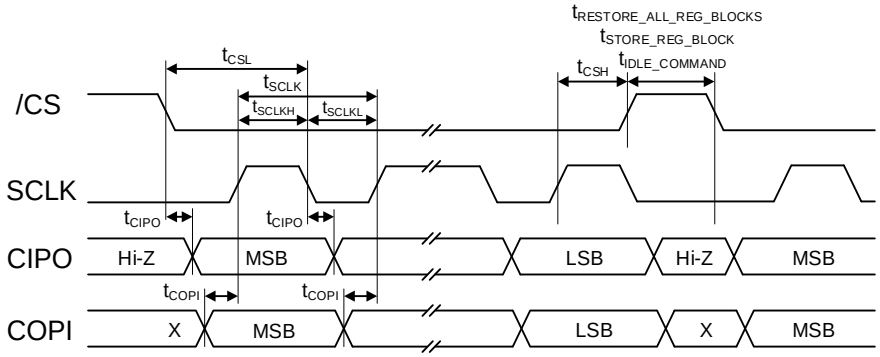


SPI Mode 3



SPI Mode 0

Figure 8: SPI Timing Diagram

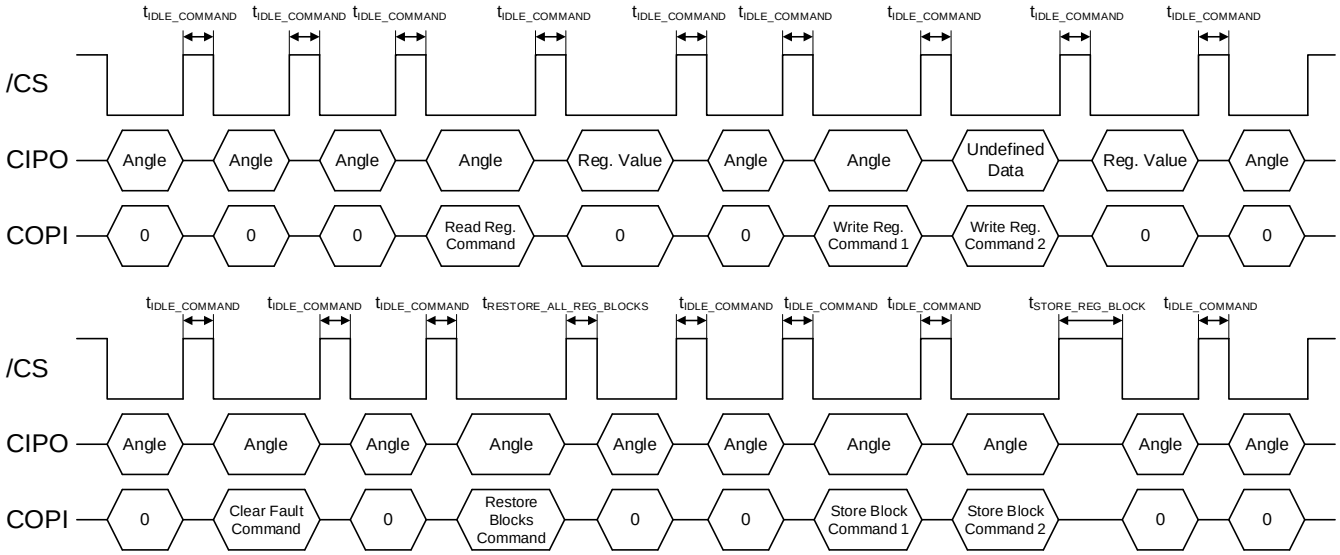


Figure 9: Minimum Idle Time

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Table 4: SPI Timing

Parameter (9)	Description	Min	Max	Unit
$t_{IDLE_COMMAND}$	Idle time between transmissions	120	-	ns
$t_{STORE_REG_BLOCK}$	Time required to store a register block to the NVM	600	-	ms
$t_{RESTORE_ALL_REG_BLOCKS}$	Time required to restore all register blocks from the NVM	240	-	µs
t_{CSL}	Time between /CS falling edge and SCLK falling edge	20	-	ns
t_{SCLK}	SCLK period	40	-	ns
t_{SCLKL}	Low level of the SCLK signal	20	-	ns
t_{SCLKH}	High level of the SCLK signal	20	-	ns
t_{CSH}	Time between the SCLK rising edge and /CS rising edge	20	-	ns
t_{CIPO}	SCLK setting edge to data output valid	-	15	ns
t_{COPI}	Data input valid to SCLK rising edge	15	-	ns

Note:

9) All values are guaranteed by design.

SPI Communication

The sensor supports eight types of SPI operation:

- Read angle
- Read multi-turn
- Read speed
- Read register
- Write register
- Store a single register block to the NVM
- Restore all register blocks from the NVM
- Clear error flags

Each operation has a specific frame structure, described in greater detail below. Table 6 on page 20 shows a summary of these operations.

SPI Read Angle

The refresh period is $1/f_{REFRESH}$. New data is transferred into the output buffer each refresh period. The controller device triggers the reading operation by pulling /CS low.

When a trigger event is detected, the data remains in the output buffer until the /CS signal is pulled high by the controller (see Table 5).

Table 5: Sensor Data Timing

Event	Action
/CS falling edge	Start reading and freeze the output buffer
/CS rising edge	Release the output buffer

A full angle reading requires 16 clock pulses. The angle output value is read with the most significant bit (MSB) first. Figure 10 shows a diagram of a full SPI angle reading.

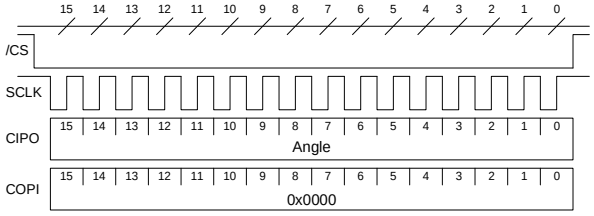

Figure 10: Diagram of a Full 16-Bit SPI Angle Reading

The angle (in degrees) can be calculated with Equation (1):

$$\text{Angle (deg)} = \frac{\text{Angle (dec)}}{2^{16}} \times 360 \qquad (1)$$

If less resolution is sufficient, the angle can be read by sending fewer clock counts since the MSB is first. Figure 11 shows a diagram of a partial 8-bit SPI angle reading.

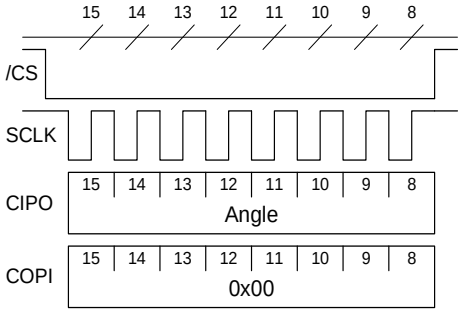

Figure 11: Diagram of a Partial 8-Bit SPI Angle Reading

If there are very fast reading cycles, the MA600A continues sending the same data until the data refreshes. See the General Characteristics section starting on page 8 for the refresh rate.

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SPI Read Multi-Turn or Speed

By sending 32 clock pulses in one frame, the user can obtain the multi-turn or speed information.

The first 16 bits returned on the CIPO line contain the angle value. When the MTSP bit in the PRT register is set to 0 (default setting), the second 16 bits contain the multi-turn count; when MTSP is set to 1, the second 16 bits contain the speed (see Figure 12).

See the Multi-Turn Output section on page 38 for more details on multi-turn.

See the Speed Output and Calculation section on page 37 for more details of speed.

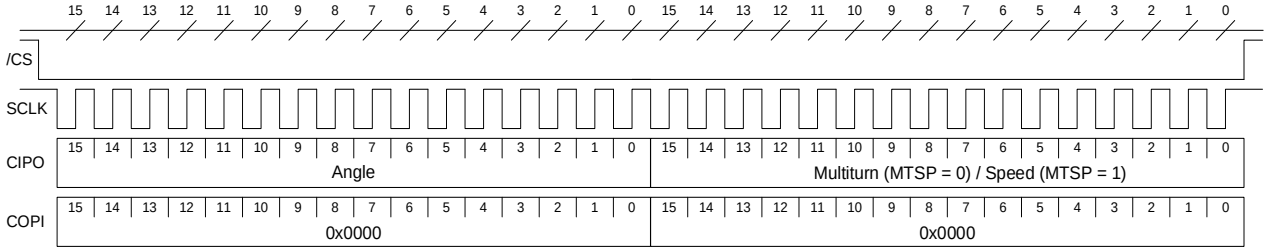
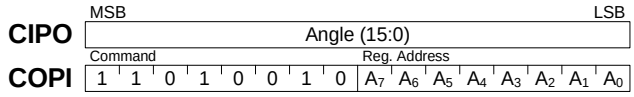


Figure 12: 32-Bit Frame Read Multi-Turn or Speed Operation

SPI Read Register

A read register operation consists of two 16-bit frames. In the first frame, the controller sends a read request, which contains the 8-bit read command followed by the 8-bit register address, and the sensor sends the 16-bit angle value. In the second frame, the sensor sends the 8 most significant bits (MSB) of the angle value followed by the requested 8-bit register value.

The first 16-bit SPI frame (read request) is:



The second 16-bit SPI frame (response) is:

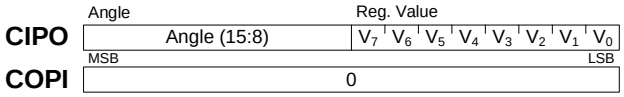


Figure 13 shows a complete transmission.

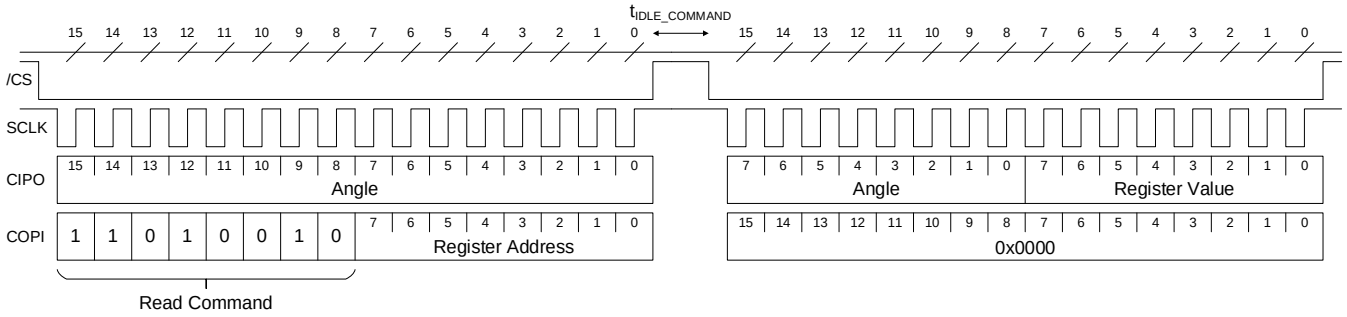
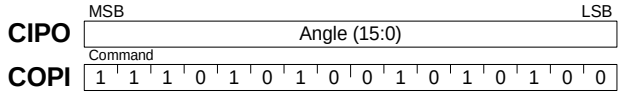


Figure 13: Overview of a Read Register Operation with Two 16-Bit Frames

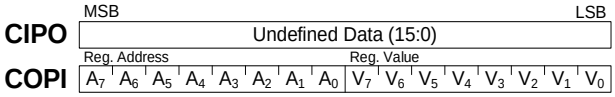
SPI Write Register

A write register operation consists of three 16-bit frames. In the first frame, the controller sends a write request, which contains the 16-bit write command, while the sensor sends the 16-bit angle value. In the second frame, the controller sends the 8-bit register address and the 8-bit value. In the third frame, the sensor sends the 8 MSB of the angle value followed by the newly written 8-bit register value.

The first 16-bit SPI frame (write request) is:



The second 16-bit SPI frame (address and value) is:



The third 16-bit SPI frame (response) is:

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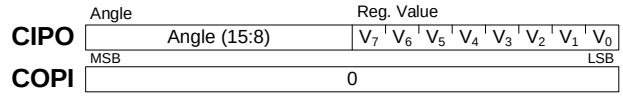
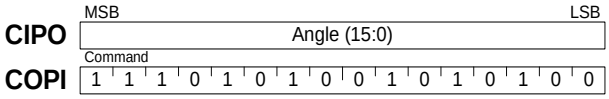
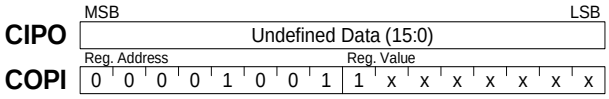


The readback register content can be used to verify the register configurations.

For example, to set the value of the output rotation direction (RD) to counterclockwise (RD bit = 1), write to the DIR register by sending the following first and second frames:





Then send the third frame. If the register is written correctly, the reply is:

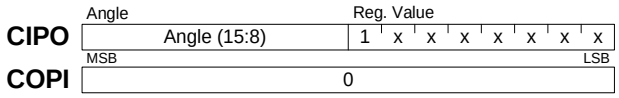


Figure 14 shows a complete transmission.

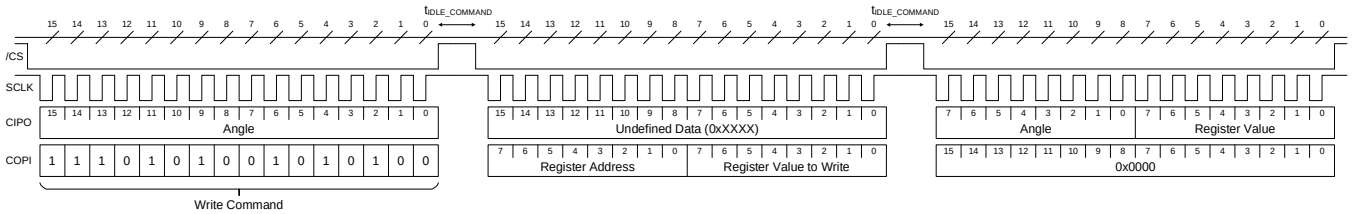


Figure 14: Overview of a Write Register Operation with Three 16-Bit Frames

Non-Volatile Memory (NVM) Operation

The sensor contains a non-volatile memory (NVM) that is divided into two separate memory blocks. Each block contains 32 registers. Block 0 contains registers ZERO0 to RMAPID, and block 1 contains registers CORR0 to CORR31. The values stored in the NVM are automatically loaded into the sensor's registers during start-up.

By using the "Store a Single Register Block to the NVM" SPI operation, the register values in the block are copied to the NVM.

If the user wants to change the value of a register in the NVM, they must follow the steps below:

1. Write the target value to the register with a "Write Register" operation.
2. Check the block number (*B*) to which the register belongs.
3. Use the "Store a Single Register Block to the NVM" operation to store the block (*B*).

It is possible to manually force the restoration of the NVM values to the registers by using the "Restore All Register Blocks" SPI operation.

When the sensor receives an NVM operation ("Store a Single Register Block to the NVM" or "Restore All Register Blocks"), the NVM is busy for the time required to execute the command.

If another NVM command is sent while the NVM is busy, the command is ignored and the ERRMEM bit is set to 1.

SPI Store a Single Register Block to the NVM

Store a single register block operation consists of two 16-bit frames (see Figure 15). The third frame in Figure 15 shows that the other commands must be sent after a minimum time of $t_{STORE_REG_BLOCK}$ (see Table 4 on page 16).

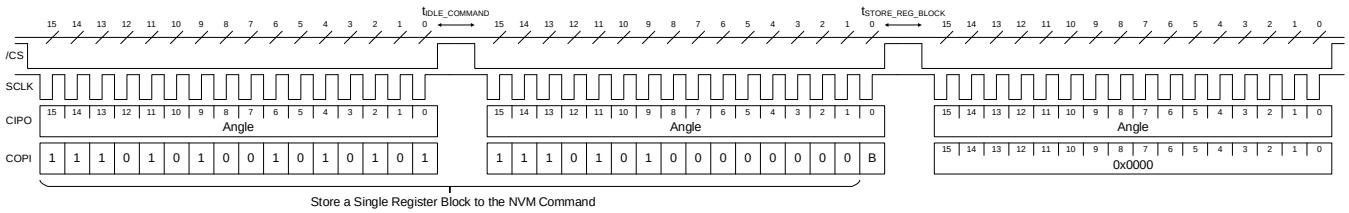


Figure 15: Overview of Store a Single Register Block to the NVM Operation with Three 16-Bit Frames (B = 0 for Block 0, B = 1 for Block 1)

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SPI Restore All Register Blocks from the NVM

A restore all register blocks operation consists of one 16-bit frame. This command restores all register blocks from the NVM (see Figure 16).

The second frame in Figure 16 shows that other commands must be sent after a minimum time of $t_{RESTORE_ALL_REG_BLOCKS}$.

This operation is done automatically (without user intervention) at each start-up.

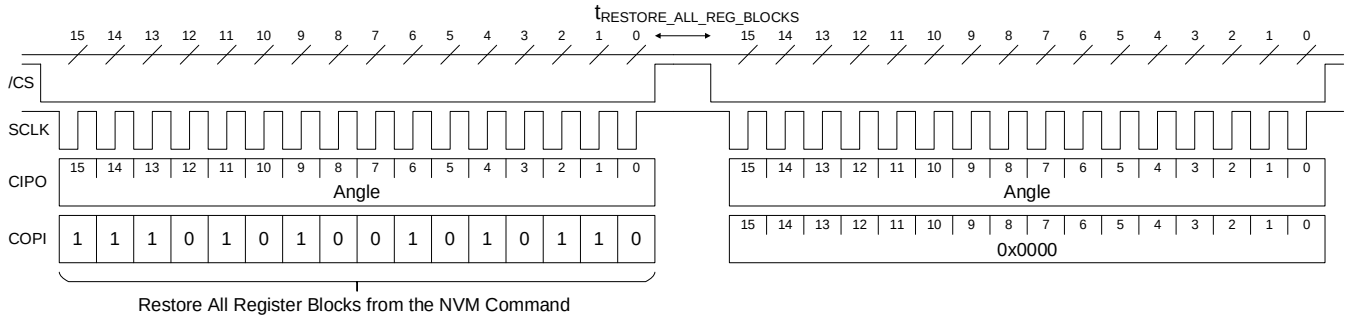

Figure 16: Overview of Restore All Register Blocks from the NVM Operation with Two 16-Bit Frames

SPI Clear Error Flags

A clear error flags operation consists of one 16-bit frame. This command clears all error flags in the STATUS register, including NVMB, ERRCRC, ERRMEM, and ERRPAR (see Figure 17). Other commands should be sent after $t_{IDLE_COMMAND}$.

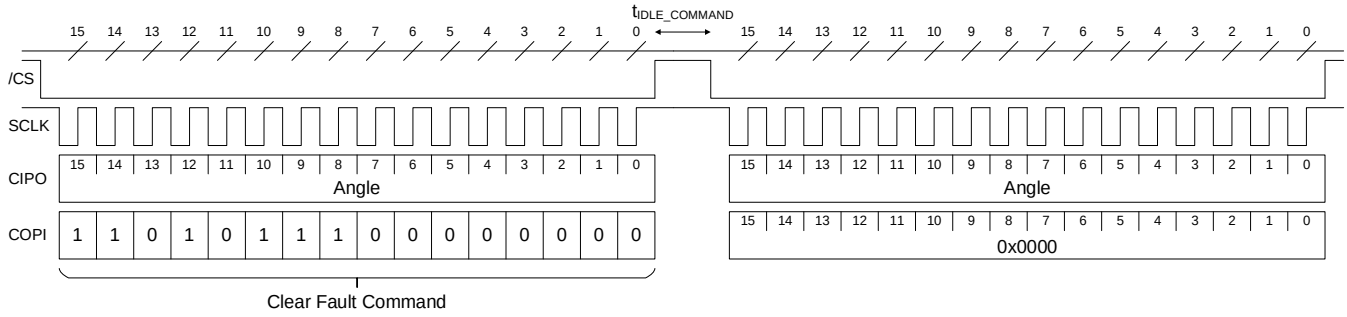

Figure 17: Overview of Clear Error Flags Operation with Two 16-Bit Frames

Table 6 on page 20 shows a summary of all SPI commands.

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Table 6: SPI Commands List Overview

Command Function	Transaction Length	Command		Returned Value on Last Command
Read Angle	1 x 16-bit	0x0000		16-bit angle
Read Multi-Turn	1 x 32-bit	0x00000000		16-bit angle + 16-bit multi-turn
Read Speed	1 x 32-bit	0x00000000		16-bit angle + 16-bit speed
Read Register	2 x 16-bit	1st command	0xD2 (10) + 8-bit reg. address	8-bit angle MSB + 8-bit reg. value
		2nd command	0x0000	
Write Register	3 x 16-bit	1st command	0xEA54 (10)	8-bit angle MSB + 8-bit reg. value
		2nd command	8-bit reg. address + 8-bit reg. value	
		3rd command	0x0000	
Store a Single Register Block to the NVM	2 x 16-bit	1st command	0xEA55 (10)	16-bit angle
		2nd command	0xEA00 (10) for block 0, 0xEA01 (10) for block 1	
Restore All Register Blocks from the NVM	1 x 16-bit	0xEA56 (10)		16-bit angle
Clear Error Flags	1 x16-bit	0xD700 (10)		16-bit angle

Note:

10) These values are in hexadecimal format. For example, 0xD2 indicates 1101 0010 in binary format.

SPI Parity Check

An SPI parity check is enabled by setting the PRT bit in the PRT register to 1. The parity sign is determined by the PRTS bit, where the sign is even by default (PRTS = 0) and can be changed to odd by setting PRTS to 1. When the parity check is enabled, changing the PRTS value leads to the ERRPAR flag becoming active.

When the SPI parity check is enabled, the controller must send one parity bit after the 16-bit command. The MA600A also returns one parity bit after the 16-bit data. Figure 18 shows the SPI read angle with a parity check.

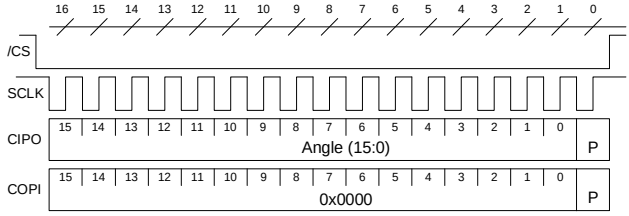

Figure 18: SPI Read Angle When an SPI Parity Check is Enabled

If the parity bit sent by controller is wrong, the error bit (ERRPAR) in the STATUS register is set to 1. See the ERRPAR bit description on page 28 for more details.

Table 7 shows a summary of SPI commands with a parity check.

Table 7: SPI Commands with Parity Check Overview

Command Function	Command Sent by Controller	Returned Value	Action when Parity Sent by Controller Is Wrong
Read Angle	0x0000 + parity bit	16-bit angle + parity bit	ERRPAR = 1
Read Multi-Turn or Speed	0x0000 + parity bit + 0x0000 + parity bit	16-bit angle + parity bit + 16-bit multi-turn/speed + parity bit	ERRPAR = 1
Read/Write Register	Several 17-bit commands, where each command is a 16-bit command + parity bit	Several 17-bit replies, where each reply is a 16-bit reply + parity bit	ERRPAR = 1, the command is discarded
Store/Restore NVM			
Clear Error Flags			

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SPI Angle Parity Check on CIPO

An SPI angle parity check can be enabled by setting the APRT bit in the PRT register to 1.

If the APRT bit = 1, the least significant bit (LSB) of the 16-bit angle output on CIPO is replaced by the angle parity bit. Figure 19 shows an example of angle reading with the angle parity bit, where *AP* stands for the angle parity bit.

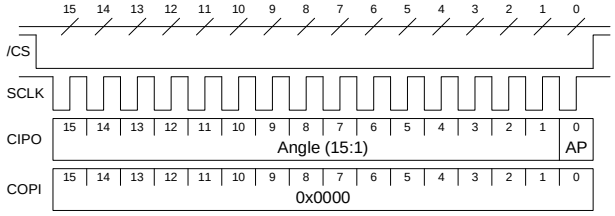


Figure 19: Angle Output with Parity Bit when APRT = 1

When APRT = 1, an SPI angle parity check is applied to all SPI CIPO replies containing a 16-bit angle.

The angle parity bit sign is controlled by the PRTS bit in the PRT register.

An SPI parity check and angle parity check can be enabled at the same time. Figure 20 shows an example of angle reading with both the angle parity bit and SPI parity bit, where *P* stands for the parity bit of the previous 16-bit data.

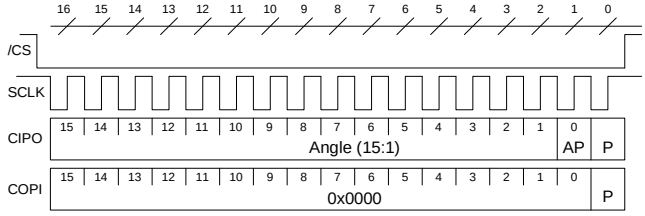


Figure 20: Angle Output with Parity Bit when PRT = 1 and APRT = 1

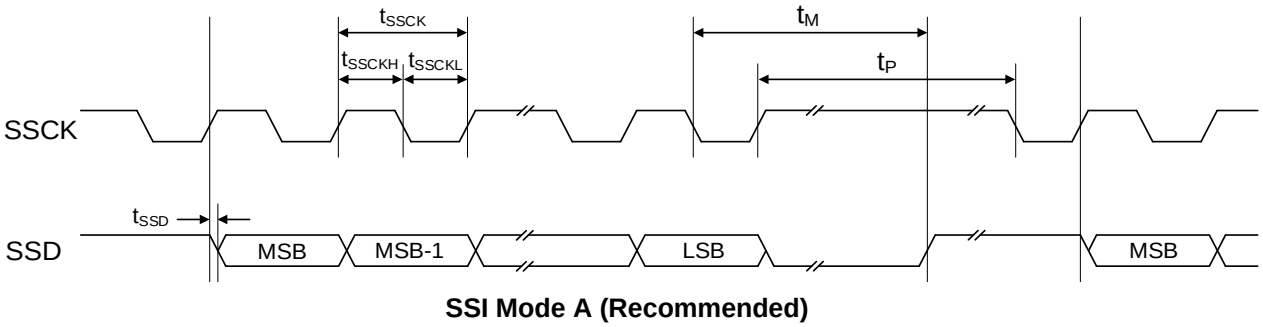
Synchronous Serial Interface (SSI)

The SSI is a 2-wire, synchronous, serial interface, and the sensor operates as a peripheral to the external SSI controller.

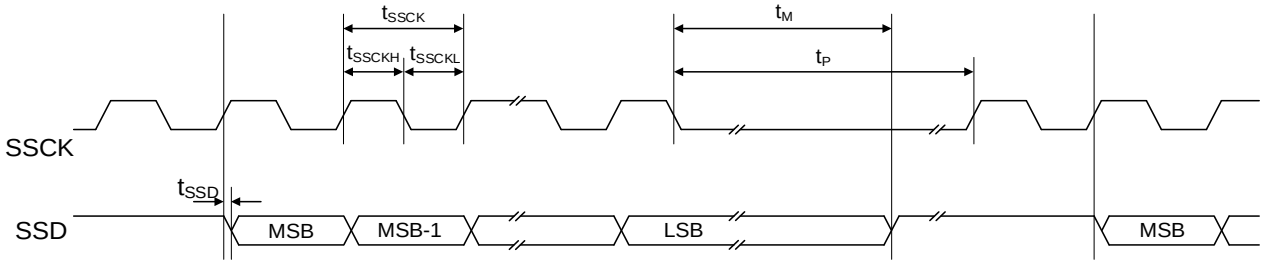
Only angle reading can be done by the SSI. It is not possible to read or write registers using the SSI.

The maximum SSI clock frequency supported by the MA600A is 5MHz. Real maximum data rates depend on the PCB layout quality and signal trace length.

Figure 21 shows the SSI timing for mode A and mode B. Table 8 on page 22 shows the timing for SSI communication.



SSI Mode A (Recommended)



SSI Mode B

Figure 21: SSI Timing for Mode A and Mode B (Both Modes are Supported)

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Table 8: SSI Timing

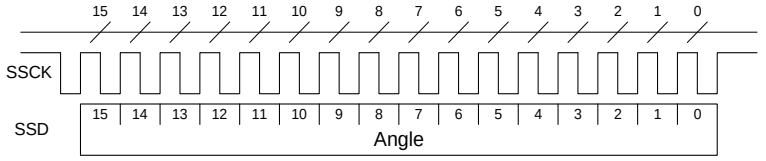
Parameter	Description	Min	Max	Unit
t_{SSD}	Delay between SSCK and SSD edge		81	ns
t_{SSCK}	SSCK period	0.2	16	µs
t_{SSCKL}	Low level of the SSCK signal	0.1	8	µs
t_{SSCKH}	High level of the SSCK signal	0.1	8	µs
t_M	Transfer timeout (monoflop time)	25	-	µs
t_P	Dead time: SSCK high time for the next data reading	40	-	µs

SSI Read Angle

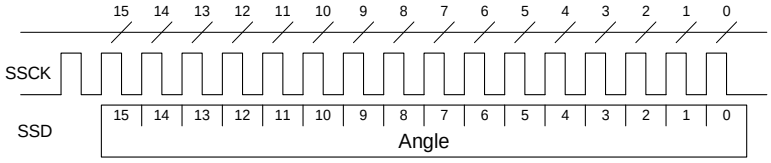
The MSBs are transmitted first. Every refresh period, new data is transferred into the output buffer.

The first clock count is a dummy clock to start the transmission. The first MSB data is then transmitted on the second clock count. The controller device triggers the reading by driving the SSCK signal high.

The MA600A's data length is 16 bits long, meaning a full reading requires one dummy clock and 16 clock counts (see Figure 22). The reading can also be performed with fewer than 17 clock counts. For example, if an application requires only 12-bit angle information, it is sufficient to send the first dummy clock to start the transmission as well as 12 additional clock cycles to read the angle data.



SSI Mode A (Recommended)



SSI Mode B

Figure 22: Diagram of a Full 16-Bit SSI Angle Reading (with First Dummy Clock)

When a trigger event is detected, the data remains in the output buffer until the transfer timeout passes (see Table 9).

Table 9: Sensor Data Timing

Trigger Event	Release of the Output Buffer
First SSCK rising edge after dummy clock	Last SSCK falling edge + timeout (t_M) (see Figure 21 on page 21)

Figure 23 shows the timing for consecutive angle readings.

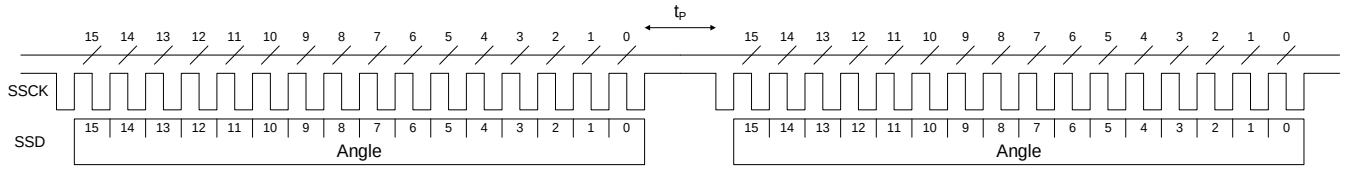


Figure 23: Two Consecutive 16-Bit SSI Angle Readings (with Required Dead Time Between the Frames)

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SSI Parity Check

The SSI parity check is enabled by default. To obtain the parity bit, the user must send one dummy clock and 17 clock counts. The parity bit follows the LSB of the angle data (see Figure 24).

The parity sign is even parity by default and can be configured to odd parity by setting the PRTS bit in the PRT register to 1 with an SPI command.

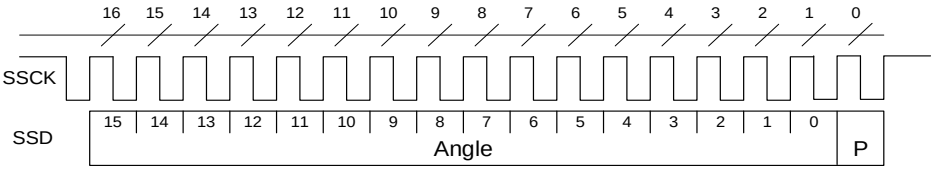

Figure 24: 17-Bit SSI Angle Reading with Parity Check (with First Dummy Clock)

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REGISTER MAP

Table 10: Register Map (11)

#	Block	Hex	Bit[7] (MSB)	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0] (LSB)
0	0	0x00	Z[7:0]							
1		0x01	Z[15:8]							
2		0x02	BCT							
3		0x03	-						ETY	ETX
4		0x04	PPT[2:0]			ILIP				PPT[11]
5		0x05	PPT[10:3]							
7		0x07	NPP			-				
8		0x08	PWMM	PWMF	-					
9		0x09	RD	-						
10		0x0A	DAISY	-						RWM
11		0x0B	OD615	OD243	SPULLIN	-				
12		0x0C	HYS							
13		0x0D	-				FW			
14		0x0E	INTF_SEL			-		DAZ	-	CK100
18		0x12	MTOFFSET[7:0]							
19		0x13	MTOFFSET[15:8]							
26		0x1A	NVMB	-				ERRCRC	ERRMEM	ERRPAR
28		0x1C	MTSP	-	PRT	PRTS	APRT	FTA		FTM
31		0x1F	SUFFIXID							
32	1	0x20	CORR0							
33		0x21	CORR1							
…		…	…							
62		0x3E	CORR30							
63		0x3F	CORR31							
132	4	0x84	-							UR10

Note:

11) “-” indicates bits that are not accessible by the user.

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REGISTERS DESCRIPTION

ZERO0 (0x00)

The ZERO0 register sets the LSB for the zero position (see the Zero Setting section on page 30 for more details).

Bits	Access	Bit Name	Default	Description
7:0	R/W	Z[7:0]	0	8 least significant bits (LSB) of the zero setting.

ZERO1 (0x01)

The ZERO1 register sets the MSB for the zero position (see the Zero Setting section on page 30 for more details).

Bits	Access	Bit Name	Default	Description
7:0	R/W	Z[15:8]	0	8 most significant bits (MSB) of the zero setting.

BCT0 (0x02)

The BCT0 register is for the side-shaft configuration and trims the bias current of the X or Y direction TMR bridge (see the Bias Current Trimming Settings section on page 31 for more details).

Bits	Access	Bit Name	Default	Description
7:0	R/W	BCT	0	Reduces the bias current of the TMR bridge selected via the BCT1 register.

BCT1 (0x03)

The BCT1 register is for the side-shaft configuration and determines the direction (X or Y) in which the TMR bridge bias current is trimmed (see the Bias Current Trimming Settings section on page 31 for more details).

Bits	Access	Bit Name	Default	Description
7:2	N/A	-	N/A	Reserved.
1	R/W	ETY	0	Enables bias current trimming in the Y-direction TMR bridge. 0: Disabled 1: Enabled
0	R/W	ETX	0	Enables bias current trimming in the X-direction TMR bridge. 0: Disabled 1: Enabled

ABZ0 (0x04)

The ABZ0 register is for ABZ configuration and determines the ABZ index parameterization and number of pulses per turn (see the ABZ Incremental Encoder Output section on page 34 for more details).

Bits	Access	Bit Name	Default	Description
7:5	R/W	PPT[2:0]	7	Sets the number of pulses per turn for the ABZ output. 3 least significant bits (LSB) of PPT (see Table 18 on page 35).
4:1	R/W	ILIP	0	Parametrization of the ABZ index pulse (see Figure 36 on page 35).
0	R/W	PPT[11]	0	Sets the number of pulses per turn for the ABZ output. Most significant bit (MSB) of PPT (see Table 18 on page 35).

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ABZ1 (0x05)

The ABZ1 register is for ABZ configuration and determines the pulses per turn (see the ABZ Incremental Encoder Output section on page 34 for more details).

Bits	Access	Bit Name	Default	Description
7:0	R/W	PPT[10:3]	63	7 middle bits of PPT (see Table 18 on page 35). Sets the number of pulses per turn of the ABZ output.

UVW (0x07)

The UVW register is for UWV configuration and determines the number of pole pairs (see the UVW Incremental Encoder Output section on page 36 for more details).

Bits	Access	Bit Name	Default	Description
7:5	R/W	NPP	0	Sets the number of pole pairs for the UVW output (see Table 22 on page 36).
4:0	N/A	-	N/A	Reserved.

PWM (0x08)

The PWM register is for PWM configuration and determines the PWM frequency and mode (see the Absolute Output section on page 36 for more details).

Bits	Access	Bit Name	Default	Description
7	R/W	PWMM	1	Adds error detection to the PWM frame. When PWMM = 1, if ERRCRC, ERRMEM, or ERRPAR are detected, the PWM error and data bands are zero (see Figure 41 on page 37). 0: Disabled 1: Enabled
6	R/W	PWMF	1	Sets the pulse-width modulation output frequency. 0: 1kHz 1: 250Hz
5:0	N/A	-	N/A	Reserved.

DIR (0x09)

The DIR register determines the sensor's positive direction (see the Rotation Direction section on page 31 for more details).

Bits	Access	Bit Name	Default	Description
7	R/W	RD	0	0: Clockwise (CW) 1: Counterclockwise (CCW)
6:0	N/A	-	N/A	Reserved.

IO0 (0x0A)

The IO0 register is for I/O configuration and determines the state of the reduced wire mode (RWM) and daisy chain (see the Special Interfaces section on page 39 for more details).

Bits	Access	Bit Name	Default	Description
7	R/W	DAISY	0	Enables daisy-chain mode. This bit can only be written if UR10 = 1. 0: Disabled 1: Enabled
6:1	N/A	-	N/A	Reserved.

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0	R/W	RWM	0	Enables reduced wire mode. This bit can only be written if UR10 = 1. 0: Disabled 1: Enabled

IO1 (0x0B)

The IO1 register is for I/O configuration and determines the internal circuit of various I/O pins (see the Digital I/O Pin Circuit section on page 39 for more details).

Bits	Access	Bit Name	Default	Description
7	R/W	OD615	0	Determines the output circuits for the IO6, IO1, and IO5 pins. 0: Push-pull 1: Open-drain
6	R/W	OD243	0	Determines the output circuits for the IO2, IO4, and IO3 pins. 0: Push-pull 1: Open-drain
5	R/W	SPULLIN	1	Determines the input circuits for the /CS, SCLK, and COPI pins. 0: Hi-Z 1: Pull-up (for /CS) or pull-down (for SCLK, COPI)
4:0	N/A	-	N/A	Reserved.

HYST (0x0C)

The HYST register sets the hysteresis for the ABZ output (see the ABZ Hysteresis section on page 35 for more details).

Bits	Access	Bit Name	Default	Description
7:0	R/W	HYS	16	Sets the configurable hysteresis used for the ABZ output.

FILT (0x0D)

The FILT register is for filter window configuration and determines the window size of the digital filter (see the Digital Filter Configuration section on page 30 for more details).

Bits	Access	Bit Name	Default	Description
7:4	N/A	-	N/A	Reserved.
3:0	R/W	FW	5	Sets the digital filter window size (see Table 11 on page 30).

IF (0x0E)

The IF register configures the interface (see the Input/Output Matrix section on page 38 for more details).

Bits	Access	Bit Name	Default	Description
7:5	R/W	INTF_SEL	0	Selects the function of the IO1~IO6 pins (see Table 28 on page 39).
4:3	N/A	-	N/A	Reserved.
2	R/W	DAZ	0	Enables the DAZ interface for the incremental encoder output. If enabled, the D signal indicates rotation direction (CW = 0, CCW = 1), while the A and Z signals remain unchanged. 0: Disabled 1: Enabled
1	N/A	-	N/A	Reserved.

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0	R/W	CK100	0	If enabled, the 100kHz system clock is available at the CK100 pin. 0: Disabled 1: Enabled

MT0 (0x12)

The MT0 register sets the multi-turn offset value (see the Multi-Turn Output section on page 38 for more details).

Bits	Access	Bit Name	Default	Description
7:0	R/W* (12)	MTOFFSET[7:0]	0	Sets the 8 least significant bits (LSB) of the multi-turn offset value.

MT1 (0X13)

The MT1 register sets the multi-turn offset value.

Bits	Access	Bit Name	Default	Description
7:0	R/W* (12)	MTOFFSET[15:8]	0	Sets the 8 most significant bits (MSB) of the multi-turn offset value.

STATUS (0x1A)

The STATUS register contains status and error flags. The error bits can be cleared by sending the Clear Error Flags operation (see the Status Byte section on page 38 for more details).

Bits	Access	Bit Name	Default	Description
7	R	NVMB	0	Indicates whether the NVM is busy. 0: The NVM is ready for use 1: The NVM is busy
6:3	N/A	-	N/A	Reserved.
2	R	ERRCRC	0	Indicates whether a CRC error was detected during NVM restoration. 0: No error was detected 1: An error was detected
1	R	ERRMEM	0	Rises to 1 if an “SPI write” is performed while the NVM is busy. 0: No error was detected 1: An error was detected
0	R	ERRPAR	0	Indicates whether a parity error was detected on the COPI line, and SPI operation is ignored. 0: No error was detected 1: An error was detected

PRT (0x1C)

The PRT register configures the parity check (see the SPI Parity Check section on page 20 for more details) and test angle (see the Functional Test section on page 34 for more details).

Bits	Access	Bit Name	Default	Description
7	R/W* (12)	MTSP	0	Determines the data returned by SPI “Read Multi-Turn or Speed” operation. 0: Multi-turn 1: Speed
6	N/A	-	N/A	Reserved.

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5	R/W* (12)	PRT	0	Enables the SPI parity check. 0: Disabled 1: Enabled
4	R/W* (12)	PRTS	0	Determines the sign of parity bit (even/odd). 0: Even 1: Odd
3	R/W* (12)	APRT	0	Enables the 16th bit of the SPI angle data to be replaced by the parity bit. 0: Disabled 1: Enabled
2:1	R/W* (12)	FTA	0	Sets the functional test angle, which is the angle output in functional test mode (FTM = 1). 0: 0° 1: 90° 2: 180° 3: 270°
0	R/W* (12)	FTM	0	Enables functional test mode. When enabled, a reference signal replaces the TMR front-end output as input of the signal treatment circuit. 0: Disabled 1: Enabled

RMAPID (0x1F)

The RMAPID register contains the register map identification number.

Bits	Access	Bit Name	Default	Description
7:0	R	SUFFIXID	0	Contains the suffix for the custom register setting version.

CORR0~CORR31 (0x20~0x3F)

The CORR0~CORR31 registers are for user output calibration (see the User Output Calibration section on page 33 for more details).

Bits	Access	Bit Name	Default	Description
7:0	R/W	CORR0~CORR31	0	User correction table (32 x 8 bits) for linear interpolation.

UR10 (0x84)

The UR10 register unlocks write access to the IO0 register.

Bits	Access	Bit Name	Default	Description
7:1	N/A	-	N/A	Reserved.
0	R/W* (12)	UR10	0	0: Register 10 is write-locked. 1: Register 10 is not write-locked.

Note:

12) R/W* indicates write access to the register only. These values are not stored in the NVM.

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REGISTER SETTINGS

Digital Filter Configuration

The filter window (FW) setting controls the sensor's resolution of the angle output (defined as the ±3σ noise interval), the latency, and the cutoff frequency (f_{CUTOFF}).

Table 11 shows the filter setting options and resulting performance. It is not recommended to use FW 1–4 or 13–15.

Table 11: Filter Settings

FW	τ (µs)	Resolution (bits)	Latency Cancellation at Constant Speed	f_{CUTOFF} (kHz) (13)
0	0	12.3	No	17
5 (default)	40	12.5	Yes	12
6	80	13	Yes	5.8
7	160	13.5	Yes	2.7
8	320	14	Yes	1.3
9	640	14.3	Yes	0.63
10	1280	14.6	Yes	0.31
11	2560	14.8	Yes	0.15
12	5120	15	Yes	0.075

Note:

13) f_{CUTOFF} is defined as the -3dB frequency on the spectrum.

The cutoff frequency is 17kHz when FW = 0. With this setting, the digital filter and latency cancellation are disabled.

See the Typical Characteristics section starting on page 10 for more details on the spectrum and phase for different FW settings.

To accurately model the system and analyze the control loop stability, the front-end signal's transfer function (H_{FE}) can be calculated with Equation (2):

$$H_{FE} = \frac{1}{(1+\tau_{FE}s)^2} \quad (2)$$

The digital filter transfer function (H_{FILTER}) can be calculated with Equation (3):

$$H_{FILTER} = \frac{1+(2+\delta)\tau s}{(1+\tau s)^2} \quad (3)$$

The digital processing adds a propagation delay (τ_{DP}). The sensor transfer function (*H*) can then be calculated with Equation (4):

$$H = H_{FE} \times e^{-\tau_{DP}s} \times H_{FILTER} \quad (4)$$

Where $\delta = \frac{L}{\tau}$. The time constant (τ) can be determined based on Table 11. For the total latency without the digital filter (*L*), see the General Characteristics section starting on page 8.

Figure 25 shows a simplified block diagram of the system's transfer function.

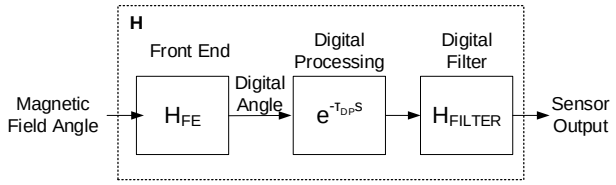

Figure 25: Simplified Block Diagram

Effect of Switching Signals on Resolution

The MA600A's resolution may be negatively affected by the switching signals on its pins within a specific frequency range. This applies both to signals coming from an external source (e.g. /CS) and signals generated by the sensor itself (e.g. the A and B signals from the ABZ interface). Figure 26 shows the relationship between resolution and the signal frequency.

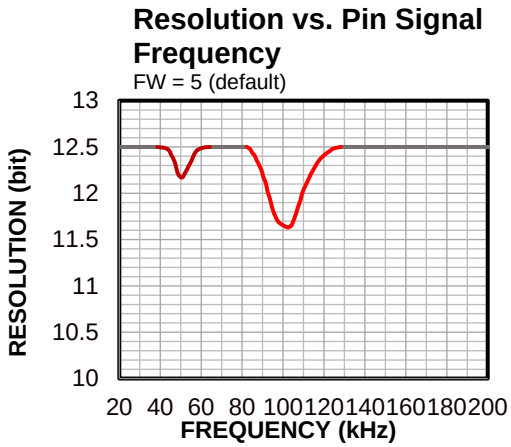

Figure 26: Resolution and Signal Frequency

Zero Setting

The zero position (a_0) of the MA600A can be configured with 16 bits of resolution. The angle output by the MA600A (a_{OUT}) can be calculated with Equation (5):

$$a_{OUT} = a_{RAW} - a_0 \quad (5)$$

Where a_{RAW} is the raw angle provided by the MagAlpha front end.

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The Z parameter is 0 by default and is the zero-angle position. a_0 can be calculated in decimals with Equation (6):

$$a_0 = \frac{Z}{2^{16}} \times 360 \quad (6)$$

Table 12 shows the zero-setting parameter.

Table 12: Zero-Setting Parameter

Z	Zero Position a_0 (deg)
0	0
1	0.005
2	0.011
…	…
65534	359.989
65535	359.995

Zero Position Example

To set the zero position to 20 degrees, the Z parameter can be calculated with Equation (7):

$$Z = \frac{20^\circ}{360^\circ} \times 2^{16} = 3641 \quad (7)$$

In binary format, it is written as 0000 1110 0011 1001.

Rotation Direction

By default, when looking at the top of the package, the angle increases when the magnetic field rotates clockwise (CW) (see Figure 27).

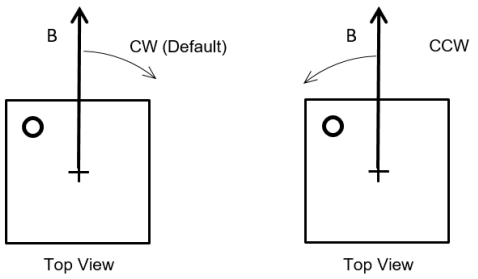

Figure 27: Positive Rotation Direction of the Magnetic Field

Table 13 shows the rotation direction parameter.

Table 13: Rotation Direction Parameter

RD	Positive Direction
0	Clockwise (CW)
1	Counterclockwise (CCW)

Bias Current Trimming Settings

Side-Shaft

When the MA600A is mounted on the side of the magnet, the relationship between the field angle and the mechanical angle is not directly linear. This effect is related to the fact that the tangential magnetic field is typically smaller than the radial field. The field ratio (*k*) can be calculated with Equation (8):

$$k = \frac{B_{RAD}}{B_{TAN}} \quad (8)$$

Where B_{RAD} is the maximum radial magnetic field, and B_{TAN} is the maximum tangential magnetic field (see Figure 28).

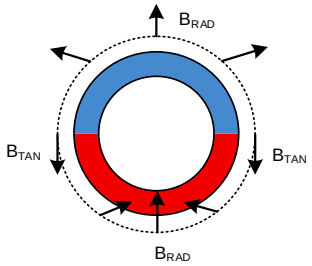

Figure 28: Side-Shaft Field

The *k* ratio depends on the magnet geometry and distance to the sensor. If the *k* ratio does not equal 1, the sensor output response is nonlinear with respect to the mechanical angle. The error curve has the shape of a double sinewave, where *E* is the amplitude of this error (see Figure 30 on page 32).

The bias current of the X or Y TMR bridge can be reduced to recover linearity. The direction in which the bias current is reduced corresponds to the direction where the field amplitude is the largest. The ETX and ETY parameters control this direction. The current reduction is set by the bias current trimming (BCT) parameter, which is an integer from 0 to 255. If the BCT bits value exceeds 200, the compensation result can be affected by the temperature.

In a side-shaft configuration (when the sensor's center is located beyond the magnet's outer diameter), the *k* ratio exceeds 1. For optimal compensation, the radial axis current should be reduced by setting BCT, which can be calculated with Equation (9):

$$BCT = 258 \times \left(1 - \frac{1}{k}\right) \quad (9)$$

Figure 29 on page 32 plots Equation (9).

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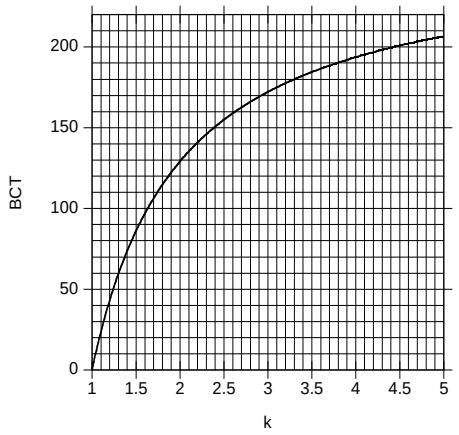

Figure 29: Relationship Between the k Ratio and the Optimal BCT to Recover Linearity

Table 14 shows an example of the BCT settings.

Table 14: Example of BCT Settings

E (deg)	Magnet Ratio (*k*)	BCT
0	1	0
11.5	1.5	86
19.5	2	129
25.4	2.5	155
30	3	172
33.7	3.5	184
36.9	4	194
39.5	4.5	201
41.8	5	207

Determining the *k Ratio*

It is possible to deduce the *k* ratio from the error curve obtained with the default BCT setting (BCT = 0). Rotate the magnet one revolution and record the MA600A's output.

Next, plot the error curve (the difference between the MA600A's output and the real mechanical position vs. the real mechanical position) and extract two parameters: the maximum error (E), and the position of the maximum with respect to a zero crossing (α_M) (see Figure 30). In this scenario, the *k* ratio can be calculated with Equation (10):

$$k = \frac{\tan(E + \alpha_m)}{\tan(\alpha_m)} \quad (10)$$

Figure 30 shows the error curve.

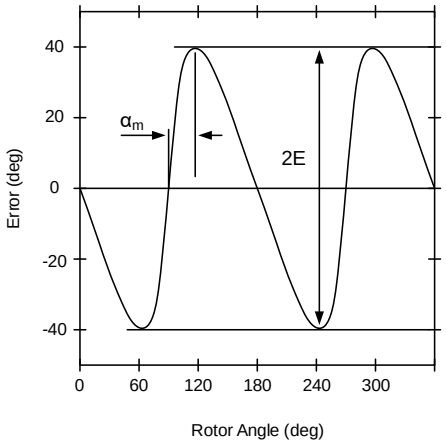

Figure 30: Error Curve in Side-Shaft Configuration with BCT = 0

Figure 31 shows an alternative approach to obtain the *k* parameter.

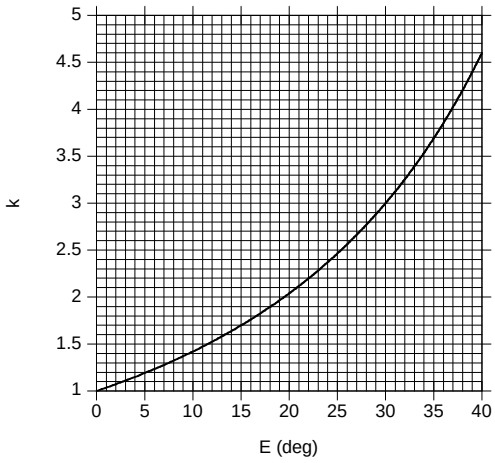

Figure 31: Relationship between the Error Measured with BCT = 0 and the Magnet Ratio (*k*)

Sensor Orientation

The dot marked on the package indicates whether the radial field is aligned with the sensor's X or Y coordinate (see Figure 32).

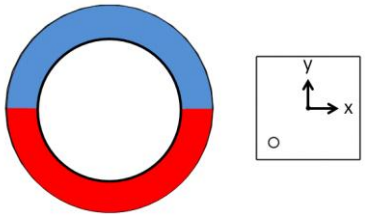

Figure 32: Package Top View with the X and Y Axes

Determine which axis should be reduced based on the qualitative field distribution around a ring (see Figure 28 on page 31).

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For example, Figure 28 on page 31 shows that the field along the sensor's Y-direction is tangential and weaker. This means that the X-axis should be reduced (ETX = 1 and ETY = 0).

If both ETX and ETY are set to 1, the current bias is reduced in both directions the same way (e.g. the linearity is the same as BCT = 0) (see Table 15).

Table 15: Trimming Direction Parameters

ETX	Enable Trimming of the X-Axis
0	Disabled
1	Enabled
ETY	**Enable Trimming of the Y-Axis**
0	Disabled
1	Enabled

Factory Output Linearization

The sensor is factory-calibrated with the precision (see the General Characteristics section starting on page 8) at the nominal magnetic field and room temperature.

User Output Calibration

The MA600A contains a 32-point lookup table for in-system calibration. This enables the removal of errors induced by the magnetic configuration (misalignments and magnet defaults) as well as the intrinsic MA600A error.

The user calibration consists of storing 32 angle correction values ($corr_i$) in the NVM for 32 equidistant positions of the MagAlpha output, which are referred as out_i (out_i = 0°, 11.25°, 22.5°, and so on. Where i = 0, 1…31).

During operation, the sensor makes a linear interpolation using the two out_i surrounding the present output to determine the correct compensation to apply (see Figure 33).

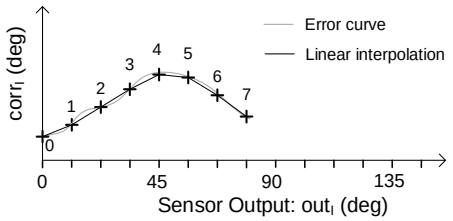

Figure 33: Linear Interpolation for On-Chip Calibration

Figure 34 shows an example comparing the error before and after calibration.

out_i refers to the sensor output with the default zero setting (ZERO bits) and default rotation direction (RD bit). Therefore, calibration should be performed prior to changing the ZERO and RD bits.

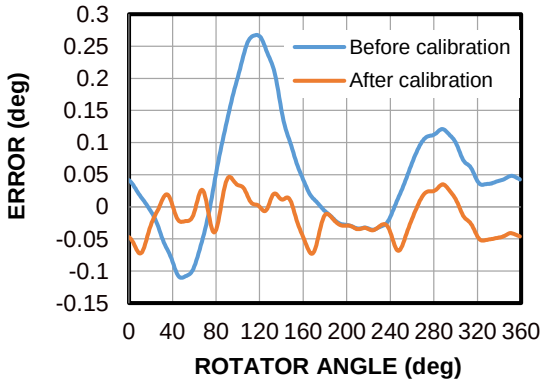

Figure 34: Error Before and After Calibration

Correction Values Calculation

The 32 correction values ($corr_i$) are the negative value of the measured error. $corr_i$ can be calculated with Equation (11):

$$corr_i = -err_i \quad (11)$$

The measured errors (err_i) are the difference between the sensor's output and the ideal output, calculated with Equation (12):

$$err_i = out_i - ref_i \quad (12)$$

where out_i is the MA600A's output in degrees, and ref_i is the real mechanical angle in degrees. ref_i is measured by a reference (e.g. a precise encoder). The mean value of err_i corresponds to the angular distance between the reference encoder zero and the MA600A zero. Therefore, if the zeroes are far apart (e.g. more distant than the INL), then the err_i values have a large common mode value (with respect to the INL). Having a large common mode for an err_i is fine as long as no err_i exceeds the full scale of the correction values: 11.25°. err_i can be offset by a constant value without affecting the linearity after correction. The error without the offset (err'_i) can be calculated with Equation (13):

$$err'_i = err_i - mean(err_i) \quad (13)$$

Once the correction values ($corr_i$ in degrees, which can be notated as $corr_i(deg)$) are obtained, they must be transformed into an integer number ($corr_i(int)$) to be stored to the memory.

Calibration allows for corrections with an accuracy of 0.09°. To save memory space, the correction values $corr_i(int)$ are coded only on 8

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bits, corresponding to a correction ranging from -11.25° to +11.25°. The format of $corr_i(int)$ is signed integer.

If $corr_i(deg) \geq 0$, then $corr_i(int)$ can be calculated with Equation (14):

$$corr_i(int) = \frac{corr_i(deg)}{360°} \times 32° \times 128 \quad (14)$$

If $corr_i(deg) < 0$, then $corr_i(int)$ can be calculated with Equation (15):

$$corr_i(int) = \frac{corr_i(deg)}{360°} \times 32° \times 128 + 256 \quad (15)$$

The user then stores the 32 correction values in decimal format into block 1 (the CORR0~CORR31 registers), which is reserved for calibration.

User Calibration Example

Before starting the calibration, the CORR0~CORR31 registers must be set to 0. As the first step, the 32 correction values are measured and calculated. Table 16 shows the correction values.

Table 16: Calibration Table Example

#	out_i (deg)	$corr_i$(deg)	$corr_i$(int)
0	0	0.45	5
1	11.25	0.33	4
2	22.5	0.12	1
3	33.75	-0.07	255
…	…	…	…
31	348.75	0.53	6

Then store $corr_i(int)$ into the NVM on block 1.

If a high-accuracy reference is not available, the calibration can be done with a magnet rotating at constant speed. The maximum recommended magnet speed is 5krpm. The user calibration flow is described below, and the calculations must be done outside of the MA600A:

- Use the product of the constant speed and time as the reference angle, then calculate the error curve as a function of the MA600A output.
- Extract the first, second, fourth, and eighth harmonics of the error curve to rebuild an accurate error fitting curve to exclude the potential effect of noise.
- At every 11.25°, calculate err_i using the fitting curve and convert the 32 obtained values from degrees to decimal.
- Write the 32 $corr_i$ values into corresponding registers and then store into the NVM.

In principle, user digital calibration can be used instead of BCT adjustment for side-shaft configuration. When the *k* ratio is sufficiently large, the 11.25° range of the digital calibration is not sufficient, and the BCT adjustment should be executed first.

If multiple settings are used, the settings should be executed in the following order:

1. BCT setting
2. User calibration
3. Zero and rotation direction setting

Functional Test

The functional test verifies the integrity of the sensor's signal treatment. When setting the FTM bit to 1, the signal from the TMR front end is replaced by a predetermined reference signal. The system reverts to normal operation as soon as FTM is set back to 0.

With the FTA bits, the reference signal can be virtually rotated by 90-degree steps (see Table 17).

Table 17: Functional Test Mode

FTM	FTA	Angle Output (deg)
1	00	0
1	01	90
1	10	180
1	11	270

ABZ Incremental Encoder Output

The MA600A's ABZ output emulates an incremental encoder (e.g. an optical encoder) to provide logic pulses in quadrature (see Figure 35 on page 35). Compared to signal A, signal B is shifted by a quarter of the pulse period.

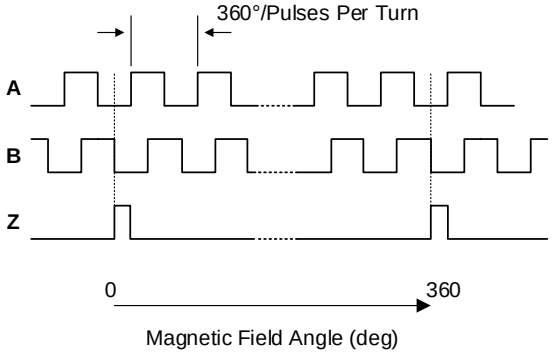

Figure 35: ABZ Output Timing

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Across one revolution, signal A pulses *n* times, where *n* is configurable between 1 pulse and 4096 pulses per revolution. The number of pulses per channel per revolution is configured by setting the PPT bits, which consists of 12 bits split between the ABZ0 and ABZ1 registers (see Table 10 on page 24). The factory default is 512 pulses per turn. Table 18 shows how to configure PPT to set the required resolution.

Table 18: PPT Configuration

PPT	Pulses per Turn	Edges per Turn	
0000 0000 0000	1	4	Min
0000 0000 0001	2	8	
0000 0000 0010	3	12	
0000 0000 0011	4	16	
…	…	…	…
0111 1111 1110	2047	8188	
0111 1111 1111	2048	8192	
…	…	…	…
1111 1111 1101	4094	16376	
1111 1111 1110	4095	16380	
1111 1111 1111	4096	16384	Max

For example, to set 120 pulses per revolution (480 edges), set PPT to 120 - 1 = 119 (binary: 0000 0111 0111). Table 19 shows the required settings for the ABZ0 and ABZ1 registers.

Table 19: Registers ABZ0 and ABZ1 Setting

Reg	B7	B6	B5	B4	B3	B2	B1	B0
ABZ0	1	1	1	0	0	0	0	0
ABZ1	0	0	0	0	1	1	1	0

Signal Z (zero or index) is raised only once per turn at the zero-angle position. The Z pulse's position and length can be configured via ILIP in the ABZ1 register (see Figure 36).

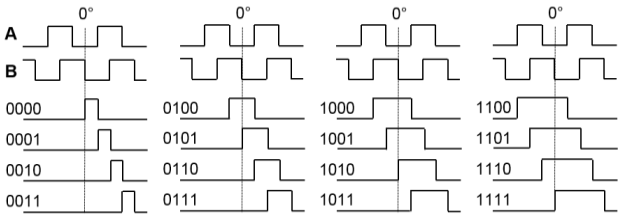

Figure 36: ILIP Parameter Effect on Index Shape

By default, the ILIP parameter is 0000. The index rising edge is aligned with channel B's falling edge, and the index length is half of the A or B pulse length.

ABZ Hysteresis

The hysteresis is set by the HYS bits. The hysteresis (*H*) in degrees can be calculated with Equation (16):

$$H\ (deg) = 2.8 \times \frac{HYS}{256} \quad (16)$$

Table 20 shows the HYS configuration.

Table 20: HYS Configuration

HYS	H (deg)
00000000	0
00000001	0.011
00000010	0.022
…	…
11111110	2.778
11111111	2.789

Figure 37 shows the incremental output hysteresis.

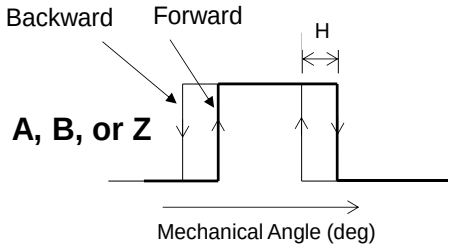

Figure 37: Incremental Output Hysteresis

Table 21 on page 36 shows the recommended settings of HYS and the hysteresis to avoid spurious transitions.

Table 21: Recommended Settings of HYS

FW	Resolution (Bit)	HYS (decimal)	Hysteresis (deg)
0	12.3	22	0.24
5 (default)	12.5	16	0.18
6	13	11	0.12
7	13.5	7	0.08
8	14	5	0.05
9	14.3	4	0.04
10	14.6	3	0.03
11	14.8	3	0.03
12	15	3	0.03

DAZ Interface

For angular speed-related applications, the ABZ interface can be converted to DAZ (where D is the direction, A is the pulsing signal, and Z is the index) by configuring the DAZ bit to 1.

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In this configuration, the D signal indicates clockwise (CW) (logic 0) or counterclockwise (CCW) (logic 1) magnetic field rotation. The A and Z signals remain unchanged compared to the ABZ interface.

UVW Incremental Encoder Output

The UVW output emulates the three Hall switches that are typically used for the block commutation of a 3-phase brushless motor. The three logic signals have a duty cycle of 50% and are shifted by 60° relative to each other (see Figure 38).

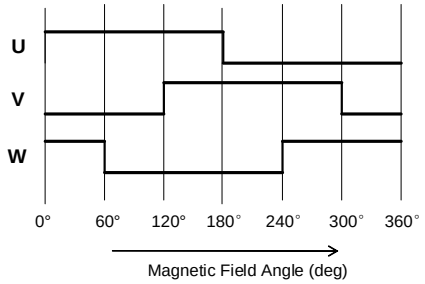

Figure 38: UVW Output for 1 Pole Pair Rotor during Rotation

If the number of the rotor's pole pairs exceeds the number of pole pairs of the target magnet, then the MA600A generates more than one UVW cycle per revolution by dividing the digital angle into the required number of commutation steps per 360 degree revolution. The NPP bits sets the number of emulated pole pairs and the corresponding commutation step angle for the UVW signals.

Table 22 shows the rotor pole pair options.

Table 22: Number of UVW Pole Pairs

NPP	Pole Pairs	States per Revolution	State Width (deg)
000 (default)	1	6	60
001	2	12	30
010	3	18	20
011	4	24	15
100	5	30	12
101	6	36	10
110	7	42	8.6
111	8	48	7.5

Figure 39 shows an example of the 30° UVW commutation signal spacing for a 4-pole (2-pole pair) motor.

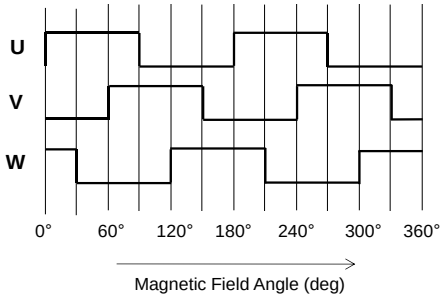

Figure 39: UVW Commutation Signals for a 4-Pole (2-Pole Pair) Motor

UVW Hysteresis

A hysteresis exceeding the output noise is introduced on the UVW output to avoid any spurious transitions (see Figure 40).

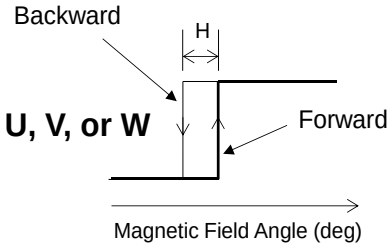

Figure 40: Hysteresis of the UVW Signal PWM

The UVW hysteresis is also set by HYS and is subject to the same recommendations (see Table 20 on page 35).

Absolute Output

This output provides a logic signal with a duty cycle corresponding to the magnetic field angle.

The signal frame consists of four different segments:

- Start band (always high)
- Error
- Data
- End band (always low)

Figure 41 shows one period of the PWM signal.

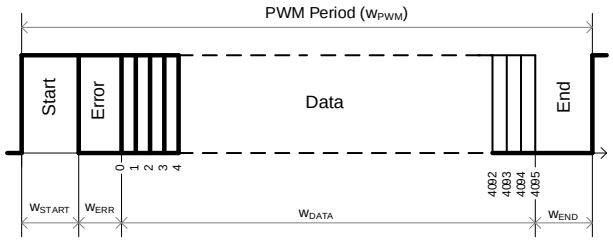

Figure 41: PWM Frame Composed of Four Bands (Start, Error, Data, End)

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To display errors in the PWM frame, enable the PWMM parameter. Under normal conditions, the error band (W_{ERR}) is 1.

W_{ERR} is 0 if one of the following flags in the STATUS register is raised to 1:

- ERRCRC
- ERRMEM
- ERRPAR

If the PWMM bit is enabled and an error is detected, then the data (W_{DATA}) remains at 0.

The frequency can be selected via the PWMF bit. Table 23 shows the PWM frequency selection.

Table 23: PWM Frequency Selection

PWMF	PWM Frequency
0	1kHz
1	250Hz

Table 24 shows the PWM time durations in counts.

Table 24: PWM Time Duration in Counts

PWMM	PWMF	W_{PWM}	W_{START}	W_{ERR}	W_{DATA}	W_{END}
0	0	4119	16	0	4095	8
0	1	4119	16	0	4095	8
1	0	4119	12	4	4095	8
1	1	4119	12	4	4095	8

Speed Output and Calculation

When the MTSP bit in the PRT register is set to 1, the user can obtain the 16-bit speed output from SPI communication (see the SPI Read Multi-Turn or Speed section on page 17 for more details).

The speed is transmitted as a signed 16-bit number using two's complement representation. When calculating the signed decimal value, the user must multiply the MSB of the 16-bit speed value by -1 instead of +1.

The speed scale is 5.722rpm/LSB, which is based on a 100kHz inner clock. Therefore, the measured speed range is from -187498rpm to +187492rpm (see Table 25).

Table 25: Speed Conversion

16-Bit Signed Value	Signed Decimal Value	Speed (rpm)
0000 0000 0000 0000	0	0
0000 0000 0000 0001	1	5.722
1111 1111 1111 1111	-1	-5.722
1000 0000 0000 0000	-32768	-187498.50
0111 1111 1111 1111	32767	187492.78

Speed Output Example

If the readback 16-bit signed speed value is 1110 0100 1110 1010, then the speed in decimal format can be calculated with Equation (17):

$$\text{Speed (Decimal)} = -1\times2^{15}+1\times2^{14}+1\times2^{13}+ +1\times2^{10}+1\times2^{7}+1\times2^{6} +1\times2^{5}+1\times2^{3}+1\times2 = -6934 \quad (17)$$

The corresponding speed can be calculated with Equation (18):

$$\text{Speed (rpm)} = -6934 \times 5.722 = -39676.35 \quad (18)$$

Table 26 shows the speed output's resolution, time constant, and cutoff frequency.

Table 26: Speed Output Typical Parameters

Resolution at 5krpm (Bits)	Time Constant (τ) (μs)	Cutoff Frequency (Hz)
9.5	320	500

If the user wants to monitor the clock frequency and achieve a more precise speed calculation, the clock related to the speed scale (S_{SPEED}) can be output on the CK100 pin by setting the CK100 bit in the IF register to 1.

The relationship between S_{SPEED} and the CK100 frequency in kHz (f_{CK100}) can be calculated with Equation (19):

$$S_{SPEED}\ (\text{rpm/LSB}) = 5.722 \times \frac{f_{CK100}}{100} \quad (19)$$

Multi-Turn Output

If the MTSP bit in the PRT register is set to 0 (default setting), the user can obtain the 16-bit multi-turn output from SPI communication (see the SPI Read Multi-Turn or Speed section on page 17 for more details).

When the angle detected by the MA600A passes the zero position in a positive direction (CW), the multi-turn count increases by 1; when the detected angle passes the zero position in a negative direction (CCW), the multi-turn count decreases by 1.

It is possible to set a multi-turn offset by configuring MTOFFSET in the MT0 and MT1 registers. The multi-turn count (MT) returned by

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the sensor is computed by adding the offset to the measured multi-turn (MT_{MEAS}).

MT can be calculated with Equation (20):

$$MT = MT_{MEAS} + MTOFFSET \quad (20)$$

MT_{MEAS} and MTOFFSET are set to 0 at system start-up. Consider that the MTOFFSET setting cannot be stored to the NVM. The user must set MTOFFSET after each start-up event if the offset is required.

Multi-turn is a signed 16-bit value. The user must multiply the MSB of the 16-bit multi-turn value by -1 instead of +1 (see Equation (17) on page 37).

The measured multi-turn range is from -32768 to +32767 (see Table 27).

Table 27: Multi-Turn Conversion

16-Bit Signed Value	Signed Multi-Turn Decimal Value
0000 0000 0000 0000	0
0000 0000 0000 0001	1
1111 1111 1111 1111	-1
1000 0000 0000 0000	-32768
0111 1111 1111 1111	32767

Status Byte

The STATUS register contains one status bit (NVMB) and three error bits (ERRPAR, ERRMEM, and ERRCRC) that trigger a flag when some errors are detected. These bits can be cleared by sending the Clear Error Flags operation.

NVMB

When the Store a Single Register Block to the NVM operation or the Restore All Register Blocks from the NVM operation is sent to the MA600A, the NVM is busy until the operation is executed. During this busy period, the NVMB status bit is temporarily set to 1 and then reset back to 0 after the operation is executed.

ERRMEM

If a command triggers NVM access (store or restore) while the NWM is busy, it is ignored and the ERRMEM bit is set to 1.

ERRPAR

When a parity check is enabled by PRT, the controller must send a parity bit on the COPI line after the 16-bit command.

The MA600A checks the parity of this 17-bit long frame. If a parity error occurs, the command is discarded and the ERRPAR bit is set to 1. The angle data is returned in the next frame.

When a parity check is enabled, if the user only sends a 16-bit command, ERRPAR is not asserted and the command is discarded.

ERRCRC

The restoration of register values from the NVM is secured by a CRC algorithm. A mismatch between the generated CRC result with the previously stored value is flagged by the ERRNVM bit being asserted (set to 1).

Input/Output Matrix

The function of the digital input/output (I/O) pins (IO1~IO6) can be set by the INTF_SEL bits. Table 28 on page 39 shows the I/O matrix, where "/" means the signal is inverted.

Table 28: I/O Matrix

INTF_SEL	IO6	IO1	IO5	IO2	IO4	IO3
000 (default)	U	V	W	A	B	Z
001	U	V	W	SSD	SSCK	PWM
010	SSCK	SSD	PWM	A	B	Z
011	U	V	W	/V	/U	/W
100	/B	/A	/Z	A	B	Z
101	U	V	W	-	-	-
110	-	-	-	A	B	Z
111	SSCK	SSD	PWM	-	-	-

Digital I/O Pin Circuit

The digital I/O pins (IO1~IO6) are set to push-pull by default and can be changed to open drain to allow I/O voltages different from V_{DD} (up to 5.5V). If the I/O pin is set as SSCK by the INTF_SEL bits, then neither OD615 nor OD243 can affect SSCK.

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Table 29 shows the internal circuit of the IO6, IO1, and IO5 pins.

Table 29: IO6, IO1, and IO5 Internal Circuit

OD615	Internal Circuit
0 (default)	Push-pull
1	Open drain

Table 30 shows the internal circuit of the IO2, IO4, and IO3 pins.

Table 30: IO2, IO4, and IO3 Internal Circuit

OD243	Internal Circuit
0 (default)	Push-pull
1	Open drain

Figure 42 shows the internal circuits for IO1~IO6.

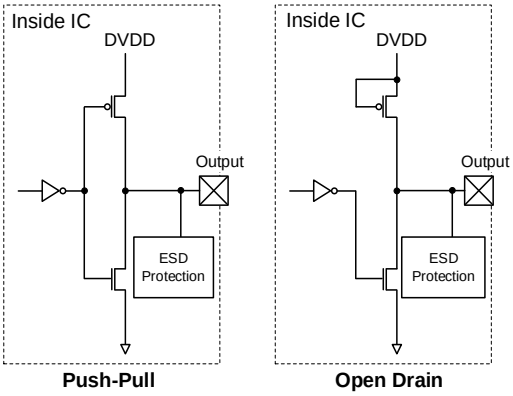

Figure 42: Output Circuits Inside IC for IO1 to IO6

The SPI input pins (/CS, SCLK, and COPI) are configured as pull-up or pull-down by default.

If required, the SPI inputs can be set to a high-impedance (Hi-Z) state by the SPULLIN parameter (see Table 31). When the internal pin's impedance is high, it is recommended to pull SCLK and COPI to GND externally and pull /CS to DVDD to prevent any voltage buildup and inadvertent configuration when the SPI is idle (e.g. high /CS).

Table 31: SPI Input Pin Circuit

SPULLIN	SPI Input Pins	
	/CS	SCLK, COPI
0	Hi-Z	Hi-Z
1 (default)	Pull-up	Pull-down

Figure 43 shows the inside circuit of the SPI inputs.

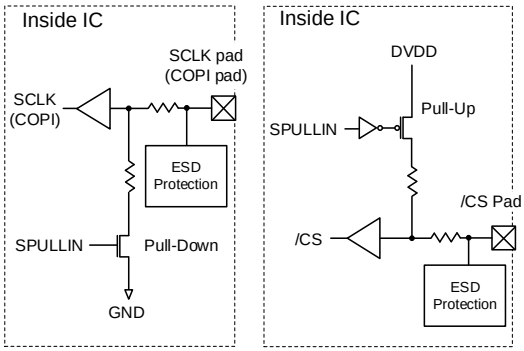

Figure 43: Circuit of the SPI Input Pins in the IC

The SPI output pin (CIPO) is configured as push-pull when the SPI is active. CIPO is configured as pull-down by default when the SPI is idle.

Special Interfaces

The MA600A supports special interfaces such as reduced wire mode (RWM) and daisy chain (DAISY), which provide more flexibility to communicate with the controller.

The DAISY and RWM bits in the IO0 register can disable the SPI communication permanently.

A security mechanism is built in to avoid accidental configuration of the IO0 register.

The security mechanism process is described below:

- By default, the IO0 register is locked, meaning the RWM and DAISY bits cannot be written.
- To unlock the IO0 register, the UR10 bit must be enabled.
- RWM or DAISY mode are effective only when the UR10 bit is reset to zero.

To enable RWM or DAISY mode for temporary testing purposes, follow the steps below:

1. Set the UR10 bit to 1.
2. Set the RWM or DAISY bit to 1.
3. Set the UR10 bit to 0.

At this stage, RWM or DAISY mode is enabled. After shutting down and starting up, the MA600A returns to normal SPI mode.

To switch to RWM or DAISY mode permanently, follow the steps below:

1. Set the UR10 bit to 1.
2. Set the RWM or DAISY bit to 1.

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3. Store register block 0 to the NVM.
4. Set the UR10 bit to 0 or shut down and start up the MA600A.

Reduced Wire Mode

The MA600A supports reduced wire mode by setting the RWM bit to 1.

Reduced wire mode enables the user to configure the chip during a set-up stage, and then transforms the SPI pin into outputs with other functionalities for normal operation to save three connections.

Table 32 shows the RWM and redirection of pin functionality.

Table 32: RWM and Redirection of Pin Functionality

RWM	Pin 4	Pin 5	Pin 7	Pin 12
0 (default)	COPI	/CS	CIPO	SCLK
1	IO3	IO4	CIPO	IO2

For example, if only the ABZ output is required, the user can configure the ABZ-related parameters first via SPI communication, then redirect the ABZ signal to the SPI pins. In this case, no additional wiring is needed at IO2, IO3, and IO4. A similar process applies if only UVW, SSI, or PWM is required. The functionality of IO2~IO4 is determined by the INTF_SEL bits.

Daisy Chain

When connecting multiple sensors on the same bus, a daisy-chain configuration enables saving device, and so on. Figure 45 shows an example of the SPI read angle for *n* daisy-chained MA600A devices.

the I/O pins. Daisy-chain mode is enabled by setting the DAISY bit to 1.

In this mode, the CIPO data output of each peripheral sensor is chained to the COPI data input of the next peripheral sensor. The CIPO data output from the last peripheral sensors is connected back to the controller's CIPO input (see Figure 44).

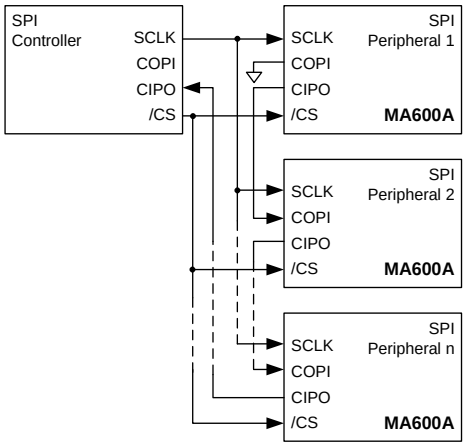

Figure 44: Daisy Chain Mode Configuration

In daisy-chain mode, data can only be read. If *n* is the number of connected devices, (*n* x 16) clock counts are required to read the data of all sensors. The SPI bus chip selection signal (/CS) should remain low during the (*n* x 16) clock counts.

The first 16 bits are the angle data from the last peripheral (*n*) device in the chain, followed by the 16-bit angle data from the preceding (*n* - 1)

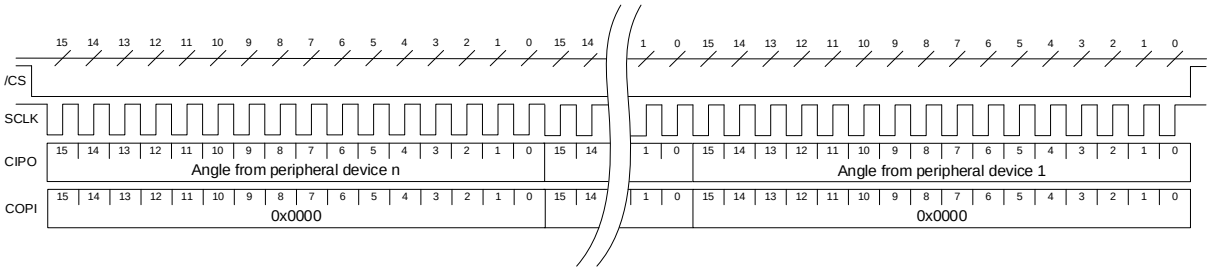

Figure 45: SPI Read Angle for *n* Daisy Chained MA600A Devices

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APPLICATION INFORMATION

Electrical Mounting and Power Supply Decoupling

The two decoupling capacitors are connected to the supply lines (AVDD and DVDD) via a low-impedance path (see Figure 46).

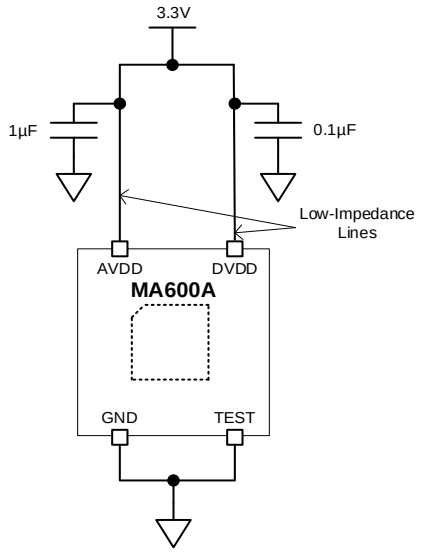

Figure 46: Power Supply Decoupling

If the decoupling capacitors are placed close to the sensor, the target magnetic field may be influenced and negatively impact the sensor's accuracy (INL) due to the MA600A's high accuracy. For example, an SMD capacitor (0603) placed 3mm from the MA600A's center can create a second harmonic nonlinearity up to 0.2°. To avoid magnetic interference that affects sensor accuracy, it is recommended to place the capacitor at a distance of at least 5mm from the MA600A's center. A larger distance further prevents the capacitor magnetic interference.

Keep the high-current path and ground as far away from the MA600A as possible to prevent potential interference.

It is recommended to float the MA600A's exposed pad to minimize mechanical stress.

SPI Signals Routing On PCB

Typically, a direct connection between the sensor and controller SPI pins is sufficient to ensure a proper data transfer across the SPI bus. However, in specific situations (e.g. long signal traces, external EMI presence), it is possible to improve signal integrity by making special considerations during the PCB design, in particular for the SCLK line. A list of guidelines are listed below.

- Properly shield all SPI signals (CIPO, COPI, SCLK, and /CS) with a GND plane on both sides of each trace, as well as the GND plane underneath the SPI signals.
- Place vias alongside the SPI signal traces to connect the top and bottom GND planes.
- To avoid EMI issues, route the SCLK signal away from the other SPI signals and noise sources. The distance should be at least three times that of the SCLK trace width.
- Insert an RC low-pass filter on SCLK (see Figure 47 on page 43). This RC filter must be located close to the sensor. It is recommended to use a 200Ω serial resistor with a 10pF shunt capacitor to obtain an 80MHz filter cutting frequency.
- Use a star topology for the GND connection and keep it as direct and short as possible to avoid ground loops.
- Insert RC low-pass filters on the CIPO and COPI signals (see Figure 47 on page 43). The RC filter on COPI must be located close to the controller, while the filter on CIPO must be located close to the sensor. It is recommended to use a 200Ω resistor with a 10pF capacitor.
- Avoid a significant trace length mismatch between the SPI signals, especially between the CIPO, COPI, and SCLK signals. These signals should have similar propagation delays.
- If possible, avoid placing vias on the SCLK signal.

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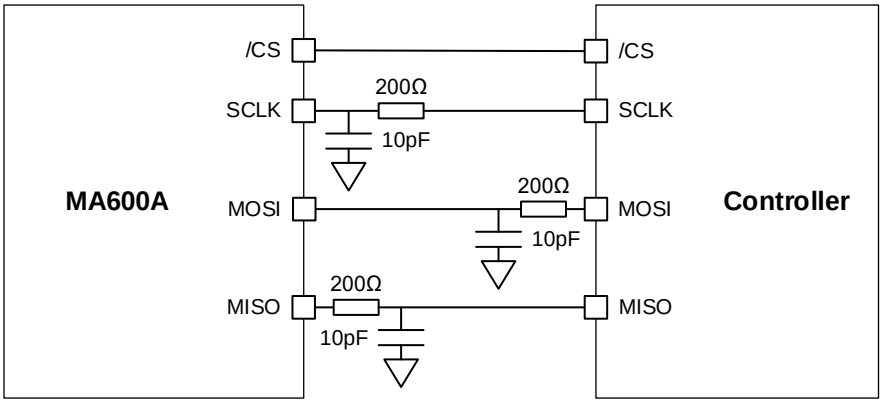

Figure 47: Example of RC Low-Pass Filters on the SPI Signals

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TYPICAL APPLICATION CIRCUIT

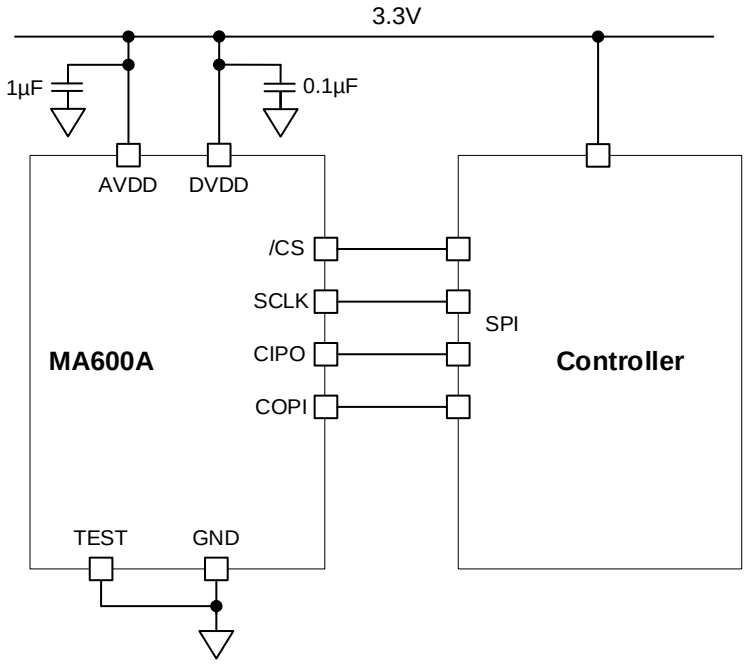

Figure 48: Typical Application Circuit (Configuration Using the SPI)

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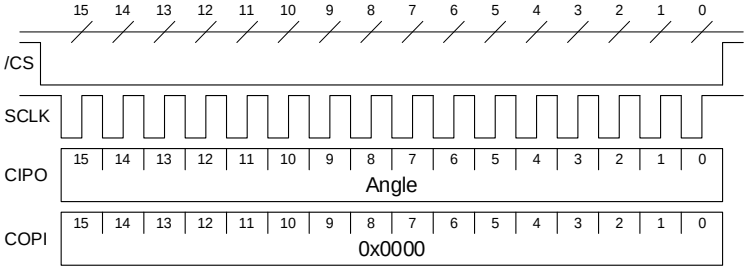
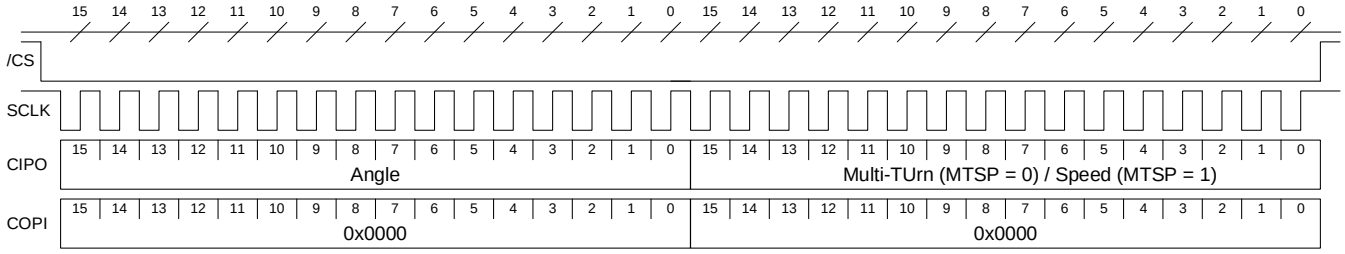
APPENDIX A: SPI COMMUNICATION CHEATSHEET

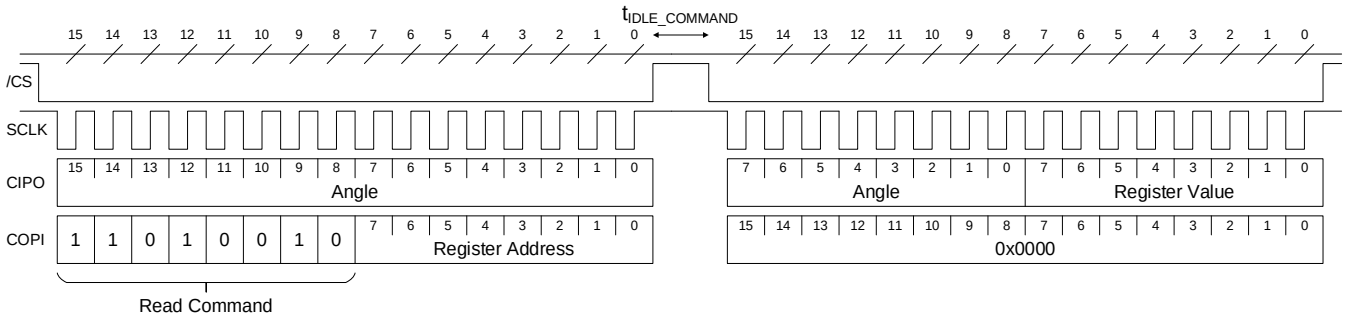
Read Angle (see the SPI Read Angle section on page 16)



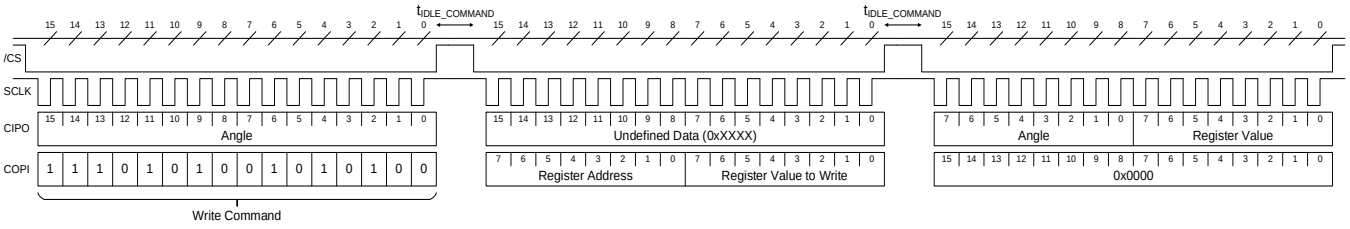
32-Bit Frame Read Multi-Turn or Speed Operation (see the SPI Read Multi-Turn or Speed section on page 17)



Read Register (see the SPI Read Register section on page 17)



Write Register (see the SPI Write Register on page 17)



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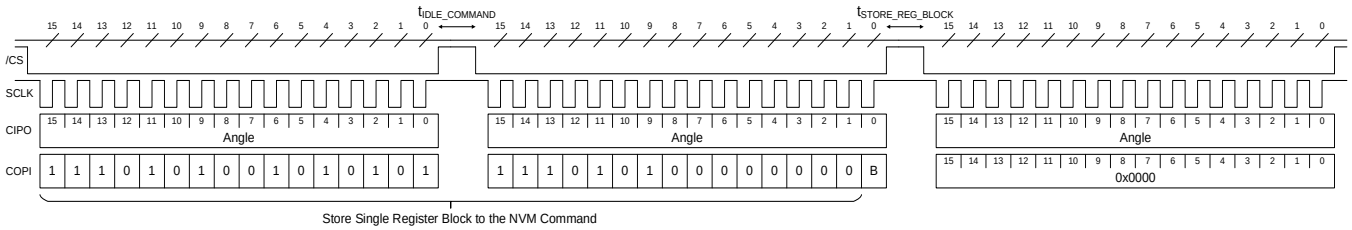
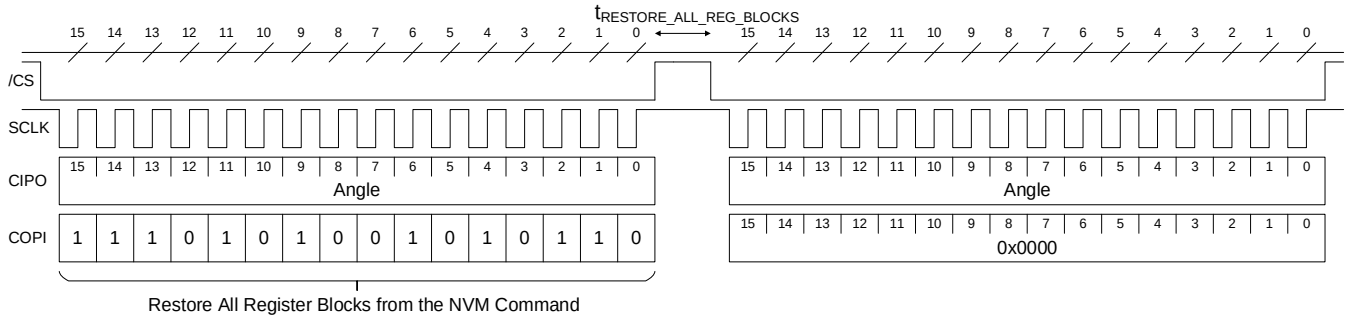
APPENDIX A: SPI COMMUNICATION CHEATSHEET *(continued)*

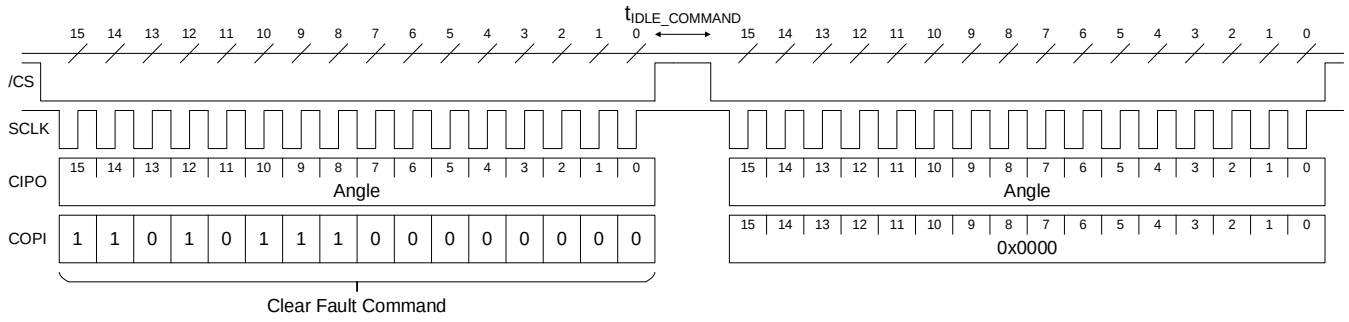
Store a Single Register Block to the NVM (see the SPI Store a Single Register Block to the NVM section on page 18)



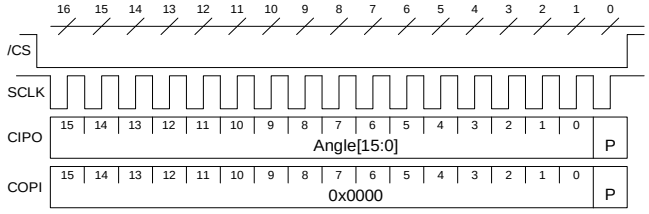
Restore All Register Blocks from the NVM (see the SPI Restore All Register Blocks from the NVM section on page 19)



Clear Error Flags (see the SPI Clear Error Flags section on page 19)



Read Angle when SPI Parity Check Is Enabled (see the SPI Parity Check section on page 20)



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APPENDIX B: DEFINITIONS

Resolution (3σ noise level) Smallest angle increment distinguishable from the noise. The resolution is measured by computing three times σ (the standard deviation in degrees) taken over 1,000 data points at a constant position. The resolution in bits is obtained with log2(360 / 6σ).

Refresh Rate Rate at which new data points are stored in the output buffer.

ABZ Update Rate Rate at which a new ABZ state is computed. The inverse of this rate is the minimum time between two ABZ edges.

ABZ Jitter The jitter characterizes how far a particular ABZ edge can occur at an angular position different from the ideal position (see Figure B1).

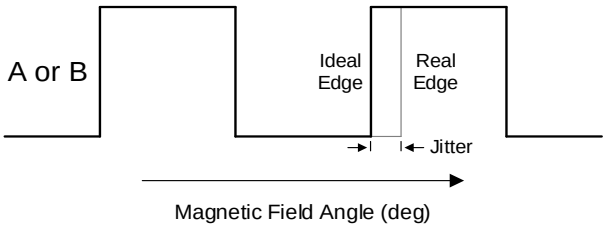

Figure B1: ABZ Jitter

Latency Time elapsed between the instant when the data is ready to be read and the instant at which the shaft passes that position. The lag (in degrees) is *Lag = Latency × v* , where *v* is the angular velocity (in deg/s).

Start-Up Time Time until the sensor delivers valid data, starting at start-up.

Integral Nonlinearity (INL) Maximum deviation between the average sensor output (at a fixed position) and the true mechanical angle (see Figure B2).

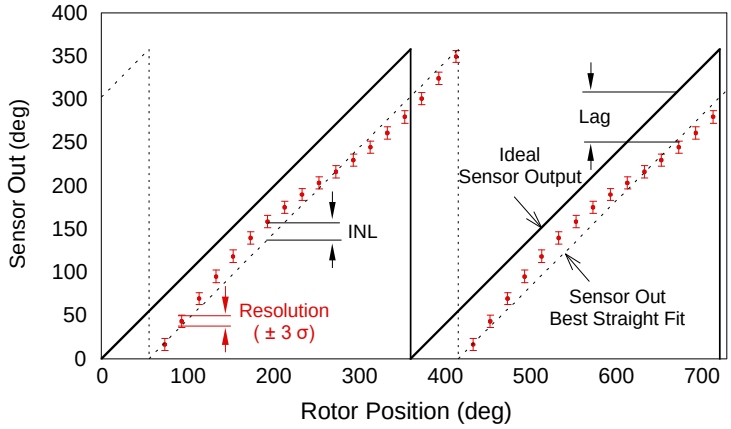

Figure B2: Resolution, INL, Lag

INL can be obtained from the error curve *err(α) = out(α) - α*, where *out(α)* is the average sensor output calculated over many samples (e.g. 1000), and *α* is the mechanical angle indicated by a high-precision (<0.001°) encoder. The INL can be calculated with Equation (B1):

$$INL = \frac{\max(err(\alpha)) - \min(err(\alpha))}{2} \quad (B1)$$

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APPENDIX B: DEFINITIONS *(continued)*

Differential Nonlinearity (DNL)

The DNL is the maximum variation of the error after user calibration ($err_C(\alpha)$) over a full turn. The DNL can be calculated with Equation (B2).

$$DNL = \max_i \left| \frac{err_C(\alpha_i) - err_C(\alpha_{i-1})}{\alpha_i - \alpha_{i-1}} \right| \quad (B2)$$

INL Harmonics

Since the error is a periodical function of period 2π, it can be expressed as a Fourier series. The error can be calculated with Equation (B3).

- *err(α)* is the error curve
- α is the mechanical angle (in radians)
- each n^{th} element of the summation is referred to as the n^{th} harmonic component of the error
- Where H_0 is the offset between the sensor output and the mechanical angle, namely the mean value of err(α) (see Equation (B4))
- Where H_n is the amplitude of the n^{th} harmonic component (see Equation (B5))
- Where φ_n is the phase in radians of the n^{th} harmonic component (see Equation (B6))
- A_n and B_n are the Fourier series coefficients from which H_n and φ_n are obtained (see Equation (B7) and Equation (B8))

$$err(\alpha) = H_0 + \sum_{n=1}^{\infty} H_n \cos(n\alpha - \varphi_n) \quad (B3)$$

$$H_0 = \frac{1}{2\pi} \int_0^{2\pi} err(\alpha)\, d\alpha \quad (B4)$$

$$H_n = \sqrt{A_n^2 + B_n^2} \quad (B5)$$

$$\varphi_n = \tan^{-1}\left(\frac{B_n}{A_n}\right) \quad (B6)$$

$$A_n = \frac{1}{\pi} \int_0^{2\pi} err(\alpha)\cos(n\alpha)\, d\alpha \quad (B7)$$

$$B_n = \frac{1}{\pi} \int_0^{2\pi} err(\alpha)\sin(n\alpha)\, d\alpha \quad (B8)$$

Drift

Angle variation rate when one parameter is changed (e.g. temperature or V_{DD}) and all the others, including the shaft angle, are kept constant.

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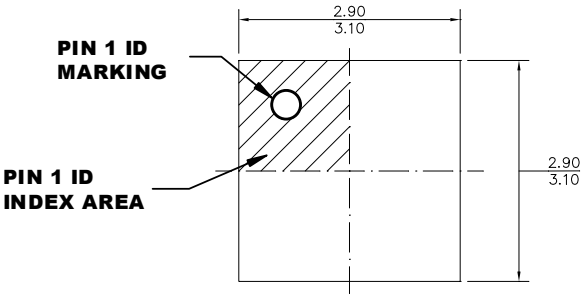
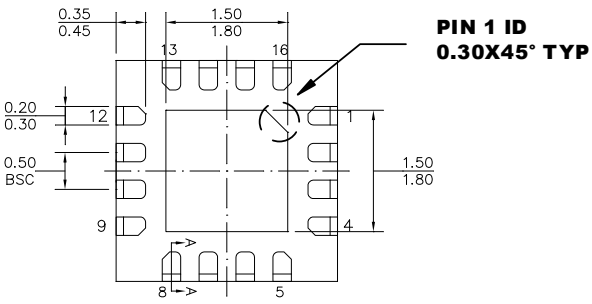
PACKAGE INFORMATION

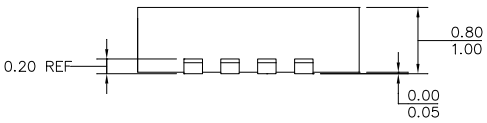
QFN-16 (3mmx3mm)
Wettable Flank



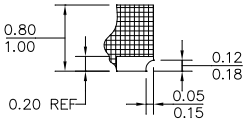
TOP VIEW



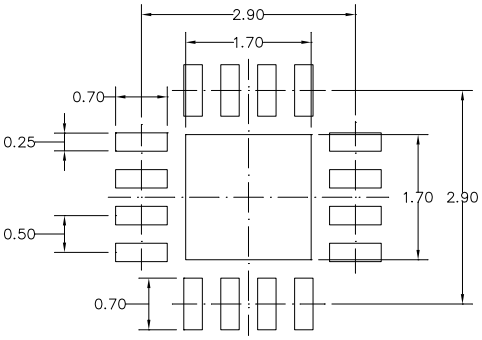
BOTTOM VIEW



SIDE VIEW



SECTION A-A



RECOMMENDED LAND PATTERN

NOTE:

1) THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
4) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
5) JEDEC REFERENCE IS MO-220.
6) DRAWING IS NOT TO SCALE.

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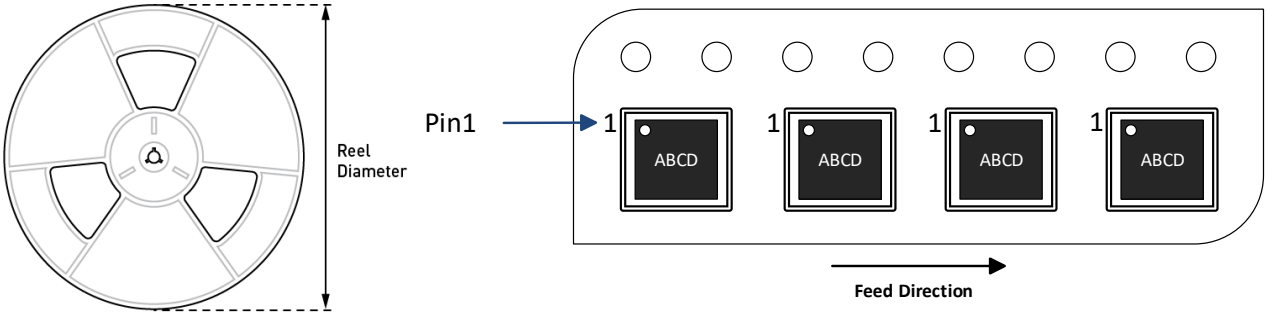
CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MA600AGQE-xxxx-Z	QFN-16 (3mmx3mm)	5000	N/A	N/A	13in	12mm	8mm

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REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	6/5/2025	Initial Release	-

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