HFG611-45

High-Frequency Quasi-Resonant Flyback Regulator with Integrated 300mΩ GaN FET

DESCRIPTION

The HFG611-45 is a quasi-resonant (QR) flyback regulator with an integrated GaN FET, which is suitable for the high-performance and high-frequency designs.

The HFG611-45 is a secondary-side regulation (SSR) based primary regulator, and must work with secondary-side feedback circuitry. The higher frequency shrinks the passive component size and achieves higher power density. The HFG611-45 integrates a high-voltage start-up circuit and an X-capacitor discharger circuit, in addition to an ultra-low quiescent current (I_Q) during burst mode. The no-load power consumption can be below 30mW.

The HFG611-45 adopts MPS's patented valley lock technique to restrain the valley jumping from one to another during steady state operation and help avoid audible noise. The wide supply voltage (V_{CC}) range makes the device suitable for applications with a wide output voltage (V_{OUT}) range without adding auxiliary winding.

Advanced protections include primary-sense output over-voltage protection (ZCD OVP), primary-sense output under-voltage protection (ZCD UVP), V_{CC} over-voltage protection (V_{CC} OVP), output overload protection (OLP), internal brown-in and brownout (BI and BO, respectively), short-circuit protection (SCP), internal thermal shutdown (OTP), and under-voltage lockout (UVLO).

The HFG611-45 is available in QFN-21 (5mmx6mm) and QFN-25 (7mmx7mm) packages.

	Recommended Output Power (3) (W)			
	90V_{AC} to 265V_{AC}		**230V_{AC} ±15%**	
	Adapter (1)	**Open Frame** (2)	**Adapter**	**Open Frame**
QFN-21 (5mmx6mm) Version	45	50	50	55
QFN-25 (7mmx7mm) Version	50	55	55	60

FEATURES

- Integrated 700V/300mΩ GaN FET
- Novel Patented Quasi-Resonant (QR) Control to Eliminate Audible Noise
- Ultra-Wide Supply Voltage (V_{CC}) Range to Support USB Power Delivery (PD) Applications
- Built-in X-Capacitor Discharger
- Built-In High-Voltage Start-Up Circuit
- Ultra-Low Standby Power Consumption with PD Protocol IC (<30mW)
- Peak Current Mode Control and Leading-Edge Blanking (LEB)
- Under-Voltage Lockout (UVLO), V_{CC} Over-Voltage Protection (OVP), ZCD OVP, ZCD Under-Voltage Protection (UVP), Overload Protection (OLP), Internal Brown-In (BI) and Brownout (BO), Short-Circuit Protection (SCP), and Over-Temperature Protection (OTP)
- Available in QFN-21 (5mmx6mm) and QFN-25 (7mmx7mm) Packages

APPLICATIONS

- Cellphone Chargers
- Standby Power

Notes:

1) Maximum continuous power in a non-ventilated enclosed adapter measured at 40°C ambient temperature (T_A).
2) Maximum continuous power in an open frame design at T_A = 40°C.
3) The junction temperature (T_J) can limit the maximum P_{OUT}.

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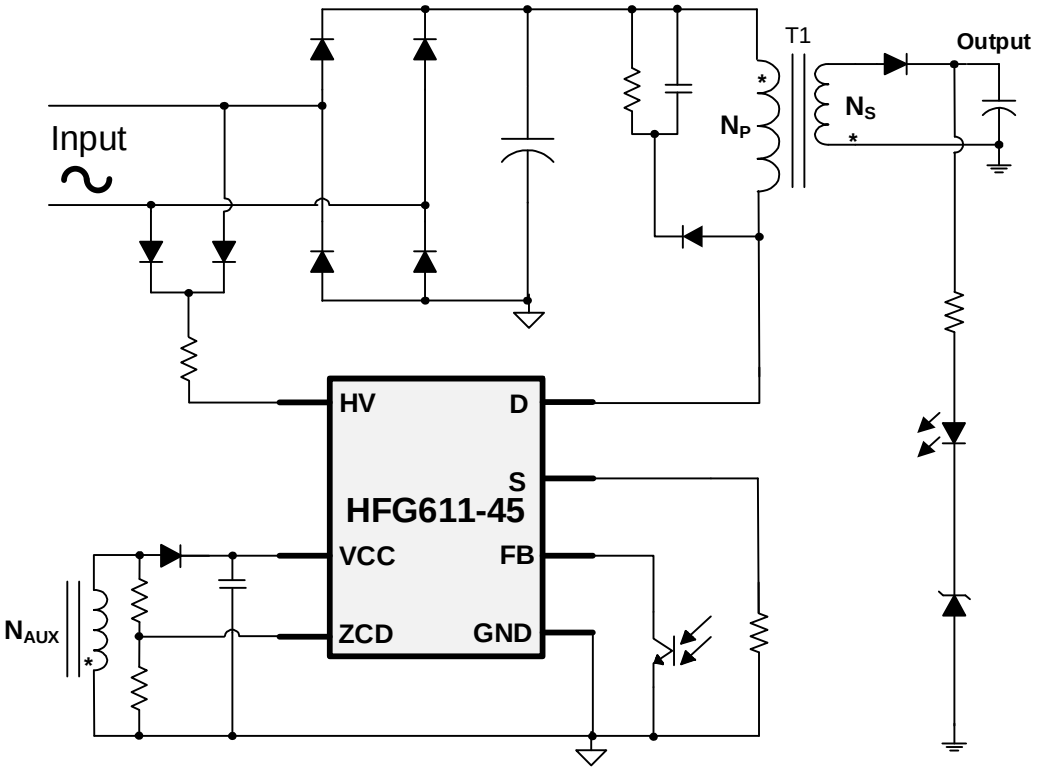
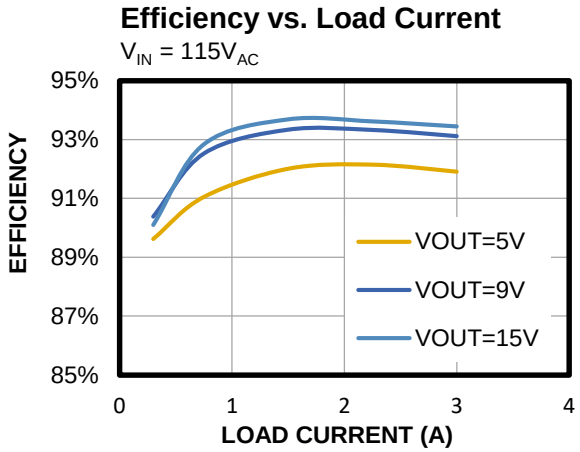
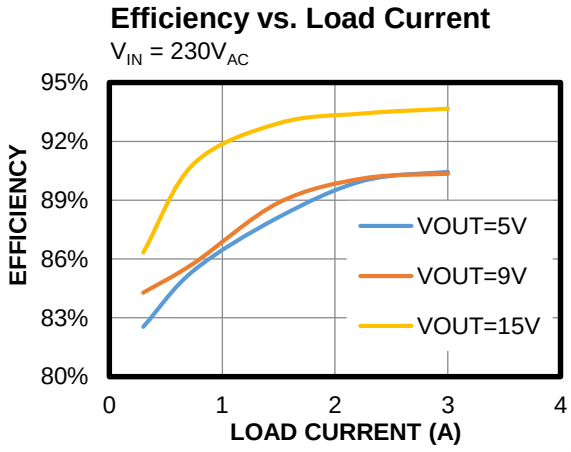
TYPICAL APPLICATION







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ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
HFG611GQJ-45	QFN-21 (5mmx6mm)	*See Below*	2
HFG611GQN-45	QFN-25 (7mmx7mm)	*See Below*	3

* For Tape & Reel, add suffix -Z (e.g. HFG611GQJ-45-Z).

* For Tape & Reel, add suffix -Z (e.g. HFG611GQN-45-Z).

TOP MARKING (HFG611GQJ-45)

MPSYYWW
HFG611
LLLLLLL
45

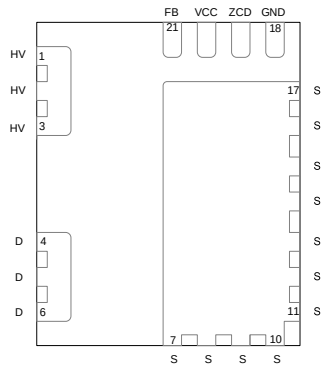
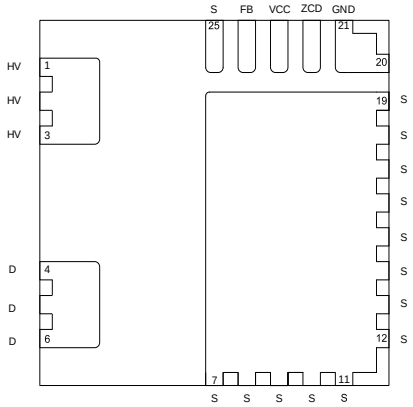
MPS: MPS prefix
YY: Year code
WW: week code
HFG611-45: Part number
LLLLLLL: Lot number

TOP MARKING (HFG611GQN-45)

MPS YYWW
HFG611-45
LLLLLLLLL

MPS: MPS prefix
YY: Year code
WW: week code
HFG611-45: Part number
LLLLLLLLL: Lot number

PACKAGE REFERENCE

TOP VIEW	TOP VIEW
	
QFN-21 (5mmx6mm)	**QFN-25 (7mmx7mm)**

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PIN FUNCTIONS

Pin #		Name	Description
QFN-21	QFN-25		
1, 2, 3	1, 2, 3	HV	**Input for the start-up high-voltage current source.** The HV pin also provides line voltage sensing, brown-in and brownout, line remove detection circuit, and X-capacitor discharge functions.
4, 5, 6	4, 5, 6	D	**GaN FET drain.**
7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17	7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 25	S	**GaN FET source.** This pin also serves as current-sense (CS) node. A current-sense resistor is connected between this pin and GND to sense the primary current for current-mode operation.
18	20, 21	GND	**Ground.**
19	22	ZCD	**Integrated over-voltage protection (OVP) and under-voltage protection (UVP).** A resistor divider placed between the auxiliary winding and the ZCD pin provides input to the demagnetization detection comparator and output voltage (V_{OUT}) information to achieve protection.
20	23	VCC	**IC power supply.**
21	24	FB	**Feedback.** A pull-down optocoupler controls the output regulation.

ABSOLUTE MAXIMUM RATINGS (4)

HV to GND ..... -0.3V to +650V
D to GND (8) ..... -0.3V to +700V
D to GND, pulse (9) ..... -0.3V to +750V
D to GND, transient (10) ..... -0.3V to +800V
Pulsed DS current (11) 8.5A
Continuous DS current (12) 2.8A
VCC to GND .....-0.3V to +57V
ZCD to GND .....-0.7V to +15V
FB GND .....-0.3V to +6.5V
S to GND, gate on .....-0.3V to +6.5V
S to GND, gate off (8).....-0.3V to +1.4V
Continuous power dissipation (T_A = 25°C) (8)
QFN-21 (5mmx6mm) 4.2W
QFN-25 (7mmx7mm) 5.3W
Junction temperature (T_J) .....150°C
Lead temperature .....260°C
Storage temperature ..... -60°C to +150°C

Recommended Operating Conditions (6)

Supply voltage (V_{CC}) .....9V to 49V
Operating junction temp (T_J).... -40°C to +125°C

Thermal Resistance (7) θ_{JA} θ_{JC}

QFN-21 (5mmx6mm)……..29.2.....5.4…°C/W
QFN-25 (7mmx7mm)……..23.5.....2…..°C/W

Notes:

4) The device is not guaranteed to function outside of its operating conditions.
5) Exceeding these ratings may damage the device.
6) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
7) Measured on a JESD51-7, 4-layer.
8) Guaranteed by characterization.
9) Repetitive pulse, t_{PULSE} < 100ns. T_J = 25°C, total time < 10h. T_J = 125°C, total time < 1h. Guaranteed by characterization.
10) Non-repetitive pulse, t_{PULSE} < 200µs. Guaranteed by characterization.
11) T_J = 25°C, t_{PULSE} = 10µs. Guaranteed by characterization.
12) T_J = 125°C. Guaranteed by characterization.

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ELECTRICAL CHARACTERISTICS

T_J = -40°C to +125°C, typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Breakdown voltage	V_{HV_BD}	T_J = 25°C	700			V
HV leakage current	I_{HV_LK}	V_{HV} = 500V			15	µA
HV supply current	I_{HV_SP}	V_{CC} = 12V, V_{HV} = 80V	4.5			mA
		V_{CC} = V_{CC_IOFF} - 0.1V, V_{HV} = 80V	2.7			
	$I_{HV_SP_SC}$	V_{CC} = 0V, V_{HV} = 80V		1		
Drain (D Pin)						
Drain breakdown voltage	V_{D_BD}	I_{DSS} < 15µA, T_J = 25°C	700			V
Drain-to-source leakage current	I_{DSS}	V_{DS} = 400V, V_{GS} = 0V, T_J = 25°C		0.8	12	µA
Drain-to-source on resistance	$R_{DS(ON)}$	V_{GS} = 5.5V, T_J = 25°C, I_{DS} = 0.1A		300	380	mΩ
		V_{GS} = 5.5V, T_J = 125°C, I_{DS} = 0.1A		560		mΩ
Brownout (BO) Detection and X-Capacitor Discharger (HV Pin)						
Brown-in (BI) threshold voltage	V_{HV_ON}		92	105	120	V
BO threshold voltage	V_{HV_OFF}		82	95	110	V
BI and BO hysteresis	V_{HV_HYS}			10		V
BO detection blanking time	t_{BO}			62		ms
Discharge time duration	t_{LINE_DIS}			144		ms
Discharge current	I_{DIS_HV}		4.2			mA
HV high-line voltage threshold	V_{HV_HL}		210	240	270	V
HV high-line voltage detection hysteresis	$V_{HV_HL_HYS}$			10		V
Supply Voltage Management (VCC Pin)						
I_{HV_SP} turn-off voltage	V_{CC_IOFF}	V_{CC} increasing	16.5	17.5	19	V
Minimum operation voltage	V_{CC_MIN}	V_{CC} decreasing	7.4	8.0	8.6	V
Operation voltage hysteresis	V_{CC_HYS}		8			V
V_{CC} release level after auto-recovery protection	V_{CC_PRO}	V_{CC} decreasing	5.5	6.3	7	V
VCC release level after latch-off protection	V_{CC_LATCH}	V_{CC} decreasing		2.9		V
Transition from $I_{HV_SP_SC}$ to I_{HV_SP}	V_{CC_LC}	V_{CC} increasing		0.8		V
Over-voltage protection (OVP) level	V_{CC_OVP}		50	53	57	V
Operating current	I_{OP}	V_{CC} = 15V		2	3	mA
Quiescent current	I_Q	V_{CC} = 15V, V_{FB} = 0V			470	µA
Current Sense (S Pin)						
Current-sense voltage	V_{CS_MAX}		0.388	0.4	0.408	V
	V_{CS_MIN}			0.15		V
Maximum soft-start duration	t_{SOFT}			6.2		ms

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ELECTRICAL CHARACTERISTICS *(continued)*

T_J = -40°C to +125°C, Typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Jittering amplitude	ΔV_{CS}	V_{CS} = 0.4V	±4%	±5%	±6%	V_{CS}
Jittering period	t_{JITTER}			32		cycles
Leading-edge blanking (LEB) for current limitation	t_{LEB_L}			200		ns
LEB for short-circuit protection (SCP)	t_{LEB_S}			150		ns
SCP threshold	V_{SCP}		0.6	0.65	0.7	V
Second SCP blanking time	t_{SCP}			130		µs
Maximum on time	t_{ON_MAX}			14.5		µs
Feedback (FB Pin)						
Maximum FB voltage (V_{FB})	V_{FB_MAX}		3.6	3.7	3.9	V
Delta V_{FB_MAX} - V_{OLP}	$V_{FB_MAX_VOLP}$			0.3		V
Time duration before overload protection (OLP) (13)	t_{OLP}			50		ms
Internal pull-up resistor	R_{FB}			18		kΩ
V_{FB} high threshold to fix current limit	$V_{FB_CS_MAX}$			3.2		V
V_{FB} low threshold to fix current limit	$V_{FB_CS_MIN}$			1.54		V
Burst mode entrance	V_{BUR_IN}	V_{FB} decreasing		0.7		V
Burst mode exit	V_{BUR_OUT}	V_{FB} increasing		0.8		V
Burst exit hysteresis	V_{BUR_HYS}			0.1		V
Demagnetization Detection for QR (ZCD Pin)						
ZCD threshold voltage	V_{ZCD_TH}	V_{ZCD} decreasing	36	62	88	mV
ZCD hysteresis voltage	V_{ZCD_HYS}	V_{ZCD} increasing		30		mV
ZCD sample blanking time after turn-off	t_{ZCD_BLANK1}	V_{CS} = 0.4V		820		ns
	t_{ZCD_BLANK2}	V_{CS} = 0.15V		510		ns
Timeout after last demagnetization detection (watchdog)	t_{OUT}		2	2.7	3.6	µs
ZCD OVP threshold	V_{ZCD_OVP}		11.7	12.2	12.6	V
ZCD OVP blanking time	t_{ZCD_OVP}			3		cycles
ZCD under-voltage protection (UVP)	V_{ZCD_UVP}	After soft start	0.29	0.4	0.48	V
ZCD UVP blanking time (13)	t_{ZCD_UVP}	After soft start		250		µs
ZCD pin negative clamp voltage	V_{ZCD_MIN}	I_{ZCD} = -2mA	-0.4	-0.13	0	V
Internal Over-Temperature Protection (OTP)						
OTP threshold (13)	T_{OTP}			150		°C
Hysteresis to release OTP (13)	ΔT_{OTP}			40		°C

Note:

13) Guaranteed by design.

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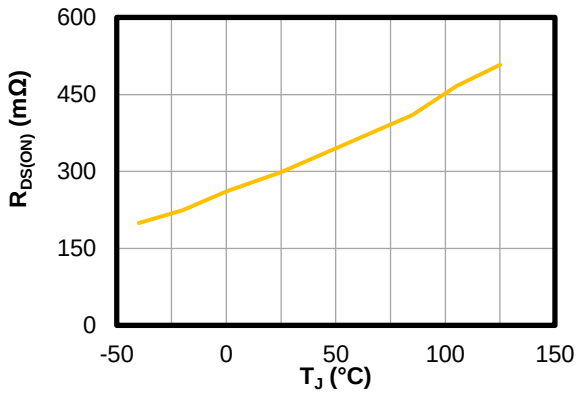
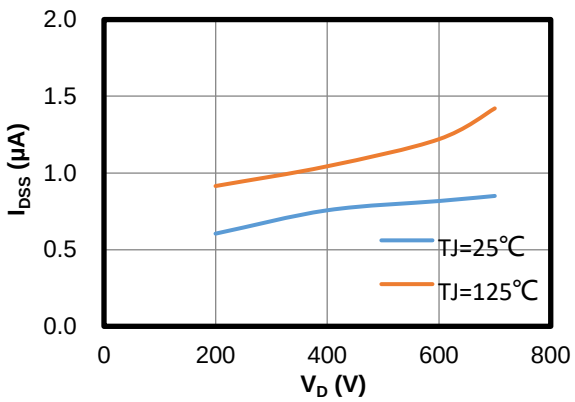
TYPICAL CHARACTERISTICS

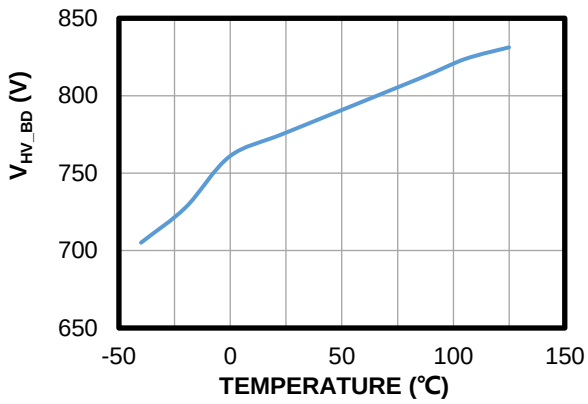
$R_{DS(ON)}$ vs. T_J



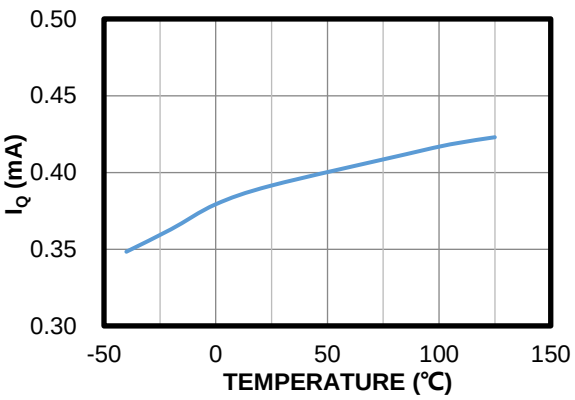
I_{DSS} vs. V_D



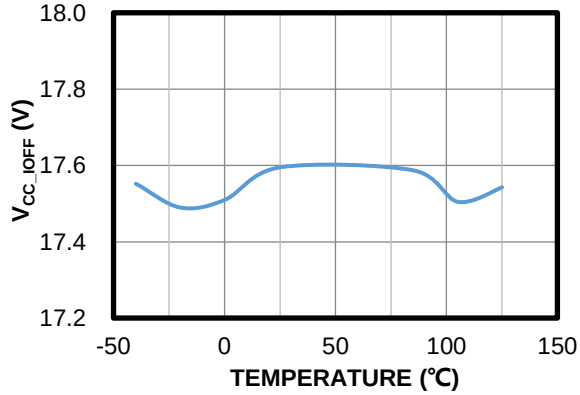
V_{HV_BD} vs. Temperature



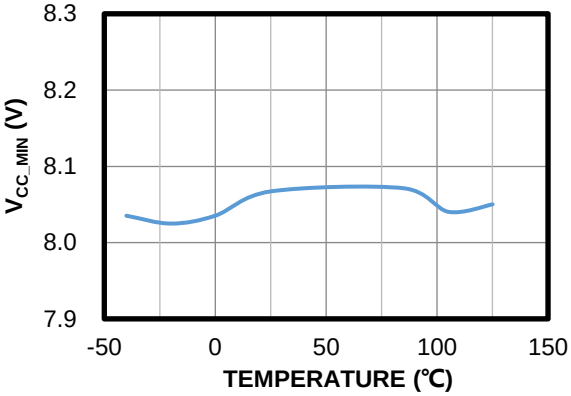
I_Q vs. Temperature



V_{CC_IOFF} vs. Temperature



V_{CC_MIN} vs. Temperature



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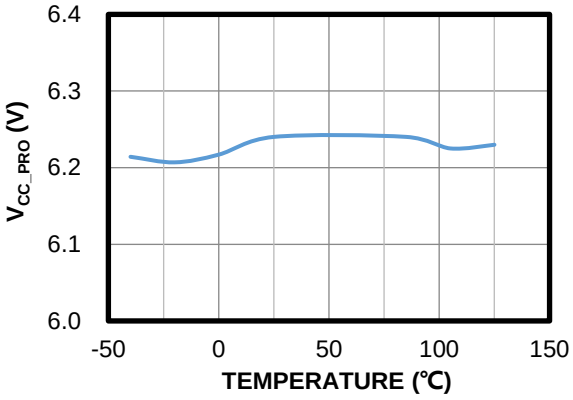
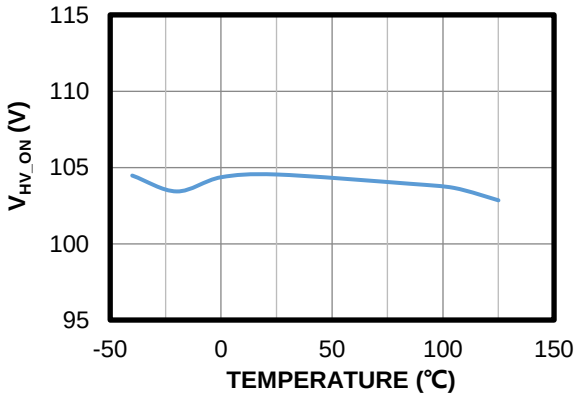
TYPICAL CHARACTERISTICS *(continued)*

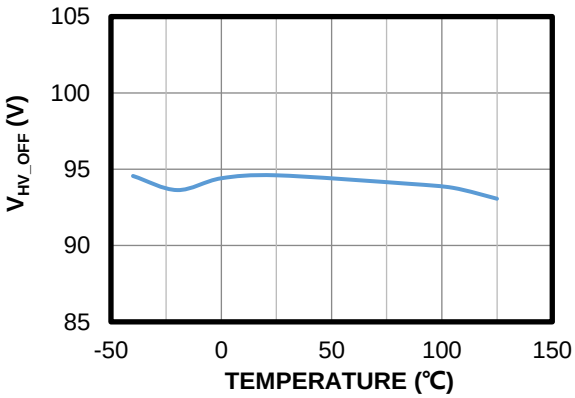
V_{CC_PRO} vs. Temperature



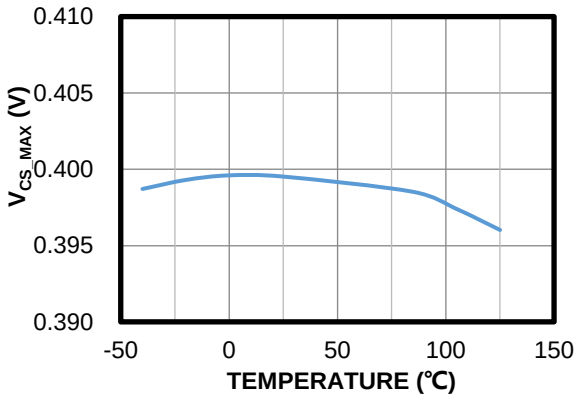
V_{HV_ON} vs. Temperature



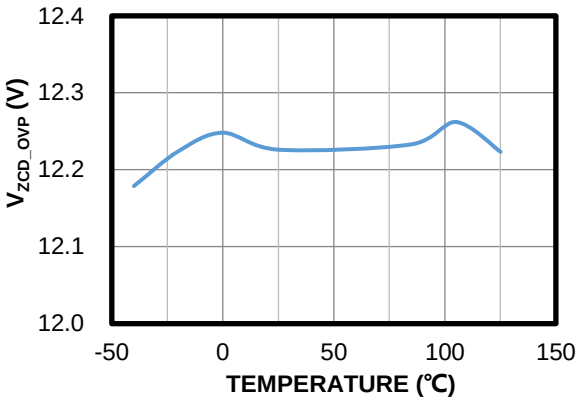
V_{HV_OFF} vs. Temperature



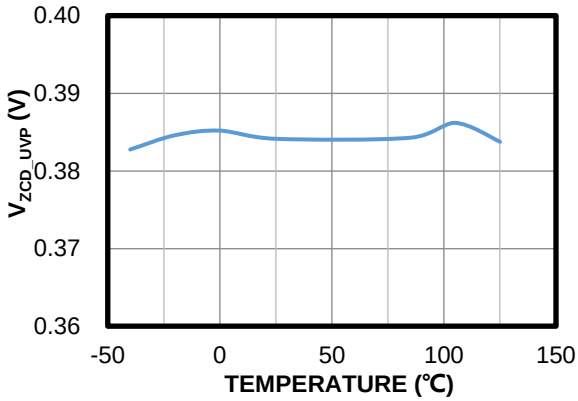
V_{CS_MAX} vs. Temperature



V_{ZCD_OVP} vs. Temperature



V_{ZCD_UVP} vs. Temperature



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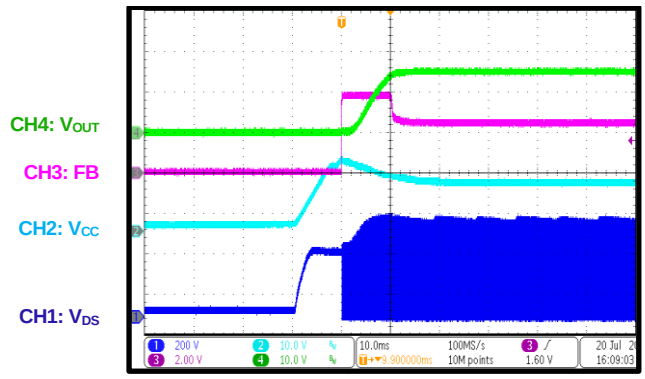
TYPICAL PERFORMANCE CHARACTERISTICS.

V_{IN} = 90V_{AC} to 265V_{AC}, V_{OUT} = 5V, 9V, or 15V, I_{OUT} = 0A to 3A, unless otherwise noted.

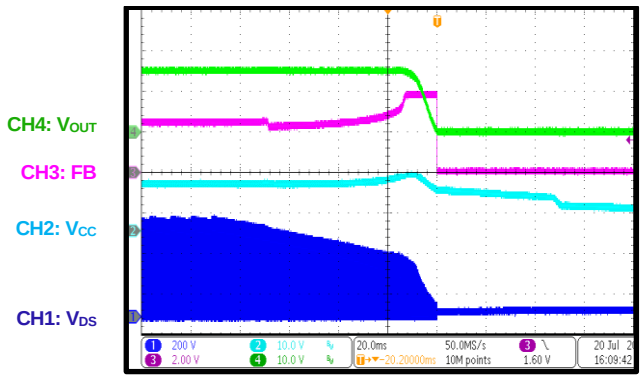
Start-Up

V_{IN} = 230V_{AC}, V_{OUT} = 15V, I_{OUT} = 3A



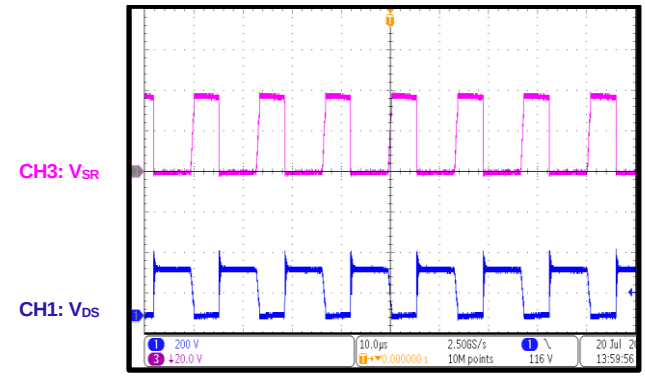
Shutdown

V_{IN} = 230V_{AC}, V_{OUT} = 15V, I_{OUT} = 3A



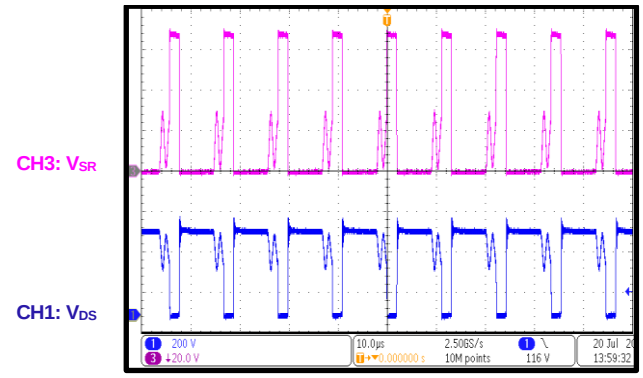
Steady State

V_{IN} = 115V_{AC}, V_{OUT} = 15V, I_{OUT} = 3A



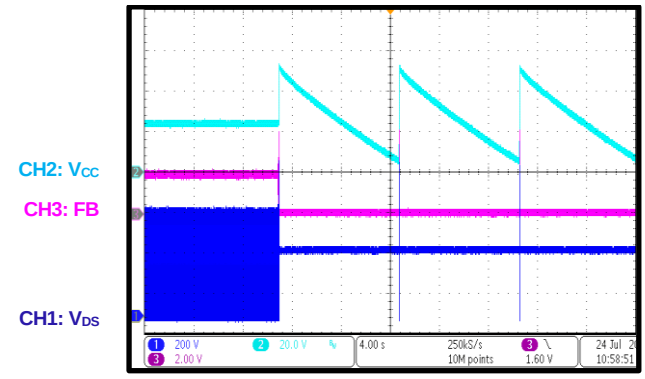
Steady State

V_{IN} = 230V_{AC}, V_{OUT} = 15V, I_{OUT} = 3A



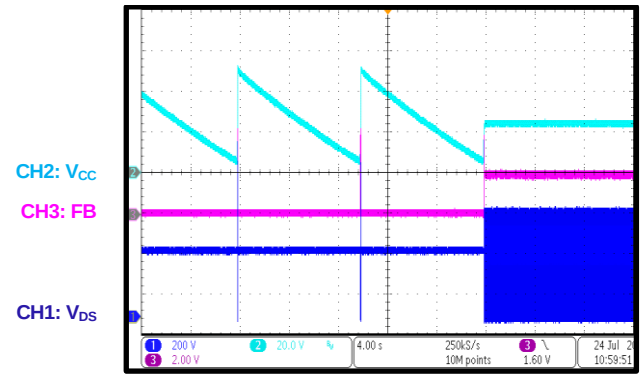
OVP

V_{IN} = 230V_{AC}, V_{OUT} = 15V



OVP Recovery

V_{IN} = 230V_{AC}, V_{OUT} = 15V



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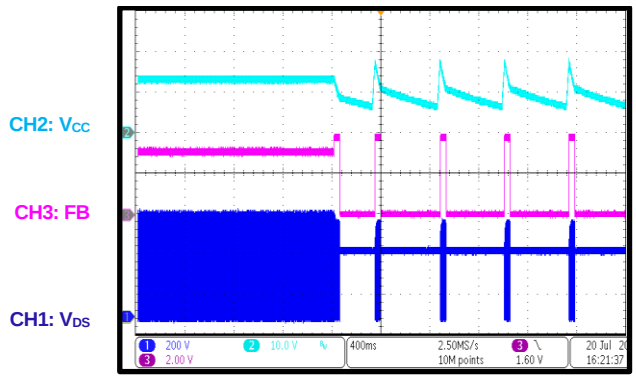
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 90V_{AC} to 265V_{AC}, V_{OUT} = 5V, 9V, or 15V, I_{OUT} = 0A to 3A, unless otherwise noted.

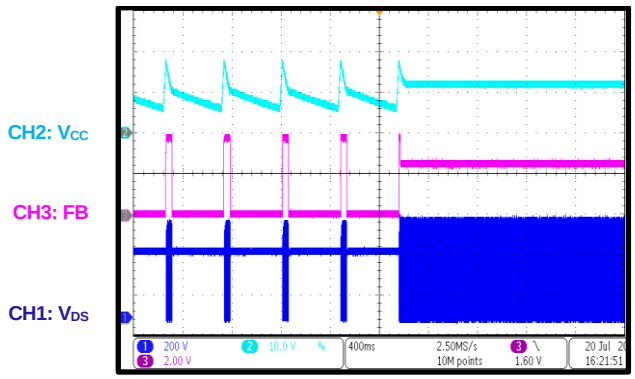
OLP

V_{IN} = 230V_{AC}



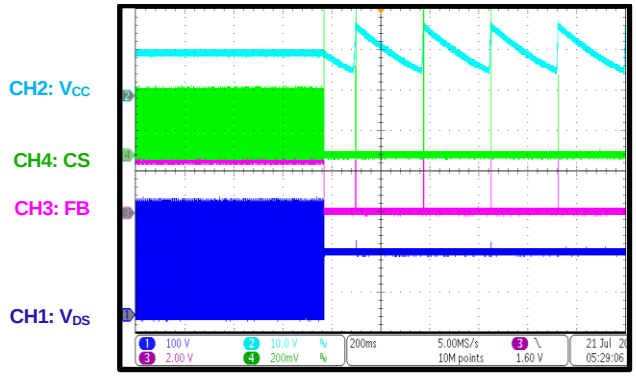
OLP Recovery

V_{IN} = 230V_{AC}



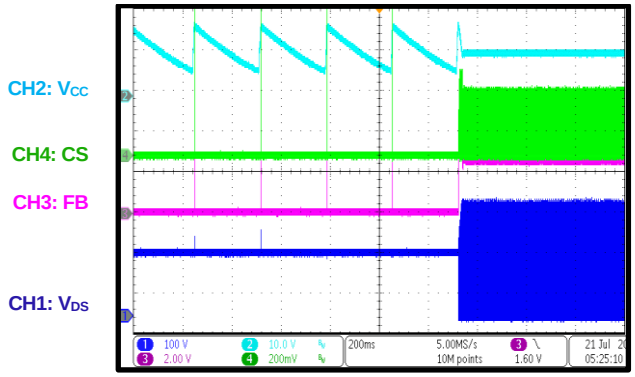
SCP

V_{IN} = 115V_{AC}



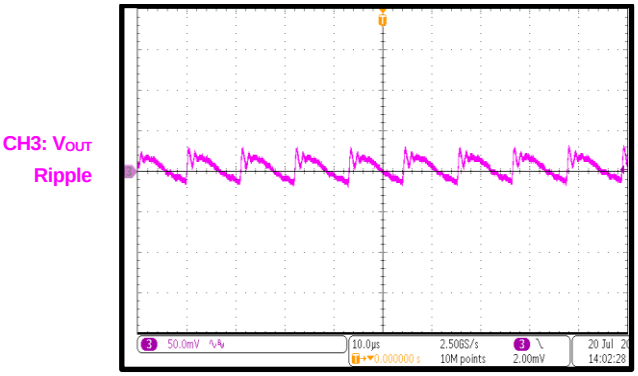
SCP Recovery

V_{IN} = 115V_{AC}



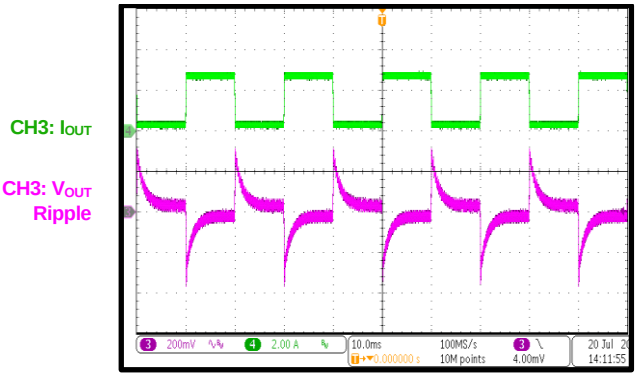
Output Voltage Ripple

V_{IN} = 230V_{AC}, V_{OUT} = 15V, I_{OUT} = 3A



Output Voltage Transient Response

V_{IN} = 230V_{AC}, V_{OUT} = 15V



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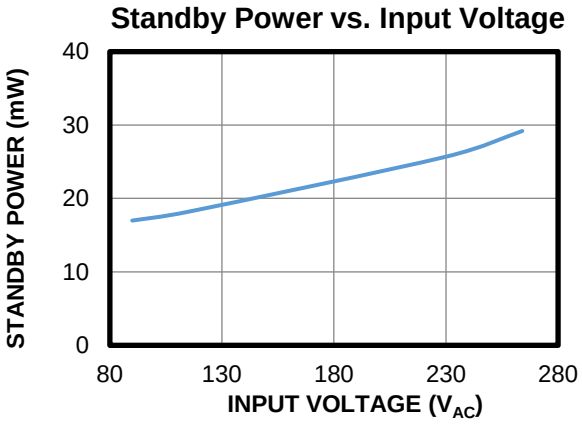
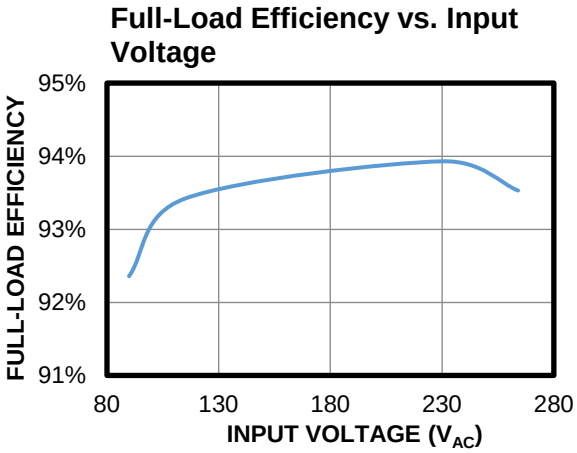
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 90V_{AC} to 265V_{AC}, V_{OUT} = 5V, 9V, or 15V, I_{OUT} = 0A to 3A.





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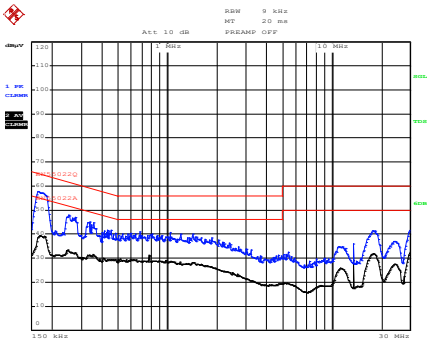
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 115V_{AC}/230V_{AC}, V_{OUT} = 5V, 9V, or 15V, I_{OUT} = 0A to 3A, unless otherwise noted.

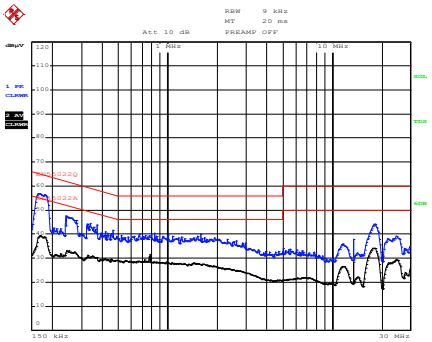
EMI

V_{IN} = 115V_{AC}, L line, V_{OUT} = 15V, I_{OUT} = 3A



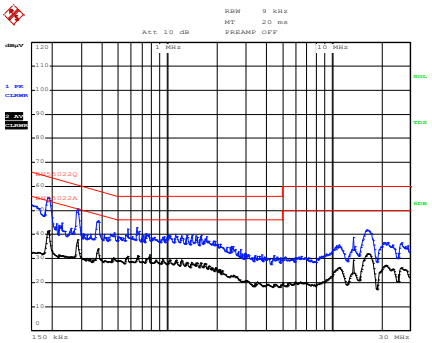
EMI

V_{IN} = 115V_{AC}, N line, V_{OUT} = 15V, I_{OUT} = 3A



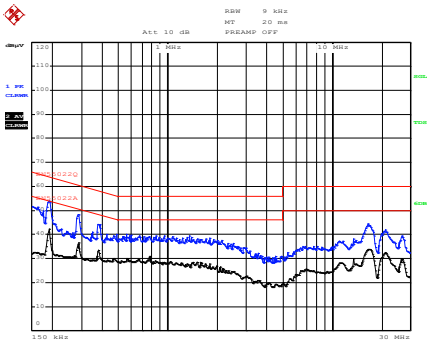
EMI

V_{IN} = 230V_{AC}, L line, V_{OUT} = 15V, I_{OUT} = 3A



EMI

V_{IN} = 230V_{AC}, N line, V_{OUT} = 15V, I_{OUT} = 3A



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FUNCTIONAL BLOCK DIAGRAM

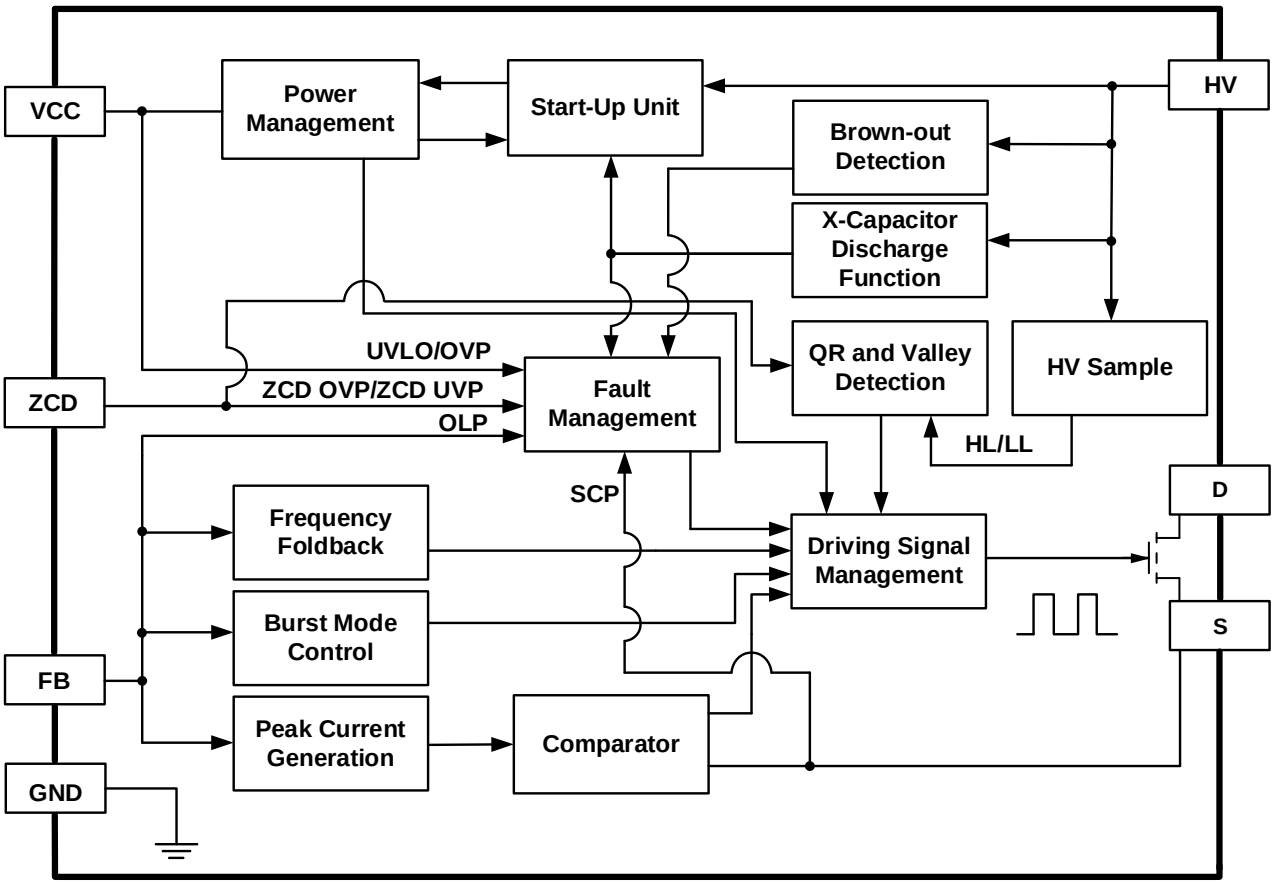

Figure 1: Functional Block Diagram

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OPERATION

The HFG611-45 is a high-frequency, quasi-resonant (QR) flyback regulator with an integrated GaN FET based on peak current mode control. The device runs QR mode under heavy loads, and the valley transfers back and forth smoothly by decreasing the load. Under light loads, the HFG611-45 operates in frequency foldback mode and enters burst mode when the load is extremely light.

For conventional QR control, the switching frequency (f_{SW}) is inverse and proportional to the system load, which leads to a higher f_{SW} during lighter loads and severely deteriorates the light-load efficiency. To improve light-load performance and limit the maximum f_{SW}, the HFG611-45 operates in discontinuous conduction mode (DCM) with frequency foldback, while the minimum f_{SW} is about 30kHz.

The HFG611-45 implements a patented, valley-locked circuit with proper hysteresis to prevent jumping back and forth between two adjacent valleys. Based on the proposed control scheme, the operation always remains in the selected valley until there is a significant change in the output power (P_{OUT}).

Internal High-Voltage Start-Up Circuit with Brown-In and Brownout Detection (HV)

Initially, the IC is self-supplied by the internal high-voltage current source via the HV pin. The charge current is divided into two segments. If the VCC voltage (V_{CC}) is below the transition voltage between the HV supply currents (V_{CC_LC}), then the charging current is limited to the HV supply current ($I_{HV_SP_SC}$, typically 1mA) to protect the IC from breaking under certain fault conditions, such as if V_{CC} is shorted to GND. When V_{CC} exceeds V_{CC_LC}, the charging current increases to its normal level (I_{HV_SP}, minimum 4.5mA) to ensure that V_{CC} charges up as quickly as possible.

When V_{CC} reaches the turn-off voltage (V_{CC_IOFF}, typically 17.5V), the IC turns off the current source and begins detecting the voltage on the HV pin. Once the HV voltage (V_{HV}) exceeds the brown-in voltage threshold (V_{HV_ON}, typically 105V), V_{CC} charges up again via the HV current source. When V_{CC} reaches V_{CC_IOFF} again, the IC begins switching.

Recharging before V_{CC} drops to the minimum operating voltage (V_{CC_MIN}, typically 8V) guarantees the maximum start-up period. When the output voltage (V_{OUT}) reaches a high enough level, the transformer auxiliary winding takes over the IC supply. If V_{CC} falls back to V_{CC_MIN}, the switching stops and the HV current source turns on again. Figure 2 shows the typical waveforms for the HV charge and V_{CC} under-voltage lockout (UVLO).

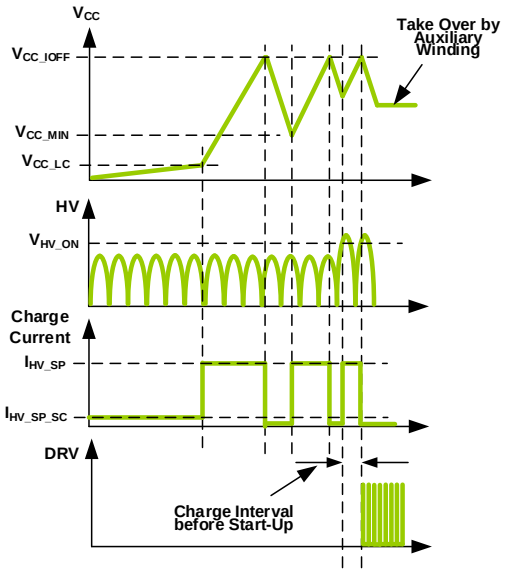

Figure 2: Start-Up with Brown-In and Brownout Detection

Soft Start (SS)

To reduce the stress on power components and smoothly establish V_{OUT}, the HFG611-45 employs soft start (SS). Figure 3 shows the peak current limit gradually increasing from V_{CS_MIN} to the maximum current-sense voltage (V_{CS_MAX}) during start-up, unless the feedback takes over.

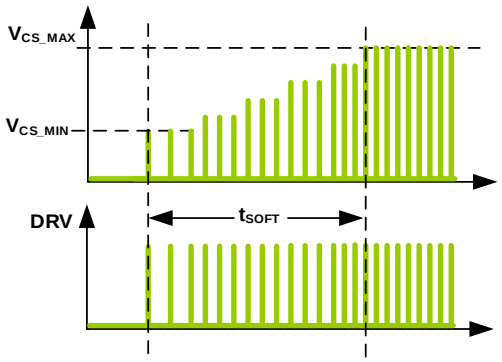

Figure 3: Soft Start

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Frequency Modulation and Peak Current Mode Control

When the load becomes lighter for conventional QR control, f_{SW} rises and decreases light-load efficiency. The HFG611-45 adopts a novel form of QR control, in which the pulse-frequency modulation (PFM) signal is generated to control f_{SW} and the valley detection signal. This novel QR control method achieves frequency foldback to boost efficiency and prevent an undesirable, high f_{SW} at light loads.

Figure 4 shows the f_{SW} vs. feedback voltage (V_{FB}) curve with the patented QR control.

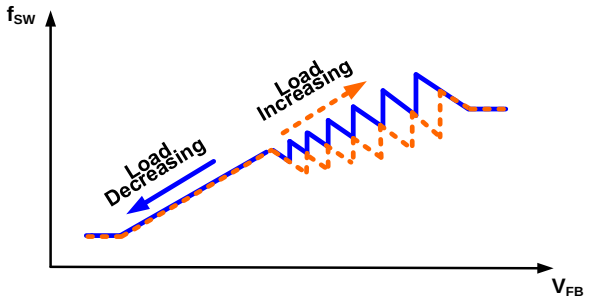

Figure 4: f_{SW} vs. V_{FB}

The HFG611-45 adopts peak current mode for on-time control via the S pin. The CS reference voltage (V_{REF}) is also regulated by V_{FB}, along with a maximum amplitude of V_{CS_MAX} and a minimum of V_{CS_MIN}. Figure 5 shows the V_{REF} amplitude decreasing as the frequency decreases.

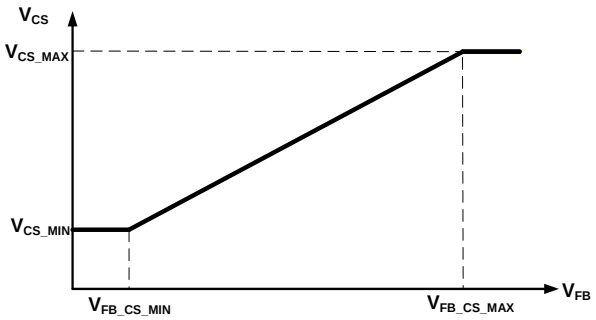

Figure 5: Current Limit Modulation vs. FB

Valley-Lock Quasi-Resonant (QR) Control

Unlike conventional QR control, the turn-on valley jumps between adjacent valleys many times in one line cycle.

The HFG611-45 locks the turn-on valley under certain load conditions, which can prevent audible noise caused by the valley jumping.

The valley signal generates a time window by detecting the zero-current detection (ZCD) voltage (V_{ZCD}) and comparing it with the V_{ZCD} internal threshold (V_{ZCD_TH}). When V_{ZCD} is below V_{ZCD_TH}, the main switch's drain-to-source voltage has reached its valley. Figure 6 shows the valley signal generation.

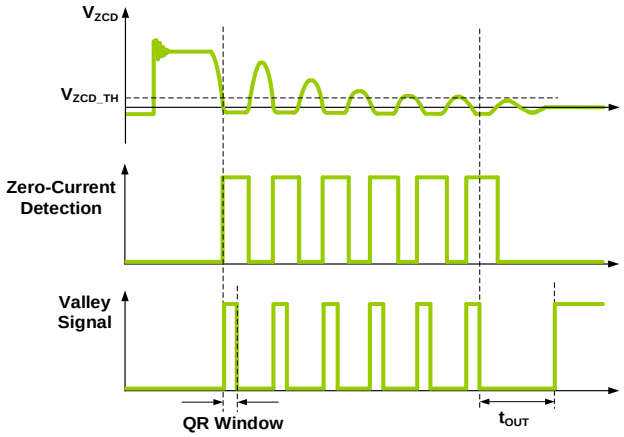

Figure 6: QR Signal Generation

The HFG611-45 monitors the PFM signal by recording the previous turn-on valley and inserting a hysteresis surrounding the PFM signal. If the PFM signal goes high within the hysteresis, the device keeps turning on the driver at the same valley. If the PFM signal goes high ahead of the hysteresis, the device turns on the driver at the next valley following the PFM signal. If the PFM signal goes high after the hysteresis, the turn-on valley moves backwards. The turn-on valley can be locked using this method.

Forced Burst Mode

Since both the peak current and a minimum frequency are limited, burst mode is required to keep the power continuously down to 0W. The HFG611-45 stops switching and enters burst mode when V_{FB} drops below the burst mode entry threshold (V_{BUR_IN}, typically 0.7V), and resumes switching once V_{FB} exceeds the burst mode exit threshold (V_{BUR_OUT}, typically 0.8V). Figure 7 on page 16 shows forced burst mode.

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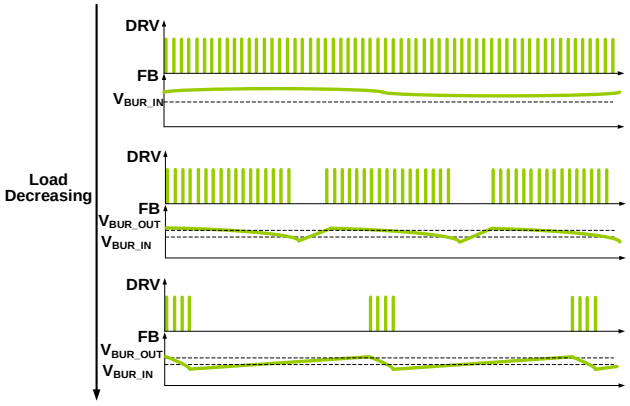

Figure 7: Forced Burst Mode

X-Capacitor Discharger

X-capacitors are typically positioned across a power supply's input terminals to filter differential mode EMI noise. When operating alone, these components can present a safety hazard because they can store unsafe levels of high-voltage energy for long periods of time after the AC supply is disconnected. To be compliant with safety standards, use resistors in parallel with the X-capacitor across the AC supply line to provide a discharge path.

However, these discharge resistors produce a constant power loss while the AC is connected, and contribute significantly to no-load and standby input power consumption.

When the AC voltage is applied, the internal high-voltage current source turns off to block the HV current, and the HFG611-45 monitors V_{HV}. If it detects that no AC voltage is supplied, then the HFG611-45 starts discharging for the discharge time (t_{LINE_DIS}, typically 144ms) with the discharge current (I_{DIS_HV}, minimum 4.2mA). Then the HFG611-45 resumes normal operation.

After the first discharge, the HFG611-45 turns off the discharge current source and detects whether the input is re-plugged to the AC line. If the AC input remains disconnected, the HFG611-45 resumes discharging for t_{LINE_DIS} again, then turns off for a duration before continuing this detection cycle. This process continues until V_{HV} is below V_{CC}.

Figure 8 shows the X-capacitor discharge behavior. This approach provides an intelligent discharge path for the X-capacitor, eliminating the power loss from external discharge resistors.

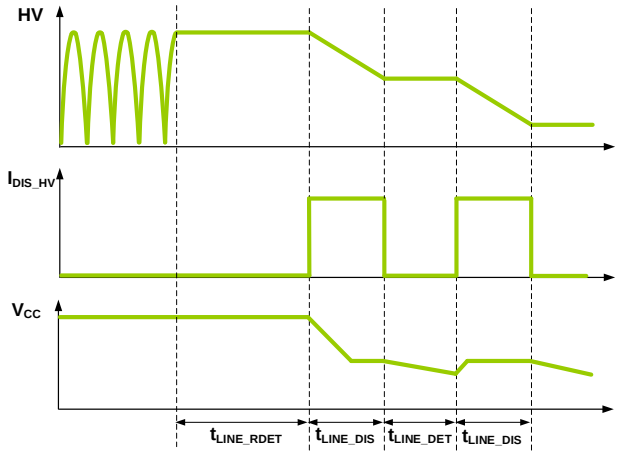

Figure 8: X-Capacitor Discharger

Frequency Jittering

Frequency jittering reduces EMI by spreading energy across the jitter frequency range. A low-frequency ramp is added onto the peak current reference. The jittering amplitude stays proportional to the peak current as it regulates during the t_{JITTER} period (typically 32 switching cycles) (see Figure 9).

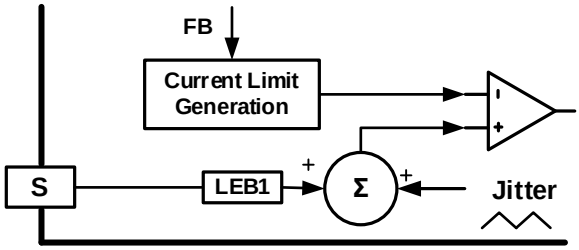

Figure 9: Frequency Jittering

The jitter is removed once the IC enters the burst mode.

Leading-Edge Blanking (LEB)

To prevent the parasitic capacitance from prematurely terminating the switching pulse, an internal leading-edge blanking (LEB) unit is employed between the S pin and the current comparator input. During the blanking time, the current comparator is disabled and cannot turn off the GaN FET. There are two LEB times: the LEB time for a normal current limit (t_{LEB_L}, typically 200ns) and the LEB time for the current limit during fault conditions (t_{LEB_S}, typically 150ns).

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Under-Voltage Lockout (UVLO)

If V_{CC} falls below V_{CC_MIN} (typically 8V), UVLO immediately stops the regulator from switching, and recharges V_{CC} via the HV current source. If this protection occurs, it resets once V_{CC} falls below V_{CC_PRO} (typically 6.3V). In this case, the HV current source is enabled once V_{CC} is below V_{CC_PRO}.

Short-Circuit Protection (SCP)

The current flowing through the current-sensing resistor can increase sharply. It can greatly exceed V_{CS_MAX} (typically 0.4V) after t_{LEB_L} (typically 200ns) under some fault conditions, such as a transformer winding short. Such a high current may damage the system. To prevent system damage, t_{LEB_S} (typically 150ns) is recommended to prevent the current from being too high.

The HFG611-45 does not enter short-circuit protection (SCP) immediately when V_{CS} exceeds the SCP threshold (V_{SCP}, typically 0.65V) after t_{LEB_S}. The device stops switching for t_{SCP} (typically 130µs), then starts switching again. If the HFG611-45 detects 8 consecutive pulses where V_{CS} exceeds V_{SCP}, SCP is triggered. Otherwise, the HFG611-45 resumes normal operation. SCP can be immune to surge testing.

Over-Temperature Protection (OTP)

To prevent lethal thermal damage, the HFG611-45 shuts down the switching cycle if the inner temperature exceeds 150°C. Once the inner junction temperature (T_J) drops below 110°C, the power supply resumes operation.

V_{CC} Over-Voltage Protection (OVP)

V_{CC} over-voltage protection (OVP) protects system operation. If V_{CC} exceeds the OVP level (V_{CC_OVP}, typically 53V) for the V_{CC} OVP delay time (t_{VCC_OVP}, typically 23µs), V_{CC} OVP is triggered.

ZCD Over-Voltage Protection (ZCD OVP) and Under-Voltage Protection (ZCD UVP)

The positive plateau is the auxiliary winding voltage when the gate is off. When the positive plateau is proportional to V_{OUT}, both ZCD over-voltage protection (ZCD OVP) and ZCD under-voltage protection (ZCD UVP) use the auxiliary winding voltage instead of monitoring V_{OUT} directly. Figure 10 shows the ZCD OVP and ZCD UVP block.

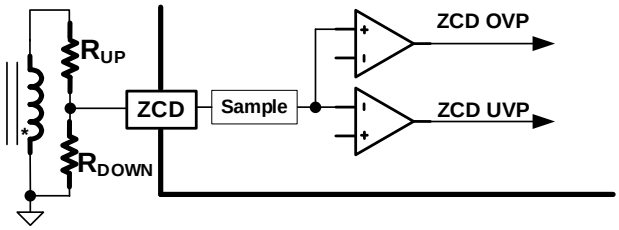

Figure 10: ZCD OVP and ZCD UVP Circuit

The plateau voltage (V_{ZCD}) can be calculated with Equation (1):

$$V_{ZCD} = \frac{V_{OUT} \times N_{AUX}}{N_S} \times \frac{R_{DOWN}}{R_{DOWN} + R_{UP}} \quad (1)$$

Where N_{AUX} is the transformer's auxiliary winding turns, and N_S is the transformer's secondary winding turns.

When V_{ZCD} reaches the ZCD OVP threshold (V_{ZCD_OVP}, typically 12.2V) for 3 consecutive cycles, ZCD OVP is triggered (see Figure 11).

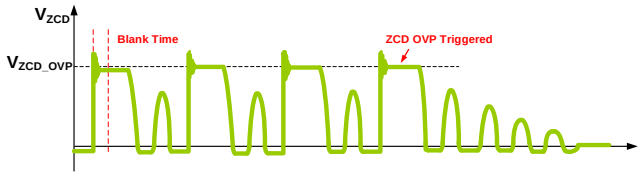

Figure 11: ZCD OVP Voltage Sampling

If the voltage sampled on the ZCD pin is below the ZCD UVP threshold (V_{ZCD_UVP}, typically 0.4V) for t_{ZCD_UVP} except during the soft-start period, then ZCD UVP is triggered (see Figure 12).

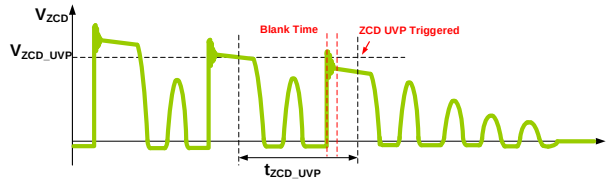

Figure 12: ZCD UVP Voltage Sampling

To avoid mistriggers due to the oscillation of the leakage inductance and the parasitic capacitance, both ZCD OVP and ZCD UVP sampling have a blanking time.

Overload Protection (OLP)

If f_{SW} is fixed in the flyback converter, the maximum P_{OUT} is limited by the peak current.

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If P_{OUT} exceeds the power limit, V_{OUT} drops below the set value. This reduces the current through the optocoupler, and V_{FB} is pulled high. If V_{FB} exceeds V_{OLP}, it is considered an error flag, and the internal timer begins counting. If the OLP condition lasts for the OLP timer duration (t_{OLP}, typically 50ms), OLP triggers and the HFG611-45 stops switching.

If the error flag is removed during the count period, the timer resets. This timer duration excludes the SS duration (t_{SOFT}). The OLP timer can avoid protection mistriggers during normal load transients.

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APPLICATION INFORMATION

Selecting the VCC Capacitor (C_{VCC})

Figure 13 shows the start-up circuit.

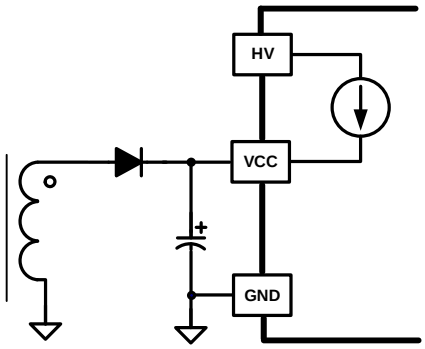

Figure 13: Start-Up Circuit

The HV pin charges V_{CC}. When V_{CC} reaches the HV supply current turn-off voltage (V_{CC_IOFF}), the HV pin stops charging V_{CC} and the IC starts to operate. To guarantee successful start-up, V_{OUT} should be set up before V_{CC} drops to the minimum operating voltage (V_{CC_MIN}). For most applications, choose a VCC capacitor (C_{VCC}) to be about 22µF. To ensure safe operation across the entire input and output range, especially under no-load conditions, V_{CC} should have some margin. It is recommended to have a minimum V_{CC} that is about 1V greater than V_{CC_MIN}. The recommended C_{VCC} can be calculated with Equation (2):

$$C_{VCC} > \frac{I_{OP} \times t_{START_UP}}{V_{CC_IOFF} - (V_{CC_MIN} + 1)} \quad (2)$$

Designing the Transformer

Table 2 shows a typical 45W application inductance calculation procedure.

Table 2: Designing the Transformer

Parameter	Symbol	Value
Input AC RMS Voltage	V_{AC}	$90V_{AC}$ to $265V_{AC}$
Output Voltage	V_{OUT}	15V
Output Current	I_{OUT}	3A
Efficiency	η	92%
Switching Frequency	f_{SW}	130kHz

The input power (P_{IN}) can be estimated with Equation (3):

$$P_{IN} = \frac{V_{OUT} \times I_{OUT}}{\eta} \quad (3)$$

According to the power device's voltage rating and selecting turns ratio, a proper N_{PS} should satisfy Equation (4) and Equation (5):

$$\sqrt{2}V_{AC_MAX} + N_{PS} \times V_{OUT} + V_{SPIKE_PRI} \le 0.9V_{BV_PRI} \quad (4)$$

$$\frac{\sqrt{2}V_{AC_MAX}}{N_{PS}} + V_{OUT} + V_{SPIKE_SEC} \le 0.9V_{BV_SEC} \quad (5)$$

In this application, N_{PS} = 6.

The converter's duty cycle can be calculated with Equation (6):

$$D = \frac{N_{PS} \times V_{OUT}}{\sqrt{2}V_{AC} + N_{PS} \times V_{OUT}} \quad (6)$$

According to the HFG611-45's operation mode, f_{SW} increases as V_{IN} increases, but a higher frequency means more switching loss and EMI. The HFG611-45 cannot turn on at the first valley in high line (see Figure 14).

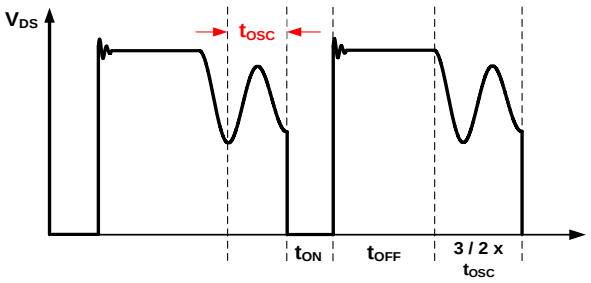

Figure 14: Switching Period in High Line

Where t_{OSC} is the DCM oscillation period, and is related to the inductance (L) and parasitic parameters. f_{SW} is 130kHz, and the oscillation period can be estimated to be 1.2µs. The switching period can be calculated with Equation (7):

$$\frac{1}{f_{SW}} = t_{ON} + t_{OFF} + \frac{3}{2}t_{OSC} \quad (7)$$

The on time (t_{ON}) and off time (t_{OFF}) for the duty cycle also satisfy Equation (8):

$$\frac{t_{ON}}{t_{OFF}} = \frac{D_{MIN}}{1 - D_{MIN}} \quad (8)$$

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In DCM flyback topology, Equation (9) and Equation (10) can be derived as follows:

$$P_{IN} = \frac{1}{2} L \times f_{SW} \times I_{PK}^2 \quad (9)$$

$$I_{PK} = \frac{\sqrt{2} V_{AC_MAX}}{L} \times T_{ON} \quad (10)$$

For Equation (3), Equation (4), Equation (5), Equation (6), Equation (7), Equation (8), and Equation (9), and Equation (10), *L* can be calculated with Equation (11):

$$L = \frac{f_{SW} \times \left(\sqrt{2} V_{AC_MAX}\right)^2 \times D_{MIN}^2}{2P_{IN}} \left(\frac{1}{f_{SW}} - \frac{3}{2} t_{OSC}\right)^2 \quad (11)$$

Where *L* = 300μH.

After calculating *L*, it is necessary to calculate the maximum inductor current (I_{PK_MAX}) before calculating the turns. According to the HFG611-45's operation mode, the inductor current (I_L) reaches its maximum when the input capacitor voltage drops to its lowest point (V_{DC_MIN}). At low line, the device locks the first valley (see Figure 15).

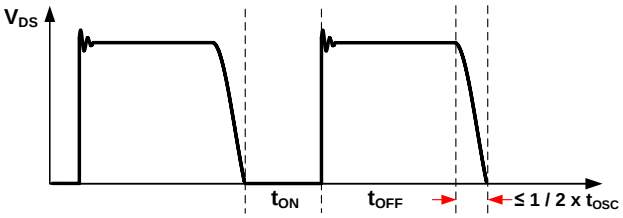

Figure 15: Switching Period in Low Line

Similarly, for Equation (3), Equation (4), Equation (5), Equation (6), Equation (7), Equation (8), Equation (9), and Equation (10), I_{PK_MAX} can be calculated with Equation (12):

$$I_{PK_MAX} = \frac{V_{DC_MIN} \times D_{MAX}}{L} \left(\frac{L \times I_{PK_MAX}^2}{2P_{IN}} - \frac{t_{OSC}}{2}\right) \quad (12)$$

Since 1 / 2 x t_{OSC} is a small value, it can be ignored; Equation (12) can be simplified with Equation (13):

$$I_{PK_MAX} = \frac{2P_{IN}}{V_{DC_MIN} \times D_{MAX}} \quad (13)$$

I_{PK_MAX} should be below the continuous DS current (typically 2.8A at 125°C). After calculating *L* and I_{PK_MAX} according to the magnetic core parameter, N_P and N_S can be calculated.

Selecting the Current Sense Resistor

The HFG610A-45's V_{CS_MAX} is 0.4V, so the current-sense resistor (R_{SENSE}) can be calculated with Equation (14):

$$R_{SENSE} = \frac{V_{CS_MAX}}{I_{PK_MAX}} \times 0.9 \quad (14)$$

The selected R_{SENSE} should ensure that I_{PK_MAX} is below the continuous DS current (typically 2.8A at 125°C).

Selecting the ZCD Divider Resistor

The ZCD pin integrates ZCD OVP. Suitable divider resistors should guarantee that ZCD OVP and ZCD UVP do not mistrigger and the ZCD OVP voltage is not too high. It is recommended for V_{ZCD} to be below 0.8 x V_{ZCD_OVP}, and V_{ZCD} to exceed V_{ZCD_UVP}. V_{ZCD} can be calculated with Equation (15):

$$V_{ZCD} = \frac{V_{OUT} \times N_{AUX}}{N_S} \times \frac{R_{DOWN}}{R_{DOWN} + R_{UP}} \quad (15)$$

Where N_{AUX} is the auxiliary winding turns of the transformer, and N_S is the secondary winding turns of the transformer.

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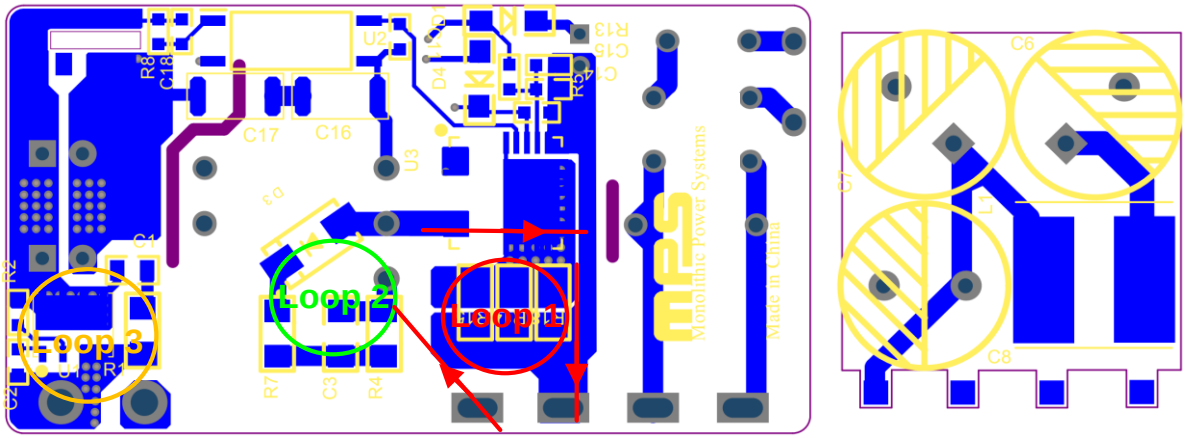
PCB Layout Guidelines

Efficient PCB layout is critical for achieving reliable operation and excellent EMI performance. For the best results, refer to Figure 16 and follow the guidelines below:

1. Minimize the power stage loop area, including the primary power loop (Loop 1), the snubber loop (Loop 2), and the secondary power loop (Loop 3).
2. Separate the IC GND and the power GND.
3. Place the decoupling capacitors for VCC, FB, CS, and ZCD close to the IC.
4. Route the EMI filter away from the hopping point.



Bottom Layer

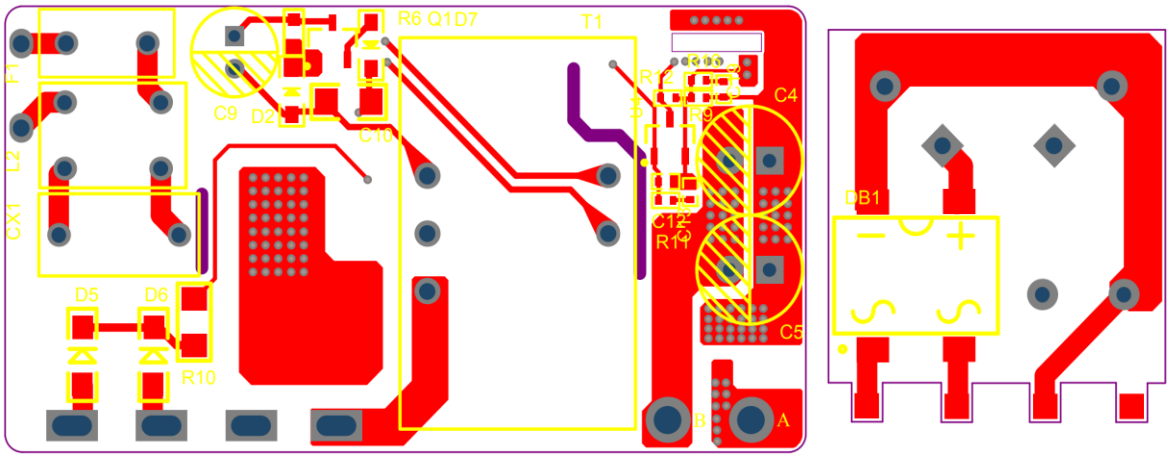


Figure 16: Top Layer

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TYPICAL APPLICATION CIRCUIT

Figure 17 shows the HFG611-45's typical application circuit with a universal input and 45W output specification.

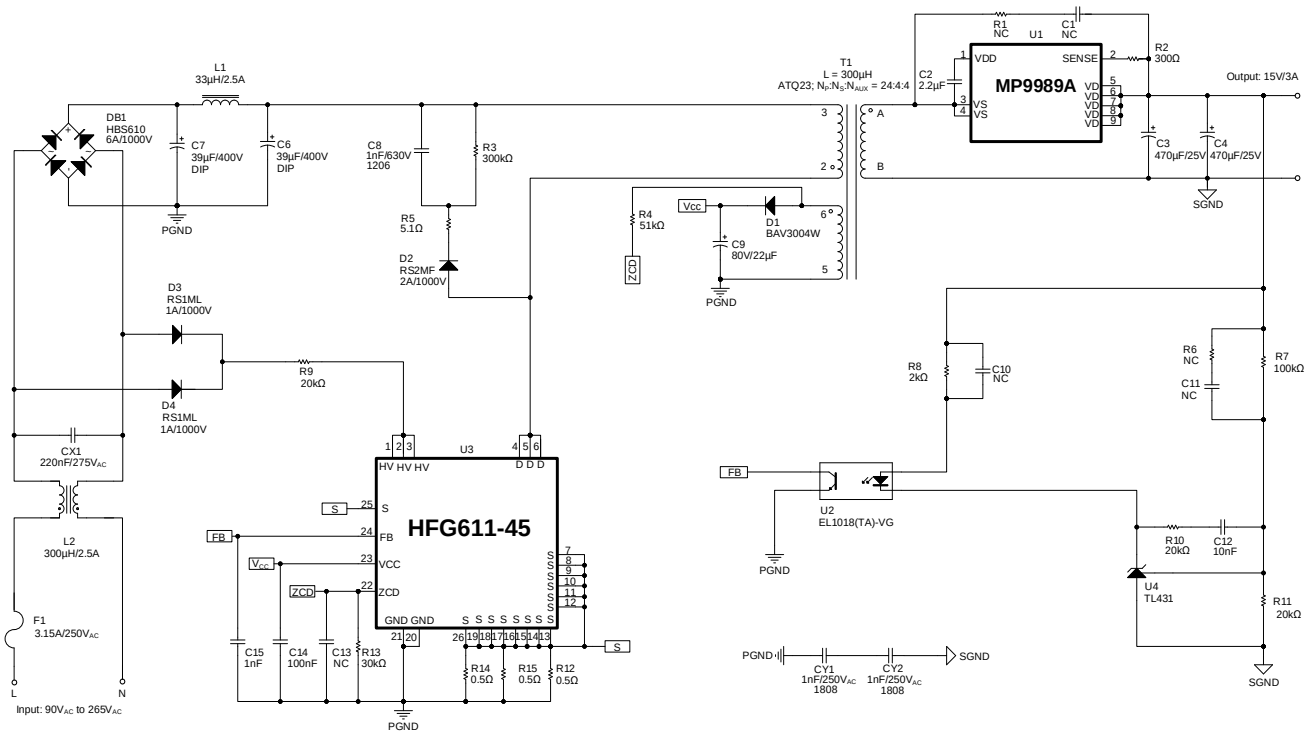

Figure 18: Typical Application Circuit (45W)

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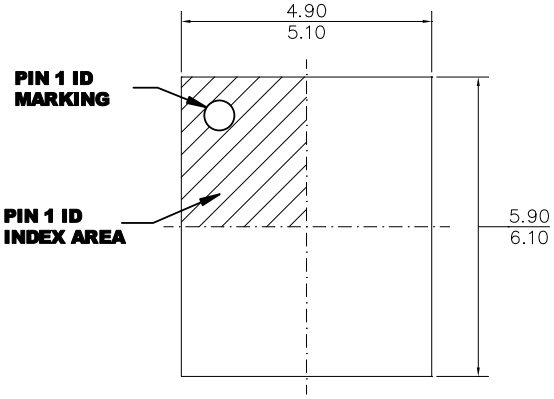
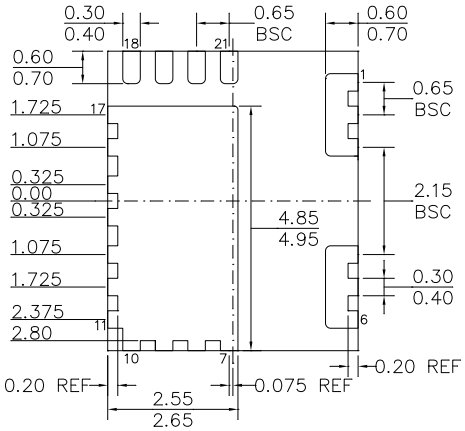
PACKAGE INFORMATION

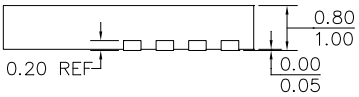
QFN-21 (5mmx6mm)



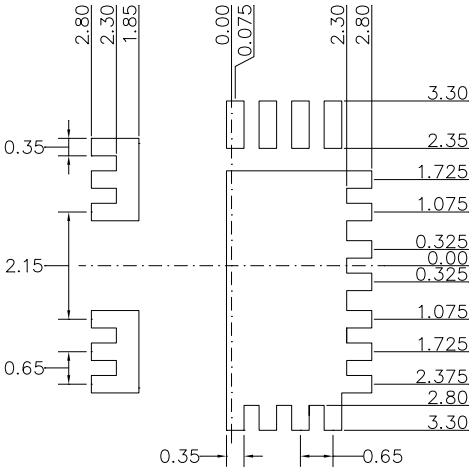
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

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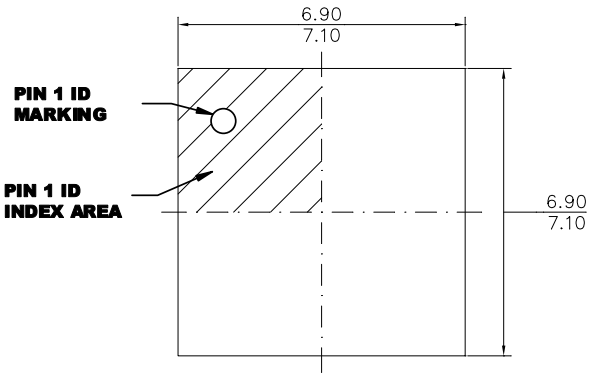
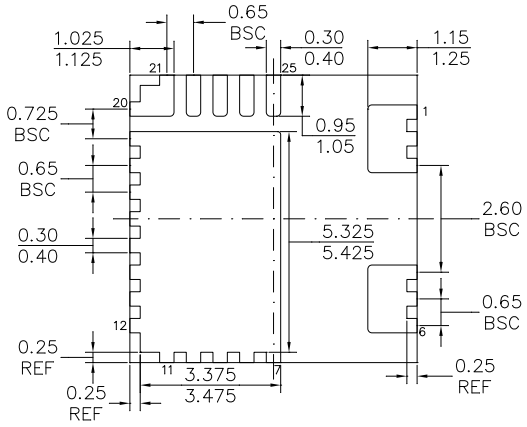
PACKAGE INFORMATION *(continued)*

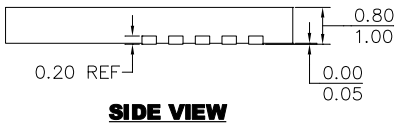
QFN-25 (7mmx7mm)



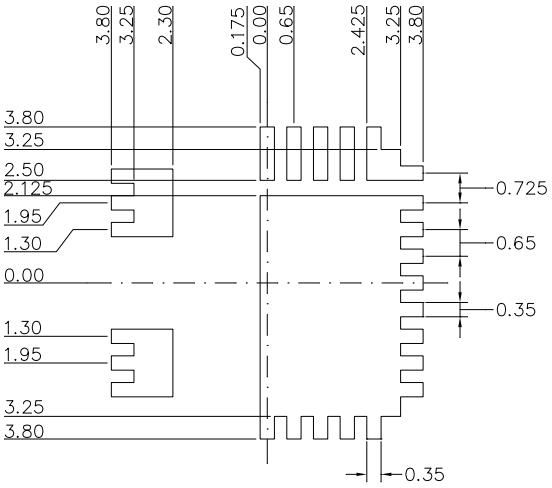
TOP VIEW



BOTTOM VIEW



SIDE VIEW



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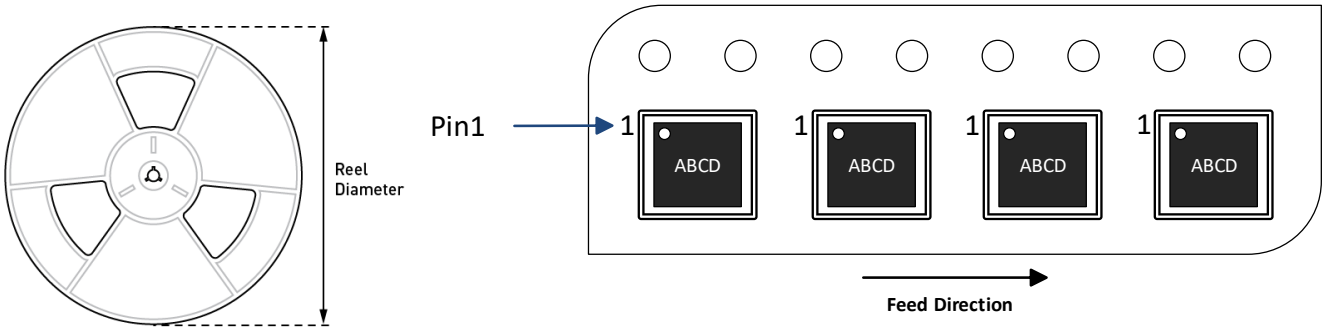
CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
HFG611GQJ-45-Z	QFN-21 (5mmx6mm)	5000	N/A	N/A	13in	12mm	8mm
HFG611GQN-45-Z	QFN-25 (7mmx7mm)	2500	N/A	N/A	13in	16mm	12mm

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REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	11/11/2024	Initial Release	-

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