EVQ77240FS-LT-00A

16V, 0.8A,180mΩ $R_{DS(ON)}$, Quad-Channel, High-Side Load Switch Evaluation Board, AEC-Q100 Qualified

DESCRIPTION

The EVQ77240FS-LT-00A evaluation board is designed to demonstrate the capabilities of the MPQ77240FS, a quad-channel high-side power switch for a nominal 0.8A load per channel. The device covers a 5V to 16V input voltage ($V_{INA/B}$) range.

The MPQ77240FS supports an internal current limit and a configurable, high-accuracy current limit via the I²C. This helps to clamp the inrush current under short-circuit conditions, which improves system reliability. A selectable start-up slew rate also helps to reduce the inrush current during start-up. In addition, a fast-off function can quickly turn off the device if the channel current increases sharply.

The MPQ77240FS communicates to the microcontroller (MCU) via the I²C interface. The device supports up to six addresses, set via an external resistor.

With the help of an internal analog-to-digital converter (ADC), the channel currents, supply voltages, reference voltage (V_{REF}), and output voltages can be obtained without additional external circuitry. Full diagnostics and protection are developed for the device, including input over-voltage (OV) and under-voltage (UV) detection, output OV for each channel, open-load and short-to-battery detection, over-current protection (OCP), fast-off short-circuit protection (SCP, fast-off) and over-temperature shutdown. Average and peak current detection improves diagnostic reliability in driver monitoring systems (DMS). Fault statuses can be reported via both the FT pin and I²C interface.

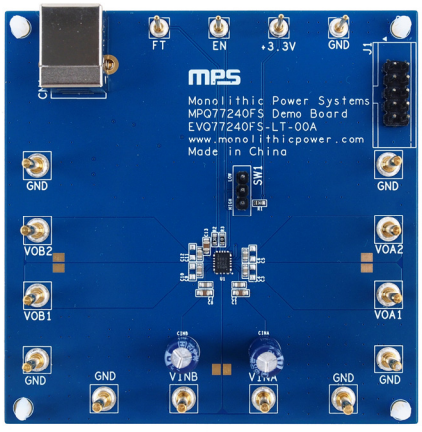
The MPQ77240FS is available in a TQFN-17 (3mmx4mm) package. It is available in AEC-Q100 Grade 1 and compliant with AEC-Q100-012 Test Grade A.

PERFORMANCE SUMMARY

Specifications are at T_A = 25°C, unless otherwise noted.

Parameters	Conditions	Value
Recommended continuous supply voltage		5V to 16V
Maximum output current (I_{OUT}) per channel		0.8A

EVQ77240FS-LT-00A EVALUATION BOARD



LxWxH (8.3cmx8.3cmx1cm)

Board Number	MPS IC Number
EVQ77240FS-LT-00A	MPQ77240FSGLTE-xxxx-AEC1

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QUICK START GUIDE

1. Connect the load terminals to:
   a. Positive (+): OUT_A1, OUT_A2, OUT_B1, OUT_B2
   b. Negative (-): GND
2. Preset the power supply output to the expected value (5V to 16V), and then turn it off.
3. Connect the power supply output terminals to:
   a. Positive (+): VINA/VINB
   b. Negative (-): GND
4. Connect a 3.3V power supply to the +3.3V connector.
5. After making the connections, turn on the VINA (VINB) power supply.
6. Select the correct I^2C address based on R3 (see Table 1). The default I^2C address is 0x70.

Table 1: I^2C Address Setting

Recommended R3	I^2C R/W
Tie to GND	0x70
3.65kΩ	0x73
5.62kΩ	0x74
8.06kΩ	0x75
11.0kΩ	0x76
float	0x77

7. Note that the IC is off by default when it has been connected to the evaluation board, so the user must enable OUT_A1, OUT_A2, OUT_B1, and OUT_B2 via the register.

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EVALUATION BOARD SCHEMATIC

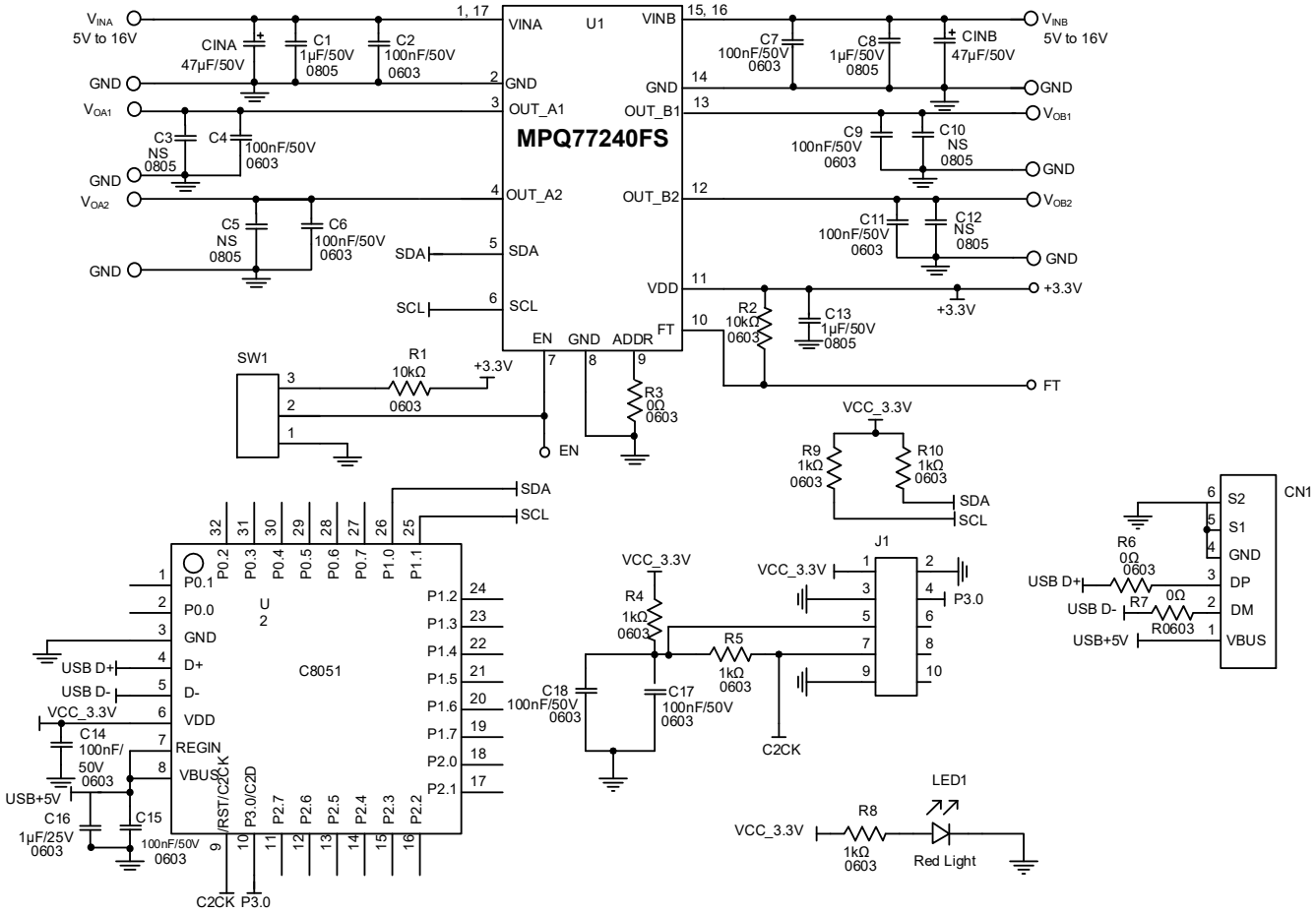

Figure 1: Evaluation Board Schematic

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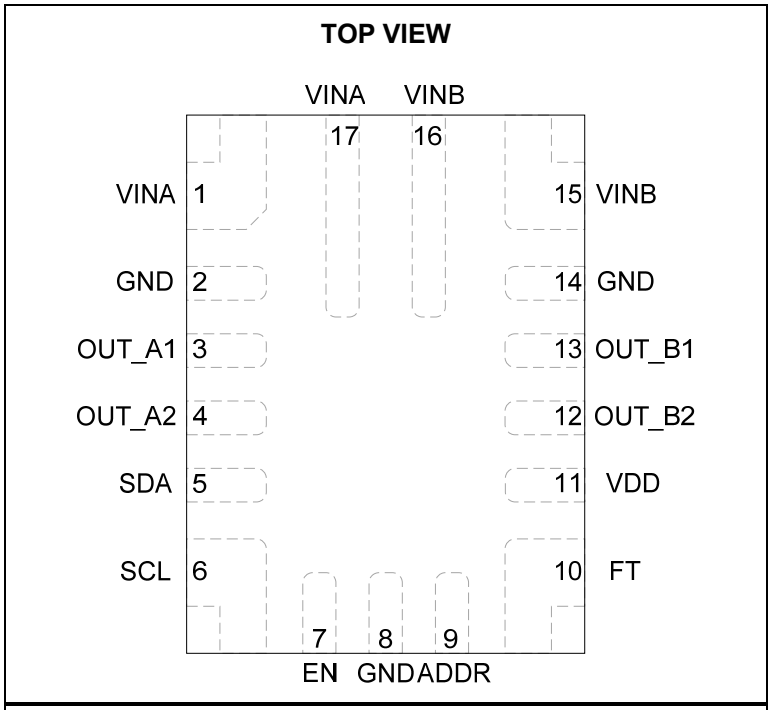
PACKAGE REFERENCE



TQFN-17 (3mmx4mm)

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EVQ77240FS-LT-00A BILL OF MATERIALS

Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
2	CINA,CINB	47μF	Electrolytic capacitor, 50V	DIP	Jianghai	CD263-50V47
3	C1, C8, C13	1μF	Ceramic capacitor, 50V, X7R	0805	Wurth	885012207103
10	C2, C4, C6, C7, C9, C11, C14, C15, C17, C18	0.1μF	Ceramic capacitor, 50V, X7R	0603	Murata	GRM188R71H104KA93D
0	C3, C5 C10, C12	NS				
1	C16	1μF	Ceramic capacitor, 25V, X7R	0603	Murata	GCM188R71E105KA64D
2	R1, R2	10kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-0710KL
3	R3, R6, R7	0Ω	Film resistor, 1%	0603	Yageo	RC0603FR-070RL
5	R4, R5, R8, R9, R10	1kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-071KL
1	CN1	10mm	USB Type-B connector	DIP	Any	
12	VOB1, VOA1, GND, VOB2, VOA2, VINB, VINA	2mm	Golden pin	DIP	Any	
4	GND, +3.3V, FT, EN	1mm	Golden pin	DIP	Any	
1	J1	180°, 2x 2.54mm	Connector	DIP	Any	
1	SW1	2.54mm	3-digit dip switch	DIP	Any	
1	LED1	Red	Red LED	0805	Baihong	BL-HUE35A-AV-TRB
1	U2	9mmx9mm	Microcontroller unit (MCU)	LQFP-32	Silicon	C8051F320-GQR
1	U1	MPQ77240FS-AEC1	16V, 0.8A, quad-channel, high-side switch	TQFN-17 (3mmx4 mm)	MPS	MPQ77240FSGLTE-xxxx-AEC1

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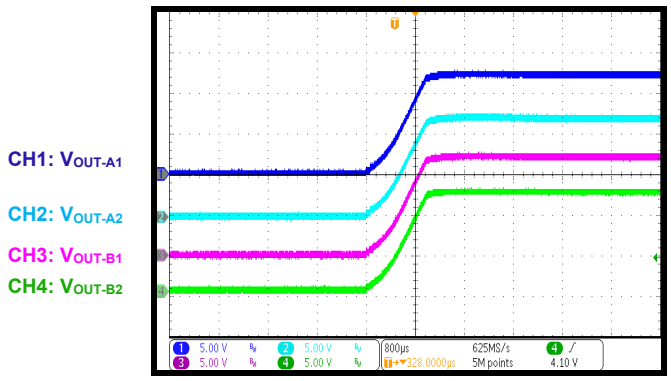
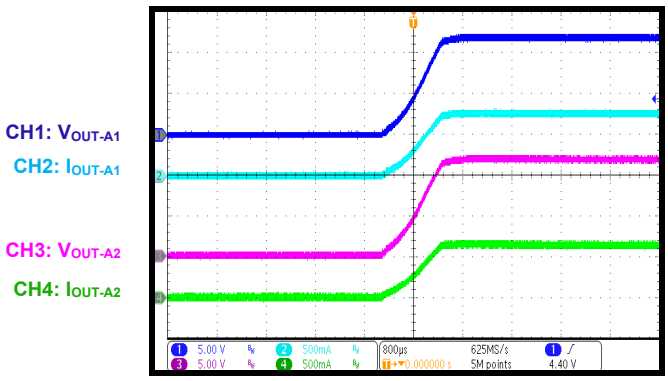
EVB TEST RESULTS

V_{INA} = V_{INB} = 12V, V_{DD} = 3.3V, soft-start time = 1ms, T_A = 25°C, unless otherwise noted.

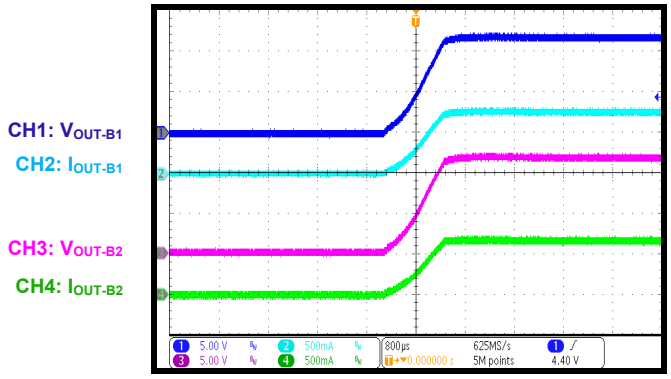
Start-Up through VIN
All I_{OUT} = 0A



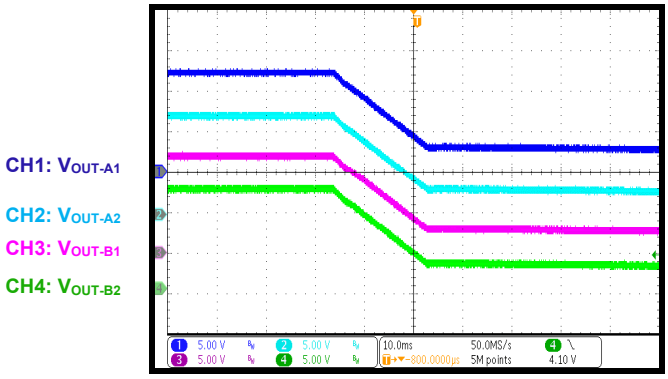
Start-Up through VIN
All I_{OUT} = 0.8A



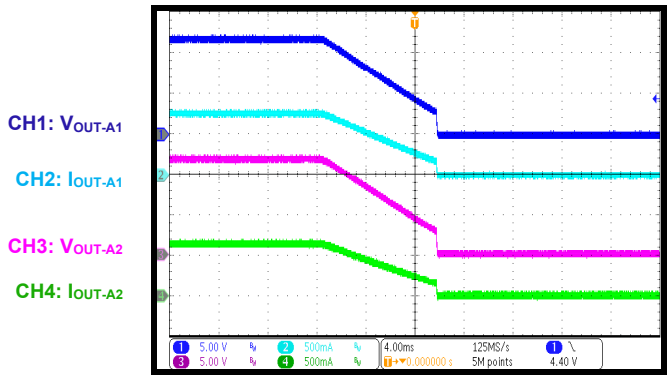
Start-Up through VIN
All I_{OUT} = 0.8A



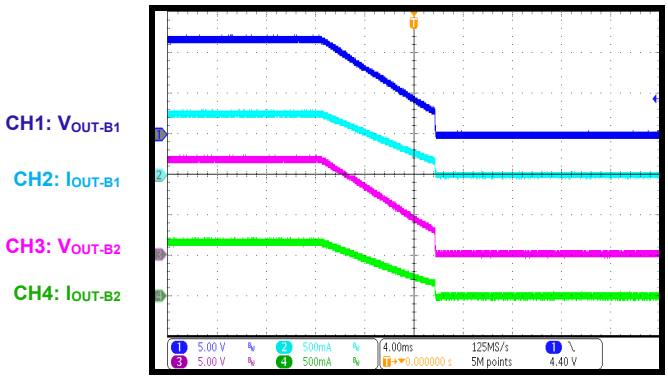
Shutdown through VIN
All I_{OUT} = 0A



Shutdown through VIN
All I_{OUT} = 0.8A



Shutdown through VIN
All I_{OUT} = 0.8A



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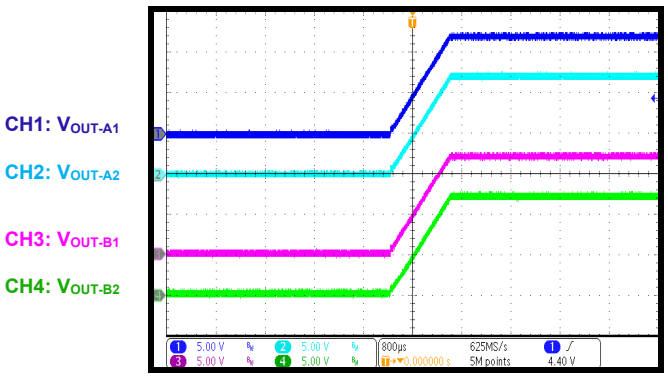
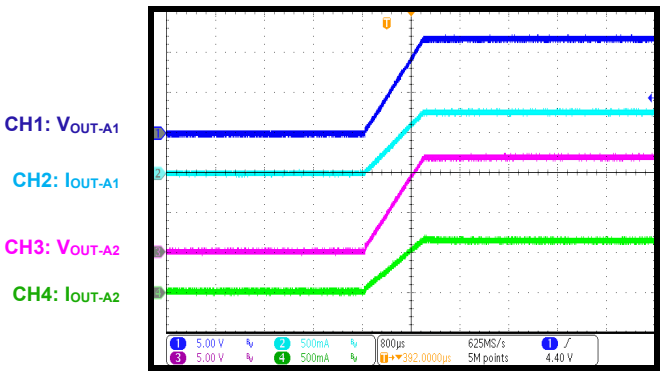
EVB TEST RESULTS *(continued)*

V_{INA} = V_{INB} = 12V, V_{DD} = 3.3V, soft-start time = 1ms, T_A = 25°C, unless otherwise noted.

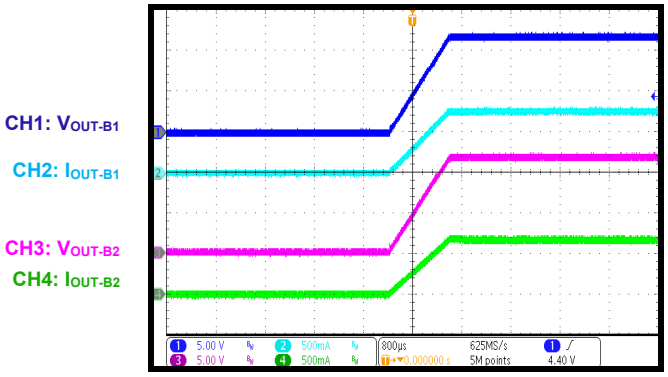
Start-Up through EN Channel
All I_{OUT} = 0A



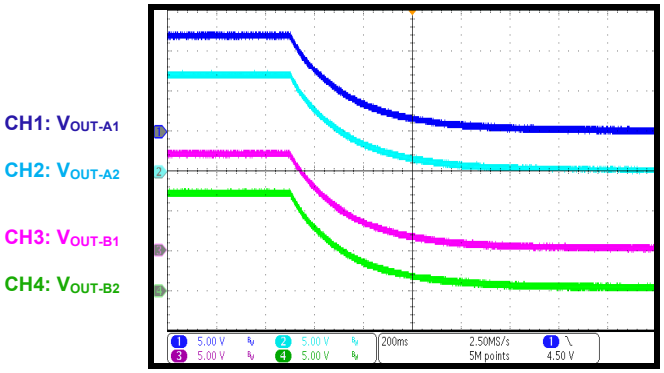
Start-Up through EN Channel
All I_{OUT} = 0.8A



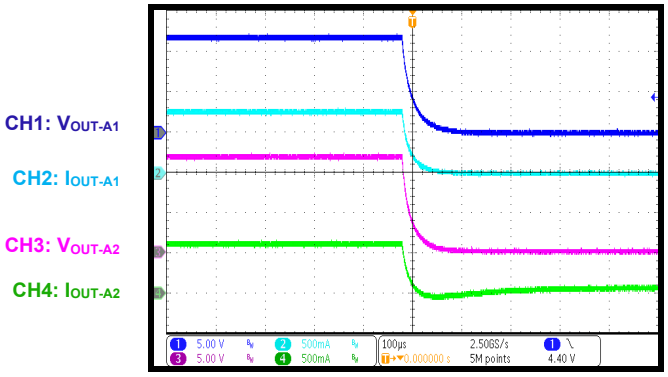
Start-Up through EN Channel
All I_{OUT} = 0.8A



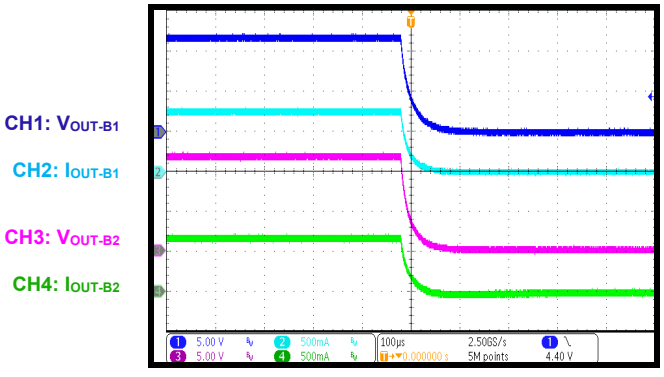
Shutdown through EN Channel
All I_{OUT} = 0A



Shutdown through EN Channel
All I_{OUT} = 0.8A



Shutdown through EN Channel
All I_{OUT} = 0.8A



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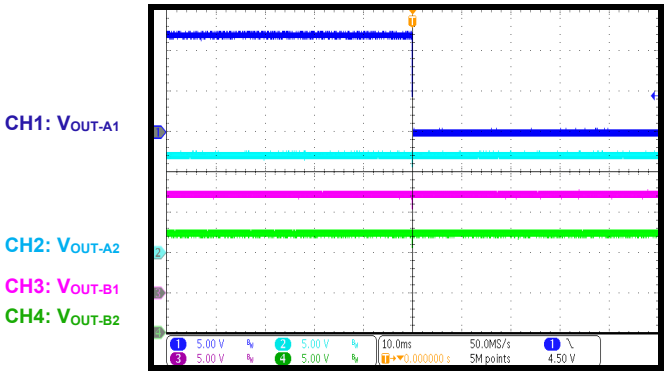
EVB TEST RESULTS *(continued)*

V_{INA} = V_{INB} = 12V, V_{DD} = 3.3V, soft-start time = 1ms, T_A = 25°C, unless otherwise noted.

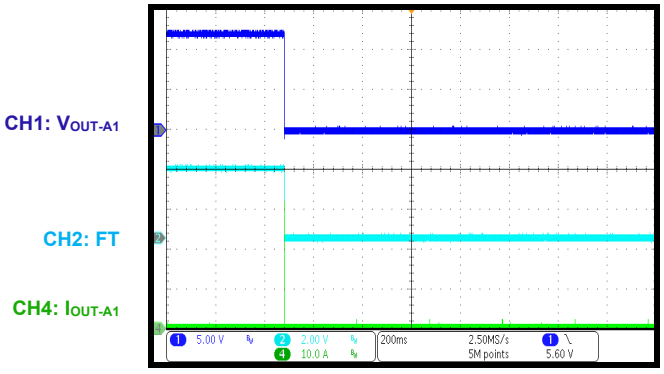
SCP Entry

All I_{OUT} = 0A, OUT_A1 SCP in auto-recovery mode



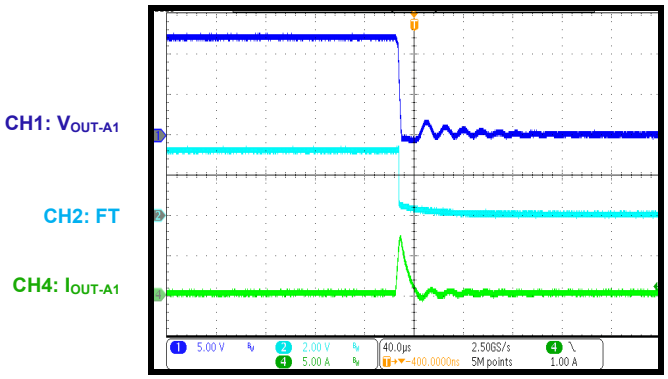
SCP Entry

All I_{OUT} = 0A, OUT_A1 SCP in auto-recovery mode



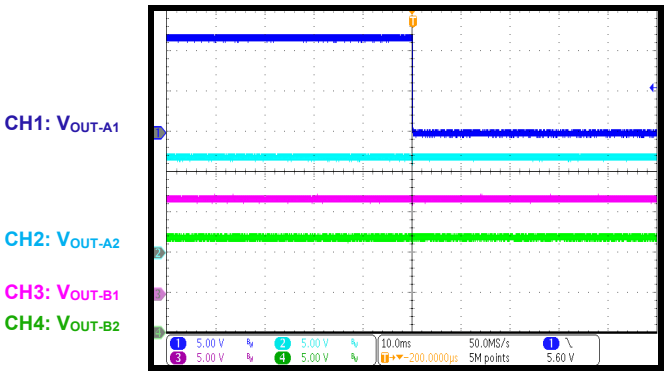
SCP Entry

All I_{OUT} = 0A, OUT_A1 SCP in auto-recovery mode



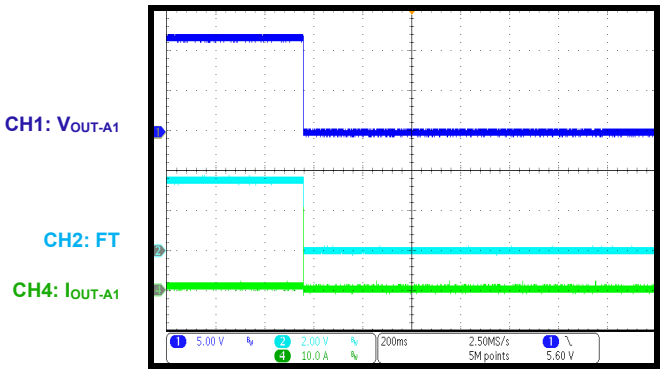
SCP Entry

All I_{OUT} = 0.8A, OUT_A1 SCP in auto-recovery mode



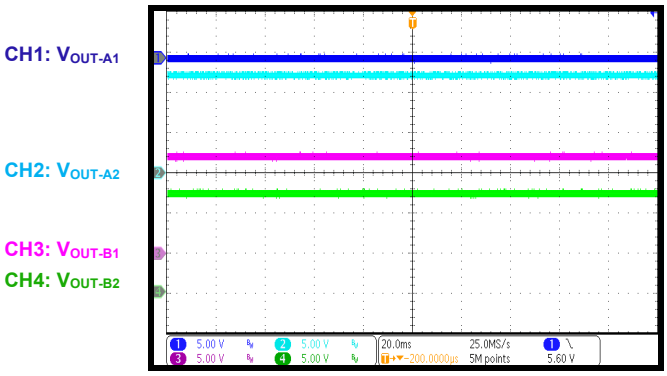
SCP Entry

All I_{OUT} = 0.8A, OUT_A1 SCP in auto-recovery mode



SCP Steady State

All I_{OUT} = 0.8A, OUT_A1 SCP in auto-recovery mode



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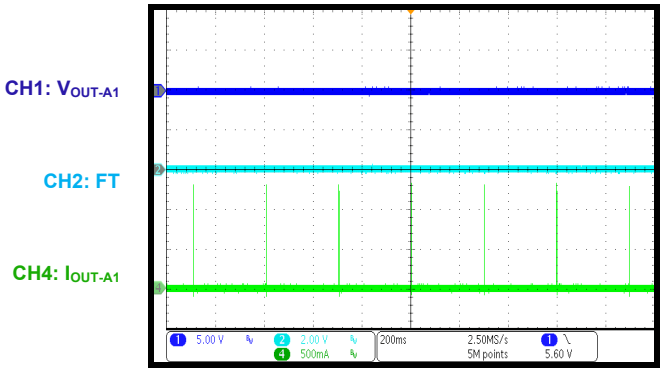
EVB TEST RESULTS *(continued)*

V_{INA} = V_{INB} = 12V, V_{DD} = 3.3V, soft-start time = 1ms, T_A = 25°C, unless otherwise noted.

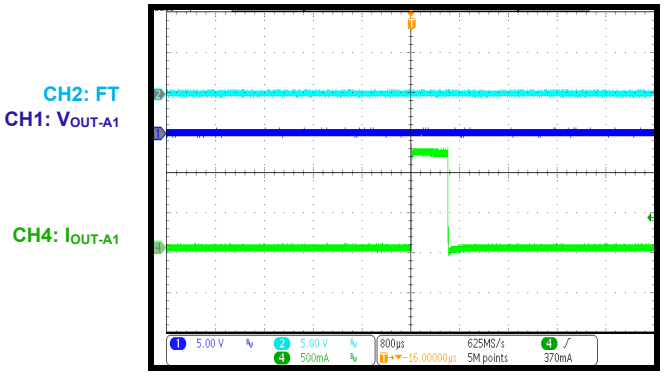
SCP Steady State

All I_{OUT} = 0.8A, OUT_A1 SCP in auto-recovery mode



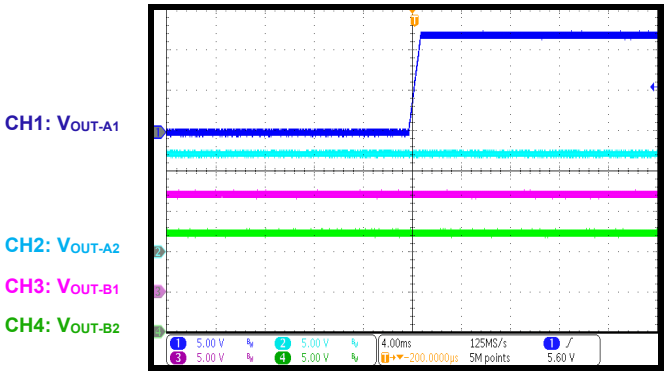
SCP Steady State

All I_{OUT} = 0.8A, OUT_A1 SCP in auto-recovery mode



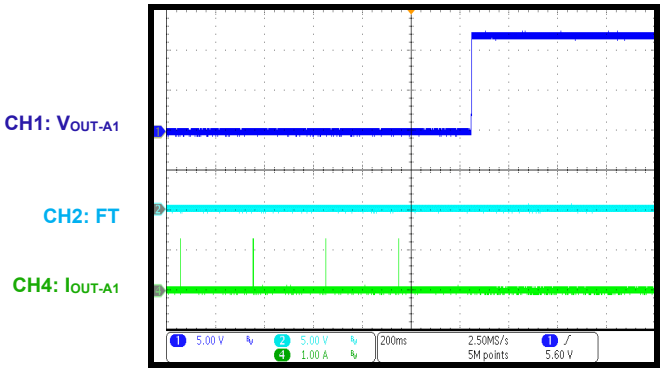
SCP Recovery

All I_{OUT} = 0A, OUT_A1 SCP in auto-recovery mode



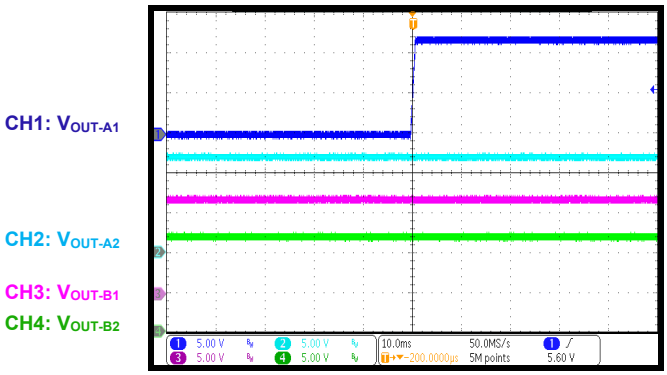
SCP Recovery

All I_{OUT} = 0A, OUT_A1 SCP in auto-recovery mode



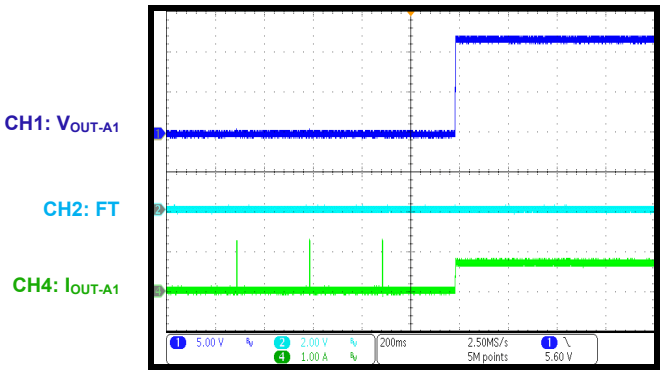
SCP Recovery

All I_{OUT} = 0.8A, OUT_A1 SCP in auto-recovery mode



SCP Recovery

All I_{OUT} = 0.8A, OUT_A1 SCP in auto-recovery mode



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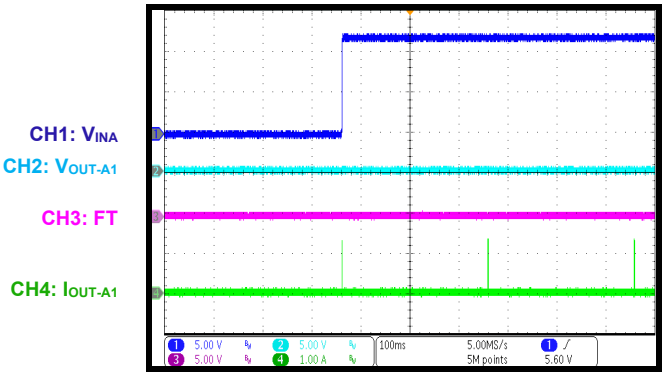
EVB TEST RESULTS *(continued)*

V_{INA} = V_{INB} = 12V, V_{DD} = 3.3V, soft-start time = 1ms, T_A = 25°C, unless otherwise noted.

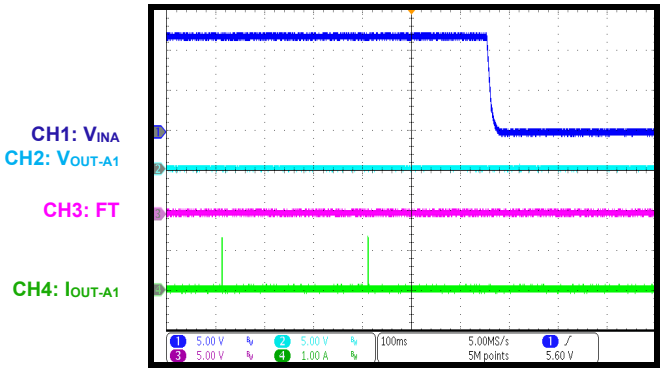
SCP Start-Up

All I_{OUT} = 0.8A, OUT_A1 SCP in auto-recovery mode



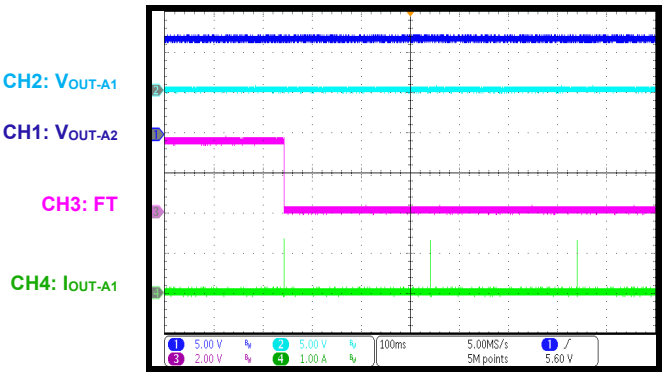
SCP Shutdown

All I_{OUT} = 0.8A, OUT_A1 SCP in auto-recovery mode



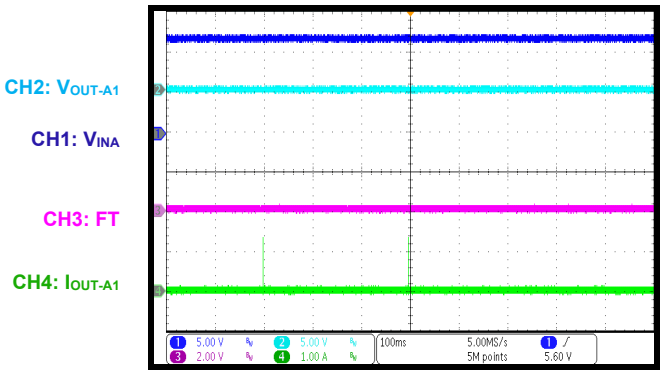
SCP EN Channel On

All I_{OUT} = 0.8A, OUT_A1 SCP in auto-recovery mode



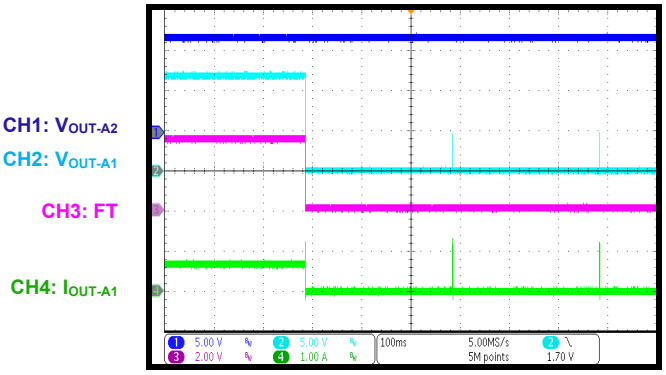
SCP EN Channel Off

All I_{OUT} = 0.8A, OUT_A1 SCP in auto-recovery mode



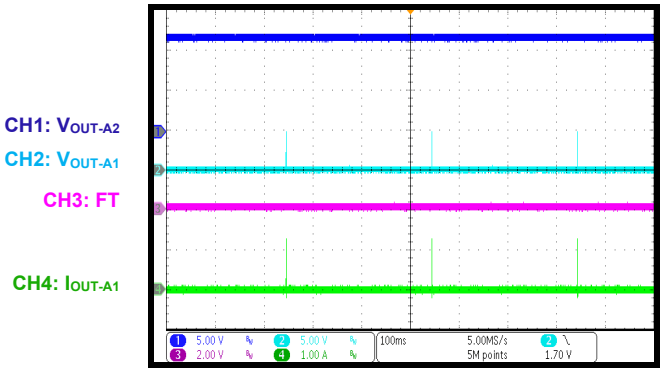
OCP Entry

All I_{OUT} = 0.8A, OUT_A1 SCP in auto-recovery mode



OCP Steady State

All I_{OUT} = 0.8A, OUT_A1 SCP in auto-recovery mode



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PCB LAYOUT

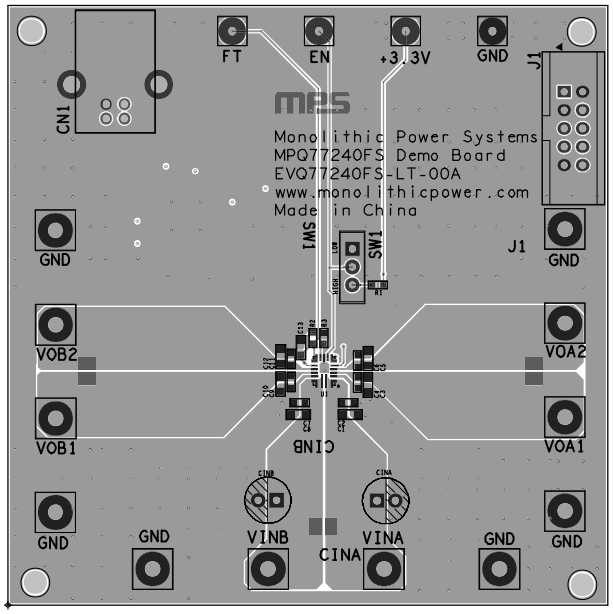

Figure 2: Top Layer

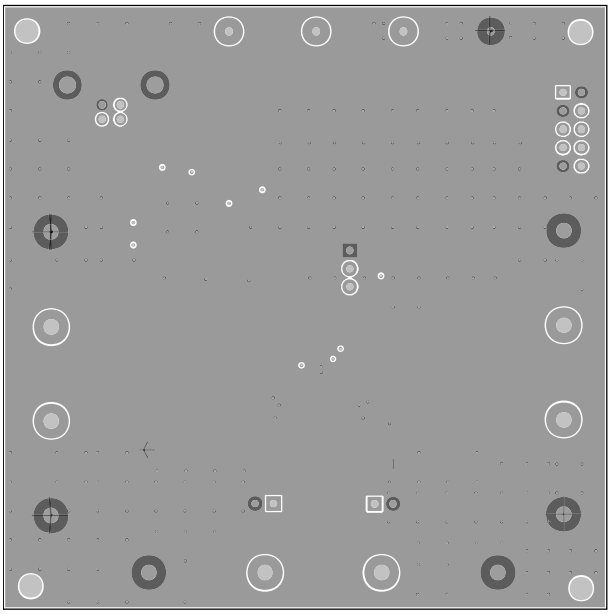

Figure 3: Mid-Layer 1

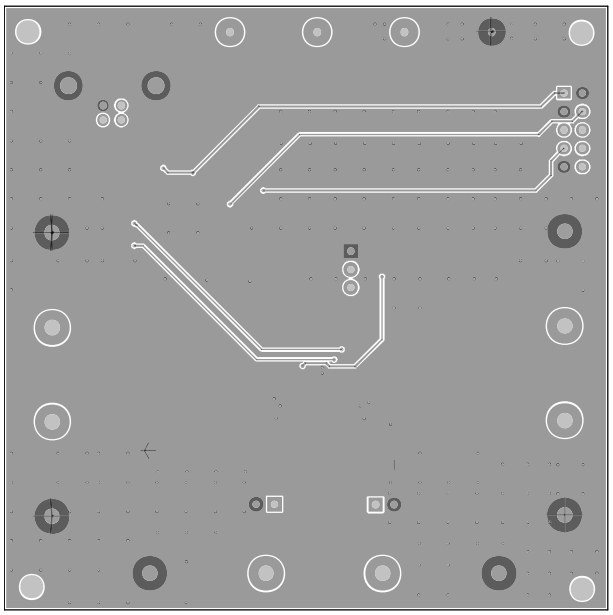

Figure 4: Mid-Layer 2

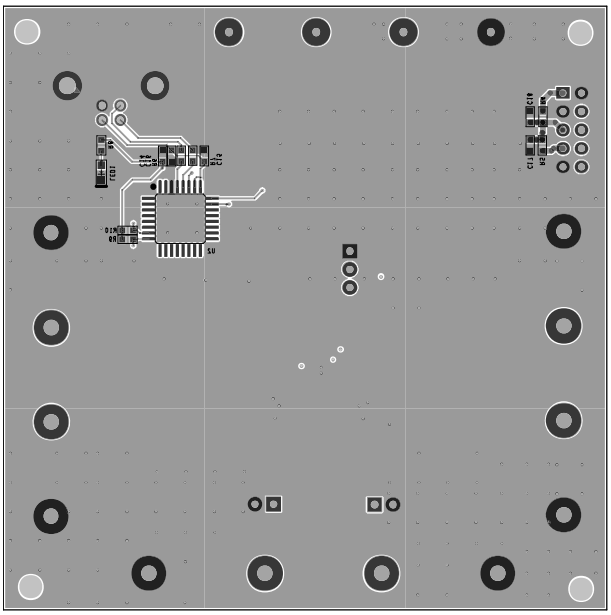

Figure 5: Bottom Layer

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REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	9/6/2024	Initial Release	-

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