EVQ70241FS-RH-00A

MPSafe™ ASIL-B, 18V, 4-Channel PMIC with 3 Bucks and 1 LDO, Uprated Current Evaluation Board, AEC-Q100 Qualified

DESCRIPTION

The EVQ70241FS-RH-00A is an evaluation board designed to demonstrate the capabilities of the MPQ70241FS, a power management IC (PMIC) solution that integrates three high-efficiency step-down DC/DC converters and a low-noise, low-dropout (LDO) regulator.

The MPQ70241FS uses a unique, dual-stage, 18V buck architecture that maximizes efficiency for the 1.8V image sensor input/output (I/O) rail in the complementary metal oxide semiconductor (CMOS) sensor in high-resolution camera modules.

Constant-on-time (COT) control with phase-locked loop (PLL) provides fast transient response time. The MPQ70241FS supports a 2.2MHz fixed switching frequency (f_{SW}).

The MPQ70241FS supports a PMBus interface for application flexibility. In addition, fault statuses can be monitored. Fault protections include input under-voltage lockout (UVLO), over-current protection (OCP), over-voltage protection (OVP), under-voltage protection (UVP), and thermal shutdown. A one-time programmable (OTP) memory is provided to preset these functions.

The MPQ70241FS supports applications with a high automotive safety integrity level, up to ASIL-B. Functional safety features include analog built-in self-testing (ABIST), diagnostics, and a power good (PG) output pin. The MPQ70241FS is developed under MPS's advanced MPSafe™ functional safety product development process, which has been independently certified to meet ISO 26262 guidelines.

The EVQ70241FS-RH-00A is a fully assembled and tested evaluation board. The MPQ70241FS is available in a QFN-15 (2.5mmx3.5mm) package with wettable flanks, and is available in AEC-Q100 Grade 1.

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PERFORMANCE SUMMARY

Specifications are at T_A = 25°C, unless otherwise noted.

Parameters	Conditions	Value
Input voltage (V_{IN}) range		3.5V to 18V
Buck 1 output voltage (V_{OUT1})	V_{IN} = 3.5V to 18V, I_{OUT1} = 0A to 1A, I_{OUT3} = I_{LDO} = 0A	3V
Buck 1 maximum output current (I_{OUT1})	V_{IN} = 3.5V to 18V, V_{OUT1} = 3V, I_{OUT3} = I_{LDO} = 0A	1A
Buck 2 output voltage (V_{OUT2})	V_{IN} = 3.5V to 18V, I_{OUT2} = 0A to 0.6A	1.8V
Buck 2 maximum output current (I_{OUT2})	V_{IN} = 3.5V to 18V, V_{OUT2} = 1.8V	0.6A
Buck 3 output voltage (V_{OUT3})	V_{IN} = 3.5V to 18V, V_{OUT1} = 3V, I_{OUT3} = 0A to 1.5A, I_{OUT1} = 0A	1.2V
Buck 3 maximum output current (I_{OUT3})	V_{IN} = 3.5V to 18V, V_{OUT1} = 3V, V_{OUT3} = 1.2V, I_{OUT1} = 0A	1.5A
LDO output voltage (V_{LDO})	V_{IN} = 3.5V to 18V, V_{OUT1} = 3V, I_{LDO} = 0A to 0.2A, I_{OUT1} = 0A	2.5V
LDO maximum output current (I_{LDO})	V_{IN} = 3.5V to 18V, V_{OUT1} = 3V, V_{LDO} = 2.5V, I_{OUT1} = 0A	0.2A
Buck 1 typical efficiency	V_{IN} = 8V, V_{OUT1} = 3V, I_{OUT1} = 1A, other rails are disabled	87.9%
Buck 1 peak efficiency	V_{IN} = 4V, V_{OUT1} = 3V, I_{OUT1} = 0.2A, other rails are disabled	93.9%
Buck 2 typical efficiency	V_{IN} = 8V, V_{OUT2} = 1.8V, I_{OUT2} = 0.6A, other rails are disabled	82.4%
Buck 2 peak efficiency	V_{IN} = 4V, V_{OUT2} = 1.8V, I_{OUT2} = 0.25A, other rails are disabled	90.2%
Buck 3 typical efficiency	V_{IN3} = 3.3V, V_{OUT3} = 1.2V, I_{OUT3} = 1.5A, LDO is disabled	80%
Buck 3 peak efficiency	V_{IN3} = 2.5V, V_{OUT3} = 1.2V, I_{OUT3} = 0.3A, LDO is disabled	89.4%
Switching frequency (f_{SW})		2.2MHz

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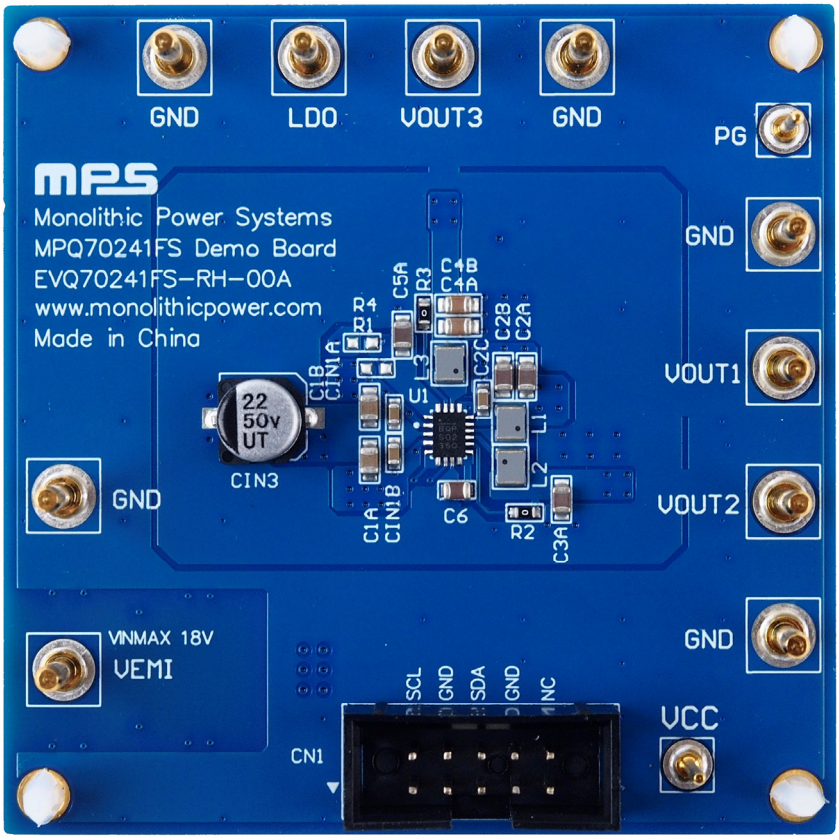
EVQ70241FS-RH-00A EVALUATION BOARD



LxWxH (6.35cmx6.35cmx1cm)

Board Number	MPS IC Number
EVQ70241FS-RH-00A	MPQ70241FSGRHE-0000AEC1

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QUICK START GUIDE

The EVQ70241FS-RH-00A evaluation board is easy to set up and use to evaluate the MPQ70241FS's performance. For the proper measurement equipment set-up, refer to Figure 2 on page 4 and follow the steps below:

1. Preset the power supply (V_{IN}) between 3.5V and 18V, then turn off the power supply.
2. Set the load current for each channel (I_{OUT2} = 0A to 0.6A, I_{OUT3} = 0A to 1.5A, and I_{LDO} = 0A to 0.2A).(1) Electronic loads represent a negative impedance to the converter, and setting a current too high can trigger hiccup mode.
3. If longer cables (>0.5m total) are used between the source and the evaluation board, place a damping capacitor at the input terminals.
4. Connect the power supply terminals to:
   a. Positive (+): VEMI
   b. Negative (-): GND
5. Connect the load terminals to:
   a. Positive (+) channel: VOUT2, VOUT3, or LDO
   b. Negative (-) channel: GND
6. After making the connections, turn on the power supply. The MPQ70241FS should start up automatically.
7. Evaluate with the PMBus digital interface by following the steps below:
   a. Download and install the Virtual Bench Pro 4.0 (VBP 4.0) GUI software from the MPS website. The MPQ70241FS GUI is embedded in VBP 4.0.
   b. Connect the EVKT-USBI2C-02 to CN1 with a ribbon cable, then connect the EVKT-USBI2C-02 to the computer with a USB cable. The EVKT-USBI2C-02 (including the ribbon cable and USB cable) is included with product evaluation kits, or can be purchased separately from the MPS website.
   c. Using the MPQ70241FS GUI, scan for the evaluation board address, which is 03h by default.
   d. Evaluate and configure the device, such as the turn-on delay time and soft-start time (t_{SS}), using the MPQ70241FS GUI. Figure 1 shows the PMBus evaluation kit set-up.

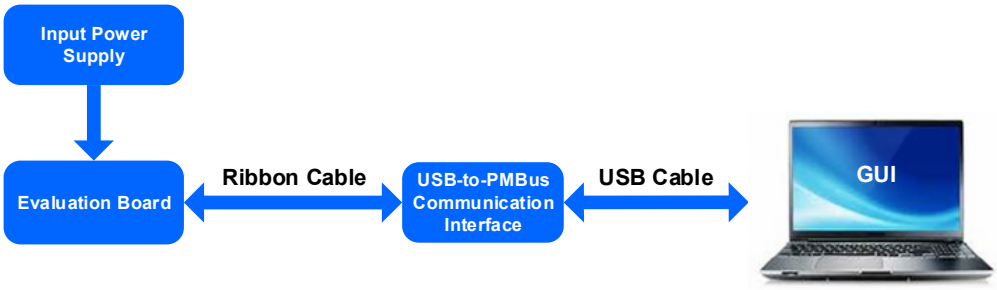

Figure 1: PMBus Evaluation Kit Set-Up

Note:

1) Buck 1's output is the input for buck 3 and the LDO. Do not let the total load current of buck 1 exceed 1A to avoid triggering buck 1's over-current protection (OCP).

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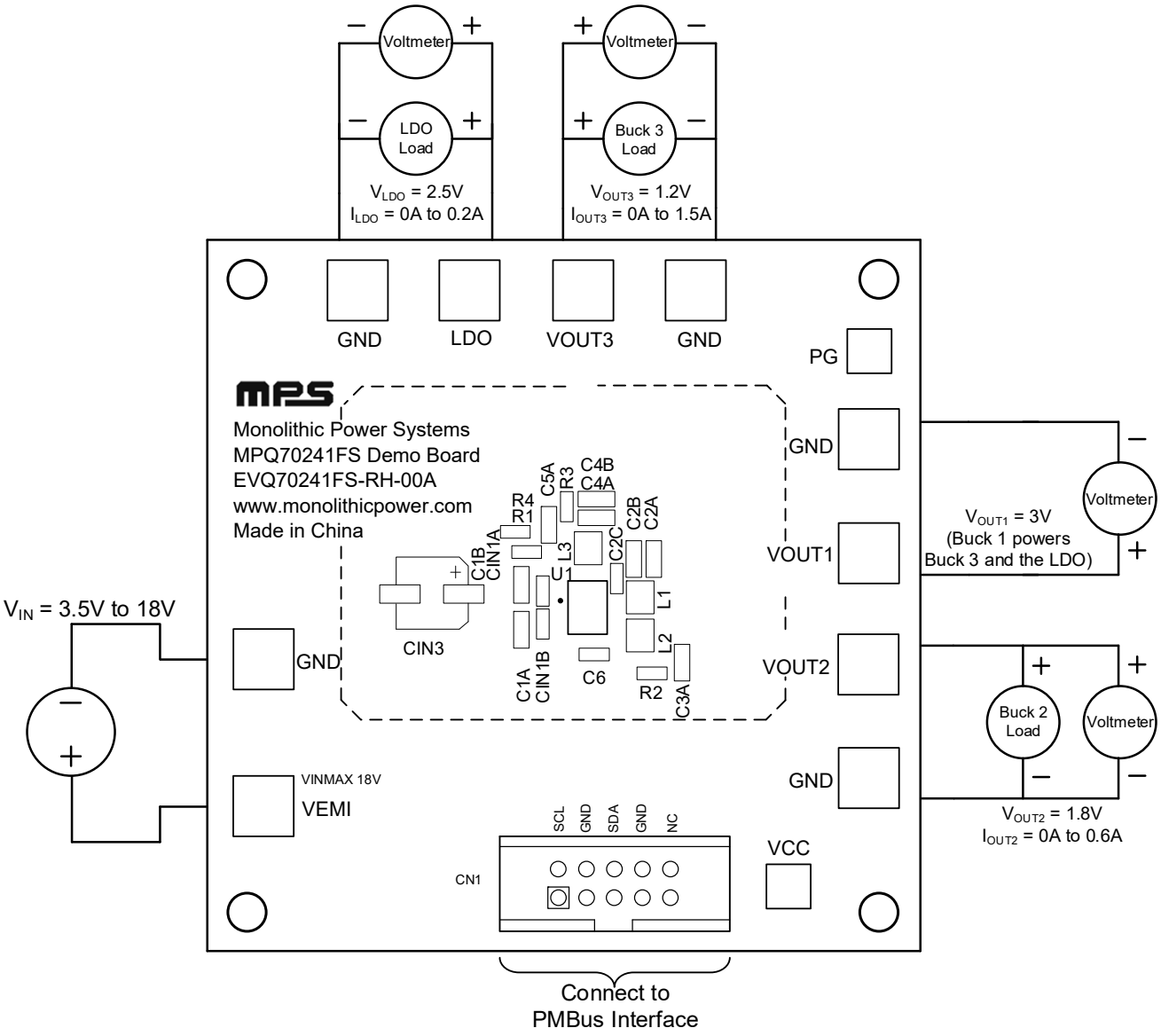

Figure 2: Measurement Equipment Set-Up

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MPQ70241FS-0000 DEFAULT REGISTER VALUES

Register Number	Page	Register Name	Register Value	Description
01h	0	OPERATION	80h	Buck 1 is enabled.
10h	0	WRITE_PROTECT	00h	Enable writes to all registers.
21h	0	VOUT_COMMAND	05h	V_{OUT1} = 3V
61h	0	TON_RISE	00h	Buck 1's soft-start time = 0.5ms
C4h	0	FREQ_DITHER	11h	Frequency spread spectrum (FSS) is disabled.
C5h	0	PG_MAPPING	00h	A communication failure, CRC failure, reference failure, or BIST failure causes PG to go low and register assertion.
CBh	0	PROTECTION_CONFIG	1Ch	• V_{OUT} OVP/UVP enabled • Built-in self-testing (BIST) enabled • PG_REACTION = 0, PG low fault does not cause a safe state • Packet error checking (PEC) is disabled
CCh	0	PG_CONFIG	03h	• V_{PGOUT} = 1.8V • PG de-assertion time = 2ms • PG threshold = ±6%
CDh	0	GATE_DRIVE_STRENGTH	03h	High gate drive strength is selected.
CEh	0	LIGHT_LOAD	02h	• Output discharge is enabled • Continuous conduction mode (CCM) is selected as the light-load mode
CFh	0	TON_OFF_DELAY	00h	• Buck 1's turn-on delay time = 0ms • Buck 1's turn-off delay time = 0ms
D0h	0	TON_OFF_SCALE	00h	Turn-on/turn-off delay scale = 0.25ms
D1h	0	FREQUENCY_ILIM_SCALE	01h	• f_{SW1} = f_{SW2} = f_{SW3} = 2.2MHz • Current limit scale = 125%
D2h	0	VIN_START_STOP	00h	• V_{IN_START} = UVLO threshold • V_{IN_STOP} = UVLO threshold
D3h	0	ADDRESS	03h	The chip's PMBus communication address is 03h.
01h	1	OPERATION	80h	Buck 2 is enabled.
21h	1	VOUT_COMMAND	18h	V_{OUT2} = 1.8V
61h	1	TON_RISE	00h	Buck 2's soft-start time = 0.5ms
CFh	1	TON_OFF_DELAY	00h	• Buck 2's turn-on delay time = 0ms • Buck 2's turn-off delay time = 0ms
01h	2	OPERATION	80h	Buck 3 is enabled.
21h	2	VOUT_COMMAND	0Ch	V_{OUT3} = 1.2V
61h	2	TON_RISE	00h	Buck 3's soft-start time = 0.5ms
CFh	2	TON_OFF_DELAY	00h	• Buck 3's turn-on delay time = 0ms • Buck 3's turn-off delay time = 0ms
01h	3	OPERATION	80h	The LDO is enabled.
21h	3	VOUT_COMMAND	26h	V_{LDO} = 2.5V
CFh	3	TON_OFF_DELAY	00h	• LDO's turn-on delay time = 0ms • LDO's turn-off delay time = 0ms

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EVALUATION BOARD SCHEMATIC

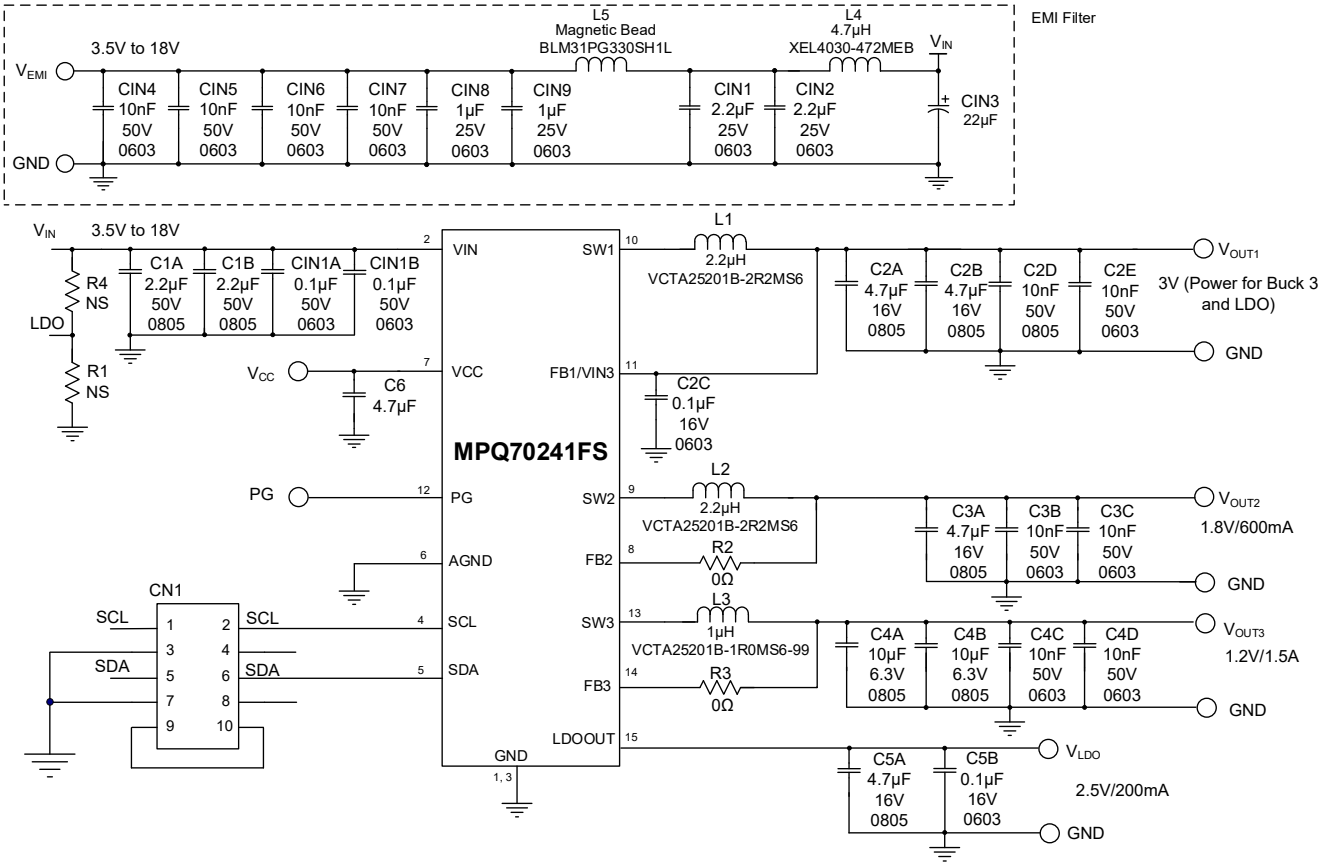
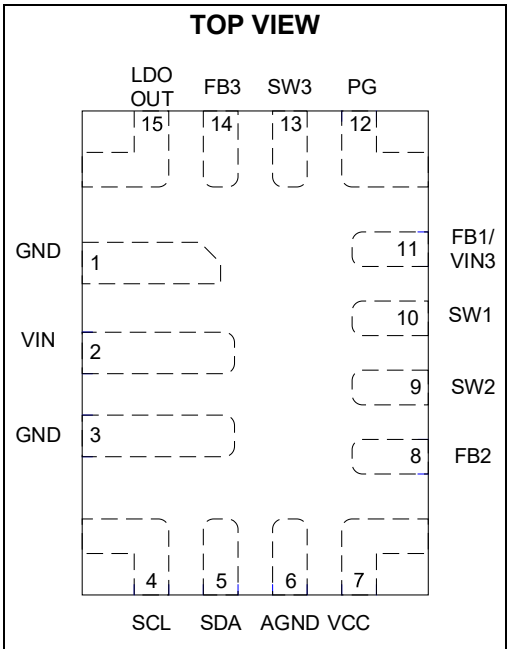


Figure 3: Evaluation Board Schematic

PACKAGE REFERENCE



QFN-15 (2.5mmx3.5mm)

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EVQ70241FS-RH-00A BILL OF MATERIALS

Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
2	C1A, C1B	2.2µF	Ceramic capacitor, 50V, X7R	0805	TDK	CGA4J3X7R1H225K125 AB
2	CIN1A, CIN1B	0.1µF	Ceramic capacitor, 50V, X7R	0603	Murata	GRM188R71H104KA93D
2	CIN1, CIN2	2.2µF	Ceramic capacitor, 25V, X7S	0603	Murata	GRM188C71E225KE11D
1	CIN3	22µF	Electrolytic capacitor, 50V	SMD	Cotronic	UT1H220M0605VG
5	C2A, C2B, C3A, C5A, C6	4.7µF	Ceramic capacitor, 16V, X7R	0805	Murata	GCM21BR71C475KA73L
2	C4A, C4B	10µF	Ceramic capacitor, 6.3V, X7R	0805	Murata	GCM21BR70J106KE22L
2	C2C, C5B	0.1µF	Ceramic capacitor, 16V, X7R	0805	Murata	GRM188R71C104KA01D
10	C2D, C2E, C3B, C3C, C4C, C4D, CIN4, CIN5, CIN6, CIN7	10nF	Ceramic capacitor, 50V, X7R	0603	Murata	GRM188R71H103KA01D
2	CIN8, CIN9	1µF	Ceramic capacitor, 25V, X7R	0603	Murata	GCM188R71E105KA64D
2	L1, L2	2.2µH	Inductor, 70mΩ DCR, 3.5A	0603	Murata	VCTA25201B-2R2MS6
1	L3	1µH	Inductor, 35mΩ DCR, 3.8A	SMD	Cyntec	VCTA25201B-1R0MS6-99
1	L4	4.7µH	Inductor, 44.1mΩ DCR, 5.1A	SMD	Cyntec	XEL4030-472MEB
1	L5	33Ω, 6A	Magnetic bead	SMD	Coilcraft	BLM31PG330SH1L
2	R2, R3	0Ω	Film resistor, 1%	1206	Yageo	RC0603FR-070RL
1	CN1	2.54mm	180° pin header, 2x5 pin, 2.54mm	DIP	Wurth	61201021621
10	VEMI, GND*5, VOUT1, VOUT2, VOUT3, LDO	2mm	2.0 golden pin	DIP	Custom (2)	
2	PG, VCC	1mm	1.0 golden pin	DIP	Custom (2)	
2	R1, R4	NS				
1	U1	MPQ70241FS	MPSafe™ ASIL-B, 18V, 4-channel PMIC with 3 bucks and 1 LDO, uprated current	QFN-15 (2.5mmx 3.5mm)	MPS	MPQ70241FSGRHE-0000AEC1

Note:

2) MPS custom-produces these pins. Contact an MPS FAE for more information.

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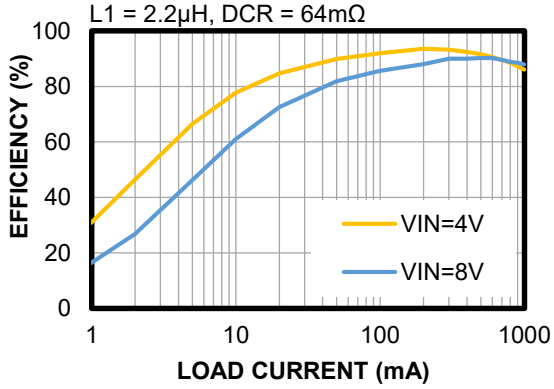
EVB TEST RESULTS

Performance curves and waveforms are tested on the evaluation board. V_{IN} = 8V, V_{OUT1} = 3V, V_{OUT2} = 1.8V, V_{OUT3} = 1.2V, V_{LDO} = 2.5V, L_1 = L_2 = 2.2µH, L_3 = 1µH, f_{SW1} = f_{SW2} = f_{SW3} = 2.2MHz, FCCM, T_A = 25°C, unless otherwise noted.

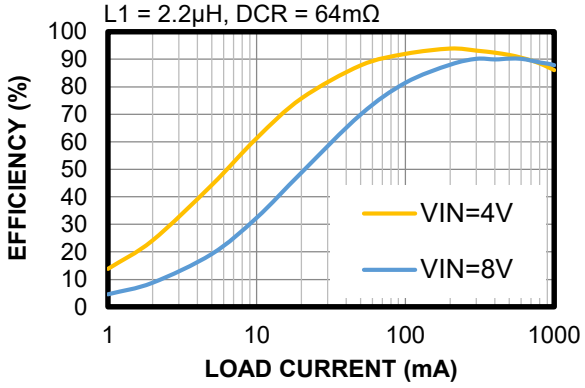
Efficiency vs. Load Current (Buck 1)

V_{OUT1} = 3V, f_{SW1} = 2.2MHz, DCM, other channels are disabled, L1 = 2.2µH, DCR = 64mΩ



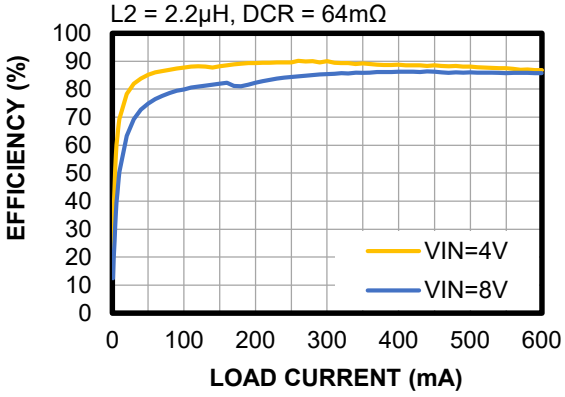
Efficiency vs. Load Current (Buck 1)

V_{OUT1} = 3V, f_{SW1} = 2.2MHz, FCCM, other channels are disabled, L1 = 2.2µH, DCR = 64mΩ



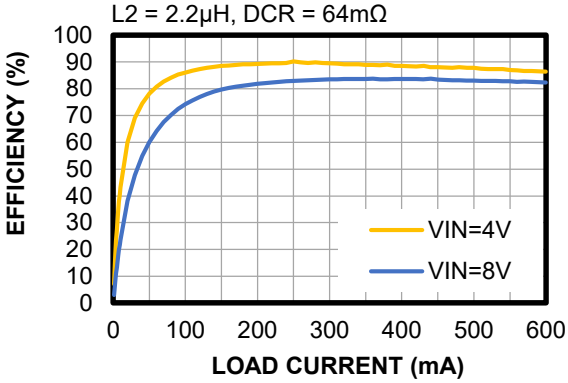
Efficiency vs. Load Current (Buck 2)

V_{OUT2} = 1.8V, f_{SW2} = 2.2MHz, DCM, other channels are disabled, L2 = 2.2µH, DCR = 64mΩ



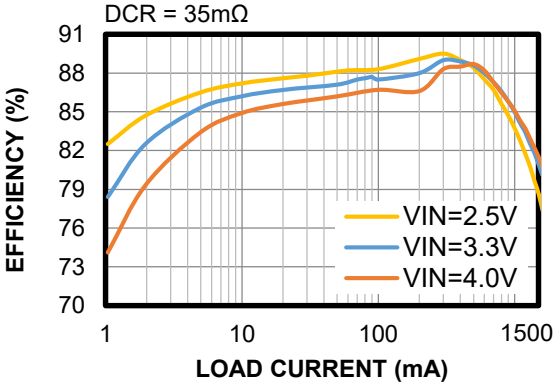
Efficiency vs. Load Current (Buck 2)

V_{OUT2} = 1.8V, f_{SW2} = 2.2MHz, FCCM, other channels are disabled, L2 = 2.2µH, DCR = 64mΩ



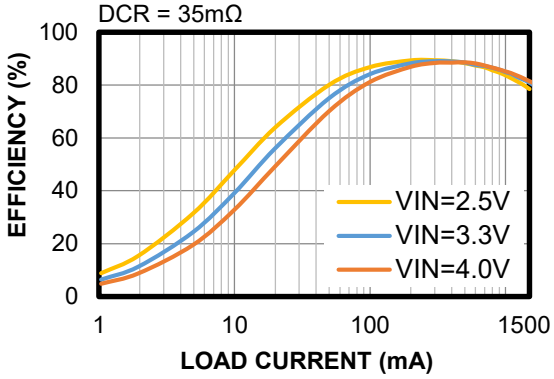
Efficiency vs. Load Current (Buck 3)

V_{OUT3} = 1.2V, f_{SW3} = 2.2MHz, DCM, LDO is disabled, L3 = 1µH, DCR = 35mΩ



Efficiency vs. Load Current (Buck 3)

V_{OUT3} = 1.2V, f_{SW3} = 2.2MHz, FCCM, LDO is disabled, L3 = 1µH, DCR = 35mΩ



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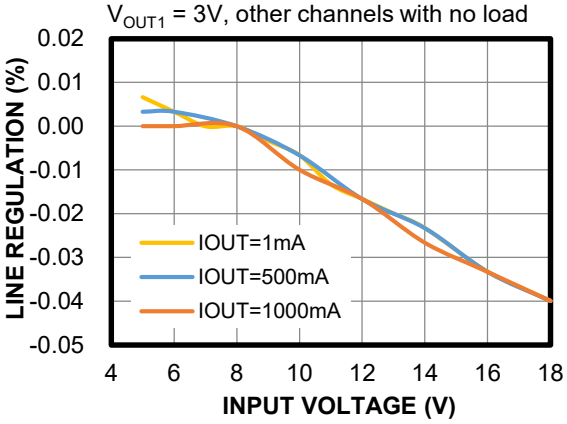
EVB TEST RESULTS *(continued)*

Performance curves and waveforms are tested on the evaluation board. V_{IN} = 8V, V_{OUT1} = 3V, V_{OUT2} = 1.8V, V_{OUT3} = 1.2V, V_{LDO} = 2.5V, L_1 = L_2 = 2.2µH, L_3 = 1µH, f_{SW1} = f_{SW2} = f_{SW3} = 2.2MHz, FCCM, T_A = 25°C, unless otherwise noted.

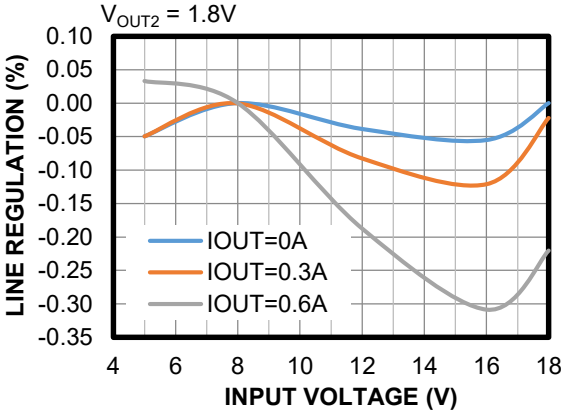
Line Regulation (Buck 1)

V_{OUT1} = 3V, other channels with no load



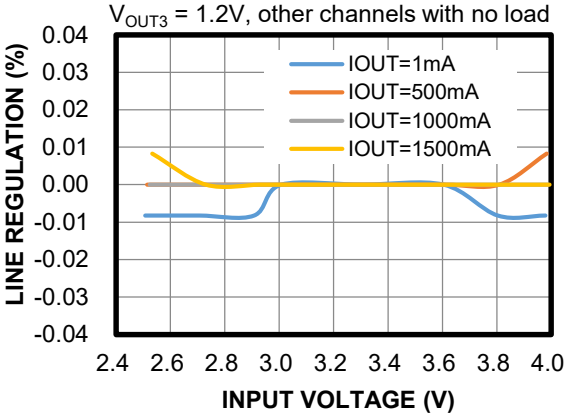
Line Regulation (Buck 2)

V_{OUT2} = 1.8V



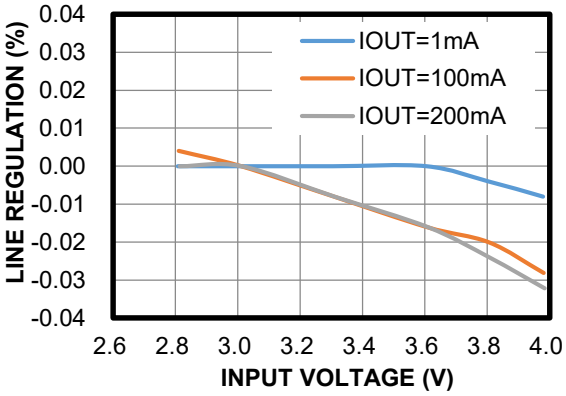
Line Regulation (Buck 3)

V_{OUT3} = 1.2V, other channels with no load



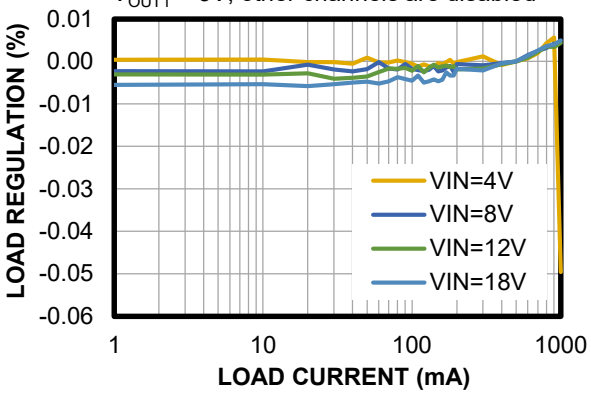
Line Regulation (LDO)

V_{LDOOUT} = 2.5V, other channels with no load



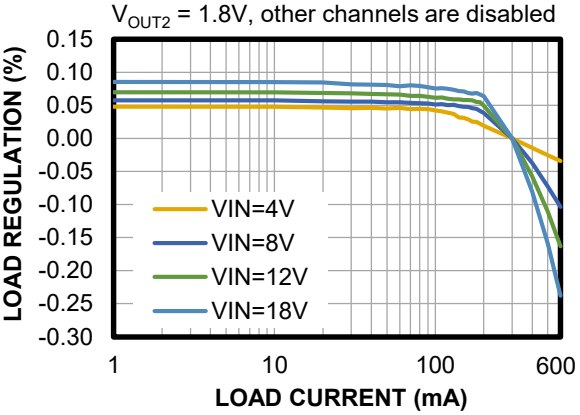
Load Regulation (Buck 1)

V_{OUT1} = 3V, other channels are disabled



Load Regulation (Buck 2)

V_{OUT2} = 1.8V, other channels are disabled



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EVB TEST RESULTS *(continued)*

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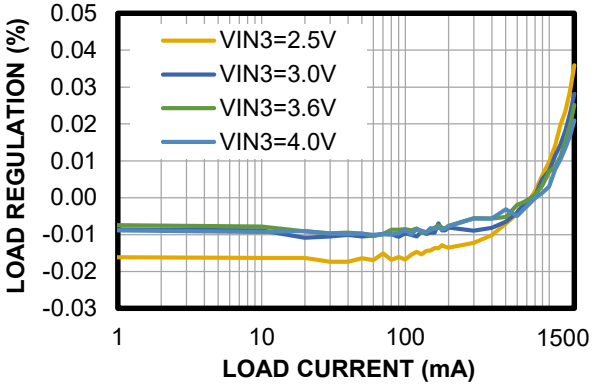
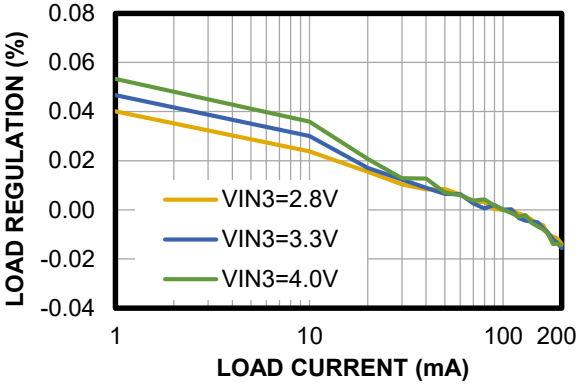
Load Regulation (Buck 3)

V_{IN} = 8V, buck 1 is enabled, other channels are disabled



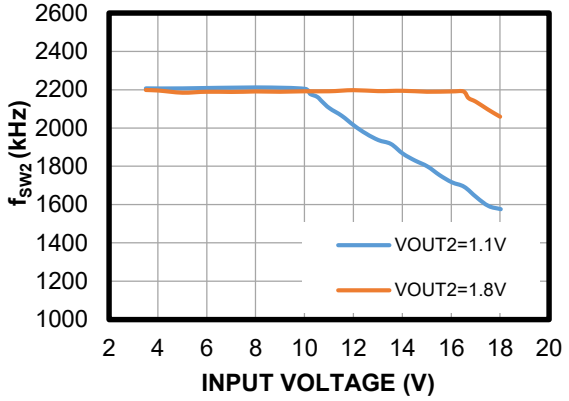
Load Regulation (LDO)

V_{IN} = 8V, buck 1 is enabled, other channels are disabled



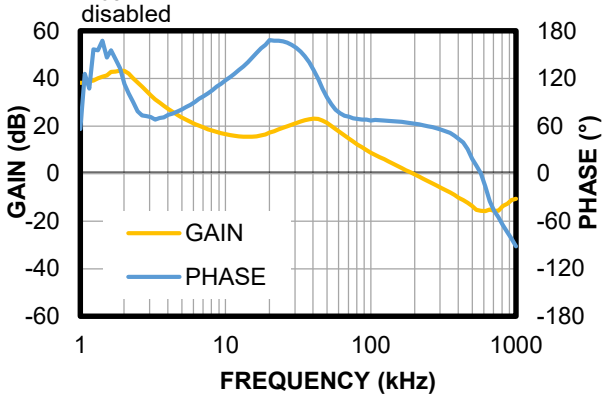
f_{SW2} vs. V_{IN}

FCCM, FREQUENCY[0] = 0



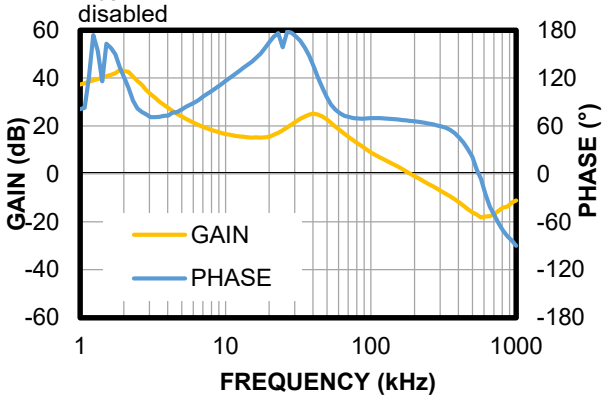
Bode Plot vs. Frequency (Buck 1)

V_{IN} = 8V, V_{OUT1} = 3V, I_{OUT1} = 1A, FCCM, f_{SW1} = 2.2MHz, L1 = 2.2µH, C_{OUT1} = 2 x 4.7µF, other channels are disabled



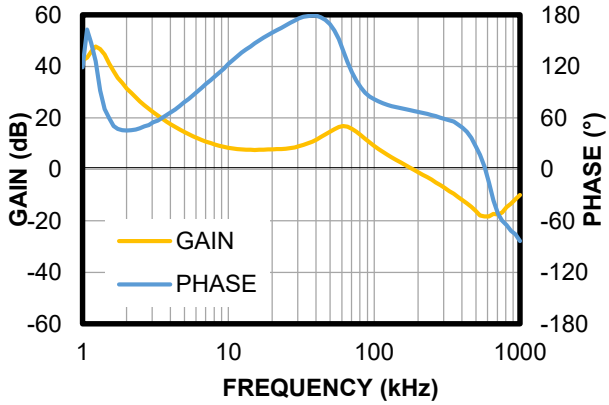
Bode Plot vs. Frequency (Buck 1)

V_{IN} = 8V, V_{OUT1} = 3V, I_{OUT1} = 1A, FCCM, f_{SW1} = 3.3MHz, L1 = 2.2µH, C_{OUT1} = 2 x 4.7µF, other channels are disabled



Bode Plot vs. Frequency (Buck 2)

V_{IN} = 8V, V_{OUT2} = 1.8V, I_{OUT2} = 0.6A, FCCM, f_{SW2} = 2.2MHz, L2 = 2.2µH, C_{OUT2} = 4.7µF, other channels are disabled



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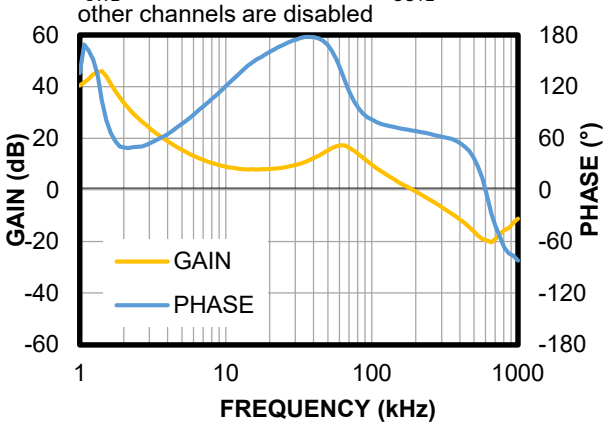
EVB TEST RESULTS *(continued)*

Performance curves and waveforms are tested on the evaluation board. V_{IN} = 8V, V_{OUT1} = 3V, V_{OUT2} = 1.8V, V_{OUT3} = 1.2V, V_{LDO} = 2.5V, L_1 = L_2 = 2.2µH, L_3 = 1µH, f_{SW1} = f_{SW2} = f_{SW3} = 2.2MHz, FCCM, T_A = 25°C, unless otherwise noted.

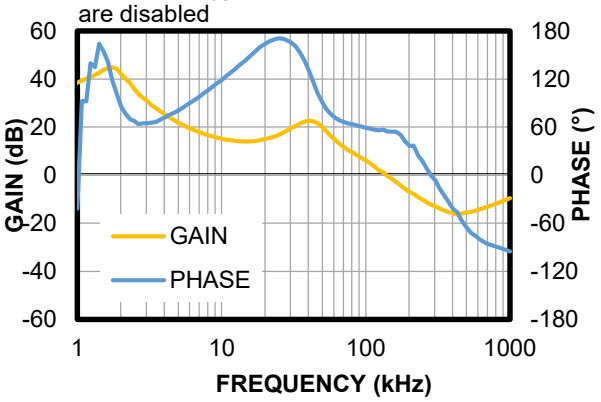
Bode Plot vs. Frequency (Buck 2)

V_{IN} = 8V, V_{OUT2} = 1.8V, I_{OUT2} = 0.6A, FCCM, f_{SW2} = 3.3MHz, L2 = 2.2µH, C_{OUT2} = 4.7µF, other channels are disabled



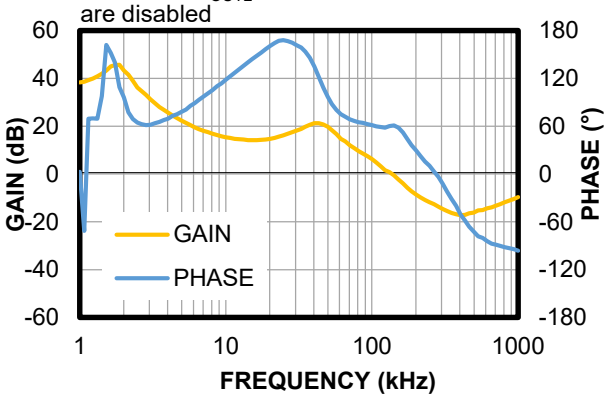
Bode Plot vs. Frequency (Buck 3)

V_{IN} = 8V, V_{OUT1} = 3V, V_{OUT3} = 1.2V, I_{OUT3} = 1.5A, FCCM, f_{SW3} = 2.2MHz, L3 = 1µH, C_{OUT2} = 2 x 10µF, other channels are disabled



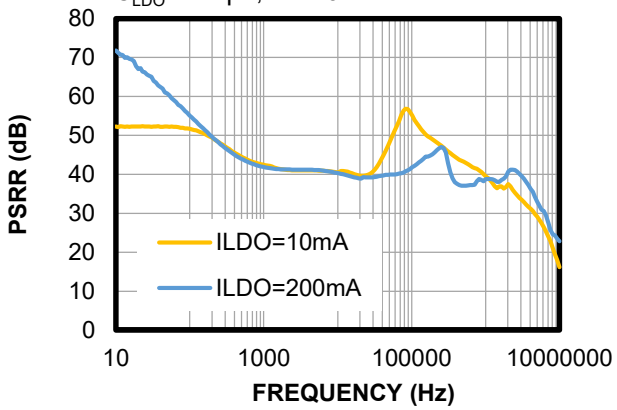
Bode Plot vs. Frequency (Buck 3)

V_{IN} = 8V, V_{OUT1} = 3V, V_{OUT3} = 1.2V, I_{OUT3} = 1.5A, FCCM, f_{SW3} = 3.3MHz, L3 = 1µH, C_{OUT2} = 2 x 10µF, other channels are disabled



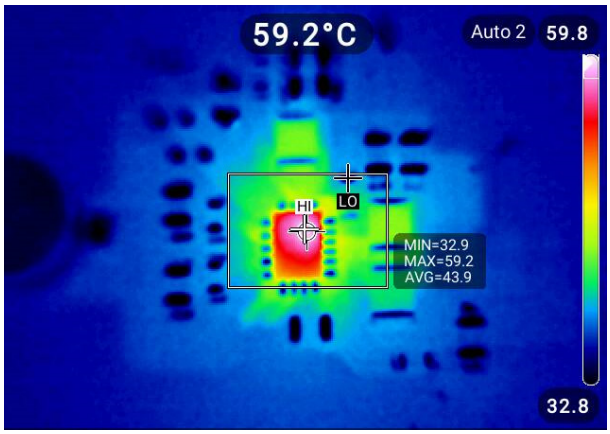
PSRR vs. Frequncy

V_{IN3} = 4V, V_{LDO} = 2.5V, C_{IN3} = 100nF, C_{LDO} = 4.7µF, buck 3 is disabled



Thermal Performance

I_{OUT1} = 0A, I_{OUT2} = 600mA, I_{OUT3} = 1.5A, I_{LDO} = 200mA, no forced airflow, T_A = 25°C



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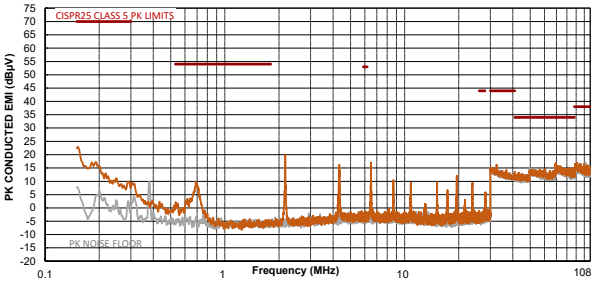
EVB TEST RESULTS *(continued)*

Performance curves and waveforms are tested on the evaluation board. V_{IN} = 12V, V_{OUT1} = 3V, V_{OUT2} = 1.8V, V_{OUT3} = 1.2V, V_{LDO} = 2.5V, L_1 = L_2 = 2.2µH, L_3 = 1µH, f_{SW1} = f_{SW2} = f_{SW3} = 2.2MHz, FCCM, T_A = 25°C, unless otherwise noted. (3)

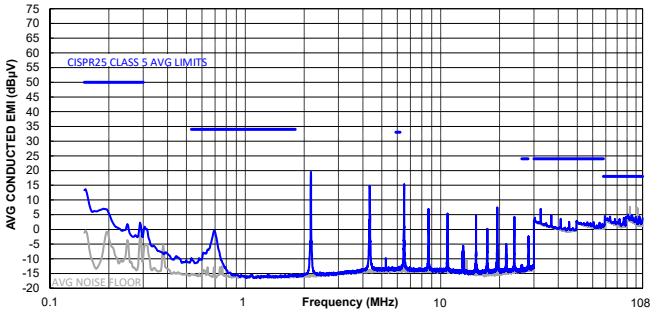
CISPR 25 Class 5 Peak Conducted Emissions

150kHz to 108MHz



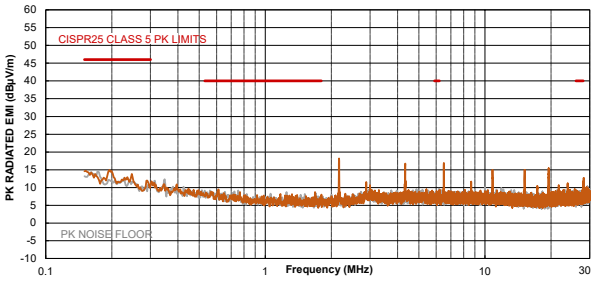
CISPR 25 Class 5 Average Conducted Emissions

150kHz to 108MHz



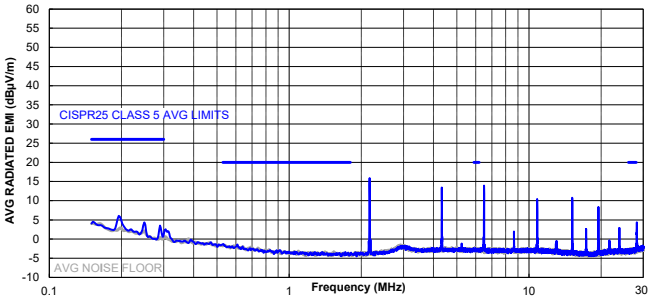
CISPR 25 Class 5 Peak Radiated Emissions

150kHz to 30MHz



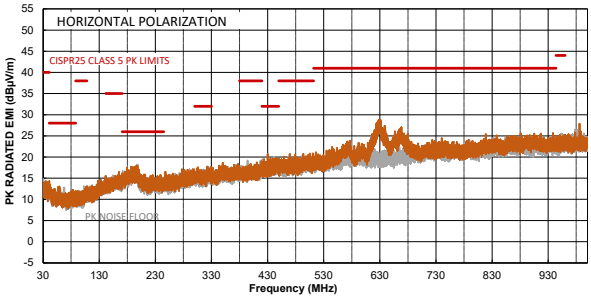
CISPR 25 Class 5 Average Radiated Emissions

150kHz to 30MHz



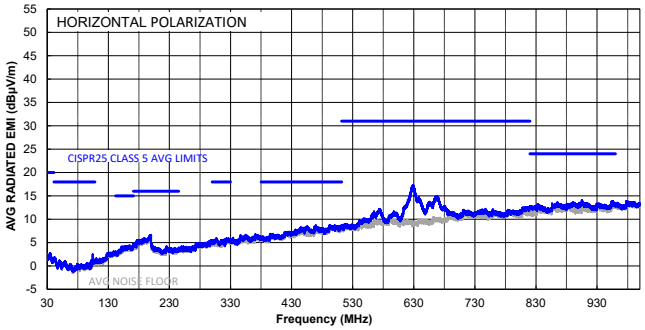
CISPR 25 Class 5 Peak Radiated Emissions

Horizontal, 30MHz to 1GHz



CISPR 25 Class 5 Average Radiated Emissions

Horizontal, 30MHz to 1GHz



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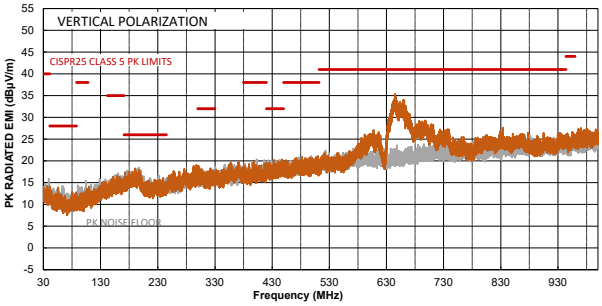
EVB TEST RESULTS *(continued)*

Performance curves and waveforms are tested on the evaluation board. V_{IN} = 12V, V_{OUT1} = 3V, V_{OUT2} = 1.8V, V_{OUT3} = 1.2V, V_{LDO} = 2.5V, L_1 = L_2 = 2.2µH, L_3 = 1µH, f_{SW1} = f_{SW2} = f_{SW3} = 2.2MHz, FCCM, T_A = 25°C, unless otherwise noted. (3)

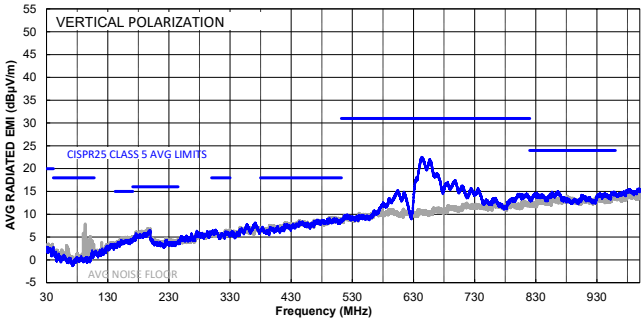
CISPR 25 Class 5 Peak Radiated Emissions

Vertical, 30MHz to 1GHz



CISPR 25 Class 5 Average Radiated Emissions

Vertical, 30MHz to 1GHz



Note:

3) All EMC test results are based on the evaluation board schematic with EMI filters (see Figure 3 on page 7).

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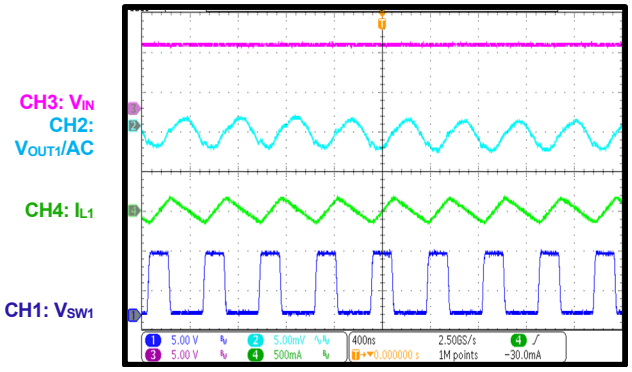
EVB TEST RESULTS *(continued)*

Performance curves and waveforms are tested on the evaluation board. V_{IN} = 8V, V_{OUT1} = 3V, V_{OUT2} = 1.8V, V_{OUT3} = 1.2V, V_{LDO} = 2.5V, L_1 = L_2 = 2.2µH, L_3 = 1µH, f_{SW1} = f_{SW2} = f_{SW3} = 2.2MHz, FCCM, T_A = 25°C, unless otherwise noted.

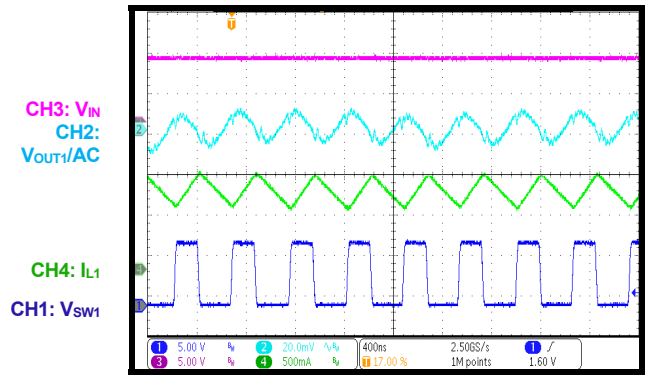
Steady State (Buck 1)

I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{LDO} = 0A



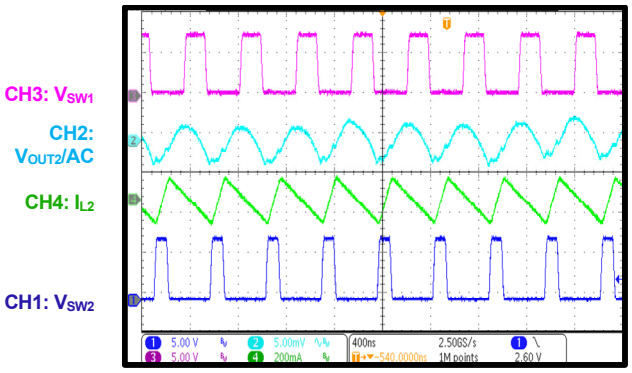
Steady State (Buck 1)

I_{OUT1} = 0A, I_{OUT2} = 600mA, I_{OUT3} = 1.5A, I_{LDO} = 200mA



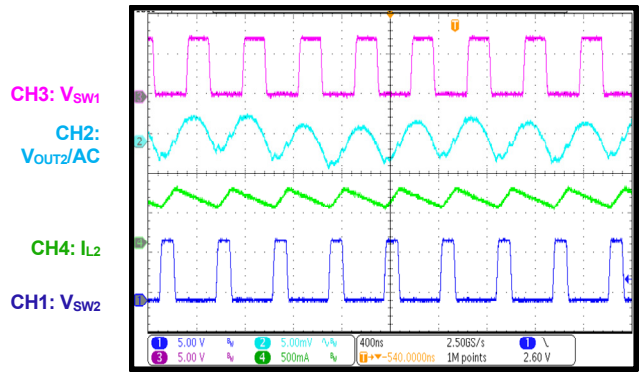
Steady State (Buck 2)

I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{LDO} = 0A



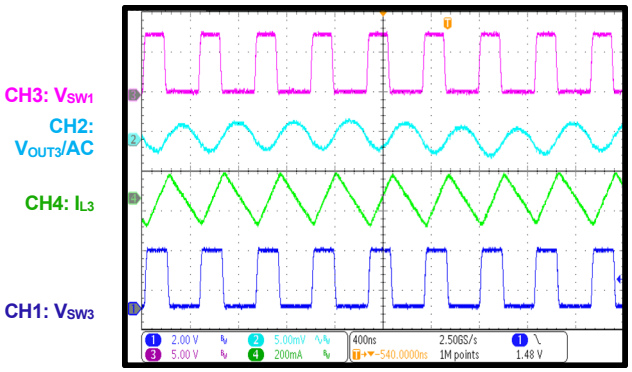
Steady State (Buck 2)

I_{OUT1} = 0A, I_{OUT2} = 600mA, I_{OUT3} = 1.5A, I_{LDO} = 200mA



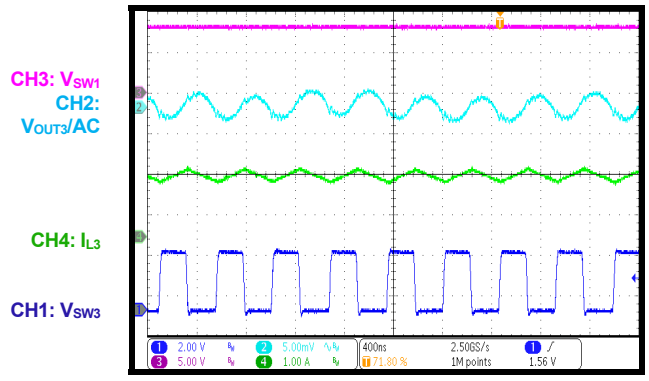
Steady State (Buck 3)

I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{LDO} = 0A



Steady State (Buck 3)

I_{OUT1} = 0A, I_{OUT2} = 600mA, I_{OUT3} = 1.5A, I_{LDO} = 200mA



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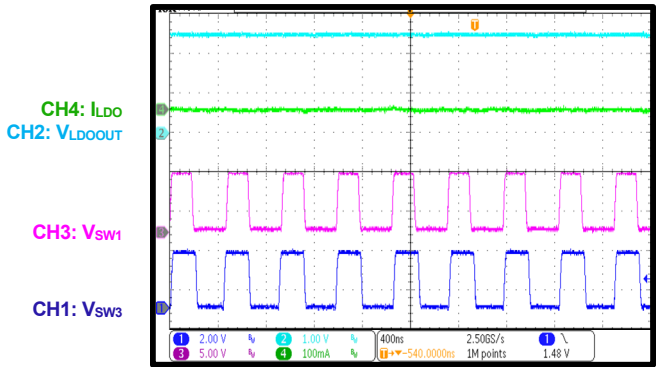
EVB TEST RESULTS *(continued)*

Performance curves and waveforms are tested on the evaluation board. V_{IN} = 8V, V_{OUT1} = 3V, V_{OUT2} = 1.8V, V_{OUT3} = 1.2V, V_{LDO} = 2.5V, L_1 = L_2 = 2.2µH, L_3 = 1µH, f_{SW1} = f_{SW2} = f_{SW3} = 2.2MHz, FCCM, T_A = 25°C, unless otherwise noted.

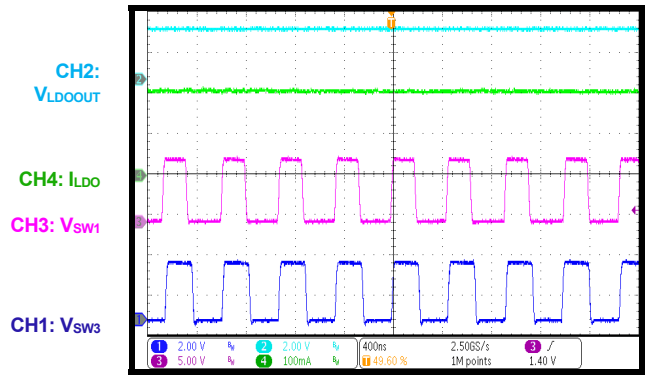
Steady State (LDO)

I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{LDO} = 0A



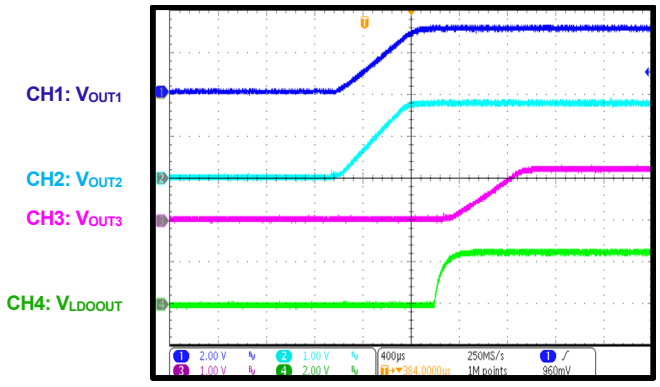
Steady State (LDO)

I_{OUT1} = 0A, I_{OUT2} = 600mA, I_{OUT3} = 1.5A, I_{LDO} = 200mA



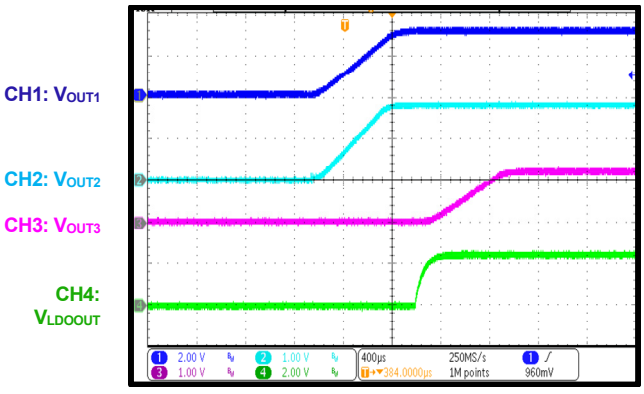
Start-Up through VIN (Start-Up Sequence)

I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{LDO} = 0A



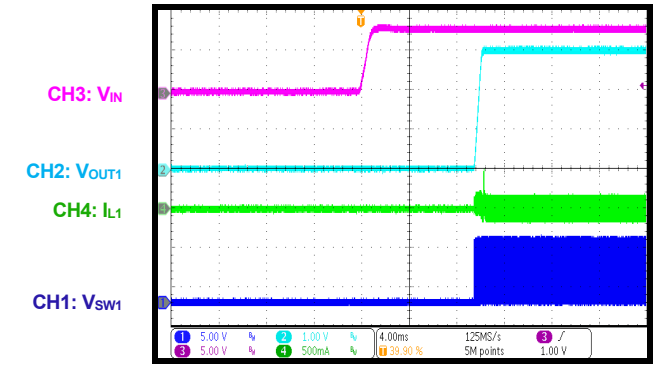
Start-Up through VIN (Start-Up Sequence)

I_{OUT1} = 0A, I_{OUT2} = 600mA, I_{OUT3} = 1.5A, I_{LDO} = 200mA



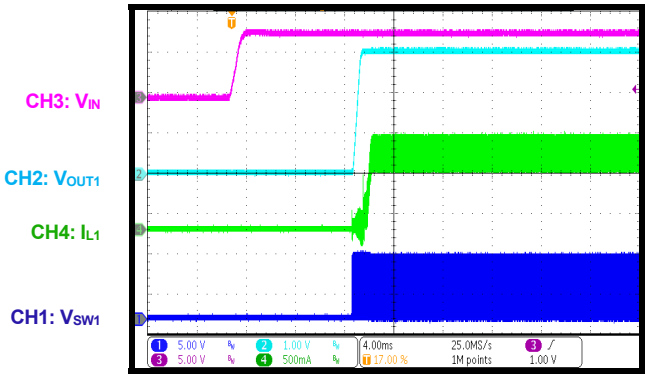
Start-Up through VIN (Buck 1)

I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{LDO} = 0A



Start-Up through VIN (Buck 1)

I_{OUT1} = 0A, I_{OUT2} = 600mA, I_{OUT3} = 1.5A, I_{LDO} = 200mA



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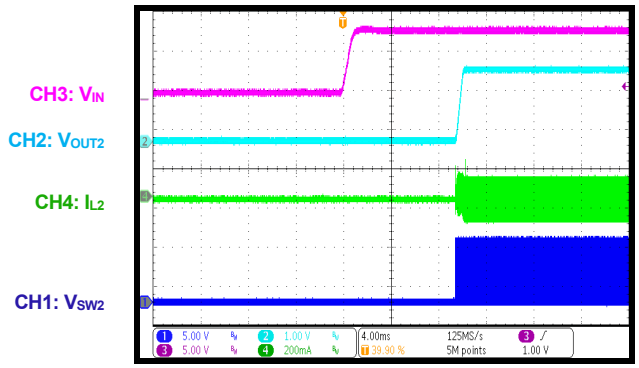
EVB TEST RESULTS *(continued)*

Performance curves and waveforms are tested on the evaluation board. V_{IN} = 8V, V_{OUT1} = 3V, V_{OUT2} = 1.8V, V_{OUT3} = 1.2V, V_{LDO} = 2.5V, L_1 = L_2 = 2.2µH, L_3 = 1µH, f_{SW1} = f_{SW2} = f_{SW3} = 2.2MHz, FCCM, T_A = 25°C, unless otherwise noted.

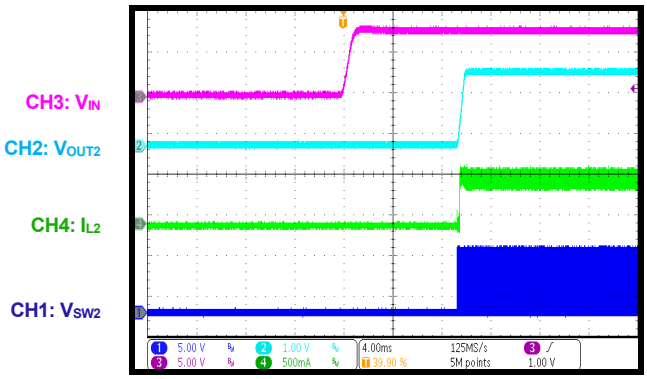
Start-Up through VIN (Buck 2)

I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{LDO} = 0A



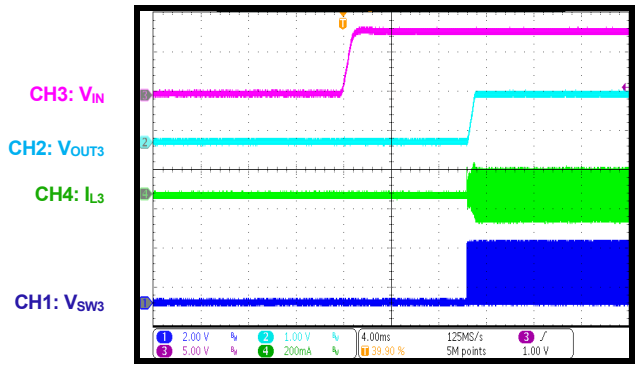
Start-Up through VIN (Buck 2)

I_{OUT1} = 0A, I_{OUT2} = 600mA, I_{OUT3} = 1.5A, I_{LDO} = 200mA



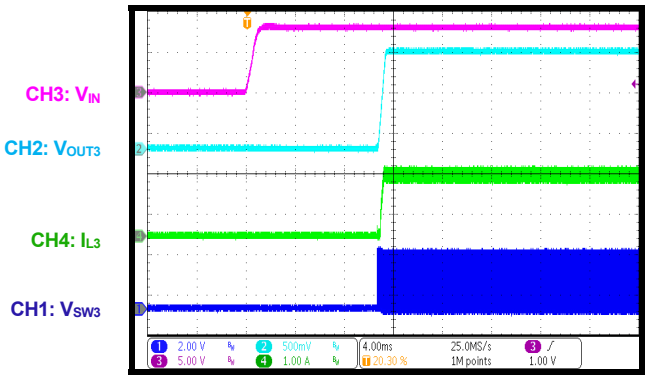
Start-Up through VIN (Buck 3)

I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{LDO} = 0A



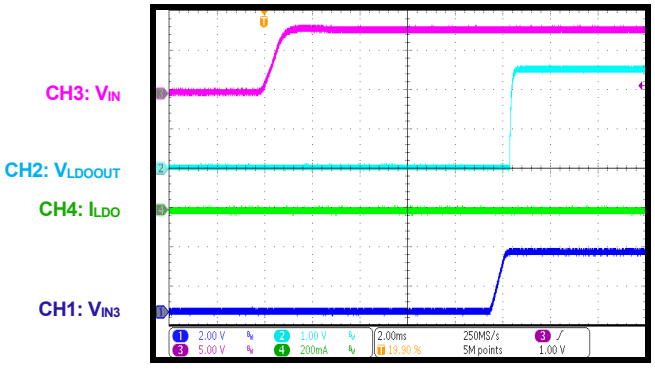
Start-Up through VIN (Buck 3)

I_{OUT1} = 0A, I_{OUT2} = 600mA, I_{OUT3} = 1.5A, I_{LDO} = 200mA



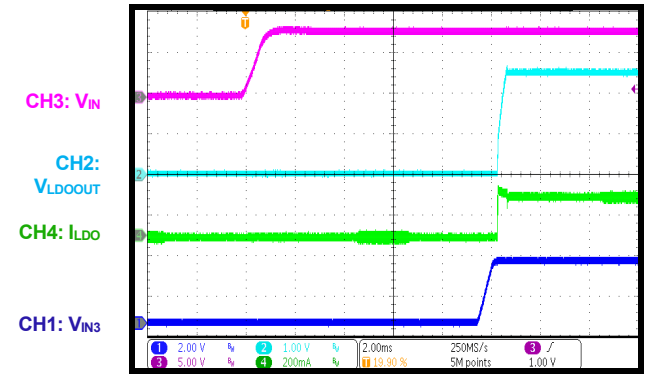
Start-Up through VIN (LDO)

I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{LDO} = 0A



Start-Up through VIN (LDO)

I_{OUT1} = 0A, I_{OUT2} = 600mA, I_{OUT3} = 1.5A, I_{LDO} = 200mA



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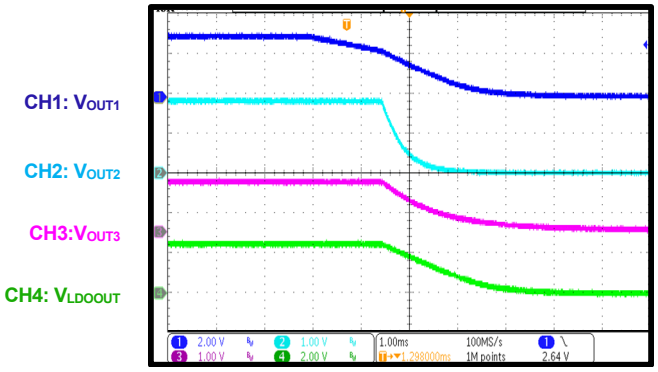
EVB TEST RESULTS *(continued)*

Performance curves and waveforms are tested on the evaluation board. V_{IN} = 8V, V_{OUT1} = 3V, V_{OUT2} = 1.8V, V_{OUT3} = 1.2V, V_{LDO} = 2.5V, L_1 = L_2 = 2.2µH, L_3 = 1µH, f_{SW1} = f_{SW2} = f_{SW3} = 2.2MHz, FCCM, T_A = 25°C, unless otherwise noted.

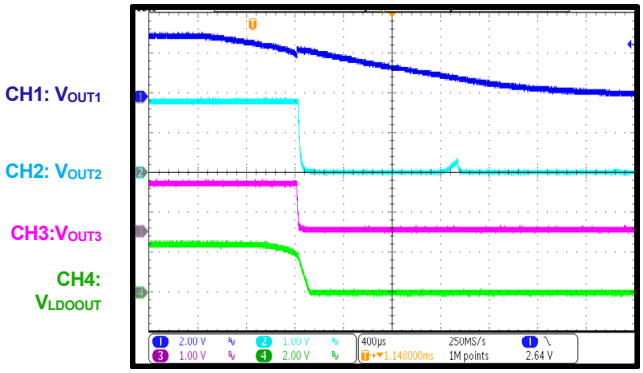
Shutdown through VIN

I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{LDO} = 0A



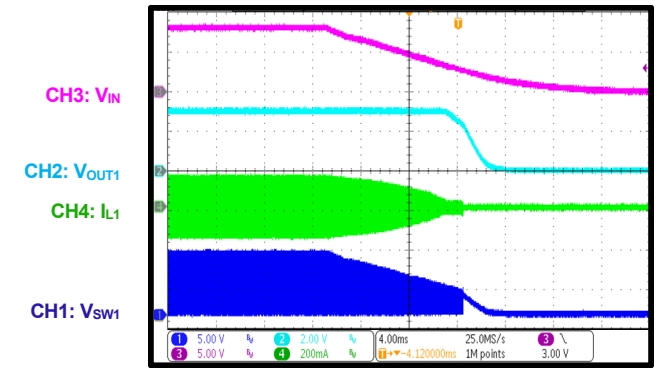
Shutdown through VIN

I_{OUT1} = 0A, I_{OUT2} = 600mA, I_{OUT3} = 1.5A, I_{LDO} = 200mA



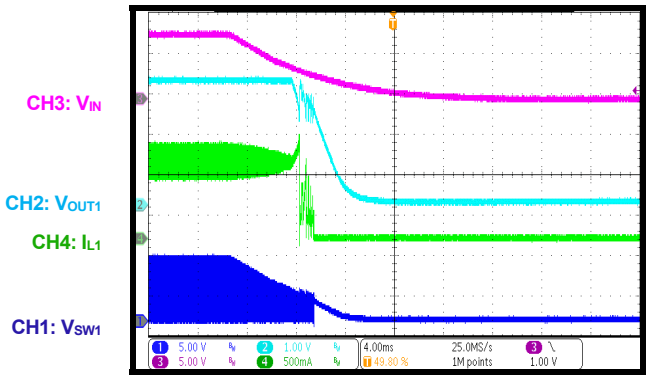
Shutdown through VIN (Buck 1)

I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{LDO} = 0A



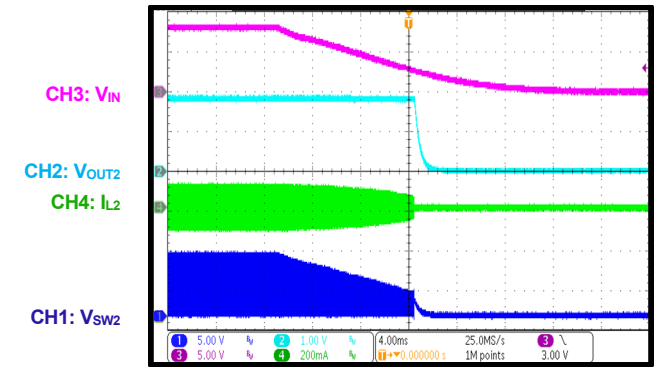
Shutdown through VIN (Buck 1)

I_{OUT1} = 0A, I_{OUT2} = 600mA, I_{OUT3} = 1.5A, I_{LDO} = 200mA



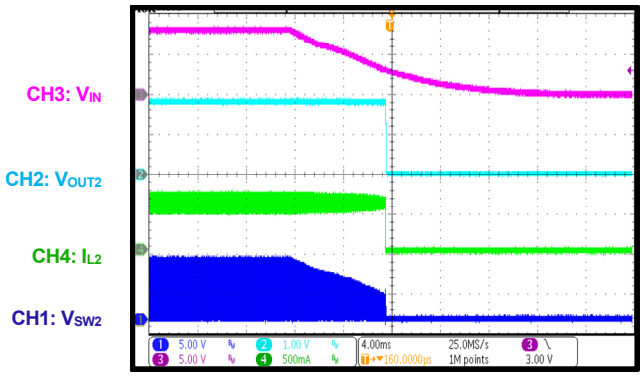
Shutdown through VIN (Buck 2)

I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{LDO} = 0A



Shutdown through VIN (Buck 2)

I_{OUT1} = 0A, I_{OUT2} = 600mA, I_{OUT3} = 1.5A, I_{LDO} = 200mA



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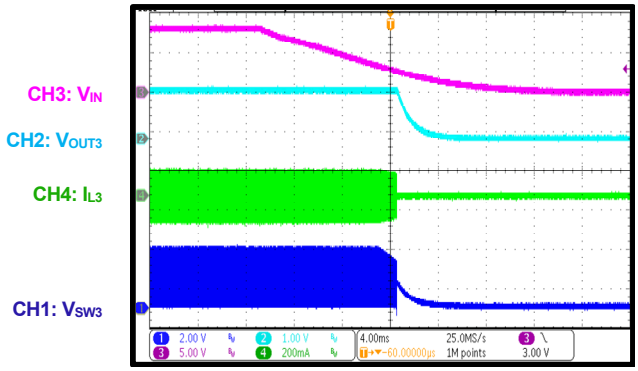
EVB TEST RESULTS *(continued)*

Performance curves and waveforms are tested on the evaluation board. V_{IN} = 8V, V_{OUT1} = 3V, V_{OUT2} = 1.8V, V_{OUT3} = 1.2V, V_{LDO} = 2.5V, L_1 = L_2 = 2.2µH, L_3 = 1µH, f_{SW1} = f_{SW2} = f_{SW3} = 2.2MHz, FCCM, T_A = 25°C, unless otherwise noted.

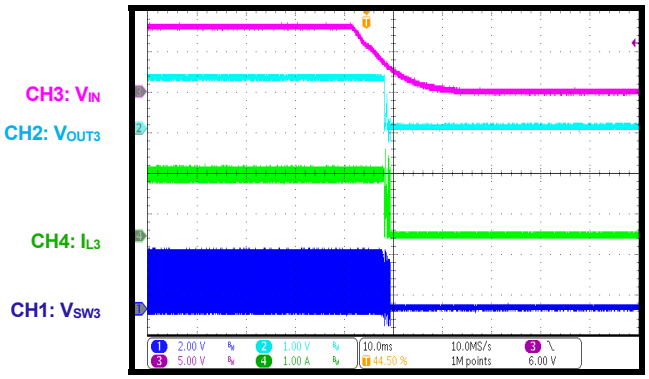
Shutdown through VIN (Buck 3)

I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{LDO} = 0A



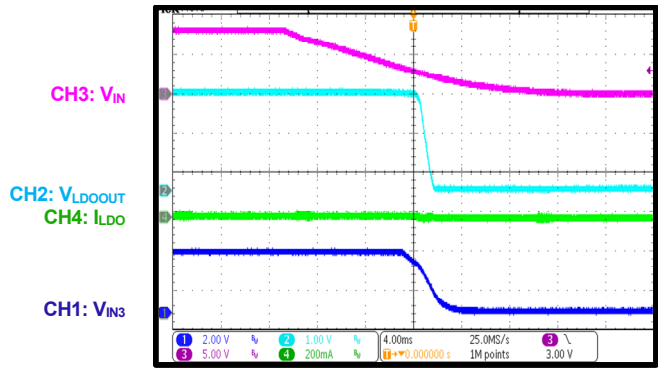
Shutdown through VIN (Buck 3)

I_{OUT1} = 0A, I_{OUT2} = 600mA, I_{OUT3} = 1.5A, I_{LDO} = 200mA



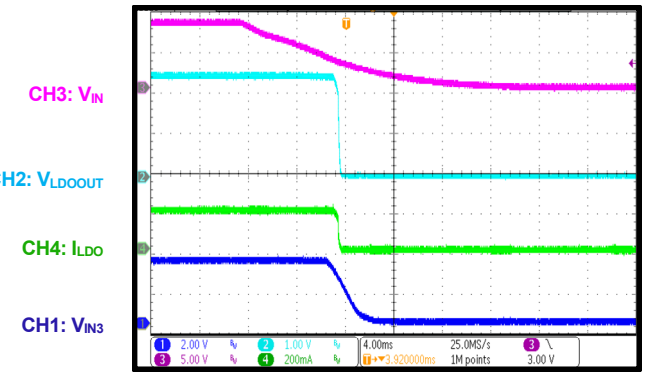
Shutdown through VIN (LDO)

I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{LDO} = 0A

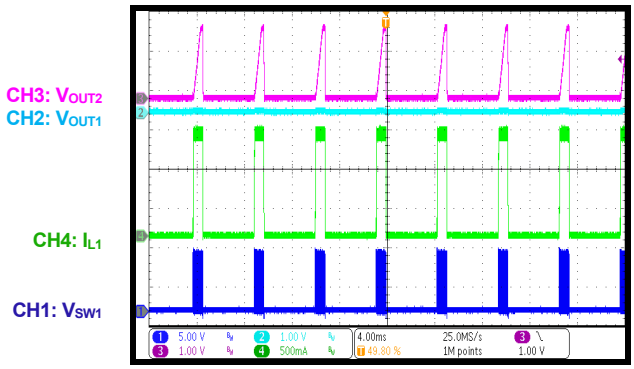


Shutdown through VIN (LDO)

I_{OUT1} = 0A, I_{OUT2} = 600mA, I_{OUT3} = 1.5A, I_{LDO} = 200mA

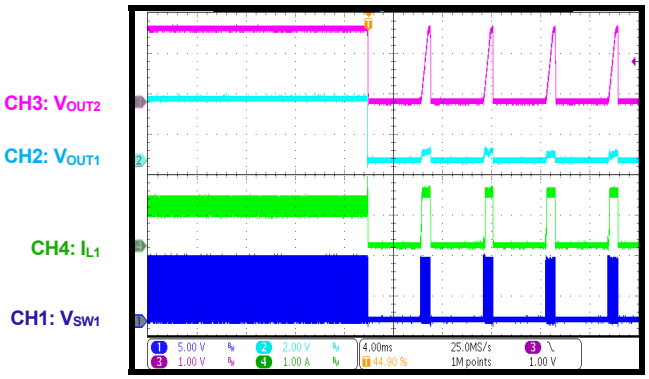


SCP Steady State (Buck 1)



SCP Entry (Buck 1)

I_{OUT1} = 0A, I_{OUT2} = 600mA, I_{OUT3} = 1.5A, I_{LDO} = 200mA



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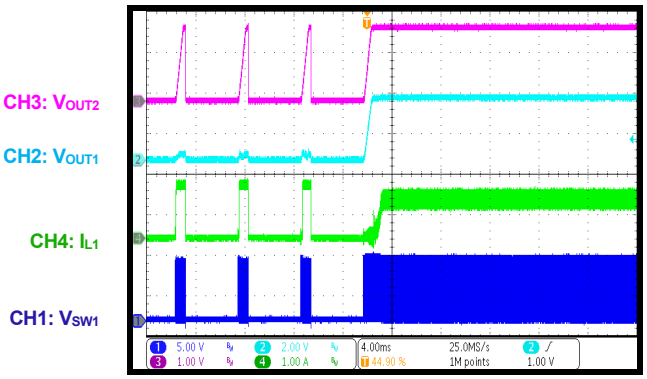
EVB TEST RESULTS *(continued)*

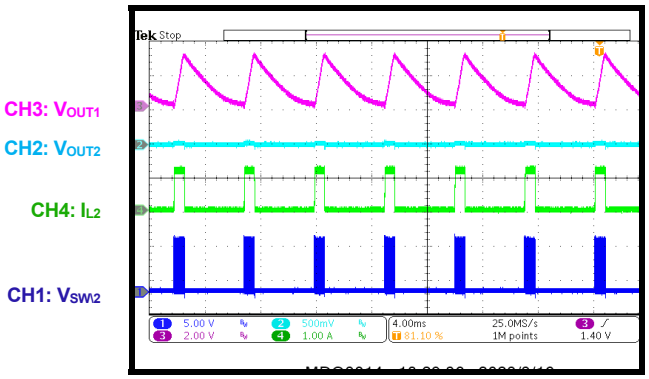
Performance curves and waveforms are tested on the evaluation board. V_{IN} = 8V, V_{OUT1} = 3V, V_{OUT2} = 1.8V, V_{OUT3} = 1.2V, V_{LDO} = 2.5V, L_1 = L_2 = 2.2µH, L_3 = 1µH, f_{SW1} = f_{SW2} = f_{SW3} = 2.2MHz, FCCM, T_A = 25°C, unless otherwise noted.

SCP Recovery (Buck 1)

I_{OUT1} = 0A, I_{OUT2} = 600mA, I_{OUT3} = 1.5A, I_{LDO} = 200mA

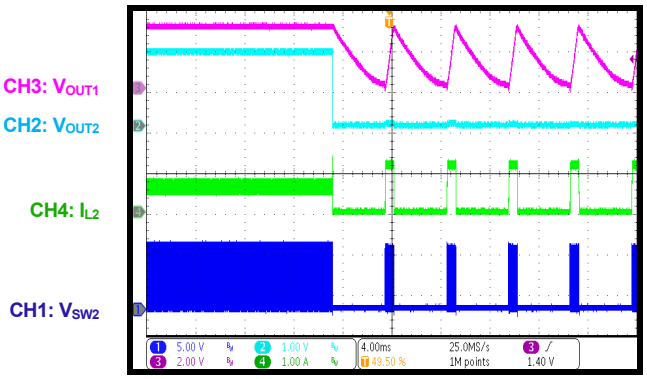


SCP Steady State (Buck 2)



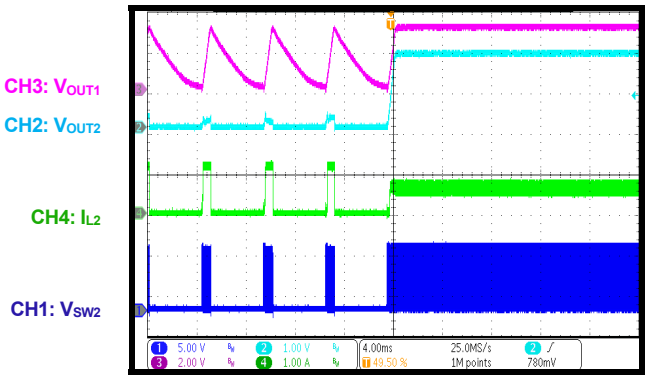
SCP Entry (Buck 2)

I_{OUT1} = 0A, I_{OUT2} = 600mA, I_{OUT3} = 1.5A, I_{LDO} = 200mA

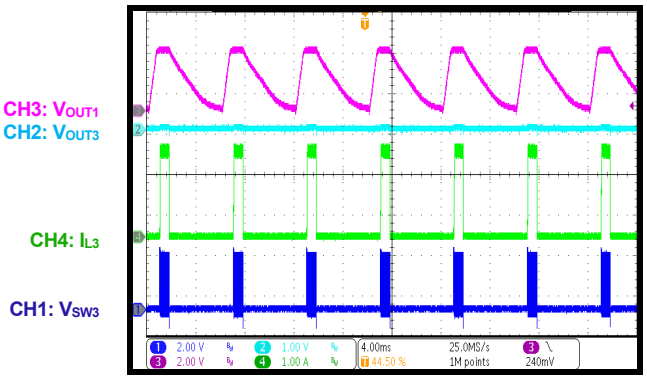


SCP Recovery (Buck 2)

I_{OUT1} = 0A, I_{OUT2} = 600mA, I_{OUT3} = 1.5A, I_{LDO} = 200mA

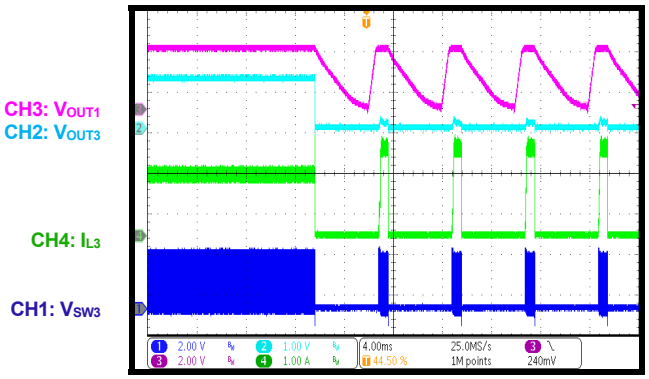


SCP Steady State (Buck 3)



SCP Entry (Buck 3)

I_{OUT1} = 0A, I_{OUT2} = 600mA, I_{OUT3} = 1.5A, I_{LDO} = 200mA



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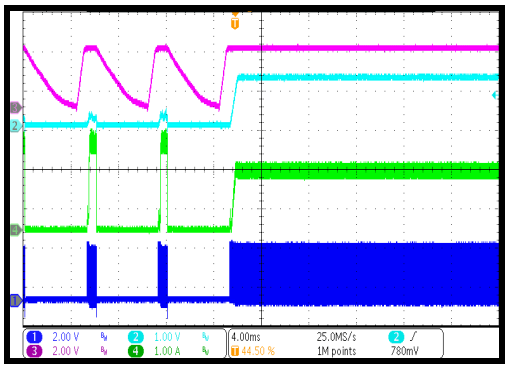
EVB TEST RESULTS *(continued)*

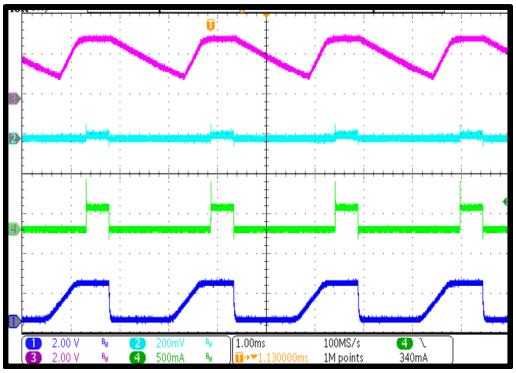
Performance curves and waveforms are tested on the evaluation board. V_{IN} = 8V, V_{OUT1} = 3V, V_{OUT2} = 1.8V, V_{OUT3} = 1.2V, V_{LDO} = 2.5V, L_1 = L_2 = 2.2µH, L_3 = 1µH, f_{SW1} = f_{SW2} = f_{SW3} = 2.2MHz, FCCM, T_A = 25°C, unless otherwise noted.

SCP Recovery (Buck 3)

I_{OUT1} = 0A, I_{OUT2} = 600mA, I_{OUT3} = 1.5A, I_{LDO} = 200mA

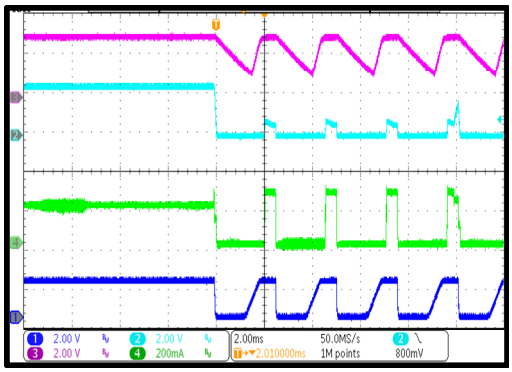


SCP Steady State (LDO)



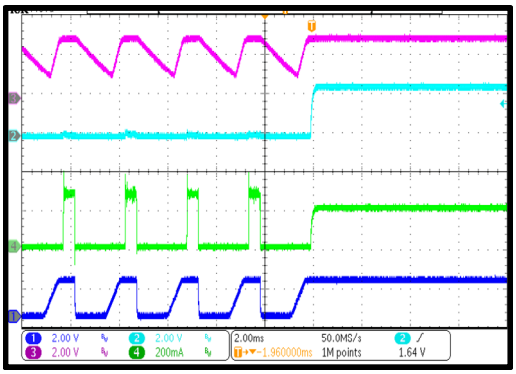
SCP Entry (LDO)

I_{OUT1} = 0A, I_{OUT2} = 600mA, I_{OUT3} = 1.5A, I_{LDO} = 200mA



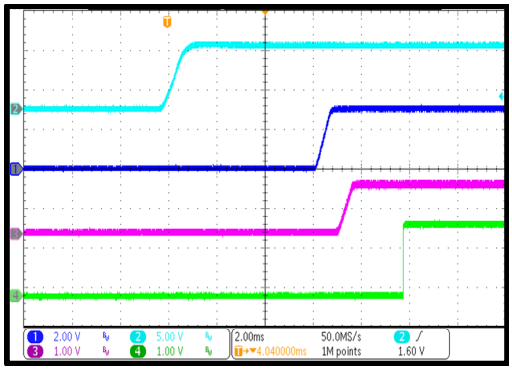
SCP Recovery (LDO)

I_{OUT1} = 0A, I_{OUT2} = 600mA, I_{OUT3} = 1.5A, I_{LDO} = 200mA



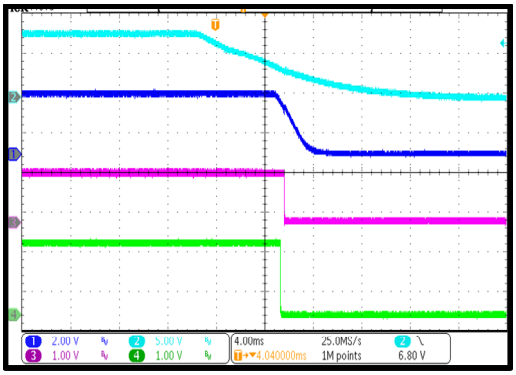
PG in Start-Up through VIN

I_{OUT1} = 0A, I_{OUT2} = 600mA, I_{OUT3} = 1.5A, I_{LDO} = 200mA



PG in Shutdown through VIN

I_{OUT1} = 0A, I_{OUT2} = 600mA, I_{OUT3} = 1.5A, I_{LDO} = 200mA



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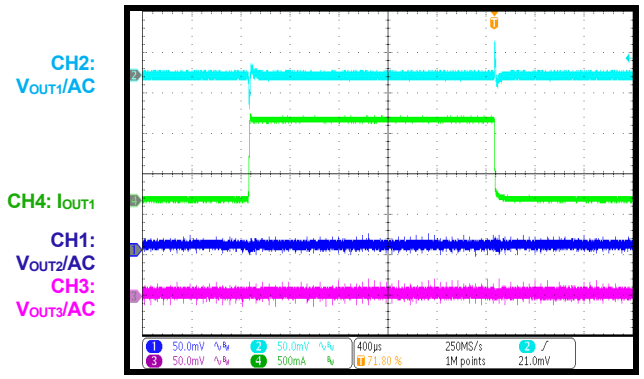
EVB TEST RESULTS *(continued)*

Performance curves and waveforms are tested on the evaluation board. V_{IN} = 8V, V_{OUT1} = 3V, V_{OUT2} = 1.8V, V_{OUT3} = 1.2V, V_{LDO} = 2.5V, L_1 = L_2 = 2.2µH, L_3 = 1µH, f_{SW1} = f_{SW2} = f_{SW3} = 2.2MHz, FCCM, T_A = 25°C, unless otherwise noted.

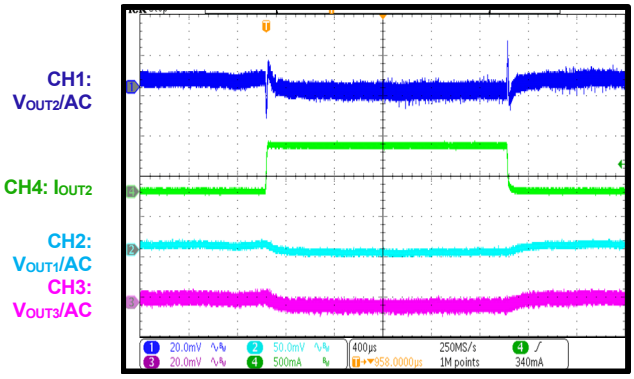
Load Transient (Buck 1)

I_{OUT1} = 0A to 1000mA, I_{OUT2} = I_{OUT3} = I_{LDO} = 0A



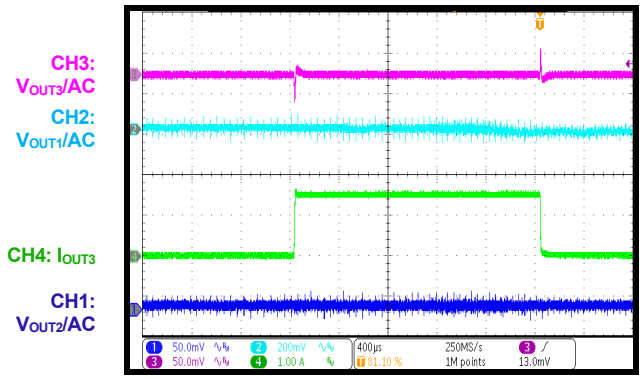
Load Transient (Buck 2)

I_{OUT1} = 0A, I_{OUT2} = 0A to 600mA, I_{OUT3} = 1.5A, I_{LDO} = 200mA



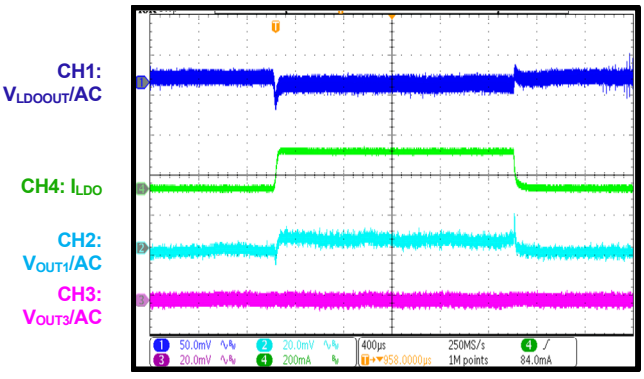
Load Transient (Buck 3)

I_{OUT1} = 0A, I_{OUT2} = 600mA, I_{OUT3} = 0A to 1.5A, I_{LDO} = 200mA



Load Transient (LDO)

I_{OUT1} = 0A, I_{OUT2} = 600mA, I_{OUT3} = 1.5A, I_{LDO} = 0 to 200mA



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PCB LAYOUT (4)

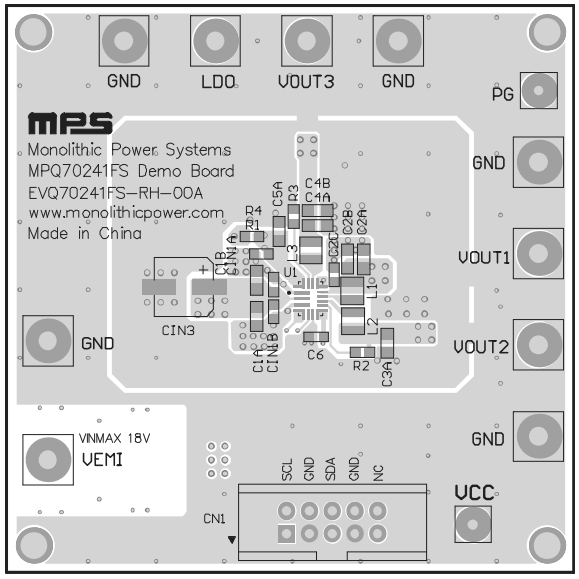

Figure 4: Top Silk and Top Layer

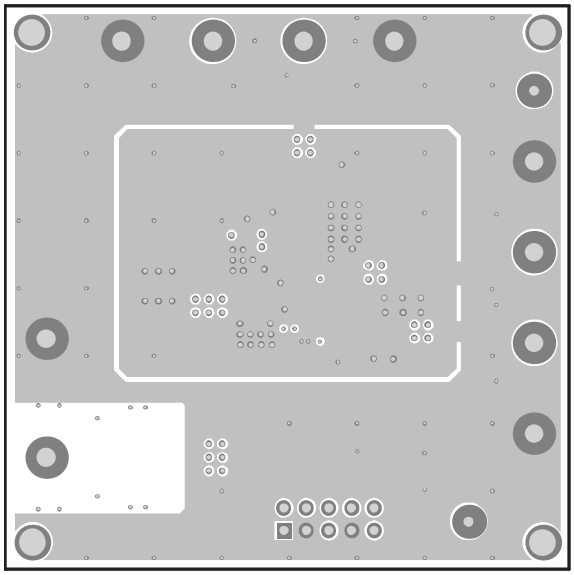

Figure 5: Mid-Layer 1

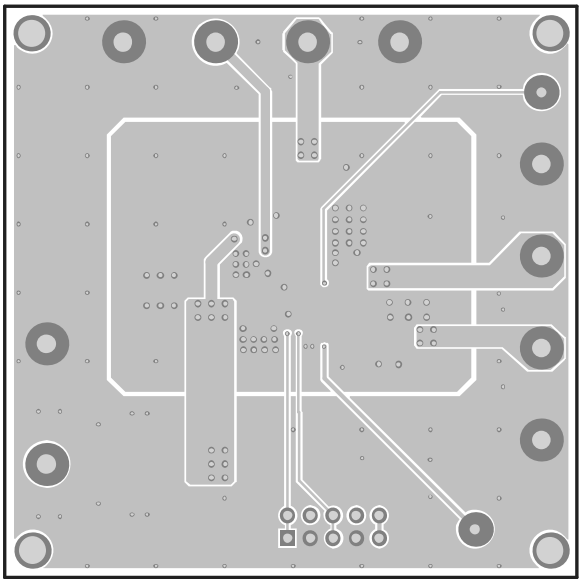

Figure 6: Mid-Layer 2

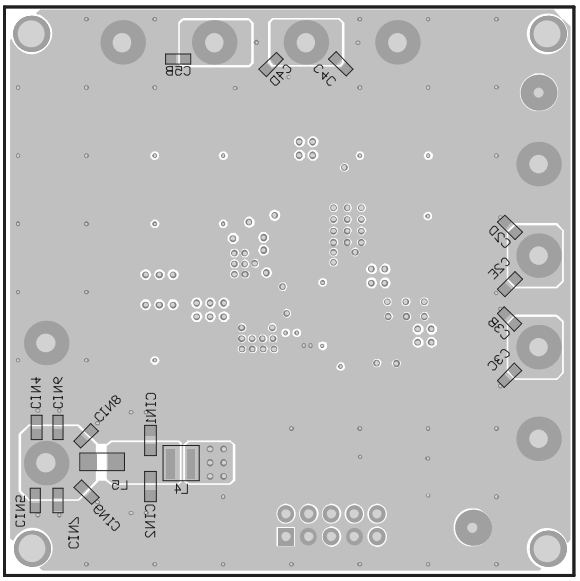

Figure 7: Bottom Layer and Bottom Silk

Note:

4) The EVQ70241FS-RH-00A is a 4-layer PCB with a 2oz copper thickness PCB (6.35cmx6.35cm).

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REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	11/6/2024	Initial Release	-

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