



# EVQ18913-D-00A

## 30V, 0.5A, High-Frequency Transformer Driver, AEC-Q100 Qualified Evaluation Board

### DESCRIPTION

The EVQ18913-D-00A is an evaluation board designed to demonstrate the capabilities of the MPQ18913, a high-frequency, half-bridge transformer driver that is ideal for primary-side switchers used in isolated power supplies.

The MPQ18913 features an adjustable switching frequency ( $f_{sw}$ ) with a wide range, which is particularly useful in resonant topologies such as LLC converters. It also offers input over-voltage protection (OVP),

over-current protection (OCP), and fault indication. Soft start (SS) is built in to control the inrush current.

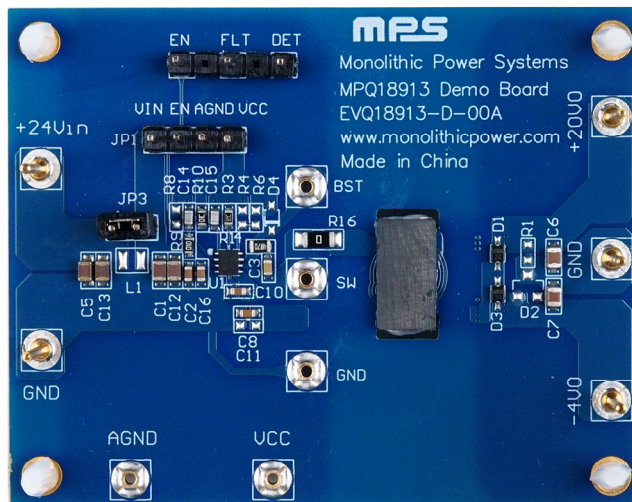
The MPQ18913 is available in a QFN-10 (2mmx2.5mm) package with wettable flanks, and is available in AEC-Q100 Grade 1. It is recommended to read the MPQ18913 datasheet prior to making any changes to the EVQ18913-D-00A.

### PERFORMANCE SUMMARY

Specifications are at  $T_A = 25^\circ\text{C}$ , unless otherwise noted.

Parameters	Conditions	Value
Input voltage ( $V_{IN}$ ) range		10.8V to 26.4V
Output voltage ( $V_{OUT}$ )		9V to 30V
Maximum output current ( $I_{OUT}$ )	$V_{IN} = 10.8\text{V to } 26.4\text{V}$	0.25A
Typical efficiency	$V_{IN} = 24\text{V}, V_{OUT} = 23.6\text{V}, I_{OUT} = 0.25\text{A}$	84.9%
Peak efficiency	$V_{IN} = 24\text{V}, V_{OUT} = 25\text{V}, I_{OUT} = 0.125\text{A}$	87.5%
Switching frequency ( $f_{sw}$ )		1.33MHz

### EVALUATION BOARD



LxWxH (6.5cmx5cmx1cm)

Board Number	MPS IC Number
EVQ18913-D-00A	MPQ18913GRPE-AEC1

## QUICK START GUIDE

1. Preset the power supply ( $V_{IN}$ ) between 10.8V and 26.4V, then turn off the power supply (see Figure 1).
2. Connect the power supply terminals to:
  - a. Positive (+):  $+24V_{IN}$
  - b. Negative (-): GND
3. Connect the load terminals to:
  - a. Positive (+):  $+20V_{OUT}$
  - b. Negative (-):  $-4V_{OUT}$
4. After making the connections, turn on the power supply. The default switching frequency ( $f_{sw}$ ) is 1.3MHz.
5. To use the enable function, remove R9 and apply a digital input to the EN pin. Drive EN above 2V to turn the converter on; drive EN below 0.8V to turn it off.
6. To use the SYNC function, remove R9 and change R3 based on the required clock scale factor. Then apply a clock signal to the EN pin and turn on the power supply.

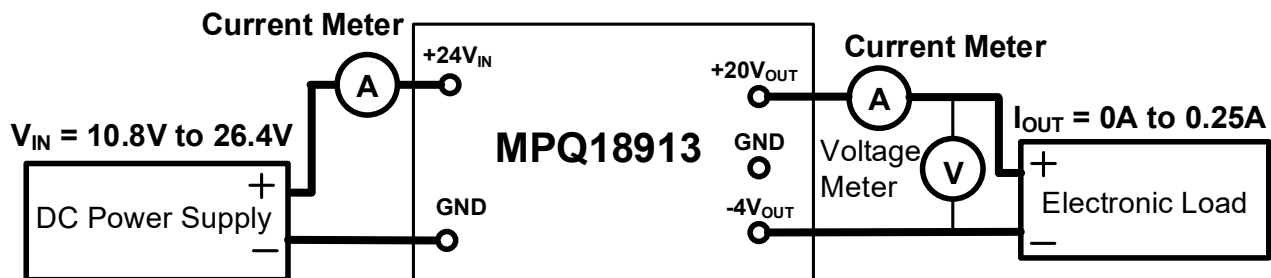


Figure 1: Measurement Equipment Set-Up

## EVALUATION BOARD SCHEMATIC

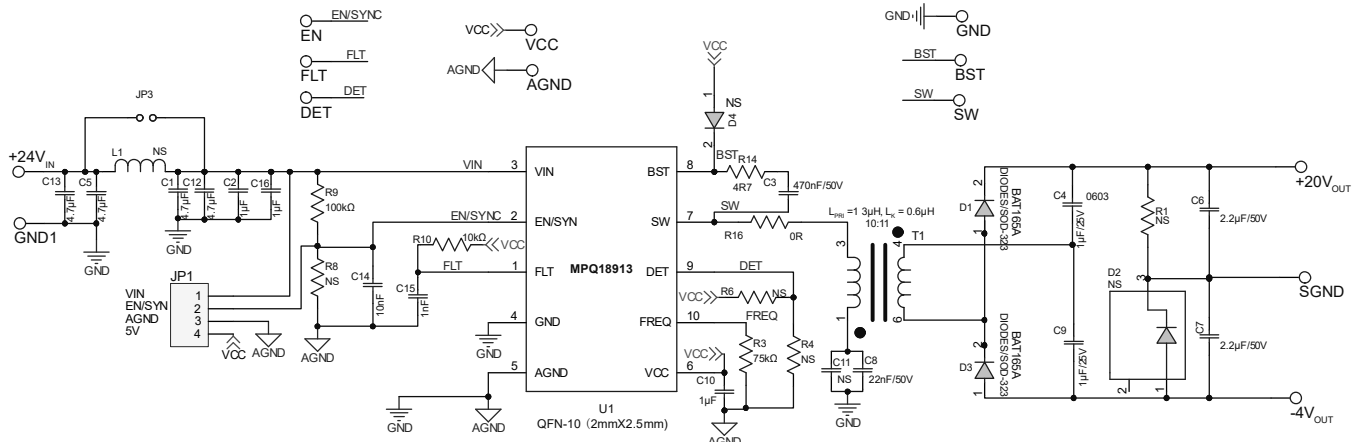


Figure 2: Evaluation Board Schematic

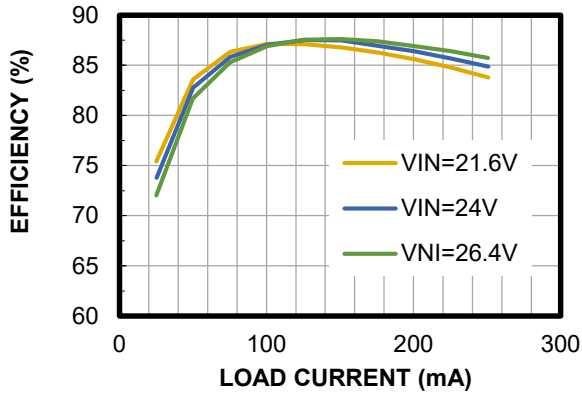
**EVQ18913-D-01A BILL OF MATERIALS**

Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
4	C1, C5, C12, C13	4.7 $\mu$ F	Ceramic capacitor, 50V, X7S	0805	Murata	GRM21BC71H475KE11L
3	C2, C10, C16	1 $\mu$ F	Ceramic capacitor, 50V, X5R	0603	Murata	GRM188R61H105KAAL
1	C3	470nF	Ceramic capacitor, 50V, X7R	0603	TDK	C1608X7R1H474K
2	C4, C9	1 $\mu$ F	Ceramic capacitor, 25V, X7R	0603	TDK	C1608X7R1E105K
2	C6, C7	2.2 $\mu$ F	Ceramic capacitor, 50V, X7R	0805	TDK	C2012X7R1H225K
1	C8	22nF	Ceramic capacitor, 50V, X7R	0603	TDK	C1608X7R1H223K
1	C11	NS				
1	C14	10nF	Ceramic capacitor, 50V, C0G	0603	Murata	GRM1885C1H103JA01D
1	C15	1nF	Ceramic capacitor, 50V, C0G	0603	TDK	GRM1885C1H102JA01D
2	D1, D3	40V	Schottky diode, 0.75A	SOD-323	NXP	BAT165A
1	D2	NS				
1	D4	NS				
1	L1	NS				
4	R1, R4, R6, R8	NS				
1	R3	75k $\Omega$	Film resistor, 1%	0603	Yageo	RC0603FR-0793K1L
1	R9	100K $\Omega$	Film resistor, 1%	0603	Yageo	RC0603FR-07100KL
1	R10	10k $\Omega$	Film resistor, 1%	0603	Yageo	RC0603FR-0710KL
1	R14	4R7	Film resistor, 1%	0805	Yageo	RC0805FR-074R7L
1	R16	0 $\Omega$	Film resistor, 1%	1206	Yageo	RC1206FR-070RL
1	T1	13 $\mu$ H	Ferrite core	ER11/3.9	TDK	PC50ER11/3.9-Z
5	+24V <sub>IN</sub> , GND, +20V <sub>OUT</sub> , GND, -4V <sub>OUT</sub>	1mm	Connector			
5	AGND, VCC, BST, GND, SW	NS				
1	JP1, EN, FLT, DET	2.54mm	Pin header	TH	Any	
1	JP3	2.54mm	Pin header with jumper cap	TH	Any	
1	U1	MPQ18913	30V, 0.5A high-frequency transformer driver	QFN-10 (2mmx2.5mm)	MPS	MPQ18913GRPE-AEC1

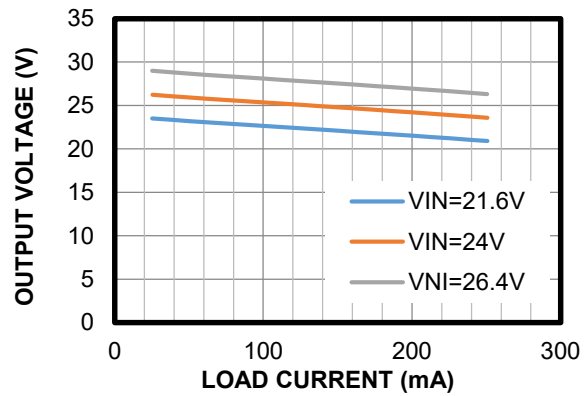
## EVB TEST RESULTS

Performance curves and waveforms are tested on the evaluation board.  $V_{IN} = 24V$ ,  $V_{OUT} = 24V$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

### Efficiency vs. Load Current

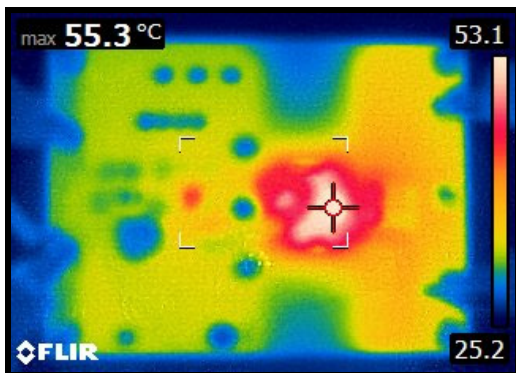


### Load Regulation



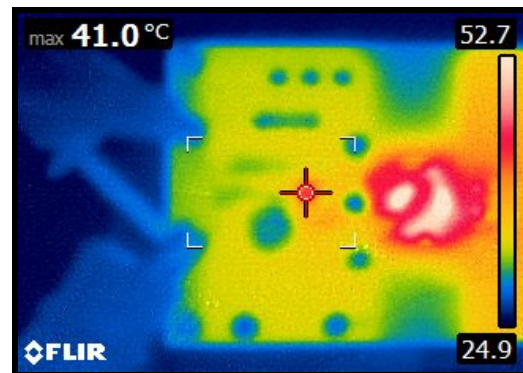
### Thermal Performance

$V_{IN} = 24V$ ,  $I_{OUT} = 0.25A$ , no forced airflow,  
 $T_{CASE} = 55.3^\circ C$ , transformer



### Thermal Performance

$V_{IN} = 24V$ ,  $I_{OUT} = 0.25A$ , no forced airflow,  
 $T_{CASE} = 41^\circ C$ , MPQ18913



## EVB TEST RESULTS (continued)

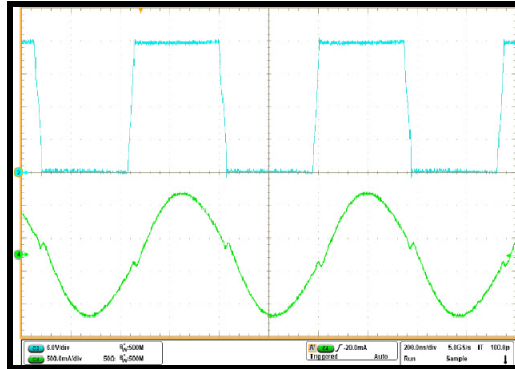
Performance curves and waveforms are tested on the evaluation board.  $V_{IN} = 24V$ ,  $I_{OUT} = 0.25A$ ,  $T_A = 25^{\circ}C$ , unless otherwise noted.

### Steady State

$I_{OUT} = 0.25A$

CH2: SW  
6V/div.

CH4:  $I_{PRI}$   
0.5A/div.



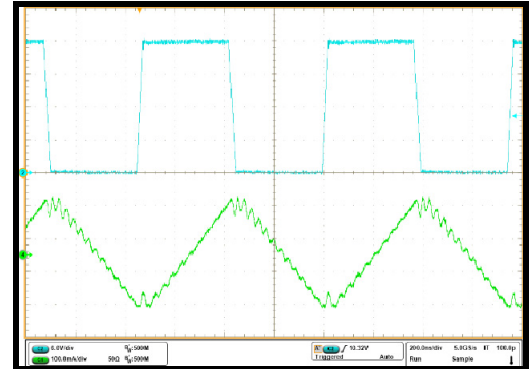
200ns/div.

### Steady State

$I_{OUT} = 0A$

CH2: SW  
6V/div.

CH4:  $I_{PRI}$   
0.1A/div.



200ns/div.

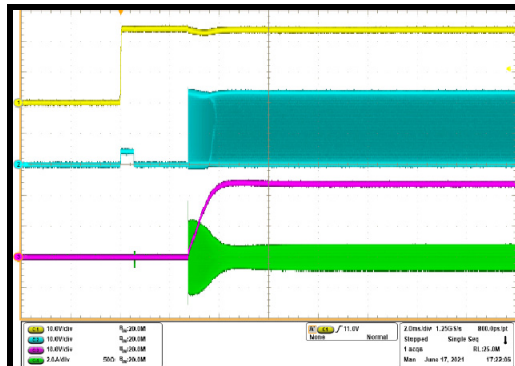
### Start-Up through VIN

CH1:  $V_{IN}$   
10V/div.

CH2: SW  
10V/div.

CH3:  $V_{OUT}$   
10V/div.

CH4:  $I_{PRI}$   
2A/div.



2ms/div.

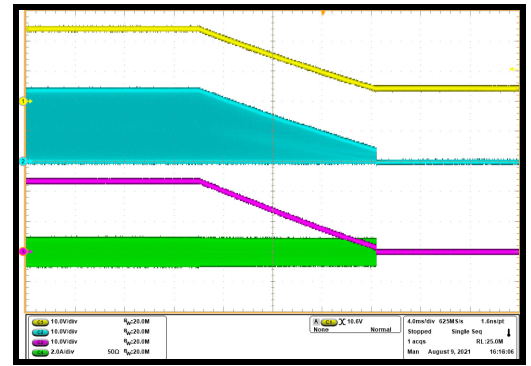
### Shutdown through VIN

CH1:  $V_{IN}$   
10V/div.

CH2: SW  
10V/div.

CH3:  $V_{OUT}$   
10V/div.

CH4:  $I_{PRI}$   
2A/div.



5ms/div.

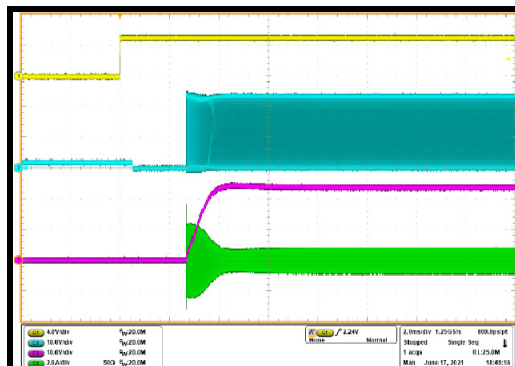
### Start-Up through EN

CH1: EN  
5V/div.

CH2: SW  
10V/div.

CH3:  $V_{OUT}$   
10V/div.

CH4:  $I_{PRI}$   
2A/div.



2ms/div.

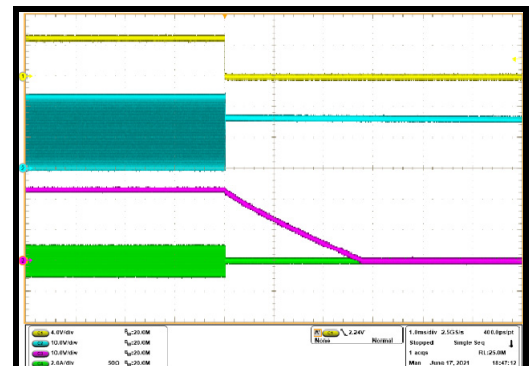
### Shutdown through EN

CH1: EN  
5V/div.

CH2: SW  
10V/div.

CH3:  $V_{OUT}$   
10V/div.

CH4:  $I_{PRI}$   
2A/div.

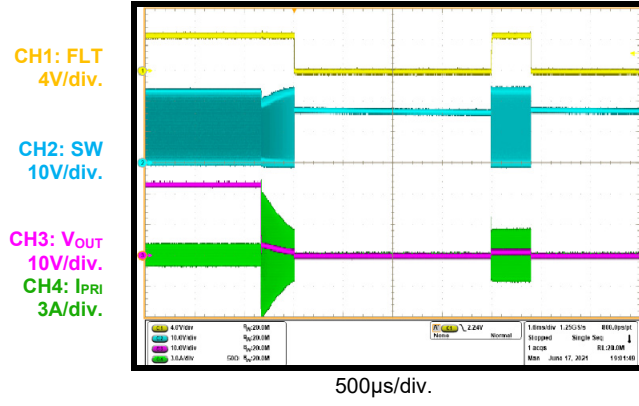


1ms/div.

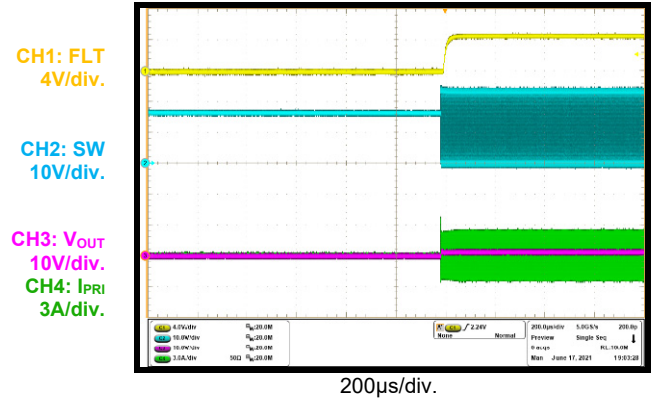
### EVB TEST RESULTS *(continued)*

Performance curves and waveforms are tested on the evaluation board.  $V_{IN} = 24V$ ,  $V_{OUT} = 24V$ ,  $T_A = 25^{\circ}C$ , unless otherwise noted.

**Output Short**



**Output Short Recovery**



## PCB LAYOUT

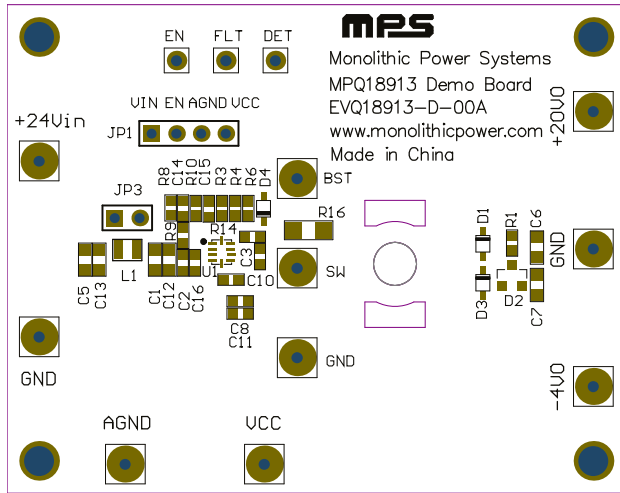


Figure 3: Top Silk

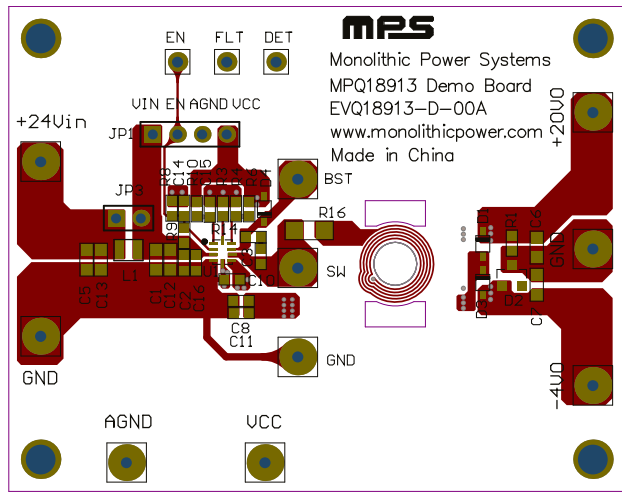


Figure 4: Top Layer

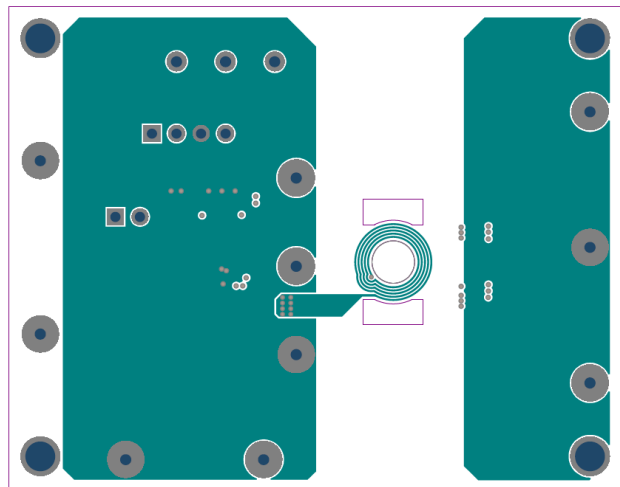


Figure 5: Mid-Layer 1

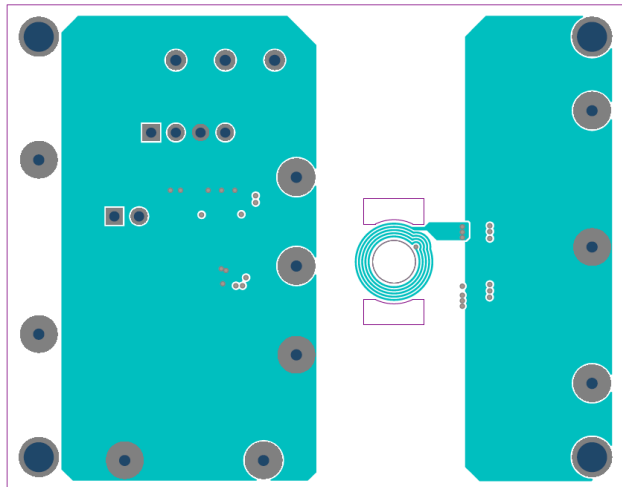


Figure 6: Mid-Layer 2



PCB LAYOUT (continued)

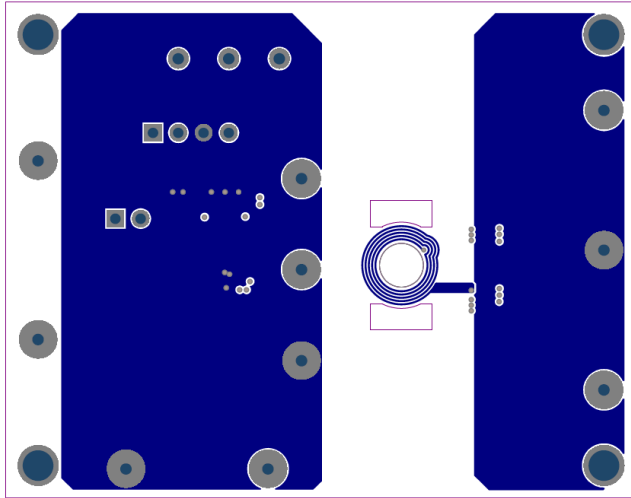


Figure 7: Mid-Layer 3

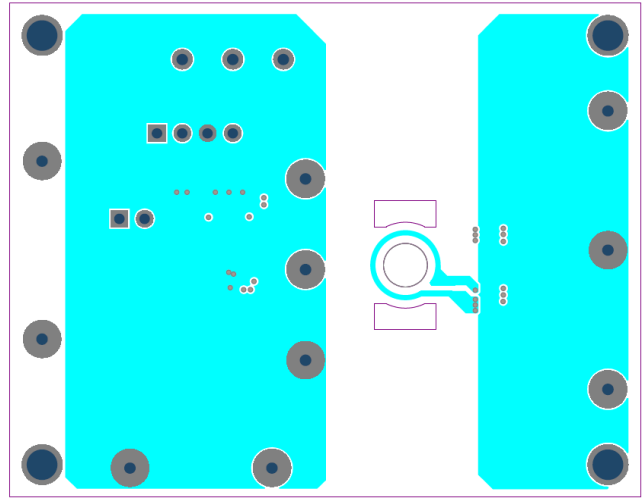


Figure 8: Mid-Layer 4

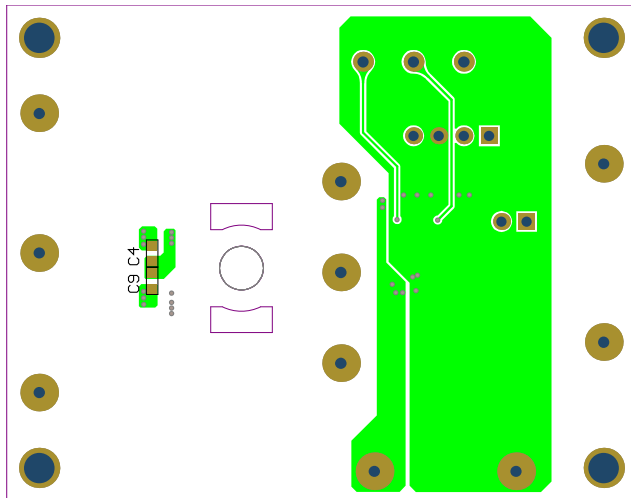


Figure 9: Bottom Layer

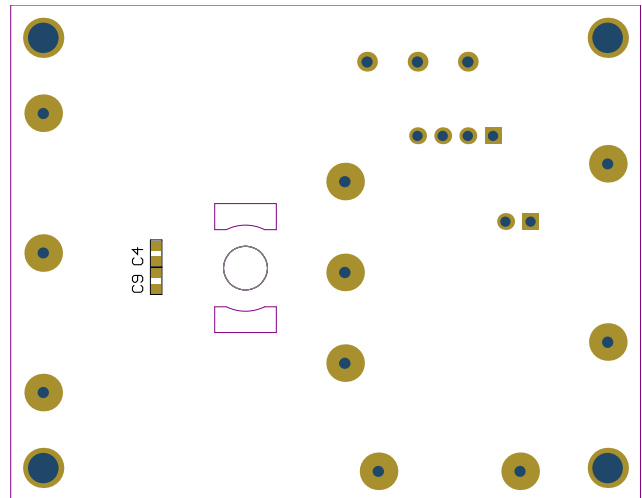


Figure 10: Bottom Silk

## REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	1/18/2022	Initial Release	-

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