EV5514-U-00A

18V, Power Backup and Management Unit for SSD Applications, Evaluation Board

DESCRIPTION

The EV5514-U-00A is an evaluation board designed to demonstrate the capabilities of the MP5514, an input power conditioning power management IC (PMIC) for enterprise solid-state drive (SSD) applications.

The MP5514 features input current limiting and reverse current blocking. It also integrates an MPS-patented, high-efficiency, bidirectional, boost-buck converter with a single inductor for energy storage and system power backup during an input power failure. The device also provides an I²C interface, accurate input current sensing, an analog-to-digital converter (ADC), and backup capacitor health test.

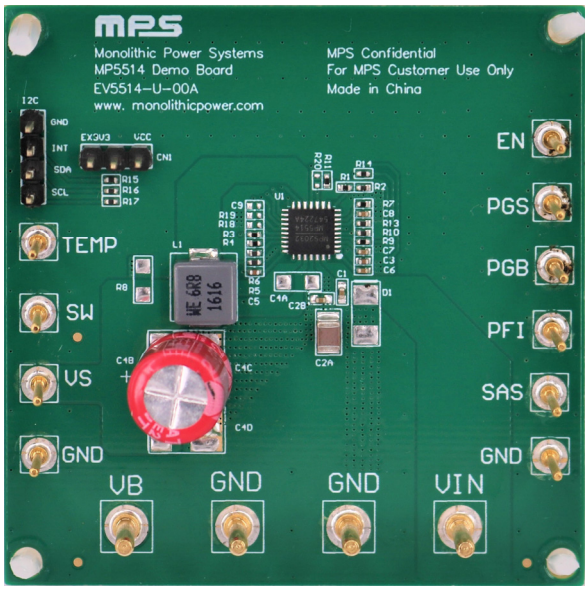
The MP5514 is available in a QFN-30 (5mmx5mm) package.

PERFORMANCE SUMMARY

Specifications are at T_A = 25°C, unless otherwise noted.

Parameters	Conditions	Value
Input voltage (V_{IN}) range		2.7V to 18V
Storage voltage (V_{STRG})	Configured by the FBS divider	Up to 32V
Input power failure threshold (V_{PFI})	Configured by the DET divider (V_{DET_REF} = 0.8V, R1 = 100kΩ, R2 = 11kΩ)	8V
Backup bus voltage (V_{BUS_RLS})	Configured by the FBB divider (V_{FBB_REF} = 0.8V, R3 = 105kΩ, R4 = 12.4kΩ)	7.5V
Backup bus max load (I_{BUS_LOAD})		5A

EV5514-U-00A EVALUATION BOARD



LxW (6.3cmx6.3cm)

Board Number	MPS IC Number
EV5514-U-00A	MP5514GU

QUICK START GUIDE

The layout of the EV5514-U-00A accommodates most commonly used components.

1. Connect the load terminals to:
   a. Positive (+): VB
   b. Negative (-): GND
2. Preset the power supply to 12V, then turn off the power supply.
3. Connect the power supply terminals to:
   a. Positive (+): VIN
   b. Negative (-): GND
4. After making connections, turn on the power supply. The MP5514 charges the storage capacitor to 28V.
5. Turn off the power supply to observe the power release performance.
6. To use the enable function, apply a digital input to the EN pin. When EN is pulled high, the MP5514 is enabled; when EN is pulled from high to low, the MP5514 is forced into buck mode until the storage voltage (V_{STRG}) is discharged.
7. Connect the 2-pin and 3-pin of the I^2C interface pin header together to set the MP5514's I^2C interface signal via the VCC voltage (V_{CC}). Connect the 1-pin and 2-pin connectors of the I^2C interface pin header together to set the MP5514's I^2C interface signal via an external voltage, which is connected to the 3-pin CN1.
8. Set the power failure indication voltage (V_{PFI}) with R1 and R2. V_{PFI} can be calculated with Equation (1):

$$V_{PFI} = (1+\frac{R1}{R2})\times 0.792V \quad (1)$$

9. If a power failure occurs, set the backup bus voltage (V_{BUS_RLS}) with R3 and R4. V_{BUS_RLS} can be calculated with Equation (2):

$$V_{BUS\_RLS} = (1+\frac{R_X \times R3}{(R_X + R3)\times R4})\times V_{FBB\_REF} \quad (2)$$

   Where R_X = 9MΩ and V_{FBB_REF} is typically 0.8V.

10. Set the storage voltage ($V_{STORAGE}$) with R5 and R6. $V_{STORAGE}$ can be calculated with Equation (3):

$$V_{STORAGE} = (1+\frac{R5}{R6})\times V_{FBS\_REF} \quad (3)$$

    Where V_{FBS_REF} is typically 0.8V.

11. Figure 1 shows the proper measurement equipment set-up.

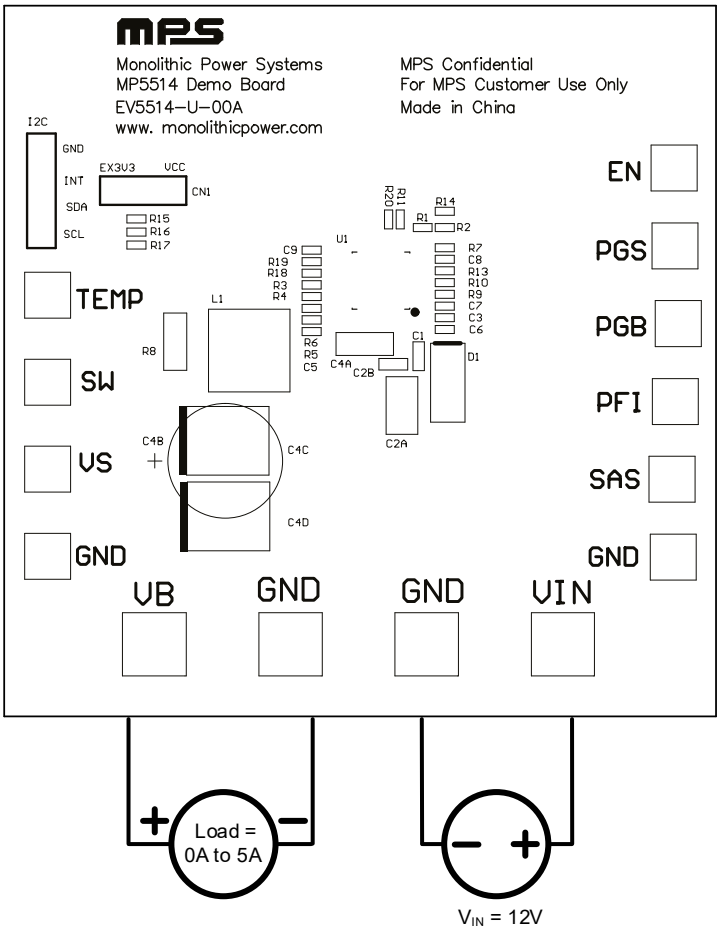


Figure 1: Measurement Equipment Set-Up

EVALUATION BOARD SCHEMATIC

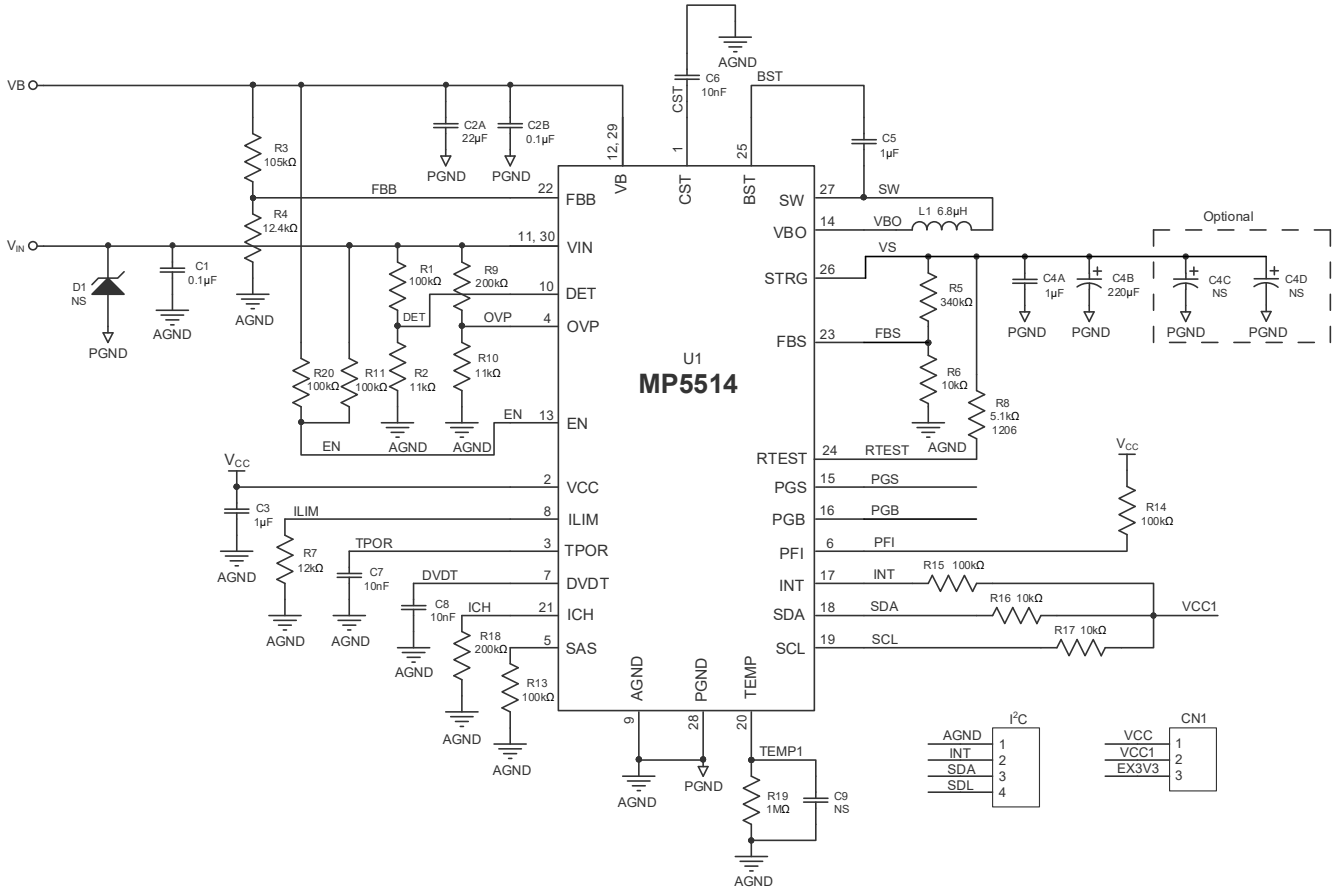


Figure 2: Evaluation Board Schematic

EV5514-U-00A BILL OF MATERIALS

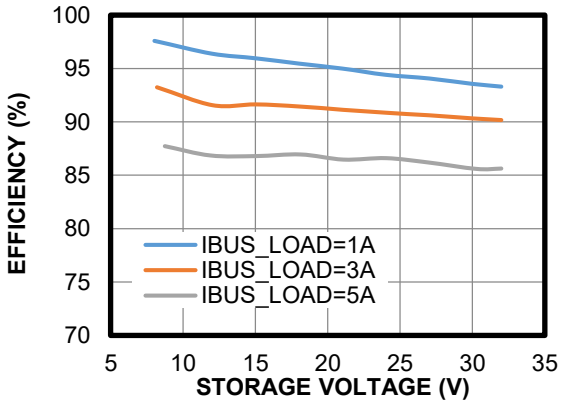
Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
2	C1, C2B	100nF	Ceramic capacitor, 50V, X7R	0603	Murata	GRM155R71H104ME14D
1	C2A	22µF	Ceramic capacitor, 25V, X5R	1210	Murata	GRM32ER61E226KE15L
2	C3, C5	1µF	Ceramic capacitor, 25V, X7R	0402	TDK	C1005X7R1E105KT00E
1	C4A	1µF	Ceramic capacitor, 50V, X7R	1210	Murata	GRM32RR71H105KA01L
1	C4B	220µF	Aluminum electrolytic capacitor, 35V	DIP	Wurth	860080575012
0	C4C, C4D, C9	NS				
3	C6, C7, C8	10nF	Ceramic capacitor, 50V, X7R	0402	Wurth	885012205067
1	L1	6.8µH	Inductor, DCR = 54mΩ, I_{SAT} = 8A	7.3mmx 6.6mmx 2.8mm	Wurth	74437346068
6	R1, R11, R20, R13, R14, R15,	100kΩ	Film resistor, 1%	0402	Yageo	RC0402FR-07100KL
2	R2, R10	11kΩ	Film resistor, 1%	0402	Yageo	RC0402FR-0711KL
1	R3	105kΩ	Film resistor, 1%	0402	Yageo	RC0402FR-07105KL
1	R4	12.4kΩ	Film resistor, 1%	0402	Yageo	RC0402FR-0712K4L
1	R5	340kΩ	Film resistor, 1%	0402	Yageo	RC0402FR-07340KL
3	R6, R16, R17	10kΩ	Film resistor, 1%	0402	Yageo	RC0402FR-0710KL
1	R7	12kΩ	Film resistor, 1%	0402	Yageo	RC0402FR-0712KL
1	R8	5.1kΩ	Film resistor, 5%	1206	Yageo	RC1206JR-7W5K1L
2	R9, R18	200kΩ	Film resistor, 1%	0402	Yageo	RC0402FR-07200KL
1	R19	1MΩ	Film resistor, 1%	0402	Yageo	RC0402JR-071ML
1	U1	MP5514	2.7V to 18V, 5A, energy backup and management unit	QFN-30 (5mmx 5mm)	MPS	MP5514GU

EVB TEST RESULTS

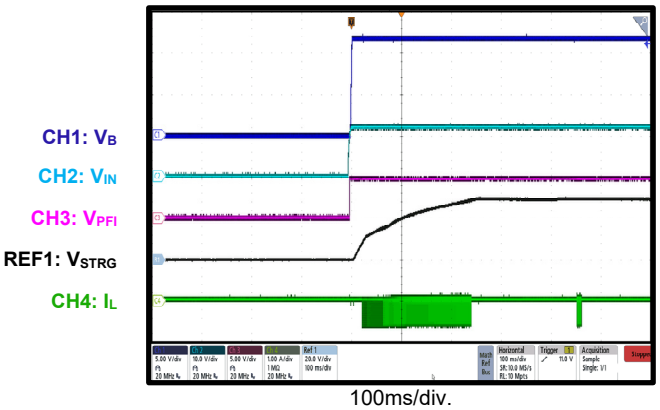
Performance curves and waveforms are tested on the evaluation board. V_{IN} = 12V, V_{STRG} = 30V, V_{PFI} = 8V, V_{BUS_RLS} = 7.5V, L = 10µH, T_A = 25°C, I_{BUS_LOAD} = 5A, unless otherwise noted.

Backup Release Efficiency

V_{BUS_RLS} = 7.5V, L = 10µH

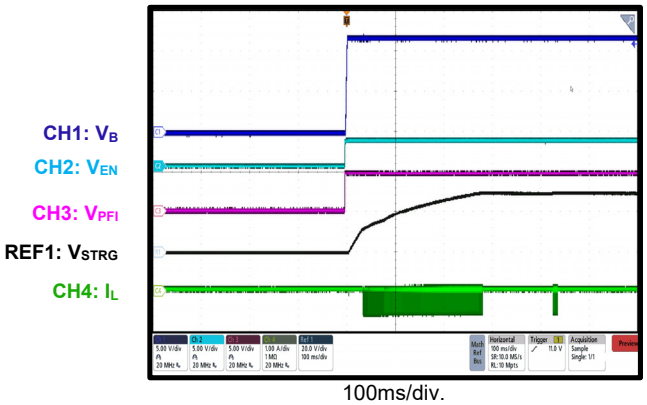


Start-Up through VIN



100ms/div.

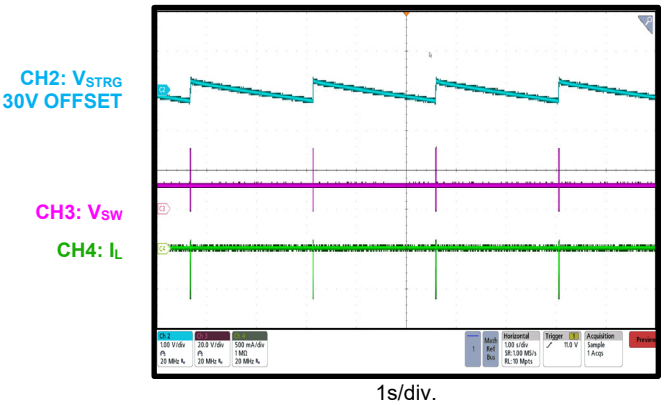
Start-Up through EN



100ms/div.

Boost Steady State

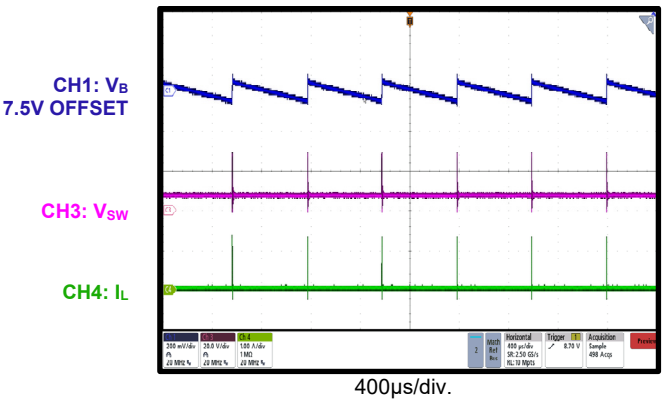
R_{ICH} = 200kΩ



1s/div.

Buck Steady State

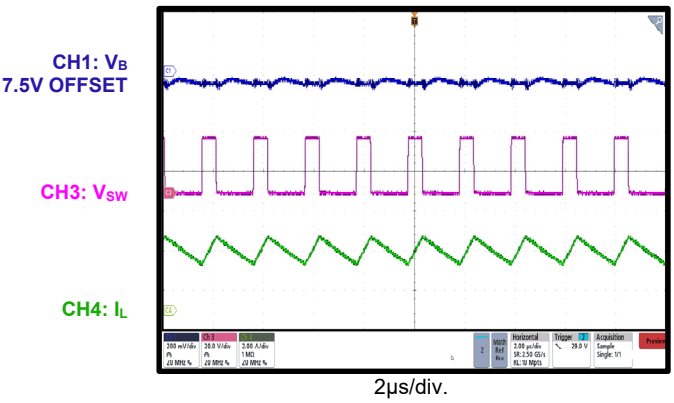
I_{BUS_LOAD} = 0A



400µs/div.

Buck Steady State

I_{BUS_LOAD} = 3A



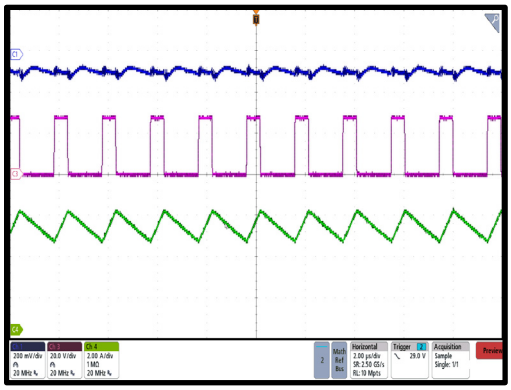
2µs/div.

EVB TEST RESULTS *(continued)*

Performance curves and waveforms are tested on the evaluation board. V_{IN} = 12V, V_{STRG} = 30V, V_{PFI} = 8V, V_{BUS_RLS} = 7.5V, L = 10µH, T_A = 25°C, I_{BUS_LOAD} = 5A, unless otherwise noted.

Buck Steady State

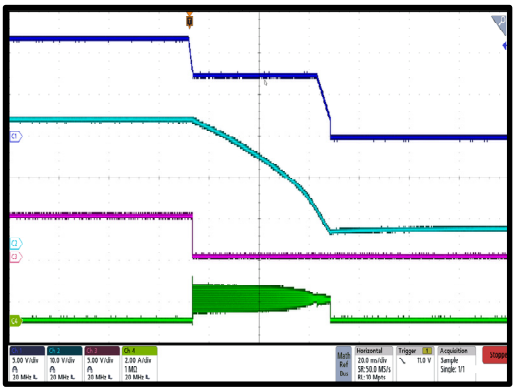
I_{BUS_LOAD} = 5A



2µs/div.

V_{STRG} Release

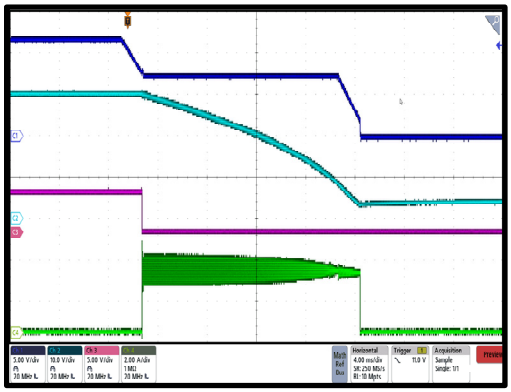
I_{BUS_LOAD} = 1A



20ms/div.

V_{STRG} Release

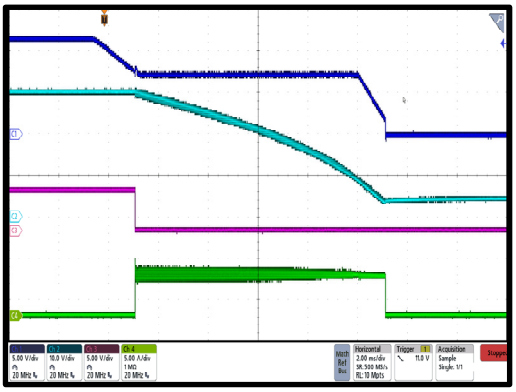
I_{BUS_LOAD} = 3A



4ms/div.

V_{STRG} Release

I_{BUS_LOAD} = 5A



2ms/div.

PCB LAYOUT

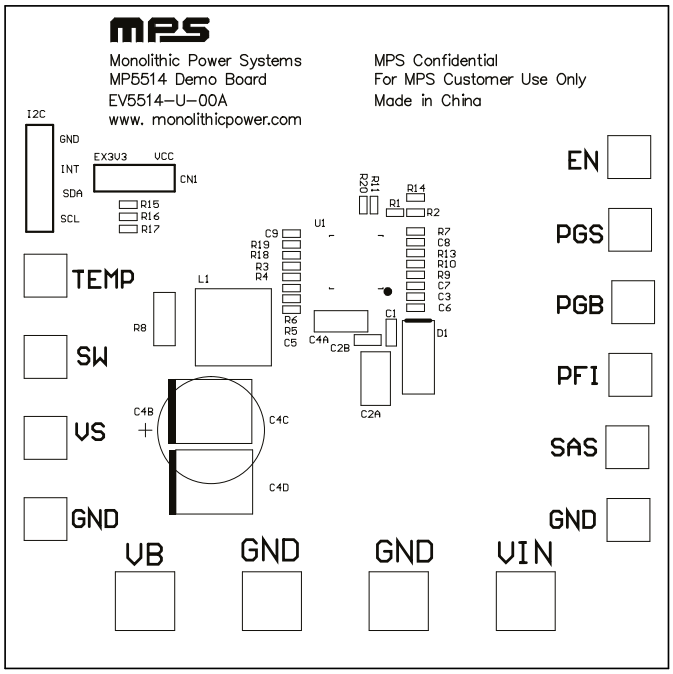


Figure 3: Top Silk

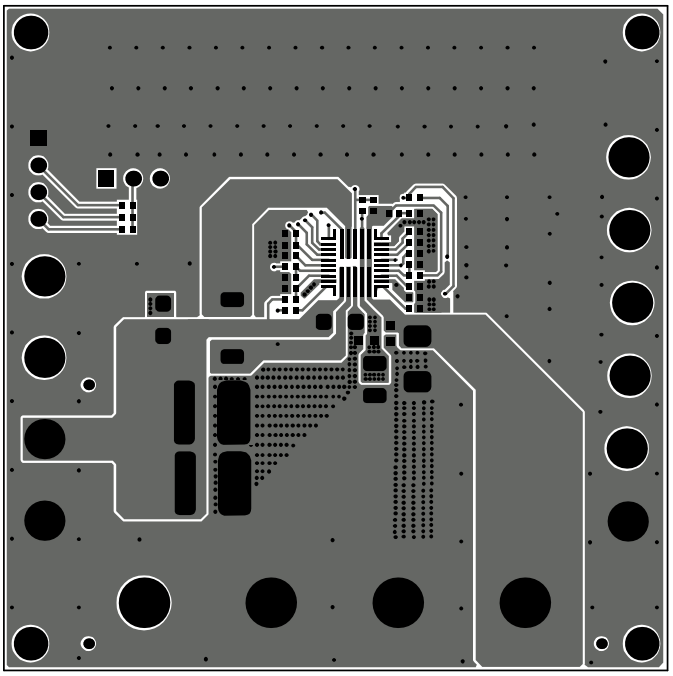


Figure 4: Top Layer

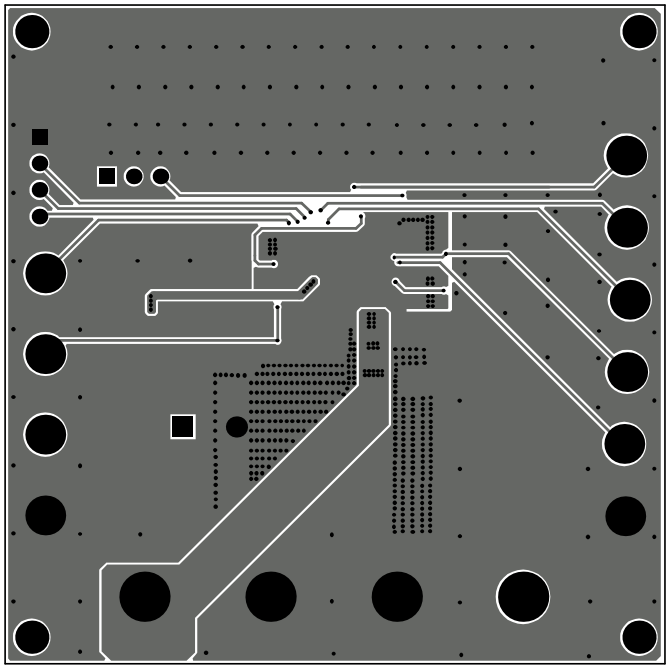


Figure 5: Bottom Layer

Figure 6: Bottom Silk

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	12/12/2023	Initial Release	-