

## DESCRIPTION

The MP5021 is a hot-swap protection device designed to protect circuitry on its output from transients on its input. It also protects its input from undesired shorts and transients coming from its output.

An internal charge pump drives the gate of the power device, allowing for a power FET with a very low ON resistance of 7mΩ.

The MP5021 includes an optional discharge function that provides a discharge path for the external output capacitor when the part is disabled. Fault protection includes current limit, thermal shutdown and damaged MOSFET detection. Both of the current limit and thermal shutdown have user settable auto retry and latch off mode. The device also features over-voltage protection and under-voltage protection

The MP5021 is available in 3mmx5mm QFN package.

## ELECTRICAL SPECIFICATIONS

Parameter	Symbol	Value	Units
Input Voltage Range	V <sub>IN</sub>	8-16	V
Output Voltage	V <sub>OUT</sub>	8-16	V
Load Max	I <sub>OUT</sub>	10	A

## FEATURES

- Integrated 7mΩ Power FET
- Adjustable Current Limit (5A to 15A)
- Output Current Measurement
- +/-5% Current Limit and Monitor Accuracy
- Fast Response (<200ns) for Short Protection
- PG Detector and FLTB Indication
- PG Assert Low at VIN=0
- Damaged MOSFET Detection
- External Soft Start
- Programmable EN Blanking Time
- Under/Over Voltage Lockout
- Thermal Protection
- Small 3mmx5mm QFN Package

## APPLICATIONS

- Hot Swap
- PC Cards
- Disk Drives
- Laptops

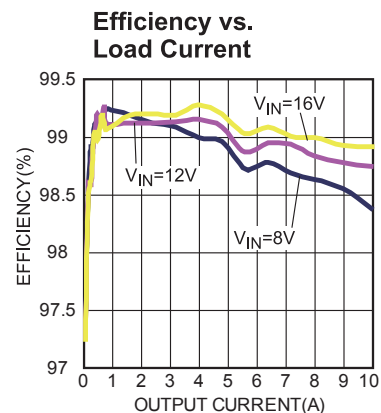
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## EV5021GQV-00A EVALUATION BOARD

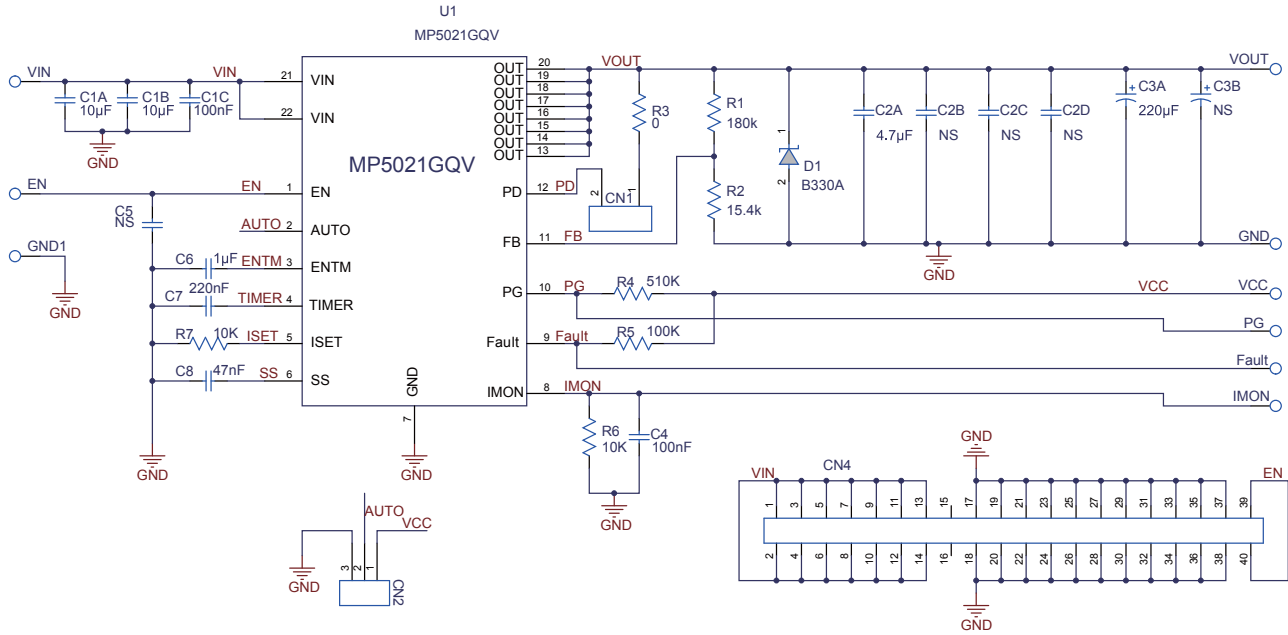


(L × W × H) 8.55cm × 8.55cm × 1.6mm

Board Number	MPS IC Number
EV5021GQV-00A	MP5021GQV



## EVALUATION BOARD SCHEMATIC



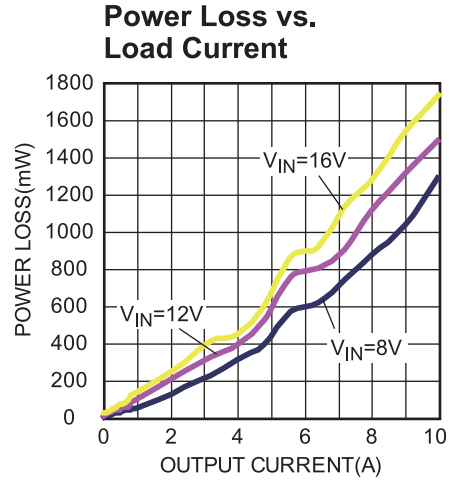
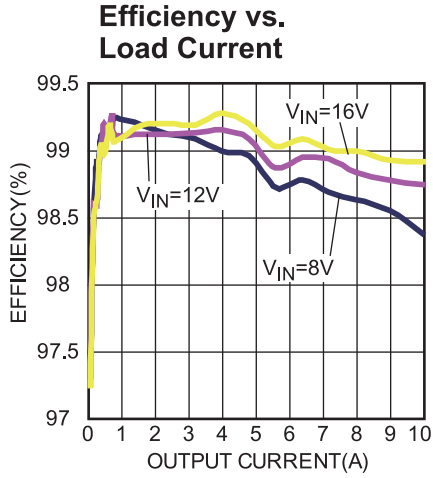
**EV5021GQV-00A BILL OF MATERIALS**

Qty	RefDes	Value	Description	Package	Manufacture	Manufacture P/N
2	C1A,C1B	10μF	Ceramic Cap.,50V, 10%, X7R	1210	muRata	GRM32ER71H106KA1 2L
1	C1C	100nF	Ceramic Cap.,100V, 10%, X7R	0805	muRata	GRM21BR72A104KAC 4L
1	C3A	220μF	Electrolytic Cap., 35V	DIP	江海	CD110-35V220
1	C2A	4.7μF	Ceramic Cap.,50V, 10%, X7R	1206	muRata	GRM31CR71H475KA1 2L
1	C4	100nF	Ceramic Cap., 25V, 10%,X7R	0603	muRata	GRM188R71C104KA0 1D
1	C5	NS	Not Stuffed			
1	C6	1μF	Ceramic Cap., 6.3V, 10%, X7R	0603	muRata	GRM188R70J105KA01
1	C7	220nF	Ceramic Cap.,16V, 10%, X7R	0603	muRata	GRM188R71C224KA0 1D
1	C8	47nF	Ceramic Cap., 50V, 10%, X7R	0603	muRata	GRM188R71H473KA6 1D
1	D1	B330A	Schottky Diodes, 30V, 3A	SMA	Diodes	B330A
1	R1	180k	Film Res., 1%	0603	Yageo	RC0603FR-07180KL
1	R2	15.4k	Film Res., 1%	0603	Yageo	RC0603FR-0715K4L
1	R3	0	Film Res., 5%	0603	Yageo	RC0603JR-070R0L
1	R4	510k	Film Res., 1%	0603	Yageo	RC0603FR-07510KL
1	R5	100k	Film Res., 1%	0603	Yageo	RC0603FR-07100KL
2	R6,R7	10k	Film Res., 1%	0603	Yageo	RC0603FR-0710KL
1	U1	IC	Hot Swap Protection device	QFN22(3*5mm)	MPS	MP5021GQV

**EVB TEST RESULTS**

Performance waveforms are tested on the evaluation board.

V<sub>IN</sub>=12V, C<sub>OUT</sub>=220μF, C<sub>6</sub>=1μF, C<sub>7</sub>=220nF, C<sub>8</sub>=47nF, R<sub>7</sub>=10kΩ, T<sub>A</sub>=+25°C, unless otherwise noted.

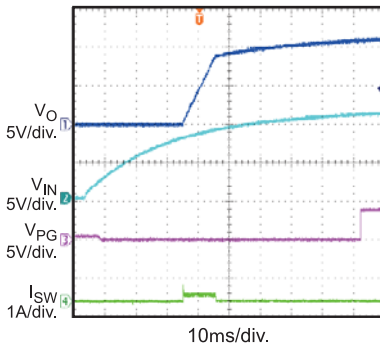


## EVB TEST RESULTS (continued)

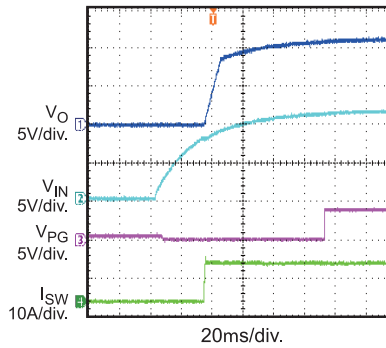
Performance waveforms are tested on the evaluation board.

$V_{IN}=12V$ ,  $C_{OUT}=220\mu F$ ,  $C_6=1\mu F$ ,  $C_7=220nF$ ,  $C_8=47nF$ ,  $R_7=10k\Omega$ ,  $T_A=+25^\circ C$ , unless otherwise noted.

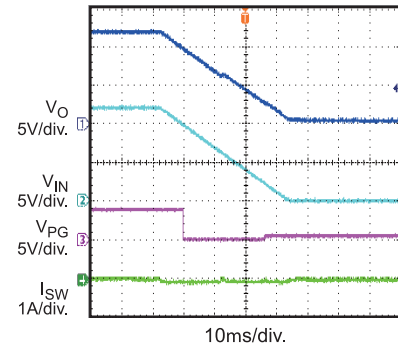
**Start Up through Vin**  
 $I_O = 0A$



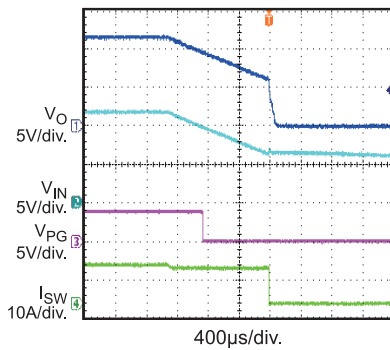
**Start Up through Vin**  
 $I_O = 10A$



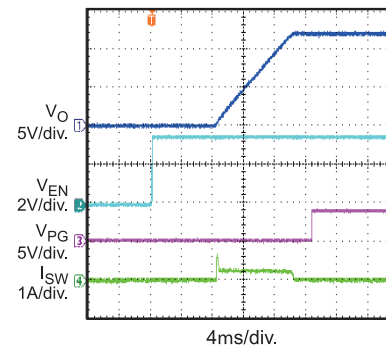
**Shut Down through Vin**  
 $I_O = 0A$



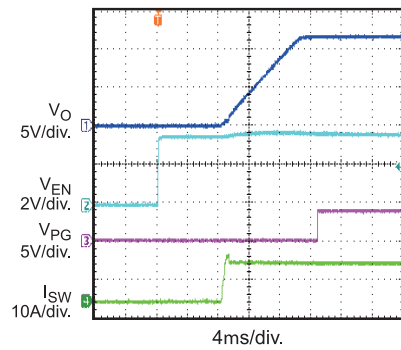
**Shut Down through Vin**  
 $I_O = 10A$



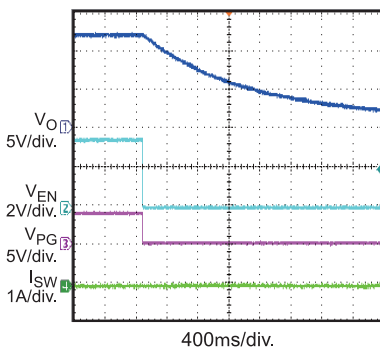
**Start Up through EN**  
 $I_O = 0A$



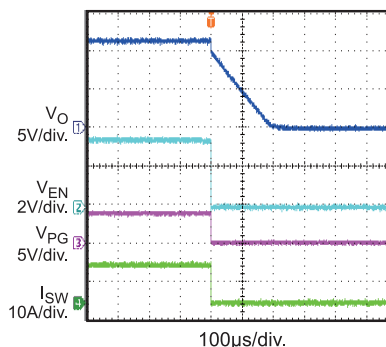
**Start Up through EN**  
 $I_O = 10A$



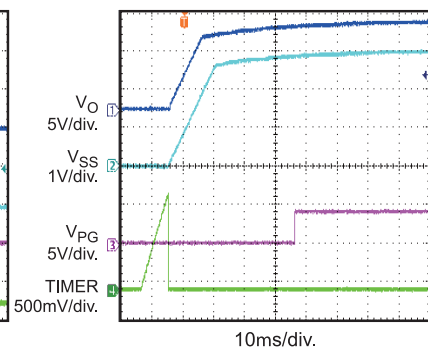
**Shut Down through EN**  
 $I_O = 0A$



**Shut Down through EN**  
 $I_O = 10A$



**Start-Up Sequence**



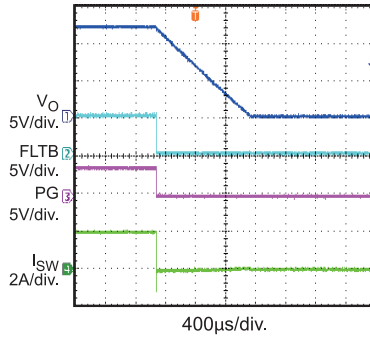
## EVB TEST RESULTS (continued)

Performance waveforms are tested on the evaluation board.

$V_{IN}=12V$ ,  $C_{OUT}=220\mu F$ ,  $C_6=1\mu F$ ,  $C_7=220nF$ ,  $C_8=47nF$ ,  $R_7=10k\Omega$ ,  $T_A=+25^\circ C$ , unless otherwise noted.

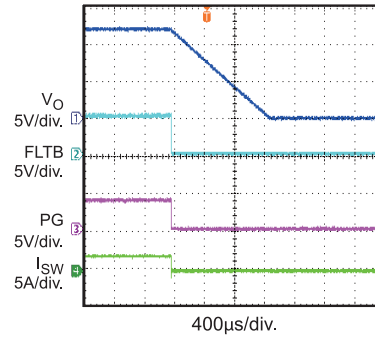
### Thermal Shutdown

$I_O = 2A$ , Latch mode



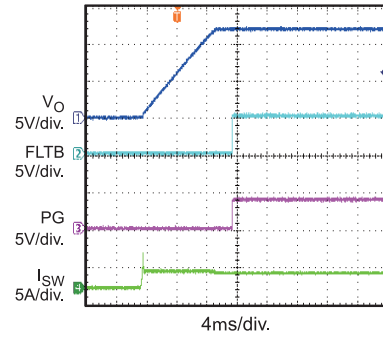
### Thermal Shutdown

$I_O = 2A$ , Retry mode



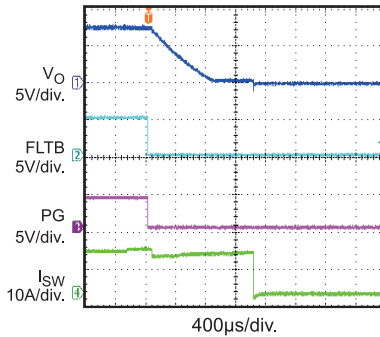
### Thermal Recovery

$I_O = 2A$ , Retry mode



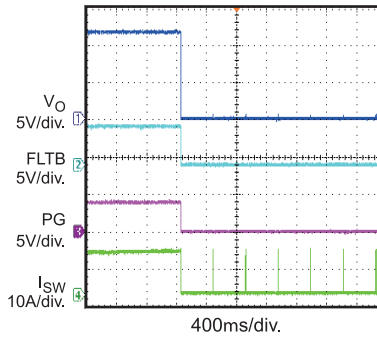
### OCP

$V_{IN} = 12V$ , Latch mode



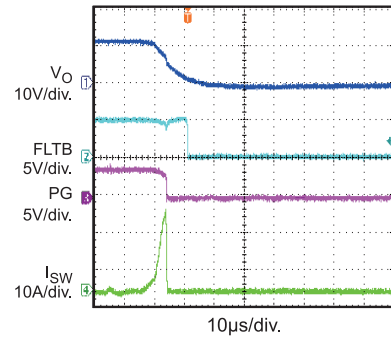
### OCP

$V_{IN} = 12V$ , Retry mode



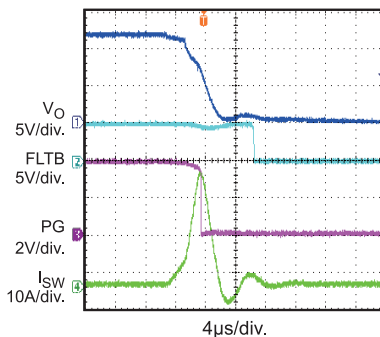
### SCP Entry

$V_{IN} = 12V$ , Latch mode



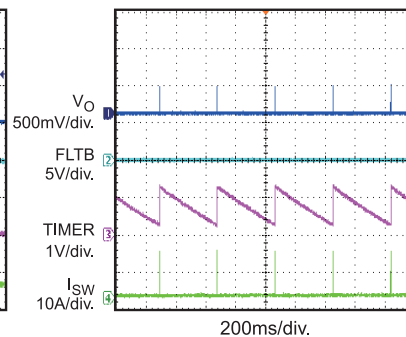
### SCP Entry

$V_{IN} = 12V$ , Retry mode



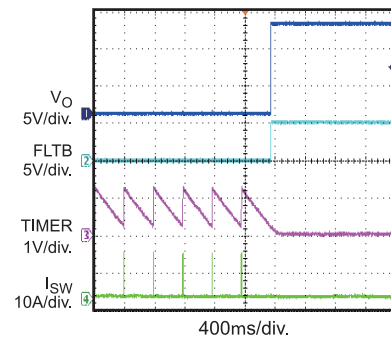
### SCP Steady State

$V_{IN} = 12V$ , Retry mode



### SCP Recovery

$V_{IN} = 12V$ , Retry mode



## PRINTED CIRCUIT BOARD LAYOUT

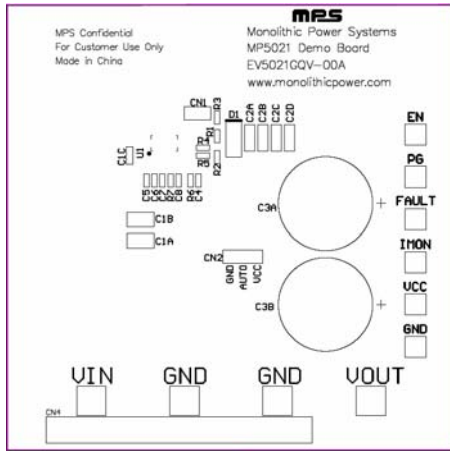


Figure 1—Top Silk Layer

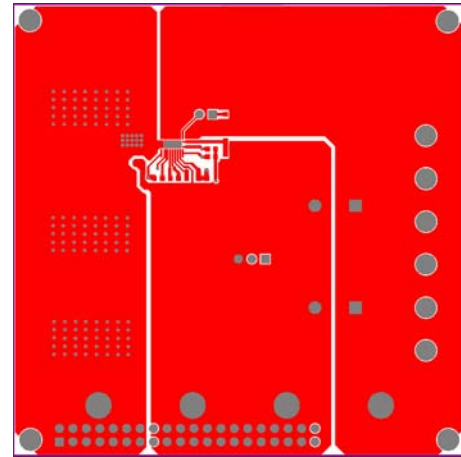


Figure 2—Top Layer

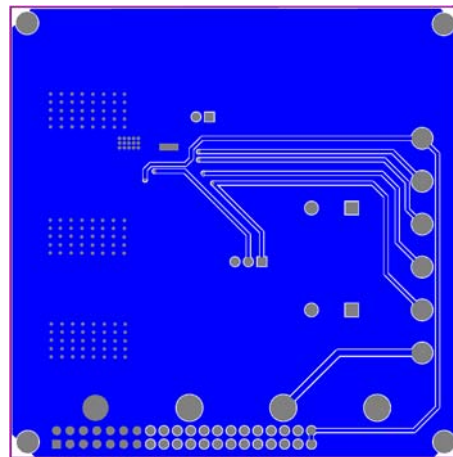


Figure 5—Bottom Layer

## QUICK START GUIDE

The default output voltage of this board is set to 12V.

The board layout accommodates most commonly used schottky and output capacitors.

1. Attach the positive and negative ends of the load to the VOUT and GND pins, respectively.
2. Attach the input voltage ( $8V \leq V_{IN} \leq 16V$ ) and input ground to the VIN and GND pins, respectively. Then the board is powered up.
3. The EV5021GQV-00A is enabled ON in default. It's turned on once the input voltage is applied. To enable the board externally, apply a voltage,  $V_{EN} \geq 2V$ , to the EN pin. To disable the board, apply a voltage,  $V_{EN} \leq 0.4V$ , to the EN pin.
4. The board is retry mode when OCP in default, users can select retry mode or latch mode by apply the auto pin to VCC or GND.

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