

### DESCRIPTION

The EV2497GN-A-00A is an evaluation board for the MP2497GN-A. The MP2497GN-A is a monolithic step-down switch mode converter with a programmable output current limit. It achieves 3A continuous output current over a wide input supply range with excellent load and line regulation. An internal 2-4ms soft start prevents inrush current at turning on. And it is capable of providing output line drop compensation.

Fault condition protection includes hiccup current limit and short circuit protection, programmable output over voltage protection and thermal shutdown.

The MP2497GN-A requires a minimum number of readily available standard external components.

### ELECTRICAL SPECIFICATIONS

Parameter	Symbol	Value	Units
Input Voltage	V <sub>IN</sub>	8 - 50	V
Output Voltage	V <sub>OUT</sub>	5	V
Output Current Limit	I <sub>OUT-L</sub>	3	A
Output OVP	V <sub>OVP</sub>	6	V

### FEATURES

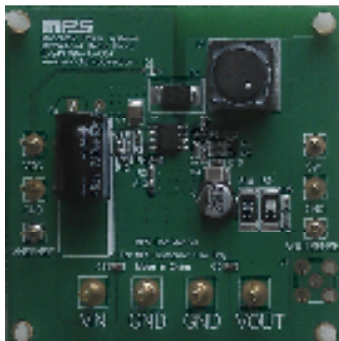
- Wide 8V to 50V Operating Input Range
- Programmable up to 3A Output Current
- Programmable Output Over Voltage Protection
- Internal 4ms Soft Start
- Stable with Low ESR Output Ceramic Capacitors
- Fixed 100kHz Frequency
- Thermal Shutdown
- Output Line Drop Compensation
- Hiccup Circuit Limit and Short Circuit Protection

### APPLICATIONS

- USB Power Supplies
- Automotive Cigarette Lighter Adapters
- Power Supply for Linear Chargers

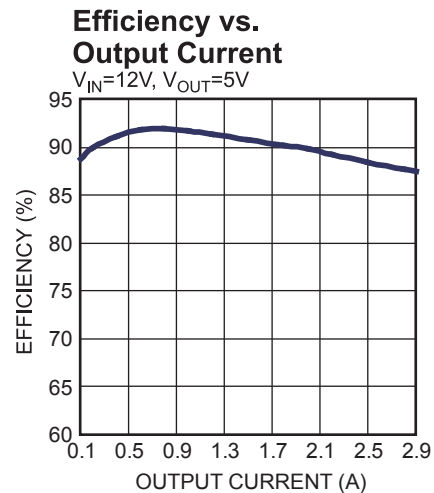
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### EV2497GN-A-00A EVALUATION BOARD

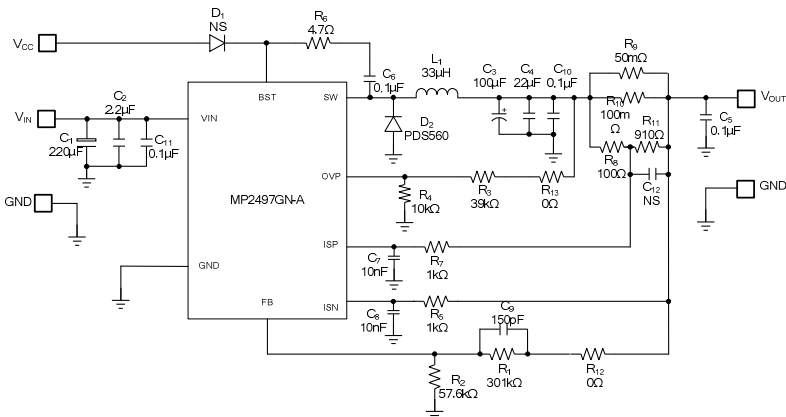


(L x W x H) 2.5" x 2.5" x 0.4"  
(6.35cm x 6.35cm x 1cm)

Board Number	MPS IC Number
EV2497GN-A-00A	MP2497GN-A



## EVALUATION BOARD SCHEMATIC



## EV2497GN-A-00A BILL OF MATERIALS

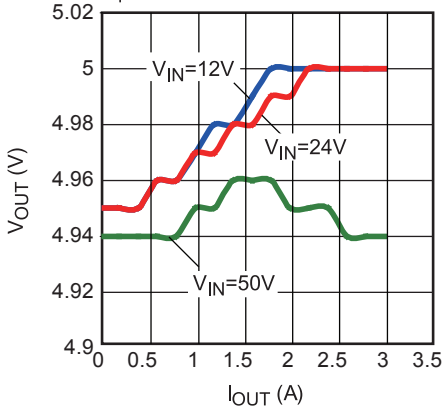
Qty	RefDes	Value	Description	Package	Manufacturer	Manufacturer P/N
1	C1	220 $\mu$ F	Electronic Cap, 63V	DIP	NICHICON	NICUVZ1J221MPH
1	C2	2.2 $\mu$ F	Ceramic Cap., 100V, X7R	1210	muRata	GRM32ER72A225KA35L
1	C3	100 $\mu$ F	Electronic Cap., 16V	SMD	TDK	S3225X7R1C107K-T
1	C4	22 $\mu$ F	Ceramic Cap., 16V, X7R	1210	muRata	GRM32ER71C226KE18L
3	C5, C6, C10	100nF	Ceramic Cap., 50V, X7R	0603	muRata	GRM188R71H104KA93D
2	C7, C8	10nF	Ceramic Cap., 50V, X7R	0603	muRata	GRM188R71H103KA01D
1	C9	150pF	Ceramic Cap., 50V, C0G	0603	muRata	GRM1885C1H151JA01D
1	C11	0.1 $\mu$ F	Ceramic Cap., 100V, X7R	0603	muRata	GRM188R72A104KA35D
0	C12	NS	Do Not Stuff			
0	D1	NS	Do Not Stuff			
1	D2	5A,60V	Diode	PowerDITM5	Diodes	PDS560
1	L1	33 $\mu$ H	Inductor, 5.5A/45m $\Omega$	SMD	SMD	7447709330
1	R1	301k $\Omega$	Film Res., 1%	0603	Yageo	RC0603FR-07301KL
1	R2	57.6k $\Omega$	Film Res., 1%	0603	Yageo	RC0603FR-0757K6L
1	R3	39k $\Omega$	Film Res., 1%	0603	Yageo	RC0603FR-0739KL
1	R4	10k $\Omega$	Film Res., 1%	0603	Yageo	RC0603FR-0710KL
1	R6	4.7 $\Omega$	Film Res., 1%	0603	Yageo	RC0603FR-074R7L
1	R8	100 $\Omega$	Film Res., 1%	0603	Yageo	RC0603FR-07100RL
1	R11	910 $\Omega$	Film Res., 1%	0604	Yageo	RC0603FR-07910RL
2	R12, R13	0 $\Omega$	Film Res., 5%	0603	Royalohm	0603J0000T5E
2	R5, R7	1k $\Omega$	Film Res., 1%	0603	Royalohm	0603F1001T5E
1	R9	50m $\Omega$	Sense Res., 1%	2512	LiZhi	2512-50MR
1	R10	100m $\Omega$	Sense Res., 1%	2512	LiZhi	2512-100MR
1	U1		DC-DC Converter	SOIC8E	MPS	MP2497GN-A

### EVB TEST RESULTS

C1=220μF, C2=2.2μF, C3=100μF, C4=22μF, L=33μH, R<sub>SENSE</sub>=R9//R10=33mΩ, R8=100Ω, R11=910Ω, T<sub>A</sub>=25°C, unless otherwise noted.

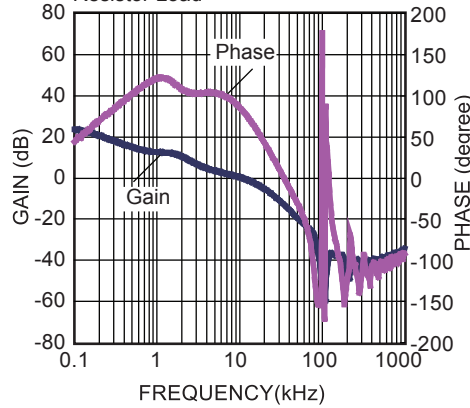
#### Output Line Drop Compensation

R<sub>SENSE</sub>=25mΩ, R<sub>TRACE</sub>=120mΩ  
R<sub>f</sub>=301kΩ



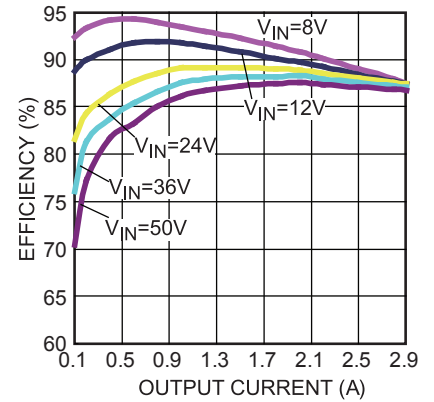
#### Loop Gain with Phase Margin

V<sub>IN</sub>=12V, V<sub>OUT</sub>=5V, I<sub>OUT</sub>=3A  
Resistor Load



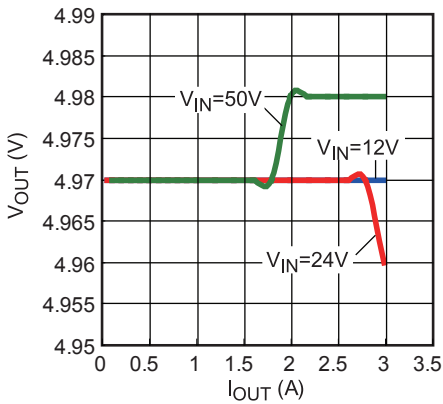
#### Efficiency vs. Output Current

All Input Voltage Range



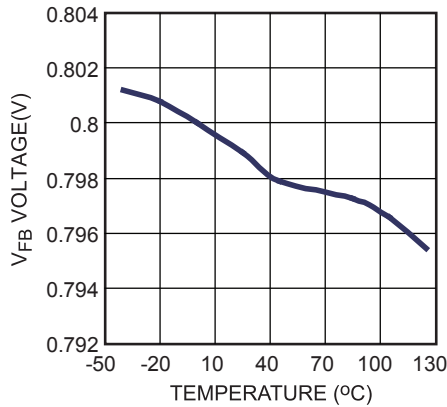
#### Load Regulation

Connect ISP, ISN to GND



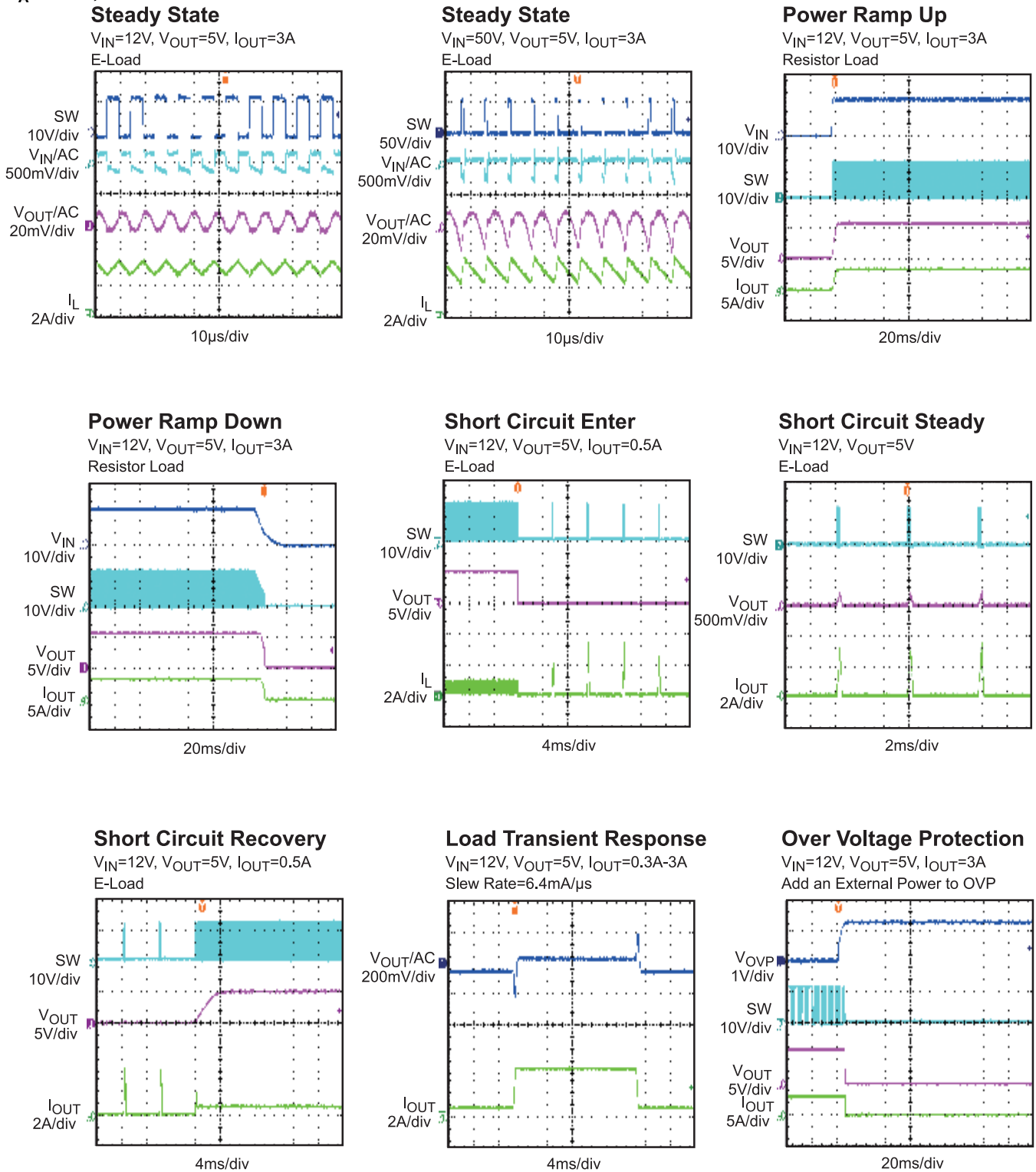
#### V<sub>FB</sub> vs. Temperature

V<sub>IN</sub>=12V

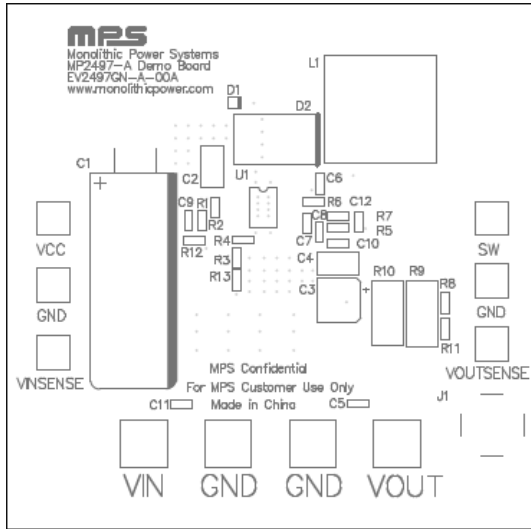


**EVB TEST RESULTS (continued)**

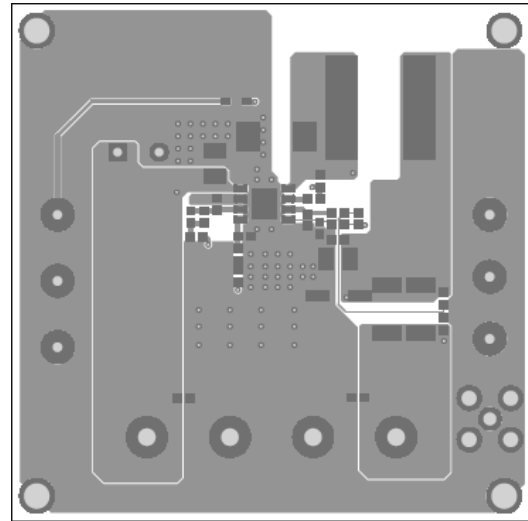
**C1=220 $\mu$ F, C2=2.2 $\mu$ F, C3=100 $\mu$ F, C4=22 $\mu$ F, L=33 $\mu$ H, R<sub>SENSE</sub>=R9//R10=33m $\Omega$ , R8=100 $\Omega$ , R11=910 $\Omega$ , T<sub>A</sub>=25 $^{\circ}$ C, unless otherwise noted.**



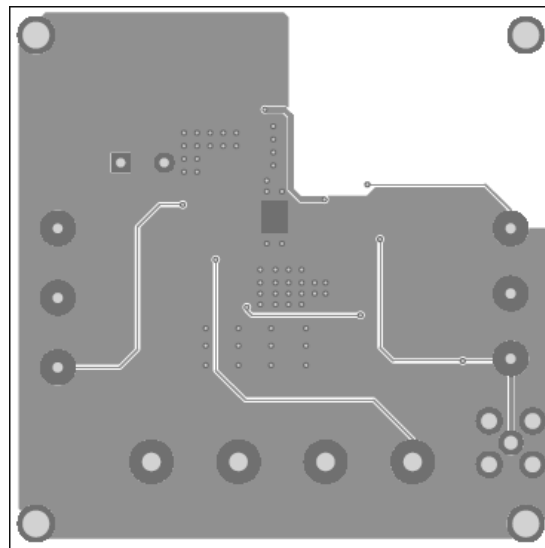
**PRINTED CIRCUIT BOARD LAYOUT**



**Figure 1—Top Silk Layer**



**Figure 2—Top Layer**



**Figure 3—Bottom Layer**

## QUICK START GUIDE

1. The output voltage of this board is set to 5V. The board layout accommodates most commonly used inductors and output capacitors.
2. Attach the positive and negative ends of the load to the VOUT and GND pins, respectively.
3. Attach the input voltage ( $8V \leq V_{IN} \leq 50V$ ) and input ground to the VIN and GND pins, respectively.
4. The output current limit is set as:

$$I_{OUT\_L} = \frac{100mV}{R_{SENSE}} \times \frac{R8 + R11}{R11} \quad (R_{SENSE} = R9 // R10)$$

5. The output line compensation is set via R1

$$R1 = \frac{R_{TRACE} \times 400k\Omega}{6 \times R_{SENSE}} \times \frac{R8 + R11}{R11}$$

Where, the  $R_{TRACE}$  is the resistance of the output line.

6. The output voltage  $V_{OUT}$  can be set by R2. The formula is:

$$R2 = R1 \times \frac{V_{FB}}{V_{OUT} - V_{FB}}$$

Where  $V_{FB} = 0.8V$

For example, for  $V_{OUT} = 5V$ ,  $R1=301k\Omega$ :

$$R2 = R1 \times \frac{V_{FB}}{V_{OUT} - V_{FB}} = 301k\Omega \times \frac{0.8V}{5V - 0.8V} = 57.6k\Omega$$

For the closest standard 1% value.

7. The short circuit current limit is set as:

$$I_{OUT\_SL} = \frac{100mV - 6.2\mu A \times R7}{R_{SENSE}} \times \frac{R8 + R11}{R11}$$

8. RC filter connected to ISN and ISP pin is better to be set as  $RC \geq 10^{-5}s$ , and it should meet

$$R7 + \frac{R8 \times R11}{R8 + R11} = R5, \quad C7 = C8$$

9. When the OVP pin voltage is higher than 1.23V, the part will shutdown. The R3 is set as:

$$R3 = \frac{(V_{OUT} - 1.23V) \times R4}{1.23V}$$

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