



EV1930-QN-01A

10A, 75V, Integrated Half-Bridge Evaluation Board

DESCRIPTION

The EV1930-QN-01A evaluation board is designed to demonstrate the capabilities of the MP1930, an integrated gate driver with one half-bridge consisting of two N-channel MOSFETs.

The EV1930-QN-01A operates from a maximum 75V power input voltage (V_{IN}) and 18V supply voltage (V_{DD}). The MP1930 can deliver up to 10A of continuous output current (I_{OUT}). The driving logic signals are generated by an external controller.

PERFORMANCE SUMMARY

Specifications are at $T_A = 25^\circ\text{C}$, unless otherwise noted.

Parameters	Conditions	Value
Input voltage (V_{IN}) range		18V to 75V
Supply voltage (V_{DD}) range		9V to 18V
Driving logic voltage (V_{SIGNAL})		3.3V to 18V
Maximum output current (I_{OUT})	$V_{IN} = 18\text{V to }75\text{V}, V_{DD} = 9\text{V to }18\text{V}$	10A

EVALUATION BOARD



LxW (7cmx7.7cm)

Board Number	MPS IC Number
EV1930-QN-01A	MP1930GQN

QUICK START GUIDE

1. Preset the input power to (V_{IN}) to $18V \leq V_{IN} \leq 75V$, then preset the supply power (V_{DD}) to $9V \leq V_{DD} \leq 18V$.
2. Turn the power supply off.
3. Connect the input power terminals to:
 - a. Positive (+): VIN
 - b. Negative (-): GND
4. Connect the power supply terminals to:
 - a. Positive (+): VDD
 - b. Negative (-): GND
5. Connect the driving logic signals (generated by the external controller) to the EN, INH, and INL pins.
6. Connect the load terminals to:
 - a. Positive (+): OUT
 - b. Negative (-): GND
7. Turn the power supply on after making the connections.

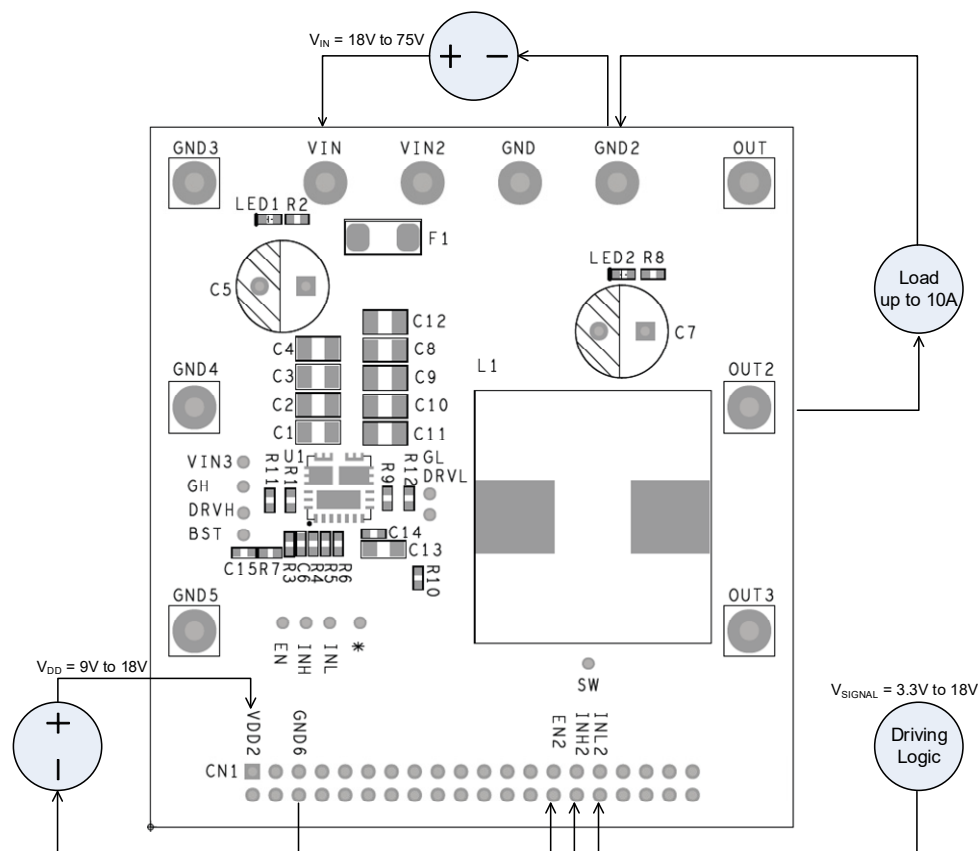


Figure 1: Measurement Equipment Set-Up

EVALUATION BOARD SCHEMATIC

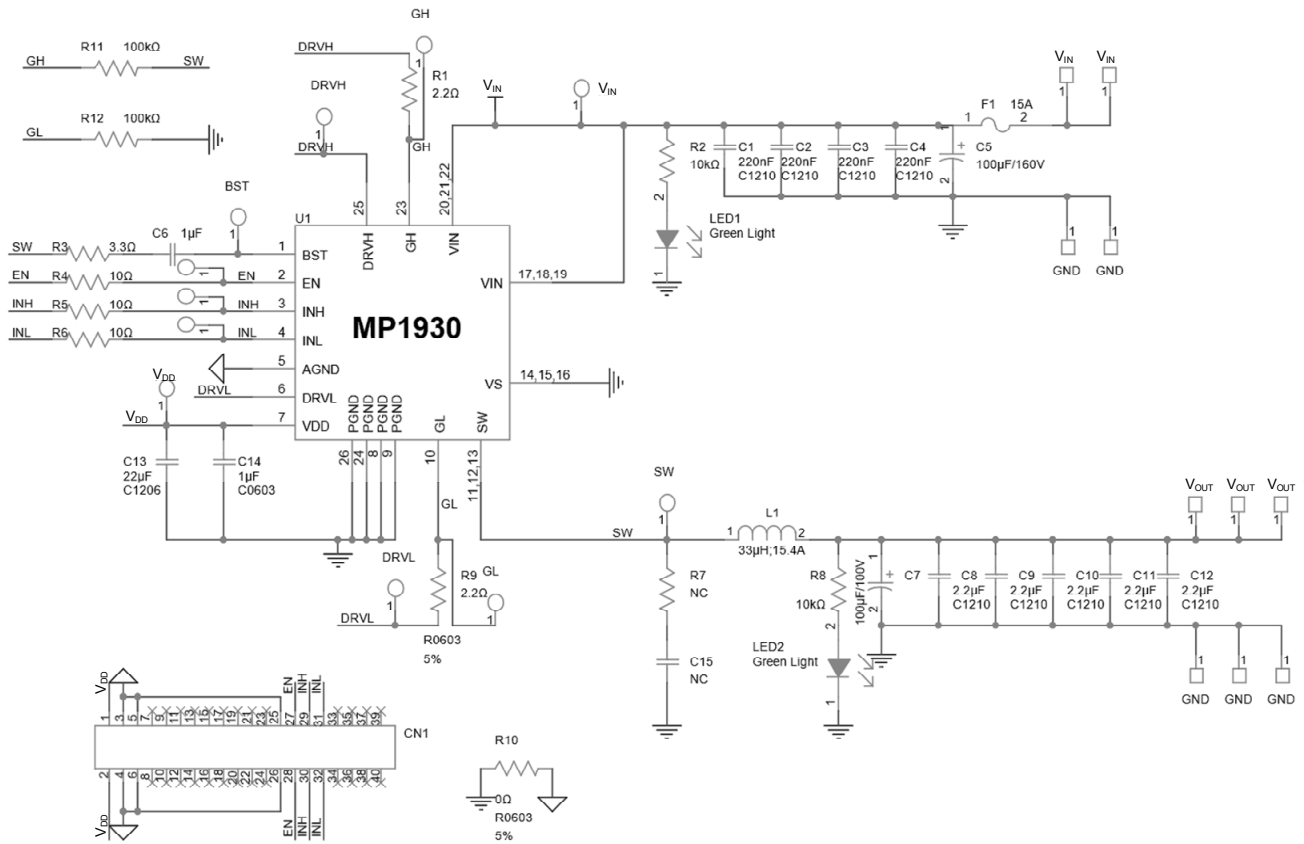


Figure 2: Evaluation Board Schematic

EV1930-QN-01A BILL OF MATERIALS

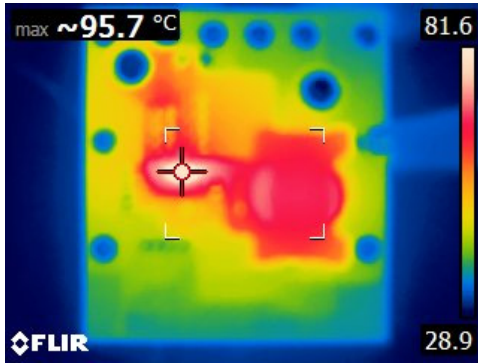
Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
11	VIN, VDD, EN, INH, INL, SW, GH, GL, BST, DRVH, DRVL	Yellow	Yellow test point	DIP	Any	
10	VINx2, GNDx5, OUTx3	2mm	Φ = 2mm needle	DIP	Any	
1	CN1	2 x 20-pin	2 x 20-pin, 180°, 2.54mm	DIP	Any	
4	C1, C2, C3, C4	220nF	Ceramic capacitor, 250V, X7R, 1210	1210	Murata	GRM32DR72E224KW01L
2	C5, C7	100μF	Electrolytic capacitor, 100V, D10xL20mm	DIP	Jianghai	CD263-100V100
2	C6, C14	1μF	Ceramic capacitor, 25V, X7R, 0603	0603	Murata	GCM188R71E105KA64D
5	C8, C9, C10, C11, C12	2.2μF	Ceramic capacitor, 100V, X7R, 1210	1210	Murata	GRM32ER72A225KA35L
1	C13	22μF	Ceramic capacitor, 25V, X5R, 1206	1206	TDK	C3216X5R1E226MT
1	C15	NC				
1	F1	15A	Fuse, 15A, SMD2410	2410	Any	
2	LED1, LED2	Green	Green LED	0603	Bright LED	BL-HGE36A-AV-TRB
1	L1	33μH	Inductor, 33μH, 15.4A	2920	Würth	74437529203330
2	R1, R9	2.2Ω	Resistor, 1%, 0603	0603	Yageo	RC0603FR-072R2L
2	R2, R8	10k Ω	Resistor, 1%, 0603	0603	Yageo	RC0603FR-0710KL
1	R3	3.3Ω	Resistor, 1%, 0603	0603	Yageo	RC0603FR-073R3L
3	R4, R5, R6	10Ω	Resistor, 1%, 0603	0603	Yageo	RC0603FR-0710RL
1	R10	0Ω	Resistor, 1%, 0603	0603	Yageo	RC0603FR-070RL
2	R11, R12	100kΩ	Resistor, 1%, 0603	0603	Yageo	RC0603FR-07100KL
1	R7	NC				
1	U1	MP1930	75V, 10A integrated Half-bridge power stage	QFN-26 (7mmx7mm)	MPS	MP1930GQN

EVB TEST RESULTS

Performance curves and waveforms are tested on the evaluation board. $V_{IN} = 48V$, $I_{OUT} = 10A$, $T_A = 25^{\circ}C$, unless otherwise noted.

Thermal Performance

$V_{IN} = 48V$, $V_{DD} = 12V$, $I_{OUT} = 10A$,
 $f_{SW} = 20kHz$, no forced airflow,
 $T_{CASE} = 95.7^{\circ}C$



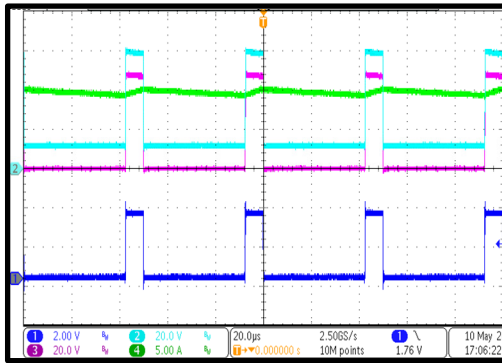
EVB TEST RESULTS (continued)

Performance curves and waveforms are tested on the evaluation board. $V_{DD} = 12V$, $f_{SW} = 20kHz$, $T_A = 25^{\circ}C$, unless otherwise noted.

Steady State and Output Voltage Ripple

$V_{IN} = 48V$, $I_{OUT} = 10A$

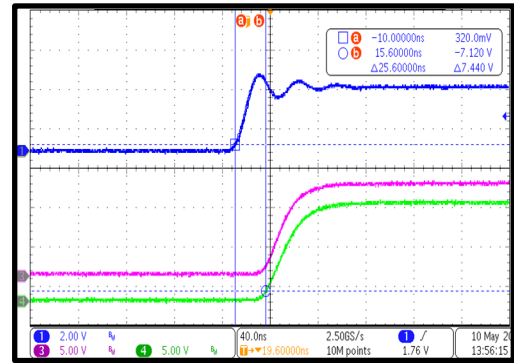
CH4: I_{OUT}
5A/div.
CH2: BST
20V/div.
CH3: SW
20V/div.
CH1: INH
2V/div.



Turn-On Propagation Delay and Drive Rising Time

CH1: INL/INH
2V/div.

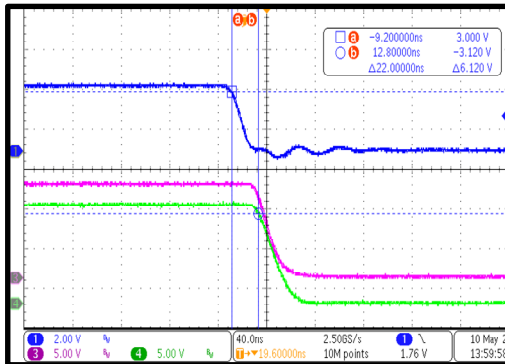
CH3: DRVH
5V/div.
CH4: DRVL
5V/div.



Turn-Off Propagation Delay and Drive Falling Time

CH1: INL/INH
2V/div.

CH3: DRVH
5V/div.
CH4: DRVL
5V/div.



PCB LAYOUT

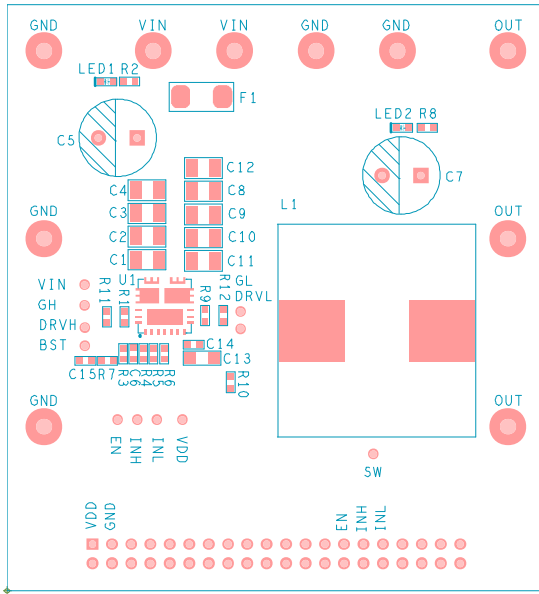


Figure 3: Top Silk

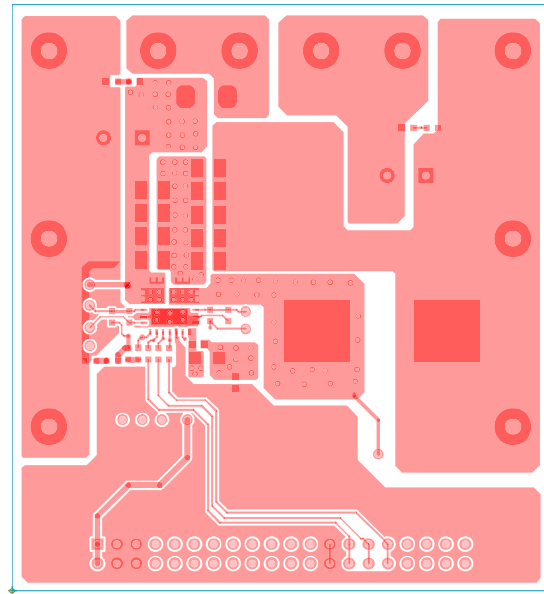


Figure 4: Top Layer

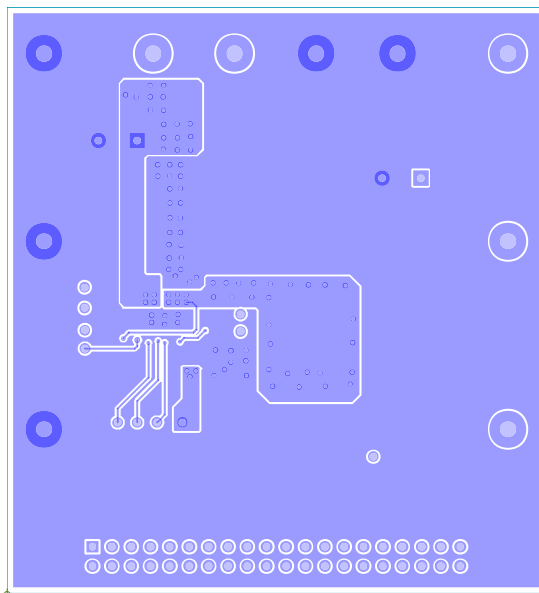


Figure 5: Bottom Layer

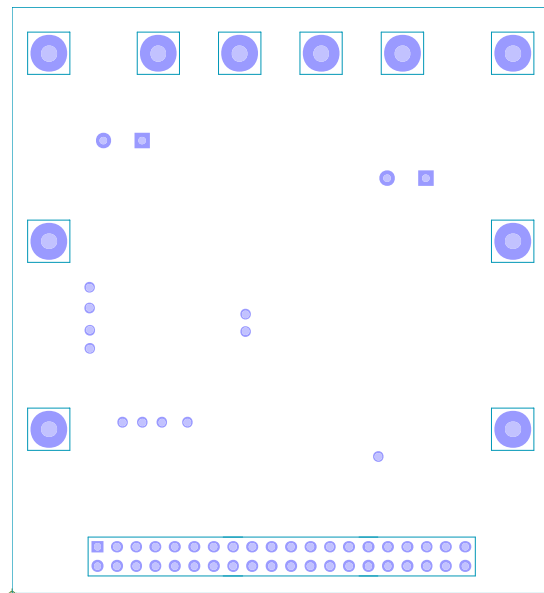


Figure 6: Bottom Silk

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	3/19/2024	Initial Release	-

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