EV18811-4X-S-00A

Isolated Single-Channel Gate Driver Evaluation Board

DESCRIPTION

The EV18811-4X-S-00A is an evaluation board designed to demonstrate the capabilities of the MP18811, a single-channel isolated gate driver solution for driving power switching devices with a short propagation delay and minimal pulse-width distortion.

By utilizing MPS's proprietary capacitive-based isolation technology, the SOIC narrow-body package option can provide up to 3kV$_{RMS}$ withstand voltage (per UL 1577). It can also provide a common-mode transient immunity (CMTI) rating above 100kV/μs between the input side and output driver. These advanced features enable high efficiency, high power density, and robustness in a wide variety of power applications.

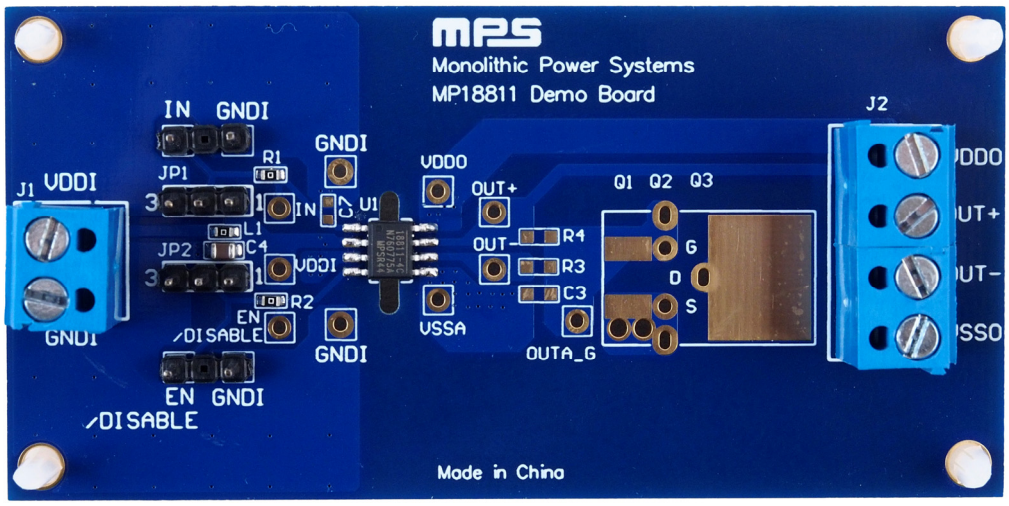
It is recommended to read the MP18811 datasheet prior to making any changes to EV18811-4X-S-00A.

PERFORMANCE SUMMARY

Specifications are at T_A = 25°C, unless otherwise noted.

Parameters	Conditions	Value
VDDI primary supply voltage (V_{DDI} - V_{GNDI})		2.8V to 5.5V
VDDO secondary supply voltage (V_{DDO} - V_{SSO})	-A version, 3V under-voltage lockout (UVLO) threshold	4.2V to 30V
	-B version, 5V UVLO threshold	6.5V to 30V
	-C version, 8V UVLO threshold	9.2V to 30V
	-E version, 12V UVLO threshold	14.5V to 30V
Peak driver current (I_{OUT})		4A source, 4A sink

EVALUATION BOARD



LxWxH (6.7cmx4.3cmx1.6mm)

Board Number	MPS IC Number
EV18811-4X-S-00A	MP18811-4XGS

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EVALUATION BOARD BASIC INFORMATION

Evaluation Board Part Number (1) (2)	Output UVLO (V)	On/Off Logic	Input Logic	Configuration	IC Package Type
EV18811-4A-S-00A	3	EN	IN	Single	SOIC-8 NB
EV18811-4B-S-00A	5				
EV18811-4C-S-00A	8				
EV18811-4E-S-00A	12				

Notes:

1) Contact MPS sales or our distributors to check the latest availability status for each part number.
2) These evaluation boards can only be ordered as a customized board though the MPS CSR team.

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QUICK START GUIDE

Jumper Setting Options

Jumper #	Jumper Name	Jumper Options		Default Setting
JP1	IN	Option A	Jumper cap not installed. The IN pin is controlled by an external signal and is default low if left open.	Option A
		Option B	Jumper cap on connection points 2 and 3, short IN to GNDI to set the IN pin to logic low.	
		Option C	Jumper cap on connection points 2 and 1, short IN to VDDI to set the IN pin to logic high.	
JP2	EN	Option A	Jumper cap not installed. The IC is enabled when the EN pin is left open.	Option C
		Option B	Jumper cap on connection points 2 and 3, short EN to GNDI.	
		Option C	Jumper cap on connection points 2 and 1, short EN to VDDI.	

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QUICK START GUIDE *(continued)*

The EV18811-4X-S-00A evaluation board is easy to set up and use to evaluate the performance of the MP18811. To get started, follow the steps below:

1. Select the desired jumper setting using the table on page 3.
2. Prepare two DC power supplies (A and B), whose outputs must be insulated from each other.
3. Preset power supply A to 2.8V ≤ V_{DDI} - V_{GNDI} ≤ 5.5V. If the chip is controlled by external signals, ensure that V_{DDI} is not below the high-level of these signals.
4. Turn off power supply A.
5. Preset power supply B to 4.2/6.5/9.2/14.5V ≤ V_{DDO} - V_{SSO} ≤ 30V (according to the UVLO threshold)., then turn off power supply B.
6. If needed, connect OUT to an external load.
7. Connect power supply A's output to J1.
8. Connect power supply B's output to J2.
9. After making the connections, turn both DC power supplies (A and B) on.
10. If needed, enable the external control signals.

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EVALUATION BOARD SCHEMATIC

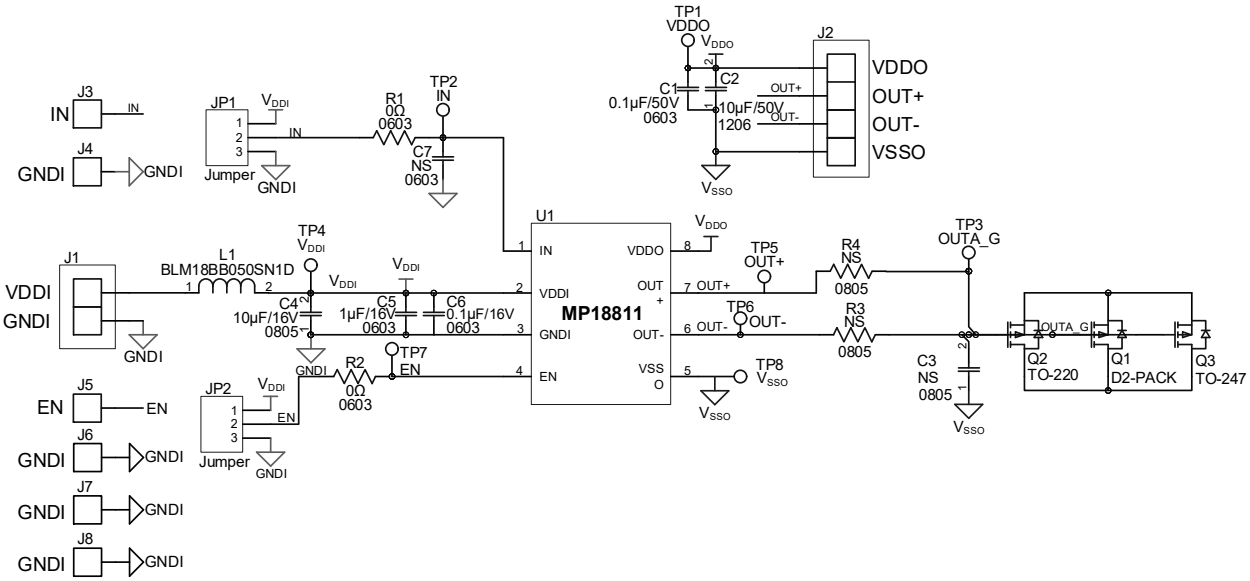

Figure 1: Evaluation Board Schematic

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EV18811-4X-S-00A BILL OF MATERIALS

Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
1	C1	0.1µF	Ceramic capacitor, 50V, X7R	0603	Murata	GCM188R71H104KA57D
1	C2	10µF	Ceramic capacitor, 50V, X7T	1206	Murata	GRM31CD71H106KE11L
1	C4	10µF	Ceramic capacitor, 16V, X7R	0805	Murata	GRM21BC71C106KE11L
1	C5	1µF	Ceramic capacitor, 16V, X7R	0603	Murata	GRM188R71C105KA12D
1	C6	0.1µF	Ceramic capacitor, 16V, X7R	0603	Murata	GRM188R71C104KA01D
1	C7	NS		0603		
1	C3	NS		0805		
6	J3, J4, J5, J6, J7, J8	2.54mm	2.54mm pin header	SIP	Any	
1	J1	5.08mm	Connection terminal block, 2 positions	Through-hole	Any	
1	J2	5.08mm	Connection terminal block, 4 positions	Through-hole	Any	
2	JP1, JP2	2.54mm	Pin header with jumper cap	SIP	Any	
1	L1	50mΩ	Ferrite bead, 5Ω at 100MHz, 700mA	0603	Murata	BLM18BB050SN1D
1	Q1	NS		D2-PACK		
1	Q2	NS		TO-220		
1	Q3	NS		TO-247		
2	R1, R2	0Ω	Thick film chip resistor, 5%	0603	Yageo	RC0603JR-070RL
2	R3, R4	NS		0805		
8	TP1 to TP8	2.5mm	Test point	Through-hole	Any	
1	U1	MP18811	Single-channel isolated gate driver	SOIC-8 NB	MPS	MP18811-4XGS

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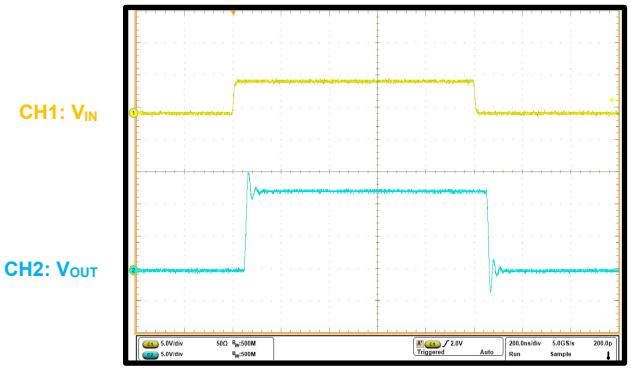
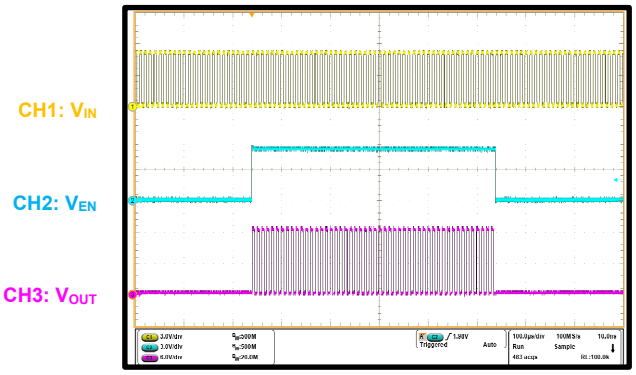
EVB TEST RESULTS

Performance waveforms are tested on the MP18811 evaluation board. V_{DDI} - V_{GNDI} = 5V, V_{DDO} - V_{SSO} = 12V, C_{LOAD} = 0pF, T_A = 25°C, all voltages with respect to the corresponding ground(s), unless otherwise noted.

Typical Switching Waveform



EN Control



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PCB LAYOUT

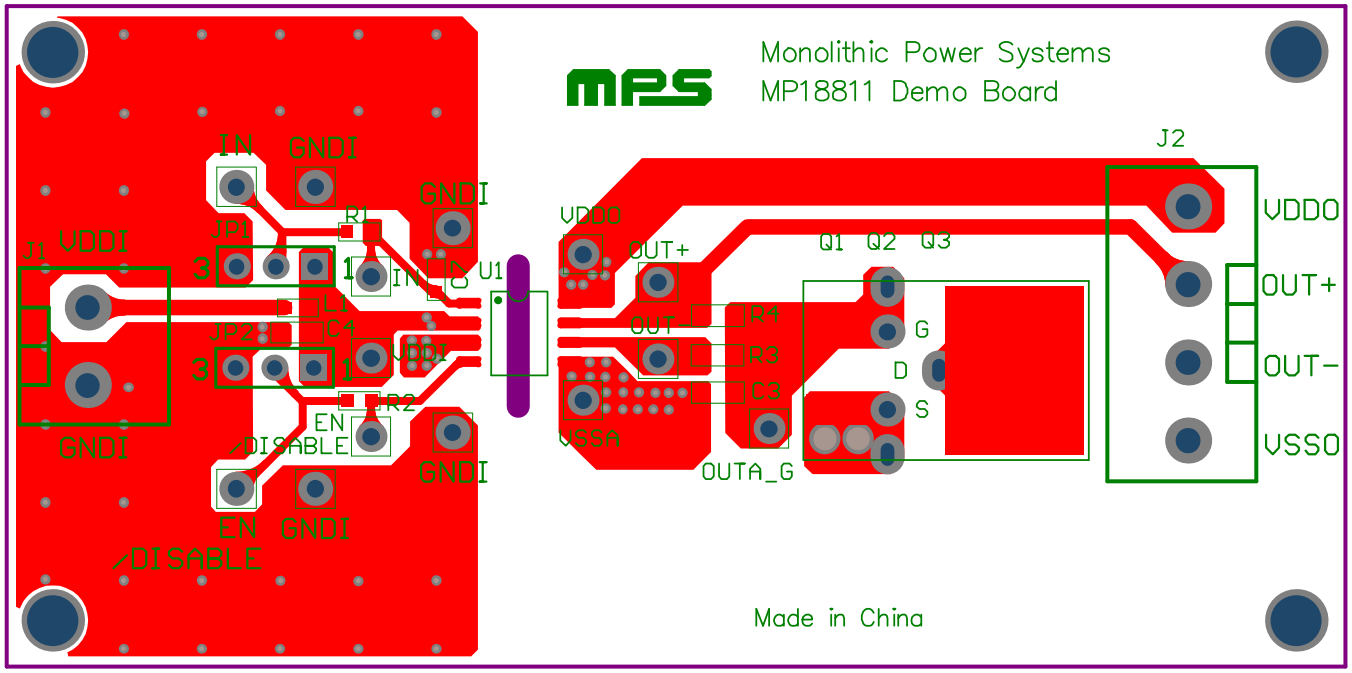

Figure 2: Top Silk and Top Layer

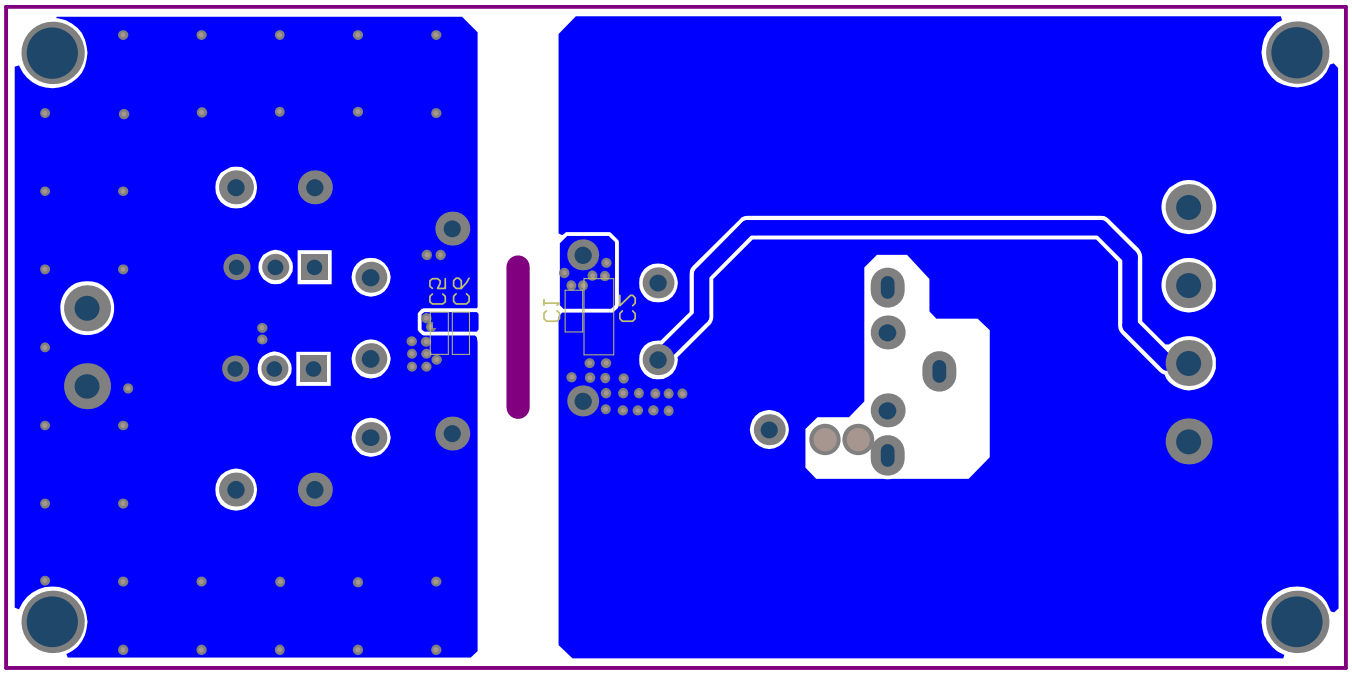

Figure 3: Bottom Layer and Bottom Silk

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REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	3/18/2024	Initial Release	-

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