



EV05W0505B-YE-00A

5V, 0.5W, Regulated, 3kV_{RMS}
Isolated DC/DC Module
Evaluation Board

DESCRIPTION

The EV05W0505B-YE-00A is an evaluation board designed to demonstrate the capabilities of the MIE05W0505BGYE, an isolated, regulated DC/DC module. It can support 3V to 5.5V input voltage (V_{IN}) applications. The MIE05W0505BGYE has excellent load regulation, line regulation, and supports up to 0.5W of output power (P_{OUT}).

The MIE05W0505BGYE uses capacitive isolation technology for the feedback block, which can regulate the output voltage (V_{OUT}) without a traditional optocoupler and precision-

configurable reference IC. This module is a small solution that provides highly reliable operation when compared to traditional isolation power modules.

The MIE05W0505BGYE features continuous short-circuit protection (SCP) and over-temperature protection (OTP). It is available in a small SOIC-8 wide body (WB) package.

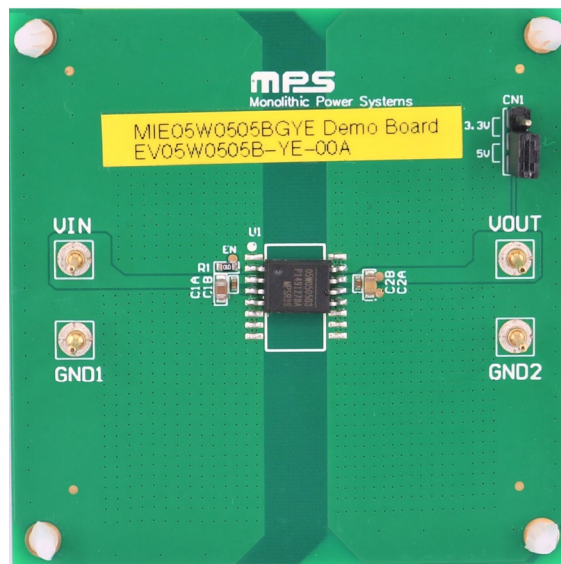
It is recommended to read the datasheet for the MIE05W0505BGYE prior to making any changes to the EV05W0505B-YE-00A.

PERFORMANCE SUMMARY

Specifications are at $T_A = 25^\circ\text{C}$, unless otherwise noted.

Parameters	Conditions	Value
Input voltage (V_{IN}) range	$V_{OUT} = 5\text{V}$	4.5V to 5.5V
	$V_{OUT} = 3.3\text{V}$	3V to 5.5V
Output voltage (V_{OUT})	$I_{OUT} = 0\text{A}$ to 0.1A	5V
Maximum output current (I_{OUT})	$V_{IN} = 4.5\text{V}$ to 5.5V	0.1A
Typical efficiency	$V_{IN} = 5\text{V}$, $V_{OUT} = 5\text{V}$, $I_{OUT} = 0.1\text{A}$	46%

EVALUATION BOARD



LxWxH (6.4cmx6.4cmx0.2cm)

Board Number	MPS IC Number
EV05W0505B-YE-00A	MIE05W0505BGYE-3R

QUICK START GUIDE

The board's output voltage is set to 5V by default. To quick start the EV05W0505B-YE-00A, refer to Figure 1 and follow the steps below:

1. Preset the power supply (V_{IN}) to be $4.5V \leq V_{IN} \leq 5.5V$.
2. Turn off the power supply.
3. Connect the power supply terminals to:
 - a. Positive (+): V_{IN}
 - b. Negative (-): GND1
4. Connect the load terminals to:
 - a. Positive (+): V_{OUT}
 - b. Negative (-): GND2
5. After making the connections, turn on the power supply. The board should automatically start up.
6. To use the enable function, apply a digital input to the EN pin. Drive EN above 2V to turn on the EV05W0505B-YE-00A; drive EN below 0.4V to turn it off.
7. Set the output voltage (V_{OUT}) to 3.3V by moving the jumper from the 5V selection to the 3.3V selection on CN1. V_{IN} should start up.

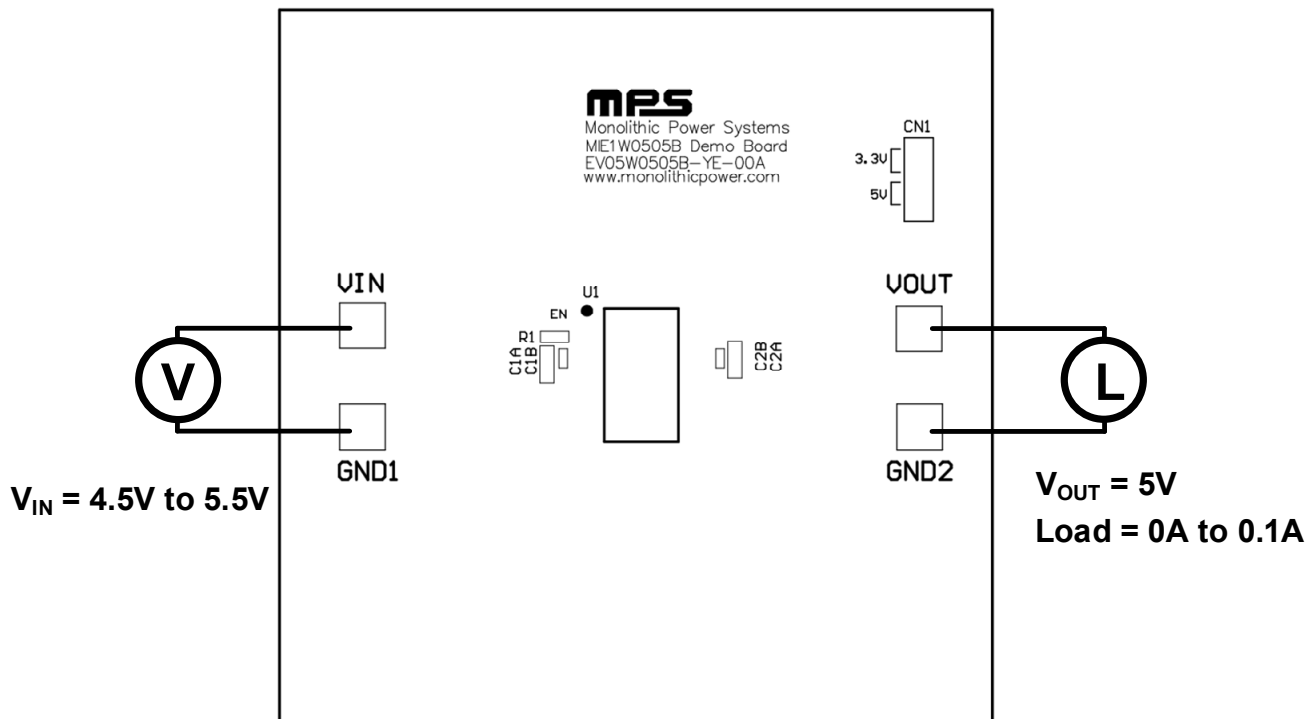


Figure 1: Measurement Equipment Set-Up

EVALUATION BOARD SCHEMATIC

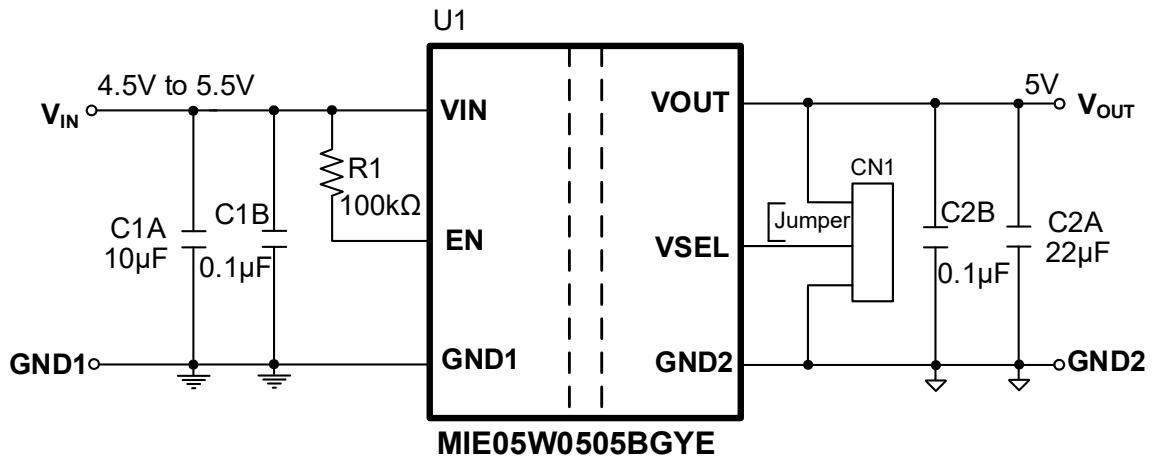


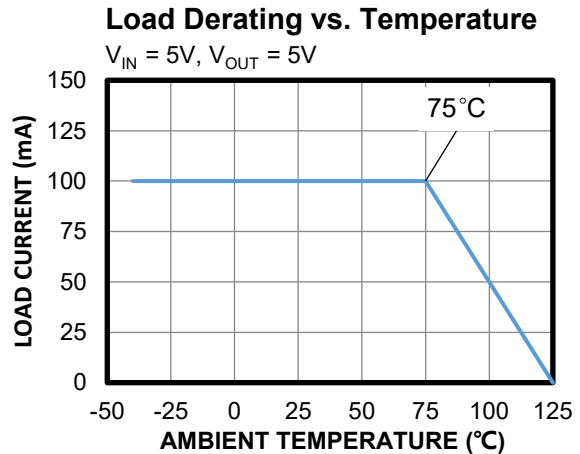
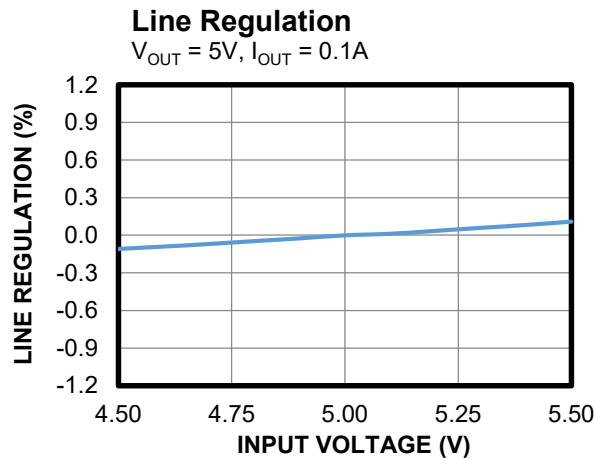
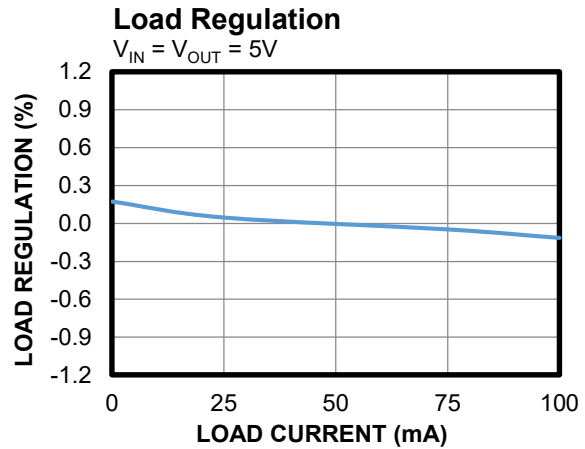
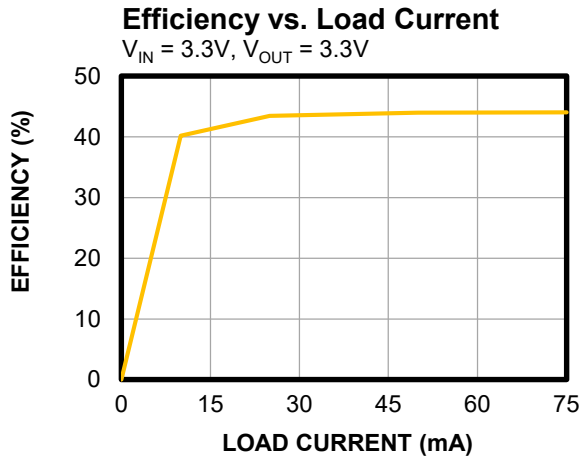
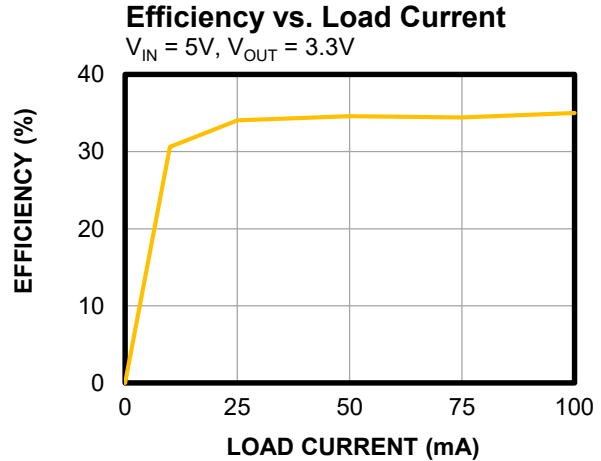
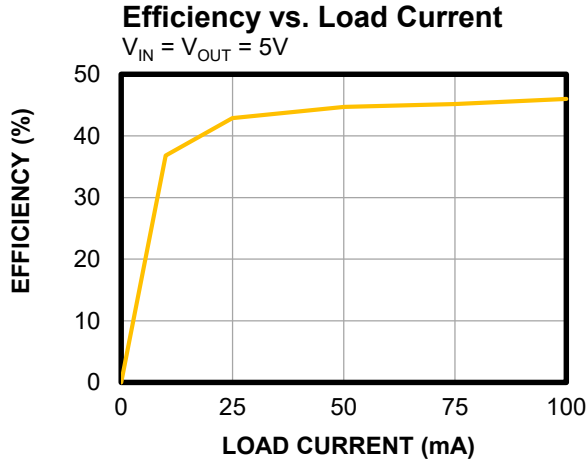
Figure 2: Evaluation Board Schematic

EV05W0505B-YE-00A BILL OF MATERIALS

Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
1	C1A	10 μ F	Ceramic capacitor, 10V	0805	Murata	GRM21BR71A106KA73L
1	C2A	22 μ F	Ceramic capacitor, 10V	0805	Würth	885012107011
2	C1B, C2B	0.1 μ F	Ceramic capacitor, 16V	0402	Murata	GRM155R71C104KA88D
1	R1	100k Ω	Film resistor, \pm 1%	0603	Yageo	RC0603FR-07100KL
1	CN1	3-pin	Header, 3-pin	SIP	Würth	61300311121
1	U1	MIE05W0505BGYE	5V, 3kV _{RMS} isolated DC/DC module	SOIC-8 WB	MPS	MIE05W0505BGYE-3R-Z

EVB TEST RESULTS

Performance curves and waveforms are tested on the evaluation board. $V_{IN} = 5V/3.3V$, $V_{OUT} = 5V/3.3V$, $C_{IN} = 0.1\mu F + 10\mu F$, $C_{OUT} = 0.1\mu F + 22\mu F$, $T_A = 25^\circ C$, unless otherwise noted.

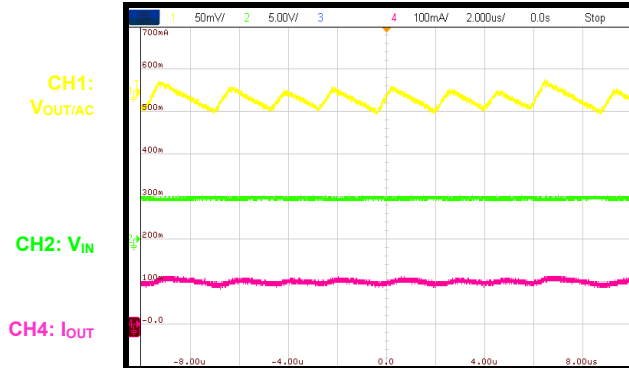


EVB TEST RESULTS (continued)

Performance curves and waveforms are tested on the evaluation board. $V_{IN} = 5V$, $V_{OUT} = 5V$, $C_{IN} = 0.1\mu F + 10\mu F$, $C_{OUT} = 0.1\mu F + 22\mu F$, $T_A = 25^\circ C$, unless otherwise noted.

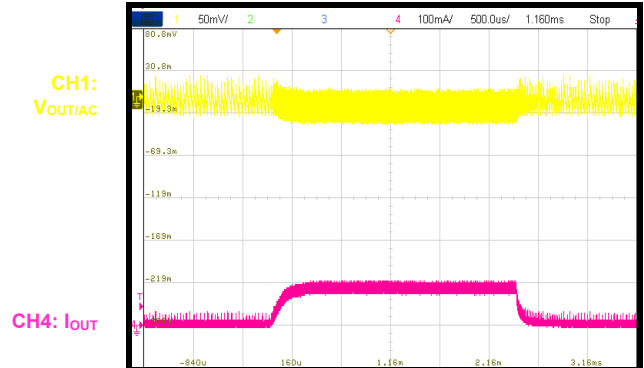
Output Voltage Ripple

$I_{OUT} = 0.1A$



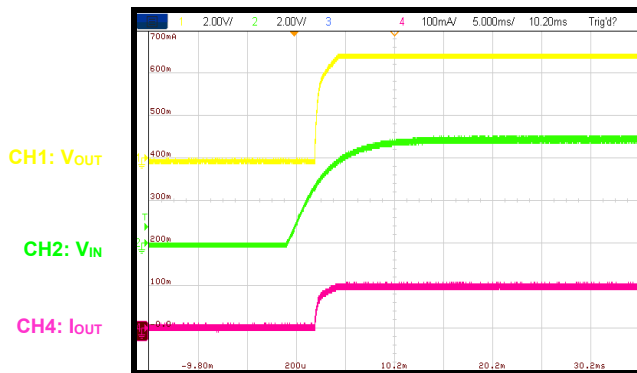
Load Transient Response

$I_{OUT} = 0A$ to $0.1A$



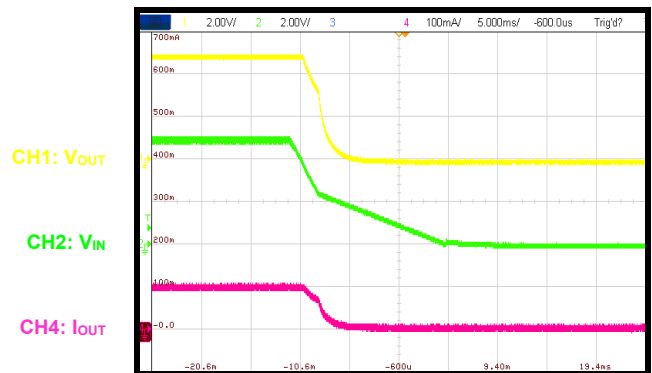
Start-Up through VIN

$I_{OUT} = 0.1A$



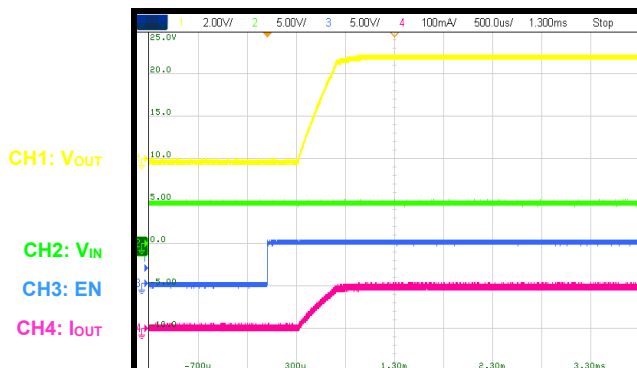
Shutdown through VIN

$I_{OUT} = 0.1A$



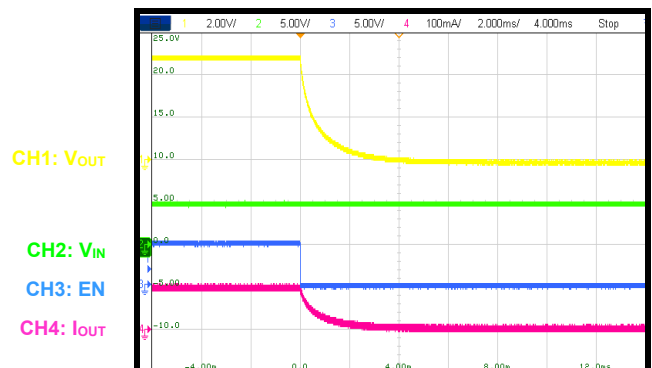
Start-Up through EN

$I_{OUT} = 0.1A$



Shutdown through EN

$I_{OUT} = 0.1A$



PCB LAYOUT

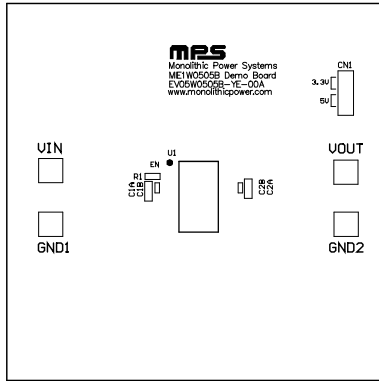


Figure 3: Top Silk

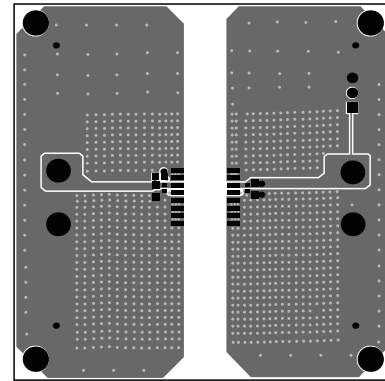


Figure 4: Top Layer

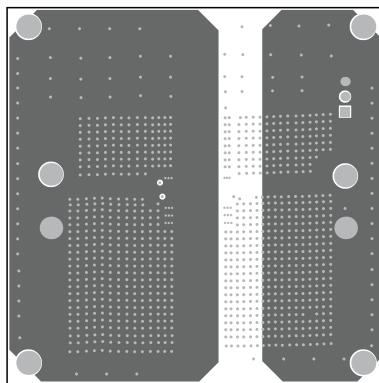


Figure 5: Mid-Layer 1

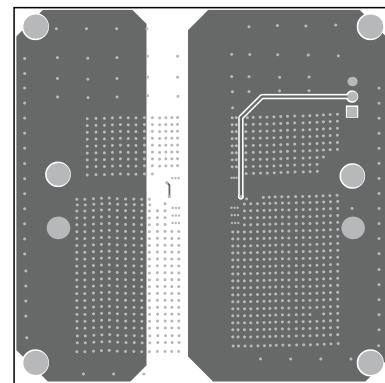


Figure 6: Mid-Layer 2

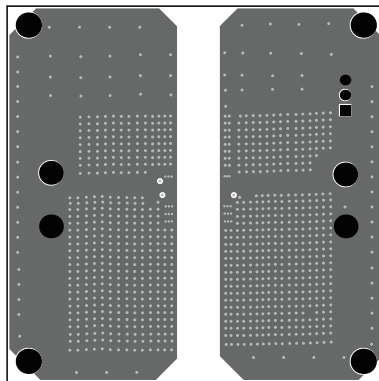


Figure 7: Bottom Layer

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	5/21/2024	Initial Release	-

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