Surface-Mount Guidelines

MPM Power Modules with QFN Packages

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Overview

Introduction

This document provides the guidelines for the surface-mount of MPS power module products with QFN packages during the SMT assembly process, to help customers apply MPS power modules in various board-level systems in a reliable, efficient, assembly-friendly way.

Quad flat no-leads (QFN) is a leadless, plastics-encapsulated package with copper lead frame as substrate. All QFNs are leadless packages where the connection is made through the leads (terminal pins) and exposed pads on the bottom surface of the package. These leads and exposed pads can be directly soldered onto the PCB. The benefits of QFN packages include:

- Small footprint per I/O, resulting in significant PCB space savings
- Superior electrical and thermal performance compared to leaded plastic packages
- Utilizes standard surface-mount assembly technology

This guideline for the surface-mount process of MPS power module products in QFN packages covers land pattern pad design, stencil design, solder paste selection, PCB surface finish selection, the solder paste printing process, reflow and rework, and more.

Scope

This note contains generic information to improve the surface-mount process for MPS power modules in QFN packages. Specific information about each device is not provided. To develop an optimized assembly process and application design for a specific device, additional information and development details are required based on the individual device requirements, industry standards such as IPC and JEDEC, and relevant practices in the assembly environment. Contact an MPS FAE for further assistance.

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Section 1. QFN Package Land Pattern

The land pattern of a QFN package is based on the product's pin out. To help facilitate design with MPS power module products at the system level, refer to the detailed land pattern design for each individual power module, located in the product's datasheet. This section focuses on PCB pad design configurations, including the solder mask defined pad, non-solder mask defined pad, and via-in-pad design. A power module product PCB design is used as an example to demonstrate recommendations regarding pad design.

1.1 SMD Pad Design

A solder mask defined (SMD) pad design features a solder mask layer partially laying on the edge of the PCB pad (see Figure 1). The solder mask opening is slightly smaller than the pad size, which creates an overlay area between the solder mask layer and the pad layer. SMD pad design offers several benefits. First, the overlapping solder mask helps prevent the pads from lifting off of the PCB surface due to thermal or mechanical stress. Secondly, SMD pad design helps to better align solder paste on the pad during the assembly process. However, SMD pad design also presents drawbacks, namely that the overlapping area creates additional interfaces, which is not good for thermal-mechanical stress management during system-level application.

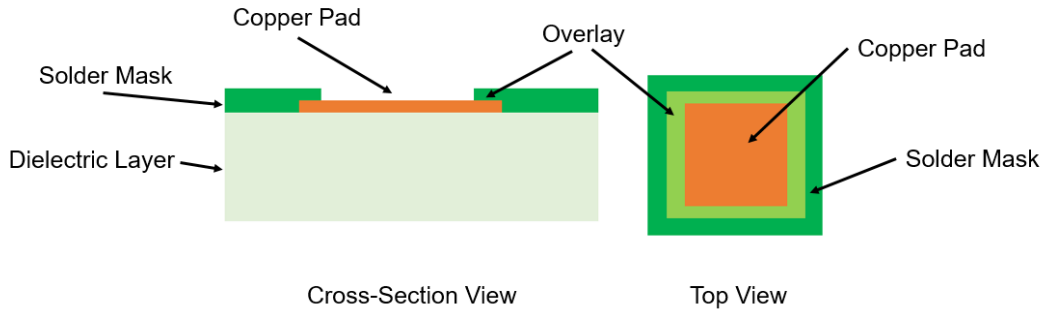

Figure 1: SMD Pad Design Illustration

1.2 NSMD Pad Design

For a non-solder mask defined (NSMD) pad, the solder mask layer is designed with a gap between the solder mask and copper pad (see Figure 2). With this pad type, the copper pad area for solder paste printing is only defined by the dimension of copper pad itself, not by the solder mask. Since NSMD pads have all the solder pasted connected to the entire pad, NSMD pad designs feature better solder connections and solder joint reliability. However, the pad also tends to be easier to lift off from the PCB during assembly or under special operation conditions.

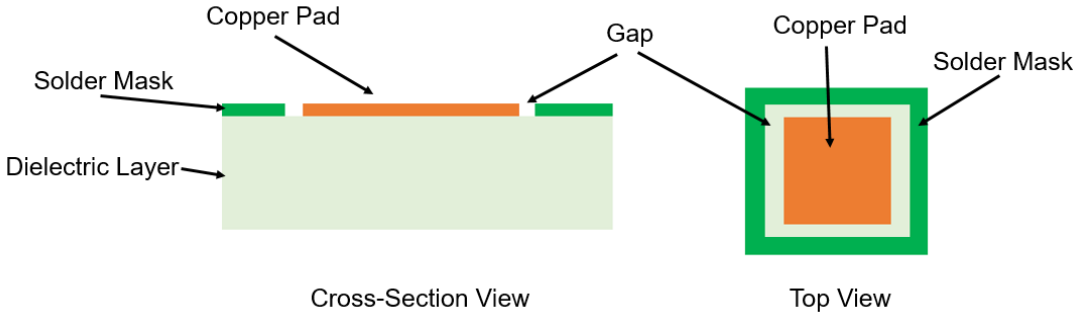

Figure 1: NSMD Pad Design Illustration

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1.3 Via-in-Pad Design

To achieve better thermal management and electrical functions, through vias or buried vias are typically placed underneath the copper pad on the PCB; this is known as “via-in-pad” design. Via-in-pad design has impacts on the PCBA process, such as the solder paste print.

Open thermal vias can be placed directly under the pad. There are multiple options to achieve better soldering performance:

1. Move the via under the area covered by the solder mask, if the thermal and electrical performance is not significantly affected.
2. Fill the vias with copper, epoxy, or other equivalent materials. Note that this approach may increase the cost of PCB manufacturing.

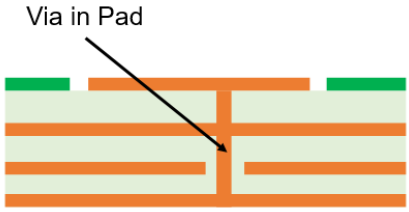

Figure 3: Via-in-Pad Design Illustration

1.4 Pad Design Recommendation for MPM Products in LGA Packages

NSMD is preferable because it offers better control of the copper etching process compared to the solder masking process. In addition, the SMD pad definition can introduce stress concentrations near the solder mask overlap region, which can result in solder joints cracking under extreme fatigue conditions. Using NSMD instead improves the reliability of solder joints, as solder can wrap around the sides of the metal pads on the board.

For these reasons, NSMD is recommended for the perimeter I/O lands, and is typically also recommended for the thermal land. However, SMD should be used on the thermal land when it is relatively large.

Section 2. Stencil Design

The stencil design is important for the assembly process of QFN-based MPS power modules, as it controls the thickness and volume of solder paste applied on each LGA pad. Various processes and key parameters must be taken care as part of the stencil design. Stencils are typically made of stainless steel.

The stencil thickness and pattern geometry determine the precise volume of solder paste deposited onto the device's land pattern. Stencil alignment accuracy and consistent solder volume transfer are critical for uniform solder reflow. Stainless steel stencils are preferred. The stencil should be laser-cut and then electropolished for better release than a standard laser-cut stencil. In addition, rounded corners and a trapezoidal cross-section enhance the release of solder paste form the aperture.

For I/O lands, stencil recommendations are as follows:

- 5mils stencil thickness: The stencil aperture opening should be 1mil/side smaller than the PCB pad size.
- 4mils stencil thickness: The stencil aperture opening should be 1:1 to the PCB pad size.

For thermal land, the larger the solder paste coverage area at the end of the thermal pad, the more likely it is to cause solder defects such as void, solder paste splash, and solder ball. To reduce the solder paste volume on the thermal land, it is recommended that an array of smaller apertures be used instead of one

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large aperture. The smaller apertures can be circular or square, and of various dimensional combinations so long as they result in 50% to 80% solder paste coverage.

Section 3. Solder Paste Recommendation

A low-residue, no-clean solder paste is commonly used in mounting QFN packages, a Type 3 (or finer) solder paste is recommended. A SAC305 solder alloy is also highly recommended, and nitrogen purge is recommended during solder reflow.

Section 4. PCB Surface Finish

PCB manufacturing is typically capable of various surface finishes based on the use requirements. Options include:

- OSP (organic solderability preservative)
- ENIG (electroless nickel, immersion gold)
- Electroplated nickel and gold
- Immersion silver
- Immersion tin

The design engineer can choose their preferred surface finish based on the system requirements. MPS recommends using OSP, ENIG, and immersion tin for the best results.

Section 5. Solder Paste Printing and Component Placement

5.1 Solder Paste Printing

During the solder paste printing process, an automatic or manual stencil printer can be used to distribute the solder paste onto the PCB lands. A design of experiment (DOE) should always be used to establish optimal printing parameters.

5.2 Component Placement

The placement of QFN components is important for good assembly quality. It is recommended to use an automatic pick-and-place machine with a vision system. The accuracy for component placement should be adjusted to ±30μm.

5.3 Reflow Assembly

The set reflow profile must satisfy JEDEC standards. The JEDEC reflow profile sets different stages of SMT heating during component board assembly. Each stage has a minimum and maximum temperature range and time value range, which are used as guidelines for optimizing the temperature profile associated with the specific printed circuit assembly. Keep in mind that each assembly is customized and requires a unique reflow profile to achieve nominal results over the entire board. For more details, refer to the IPC/JEDEC J-STD-020D standard.

The actual profile parameters also depend upon the solder paste used. Recommendations from paste manufacturers should be followed. The reflow profile guidelines are based on the temperature at the lead to PCB land pad solder joint location. The actual temperature of the solder joint is often different than the temperature settings in the reflow system.

Figure 4 on page 7 shows the typical recommended reflow profile.

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MPS Recommended IR Reflow Temperature Profile

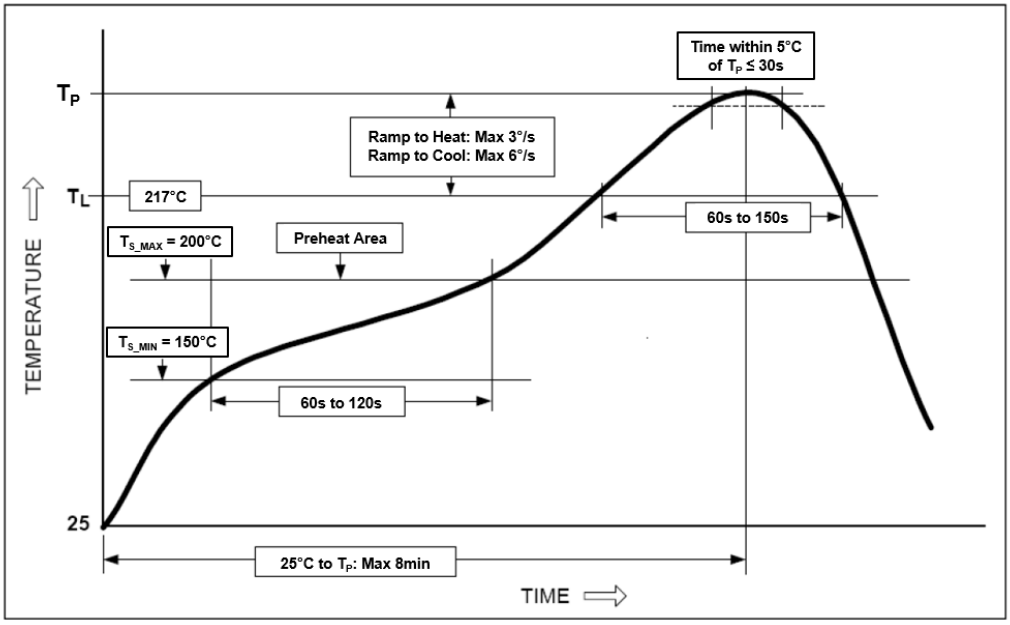

Figure 4: Typical Recommended Reflow Profile

Table 1 summarizes the typical reflow profile parameters. The recommended profile and parameters meet IPC/JEDEC J-STD-020 specifications.

Table 1: Typical Peak Reflow Temperature for Lead-Free Recommended Assembly Process

Package Thickness	Volume <350mm^3	Volume 350mm^3 to 2000mm^3	Volume >2000mm^3
<1.6mm	≤260°C	≤260°C	≤260°C
1.6mm to 2.5mm	≤260°C	≤250°C	≤245°C
>2.5mm	≤250°C	≤245°C	≤245°C

5.4 Cleaning

Since no-clean solder paste is typically used for MPS power modules in QFN packages, no cleaning procedure is required for MPS power module products.

If water-soluble paste has been used for an MPS power module, it is recommended to use a saponifier and/or deionized (DI) water spray system for the cleaning process. After cleaning, be sure to dry the board.

Refer to and follow the solder paste supplier's guidelines for cleaning.

5.5 Inspection

Post-reflow inspection of QFNs on PCBs is typically accomplished by using transmission X-ray and AOI equipment. X-rays can be used for reflow process monitoring and as a failure analysis tool.

A 2D X-ray system with an oblique view at highest magnification (OVHM) is highly recommended, as it can detect solder bridge, opens, and voids. As with any leaded package technology, the separation method is to either punch or saw off QFN packages. Therefore, the edges of the leads have bare copper exposed. Lack of solder wetting in this area is not considered a criterion for visual inspection/rejection.

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Section 6. Rework

Since QFN package-based parts are not easy to handle, directly repairing failed solder joints is not recommended. An appropriate rework station should be used for any rework on the parts.

6.1 Pre-Rework

Before the rework, identify the failure(s) and/or defect(s) of the part.

Bake the board with the failed QFN part for at least 4 hours at 125°C before removing MPS power modules. This helps prevent delamination of the molding compound from substrate of the part. It also helps prevent damage to the adjacent parts on the board.

6.2 Component Removal

It is recommended that the board be heated from the bottom side using convective heaters, and hot air should be used on the top side of the component. To melt the solder joints on the QFN package part, keep the bottom temperature as low as possible but ensure that the solder has reached its liquidation temperature.

Any removed components should not be used.

6.3 Site Redress

After the part is removed, remove any residual solder material with an appropriate vacuum nozzle or solder wick braid, and clean the site with appropriate liquid. IPA is recommended for this use.

6.4 Solder Paste Printing

The solder paste must be printed on the PCB pads for removed parts. If possible, use a mini-stencil designed specifically for the relevant part to print solder paste with similar parameters. If a mini-stencil is not available, a normal solder dispensing system can also be used, but the operator must pay attention to the volume of solder paste while dispensing.

6.5 Placement and Reflow of New Component

The new component must be handled following the MSL guidelines according to the J-STD-033 standard.

The reflow profile for the reworked component(s) must ensure adequate soaking time, as well as time above the melting point of the solder paste. Profile the temperature with thermocouples.

After the component is soldered, inspect the solder joints using an X-ray or other vision system.

The temperature profile applied at the component must never exceed the maximum temperature based on J-STD-020 standards.

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REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	12/14/2021	Initial Release	-

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