



AN139

MP5416

Optimizing Output Voltage Selection

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Optimizing Output Voltage Selection

Application Note

Prepared by MPS Standard DC/DC Product Line

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TABLE OF CONTENTS

ABSTRACT3

INTRODUCTION3

OUTPUT VOLTAGE SELECTION GUIDE4

DESIGN EXAMPLE6

ABSTRACT

This application note introduces the operation of the [MP5416](#) clock, constant-on-time (COT) control mode, and discusses the relationship between the output voltage and steady state. This application note also describes how to select an appropriate output voltage for each channel.

This application note optimizes design by allocating V_{OUT} reasonably to ensure that the [MP5416](#) has the best performance.

INTRODUCTION

Operation of the [MP5416](#) Clock

The [MP5416](#) is a complete power management solution that integrates four high-efficiency, step-down, DC/DC converters, five low-dropout regulators, and a flexible logic interface. The [MP5416](#) employs out-of-phase synchronization to minimize the input ripple and reduce interference among each power rail during continuous conduction mode (CCM) operation. From Buck 1 to Buck 4, there is a sequential phase delay between each output (see Figure 1). The clock phase delay is 90° from Buck 1 to Buck 4, Buck 4 to Buck 2, Buck 2 to Buck 3, and Buck 3 to Buck 1. The steady state is made stable by using out-of-phase synchronization (see Figure 2).

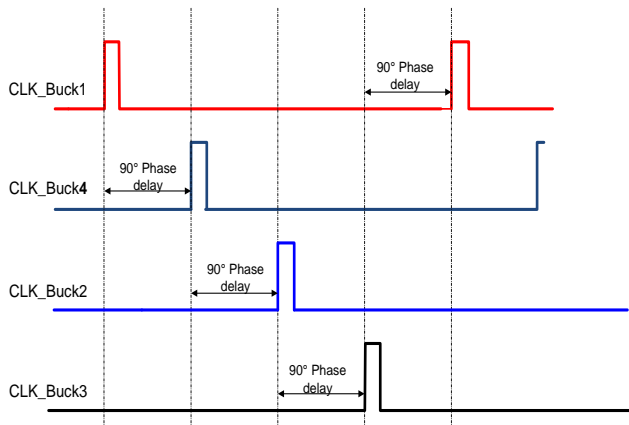


Figure 1: [MP5416](#) Clock Sequence

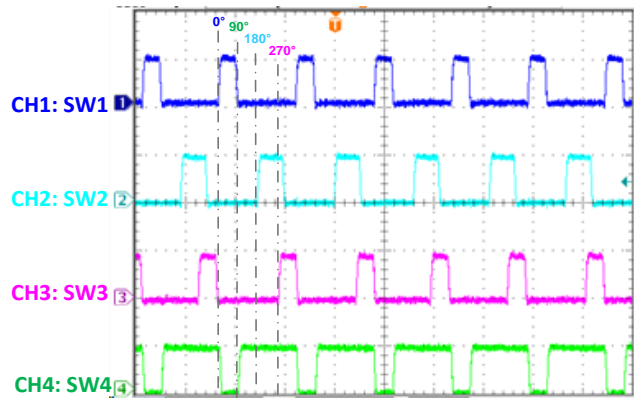


Figure 2: [MP5416](#) Steady State Waveform

Control Method of the [MP5416](#)

The [MP5416](#) adopts a constant-on-time (COT) control scheme to achieve reduced output overshoot and undershoot during load transient. The COT buck circuit diagram is shown in Figure 3. The feedback (FB) reference voltage (V_{REF}) is compared against $FB + V_{RAMP}$. The regulator turns on for a period (T_{ON}) when $FB + V_{RAMP} < V_{REF}$. V_{RAMP} is proportional to the output voltage, as shown in Equation (1):

$$V_{RAMP} = \frac{1-D}{R4 \cdot C4} \cdot V_{out} \cdot t_{sw} \quad (1)$$

Where t_{sw} is the switching period, D is the duty cycle period, and R4 and C4 refer to components in Figure 3.

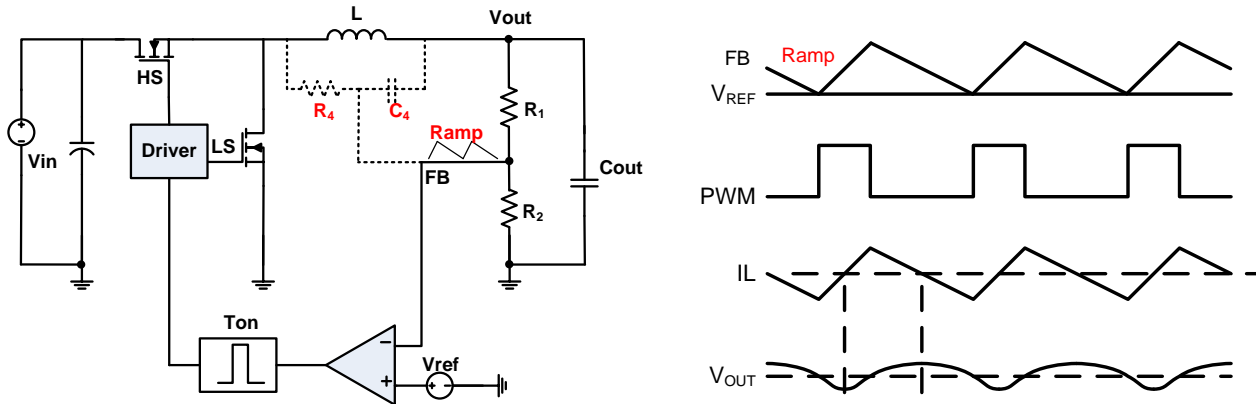


Figure 3: Circuit Diagram of COT Control and Operational Signal Diagram

OUTPUT VOLTAGE SELECTION GUIDE

COT control depends on the ramp of FB crossing V_{REF} to stabilize the system. Therefore, the ramp on FB should be large enough to reduce the jitter induced by the FB noise.

At T_0 , the SW1 falling edge is close to the SW4 rising edge. The SW1 falling edge may couple a negative voltage spike to Buck 4's FB signal. If this noise is larger than the ramp on FB4, Buck 4 SW4 will be turned on falsely. This can result in jitter on SW4 (see Figure 4).

To ensure proper phase-shift operation and to avoid interference, the falling switch node edge of regulator A can be delayed minimally from the rising switch node edge of regulator B if the V_{RAMP} signal of regulator B is sufficiently large. This implies that the output voltage of regulator B must be large enough to minimize interference.

If swapping the output voltages of Buck 2 and Buck 4, change the Buck 4 output voltage from 1V to 2.5V. For a 2.5V output voltage, the V_{RAMP} amplitude is larger. With the same FB voltage noise coupling, the Buck 4 stability will not be affected (see Figure 5).

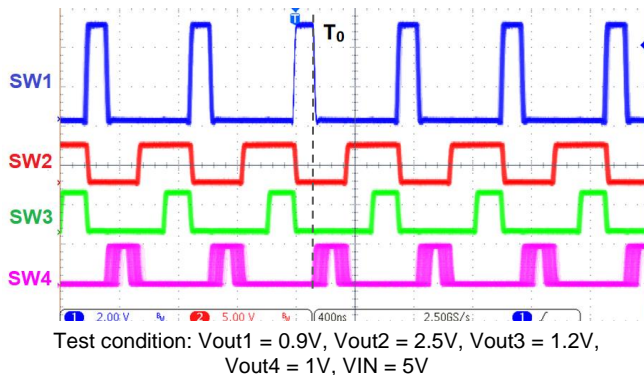


Figure 4: Unstable Waveform

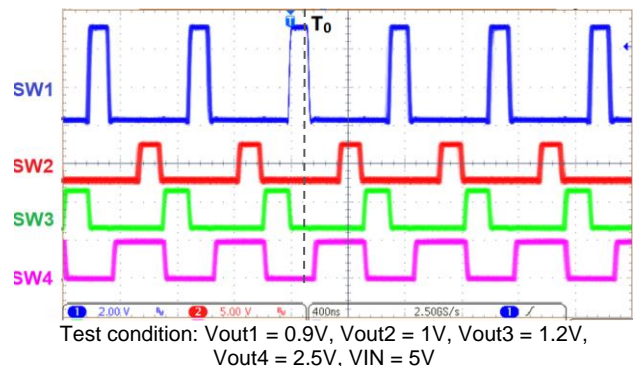


Figure 5: Stable Waveform

The [MP5416](#) evaluation GUI and output voltage selection Excel file can help users properly determine the output voltage selection for each buck converter. Please contact an MPS FAE for this GUI and Excel file. In the future, they will be available on the MPS website.

The image of the [MP5416](#) output voltage selection excel file is shown in Figure 6.

Notes:
 1. The SW operation frequency is 1.5MHz.
 2. Please choose the output voltage by the Filter Button, DO NOT fill out it.

ID	Buck1	Buck2	Buck3	Buck4	Result	Comment
1	0.9	0.9	0.9	1.2	OK	
2	0.9	0.9	0.9	1.3	OK	
3	0.9	0.9	0.9	1.5	OK	
4	0.9	0.9	0.9	2.5	OK	
5	0.9	0.9	0.9	3.3	OK	
6	0.9	0.9	1	1.2	OK	
7	0.9	0.9	1	1.3	OK	
8	0.9	0.9	1	1.5	OK	
9	0.9	0.9	1	2.5	OK	
10	0.9	0.9	1	3.3	OK	
11	0.9	0.9	1.1	1.2	OK	
12	0.9	0.9	1.1	1.3	OK	
13	0.9	0.9	1.1	1.5	OK	
14	0.9	0.9	1.1	2.5	OK	
15	0.9	0.9	1.1	3.3	OK	
16	0.9	0.9	1.2	1.2	OK	
17	0.9	0.9	1.2	1.3	OK	
18	0.9	0.9	1.2	1.5	OK	

5Vin 3.3Vin

Figure 6: MP5416 Output Voltage Selection Excel File

The [MP5416](#) evaluation GUI is only for users to filter the appropriate output voltage in the pre-design period. The GUI cannot program the IC. The image for the [MP5416](#) evaluation GUI is shown in Figure 7. Users can use the MP5416 I²C GUI to program the IC. This GUI cannot be used to filter the output voltage. The image for the [MP5416](#) I²C GUI is shown in Figure 8.

MP5416-5V POWER MANAGEMENT IC WITH I2C

Part Numbers Debug Tool Utility Help

ADDRESS:

REGISTER CONTROL:

BUCK1-BUCK4 CONTROL BIT

Input Voltage: 5V 3.3v

BUCK1(0X4)
 EN: Disable Buck1(0)
 Vout:

BUCK2(0X5)
 EN: Disable Buck2(0)
 Vout:

BUCK3(0X6)
 EN: Disable Buck3(0)
 Vout:

BUCK4(0X7)

Name	D7	D6	D5	D4	D3	D2	D1	D0
CTL0	SYSEN	SFRST	RESERVED			RESERVED		
CTL1	RESERVED	MODEBUCK1	MODEBUCK2	MODEBUCK3	MODEBUCK4	DISCHGBUCK3	DISCHGBUCK2	DISCHGBUCK1
CTL2	DVS SLEW RATE	DISCHGLDO2	DISCHGLDO3	DISCHGLDO4	DISCHGLDO5	RESERVED		
ILIMIT	ILIMBUCK1		ILIMBUCK3		ILIMBUCK2		ILIMBUCK4	
VSET1	ENBUCK1	BUCK1 OUTPUT VOLTAGE SET: 0.6V-2.1875V/12.5mV STEP						
VSET2	ENBUCK2	BUCK2 OUTPUT VOLTAGE SET: 0.8V-3.975V/25mV STEP						
VSET3	ENBUCK3	BUCK3 OUTPUT VOLTAGE SET: 0.6V-2.1875V/12.5mV STEP						
VSET4	ENBUCK4	BUCK4 OUTPUT VOLTAGE SET: 0.8V-3.975V/25mV STEP						
VSET5	ENLDO2	LDO2 OUTPUT VOLTAGE SET: 0.8V-3.975V/25mV STEP						
VSET6	ENLDO3	LDO3 OUTPUT VOLTAGE SET: 0.8V-3.975V/25mV STEP						
VSET7	ENLDO4	LDO4 OUTPUT VOLTAGE SET: 0.8V-3.975V/25mV STEP						
VSET8	ENLDO5	LDO5 OUTPUT VOLTAGE SET: 0.8V-3.975V/25mV STEP						
RESERVED								
Status1	PGLDO4	PGLDO3	PGLDO2	PGRTC	PG4	PG3	PG2	PG1

REGISTER HEX D7 D6 D5 D4 D3 D2 D1 D0

read all

Figure 7: [MP5416](#) Evaluation GUI

REGISTER	HEX	D7	D6	D5	D4	D3	D2	D1	D0
CTL0(0x0)	8F	1	0	0	0	1	1	1	1
CTL1(0x1)	87	1	0	0	0	0	1	1	1
CTL2(0x2)	7F	0	1	1	1	1	1	1	1
ILIMIT(0x3)	AA	1	0	1	0	1	0	1	0
VSET1(0x4)	C0	1	1	0	0	0	0	0	0
VSET2(0x5)	9C	1	0	0	1	1	1	0	0
VSET3(0x6)	C0	1	1	0	0	0	0	0	0
VSET4(0x7)	E4	1	1	1	0	0	1	0	0
VSET5(0x8)	DC	1	1	0	1	1	1	0	0
VSET6(0x9)	28	0	0	1	0	1	0	0	0
VSET7(0xa)	A8	1	0	1	0	1	0	0	0
VSET8(0xb)	54	0	1	0	1	0	1	0	0
Status1(0xd)	BF	1	0	1	1	1	1	1	1
Status2(0xe)	0	0	0	0	0	0	0	0	0
Status3(0xf)	0	0	0	0	0	0	0	0	0
ID2(0x11)	80	1	0	0	0	0	0	0	0

Figure 8: [MP5416](#) I²C GUI

DESIGN EXAMPLE

Customer Specs ⁽¹⁾:

- VIN: 5V (typ)
- VOUT1: 0.9V@1.24A (typ), 1.55A (max)
- VOUT2: 2.5V@300mA (typ), 375mA (max)
- VOUT3: 1.2V@700mA (typ), 900mA (max)
- VOUT4: 1.0V@220mA (typ), 280mA (max)

Using the [MP5416](#) Evaluation GUI

Open this GUI .exe file and install it on your computer. Open the software and follow the operation steps below to check output voltage options.

Step1: Select the part number ([MP5416](#)).

Step2: Click on the Buck 1 - Buck 4 control bit.

Step3: Choose input voltage (5V).

Step4: Check available voltage options for each buck ⁽²⁾

Select VOUT1 to 0.9V, VOUT2 to 2.5V, and VOUT3 to 1.2V. There is no 1.0V option when selecting VOUT4 (see Figure 9). This means the specs above are not recommended, and the test waveform in Figure 4 shows that the steady state at these specs is unstable.

If swapping the output voltages of Buck 2 and Buck 4, change the Buck 4 output voltage from 1V to 2.5V. The steady state waveform is stable (see Figure 5), and the evaluation GUI also has this option (see Figure 10).

NOTES:

- 1) These settings are not optimized.
- 2) The V_{OUT} of each buck must be selected sequentially. For example, after the V_{OUT} of Buck 1 is selected, then the V_{OUT} of Buck 2 can be selected. This cannot be done in reverse.

MP5416-5V POWER MANAGEMENT IC WITH I2C

Part Numbers Debug Tool Utility Help

ADDRESS:

REGISTER CONTROL:

EN Disable Buck1(0)
Vout 0.9

BUCK2(0X5)
EN Disable Buck2(0)
Vout 2.5

BUCK3(0X6)
EN Disable Buck3(0)
Vout 1.2

BUCK4(0X7)
EN Enable Buck4(1)
Vout 3.3

WRITE GROUP

Name	D7	D6	D5	D4	D3	D2	D1	D0
CTL0	SYSHN	SFRST	RESERVED				RESERVED	RESERVED
CTL1	RESERVED	MODEBUCK1	MODEBUCK2	MODEBUCK3	MODEBUCK4	DISCHGBUCK3	DISCHGBUCK2	DISCHGBUCK1
CTL2	DVS SLEW RATE		DISCHGBUCK4	DISCHGLDO2	DISCHGLDO3	DISCHGLDO4	DISCHGLDO5	RESERVED
ILIMIT	ILIMBUCK1		ILIMBUCK3		ILIMBUCK2		ILIMBUCK4	
VSET1	ENBUCK1	BUCK1 OUTPUT VOLTAGE SET: 0.8V-2.1875V/12.5mV STEP						
VSET2	ENBUCK2	BUCK2 OUTPUT VOLTAGE SET: 0.8V-3.975V/25mV STEP						
VSET3	ENBUCK3	BUCK3 OUTPUT VOLTAGE SET: 0.8V-2.1875V/12.5mV STEP						
VSET4	ENBUCK4	BUCK4 OUTPUT VOLTAGE SET: 0.8V-3.975V/25mV STEP						
VSET5	ENLDO2	LDO2 OUTPUT VOLTAGE SET: 0.8V-3.975V/25mV STEP						
VSET6	ENLDO3	LDO3 OUTPUT VOLTAGE SET: 0.8V-3.975V/25mV STEP						
VSET7	ENLDO4	LDO4 OUTPUT VOLTAGE SET: 0.8V-3.975V/25mV STEP						
VSET8	ENLDO5	LDO5 OUTPUT VOLTAGE SET: 0.8V-3.975V/25mV STEP						
RESERVED								
Status1	PGLDO4	PGLDO3	PGLDO2	PGRTC	PG4	PG3	PG2	PG1

REGISTER HEX D7 D6 D5 D4 D3 D2 D1 D0

read all

No slave found, Please check the connection

Figure 9: No 1.0V Vout 4 Option in the Evaluation GUI

MP5416-5V POWER MANAGEMENT IC WITH I2C

Part Numbers Debug Tool Utility Help

ADDRESS:

REGISTER CONTROL:

EN Disable Buck1(0)
Vout 0.9

BUCK2(0X5)
EN Disable Buck2(0)
Vout 1

BUCK3(0X6)
EN Disable Buck3(0)
Vout 1.2

BUCK4(0X7)
EN Disable Buck4(0)
Vout 2.5

WRITE GROUP

Name	D7	D6	D5	D4	D3	D2	D1	D0
CTL0	SYSHN	SFRST	RESERVED				RESERVED	RESERVED
CTL1	RESERVED	MODEBUCK1	MODEBUCK2	MODEBUCK3	MODEBUCK4	DISCHGBUCK3	DISCHGBUCK2	DISCHGBUCK1
CTL2	DVS SLEW RATE		DISCHGBUCK4	DISCHGLDO2	DISCHGLDO3	DISCHGLDO4	DISCHGLDO5	RESERVED
ILIMIT	ILIMBUCK1		ILIMBUCK3		ILIMBUCK2		ILIMBUCK4	
VSET1	ENBUCK1	BUCK1 OUTPUT VOLTAGE SET: 0.8V-2.1875V/12.5mV STEP						
VSET2	ENBUCK2	BUCK2 OUTPUT VOLTAGE SET: 0.8V-3.975V/25mV STEP						
VSET3	ENBUCK3	BUCK3 OUTPUT VOLTAGE SET: 0.8V-2.1875V/12.5mV STEP						
VSET4	ENBUCK4	BUCK4 OUTPUT VOLTAGE SET: 0.8V-3.975V/25mV STEP						
VSET5	ENLDO2	LDO2 OUTPUT VOLTAGE SET: 0.8V-3.975V/25mV STEP						
VSET6	ENLDO3	LDO3 OUTPUT VOLTAGE SET: 0.8V-3.975V/25mV STEP						
VSET7	ENLDO4	LDO4 OUTPUT VOLTAGE SET: 0.8V-3.975V/25mV STEP						
VSET8	ENLDO5	LDO5 OUTPUT VOLTAGE SET: 0.8V-3.975V/25mV STEP						
RESERVED								
Status1	PGLDO4	PGLDO3	PGLDO2	PGRTC	PG4	PG3	PG2	PG1

REGISTER HEX D7 D6 D5 D4 D3 D2 D1 D0

read all

No slave found, Please check the connection

Figure 10: Recommended Option in the Evaluation GUI

Using the [MP5416](#) Output Voltage Selection Excel File

Open the output voltage selection Excel file. Navigate to the 5Vin sheet and choose the output voltage using the filter button. Users do not need to choose the V_{OUT} of each buck sequentially with this Excel file. If the desired voltage combination cannot be found, this means that this option is not recommended.

The customer specs above are not in the [MP5416](#) output voltage selection Excel file (see Figure 11).

Notes: 1. The SW operation frequency is 1.5MHz. 2. Please choose the output voltage by the Filter Button, DO NOT fill out it.							
ID	Buck1	Buck2	Buck3	Buck4	Result	Comment	
195	0.9	2.5	0.9	3.3	OK		
196	0.9	2.5	1	3.3	OK		
197	0.9	2.5	1.1	3.3	OK		
198	0.9	2.5	1.2	3.3	OK		
199	0.9	2.5	1.3	2.5	OK		
200	0.9	2.5	1.3	3.3	OK		
201	0.9	2.5	1.5	2.5	OK		
202	0.9	2.5	1.5	3.3	OK		
1486							
1487							
1488							
1489							
1490							

Figure 11: No 1.0V Buck 4 Option in the Output Selection Excel File

If swapping the output voltages of Buck 2 and Buck 4, this voltage combination is one of the options in the Excel file (see Figure 12).

Notes: 1. The SW operation frequency is 1.5MHz. 2. Please choose the output voltage by the Filter Button, DO NOT fill out it.							
ID	Buck1	Buck2	Buck3	Buck4	Result	Comment	
50	0.9	1	1.2	1.2	OK		
51	0.9	1	1.2	1.3	OK		
52	0.9	1	1.2	1.5	OK		
53	0.9	1	1.2	2.5	OK		
54	0.9	1	1.2	3.3	OK		

Figure 12: Recommended Option in the Output Selection Excel File