MP44010

Boost PFC

Application Note

Prepared by Fei Wang / Jeffery Ding / Stone Lin

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ABSTRACT

This application note explains the basic operation of a boost PFC controller and provides a design example of the MP44010 operating with a wide input voltage and boundary conduction mode. The design example is described in detail with design parameters at the end of this application note.

MP44010 Introduction

The MP44010 is a boundary conduction mode PFC controller, designed to provide simple and high performance active power factor correction using minimum external components.

The MP44010 provides two-step effective over-voltage protection that guarantees safe operation. The MP44010 features ultra-low start-up current and low quiescent current. To minimize distortion, a zero-crossing detection circuit is added to the output of multiplier of the MP44010. The MP44010 is integrated with an R/C filter on the current sense pin to filter out the leading edge noise.

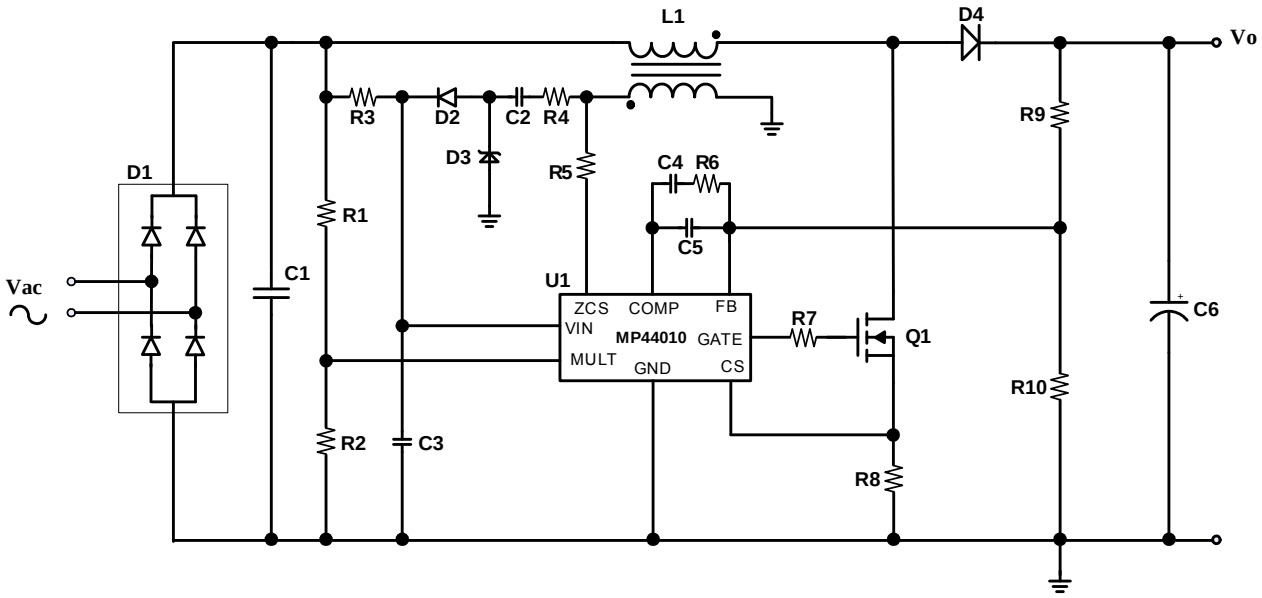

Figure 1—MP44010 Typical Application Circuit

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BOOST PFC OPERATION USING MP44010

The MP44010 senses the inductor current through the current sense pin and compares it to the sinusoidal-shaped signal, which is generated from the multiplier. When the external power MOSFET turns on, the inductor current rises linearly. When the peak current hits the sinusoidal-shaped signal, the external power MOSFET begins to turn off and the diode turns on. The inductor current also begins to fall. When the inductor current reaches zero, the power MOSFET begins to turn on again, which causes the inductor current to start rising again. The power circuit works in boundary conduction mode, and the envelope of the inductor current is sinusoidal-shaped. The average input current is half of the peak current, so the average input current is also sinusoidal-shaped. A high power factor can be achieved using this control method.

The related blocks in the PFC circuit are described in detail in the following pages.

ZCS (Zero Crossing Sensing) Block

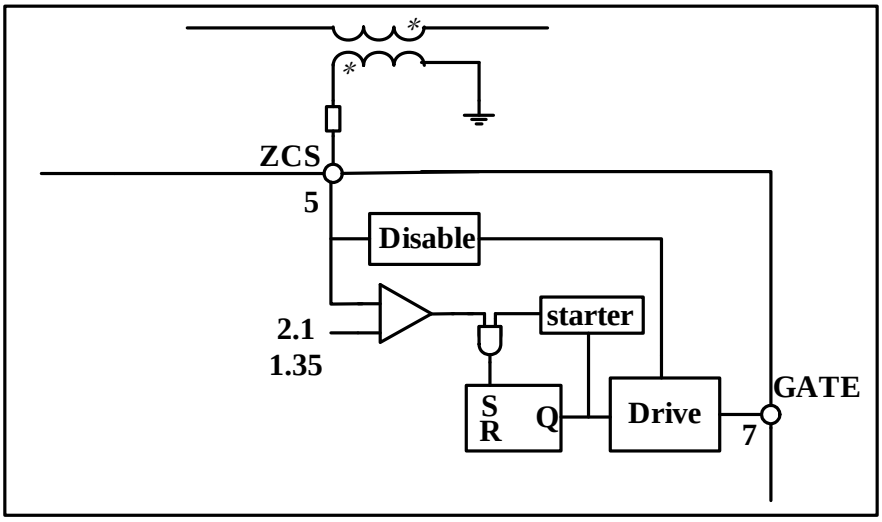


Figure 2—ZCS Block

As the converter is running, the signal of the ZCS is obtained by the auxiliary winding on the boost inductor. When the inductor current reaches zero, the voltage across the inductor reverses. When the negative edge of ZCS is going from above 2.1V to below 1.35V, it triggers the MOSFET to turn on. Thus, the external MOS can be turned on with the negative-going edge. At start-up, when there is no signal present at the ZCS, an internal starter forces the driver to deliver a pulse to the gate of the MOSFET to perform the function.

The ZCS pin is also used to activate the disable function. If the voltage on the ZCS pin is below 190 mV, the MP44010 will be shut down. As a result, its power consumption is reduced. To re-enable the chip operation, the pull-down must be released.

Current Sense Block

The current comparator senses the voltage through the current sense resistor and compares it to the output of the multiplier to determine the exact time for turning off the external MOSFET. To avoid spurious switching of the MOSFET due to noise at the CS pin, an internal R/C filter is added to the CS pin.

Multiplier Block

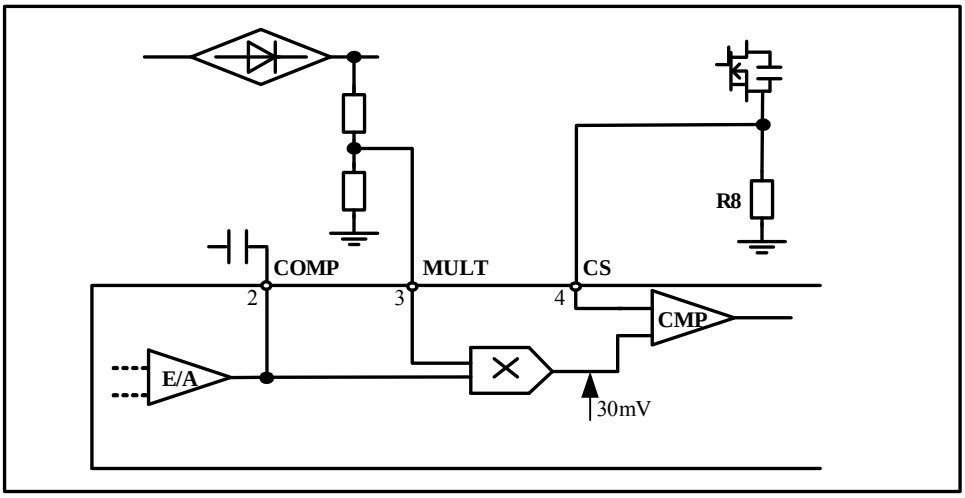


Figure 3—Multiplier Block

The multiplier has two inputs: one sees a partition of the instantaneous rectified line voltage and the other one sees the output of the E/A. If the E/A output voltage is constant during a half line cycle, the output of the multiplier will be shaped as a sinusoid and is the reference signal for the current comparator, which controls the peak current cycle by cycle.

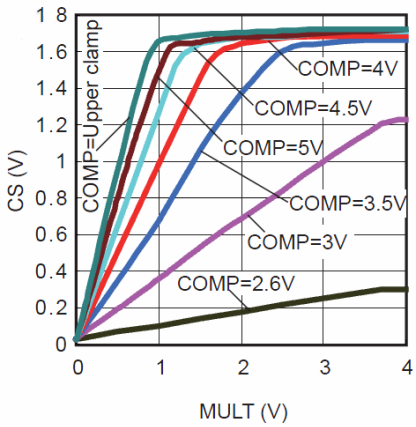


Figure 4—Multiplier Characteristics

As shown in Figure 4, the multiplier circuit operates optimally in the linear region. The two parameters that need to be determined are COMP and the peak voltage of the MULT pin. The COMP voltage can

be measured at the output of the E/A. Once the COMP voltage is chosen, the peak voltage of the MULT pin should be set according to the linear curve in Figure 4. If MULT and CS do not follow the linear curve in Figure 4, the divider ratio of the line voltage or the sense resistor should be adjusted. If the circuit works in the linear region but does not cover the full range of the multiplier, either the divider ratio of the line voltage or the sense resistor can be increased to maximize the full range of the multiplier.

Near the zero crossing of line, the output of the multiplier is close to zero, so there is no switching of the power MOSFET that results in input current distortion. A special circuit of 30mV offset that has been added to the output of the multiplier can optimize the input current THD.

OVP (Over Voltage Protection) Block

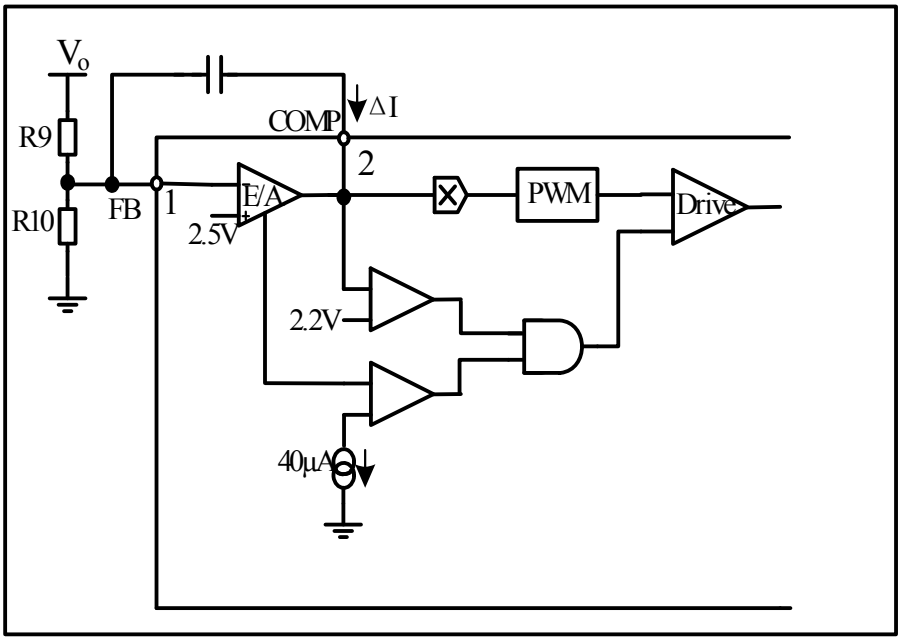


Figure 5—OVP Block

The MP44010 provides two-step precise over-voltage protection (OVP), which is accomplished by monitoring the current flow through the COMP pin. At steady state, the voltage control loop keeps the output voltage close to the nominal value, set by the resistor divider R9 and R10. Neglecting the output ripple, the current through R9-I_{R9}, equals that through R10-I_{R10}. Given that the reference voltage is 2.5V, the voltage at the FB pin will be also 2.5V, and the current through R10 and R9 is calculated as follows:

$$I_{R10} = \frac{2.5}{R10} = I_{R9} = \frac{V_o - 2.5}{R9}$$

To achieve high PF, a compensation network is connected between FB pin and COMP pin. When the output load drops, an abrupt change of output voltage $\Delta V_O>0$ will take place. Because the voltage across R10 is fixed at 2.5V, the current through R10 will remain the same, then current through R9 becomes:

$$I'_{R9}=\frac{V_o-2.5+\Delta V_o}{R9}.$$

The difference in current, $\Delta I_{R9}=I'_{R9}- I_{R10}=\Delta V_o/R9$, will flow through the compensation network and enter the E/A (COMP pin). The current is internally monitored by the MP44010. If the current exceeds 40μA, the dynamic OVP is triggered and the power MOSFET is turned off. This dynamic OVP condition is maintained until the current falls below approximately 10μA, at which point the inner starter is enabled and IC is allowed to restart.

When the output load is very light, the output voltage tends to exceed the nominal value and increase gradually. Therefore, the dynamic OVP function will not be as effective. If this condition occurs, the E/A will saturate low and triggers the static OVP to turn off the power MOSFET. As the E/A returns to the linear region, the converter will resume operation.

BOOST PFC DESIGN USING THE MP44010

This section discusses the different components of the boost PFC design as well as design example based on the MP44010 and given requirements. The definitions of frequently mentioned parameters through the following pages are summarized below.

Input AC RMS voltage: V_{ac} (V_{ac_min}~V_{ac_max})

Input RMS current: I_{ac}

Input power: P_{in}

Output DC voltage: V_o

Output power: P_o

Efficiency: $\eta=P_o/P_{in}$

Minimum switching frequency: f_{sw_min}

Switching frequency: f_{sw}

Peak inductor current: I_{Lpk}

Power Stage Design

a. Diode Bridge

The diode bridge should withstand the maximum reverse input AC voltage and the maximum input current. Two of the criteria to be considered for selecting a diode bridge are the maximum instantaneous voltage, which is the peak voltage of the line voltage, and the maximum input RMS

current (which is the input RMS current at low line). In addition, package size, and thermal performance should also be considered. For handling line frequency current, a standard low-cost diode bridge with slow recovery can be used.

b. Input Capacitor

The input capacitor after the diode bridge is used to provide a bypass path for high switching frequency current and minimize fluctuation on the rectified sinusoidal input voltage. In general, a voltage drop up to 10% on the input capacitor may be expected. A worst case occurs under minimum input voltage due to the biggest current ripple, as shown in the equation below.

$$C_{in} = \frac{I_{ac\_max}}{2\pi \cdot f_{sw} \cdot r \cdot V_{ac\_min}}$$

In the above equation, r is the coefficient (0.01~0.1) and f_{sw} is the switching frequency at the peak of the minimum input AC voltage. A capacitor with good high frequency performance, such as ceramic cap or tantalum cap should be selected.

c. Inductor

For critical mode Boost PFC, the on-time of MOSFET can be written as below:

$$T_{on} = \frac{L \cdot I_{LPK} \cdot \sin(\theta)}{\sqrt{2}\, V_{ac} \sin(\theta)} = \frac{L \cdot I_{LPK}}{\sqrt{2}\, V_{ac}}$$

From the above equation, one can see that the on-time is related to L, I_{Lpk} and V_{ac}. For a given L and P_o, T_{on} is constant when V_{ac} is fixed.

The off time of MOSFET can be written as:

$$T_{off} = \frac{L \cdot I_{LPK} \cdot \sin(\theta)}{V_o - \sqrt{2}\, V_{ac} \sin(\theta)}$$

F_{sw} is 1/T, which equals 1/ (T_{on} +T_{off}), which can be described as the following equation.

$$f_{sw}(\theta) = \frac{1}{T_{on} + T_{off}} = \frac{1}{2 \cdot L \cdot P_{in}} \cdot \frac{V_{ac}{}^2 \cdot (V_o - \sqrt{2}\, V_{ac} \sin(\theta))}{V_o}$$

The minimum switching frequency occurs at the peak of AC input voltage. As the curve in Figure 6 shows, the switching frequency varies with input AC RMS voltage with the minimum frequency occurring at the peak of the AC input voltage. The curve is measured with V_{ac}=85~265V, L=280μH at 150W output power.

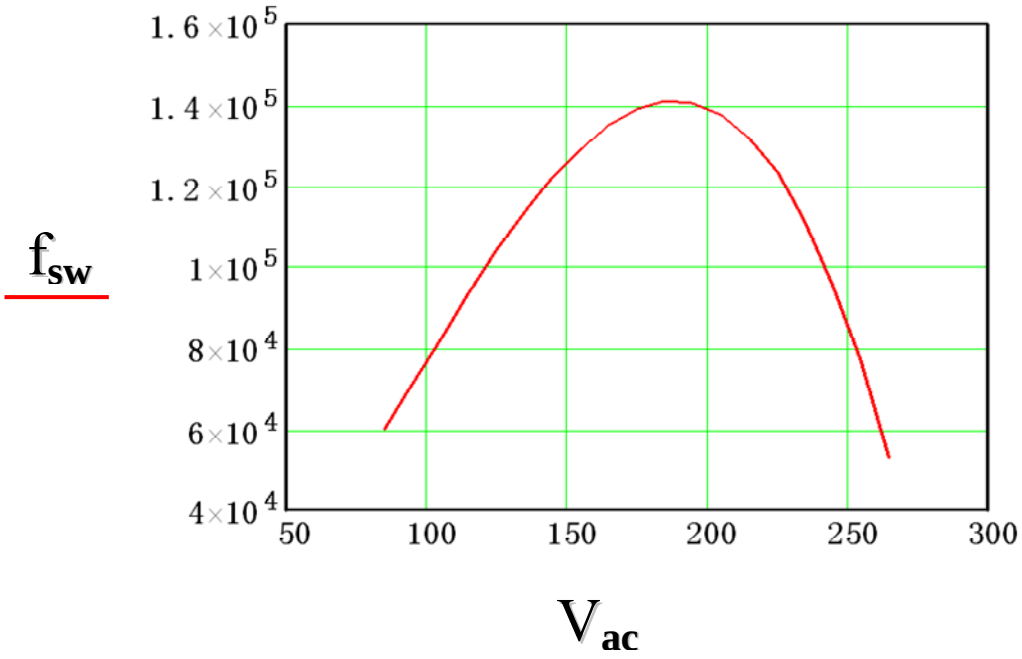


Figure 6—Switching frequency vs. V_{AC}

As the above figure shows, the minimum frequency occurs at maximum input voltage. So the inductance should be calculated based on maximum input voltage:

$$L=\frac{V_{ac\_max}{}^2(V_o-\sqrt{2}V_{ac\_max})}{2f_{sw\_min}\cdot P_{in}\cdot V_o}$$

The recommended value for f_{sw_min} is above 20kHz (typically, 30~40 kHz) which is above the audible frequency. Once inductance is calculated, magnetic core size should be chosen according to the condition below:

$$A_p = A_e \cdot A_w > \frac{L\cdot I_{Lpk}\cdot I_{Lrms}}{B_{max}\cdot K_c\cdot j}$$

Where

$$I_{Lrms}=\frac{I_{Lpk}}{\sqrt{6}}$$

A_e is the effective area of the core section; A_w is the effective area of the core window; B_{max} is the max swing of the magnetic flux density (generally B_{max}=0.3~0.4T); K_c is the winding factor, which is about 0.3 in inductor design; j is the current density in the wire, which is typically 4A/mm2.

With the selected core size, the inductor turn number is:

$$N_p=\frac{L\cdot I_{Lpk}}{B_{max}\cdot A_e}$$

To avoid saturation of the core, air gap is necessary:

$$\sigma = \frac{N_p{}^2 \cdot A_e \cdot \mu}{L}$$

Where μ is the magnetic permeability.

As previously described in this document, the zero current sensing of this MP44010 is performed by sensing the falling-edge of auxiliary winding of the inductor. Therefore, auxiliary winding turn number needs to be properly determined to guarantee normal operation of ZCS.

The maximum turns ratio of main to auxiliary winding is:

$$N = \frac{V_o - \sqrt{2}V_{acmax}}{ZCS_{rising\_max}}$$

Where: ZCS_{rising_max} is the max rising threshold of ZCS. The real turn ratio should be not higher than the calculated value and the turn number of auxiliary winding is $N_s = \frac{N_p}{N}$.

After complete the above design, the wire size should be properly chosen to minimize the winding conduction loss and the leakage inductance. The loss depends on the current value flow through the winding, the length of wire and the wire size.

The wire size is determined by the RMS current flow through the winding. So the primary wire size should be:

$$S_P = \frac{I_{Lrms}}{j}$$

Due to the skin effect and proximity effect of the conductor, the diameter of the selected wire is generally less than 2*Δd. Δd is the skin depth:

$$\Delta d = \sqrt{\frac{1}{\pi \cdot f_{s\_min} \cdot \mu \cdot G}}$$

Where G is the conductivity of the wire (for copper wire, G is typically 6×10^7S/m.

Usually, multiple strands of thinner wire or Litz wire is adopted to minimize the AC resistance. The effective cross section area of multi-strands wire or Litz wire should be large enough to meet the requirement set by the current density.

After the wire size have been determined, it is necessary to double check whether the window area with selected core can accommodate the windings calculated in the pervious steps. If not, the core should be re-selected as former design steps.

d. Power MOSFET

The voltage rating of MOSFET is determined by output voltage, OVP threshold, and some margin, such that $V_{DS}>V_o+\Delta V_{OVP}$. The current rating of the MOSFET is determined by the RMS value of the current flowing through the MOSFET. The RMS current of MOSFET follows the below equation:

$$I_{Qrms}=2\sqrt{2}I_{ac}\cdot\sqrt{\frac{1}{6}-\frac{4\sqrt{2}}{9\pi}\cdot\frac{V_{ac}}{V_o}}$$

In addition, the MOSFET pulsed- drain current should be higher than the peak inductor current.

$$I_{D\_pulse} > I_{Lpk}$$

e. Output Diode

The boost diode should have the same voltage criteria as the MOSFET.

The average current of output diode is the same with the output current of PFC regulator:

$$I_{Do}=I_o$$

And the RMS current could be calculated according to below formula to estimate the power consumption of the diode:

$$I_{Drms}=2\sqrt{2}I_{ac}\cdot\sqrt{\frac{4\sqrt{2}}{9\pi}\cdot\frac{V_{ac}}{V_o}}$$

When the inductor current drops to zero, the diode will start to block the current. However, if the recovery speed of the diode is slow, the inductor current will continue to go negative, which affects efficiency and the circuit operation. Therefore, a diode with a fast recovery is recommended.

f. Output Capacitor

In general, two criteria for selecting output capacitor are output voltage ripple, ΔVo, and hold-up time. Output ripple is a function of effective series resistance, ESR, of the capacitor, output current, I_o, line frequency (f_L), and output capacitance as shown in the equation below:

$$\Delta V_o = 2I_o\sqrt{\frac{1}{(2\pi\cdot 2f_L\cdot C_o)^2}+ESR^2}$$

The calculated ripple with the selected cap should be lower than the actual allowable output ripple. The capacitor should be chosen so that the hold-up time satisfies the following equation:

$$C_o = \frac{2P_{in}\cdot t_{hold}}{V_{o\_min}{}^2 - V_{o\_holdup}{}^2}$$

Where V_{o_min} is the minimum output voltage under all normal operating conditions and V_{o_holdup} is the required minimum operating output voltage that is needed to supply the downstream DC-DC converter when the line voltage is shut down. The maximum voltage at the output is a combination of output DC

voltage, output voltage ripple, and OVP threshold. Therefore, the voltage rating of the capacitor needs to be higher than this maximum output voltage at worst case.

Control Circuit Design

a. Start-up Resistor

Under the condition of not using an external Vin power supply, a simple approach to handling start-up is by having a start-up resistor to connect to the rectified mains voltage. The IC will be off until Vin capacitor is charged higher than threshold through start-up resistor. According to required start-up time, the start-up resistor can be roughly calculated based on below equation:

$$R_{start}=\frac{T_{start}(\sqrt{2}V_{ac}-V_{IN\_th})}{C_{vcc}\cdot V_{IN}+I_q\cdot T_{start}}$$

Since the start-up resistor causes a voltage drop between the rectified AC voltage and the supply voltage of the chip, using a big value resistor helps to minimize the power dissipation due to I^2R.

b. VIN Bias Charge Circuit through Auxiliary Winding

Generally, the current flow through the start-up resistor is not high enough during normal operation of the IC. A bias charge circuit connecting auxiliary winding could be used to power the IC, as shown in the typical application circuit in Figure 1. This circuit contains D2, D3, C2 and R4.

In the figure, when the auxiliary winding voltage is positive, C2 will be charged through R4, and the charge current will also charge C3 through D2. At the same time, the Zener diode, D3, can avoid having too much charge voltage. When the auxiliary winding voltage is negative, C2 will be discharged through R4 and D3. D2 is reverse blocked.

c. MULT Resistor Divider

As mentioned earlier, the operation of the multiplier should be in linear region. For example, to keep the MULT pin voltage below 3V which is in the linear range of MULT voltage at maximum AC input condition, the MULT voltage under minimum AC input has to satisfy the following condition:

$$V_{MULT\_min}=V_{MULT\_max}\frac{V_{ac\_min}}{V_{ac\_max}}$$

To prevent the output of the multiplier from saturating under minimum AC input voltage, the below condition must be met:

$$V_{CS\_max}=1.62\cdot V_{MULT\_min}<1.6V$$

Otherwise, the calculation has to be re-done with a lower MULT voltage.

As to the resistor divider, the value should be as below:

$$\frac{R2}{R1+R2}=\frac{V_{MULT\_max}}{\sqrt{2}V_{ac\_max}}$$

d. Current Sense Resistor

As discussed in the Multiplier section, the current flow through the MOSFET should be sensed by an external resistor. When the voltage on current sense resistor is equal to Multiplier output, the MOSFET will be turned off.

The sensed voltage on current sense resistor should be less than the maximum output of the Multiplier, such that:

$$R_S = R8 \le \frac{V_{CS\_max}}{I_{Lpk}}$$

Where V_{CS_max} is the maximum output of the Multiplier calculated in previous section.

In addition, the current limit function can be realized when the voltage on sensing resistor is equal to the high-clamp voltage of CS pin. The max current limit is:

$$I_{limit} = \frac{V_{CS\_clamp}}{R_S} = \frac{V_{CS\_clamp}}{R8}$$

When selecting a MOSFET, the current rating of the MOSFET is important. It needs to be able to handle a current higher than the current limit to avoid any damage to the MOSFET.

e. ZCS Resistor

The ZCS resistor connects the ZCS pin and auxiliary winding. The main purpose of the resistor is to avoid excessive voltage on the ZCS pin. Therefore, a minimum ZCS resistor is required to ensure that the ZCS pin voltage is lower than high clamp voltage under maximum auxiliary winding voltage:

$$R5 = R_{ZCS} \ge \frac{V_{aux\_max} - V_{ZCSclamp\_H}}{2.5mA}$$

Where V_{aux_max} is the maximum voltage on auxiliary winding output voltage, which is Vo/N. $V_{ZCSclamp\_H}$ is the upper clamp voltage of the ZCS pin. Generally, R5 is not bigger than 100kΩ.

f. Feedback Resistor

Vo can be set by using the appropriate feedback resistors. Since the OVP threshold is sestet by using the high-side feedback resistor, R9. This resistor should be selected, which is calculated as:

$$R9 = \frac{\Delta V_{OVP}}{I_{OVP}}$$

Where ΔV_{OVP} is the dynamic OVP threshold above normal V_o and I_{OVP} is dynamic OVP triggering current. The low-side feedback resistor can simply be calculated as:

$$R10 = \frac{2.5}{V_o - 2.5} \cdot R9$$

g. Compensation Network Design

Figure 7 shows the circuit block of control loop inside and outside of the MP44010.

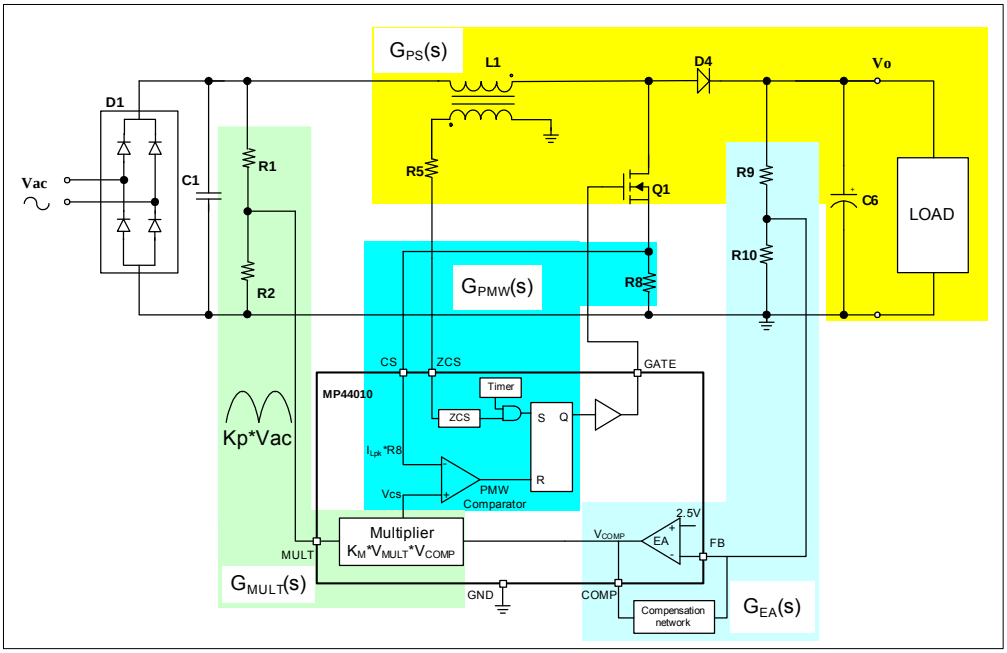


Figure 7—Control Loop Diagram of MP44010

Based on the above control loop diagram, the block diagram of voltage loop can be simplified, as is shown in the Figure 8.

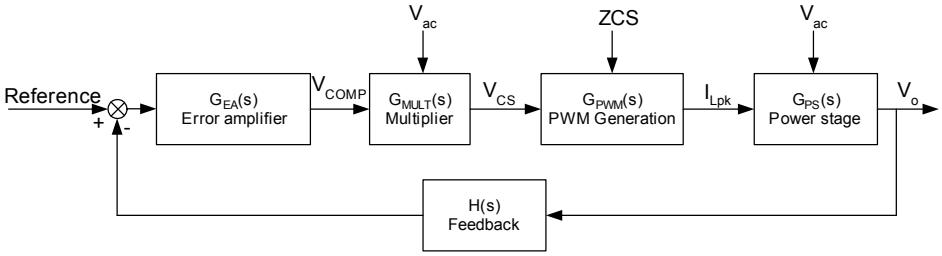


Figure8—Block Diagram of Voltage Loop

While $G_{vc}(s)$ is the control to output transfer function, it can be calculated by:

$$G_{VC}(s) = G_{PS}(s) \cdot G_{PWM}(s) \cdot G_{MULT}(s)$$

The open voltage loop transfer function can be calculated by:

$$T(s) = G_{VC}(s) \cdot G_{EA}(s)$$

Please note that H(s) is treaded as part of $G_{EA}(s)$ and H(s)=1 in this file.

To design a high stability voltage loop, the crossover frequency (bandwidth) and the phase margin of T(s) need to be properly designed. The phase margin is usually designed to be larger than 30^{o} in practical application, this can be achieved by designing compensate network of voltage error amplifier. Because PFC output has 2^{nd} line frequency harmonics, it is coupled to the output of voltage error

amplifier and causing input current reference distortion. To get better THD and high PF, the voltage error amplifier should attenuate the 2nd line frequency and maintain its output voltage to a constant value. Therefore, the bandwidth usually is very low. As a rule of thumb, the bandwidth should not exceed 25Hz.

The procedure to design the compensation is:

Step 1: Calculate control to output transfer function $G_{vc}(s)$

Control to output transfer function includes all components in voltage loop excluding error amplifier. $G_{vc}(s)$ must be calculated before designing the voltage error amplifier compensation network.

a). Calculate the transfer function of Multiplier

The Multiplier output is the reference of inductor current. The relationship between COMP voltage and Multiplier output voltage is:

$$V_{CS} = K_M \cdot V_{MULT} \cdot V_{COMP} = K_M \cdot K_P \cdot \sqrt{2} V_{ac} \cdot V_{COMP}$$

Where, K_M is the gain of the multiplier and K_M=0.64. K_P is the ratio of the resistor divider of the input voltage, it can be calculated by:

$$K_P = \frac{R2}{R1+R2}$$

For a given V_{ac}, the transfer function of Multiplier can be calculated:

$$G_{MULT}(s) = \frac{dV_{CS}}{dV_{COMP}} = K_M \cdot K_P \cdot \sqrt{2} V_{ac}$$

b). Calculate the transfer function of PWM

The T_{on} is achieved by comparing voltage of Rs and multiplier output. T_{off} is achieved by ZCS circuit. The output of the multiplier is the control signal to control the inductor current through sensing the voltage signal on sensing resistor. In such low frequency we discussed here, the inner current loop can be considered as ideal, which means the inductor current always follow the reference signal, then the relationship between inductor current and reference signal could be got:

$$V_{cs} = I_{Lpk} \cdot R_s = I_{Lpk} \cdot R8$$

So the transfer function of PWM block could be expressed as:

$$G_{PWM}(s) = \frac{dI_{Lpk}}{dV_{cs}} = \frac{1}{R8}$$

c). Calculate the transfer function of power stage

The power stage can be modeled as is shown in Figure 9 in the half line frequency cycle. It includes a controlled current source in parallel with the output capacitor C_o and load resistor R_o. R_e is the equivalent impedance which indicates disturbance of Vo.

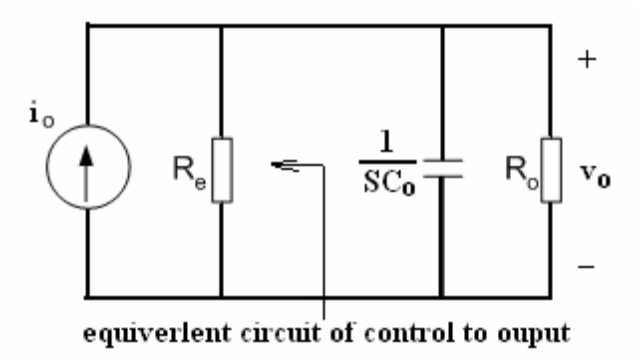


Figure 9—Small Signal of Power stage

The model is derived based on power balance equation below.

$$I_o = \frac{I_{in} \cdot V_{ac}}{V_o} = \frac{I_{Lpk}}{2 \cdot \sqrt{2}} \cdot \frac{V_{ac}}{V_o}$$

In the period of half line frequency, V_{ac} can be thought as constant for the small signal of control to voltage. Therefore, small signal of above equation is:

$$i_o = \frac{1}{2 \cdot \sqrt{2}} \cdot \frac{V_{in}}{V_o} \cdot i_{Lpk} - \frac{I_{Lpk}}{2 \cdot \sqrt{2}} \cdot \frac{V_{in}}{V_o^2} \cdot v_o = \frac{1}{2 \cdot \sqrt{2}} \cdot \frac{V_{in}}{V_o} \cdot i_{Lpk} - \frac{P_o}{V_o^2} \cdot v_o$$

Assume,

$$R_e = \frac{V_o^2}{P_o}$$

Then we can get

$$\frac{1}{2 \cdot \sqrt{2}} \cdot \frac{V_{in}}{V_0} \cdot i_{Lpk} = i_0 + \frac{v_o}{R_e}$$

The small signal is got based on above equation.

The transfer function of the power stage can be derived as:

$$G_{PS}(s) = \frac{dV_o}{dI_{Lpk}} = \frac{dV_o}{dI_o} \cdot \frac{dI_o}{dI_{Lpk}}$$

While

$$\frac{dI_o}{dI_{Lpk}} = \frac{V_{ac}}{2\sqrt{2}V_o}$$

And

$$\frac{dV_o}{dI_o} = Z_o = R_o // R_e // \frac{1}{sC_o}$$

If PFC downstream with a DC/DC converter, when load is changing, the input current of the cascaded DC/DC varied inversely with input voltage, the characteristic is similar to a constant power load within the bandwidth of DC/DC converter. Therefore,

$$R_o = -\frac{V_o^2}{P_o}$$

R_o is opposite in phase to R_e, so the effect of R_o and R_e can be ignored. $G_{PS}(s)$ can be calculated by:

$$G_{PS}(s)=\frac{\sqrt{2}}{4}\cdot\frac{V_{ac}}{V_o}\cdot\frac{1}{s\cdot C_o}$$

If PFC downstream with a resistive load, then,

$$R_o=\frac{V_o^2}{P_o}$$

So R_o equals to R_e, $G_{PS}(s)$ can be calculated by:

$$G_{PS}(s)=\frac{\sqrt{2}}{8}\cdot\frac{V_{ac}}{V_o}\cdot\frac{R_o}{1+\frac{s\cdot R_o\cdot C_o}{2}}$$

Finally, the transfer function of the control-to-output can be got with:

$$G_{VC}(s) = G_{PS}(s)\cdot G_{PWM}(s)\cdot G_{MULT}(s)$$

For constant power load, $$G_{VC}(s) = \frac{1}{2}\cdot\frac{K_M\cdot K_P\cdot V_{ac}{}^2}{R_s\cdot V_o}\cdot\frac{1}{s\cdot C_o}$$

For resistive load, $$G_{VC}(s) = \frac{1}{4}\cdot\frac{K_M\cdot K_P\cdot V_{ac}{}^2}{V_o}\cdot\frac{R_o}{R_s}\cdot\frac{1}{1+\frac{s\cdot R_o\cdot C_o}{2}}$$

Due to large Co, the pole frequency of $G_{vc}(s)$ is very low, usually 1~2Hz, the difference of $G_{vc}(s)$ between resistive load and constant power load appears in low frequency phase, while the gain is almost the same. Considering the resistive load is rarely happened to PFC, so only constant power load is taking into account for further designing.

Step 2: Determine Compensation Network Type

Bode plot is widely used to access the stability based on the phase and gain margin of open loop gain T(s). As shown in the Figure 10.

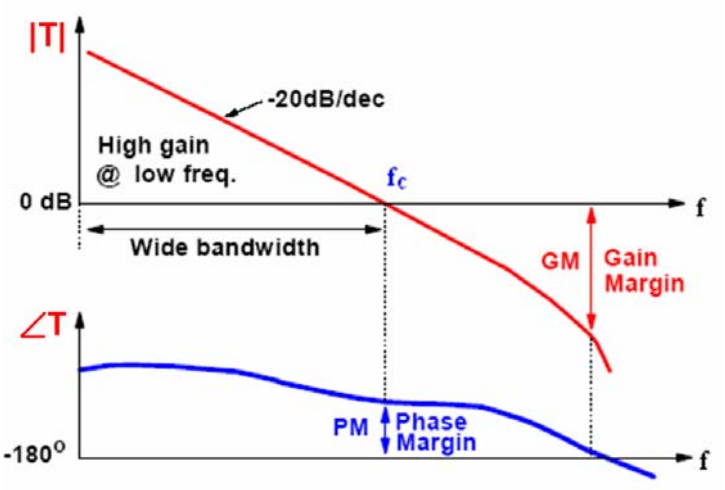


Figure 10—Gain margin and phase margin Definition

Criteria for accessing loop stability:

a). Phase margin: >45°.

b). Gain margin: >15dB.

c). Generally, the gain slope of T(s) at crossover frequency f_c is -20dB/dec.

d). High gain at lower frequency will make better regulation accuracy.

Therefore, we can draw the bode plots of the $G_{VC}(s)$ with constant power load, as is shown in Figure 11.

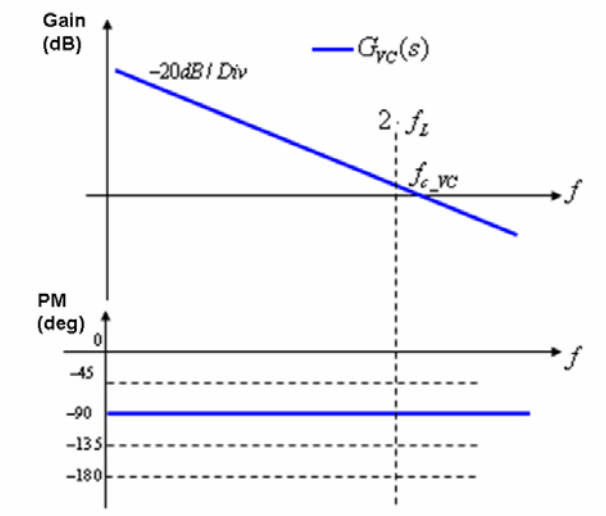


Figure 11—Bode Plots of $G_{VC}(s)$

From Figure11 to see, the DC gain of the $G_{VC}(s)$ is high enough for good regulation accuracy. But the phase margin (PM) of $G_{VC}(s)$ is always 90^0, and the crossover frequency f_{c_VC} is hundreds of Hertz.

Bode plot of the 3 types compensation networks are analysis based on the given $G_{VC}(s)$.

Type-1 compensation network includes a proportion and a pole, as shown in the Figure 12. This type of compensation can provide larger than 45° phase margin, but its drawback is the gain at lower frequency would be limited. This would cause worse load regulation.

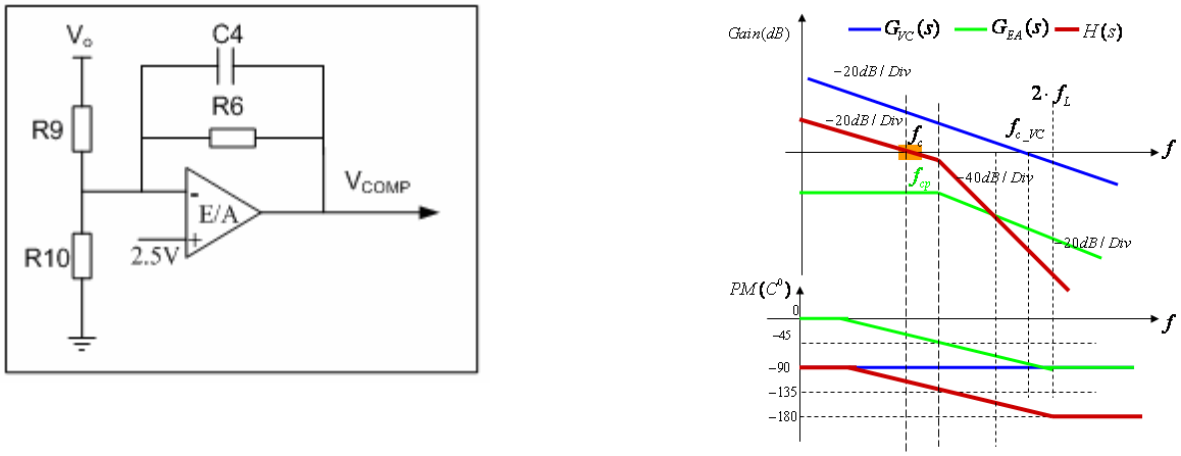


Figure 12—Bode Plots of Type1 Compensation Network

Type-2 compensation network with a pole and a zero is shown in the Figure 13. This type of compensation can provide larger than 45° phase margin and high DC gain. Comparing with type-3, it is not very easy to get very high gain margin for type-2 compensation network at two times of line frequency ($2f_L$).Therefore, the ability of attenuating 2nd line frequency harmonic at the input of E/A is a little weaker than type-3. Therefore, this type compensation network is always used in such application that PF requirement is not very strict.

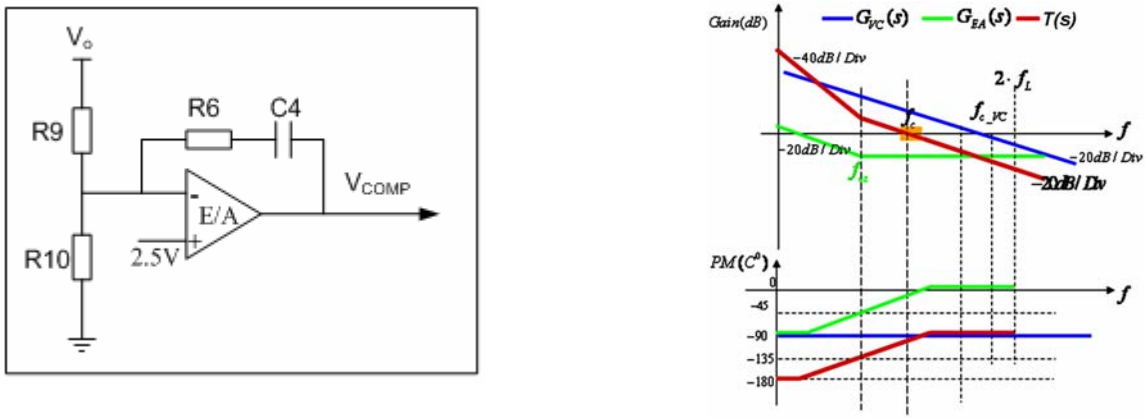


Figure 13—Bode Plots of Type2 Compensation Network

Type-3 compensation network includes two poles and a zero, as shown in the Figure 14. This type of compensation can provide larger than 45° phase margin and high DC gain. The pole with higher frequency is selected to provide enough gain to attenuate 2nd line frequency harmonic at input of E/A. Therefore, the THD and PF can be further improved.

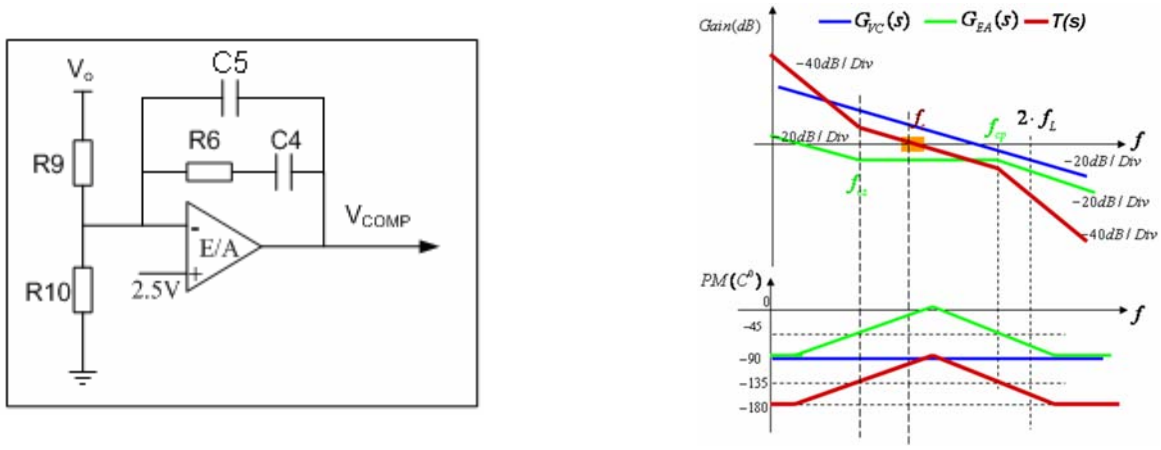


Figure 14—Bode Plots of Type3 Compensation Network

Step 3: Calculate Compensation Network

The compensation network with two poles and a zero is selected as an example. The transfer function of the voltage error amplifier is:

$$G_{EA}(s)=\frac{1+s\cdot R6\cdot C4}{s\cdot R9\cdot(C4+C5)\cdot\left(1+s\cdot R6\cdot\frac{C4\cdot C5}{C4+C5}\right)}$$

The procedure for compensation calculation is:

Firstly, determine the crossover frequency (f_C) of T(s). Generally, f_C is about 1/10~1/5 of 2 f_L (f_L is line frequency).

Secondly, determine the position of f_{cz}. If f_{cz} equals to f_c, then phase margin of H(s) would be 45°; if we want the phase margin is larger than 45°, and then the f_{cz} would be set to be smaller than fc, as is shown in the figure14.

$$f_{cz}=\frac{1}{2\cdot\pi\cdot R6\cdot C4}=f_c$$

And

$$\left|G_{EA}(f_{cp})\right|=\left|G_{VC}(f_c)\right|$$

Thirdly, the value of $\left|G_{EA}(2f_L)\right|$ can be determined to attenuate 2nd line frequency harmonic. Due to slope of $\left|G_{ea}(f)\right|$ is -20dB/div from f_{cp} to $2f_L$, therefore, below relationship is valid:

$$f_{cp}=2\cdot f_L\cdot 10^{\frac{\left|G_{EA}(f_{cp})\right|-\left|G_{EA}(2f_L)\right|}{20}}$$

And

$$f_{cp}=\frac{1}{2\cdot\pi\cdot R6\cdot(C4//C5)}\approx\frac{1}{2\cdot\pi\cdot R6\cdot C5}\quad(C4>>C5)$$

Finally,

$$f_l=\frac{1}{2\cdot\pi\cdot R9\cdot(C4+C5)}\approx\frac{1}{2\cdot\pi\cdot R9\cdot C4}$$

f_l can be selected at very low frequency, due to R9 is a known value, so base on above formulas, C4, R6 and C5 can be calculated.

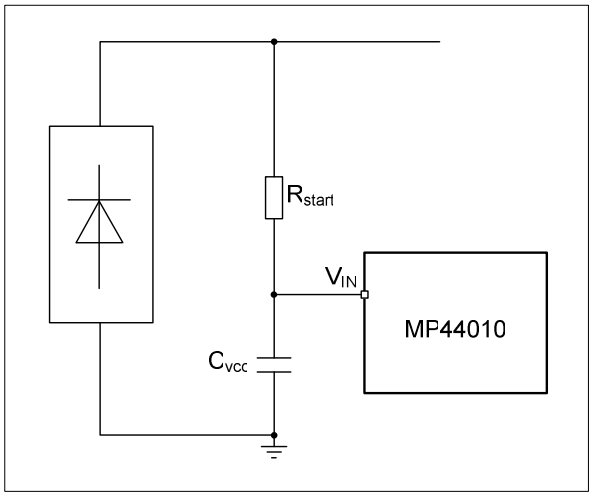
Design Tips

a. Reducing power dissipation

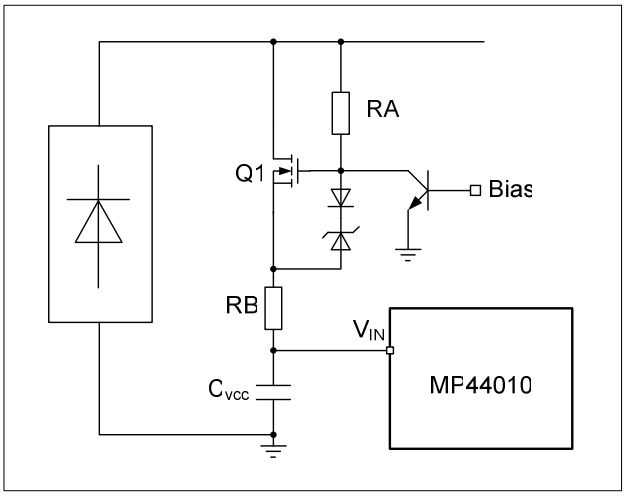
1) For the PFC stage, an NTC resistor is widely used to avoid high inrush current. When the circuit enters steady state, the resistor continuously generates power loss. To reduce this part of power loss, it is suggested that the NTC resistor is placed between the rectified diode and output cap because there is less current flowing through the NTC resistor.

2) There is some power loss associated with the EMI filter; it is mainly due to the resistance of CM choke and DM choke. Therefore, using chokes with low resistance is recommended.

3) Start-up resistor also continuously generates power loss. As start-up resistor selection section on Page 12 described, the start-up resistor is selected based on acceptable start-up time. That means shorter start-up time is, bigger power consumption on start-up resistor is (see figure (1) as below). So in some cases, the power loss caused by start-up resistor may be very considerable. Therefore, a fast start-up circuit is recommended to shorten start-up time and reduce power consumption (see figure (2) as below):



(1) Start-up using start-up resistor



(2) Start-up using high-voltage current source

Figure15—Start-up circuit

During start-up, the GS voltage of Q1 is clamped by zener diode due to no voltage on C_{vcc}. So C_{vcc} could be charged by Q1 and RB. When the voltage of C_{vcc} reaches to setting value, Q1 could be turned off so that the power consumption could be sharply reduced.

4) At light load, the downstream stage would run into burst mode. Therefore, the power loss of PFC stage can be reduced by synchronized ON/OFF of the PFC stage and the downstream stage. For example, MP44010 can be synchronized by HR1000 to reduce the light load power loss. Figure 12 shows the recommended circuit.

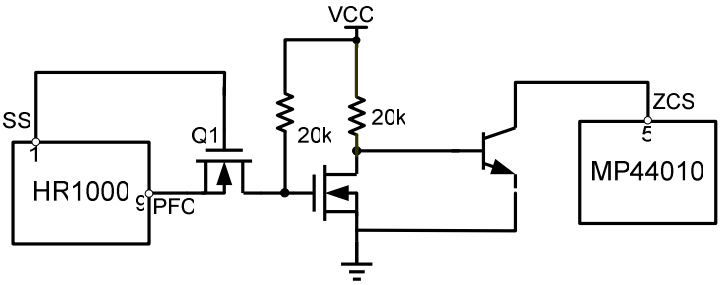


Figure 16—Circuit to synchronize between MP44010 and HR1000 at light load

5) At light load, the power loss can be further saved by inserting LN60A01 to disconnect the resistor of voltage divider. The implement circuit is shown in the Figure 17.

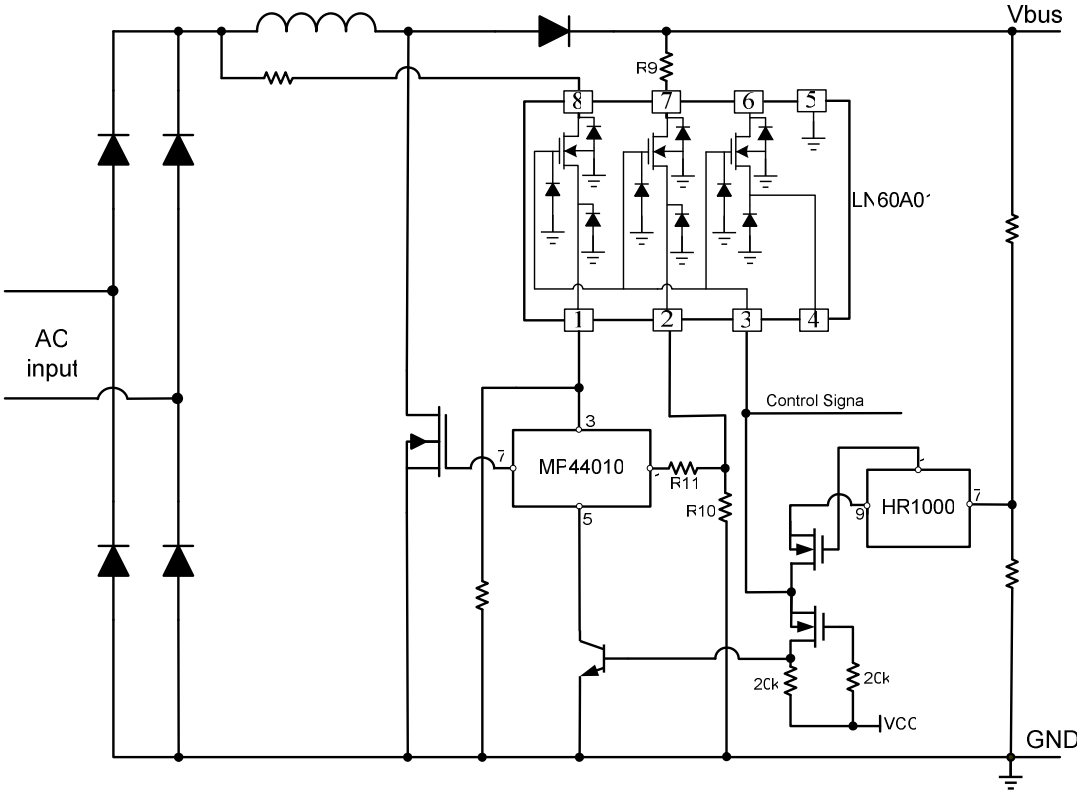


Figure 17—Power Consumption Reduction with LN60A01

At light load, the pin 9 (PFC) of HR1000 is asserted low when it operates at burst mode, and the signal generated from pin 9 is applied to synchronize the ON/OFF of MP44010; it also can drive LN60A1 to connect or disconnect resistor of voltage divider at the same time. And the control signal of LN60A01 also can be external signal from MCU system.

It's important to select proper R11, because at light load, R11 could affect OVP of MP44010. To avoid triggering dynamic OVP wrongly, R11 should be chosen to follow the below equation:

$$R11 \geq \frac{\frac{R10}{R9+R10} V_{bus\_OVP} - 2.5}{40 \cdot 10^{-6}}$$

b. Improving power factor (PF).

Having a low enough bandwidth can guarantee that PF is not affected by output ripple.

The EMI filter is also important for PF. Too large of an X-cap for the DM filter can cause big phase shift of input current and result in poor PF, especially at high line condition. Therefore, under the same EMI performance, smaller X-cap helps to provide good PF.

If having a big X-cap is necessary, a small cap from MULT pin to GND is recommended to improve PF at high line. This cap is used to compensate the phase shift of input current caused by X-cap. There will be trade-offs with this since this technique may lower the PF at low line.

DESIGN EXAMPLE

Input AC RMS voltage: V_{ac}=220V (V_{ac_min}=85V–V_{ac_max}=265V)

Output DC voltage: V_O = 400V

Output voltage ripple: V_{O_ripple}≤10V

Output voltage OVP threshold: ΔOVP=40V

Output power: P_O=100W (constant power load)

Efficiency: η_{max}=97%, η_{min}=93%

Minimum switching frequency: f_{sw_min}=40kHz

Design of power stage components:

(1) Bridge Diode

The maximum input RMS current is:

$$I_{ac\_max} = \frac{P_o}{\eta_{min} \cdot V_{ac\_min}} = 1.265 \text{ (A)} \quad (1)$$

To provide enough margin, GBU406 (600V/4A) is selected.

(2) Input capacitor

By setting the coefficient r as 0.05, the input capacitance can be obtained by using the formula below:

$$C_{in} = \frac{I_{ac\_max}}{2\pi \cdot f_{sw} \cdot r \cdot V_{ac\_min}} = 1.03 \times 10^{-6} (F) \quad (2)$$

A 1μF tantalum capacitor with 450V voltage rating is selected as the input capacitor to provide high frequency energy during switching cycle.

(3) Inductor

The inductance should be calculated based on the given specs:

$$L = \frac{V_{ac\_max}^{2} (V_o - \sqrt{2} V_{ac\_max}) \cdot \eta_{max}}{2 f_{sw\_min} \cdot P_o \cdot V_o} = 5.4 \times 10^{-4} (H) \quad (3)$$

Set the inductance as 550μH.

The needed Ap is:

$$A_p = A_e \cdot A_w = \frac{L \cdot I_{Lpk} \cdot I_{Lrms}}{B_{max} \cdot K_c \cdot j} = 6.84 \times 10^{-9} \ (mm^4) \quad (4)$$

Consider EI core, the EI30 core is selected according to above Ap.

The inductor turn number is:

$$N_p = \frac{L \cdot I_{Lpk}}{B_{max} \cdot A_e} = 51 (Turn) \quad (5)$$

The needed air gap is:

$$\sigma = \frac{N_p^{2} \cdot A_e \cdot \mu}{L} = 6.54 \times 10^{-4} (m) \quad (6)$$

The maximum turn ratio of main to auxiliary winding is:

$$N_{max} = \frac{V_o - \sqrt{2} V_{ac}}{ZCS_{rising\_max}} = 10.9 \quad (7)$$

With some margin, the turn ratio is set as N=6.

And the turn number of auxiliary winding is:

$$N_s = \frac{N_p}{N} = 8 (Turn) \quad (8)$$

(4) Power MOSFET

The maximum RMS current of MOSFET is:

$$I_{Qrms\_max} = 2\sqrt{2} I_{ac\_max} \cdot \sqrt{\frac{1}{6} - \frac{4\sqrt{2}}{9\pi} \cdot \frac{V_{ac\_min}}{V_o}} = 1.26 (A) \quad (9)$$

The pulsed-drain current should be:

$$I_{D\_pulse} > I_{Lpk} = 3.578 (A) \quad (10)$$

The CoolMOS IPP50R350CP (500V/9A) is selected to meet the power requirement of the design.

(5) Output diode

The average current of the output diode is:

$$I_{Do}=I_o=\frac{P_o}{V_o}=0.25(A) \quad (11)$$

Super-fast recovery diode MUR160 (600V/1A) is selected to meet the design.

(6) Output capacitor

Here, the output capacitor is selected only based on output voltage ripple and ESR of output capacitor is assumed as 0.2Ω:

$$C_o=\frac{1}{2\pi\cdot 2f_{line}\sqrt{\left(\frac{\Delta V_o}{2I_o}\right)^2-ESR^2}}=8\times10^{-5}(F) \quad (12)$$

The E-cap (450V/100μF) is selected as the output capacitor.

Design of control circuit:

(1) Calculate start-up resistor

With 3s start-up time, the start-up resistor can be roughly calculated as:

$$R_{start}=\frac{T_{start}(\sqrt{2}V_{ac}-V_{IN\_th})}{C_{vcc}\cdot V_{IN}+I_q\cdot T_{start}}=1.27\times10^6(\Omega) \quad (13)$$

A 1MΩ resistor is selected to meet the calculation.

(2) Calculate MULT resistor divider

Maximum MULT pin voltage should be selected within the linear operating range (0~3V). Considering some margin, the maximum MULT pin voltage is set as 2.5V.

So:

$$V_{MULT\_min}=V_{MULT\_max}\frac{V_{ac\_min}}{V_{ac\_max}}=0.8\,(V) \quad (14)$$

Then maximum CS pin voltage can be calculated as:

$$V_{CS\_max}=1.62\cdot V_{MULT\_min}<1.6V \quad (15)$$

The below value is lower than CS clamp voltage (1.6V).

The MULT resistor divider ratio can be obtained using the below equation:

$$\frac{R1}{R1+R2}=\frac{V_{MULT\_max}}{\sqrt{2}V_{ac\_max}} \quad (16)$$

Select 1.5MΩ as R1 and 10kΩ as R2.

(3) Calculate current sense resistor R8

Based on the above calculation, the current sense resistor should meet:

$$R8\le\frac{V_{CS\_max}}{I_{Lpk}}=0.363\,(\Omega) \quad (17)$$

Select 0.3Ω as sensing resistor to meet the above design.

(4) Calculate ZCS resistor R5

The ZCS resistor should meet the below equation:

$$R5 \geq \frac{V_{aux\_max} - V_{ZCDclamp\_H}}{2.5 \times 10^{-3}} = 1.688 \times 10^{4}\ (\Omega) \quad (18)$$

Select 68kΩ resistor as the ZCS resistor.

(5) Feedback resistor divider

$$R9 = \frac{\Delta V_{OVP}}{I_{OVP}} = 1 \times 10^{6}\ (\Omega) \quad (19)$$

Select a 1MΩ resistor as a high-side feedback resistor. In addition, attention to the package size of this resistor is needed, due to its power loss.

$$R10 = \frac{2.5}{V_o - 2.5} \cdot R9 = 6.29 \times 10^{3}\ (\Omega) \quad (20)$$

Select 6.34kΩ resistor as low-side feedback resistor.

(6) Calculate compensation circuit

Based on the above parameter calculation, the compensation network can be calculated according to small signal model analysis in previous section.

Step1: Set design goal, f_c=15Hz, f_I=0.1Hz, $G_{EA}(2f_L)$=-50dB and f_{cz}=10Hz.

Then C4 and R6 can be calculated:

$$C4 = \frac{1}{2 \cdot \pi \cdot R9 \cdot f_I} = 1.592 \cdot 10^{-6}\ (F) \quad (21)$$

Selecting C4=1.6uF

$$R6 = \frac{1}{2 \cdot \pi \cdot f_{cz} \cdot C4} = 9.947 \cdot 10^{3}\ (\Omega) \quad (22)$$

Selecting R6=10kohm

Due to $\left|G_{VC}(f_c)\right| = 43.154$ dB, then f_{cp} can be calculated.

$$f_{cp} = 2 \cdot f_L \cdot 10^{\frac{\left|G_{EA}(f_{cp})\right| - \left|G_{EA}(2f_L)\right|}{20}} = 45.465\ (Hz) \quad (23)$$

So C5 can be calculated too:

$$C5 \approx \frac{1}{2 \cdot \pi \cdot R6 \cdot f_{cp}} = 3.159 \cdot 10^{-7}\ (F) \quad (24)$$

Selecting C5=0.33uF

Finally, the bode plots of $G_{VC}(s)$, $G_{EA}(s)$ and T(s) are shown in the below figure:

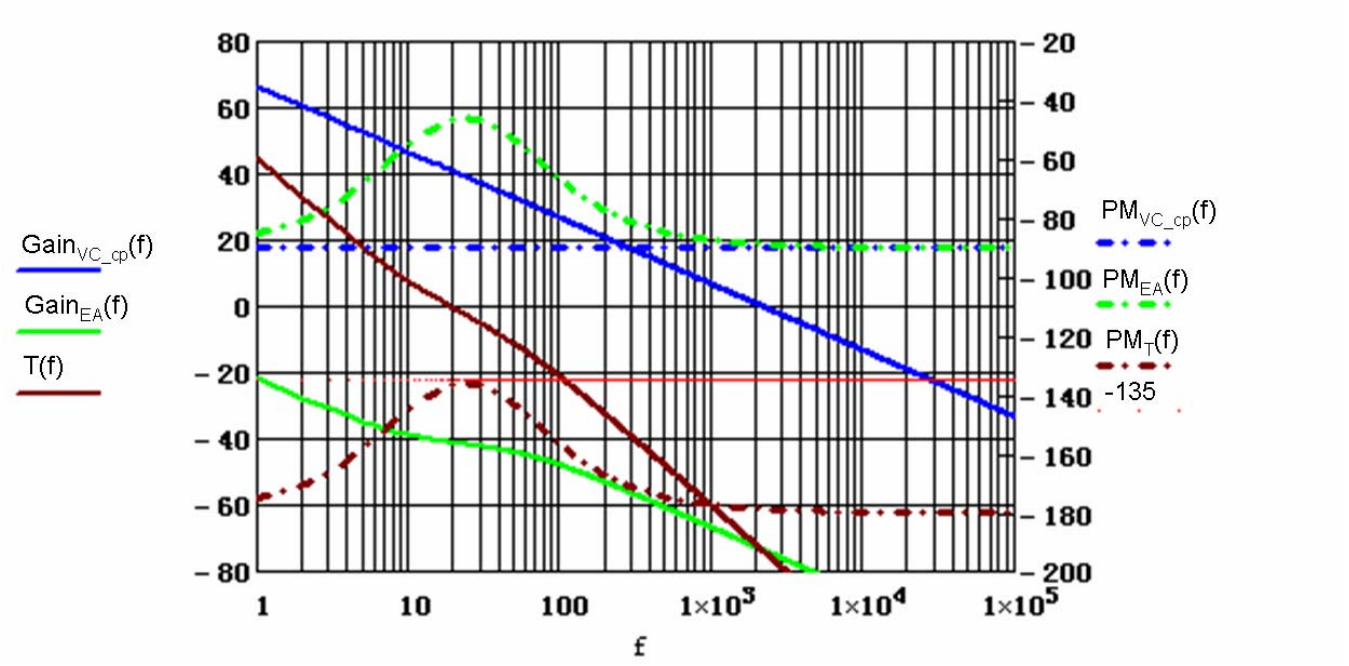


Figure 18—Final Bode Plot of the Compensation Network

From Figure18, we can see the fc is change to 20Hz, the reason is using the simplified formula to calculate it. The phase margin is about 45^o, the result can meet our design target.

The final schematic of the design is shown in the Figure 19.

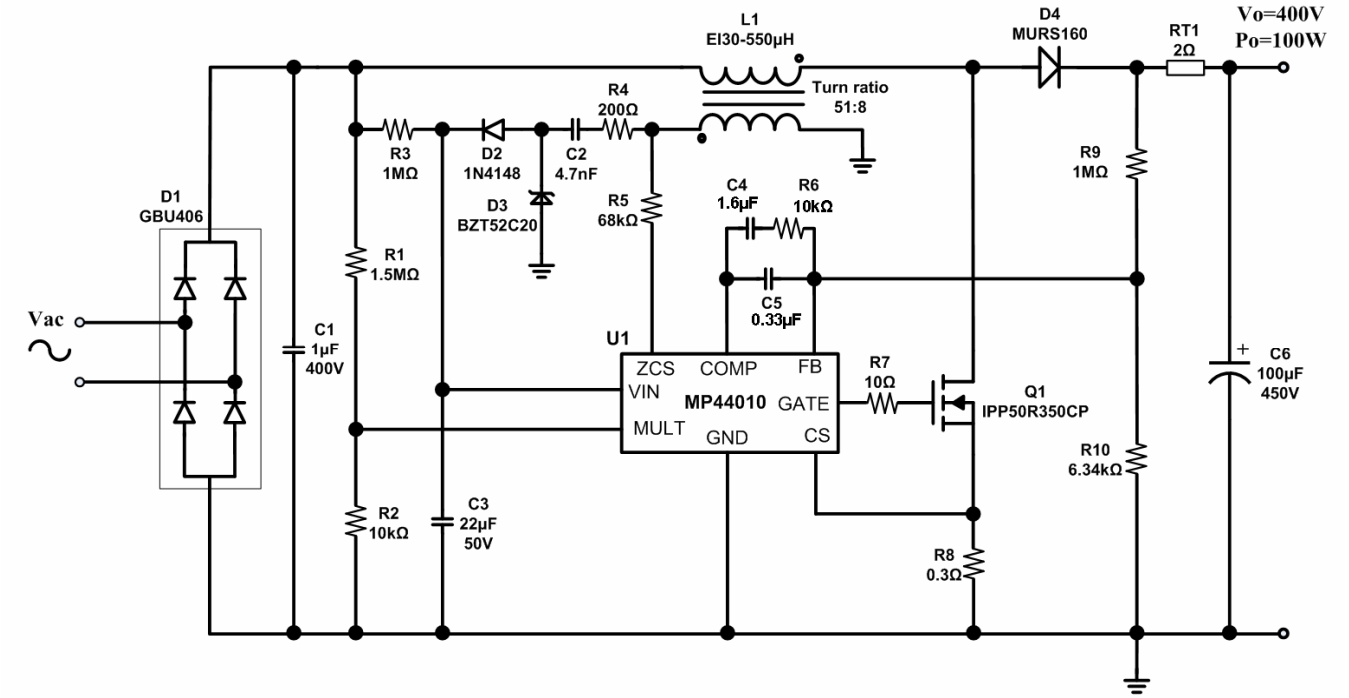


Figure 19—100W Boost PFC Design Example

REFERENCES:

[1]. Lloyd H. Dixon, “Magnetics Design for Switching Power Supplies,” in Unitrode Magnetics Design Handbook, 1990.

[2]. Yuri Panov and Milan M. Jovanovic, “Small-Signal Analysis and Control Design of Isolated Power Supplies with optocoupler feedback,” IEEE trans. Power Electronic., vol.20, NO.4, pp. 823-832, July 2005.

[3]. Robert W. Erickson and Ragan Maksimovic, Fundamentals of Power Electronics (Second Edition). Kluwer Academic Publishers, 2001

[4]. MP44010 Datasheet-MPS