MP4030: Application Note for a TRIAC-Dimmable, Offline LED Controller with Primary-Side Control and Active PFC

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1. INTRODUCTION

The MP4030 is a TRIAC-dimmable, offline, LED lighting controller with primary-side control and active PFC. The proprietary TRIAC dimming scheme increases the dimming range and avoids random flickering.

The primary-side-control significantly simplifies the LED lighting driving system by eliminating the opto-coupler and the secondary feedback components for an isolated single stage converter. Its proprietary real-current control method can accurately control the LED current from primary-side information.

The MP4030 has a power factor correction (PFC) function that can achieve a power factor (PF)>0.9 within a universal input voltage range. The device also works in boundary conduction mode to reduce switching loss and improve EMI performance.

The MP4030 has an integrated charging circuit at the VCC pin to start-up with a delay of less than 200ms when using a 22μF bulk capacitor. The low-voltage current source outputs a maximum 16mA charging current.

The MP4030 provides multiple advanced fault protections to enhance the system safety, including over-voltage protection, short–circuit protection, primary-side over-current protection, VCC under-voltage lockout, and thermal shutdown: all protections features auto-restart.

Figure 1 shows a typical application.

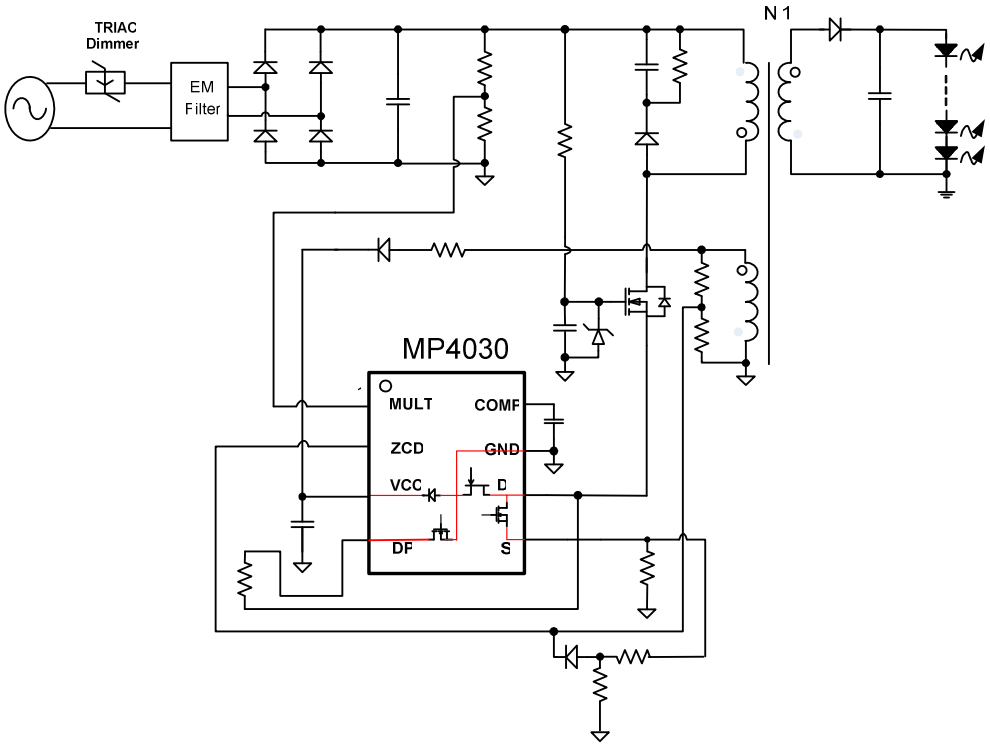

Figure 1: Typical Application

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2. PRIMARY-SIDE CONTROL, BOUNDARY-CONDUCTION MODE WITH ACTIVE PFC

Conventional off-line LED drivers use secondary-side control that senses the LED current directly. An error amplifier compares this current level against a reference produced by a device such as a TL431, and the compensated output determines the primary-side duty cycle to regulate the LED current. Although this control method can directly control the LED current and current accuracy under any condition, it requires additional secondary-side components—including a sensing circuit, comparison and compensation circuits, an opto-coupler, and bias power supplies—that significantly increase system complexity and cost.

In addition, the primary-side input stage typically uses a full-wave rectifier bridge with an E-cap filter to generate a DC voltage. The E-cap must be large enough to limit the DC voltage ripple. This means the instantaneous input line voltage is lower than the DC voltage on the E-cap for most of a line half-cycle, and that the rectifier diodes only conduct a small portion of the voltage. This voltage limitation causes the input line current to act like a series of narrow pulses whose amplitudes are about 10x higher than the average DC level. The drawbacks include: a high current peak and RMS current drawn from the line, line-input–current distortion limiting the power factor to about 0.5 to 0.6, and large induced harmonics.

Figure 1 shows that the MP4030 uses primary-side control, which eliminates secondary feedback components to significantly reduce the component count and cost. The MP4030 also works in boundary-conduction mode with active PFC, with a power factor >0.9 for the input, and reduce THD to meet IEC61000-3-2 requirements.

A. PRIMARY-SIDE CONTROL

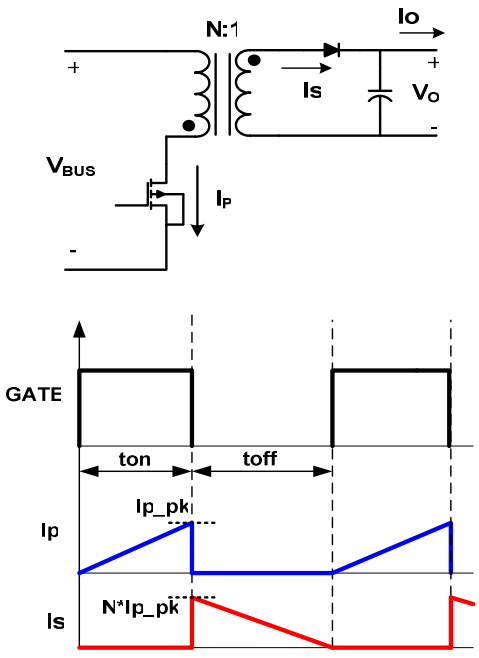

Figure 2: Transformer Currents Relative to the BCM Flyback Converter

Given that the LED current is the average current of the transformer's secondary side, $I_o = I_{s_avg}$, as shown in Figure 2, the average secondary-side current in boundary-conduction mode can be calculated as:

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$$I_{s_avg} = \frac{\frac{1}{2} \cdot N \cdot I_{p_pk} \cdot t_{off}}{t_{on} + t_{off}}$$

Where I_{s_avg} is the average secondary-side current, and I_{p_pk} is the peak primary-side current. The MP4030 samples the primary-side peak current to calculate the average current. Since the average current is proportional to the output current, if the average current is a controlled constant, the output current is also constant, allowing for primary-side control.

B. BOUNDARY-CONDUCTION MODE

The MP4030 works in boundary conduction mode where the transformer functions at the boundary between the continuous and discontinuous mode.

In a conventional fixed-frequency flyback converter working in discontinuous conduction mode (DCM), the primary switch (MOSFET) turns on at a fixed frequency and turns off when the current reaches the desired level. When the MOSFET turns off, the energy stored in the inductor forces the secondary side diode to turn on, and the inductor current decreases linearly from the peak value to zero. When the current drops to zero, the parasitic resonance of the magnetizing inductor and the sum of the parasitic capacitance causes the MOSFET drain-source voltage to oscillate. The MOSFET can turn on at any point during the parasitic resonance, including when the drain voltage is lower than the bus voltage (meaning low switching losses and high efficiency), and when the drain voltage is much higher than the bus voltage (meaning high switching loss). This feature is observable in the efficiency curves of a discontinuous flyback converter with a constant load as input-voltage efficiency fluctuations as the turn-on switching loss changes with the turn-on drain voltage.

In boundary conduction mode, the switch does not have a fixed switching frequency. Instead, the controller always turns on the switch when the drain voltage goes low by detecting the auxiliary winding voltage, V_{ZCD}, the ZCD voltage is a ratio of primary winding and auxiliary winding. Figure 3 shows that by setting the falling-edge detection near zero, the parasitic resonance causes the ZCD voltage to decrease when the secondary side current deceases to zero: Conversely, when V_{ZCD} reaches the detection threshold, the MOSFET turn-on signal triggers. The transformer magnetizing inductance, parasitic capacitance, and ZCD filtering capacitor determine the detection time delay. The feedback loop determines the switch-on time, similar to conventional peak-current–mode control. The energy stored in the magnetizing inductor then transfers to the output.

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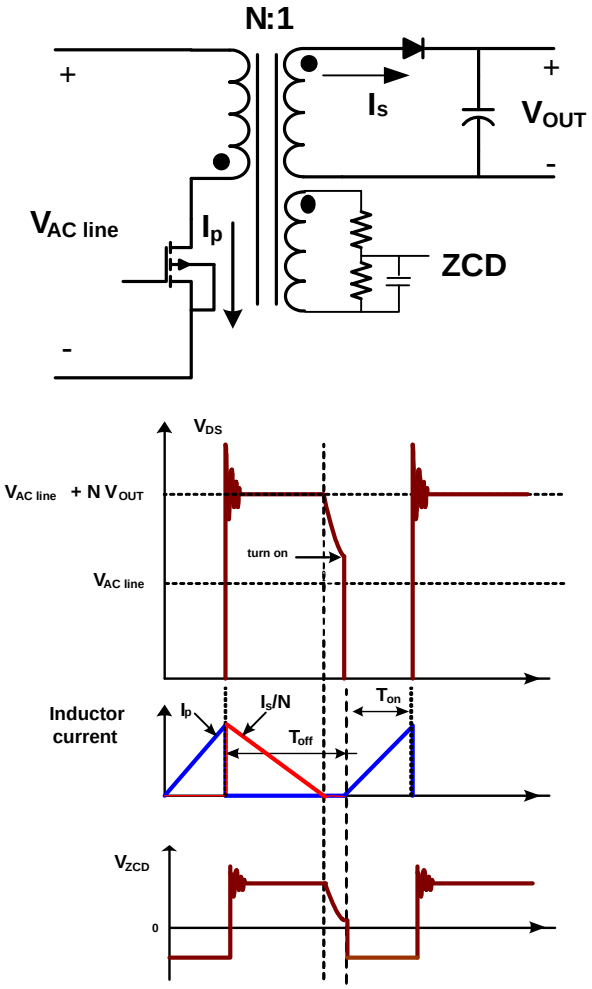

Figure 3: Boundary Conduction Mode

Compared to conventional flyback under continuous conduction mode (CCM) and DCM operation, boundary-conduction mode operation minimizes the turn-on switching loss, thus increasing efficiency and suppressing the MOSFET temperature rise.

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C. ACTIVE PFC

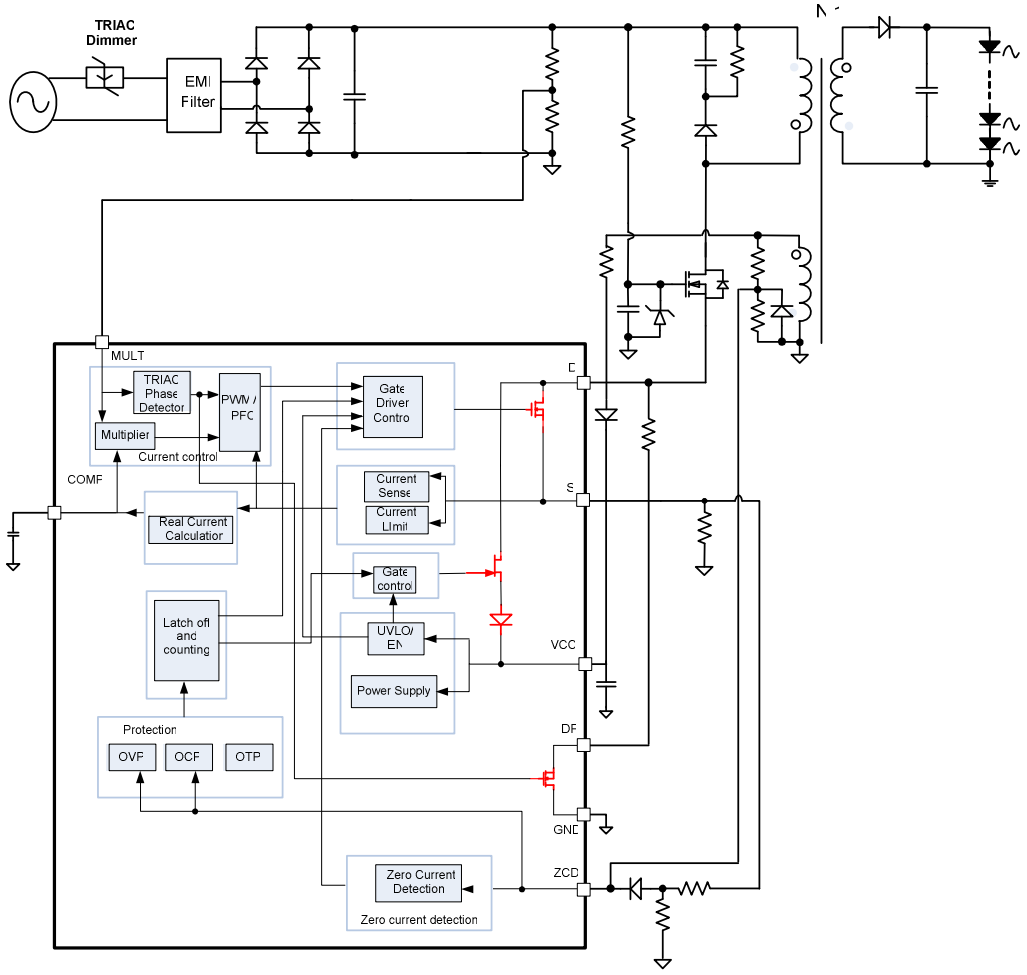

Figure 4: Functional Block Diagram and LED Driver

The MP4030 integrates active an PFC function. Figure 4 shows the functional block diagram and the LED converter driver. The converter consists of an EMI filter, a diode bridge rectifier, a flyback circuit using the MP4030. The following description summarizes converter operation with active PFC:

The diode bridge rectifies the AC line voltage, which then goes to the flyback circuit. When the internal main MOSFET turns on, the transformer's primary-side current ramps up from zero. The S pin senses this primary-side current through a sensing resistor, and this signal goes to the real-current calculation block to calculate its average value. The internal error amplifier compares the average value against an internal reference to generate an error signal that is proportional to the difference between them. If the bandwidth of the error amplifier is narrow enough (below 20Hz), then the error signal is a DC value for over a line half-cycle and kept constant until the average value equals the reference: This regulates the output LED current to a required constant value.

The error signal goes to the multiplier block with a portion of the rectified mains voltage. The resulting signal is a rectified sinusoid with a peak amplitude that depends on the peak line voltage and the value of the error signal. The output of the multiplier goes to the negative input of the current comparator to act as a sinusoidal reference for the PWM. When the S-pin voltage equals the value on the negative input of the current comparator, the external MOSFET turns off. The rectified signal envelops the peak primary current. and has the same phase as the main input voltage to implement a good power factor.

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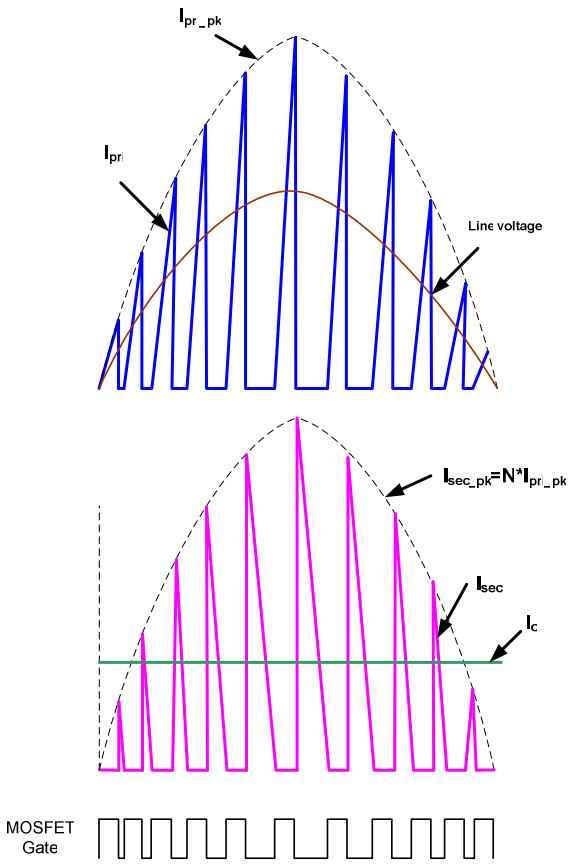

Figure 5: Primary and Secondary Transformer Currents and MOSFET Gate Timing

Figure 5 shows both transformer currents and the gate timing. The operating frequency increases as the instantaneous line voltage decreases; when the line voltage approaches the zero-crossing point, the frequency increases dramatically. The MP4030 has an internally-set 5μs minimum off-time to limit the maximum switching frequency and to improve efficiency and reduce EMI.

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3. PIN FUNCTION AND OPERATION INFORMATION

A. PIN INTRODUCTION

Pin1 (MULT)

The MULT pin provides one of the inputs to the internal multiplier. Connect this pin to the tap of the resistor divider from the rectified instantaneous line voltage, which will produce a sinusoidal multiplier output. This output signal provides the reference for the current comparator, which shapes the primary peak current into a sinusoid that is in-phase, with the input line voltage. The MULT pin also provides for TRIAC dimming phase detector (page 16) and DP MOSFET gate control (page 14).

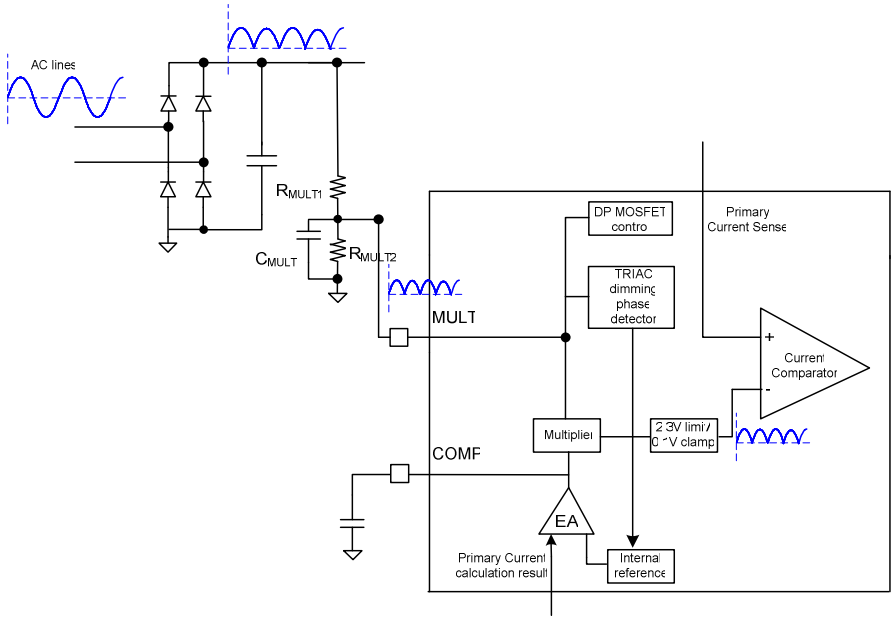

Figure 6: MULT Circuit

For the multiplier to operate at linear zone, select a MULT voltage range smaller than 3V. The multiplier output is then given by:

$$V_{multiplier_out} = k \cdot V_{MULT} \cdot (V_{COMP} - 1.5)$$

Where k is the gain of the multiplier.

The MULT voltage also determines the COMP voltage level for the system control loop. In real applications, setting the MULT pin too low cause the COMP voltage to saturate the 5V SCP point; setting the MULT pin too high causes the COMP voltage to below its 1.9V clamp voltage. For TRIAC dimming, the COMP voltage directly influences the dimming curve (page 17), so tune the MULT voltage carefully.

The multiplier output has two clamps: The 2.3V high clamp is for primary cycle-by-cycle current limiting, the 0.1V low clamp signals the output gate driver to pull down the line voltage during the TRIAC dimming OFF interval.

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Pin2 (ZCD)

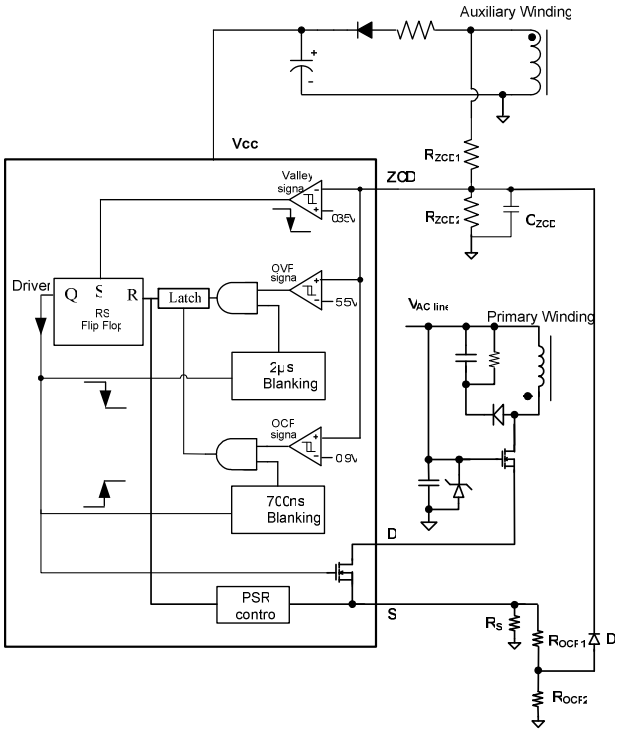

Figure 7: ZCD Circuit

Figure 7 shows the ZCD pin circuitry. The ZCD pin connects to the auxiliary winding through a resistor divider (R_{zcd1}, R_{zcd2}). The ZCD pin integrates three functions: One detects the secondary-side–current zero-crossing condition by monitoring the auxiliary winding voltage for BCM; The second function is to implement the output over voltage protection by comparing the ZCD voltage to the internal 5.5V reference; The third function is to activate the over-current protection (OCP) by sensing the primary-side current.

The internal gate turn-on signal triggers when the ZCD pin voltage falling-edge from the resistor divider goes below 0.35V, with a 0.55V hysteresis. The MP4030 switching frequency varies instantaneously with the input line voltage. To limit the maximum frequency and improve EMI and efficiency performance, the MP4030 employs an internal minimum OFF-time limiter of 5μs, as shown in Figure 8. When the input line voltage crosses the zero point, the primary current is very small and cannot turn the secondary diode on, so the ZCD does not receive the turn-on signal for the next duty cycle. To avoid unnecessary IC shutdown, the MP4030 integrates an auto starter that starts timing when the MOSFET turns off. If the ZCD fails to send out another turn-on signal after 122μs, the starter will automatically send out a turn-on signal.

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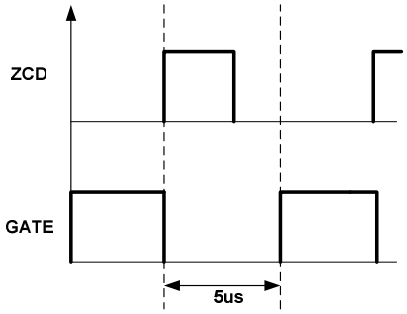

Figure 8: Minimum Off Time

Output over-voltage protection (OVP) works by detecting the auxiliary-winding voltage's positive plateau, which is proportional to the output voltage. Once the ZCD pin voltage exceeds 5.5V, the OVP signal triggers and latches, the gate driver turns off, and the VCC voltage decreases. When the VCC drops below 7V, the IC resets and restarts. The following equation estimates the output OVP set point:

$$V_{out_OVP} \cdot \frac{N_{aux}}{N_{sec}} \cdot \frac{R_{zcd2}}{R_{zcd1} + R_{zcd2}} = 5.5V$$

Where V_{out_OVP} is the output OVP setting voltage, N_{aux} is the number of transformer auxiliary windings, and N_{sec} is number of secondary windings. Consider that the ZCD falling-edge detection delay time (when coupled with the ceramic bypass capacitor) increases with larger resistor values, reducing the output LED current: limit the delay time to <1.5μs. To avoid OVP mis-triggers caused by switch-off oscillation spikes, the MP4030 integrates an internal T_{OVPS} blanking time for the OVP detection—typically 2μs (see Figure 9).

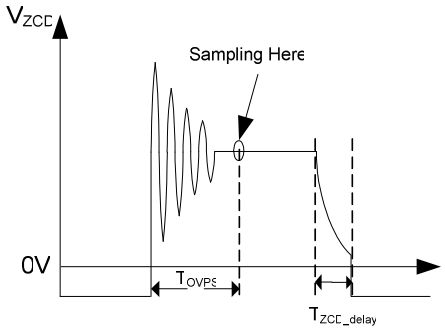

Figure 9: ZCD Voltage with Blanking Time

Selecting for R_{ZCD1} and R_{ZCD2} requires taking the ABS voltage and ZCD current into consideration. The ZCD pin's negative ABS voltage of ZCD pin is internally clamped at –8V and its source current is 5mA. Turning the primary MOSFET on applies a large negative voltage to the auxiliary winding, and may cause the ZCD pin to reach its negative voltage limit—the R_{ZCD1} and R_{ZCD2} values must be large enough to limit the ZCD pin source current to below 5mA.

Connecting a resistor divider from the S pin sensing resistor to ZCD pin, as shown in Figure 7, implement over-current protection (OCP). When the main MOSFET on the primary-side turns on, the ZCD pin monitors the rising primary-side current through the resistor divider. Once the ZCD pin reaches OCP threshold (typically 0.9V) after a 700ns blanking time, the OCP signal triggers and latches. The gate driver turns off to prevent over-current damage. The IC works in quiescent mode: VCC d

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ecreases, and when VCC drops below the 7V UVLO threshold, the IC resets and the system restarts. The primary-side OCP setting point can be calculated as:

$$I_{p_OCP} \cdot R_s \cdot \frac{R_{OCP2}}{R_{OCP1} + R_{OCP2}} - V_D = 0.9$$

Where I_{P_OCP} is primary-side OCP value and V_D is the diode voltage drop. Note that when the MOSFET is on, the taps of the ZCD resistor divider and the OCP resistor divider are connected by a diode. Therefore, set the resistor values of the OCP threshold (R_{OCP1} & R_{OCP2}) much smaller than the ZCD resistors (R_{ZCD1} & R_{ZCD2}) to minimize the ZCD influence.

The primary OCP method is also a good protection method for output SCP because it can be considered an over-load condition: The COMP voltage rises, causing the primary peak current to also rise. The primary OCP triggers when the primary peak current reaches the setting threshold.

Pin3 (VCC)

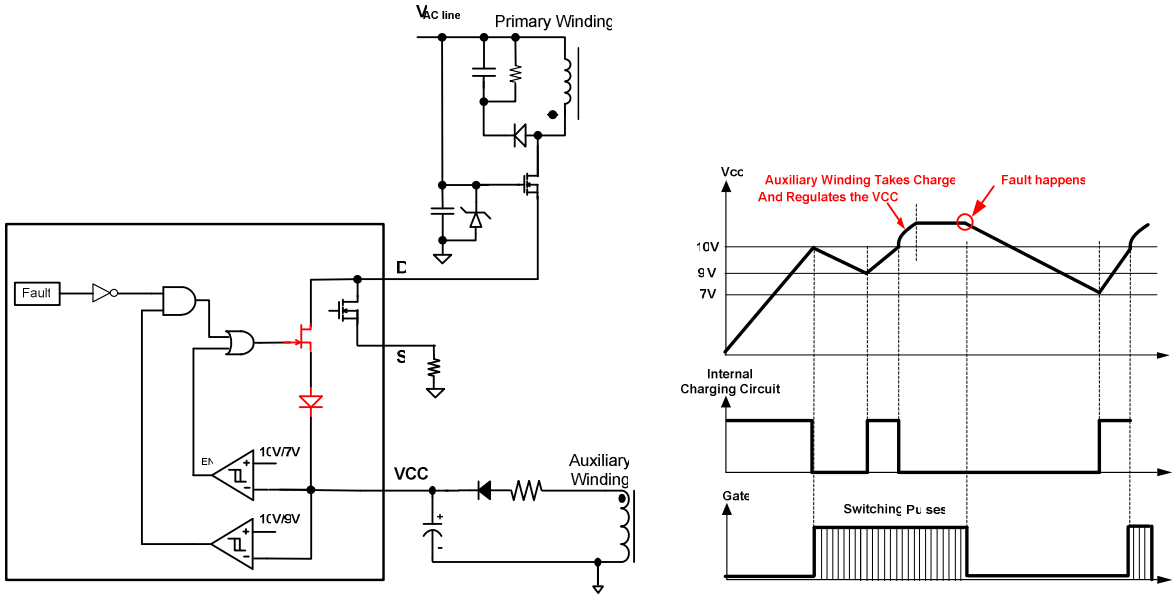

Figure 10: VCC Circuit and Power Supply Flow-Chart

VCC powers both the internal logic circuit and the gate driver signal. Figure 10 shows the VCC circuit and the power supply flow-chart. The gate of high-side MOSFET charges quickly in the presence of an AC power supply, then VCC is charged through the internal charging circuit from the AC line. When VCC reaches 10V, the internal charging ceases, then the control logic and the internal main MOSFET begin to function. Then the auxiliary winding provides power.

The initial auxiliary-winding positive voltage is low and so the VCC level drops. Once VCC drops below a 9V threshold, the internal charging circuit triggers and to charge VCC to 10V again until the auxiliary winding can take over. If any fault occurs, the switching and the internal charging circuit will stop and latch, and VCC will drop. When the VCC drops to 7V, the internal charging circuit recharges to restart the device. A bulk capacitor connected to VCC determines the system start-up time and the VCC fall time under fault and TRIAC-dimming conditions. A large bulk capacitor results a long start up time but slows the VCC voltage drop under deep TRIAC-dimming conditions. Most applications call for a 22μF electrolytic capacitor.

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Pin4 (DP)

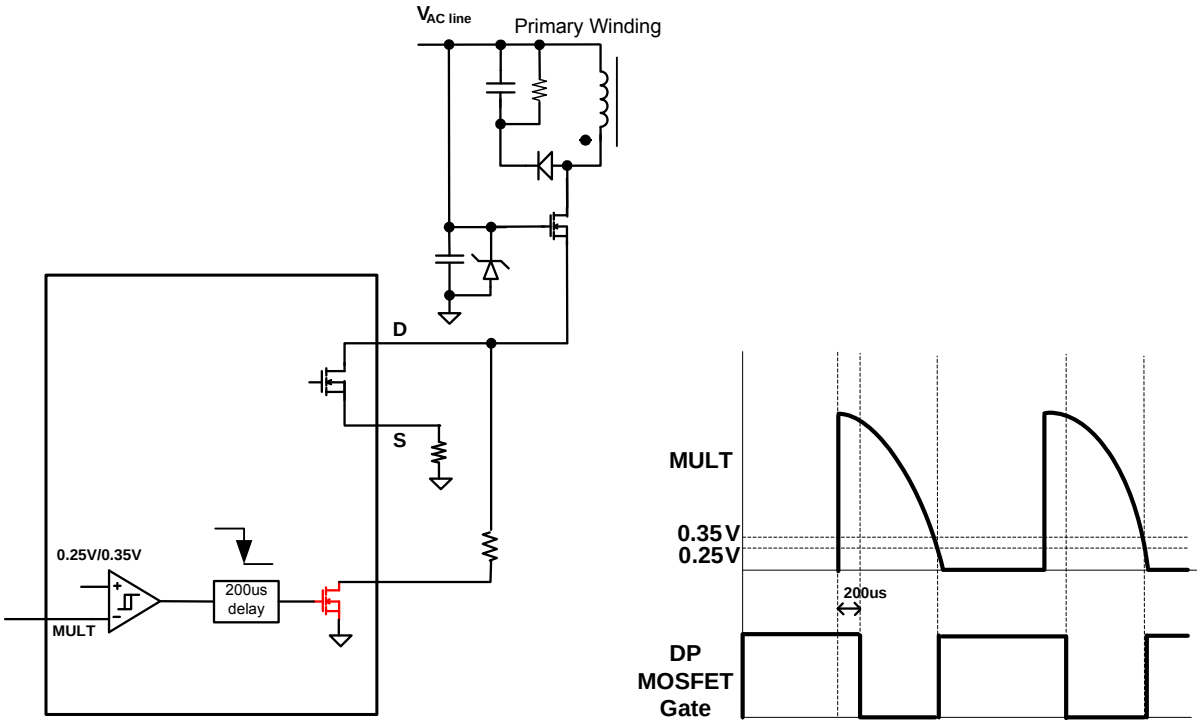

Figure 11: DP Circuit and Gate Driver Logic

The DP pin is the drain of the internal pull-down dimming MOSFET. The MULT voltage controls the MOSFET, as shown in Figure 11. If the IC detects the system is connected as dimming mode, the DP MOSFET turns on when the MULT voltage drops below 0.25V,. Conversely, when the MULT voltage exceeds 0.35V, the MOSFET turns off after a 200μs delay. For TRIAC dimming, connect a resistor from the DP pin to D to pull down the input line voltage during the TRIAC OFF interval and accurately detect the dimming phase on the MULT pin to avoid unwanted flickering. This resistor also provides a pull-down current branch when TRIAC dimming starts, and improves TRIAC turn-on performance during short dimming phases by supplementing the latch current to the TRIAC.

Pin5 (S)

The S pin senses the primary-side current through a sensing resistor. The resulting voltage goes to the current comparator with the multiplier output to determine the MOSFET turn-off time, and the average-current calculation block to calculate the average primary-current value. A stable system loop produces a primary average value, $I_{p_avg} \times R_S$, equal to the internal reference, V_{ref}. Combined with the equation on page 5, the output LED mean current can approximated as:

$$I_o = \frac{N \cdot V_{ref}}{2 \cdot R_s}$$

Where N is the turn ratio of the primary and secondary windings, V_{ref} is the internal reference voltage (typically 0.4V), and R_s is the sensing resistor connected between the main MOSFET source and GND.

An internal leading-edge blanking (LEB) unit between the S pin and the internal feedback avoids premature switching-pulse termination due to the parasitic capacitance discharging during turn-on. The internally-fed path is blocked during the blanking time. Figure 12 demonstrates the leading-edge blanking time.

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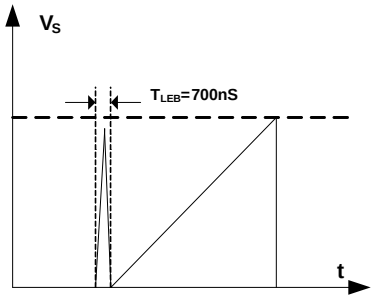

Figure 12: Leading-Edge Blanking

Pin6 (D)

Figure 13 shows the D-pin circuit. The D pin is the drain of the main, internal, low-side MOSFET. This pin also connects the internal VCC charging path to the source of the external high-side MOSFET. Under normal conditions, the main, internal, low-side MOSFET has a break-down voltage of 30V. When the MOSFET is OFF, the D voltage is the ratio of the high-side MOSFET and the low-side MOSFET voltages. The D voltage may exceed the break-down voltage and damage the device: Adding a Zener diode from the D-pin to the high-side MOSFET gate helps to clamp the D-pin voltage.

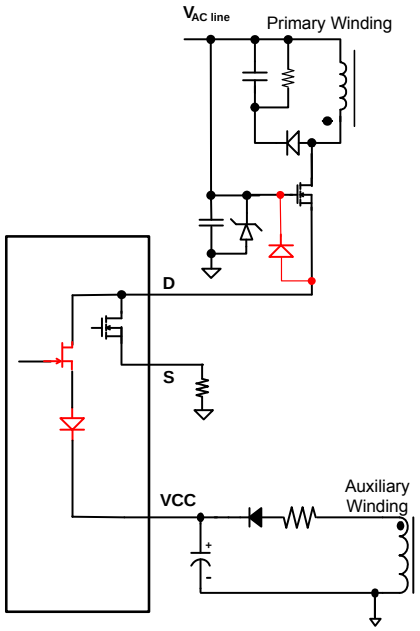

Figure 13: D-Pin Circuit

Pin7 (GND)

The Ground (GND) pin provides the current return for both the control and the gate-drive signals. Connect the power and analog GNDs at this pin only for PCB layout. The power GND (PGND) provides the reference for the power switches, and the analog GND (AGND) for the control signals.

Pin8 (COMP)

Loop compensation pin. Connect a compensation capacitor from this pin to AGND. Use a low-ESR ceramic capacitor, such as X7R. The COMP pin is the output of the internal error amplifier. To limit the loop bandwidth <20Hz for good PFC performance, select a capacitor value between 2.2μF and 10μF. A larger capacitor results in a smaller COMP voltage ripple for better thermal, EMI, steady-state performance, but also means a longer soft-start time.

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The COMP is also used for SCP. An output short can be considered an over-load, so the COMP voltage rises. Once the COMP voltage reaches 5V, the SCP signal triggers and latches, switching stops, and VCC decrease. When VCC drops below the 7V UVLO threshold, the IC resets and the system restarts.

B. TRIAC DIMMING

The MP4030 can implement TRIAC-based dimming. The TRIAC dimmer consists of a bi-directional SCR with adjustable turn-on phase. Figure 14 shows the leading-edge TRIAC dimming waveforms.

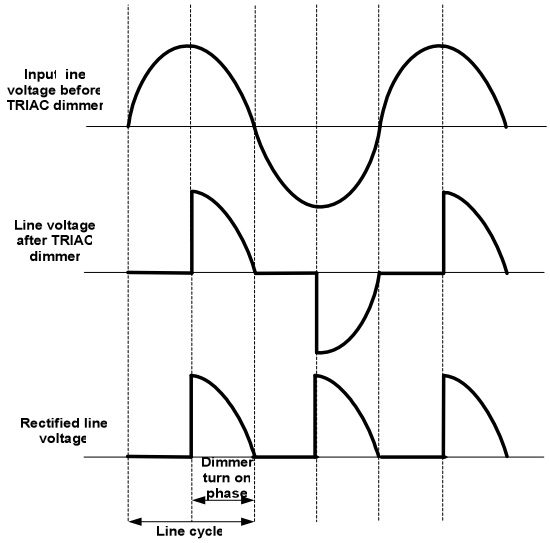

Figure 14: TRIAC Dimming Waveforms

The MP4030 will detect the dimming turn on cycle on MULT pin and fed into the control loop for adjusting the internal Reference voltage. When MULT voltage is higher than 0.35V, it will be recognized as dimmer turn on, when MULT voltage is lower than 0.15V, it will be recognized as dimmer turn off. The MP4030 has a 25% of line cycle detection blanking time at each line cycle, the real phase detector output is plus this time, shown in figure 15. That means if the turn on cycle is bigger than 75% of the line cycle, the output is kept at the same maximum current. It can help improve the line regulation in maximum TRIAC turn on cycle or without dimmer application.

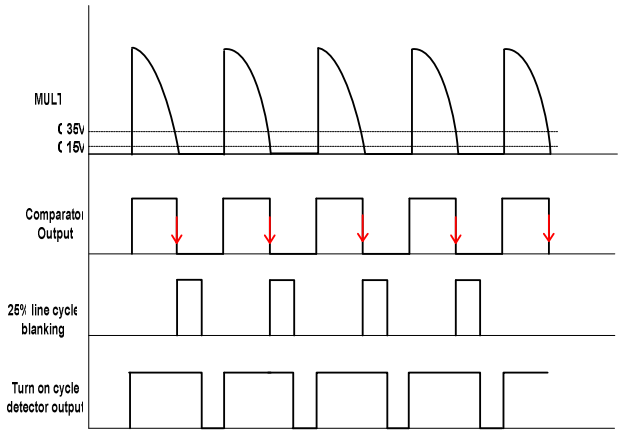

Figure 15: Dimmer Turn-On Cycle Detection

If the turn-on cycle decreases to <75%×(line cycle), the internal reference voltage decreases linearly with the falling dimming turn-on phase, and the output current decreases accordingly.

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The COMP voltage decreases with the falling dimming turn-on cycle. Once the COMP voltage reaches 1.9V, it is clamped so that the output current decreases slowly. This clamping helps maintain the TRIAC holding current to shift the TRIAC turn-off point closer to the line-voltage zero-crossing point to avoid random flicker caused by large phase differences between the TRIAC-current zero-crossing point and the input-line–voltage zero-crossing point.

Figure 16 shows the relationship between the dimming turn-on phase and the output current. The output current turning point happens when COMP voltage is clamped at 1.9V, so the COMP voltage will influence the output current dimming curve. The MULT pin voltage also adjusts the COMP voltage level. However, a low COMP voltage narrows the dimming range, and a high COMP voltage can cause random flickering. For typical applications, the COMP voltage is usually set between 2.2V and 2.3V without dimming.

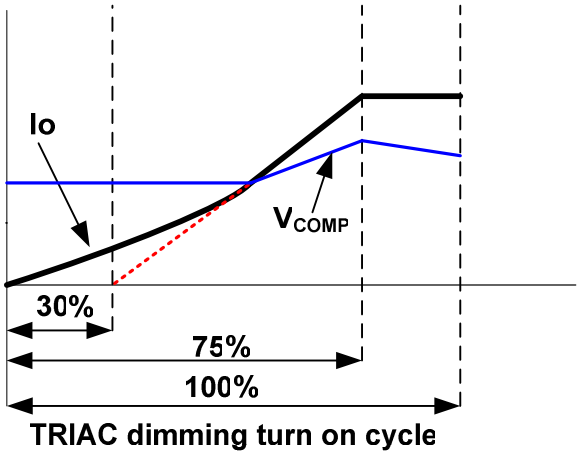

Figure 16: Dimming Curve

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4. DESIGN EXAMPLE: TRIAC-DIMMABLE, HIGH-PERFORMANCE, 8W LED LUMINAIRE DRIVER

A. SPECIFICATIONS

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Supply Voltage	V_{IN}	2 Wire	108	120	132	VAC
AC Line Frequency	f_{LINE}			60		Hz
Output Voltage	V_{OUT}	7 LEDs in series		22		V
LED Current	$I_{LED(MAX)}$	Without connecting dimmer		350		mA
Continuous Output Power	P_{OUT}			8		W
Efficiency	η	Full load, with out connecting dimmer	80%			
Power Factor			0.9			
Conducted EMI			Meets EN55015			
Harmonics			Meets IEC61000-3-2 Class C Limitation			
Surge			Meets IEC61547 surge requirement			

B. Schematic

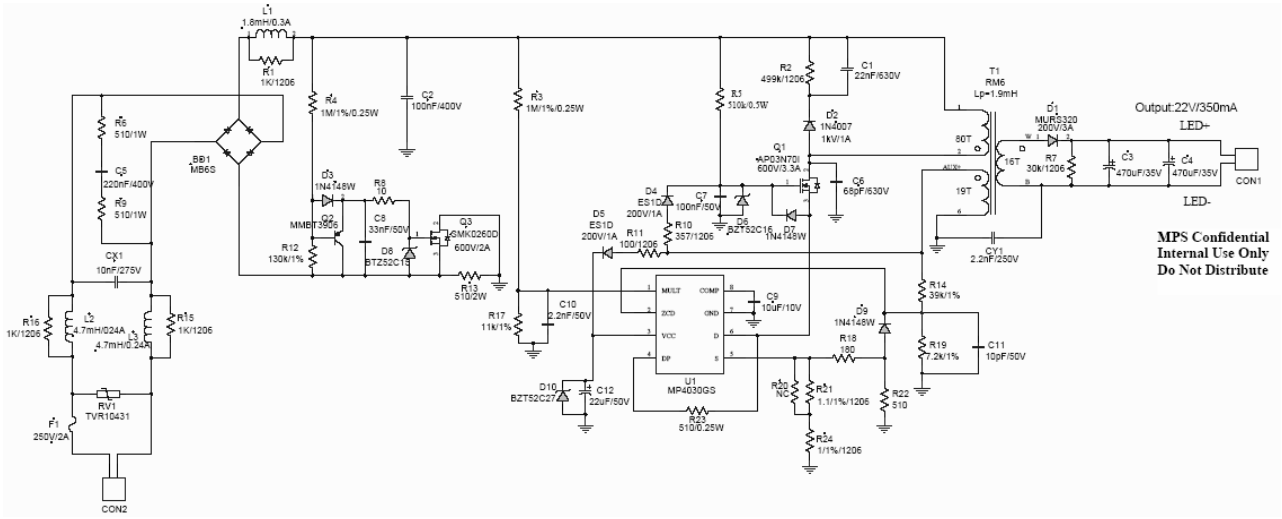

Figure 17: Example Application Schematic—8W Luminaire Driver

C. TURN RATIO (N), PRIMARY MOSFET, AND SECONDARY-RECTIFIER–DIODE VOLTAGE RATING SELECTION

The following provides a design example given the following conditions:

- V_{ac_min}=108V
- V_{ac_max}=132V
- $V_{in_max}=\sqrt{2}\cdot V_{ac_max}$
- $V_{in}(V_{ac},t)=\left|\sqrt{2}\cdot V_{ac}\cdot\sin(2\cdot\pi\cdot f_{line}\cdot t)\right|$

Figure 18 shows a typical drain-source voltage waveform for the primary high-side MOSFET and he secondary rectifier diode. From the waveform, the maximum primary high side MOSFET Drain-Source

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voltage rating V_{P-MOS_max} is

$$V_{P-MOS_max} = V_{in_max} + N \cdot V_o + 150 \quad (1)$$

Where 150V is the assumed maximum spike voltage, and is related to the RCD snubber.

The maximum secondary rectifier diode voltage rating, V_{DIODE_max}, is

$$V_{DIODE_max} = \frac{V_{in_max}}{N} + V_o + 40 \quad (2)$$

Assuming the maximum voltage spike is 40V.

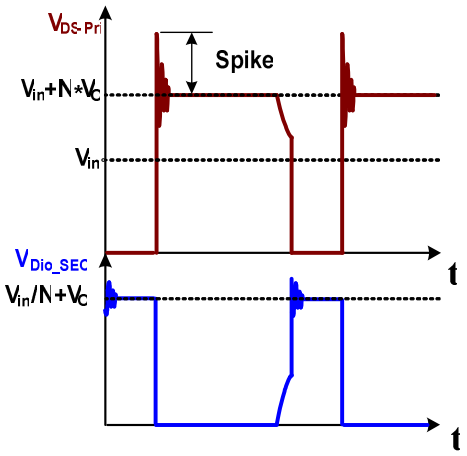

Figure 18: Drain-Source Voltage of the Primary MOSFET and the Secondary Rectifier Diode

Figure 19 shows the voltage rating curves of the primary MOSFET and secondary rectifier diode versus the turn ratio, N, based on equations (1) and (2). N can be determined by the required MOSFET and rectifier diode voltage ratings.

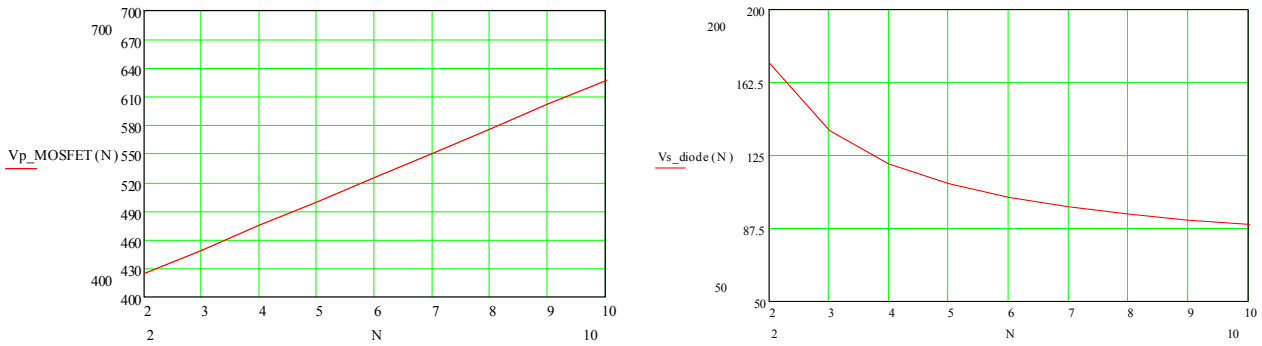

Figure 19: Votage Ratings for the Primary MOSFET and the Secondary Rectifier Diode as a function of Turn Ration, N

Some applications allow for N to be selected from within a range, which then requires the following considerations:

- A small N means a smaller T_{on}/T_{off} ratio, as per equation (5), which leads to a poor THD
- A large N leads to a large primary inductance and a physically larger transformer.

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Based on the stated conditions, N=5, so 600V or 650V MOSFET and a 100V or 200V Schottky or fast-recovery diode suffices for this particular design example.

D. TRANSFORMER DESIGN

Primary Inductance, L_P

It is possible to demonstrate that the MP4030 produces a constant ON-time over each line half-cycle, given:

- $V_S = R_s \cdot V_{in} \cdot \frac{\tau_{on}}{L_m}$, and
- $V_{Multipier} = K_1 \cdot K_2 \cdot V_{in} \cdot (V_{COMP} - 1)$, since
- $V_{CS} = V_{Multiplier}$,
- then $\tau_{on} = \frac{L_m \cdot K_1 \cdot K_2 \cdot (V_{COMP} - 1)}{R_s}$

Where L_m is the primary inductance, R_s is the current sensing resistor, K_1 is the multiplier gain, K_2 is the ratio of the MULT pin voltage vs. the line voltage, and V_{COMP} can a constant DC value when decoupled with a large COMP capacitor. The turn-off time varies with the instantaneous line voltage.

$$\tau_{on} = \frac{L_p \cdot I_p}{V_{in}(V_{ac}, t)} \quad (3)$$

$$\tau_{off} = \frac{L_p \cdot I_p}{N \cdot V_o} \quad (4)$$

for

$$\tau_{off}(\tau_{on}, V_{ac}, t) = \frac{V_{in}(V_{ac}, t) \cdot \tau_{on}}{N \cdot V_o} \quad (5)$$

Considering the τ_{off} limit within MP4030, the τ_{off} equation should be modified as:

$$\tau_{OFF}(\tau_{ON}, V_{ac}, t) = \begin{cases} \frac{V_{in}(V_{ac}, t) \cdot \tau_{ON}}{N \cdot V_o} \text{ if } \frac{V_{in}(V_{ac}, t) \cdot \tau_{ON}}{N \cdot V_o} > 5\mu s \\ 5\mu s, \text{otherwise} \end{cases} \quad (6)$$

Figure 20 shows that the output LED current equals the average value of the secondary winding current during a half-line cycle. Equation (7) shows that the output current is the sum of the secondary current in each cycle to produce an average value.

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$$I_o(a,b,T_{on},V_{ac},L_p) = \left| \begin{array}{l} t1 \leftarrow a \\ sum \leftarrow 0 \\ while(t1 < b) \\ \left| sum \leftarrow sum + \frac{1}{2} \cdot \left\{ \left[\frac{V_{in}(V_{ac}, t1+\tau_{on}) \cdot \tau_{on}}{L_p} \right] \cdot N \right\} \cdot \tau_{off}(\tau_{on}, V_{ac}, t1+\tau_{on}) \right. \\ \left| t1 \leftarrow t1 + \tau_{on} + \tau_{off}(\tau_{on}, V_{ac}, t1+\tau_{on}) \right. \\ \frac{sum}{b-a} \end{array} \right. \quad (7)$$

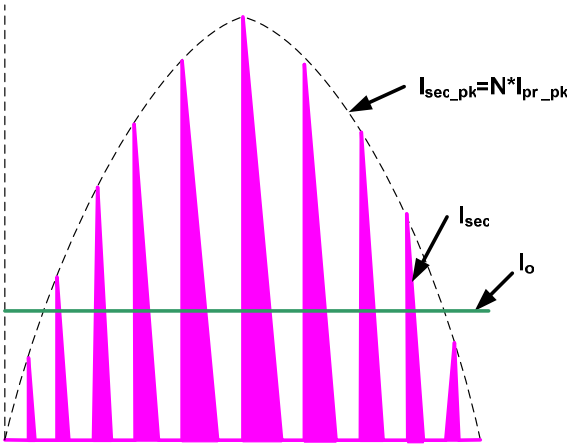

Figure 20: Secondary-Side Current

Usually, the system will define a minimum frequency, f_{s_min}, at $V_{in} = \sqrt{2} \cdot 108 \sin(\frac{\pi}{2})$, and sets the minimum switching frequency, f_{s_min}=80kHz.

$$I_o(0,0.01,\tau_{ON_108V},108,L_p) = 0.35A \quad (8)$$

$$f_{s_min} = \frac{1}{\tau_{ON_108V} + \tau_{OFF}(\tau_{ON_108V},108,0.005)} = 80kHz \quad (9)$$

Combining (8) and (9) gets L_P=1.9 mH, τ_{ON_108}=5μs.

The maximum primary-peak current is:

$$I_{pk_max} = \tau_{ON_108V} \cdot \frac{V_{in}(108,0.005)}{L_p} = 0.398A \quad (10)$$

When estimating L_P, the maximum operation frequency occurs when V_{in} approaches the zero crossing at 132VAC.

$$f_{s_max} = \frac{1}{\tau_{ON_132V} + \tau_{OFF}(\tau_{ON_132V},132,0)} = 107kHz \quad (11)$$

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The Primary-Winding RMS Current:

$$I_{pri_rms}(a,b,T_{on},V_{ac},L_p) = \left| \begin{array}{l} t1 \leftarrow a \\ sum \leftarrow 0 \\ while(t1 < b) \\ \left| sum \leftarrow sum + \left\{ \frac{1}{\tau_{on} + \tau_{off}(\tau_{on}, V_{ac}, t1 + \tau_{on})} \int_0^{\tau_{on}} \left(\frac{V_{in}(V_{ac}, t1 + \tau_{on}) \cdot t}{L_p} \right)^2 \cdot dt \right\} \cdot \right. \\ \left[\tau_{on} + \tau_{off}(\tau_{on}, V_{ac}, t1 + \tau_{on}) \right] \\ t1 \leftarrow t1 + \tau_{on} + \tau_{off}(\tau_{on}, V_{ac}, t1 + \tau_{on}) \\ \\ \sqrt{\frac{sum}{b - a}} \end{array} \right. \quad (12)$$

The maximum primary RMS current is then:

$$I_{pri_rms_max} = I_{pri_rms}(0,0.01,\tau_{ON_108V},108,1.9 \cdot 10^{-3}) = 0.11\,A \quad (13)$$

The secondary winding RMS current:

$$I_{sec_rms}(a,b,T_{on},V_{ac},L_p) = \left| \begin{array}{l} t1 \leftarrow a \\ sum \leftarrow 0 \\ while(t1 < b) \\ \left| sum \leftarrow sum + \left\{ \frac{N^4 \cdot V_o^{\,2} / L_p^{\,2}}{\tau_{on} + \tau_{off}(\tau_{on}, V_{ac}, t1 + \tau_{on})} \int_0^{\tau_{off}(\tau_{on}, V_{ac}, t1 + \tau_{on})} \left(\frac{V_{in}(V_{ac}, t1 + \tau_{on}) \cdot \tau_{on}}{N \cdot V_o} - t \right)^2 \cdot dt \right\} \cdot \right. \\ \left[\tau_{on} + \tau_{off}(\tau_{on}, V_{ac}, t1 + \tau_{on}) \right] \\ t1 \leftarrow t1 + \tau_{on} + \tau_{off}(\tau_{on}, V_{ac}, t1 + \tau_{on}) \\ \\ \sqrt{\frac{sum}{b - a}} \end{array} \right. \quad (14)$$

The maximum secondary winding RMS current is:

$$I_{sec_rms_max} = I_{sec_rms}(0,0.01,\tau_{ON_108V},108,1.9 \cdot 10^{-3}) = 0.62\,A \quad (15)$$

The Transformer Core Selection

Select the transformer core based on output power for the entire operating frequency. Ferrite is common in flyback transformers. The core area product ($A_E \cdot A_W$)—which is the core magnetic cross-section area multiplied by the available window area for winding—typically provides an initial core-size estimate for a given application. The following provides a rough estimate of the required area product:

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$$A_E \cdot A_W = \left(\frac{L_p \cdot I_{Pk_max} \cdot I_{rms_max}}{B_{max} \cdot K_u \cdot K_j} \right) cm^4 \quad (16)$$

Where:

- K_u is winding factor which is usually 0.2 to 0.3 for an off-line transformer,
- K_j is the current-density coefficient (typically 0.06 A/m^2 for ferrite core),
- I_{Pk_max} and I_{rms_max} are the maximum peak current and RMS current of the primary inductor, and
- B_{max} is the maximum-allowed flux density under normal operation—which is usually preset to the saturation flux density of the core material (0.3T to 0.4T).

So the estimated minimum core area product is 0.026 cm^4.

Refer to the manufacture's datasheet to select an appropriate core with sufficient margins. Also, select a core shape to best meet the layout dimensions and audible noise limits. For this example, choosing an RM6 core provides better mechanical construction for suppressing audible noise compared to EE or EFD cores such that:

- A_E = 0.36 cm^2, A_W = 0.26 cm^2, $A_E \times A_W$=0.095 cm^4.
- The core magnetic path length: l_c=2.86 cm
- The relative permeability of the core material: $\mu_\gamma = 2400$

Primary and Secondary Winding Turns

The transformer's primary size requires a minimum number of turns to avoid saturating a given core size. The normal saturation specification is E-t, or the volt-second rating. The E-t rating is the maximum voltage, E, applied over t seconds (The E-t rating is identical to the product of inductance, L, and the peak current). Equation (17) estimates the minimum value of N_P to avoid the core saturation:

$$N_P = \frac{L_p \cdot I_{pk_max}}{B_{max} \cdot A_E} \times 10^4 \quad (17)$$

Where:

L_p = the primary inductance of the transformer (H)

B_{max}= the maximum allowable flux density (T)

A_E= the effective cross sectional core area (cm^2)

I_{pk_max}= the maximum primary peak current (A)

Select B_{max} to be smaller than the saturation flux density, B_{sat}. B_{max} selection also requires taking the transformer's high-temperature characteristics into account because B_{sat} decreases as the temperature increases. B_{max} also influences the transformer's audible noise: a small B_{max} can reduce audible noise given a narrow window area. For PC40 material, the B_{max} is set to 0.27 to get N_P=80.

The number secondary windings is a function of the turn ratio, N, and primary turn count, N_P:

$$N_s = \frac{N_p}{N} = 16 \quad (18)$$

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Wire Size

Once the number of windings have been determined, select the wire size to minimize the winding conduction loss and the leakage inductance. The winding loss depends on the RMS current value, and the wire length and cross section.

Determine the wire size from the winding's RMS current:

$$S_{pri} = \frac{I_{pri_rms_max}}{J} = 1.83 \cdot 10^{-2} (mm^2) \quad (19)$$

$$S_{sec} = \frac{I_{sec_rms_max}}{J} = 1 \cdot 10^{-1} (mm^2) \quad (20)$$

Where J is the current density of the wire, which is typically 6A/mm^2.

Due to the skin effect and proximity effect of the conductor, select a wire diameter less than 2×Δd (where Δd is the skin-effect depth):

$$\Delta d = \sqrt{\frac{1}{\pi \cdot f_{s_min} \cdot \mu \cdot \sigma}} = 0.27(mm) \quad (21)$$

Where μ is the conductor's magnetic permeability, which is usually equal to the permeability of a vacuum for most conductors (i.e. $4\pi \times 10^{-7}$ H/m). σ is the wire's conductivity (typically 6×10^7 S/m at 0° for copper, which increases with temperature).

If the requires wire diameter exceeds 2×Δd, use multiple strands of thinner wire or Litz wire to minimize the AC resistance. Select enough strands such that the effective cross sectional area meets the current density requirement.

In offline isolated applications, the whole system needs to pass the Hipot test, which requires taking the primary to secondary isolation distance into consideration. Small power systems typically use triple-insulated wire (TIW) as the secondary winding wire to enhance the isolation distance. Using TIW negates the need for a retaining wall and conserves the transformer window area.

This example uses 0.18mm×1 wire for the primary winding, 0.35mm×1 T.I.W for the secondary winding, so the wire area for the primary winding is S_1=2.54×10^{-2} mm^2, and for the secondary winding it is S_2=0.97×10^{-1} mm^2.

Auxiliary Winding Wire Size

The auxiliary winding's current requirement is relatively small because it primarily provides power to VCC and detects the current zero crossing for boundary-mode operation. The auxiliary winding's output DC voltage is proportion to the output LED voltage with a turn ratio of N_{aux}/N_s. VCC requires high stability so that the IC can continue to function even when dimming function goes very low. Most applications VCC to go as high as 25V. Given an LED output voltage of 16V, select N_{aux} as N_{aux}=25/16×N_s, so N_{aux}=19 for a 0.18mm wire.

Window-Area Fill-Factor Calculation

After selecting appropriate wire sizes, check whether the core window area can accommodate the windings. Calculate each winding's required window area, respectively, then add the areas together—be sure to take the interwinding insulation and spaces into consideration. The fill factor—the winding area relative to the whole core window area—should be well below 1 due to these interwinding insulation and spaces between turns. Select a fill factor no greater than 20%.

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$$\frac{N_p \cdot S_1 + N_s \cdot S_2 + N_{aux} \cdot S_3}{A_{W_RM6}} = 0.15 < 0.2 \quad (22)$$

If the required window area exceeds the selected one, reduce either the wire size or use a larger core. However, reducing the wire size increases the transformer copper loss.

Air Gap

With a selected core and winding turns, the core air gap is approximately:

$$G = \mu_0 \cdot A_E \cdot \frac{N_P^2}{L_p} - \frac{l_c}{\mu_r} = 0.3\,(\text{mm}) \quad (23)$$

Where A_E is the cross sectional area of the selected core, μ_0 is the permeability of vacuum which equals $4\pi \times 10^{-7}$ H/m., L_p and N_P is the primary winding inductance and turns respectively, l_c is the core magnetic path length and μ_r is the relative magnetic permeability of the core material.

Instructions for Transformer Manufacturing

The coupling between the transformer primary side and the secondary side must be as tight as possible to minimize leakage inductance. This can be accomplished be interleaving the primary and secondary windings during transformer manufacture, as shown in Figure 21. Start with the winding connected to the drain of the high-side MOSFET first, followed by the auxiliary winding, and then the secondary winding to isolate the secondary wind from the drain to reduce parasitic capacitance and to improve the CM EMI. To meet the safety requirements, separate the transformer's primary side and secondary side and keep a safe creepage distance of at least 6mm. Do not directly connect the auxiliary winding pin (AUX+) and the two secondary winding pins (W and B) to the transformer pins. Instead, use jumpers and connect externally, as per Figure22.

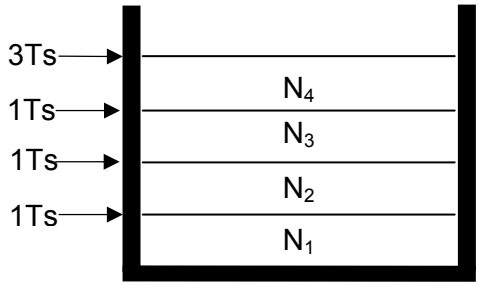

Figure 21: Transformer Winding Diagram

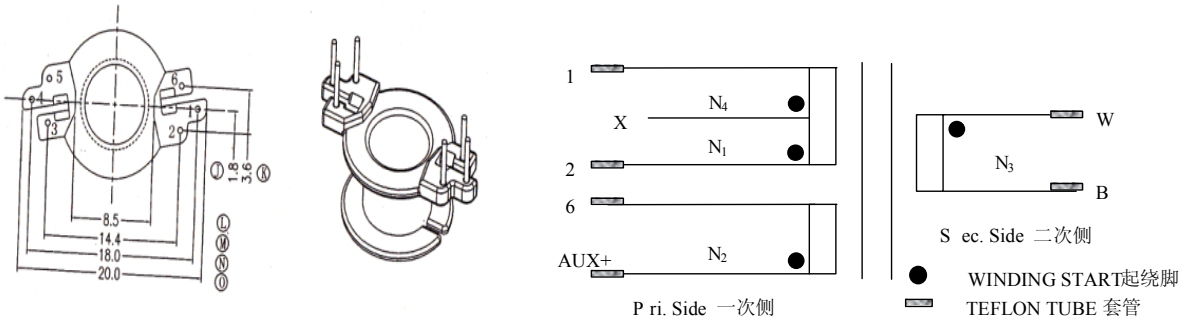

Figure 22: Transformer Pin Out and the Connection Diagram

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E. INPUT EMI FILTER (L1, L2, L3, CX1, CY1, C2)

The input EMI filter is comprised of L1, L2, L3, CX1, with the Y-class capacitor, CY1, and input film capacitor, C2. The EMI filter has two stages with –80dB attenuation for the DM noise. Soldering the L2 and L3 inductors to the L and N lines, respective, also acts as a CM noise filter. Select component values to pass EMI test standards, as well as to account for the power factor and inrush current when dimming turns on. The input capacitance plays the primary role: a small input capacitance increase the power factor and decreases the inrush current, so select a relatively small X capacitor.

F. INPUT BRIDGE (BD1)

The input bridge can use standard, slow-recovery, low-cost diodes. When selecting diodes, take into account these three items: the maximum input RMS current; the maximum input-line voltage; and thermal performance. The maximum input-line voltage occurs during surge conditions, where the surge voltage across the line may exceed 600V. This example uses MB6S as the BD, with a 600V, 0.5A rating.

G. INPUT CAPACITOR (C2)

The input capacitor, C2, mainly provides the transformer's switching frequency magnetizing current. The maximum current occurs at the peak of the input voltage. Limit the capacitor's maximum high-frequency voltage ripple to 10%, or the voltage ripple can cause the primary peak current to spike and worsen both the power loss and the EMI performance.

$$C2 > \frac{I_{pk_max} - \sqrt{2} I_{pri_rms_max}}{2 \cdot \pi \cdot f_{s_min} \cdot V_{ac_min} \cdot 0.1} = 44nF \quad (24)$$

Input capacitor selection requires taking into account the EMI filter, the power factor, and the surge current at the dimming turn-on time. A large capacitor improves EMI, but limits the power factor and increases the inrush current. This example uses a 100nF, 400V, film capacitor.

H. PASSIVE BLEEDER (C5, R6, R9) AND ACTIVE DAMPER (Q2, Q3, D3, D8, C8, R4, R8, R12, R13)

Since the LED lamp impedance is relatively large, significant ringing occurrs at leading edge TRIAC dimmer turn on due to a inrush current charging the input capacitance (shown in Figure 23). The ringing may cause the TRIAC current fall below the holding current and turn off the TRIAC, which can cause flickering.

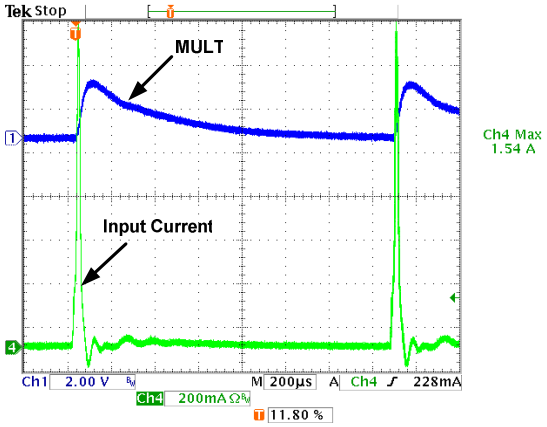

Figure 23: Input Current Ringing at the TRIAC's Leading-Edge Turn-On Period

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This example incorporates both a passive bleeder and an active damper circuit to address this issue. The passive bleeder consists of an RC circuit (C5, R6, and R9 in Figure 17) installed across the input line right before the bridge rectifier. Select a bleeder capacitance larger than the input capacitor, C2, and X capacitor, CX1, to limit the bleeder current-ringing frequency below the C2 and CX1 current ringing, as shown in Figure 24; the current through the TRIAC rises when the TRIAC turns on. However, increasing the capacitance increases the power dissipation and therefore decrease efficiency. Use the minimum acceptable value.

The bleeder resistor limits the bleeder current and damps the input current. The resistance requires fine-tuning: large resistors limit bleeder functionality, while small resistors limit damping and can lead to high-amplitude bleeder-current ringing. This examples uses 200nF, a total of 1.02kΩ, and a power rating of 2W.

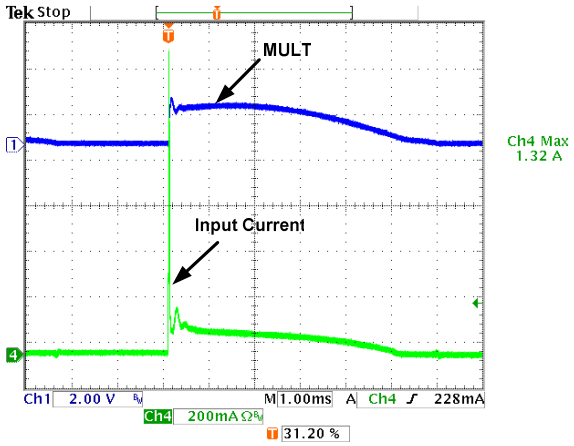

Figure 24: Input Ringing with Passive Bleeder

However, Only the passive bleeder is not enough to maintain conduction in the TRIAC for many kinds of different TRIACs, then a damper is needed. The purpose of the damper is to limit the inrush current that charges the input capacitance at TRIAC turning on. There are tow kinds of dampers, passive and active. Passive damper is simple, only need hire a resistor in series with the AC input line, limited by the power dissipation, values can not be large, the values are typically from 10 to 100Ω.The passive damper may suit for power less than 5W and the effective is strongly limited by the efficiency requirement. For higher power or higher efficiency design, an active damper is required. `Shown in figure 17, the active damper is consisted of Q2, Q3, D3, D8, C8, R4, R8, R12, and R13. Resistor R13 is used for limiting the inrush current and the value can be much higher than the passive case. R4, R12, C8 forms a 1ms delay time for R13 conduction, then the MOSFET turns on and short R13. Increasing the delay time by increasing the value of capacitor C8 can improve the damping result, but cause more power dissipation. When the rectified input voltage decreasing to low, the gate of Q2 is discharged by Q3 and turned off for the next turn on interval. Figure 25 shows the effect of adding both bleeder and active damper. The ringing is effectively suppressed.

I. OUTPUT CAPACITOR (C3, C4)

The output voltage ripple has two components: the switching-frequency ripple associated with the flyback converter, and the low-frequency ripple associated with the input-line voltage (120Hz). Selecting the output bulk capacitor depends on the output current, the allowable overvoltage, the desired voltage ripple, and with an LED load the LED current ripple. This example has a load of 7 LEDs in series, a 350mA output current, and a current ripple set within 40% without dimming. Since the LED impedance is not resistive, the output voltage ripple refers to the LED V-I characteristics as provided by the LED manufacturer to design the output voltage ripple within 2.5%.

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The maximum RMS current of the output capacitor is:

$$I_{out_cap_rms_max} = \sqrt{I_{sec_rms_max}^2 - I_{o_rms}^2} \quad (25)$$

Where I_{o_rms} is the output RMS current and $I_{sec_rms_max}$ is the maximum secondary RMS current from equation (15). Design the maximum RMS current to be smaller than the capacitor's RMS current specification.

The maximum switching voltage ripple occurs at the peak of the minimum-rated input line voltage, and the ripple (peak-to-peak) can be estimated by:

$$\Delta V_{o_swtiching} = \frac{I_{o_max} \cdot \tau_{off}(\tau_{on_108V}, 108, 0.005)}{C_{out}} + (I_{sec_pk_max} - I_{o_max}) \cdot R_{ESR} \quad (26)$$

Where I_{o_max} is the maximum instantaneous output LED current with a mean value of 350mA plus a 20% peak ripple; $\tau_{off}(\tau_{on_108V}, 108, 0.005)$ is the turn-off time at the peak of the minimum-rated input line, R_{ESR} is the ESR of output capacitor (typically 0.03Ω per capacitor), and $I_{sec_pk_max}$ is the maximum peak current of the secondary winding.

Estimate the maximum low-frequency ripple (2x the line frequency, 120Hz) from the capacitor impedance and the peak capacitor current (I_{o_max}).

$$\Delta V_{o_line} = I_{o_max} \sqrt{\frac{1}{(2\pi \cdot 2f_{line} \cdot C_{out})^2} + R_{ESR}^2} \quad (27)$$

Based on this equation, the 120Hz low-frequency ripper dominates the output voltage ripple. Set $\Delta V_{o_line} = 0.55V$ for C_{out}=1000μF. Selecting 470μF/35V bulk capacitors in parallel minimizes the ESR and distributes the capacitor RMS value. Add a 30kΩ pre-load resistor to discharge the output voltage under open-load conditions.

J. RCD Snubber (R2, C1, D2)

The peak voltage across the high-side MOSFET at turn-off includes the instantaneous input line voltage, the voltage reflected from the secondary side, and the voltage spike due to leakage inductance. The RCD snbber (shown in Figure 25) protects the MOSFET from over-voltage damage by absorbing the leakage inductance energy and clamping the drain voltage. The values of C1 and R2 depend on the leakage inductance energy dissipated by the RC network during each cycle. Figure 26 shows the primary high-side MOSFET output voltage ripple and the snubber capacitor at point A during the turn-off interval.

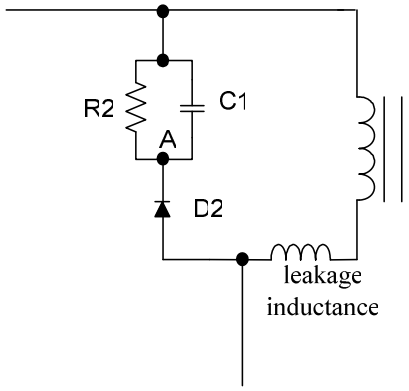

Figure 25: Primary-Side RCD Snubber

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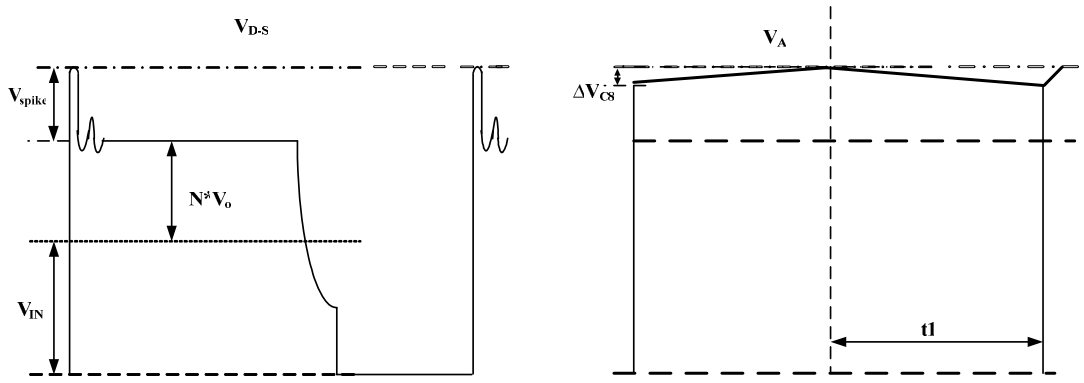

Figure 26: A Point Voltage with a High-Side MOSFET Drain Voltage and Snubber Capacitor

Estimate the energy stored in the leakage inductor at the maximum input voltage as:

$$E_{Lk_max} = \frac{1}{2} \cdot L_{leakage} \cdot I_{pk_V_{in_max}}{}^2 \quad (28)$$

Where $I_{pk_Vin_max}$ is the peak current for the primary side at the maximum input voltage. Assume all the leakage inductance energy transfers to the snubber capacitor. The secondary relationship is:

$$E_{Lk_max} = \frac{1}{2} \cdot C1 \cdot \left[(V_{in_max} + N \cdot V_o + V_{spike})^2 - (V_{in_max} + N \cdot V_o + V_{spike} - \Delta V_{C1})^2 \right] \quad (29)$$

Where V_{spike} is the spike voltage clamped by the RCD snubber, ΔV_{C1} is the snubber capacitor's voltage change caused by the leakage inductance.

Assuming $\Delta V_{C1} << V_{spike}$, and the $\frac{1}{4} \cdot 2\pi \cdot \sqrt{L_{leakage} \cdot C1} < \tau_{Vin_max}$,

$$\Delta V_{C1} = V_{spkie} \cdot (1 - e^{-\frac{t1}{R2 \cdot C1}}) \quad (30)$$

Where t1 is the time $\tau_{Vin_max} - \frac{1}{4} \cdot 2\pi \cdot \sqrt{L_{leakage} \cdot C1}$, and τ_{Vin_max} is the switching period at V_{in_max}.

To select R2, take into account the secondary-side reflecting voltage because it contributes to the snubber resistance after the MOSFET turns off. Select R2 to be large enough to reduce the reflecting voltage loss, but avoid contributing to a clamping voltage that exceeds the selected MOSFET based on equation (1).

Based on equations (6), (7), and (10), $I_{pk_Vin_max}$=0.36A, τ_{on_132V}=3.7μs, and τ_{vin_max}=10.5μs. The leakage inductance is estimated as 1% of the primary inductance, 20μH. Select the snubber parameters: C1=22nF, R2=499kΩ for V_{SPIKE}=150V and ΔVC1=0.13V.

Select a snubber capacitor with a higher voltage rating than the spike voltage, and a diode voltage rating higher than V_{in_max} + V_{spike}—use a normal-recovery diode, such as a 1N4007, which has better EMI performance than a fast-recovery diode. Given the difficulty in theoretically calculating the power dissipation of the snubber resistor R1, monitor the resistor's thermal performance during testing to determine the final appropriate value.

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K. HIGH-SIDE MOSFET GATE DRIVER (R5, R10, C7, D4, D6)

The rectified line voltage initially charges the high-side MOSFET gate through R5. C7 To stabilizes the gate voltage when line voltage goes low; typically 100nF suffices for most dimming conditions. Zener diode, D6, clamps the gate voltage to avoid damaging the MOSFET. Select a clamping voltage that exceeds 16V to ensure the VCC voltage can charge to 10V through point D. R5 and C7 introduces a delay; reducing R5 reduces the delay, but increases power dissipation. For C7 = 100nF, select R5 in the 510kΩ-to-1MΩ range for a delay time of less than 10ms— much shorter than the system start-up time.

Under deep dimming conditions the low line voltage can not remain the gate voltage ON without another power supply and ultimately limits dimming range or causes flickers. Connect an auxiliary winding through a rectifying diode improves the high-side MOSFET gate voltage for deeper dimming. Select the rectifying diode based on the voltage rating (as per equation (31)). Since the positive auxiliary winding voltage is 25V—which is higher than the 16V gate-clamping voltage—it needs a resistor to limit the current. The resistor value balance power dissipation and charging capability—this example uses a 357Ω resistor with a 0.25W power tolerance.

L. VCC POWER SUPPLY (R11, C12, D5, D10)

Page 13 shows the detailed VCC operation timing sequence. After system starts up, the auxiliary winding takes over the VCC power supply through a rectifying diode (D5) with a current-limiting resistor (R11). The bulk capacitor (C12) stabilizes the VCC voltage to limit the ripple—most applications use 22μF. Since the VCC maximum voltage is 30V, use a Zener diode (D10) to protect the VCC pin under open-load conditions, and to minimize the power dissipation. Set the clamping voltage as high as 27V. Use a relatively small current-limit resistor (R11) because of the limited power dissipation. Use the following equation to determine the D5 voltage rating:

$$V_{D5} > VCC_{max} + \frac{N_{aux}}{N_p} \cdot V_{in_max} + V_{aux_negtive_spike} \quad (31)$$

Where VCC_{max} is the maximum VCC voltage, in this case, VCC_{max}= 27V, N_{aux} and N_p are the auxiliary winding and primary winding turns, $V_{aux_negtive_spike}$ is the maximum negative spike on auxiliary winding, in this case, $V_{aux_negtive_spike}$= 40V, so D5 need a voltage rating higher than 100V.

M. ZCD AND OVP DETECTOR (R14, R19, C11)

Refer to information starting on page 11 for additional information.

The resistor divider, R14 and R19, sets the OVP threshold:

$$V_{o_ovp} \cdot \frac{N_{aux}}{N_s} \cdot \frac{R_{19}}{R_{14} + R_{19}} = 5.5V \quad (32)$$

Where V_{o_ovp} is the output OVP voltage, N_{aux} is the number of transformer auxiliary winding turns, and N_s is the number of transformer secondary winding turns. Given N_{aux}=19, N_s=16, set V_{o_ovp}=30V for R14/R19=5.4. Consider $V_{in_max} = 132 \cdot \sqrt{2}$ and the ZCD source current limitation, select R14=39kΩ, R19=7.2kΩ. Add a 10pF ceramic bypass capacitor (C11) to the ZCD pin to absorb the high-frequency ring on ZCD due to the MOSFET turning off and can cause the OVP function to mis-trigger. The resistor and capacitor form a delay time for the ZCD turn-on signal detector, and influences the output current-line regulation accuracy, so avoid large RC values.

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N. MULT PIN RESISTOR DIVIDER (R3, R17, C10)

The MULT pin resistor divider needs to be carefully tuned because the MULT voltage determines the COMP voltage level, which directly influences the dimming curve and performance (refer to information on page 10). Test the estimated divider values with different types of TRIAC dimmers to determine accurate resistor values: this example uses R3=1MΩ and R17=11kΩ for a COMP level of 2.3V at 120VAC input. The C10 is absorbs the switching frequency ripple on the ZCD voltage for accurate dimming-phase detection. Increasing the capacitance can further smooth the ZCD voltage, but increase the input-line voltage phase shift and cause diminish the power factor. Here, C10 is tuned to 2.2nF.

O. CURRENT SENSING RESISTOR (R20, R21, R24)

As described on page 14, approximate the current sensing resistor with the following equation:

$$R_s \approx \frac{V_{ref} \cdot N}{2 \cdot I_o} \quad (33)$$

Where N is the turn ratio of primary winding to secondary winding, V_{ref} is the feedback reference voltage (typically 0.4V), and R_s is the sense resistor between the S pin and GND.

Equation (33) describes R_S under BCM, but the device may enter DCM during a line cycle due to the minimum off-time limitation and a missing ZCD turn-on signal. The DCM influences and other factors also influence the output current through primary-side control, such as the IC's internal logic delay, the transformer inductance, and the ZCD detection delay. These factors make estimating the output current difficult, and why designing the current sensing resistor last provides allows for better fine-tuning for the required output current.

In this case, the sensing resistor is tuned to 2.2Ω, using two 1.1 Ω/0.25W resistors in series to distribute the power dissipation.

P. OCP DETECTOR (R18, R22, D9)

Refer to page 11 for detailed design information. Calculate the primary-side OCP set-point as:

$$I_{p_OCP} \cdot R_s \cdot \frac{R22}{R22 + R18} - V_{D9} = 0.9 \quad (34)$$

Where I_{P_OCP} is the primary-side over-current–protection value and V_{D9} is the D9 diode voltage drop. Using the 1N4148 diode, the V_{D9} is approximately 0.4V. Using equation (10), the primary maximum current is 0.398A to set the primary OCP current to about 2x the primary maximum current, I_{P_OCP}=0.8A. Then R18/R22=0.35, where R22=510Ω and R18=180Ω.

Q. LAYOUT GUIDELINE

- Design the main power flow path as short as possible using wide wires. Design the sense resistor GND return to directly connect to the input capacitor, C2. Use the largest-possible cooper pour for the power devices for good thermal performance.
- Separate the power GND and the analog GND, and connect them together only at an IC GND pin.
- Placed the IC pin components as close as possible to the corresponding pins. Provide the ZCD pin bypass capacitor and the COMP pin capacitor layout priority.
- Isolate the primary side and the secondary side by at least 4mm to meet safety requirements and the Hipot test. Tune the transformer installation position to keep the primary side far away from secondary side.

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- In order to pass the surge test, separate the input high voltage wire from other components and GND. Connect R3, R4, and R5 to the rectified input line for the DIP package.
- On the secondary side, place the rectifying diode as close as possible to the output filter capacitor, and use a short trace from the transformer output return pin to the return point of the output filter capacitor.

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R. BOM

Quantity	Designator	Value	Description	Package	Manufacturer	Manufactuer_P/N
1	BD1	MB6S	BRIDGE, 600V, 0.5A	SOIC-4	Taiwan Semiconductor	MB6S
1	C1	22nF/630V	Ceramic Cap, 630V，X7R	1206	TDK	C3216X7R2J223K
1	C2	100nF/400V	104/400v	DIP	Panasonic	CBB 0.1uF/400V
2	C3,C4	470uF/35V	Electrolytic Capacitor, 35V, Electrolytic	DIP	Rubycon	470uF/35V
1	C5	220nF/400V	CBB,400V	DIP	Panasonic	ECQE4224KF
1	C6	68pF/630V	Ceramic Cap,COG,630V	1206	muRata	GRM31A7U2J680JW31D
1	C7	0.1uF/50V	Ceramic Cap,X7R,50V	0603	muRata	GRM188R71H104KA93D
1	C8	33nF	Ceramic Cap,50V,X7R	0603	muRata	GRM188R71H333KA61D
1	C9	10uF/10V	Ceramic Capacitor;16V;X7R;0805	0805	muRata	GRM21BR61C106KE15
1	C10	2.2nF/50V	Ceramic Cap,X7R,50V	0603	muRata	GRM188R71H222KA01
1	C11	10pF	Ceramic Cap,50V,COG	0603	muRata	GRM1885C1H100JA01
1	C12	22uF/50V	Electrolytic Capacitor;50V;Electrolytic	DIP	Jianghai	
1	CX1	10nF	X Capacitor,275V	DIP	Kaili	PX103K3ID49L270D9R
1	CY1	2.2nF	Y Capacitor,250V	DIP	Hongke	JY10F332MY72N
1	D1	MURS320T3	Diodes,200V,3A	SMC	ON Semi	MURS320T3
1	D2	1N4007	Diodes,1000V,1A	DO-41	Diodes	1N4007
3	D3,D7,D9	1N4148W	DIODES/SOD-123	SOD-123	Diodes	1N4148W
2	D4,D5	ES1D	Diode, 1A,200V	SMA	Premier	ES1D
1	D6	BZT52C16	Zener DIODES/16V, 5mA	SOD-123	Diodes	BZT52C16
1	D8	BZT52C15	Zener Diode, 15V, 5mA	SOD-123	Diodes	BZT52C15
1	D10	BZT52C27	Zener Diode, 27V, 2mA	SOD-123	Diodes	BZT52C27
1	F1	250V/2A	SS-5-2A	DIP	any	
1	L1	Inductor,1.8mH	Inductor,1.8mH/0.3A	DIP	Wurth	758772182
2	L2, L3	4.7mH	Inductor, 4.7mH/0.24A	DIP	Wurth	744772472
1	Q1	AP03N70I	600V/3.3A	TO-220	APEC	AP03N70I
1	Q2	MMBT3906LT1	PNP, transistor	SOT-23	ON Semi	MMBT3906LT1
1	Q3	SMK0260D	MOSFET, 600V, 2A	TO-252	AUK	SMK0260D
3	R1,R16,R15	1kΩ	Film RES,1%	1206	Royalohm	1206F1001T5E
1	R2	499kΩ	Film RES, 1%	1206	Panasonic	ERJ8EF4993V
2	R3,R4	1MΩ	DIP,0.25W RESISTOR	DIP		
1	R5	510k	DIP,0.5W RESISTOR	DIP		
2	R6,R9	510Ω	DIP,1W RESISTOR	DIP		
1	R7	30kΩ	Film RES,1%	1206	Royalohm	1206F3002T5E
1	R8	10Ω	Film RES, 1%	0603	Yageo	RC0603FR-0710RL
2	R10,R11	357Ω	Film RES,1%	1206	Yageo	RC1206FR-07357RL
1	R12	130kΩ	Film RES,1%	0603	Yageo	RC1206FR-07130KL
1	R13	510Ω	DIP,2W RESISTOR	DIP		
1	R14	39kΩ	Film RES,1%	0603	Yageo	RC1206FR-0739KL
1	R17	11kΩ	Film RES, 1%	0603	Yageo	RC0603FR-0711KL
1	R18	180Ω	Film RES,1%	0603	Yageo	RC1206FR-07180L
1	R19	7.2kΩ	Film RES,1%	0603	Yageo	RC1206FR-077K2L
1	R20	NC				
1	R21	1.1Ω	Film RES,1%	1206	Yageo	RC1206FR-071R1L
1	R22	510Ω	Film RES,1%	0603	Yageo	RC1206FR-07510L
1	R23	510Ω	DIP,0.25W RESISTOR	DIP		
1	R24	1Ω	Film RES,1%	1206	Yageo	RC1206FR-071RL
1	RV1	TVR10431KSY	430V/2500A	DIP	TKS	TVR10431KSY
1	T1	RM6	RM6, Np:Ns:Naux=80:16:19, Lp=1.9mH	RM6	EMEI	
1	U1	MP4030	MP4030	SOIC8	MPS	MP4030

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5. EXPERIMENTAL RESULT

All measurements performed at room temperature

5.1 PERFORMANCE DATA

Vin (VAC)	Pin (W)	PF	THD	Io (A)	Vo (V)	efficiency
108	9.58	0.993	7.00%	0.36	21.62	81.2%
120	9.54	0.99	9.50%	0.364	21.65	82.6%
132	9.47	0.982	11.60%	0.364	21.64	83.1%

5.2 STEADY STATE

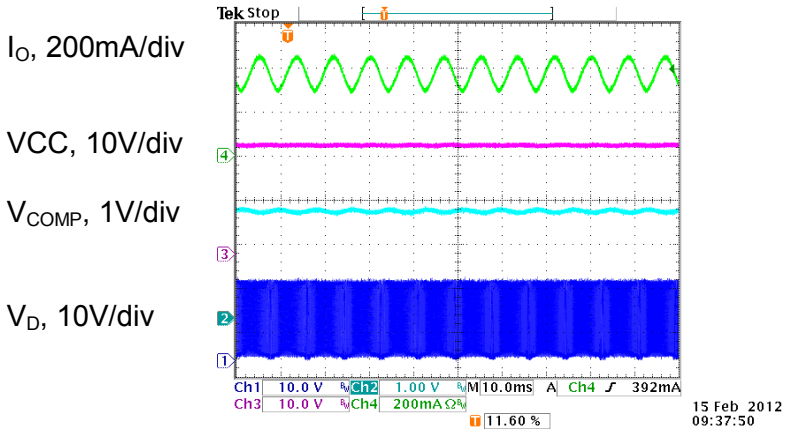

Figure 28: 120VAC, Full Load, 10ms/div

5.3 INPUT VOLTAGE AND CURRENT

Figure 29: 120VAC, Full Load, 10ms/div

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5.4 BOUNDARY CONDUCTION OPERATION

V_S, 1V/div

V_{ZCD}, 2V/div

V_D, 10V/div

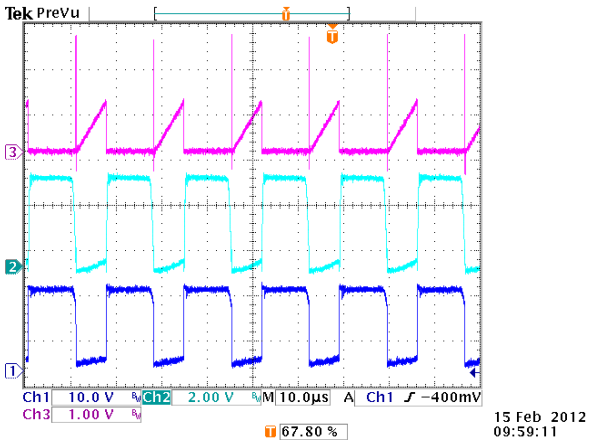

Figure 30: 120VAC, Full Load, 10µs/div

5.5 START UP

I_O, 200mA/div

VCC, 10V/div

V_{COMP}, 1V /div

V_D, 10V/div

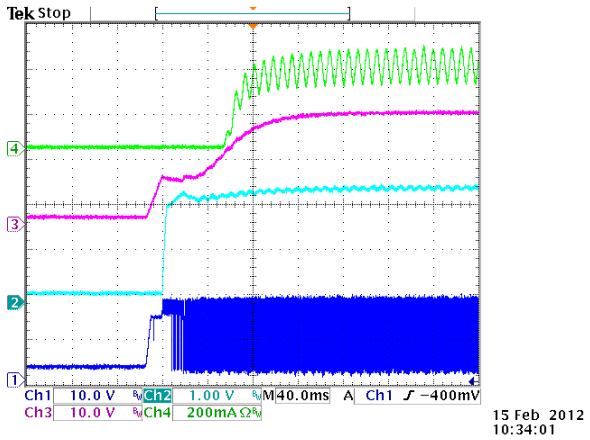

Figure 31: 120VAC, Full Load, 40ms/div

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5.6 OVP (OPEN LOAD AT NORMAL OPERATION)

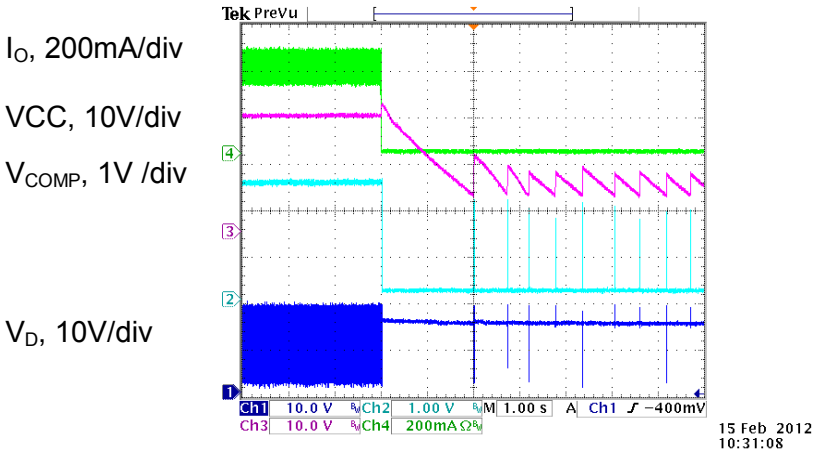

Figure 32: 120VAC, 1s/div

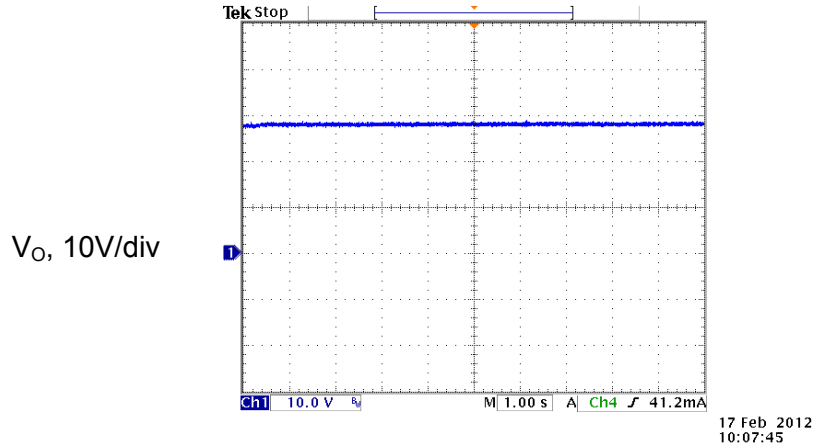

Figure 33: 120VAC, 1s/div

5.7 SCP (SHORT LED+ TO LED– AT NORMAL OPERATION)

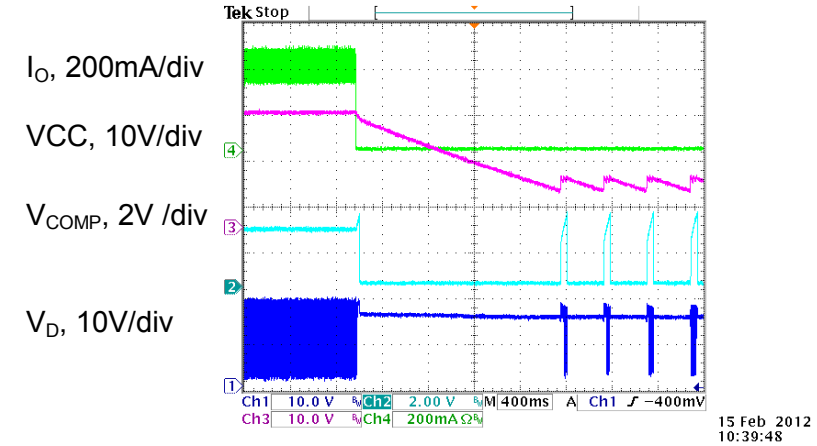

Figure 34: 120V, 400ms/div

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V_D, 10V/div

I_O, 200mA/div

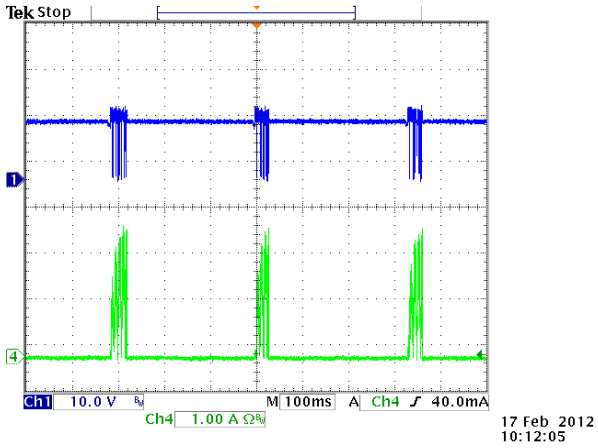

Figure 35: 120VAC, 100ms/div

5.8 TRIAC DIMMING

V_{COMP}, 1V /div

I_O, 100mA/div

V_{MULT}, 1V/div

I_{IN}, 200mA/div

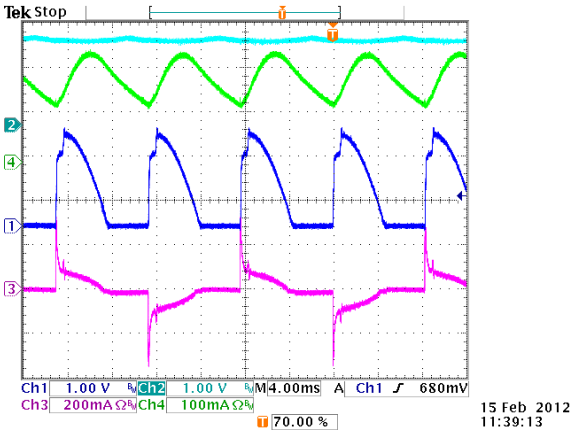

Figure 36: 120VAC, D=60%, 4ms/div

V_{COMP}, 1V /div

I_O, 100mA/div

V_{MULT}, 1V/div

I_{IN}, 200mA/div

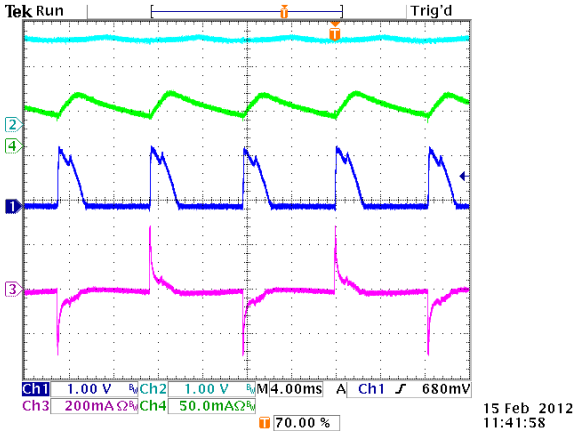

Figure 37: 120VAC, D=40%, 4ms/div

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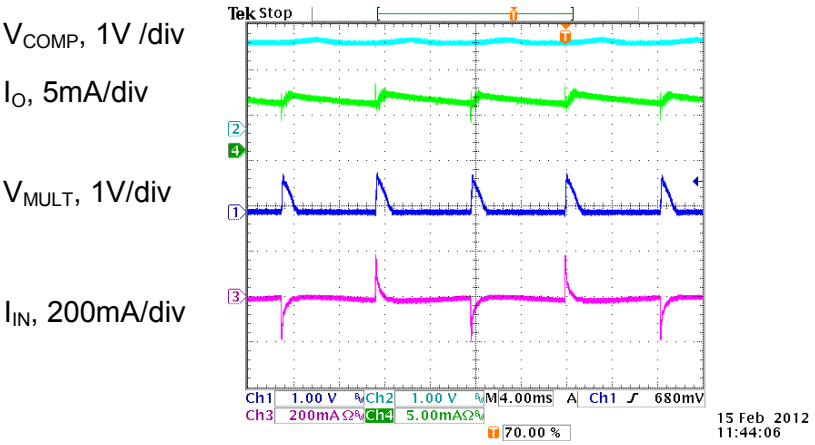

Figure 38: 120VAC, D=20%, 4ms/div

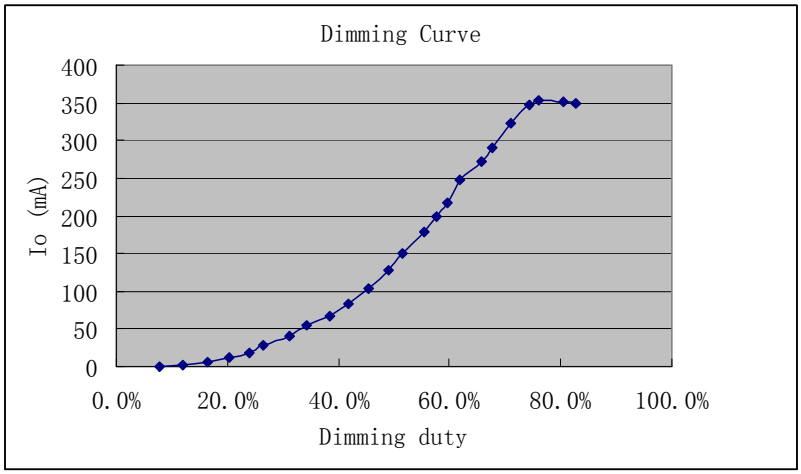

Figure 39: Dimming Curve

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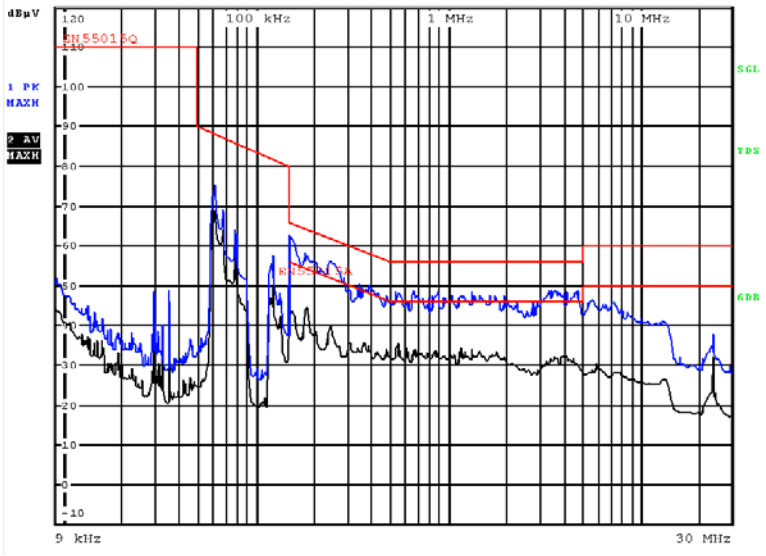
5.9 THERMAL PERFORMANCE

Test Conditions: Full load, Normal operation for 30min, room temp=18°C

RefDes	Description	Temp(℃)@108V	Temp(℃)@132V
L1,L2, L3	Differential inductor	34.5	35.4
BD1 package	Bridge diode	43.2	43.2
BD1 pin	Bridge diode	42.8	38.2
C11, C12	Bulk Cap	28.9	31
T1 windings	Transformer	36.9	40.3
T1 core	Transformer	40.5	41.4
U1 package	MP4030	38.3	38.1
U1 pin	MP4030	35.5	32.8
D1	Output diode	42.3	42
R17	Snubber resistor	41.2	40.7
C9	Snubber cap	41	41.2
D7	Snubber diode	44.4	42
Q1	MOSFET	41.6	42.5
R18, R19, R16	Sense resistor	43.3	38.2
R2, R3	Bleeder resistor	40.5	39.7
R9	damping resistor	59.4	47.8

5.10 CONDUCTED EMI



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