MP4026/4027: Application Note for a High Performance, Offline LED Controller with Primary-Side-Control and Active PFC

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TABLE OF CONTENTS

1. Introduction 4
2. Primary-side control, BOUNDARY-CONDUCTION MODE with ACTIVE pfc 5
A. Primary-Side Control 5
B. Boundary-Conduction Mode 6
C. Active PFC 8
3. Pin Function and Operation Information 10
A. PIN Introduction (here using MP4027 for example, MP4026 can refer to it) 10
Pin1 (VCC) 10
Pin2 (MULT) 11
Pin3 (NTC) 12
Pin4 (COMP) 13
Pin5 (GND) 13
Pin6 (FB) 13
Pin7 (CS/ZCD) 14
Pin8 (GATE) 16
4. Design example: 90-265VAC input, 350ma, 20v output, High-Performance, 7W A19 LED bulb driver with mp4027 17
A. Specifications 17
B. Schematic 17
C. Turn Ratio (N), Primary MOSFET, and Secondary-Rectifier–Diode Voltage Rating Selection 17
D. Transformer Design 19
Primary Inductance, L_P 19
The Primary-Winding RMS Current: 21
The secondary winding RMS current: 21
The Transformer Core Selection 21
Primary and Secondary Winding Turns 22
Wire Size 23
Auxiliary Winding Wire Size 23
Window-Area Fill-Factor Calculation 23
Air Gap 24
Instructions for Transformer Manufacturing 24
E. Input EMI Filter (L1, L2, L3, CX1, CY1, C2) 25
F. Input Bridge (BD1) 25
G. Input Capacitor (C2) 25
H. Output Capacitor (C8, C9) 25

I. RCD Snubber (R14, C6, D3) 26
J. VCC Power Supply (R4, R15, C3, D2,) 27
K. ZCD and OVP Detector (R9, R10, D4) 28
L. Current Sensing (R11, R12, C1) 28
N. Feedforward Resistor (R7) 29
O. gate driver resistor (R8) 29
P. loop compensation capacitor (C5) 29
Q. Ntc thermistor (NTC, C7) 29
R. Layout Guideline 30
S. BOM 31
5. Experimental Result 32
5.1 Performance Data 32
5.2 Line and load regulation 33
5.3 Efficiency 33
5.4 Steady State 33
5.5 Input Voltage and Current 34
5.6 Boundary Conduction Operation 34
5.7 Start Up 34
5.8 OVP (open load at normal opration) 35
5.9 SCP (Short LED+ to LED– at normal operation) 35
5.10 Primary-side OcP (short primary winding at normal opration) 35
5.11 NTC Curve 36
5.12 Emi performance 36
5.13 Surge test 37

1. INTRODUCTION

The MP4026/4027 are high performance primary-side-control offline LED lighting controller with PFC integrated. The primary-side-control can significantly simplify the LED lighting driving system by eliminating the opto-coupler and the secondary feedback components in an isolated single stage converter. Its proprietary real current control method can accurately control the LED current from the primary side information. Internally integrated current accuracy compensations can enhance the LED current accuracy with good line and load regulation.

The MP4026/4027 integrate power factor correction function and works in boundary conduction mode. The power factor correction function can achieve the PF>0.9 in a universal input voltage range. The boundary conduction mode operation can reduce the switching losses and improve the EMI performance.

The MP4026/4027 provide multiple advanced protections to enhance the system safety and reliability, including over-voltage protection, short–circuit protection, primary-side over-current protection, brown out protection, VCC under-voltage lockout, and thermal shutdown: all protections features auto-restart.

The MP4026/4027 have tow small packages, SOT23-6 for MP4026, SOT23-8 for MP4027. The MP4027 has two more pins with NTC and FB. The NTC pin provides LED thermal protection, support PWM dimming. The FB pin can make MP4027 suit for non-isolated buck applications, the feedback signal can be directly applied on FB pin. (Except these, all other features are same for MP4026 and MP4027).

Figure 1 shows a typical application.

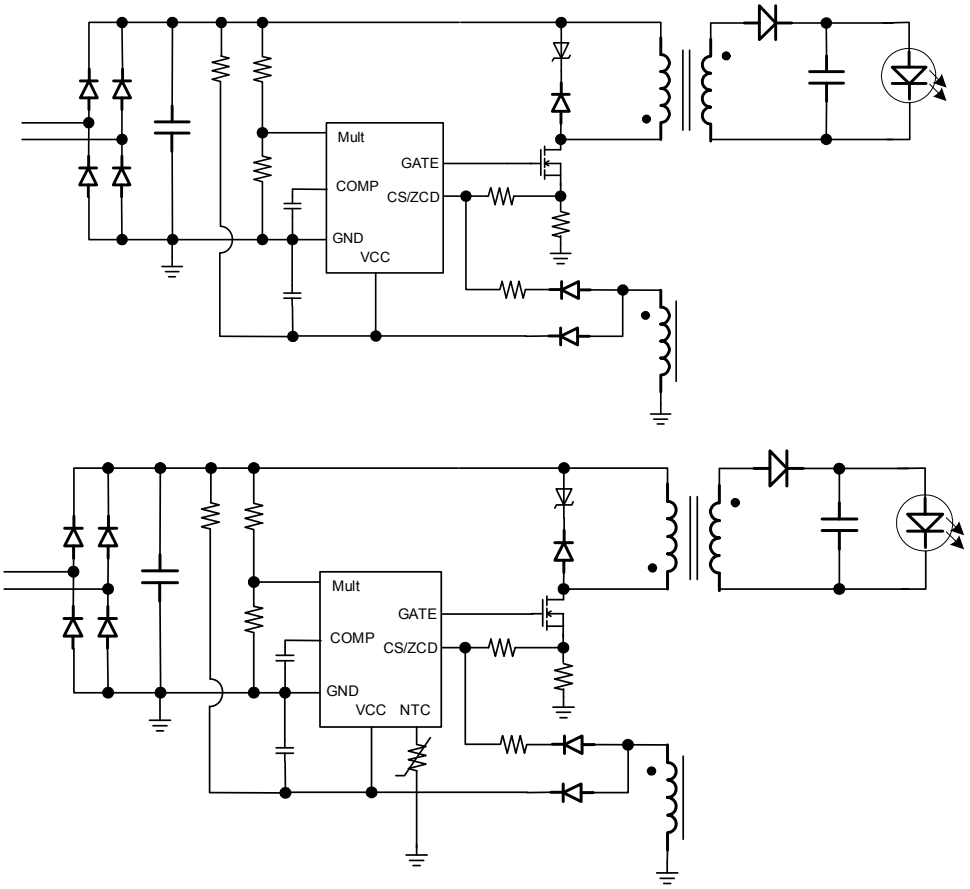


Figure 1: Typical Application

2. PRIMARY-SIDE CONTROL, BOUNDARY-CONDUCTION MODE WITH ACTIVE PFC

Conventional off-line LED drivers use secondary-side control that senses the LED current directly. An error amplifier compares this current level against a reference produced by a device such as a TL431, and the compensated output determines the primary-side duty cycle to regulate the LED current. Although this control method can directly control the LED current with high accuracy under any condition, it requires additional secondary-side components—including a sensing circuit, comparison and compensation circuits, an opto-coupler, and bias power supplies—that significantly increase system complexity and cost.

In addition, the primary-side input stage typically uses a full-wave rectifier bridge with an E-cap filter to generate a DC voltage. The E-cap must be large enough to limit the DC voltage ripple. This means the instantaneous input line voltage is lower than the DC voltage on the E-cap for most of a line half-cycle, and that the rectifier diodes only conduct a small portion of the voltage. This voltage limitation causes the input line current to act like a series of narrow pulses whose amplitudes are about 10x higher than the average DC level. The drawbacks include: a high current peak and RMS current drawn from the line, line-input–current distortion limiting the power factor to about 0.5 to 0.6, and large induced harmonics.

Figure 1 shows that the MP4026/4027 use primary-side control, which eliminates secondary feedback components to significantly reduce the component count and cost. The MP4026/4027 work in boundary-conduction mode with active PFC, achieve a power factor >0.9 for the input, and reduce THD to meet IEC61000-3-2 requirements.

A. PRIMARY-SIDE CONTROL

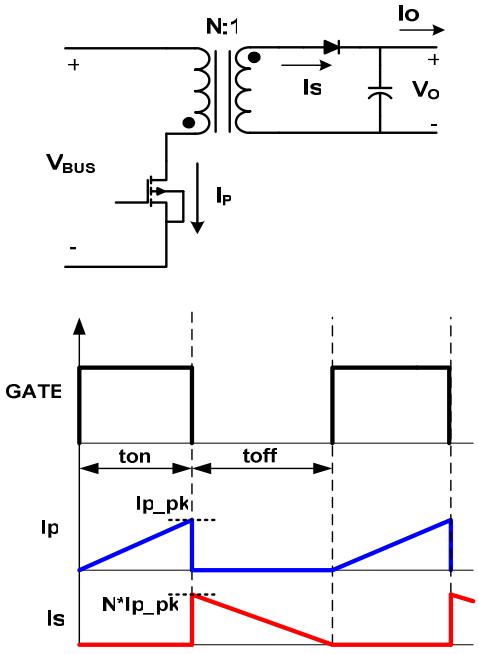


Figure 2: Transformer Currents Relative to the BCM Flyback Converter

Given that the LED current is the average current of the transformer's secondary side, $I_o = I_{s\_avg}$, as shown in Figure 2, the average secondary-side current in boundary-conduction mode can be calculated as:

$$I_{s\_avg} = \frac{\frac{1}{2} \cdot N \cdot I_{p\_pk} \cdot t_{off}}{t_{on} + t_{off}}$$

Where I_{s_avg} is the average secondary-side current, and I_{p_pk} is the peak primary-side current, N is the turn ratio of primary winding to secondary winding. The MP4026 samples the primary-side peak current to calculate the average current. Since the average current is proportional to the output current, if the average current is controlled as a constant value V_{FB}, the output current is also constant, allowing for primary-side control. So, the output LED mean current can be calculated approximately as:

$$I_0 \approx \frac{N \cdot V_{FB}}{2 \cdot R_S}$$

Where V_{FB} is IC feedback reference voltage, R_s is the sensing resistor.

B. BOUNDARY-CONDUCTION MODE

The MP4026/4027 work in boundary conduction mode where the transformer functions at the boundary between the continuous and discontinuous mode.

In a conventional fixed-frequency flyback converter working in discontinuous conduction mode (DCM), the primary switch (MOSFET) turns on at a fixed frequency and turns off when the current reaches the desired level. When the MOSFET turns off, the energy stored in the inductor forces the secondary side diode to turn on, and the inductor current decreases linearly from the peak value to zero. When the current drops to zero, the parasitic resonance of the magnetizing inductor and the sum of the parasitic capacitance causes the MOSFET drain-source voltage to oscillate. The MOSFET can turn on at any point during the parasitic resonance, including when the drain voltage is lower than the bus voltage (meaning low switching losses and high efficiency), and when the drain voltage is much higher than the bus voltage (meaning high switching loss). This feature is observable in the efficiency curves of a discontinuous flyback converter with a constant load as input-voltage efficiency fluctuations as the turn-on switching loss changes with the turn-on drain voltage.

In boundary conduction mode, the switch does not have a fixed switching frequency. Instead, the controller always turns on the switch when the drain voltage goes low by detecting the auxiliary winding voltage, V_{ZCD}, the ZCD voltage is a ratio of primary winding and auxiliary winding. Figure 3 shows that by setting the falling-edge detection near zero, the parasitic resonance causes the ZCD voltage to decrease when the secondary side current deceases to zero: Conversely, when V_{ZCD} reaches the detection threshold, the MOSFET turn-on signal triggers. The transformer magnetizing inductance, parasitic capacitance, and ZCD filtering capacitor determine the detection time delay. The feedback loop determines the switch-on time, similar to conventional peak-current–mode control. The energy stored in the magnetizing inductor then transfers to the output.

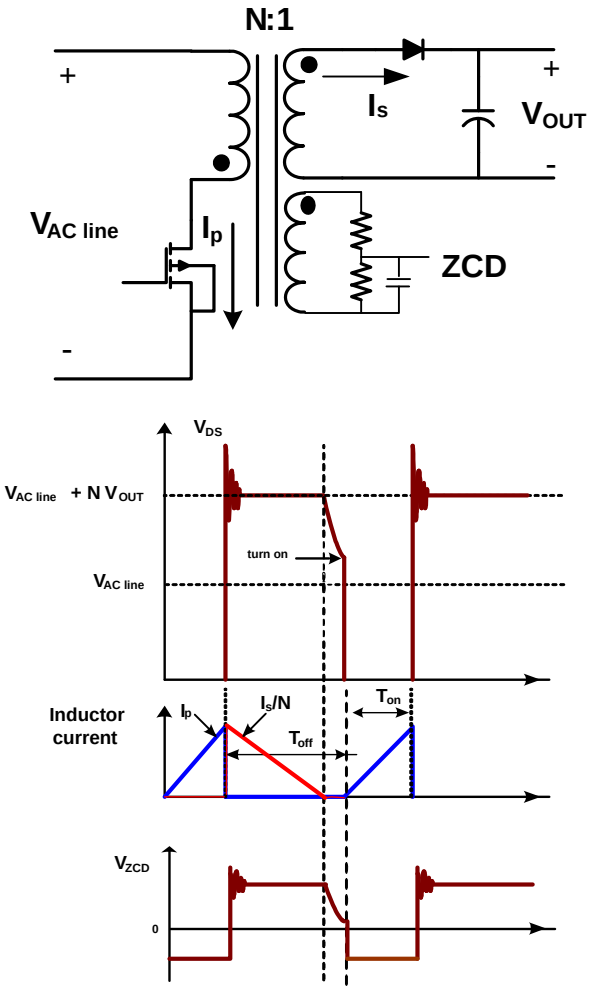


Figure 3: Boundary Conduction Mode

Compared to conventional flyback under continuous conduction mode (CCM) and DCM operation, boundary-conduction mode operation minimizes the turn-on switching loss, thus increasing efficiency and suppressing the MOSFET temperature rise.

C. ACTIVE PFC

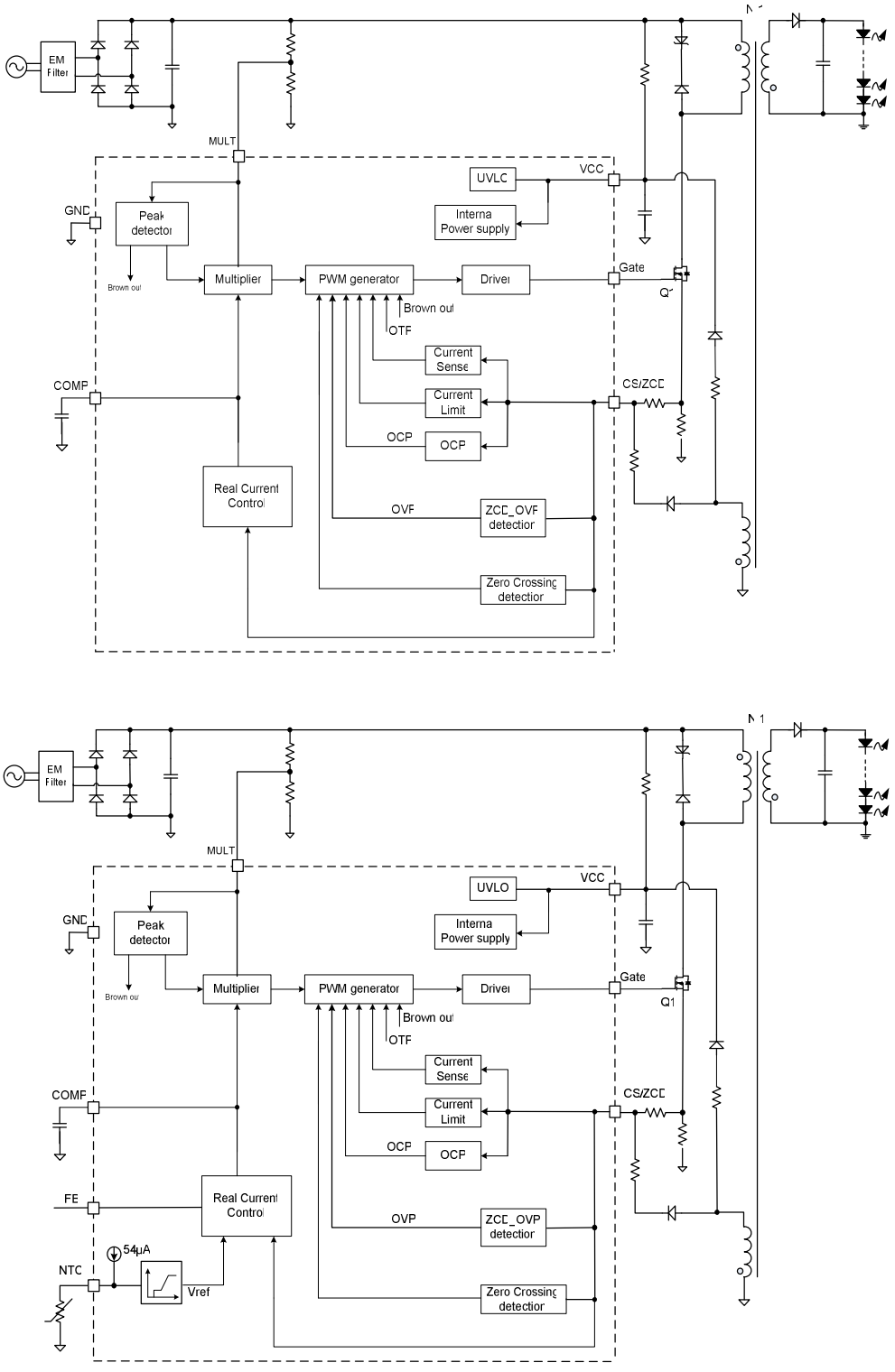


Figure 4: MP4026/4027 Functional Block Diagram and LED Driver

The MP4026/4027 integrate an active PFC function. Figure 4 shows the functional block diagram and the LED converter driver. The converter consists of an EMI filter, a diode bridge rectifier, a flyback circuit using the MP4026/4027. The following description summarizes converter operation with active PFC:

The diode bridge rectifies the AC line voltage, which then goes to the flyback circuit. When the MOSFET turns on, the transformer's primary-side current ramps up from zero. The CS/ZCD pin senses this primary-side current through a sensing resistor, and this signal goes to the real-current calculation block to calculate its average value. The internal error amplifier compares the average value against an internal reference to generate an error signal that is proportional to the difference between them. If the bandwidth of the error amplifier is narrow enough (below 20Hz), then the error signal is a DC value for over a line half-cycle and kept constant until the average value equals the reference: This regulates the output LED current to a required constant value.

The error signal goes to the multiplier block with a portion of the rectified mains voltage. The resulting signal is a rectified sinusoid with a peak amplitude that depends on the peak line voltage and the value of the error signal. The output of the multiplier goes to the negative input of the current comparator in PWM generator block to act as a sinusoidal reference for the PWM. When the CS /ZCD pin voltage equals the value on the negative input of the current comparator, the external MOSFET turns off. The sinusoidal reference signal envelops the peak primary current. and has the same phase as the main input voltage to implement a good power factor.

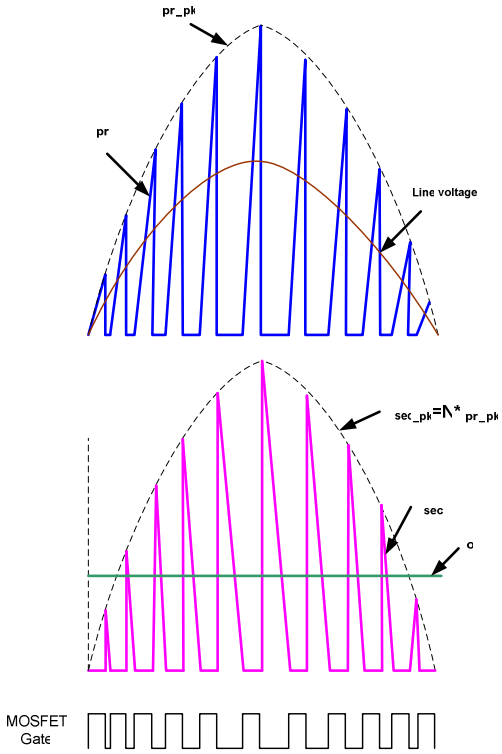


Figure 5: Primary and Secondary Transformer Currents and MOSFET Gate Timing

Figure 5 shows both transformer currents and the gate timing. The operating frequency increases as the instantaneous line voltage decreases; when the line voltage approaches the zero-crossing point, the frequency increases dramatically. The MP4026 has an internally-set 5μs minimum off-time to limit the maximum switching frequency and to improve efficiency and reduce EMI.

3. PIN FUNCTION AND OPERATION INFORMATION

A. PIN INTRODUCTION (HERE USING MP4027 FOR EXAMPLE, MP4026 CAN REFER TO IT)

Pin1 (VCC)

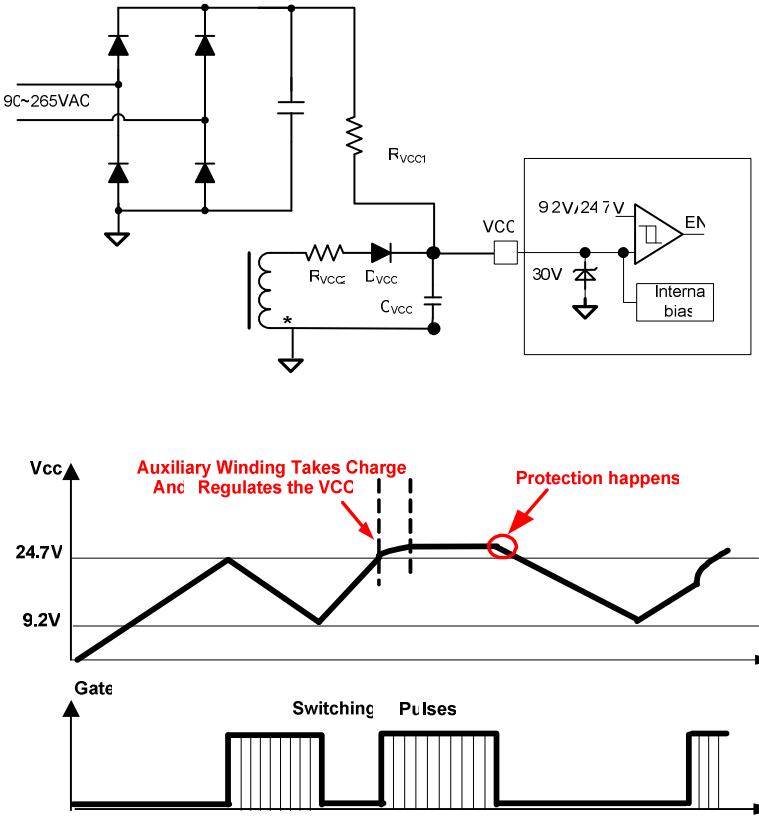


Figure 6: VCC Circuit and Power Supply Flow-Chart

VCC powers both the internal logic circuit and the gate driver signal. Figure 6 shows the VCC circuit and the power supply flow-chart. When AC power supply is on, the bulk capacitor C_{VCC} (typically 4.7μF) is first charged by the start up resistor R_{VCC1} from the AC line, once the VCC voltage reaches 24.7V, the IC will be enabled and begin to switch, the power consumption of the IC increases, then the auxiliary winding starts working and mainly takes the charge of the power supply for VCC. Since the voltage of auxiliary winding is proportion to that of the secondary winding, the VCC voltage will be finally regulated to a constant value. If VCC drops below the UVLO threshold 9.2V before the auxiliary winding can provide the power supply, the IC will be shut down and the VCC will restart charging from AC line again. If fault condition happens at normal operation, the switching signal will be stopped and latched, the IC works at fault mode, the IC quiescent current is about 2mA, when the VCC voltage drops below 9.2V, the system restarts again. So, the R_{VCC1} should be large enough to limit the charging current which ensures the VCC voltage can drop below 9.2V UVLO threshold at fault mode. But, a too large R_{VCC1} will make the start up time too long. Usually, the value need be trade off, for a universal input (90-265VAC) application, the recommended value is 470k Ohm.

The auxiliary-winding positive voltage will also influence the start up time. At start up, the initial auxiliary-winding positive voltage is low and so the VCC level drops. Once VCC drops below 9V threshold, the IC will be shut down until it is recharged to 24.7V, this consumes lots of time. To avoid this, the auxiliary-winding turns need increase, typically, the auxiliary winding positive voltage is set as

23-25V, if need higher voltage in some extreme case, make sure the VCC do not exceed 27V, or a Zener diode is needed from VCC to GND to protect the VCC pin from excessive voltage damage.

Pin2 (MULT)

The MULT pin provides one of the inputs to the internal multiplier. Connect this pin to the tap of the resistor divider from the rectified instantaneous line voltage, which will produce a sinusoidal multiplier output. This output signal provides the reference for the current comparator, which shapes the primary peak current into a sinusoid that is in-phase, with the input line voltage.

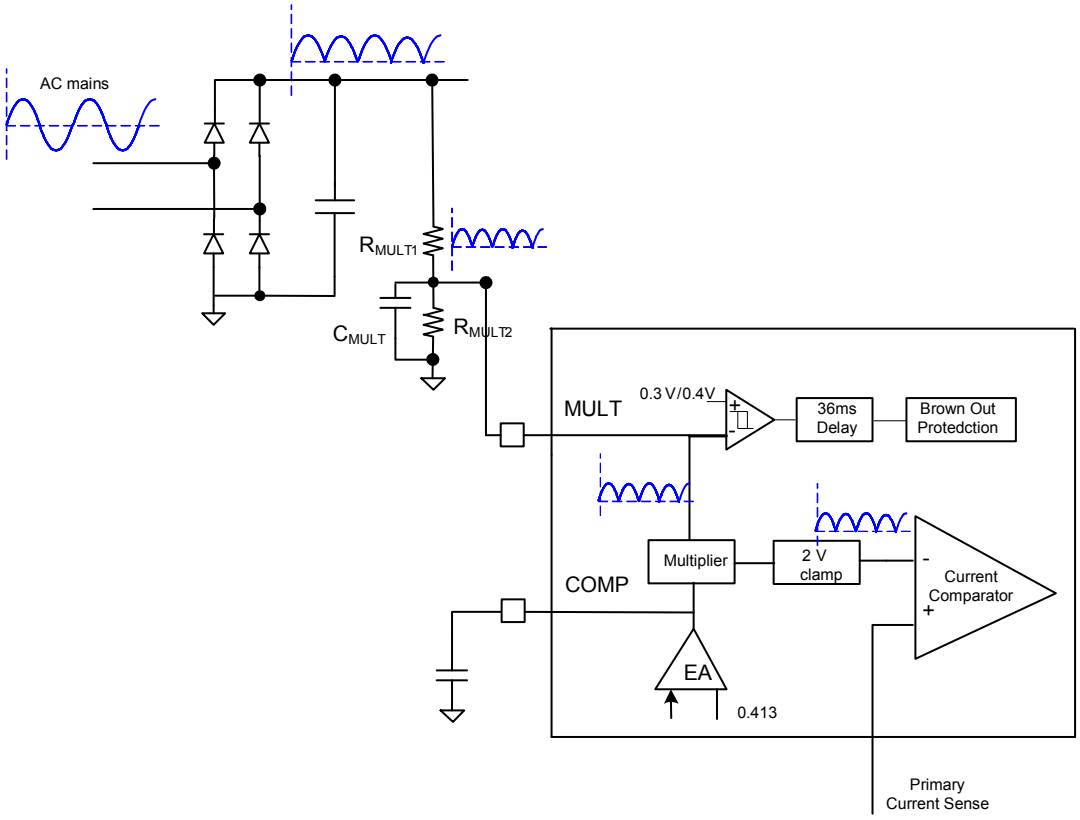


Figure 7: MULT Circuit

The multiplier output is then given by:

$$V_{multiplier\_out} = k \cdot V_{MULT} \cdot (V_{COMP} - 1.5)$$

Where k is the gain of the multiplier.

For the multiplier to operate at linear zone, select a MULT voltage range smaller than 3V. The MULT voltage also determines the COMP voltage level for the system control loop. In real applications, setting the MULT pin too low cause the COMP voltage to saturate the 4.75V high clamp point. So, tow conditions are recommended to set MULT voltage.

$$\sqrt{2} \cdot V_{in\_max(rms)} \cdot \frac{R_{MULT2}}{R_{MULT1} + R_{MULT2}} < 3, \qquad V_{COMP@in\_min} < 3.5$$

Considering the losses, the R_{MULT1} should be large enough, for example, 90V~265VAC input, the R_{MULT1}, R_{MULT2} can be first chosen as 1M, 6.2kΩ with a 2.2nF bypass capacitor. The cap is used to filter the switching frequency ripple on MULT voltage.

The multiplier has a 2V output clamp which is used as cycle-by-cycle current limit for primary current sense signal.

The MULT pin is also used for brown out protection detection. If the peak value of MULT is less than the brown out detection threshold 0.3V for 42ms, the IC recognizes this condition as a brown-out, quickly drops the COMP voltage to zero, and disables the power circuit. If the peak value exceeds 0.4V, the IC restarts and the COMP voltage rises softly again. This feature prevents both the transformer and LED currents from saturating during fast ON/OFF switching. Figure 8 shows the brown-out waveforms.

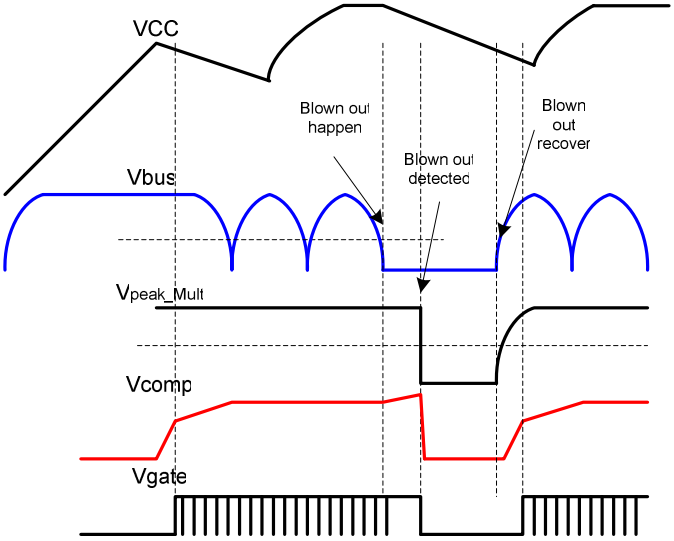


Figure 8: Brown Out Protection Waveforms

Pin3 (NTC)

The NTC pin provides tow functions. One is LED thermal protection; the other is PWM dimming. The NTC pin block is shown as Figure 9.

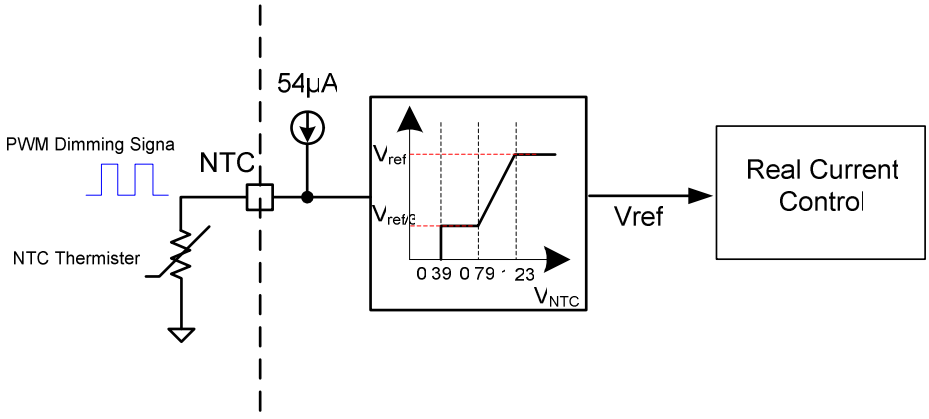


Figure 9: NTC Block

For the LED thermal protection, a NTC thermistor for monitoring the ambient temperature can be directly connected from NTC pin to GND. The internal pull up current flows through the thermistor and generates a corresponding voltage on NTC pin. The NTC voltage controls the output LED reference. The relation is the curve shown in figure 9. When the NTC voltage is higher than 1.23V, the reference is maximum, when the NTC voltage drops from 1.23V to 0.79V, the reference changes from maximum to

1/3, when the NTC voltage changes from 0.879 to 0.39V, the reference is kept same, when the NTC drops below 0.39V, the reference will set to zero, the LED current outputs minimum.

For PWM dimming, applying the PWM dimming signal on NTC pin. The PWM signal high level need be higher than 1.23V, the low level should be lower than 0.39V, the frequency is recommended to be 10 times higher than the system loop bandwidth for a steady output. Normally, the frequency should be >200Hz. The output current will linearly change with the dimming duty from maximum to minimum. The minimum output current is caused by the IC minimum on time (equals LEB time), influenced by the input voltage, MOSFET turn off delay and the transformer inductance. etc. The higher input voltage, the bigger minimum current; the longer MOS turn off delay the bigger minimum current, so a small Q_G and small C_{OSS} MOSFET is better for deep dimming.

Pin4 (COMP)

Loop compensation pin. Connect a compensation capacitor from this pin to AGND. Use a low-ESR ceramic capacitor, such as X7R. The COMP pin is the output of the internal error amplifier. To limit the loop bandwidth <20Hz for good PFC performance, select a capacitor value between 1μF and 4.7μF. A larger capacitor results in a smaller COMP voltage ripple for better PF, THD, EMI, but also means a longer soft-start time.

Pin5 (GND)

The Ground (GND) pin provides the current return for both the control and the gate-drive signals. Connect the power and analog GNDs at this pin only for PCB layout. The power GND (PGND) provides the reference for the power switches, and the analog GND (AGND) for the control signals.

Pin6 (FB)

The FB pin is internally connected to the reference comparator. Sense the output current and apply on FB pin can get accurate control. If using primary-side-control, leave this pin alone.

Pin7 (CS/ZCD)

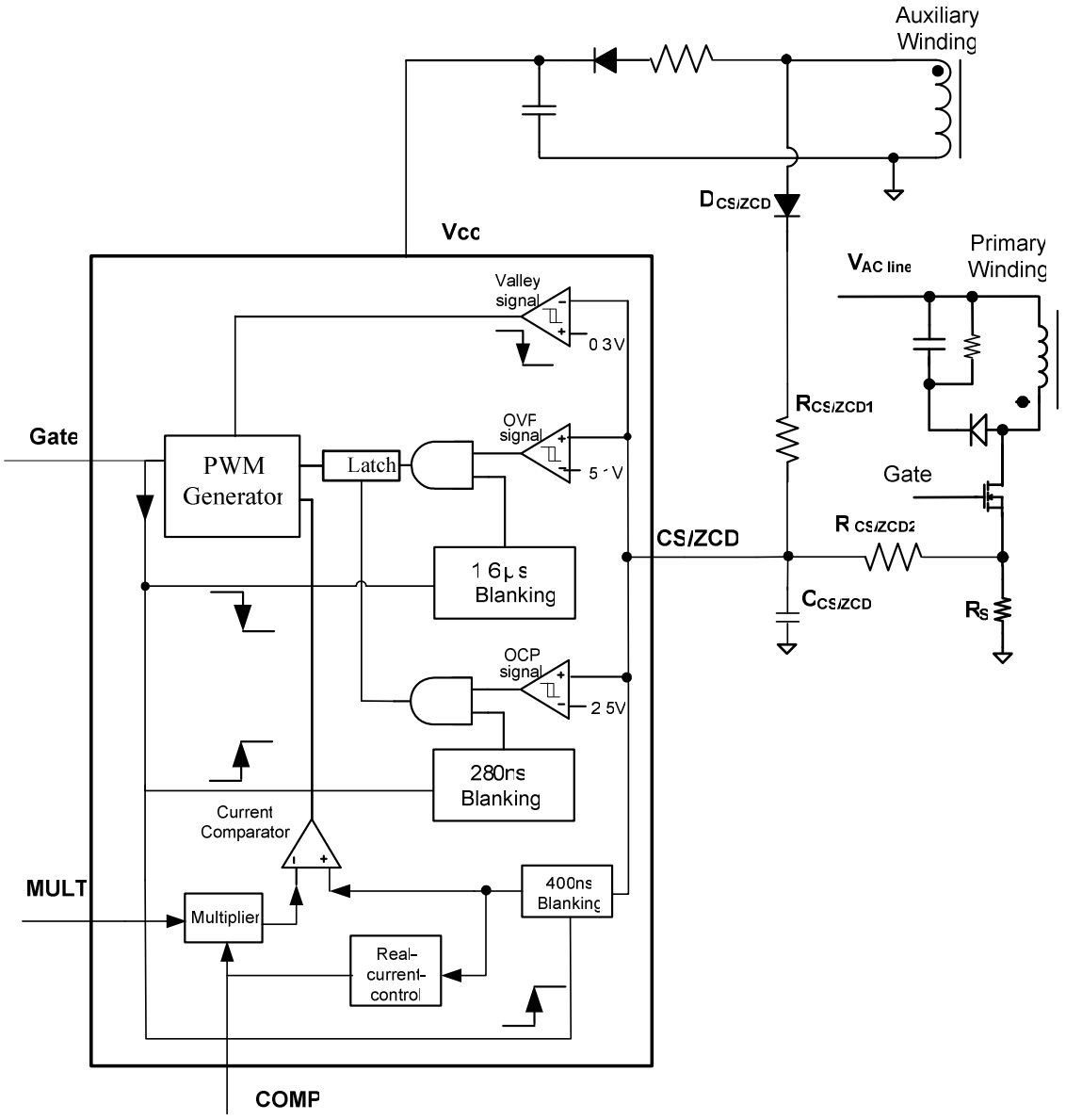


Figure 10: CS/ZCD Circuit

Figure 10 shows the CS/ZCD pin circuitry. The CS/ZCD pin integrates current sensing for real-current-control and current zero-crossing detection for BCM operation. When the MOSFET is turn on, the CS/ZCD senses the primary current signal by the sensing resistor and fed both to the current comparator to determine the MOSFET turn off time and the real-current-control block to do the current regulation. As described on page 6, the output LED mean current calculated approximately as:

$$I_0 \approx \frac{N \cdot V_{FB}}{2 \cdot R_S}$$

Where N is the turn ratio of primary winding to secondary winding, VFB is the feedback reference voltage (typically 0.413V), Rs is the sensing resistor connected between the MOSFET source and GND. To avoid premature switching-pulse termination due to the parasitic capacitances discharging when the MOSFET turns on, the MP4027 uses an internal-leading edge blanking (LEB) unit between the

CS/ZCD pin and the current comparator. When the gate is turn off, the auxiliary winding gets positive plateau voltage and reflected in CS/ZCD pin through the resistor divider (Rzcd1, Rzcd2). When the transformer current decreases to zero, the primary-side-leakage inductance, magnetizing inductance, and the parasitic capacitances make the MOSFET drain-source voltage oscillation—this oscillation is also reflected on the auxiliary winding. The internal gate turn-on signal triggers at the secondary time when the CS/ZCD pin voltage falling-edge goes below 0.3V, with a 0.65V hysteresis, see figure 11.

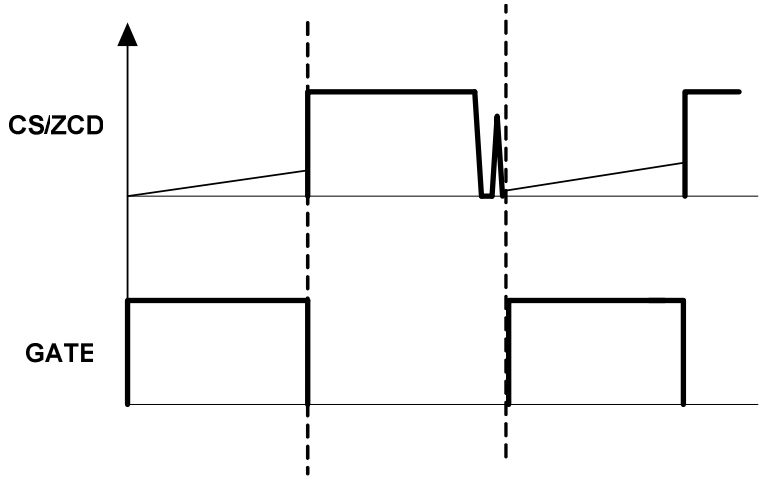


Figure 11: Gate Turn-on Logic

The MP4026 switching frequency varies instantaneously with the input line voltage. To limit the maximum frequency to improve EMI and efficiency performance, the MP4026 employs an internal minimum OFF-time limiter of 5μs.. When the input line voltage crosses the zero point, the primary current is very small and may not turn the secondary diode on, so the CS/ZCD can not generate the turn-on signal for the next duty cycle. To avoid unnecessary IC shutdown, the MP4026 integrates an auto starter that starts timing when the MOSFET turns off. If the ZCD fails to send out another turn-on signal after 190μs, the starter will automatically send out a turn-on signal.

The CS/ZCD pin is also used for output over-voltage protection and primary-side over-current protection.

Output over-voltage protection (OVP) works by detecting the auxiliary-winding voltage's positive plateau, which is proportional to the output voltage. Once the ZCD pin voltage exceeds 5.1V, the OVP signal triggers and latches, the gate driver turns off, and the VCC voltage decreases. When the VCC drops below 9V UVLO, the IC resets and restarts. The following equation estimates the output OVP set point:

$$V_{OUT\_OVP} \cdot \frac{N_{AUX}}{N_{SEC}} \cdot \frac{R_{CS/ZCD2}}{R_{CSZCD1} + R_{CS/ZCD2}} = 5.1V$$

Where V_{OUT_OVP} is the output OVP setting voltage, N_{AUX} is the number of transformer auxiliary winding turns, and N_{SEC} is number of secondary winding turns. To avoid OVP mis-triggers caused by switch-off oscillation spikes, the MP4026 integrates an internal T_{LEB_OVP} blanking time for the OVP detection (see Figure 12).

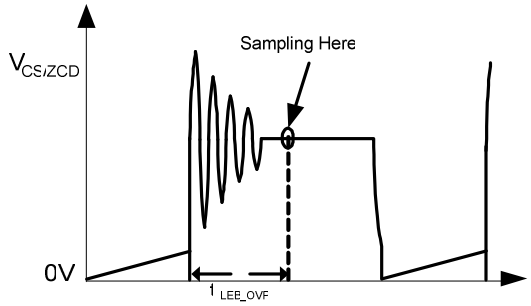


Figure 12: ZCD Voltage with Blanking Time

Selecting for $R_{CS/ZCD1}$ and R_{CSZCD2} requires taking the RC delay into consideration. In real application, a 10-22pF bypass capacitor $C_{CS/ZCD}$ is needed from CS/ZCD pin to GND to absorb the high frequency noise to make the current sensing signal more precise. But the $R_{CS/ZCD2}$ and $C_{CS/ZCD}$ forms a RC delay for the current sensing signal. Too long delay will also make the current sample signal on CS/ZCD distortion with the real signal and lead un-accurate output current. So the RC delay time need be short enough. Usually, the $R_{CS/ZCD2}$ should be chosen <3k Ohm.

The primary-side over-current protection is achieved by detecting the CS/ZCD peak voltage at gate turn on. If the CS/ZCD pin voltage rising to 2.5V at gate turn on interval, the primary-side over-current protection signal will be triggered and latched, the gate driver will be turned off and the V_{CC} voltage dropped below the UVLO which will make the IC shut down, and the system restarts again. The primary-side over-current protection prevents device damage caused by extremely excessive current, like primary winding short. To avoid mis-trigger by the parasitic capacitances discharging when the MOSFET turns on, a LEB time is needed, this LEB time is relatively smaller than current regulation sensing LEB time, typical 280ns.

Pin8 (GATE)

Gate drive output for driving external MOSFET. The internal totem pole output stage is able to drive external high power MOSFET with 0.8A source capability and 1A sink capability. The high level voltage of this pin is clamped to 14.5V to avoid excessive gate drive voltage, and the low level voltage is higher than 7V to guarantee enough drive capacity. Connect this pin to the MOSFET gate in series with a driving resistor. A smaller driving resistor provides faster MOSFET switching, reduces switching loss and improve MOSFET thermal performance. However larger driving resistors usually provide better EMI performance. It is a tradeoff. For different applications, the driving resistors should be fine tuned. Typically, the value can be 10Ω~50Ω.

4. DESIGN EXAMPLE: 90-265VAC INPUT, 350MA, 20V OUTPUT, HIGH-PERFORMANCE, 7W A19 LED BULB DRIVER WITH MP4027

A. SPECIFICATIONS

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Supply Voltage	V_{IN}	2 Wire	90		265	VAC
AC Line Frequency	f_{LINE}			50		Hz
Output Voltage	V_{OUT}	6 LEDs in series		20		V
LED Current	$I_{LED(MAX)}$	Without connecting dimmer		350		mA
Continuous Output Power	P_{OUT}			7		W
Efficiency	η	Full load, with out connecting dimmer			86%	
Power Factor			0.9			
Conducted EMI			Meets EN55015			
Harmonics			Meets IEC61000-3-2 Class C Limitation			
Surge			Meets IEC61547 surge requirement			

B. Schematic

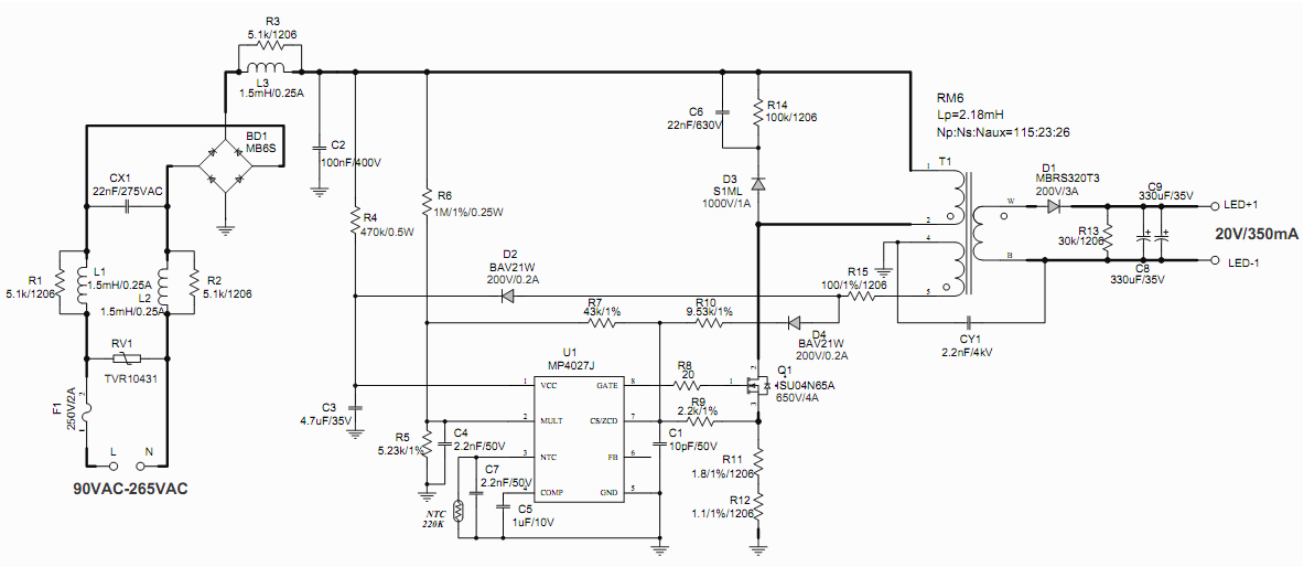


Figure 13: Example Application Schematic—7W A19 Driver

C. TURN RATIO (N), PRIMARY MOSFET, AND SECONDARY-RECTIFIER–DIODE VOLTAGE RATING SELECTION

The following provides a design example given the following conditions:

- V_{ac_min}=90V
- V_{ac_max}=265V
- $V_{in\_max}=\sqrt{2}\cdot V_{ac\_max}$
- $V_{in\_min}=\sqrt{2}\cdot V_{ac\_min}$
- $V_{in}(V_{ac},t)=\left|\sqrt{2}\cdot V_{ac}\cdot\sin(2\cdot\pi\cdot f_{line}\cdot t)\right|$

Figrure 14 shows a typical drain-source voltage waveform for the primary MOSFET and the secondary rectifier diode. From the waveform, the maximum primary high side MOSFET Drain-Source voltage rating $V_{P\text{-}MOS\_max}$ is

$$V_{P-MOS\_max} = V_{in\_max} + N \cdot V_o + 150 \quad (1)$$

Where 150V is the assumed maximum spike voltage, and is related to the RCD snubber.

The maximum secondary rectifier diode voltage rating, V_{DIODE_max}, is

$$V_{DIODE\_max} = \frac{V_{in\_max}}{N} + V_o + 40 \quad (2)$$

Assuming the maximum voltage spike is 40V.

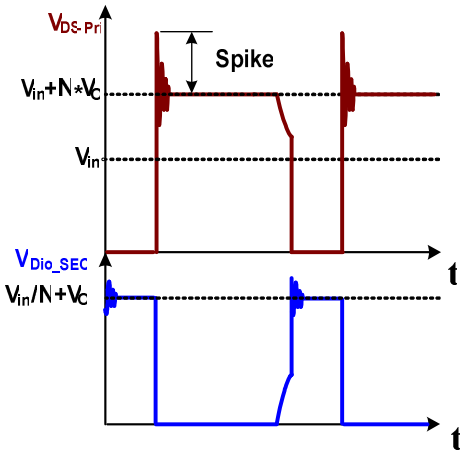


Figure 14: Drain-Source Voltage of the Primary MOSFET and the Secondary Rectifier Diode

Figure 15 shows the voltage rating curves of the primary MOSFET and secondary rectifier diode versus the turn ratio, N, based on equations (1) and (2). N can be determined by the required MOSFET and rectifier diode voltage ratings.

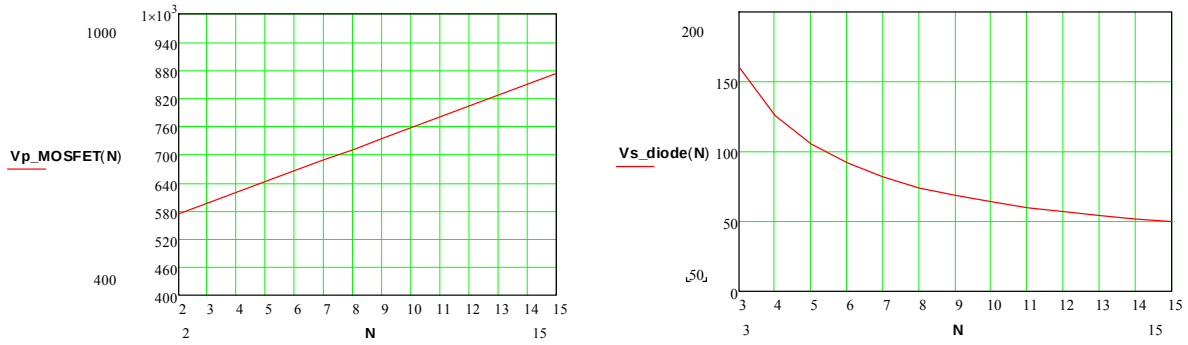


Figure 15: Votage Ratings for the Primary MOSFET and the Secondary Rectifier Diode as a function of Turn Ration, N

Some applications allow for N to be selected from within a range, which then requires the following considerations:

- A small N means a smaller τ_{on}/τ_{off} ratio, as per equation (5), which leads to a poor THD
- A large N leads to a large primary inductance and a physically larger transformer.

Based on the stated conditions, N=5, so 650V or 700V MOSFET and a 150V or 200V Schottky or fast-recovery diode suffices for this particular design example.

D. TRANSFORMER DESIGN

Primary Inductance, L_P

It is possible to demonstrate that the MP4027 produces a constant ON-time over each line half-cycle, given:

- $V_S = R_s \cdot V_{in} \cdot \frac{t_{on}}{L_m}$, and
- $V_{Multipier} = K_1 \cdot K_2 \cdot V_{in} \cdot (V_{COMP} - 1)$, since
- $V_{CS} = V_{Multiplier}$,
- then $t_{on} = \frac{L_m \cdot K_1 \cdot K_2 \cdot (V_{COMP} - 1)}{R_s}$

Where L_m is the primary inductance, R_s is the current sensing resistor, K_1 is the multiplier gain, K_2 is the ratio of the MULT pin voltage vs. the line voltage, and V_{COMP} can a constant DC value when connected with a large COMP capacitor. The turn-off time varies with the instantaneous line voltage.

$$t_{on} = \frac{L_p \cdot I_p}{V_{in}(V_{ac}, t)} \tag{3}$$

$$t_{off} = \frac{L_p \cdot I_p}{N \cdot V_o} + 1.5 \cdot 10^{-6} \tag{4}$$

for

$$t_{off}(t_{on}, V_{ac}, t) = \frac{V_{in}(V_{ac}, t) \cdot t_{on}}{N \cdot V_o} + 1.5 \cdot 10^{-6} \tag{5}$$

Considering the τ_{off} limit within MP4027, the τ_{off} equation should be modified as:

$$t_{off}(t_{on}, V_{ac}, t) = \begin{cases} \frac{V_{in}(V_{ac}, t) \cdot t_{on}}{N \cdot V_o} + 1.5 \cdot 10^{-6} \, if \, \frac{V_{in}(V_{ac}, t) \cdot t_{on}}{N \cdot V_o} + 1.5 \cdot 10^{-6} > 5\mu s \\ 5\mu s, otherwise \end{cases} \tag{6}$$

Figure 16 shows that the output LED current equals the average value of the secondary winding current during a half-line cycle. Equation (7) shows that the output current is the sum of the secondary current in each cycle to produce an average value.

$$I_o(a,b,t_{on},V_{ac},L_p) = \left| \begin{array}{l} t1 \leftarrow a \\ sum \leftarrow 0 \\ \text{while}(t1 < b) \\ \left| sum \leftarrow sum + \frac{1}{2} \cdot \left\{ \left[\frac{V_{in}(V_{ac}, t1 + t_{on}) \cdot t_{on}}{L_p} \right] \cdot N \right\} \cdot t_{off}(t_{on}, V_{ac}, t1 + t_{on}) \right. \\ \left| t1 \leftarrow t1 + t_{on} + t_{off}(t_{on}, V_{ac}, t1 + t_{on}) \right. \\ \frac{sum}{b - a} \end{array} \right. \quad (7)$$

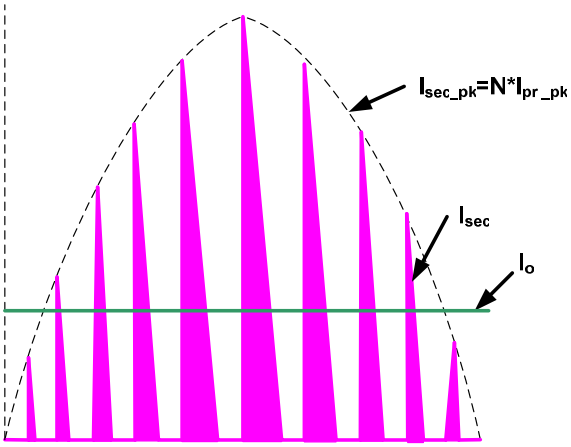


Figure 16: Secondary-Side Current

Usually, the system will define a minimum frequency f_{s_min}, the minimum frequency will occur at $V_{in} = \sqrt{2} \cdot V_{ac\_min} \cdot \sin(\frac{\pi}{2})$. The selection of minimum frequency need take the following considerations:

- A low frequency is good for EMI and load/line regulation, but it will lead a larger transformer
- A high frequency can reduce the transformer size, but cause bad EMI performance.

It is recommended the minimum switching frequency is set from 45k Hz to 50k Hz in a universal input application, here set f_{s_min}=47k Hz.

$$I_o(0,0.01,t_{on\_90V},90,L_p) = 0.35A \quad (8)$$

$$f_{s\_min} = \frac{1}{t_{on\_90V} + t_{off}(t_{on\_90V},90,0.005)} = 47k\ Hz \quad (9)$$

Combining (8) and (9) gets L_P=2.18 mH, t_{on_90V}=9.1 us.

The maximum primary-peak current is:

$$I_{pk\_max} = t_{on\_90V} \cdot \frac{V_{in}(90,0.005)}{L_p} = 0.521A \quad (10)$$

The Primary-Winding RMS Current:

$$I_{pri\_rms}(a,b,t_{on},V_{ac},L_p) = \left\| \begin{array}{l} t1 \leftarrow a \\ sum \leftarrow 0 \\ while(t1 < b) \\ \left\| \begin{array}{l} sum \leftarrow sum + \left\{ \dfrac{1}{t_{on} + t_{off}(t_{on},V_{ac},t1+t_{on})} \int_0^{t_{on}} \left(\dfrac{V_{in}(V_{ac},t1+t_{on})\cdot t}{L_p}\right)^2 \cdot dt \right\} \cdot \\ \left[t_{on} + t_{off}(t_{on},V_{ac},t1+t_{on})\right] \\ t1 \leftarrow t1 + t_{on} + t_{off}(t_{on},V_{ac},t1+t_{on}) \end{array} \right. \\ \sqrt{\dfrac{sum}{b-a}} \end{array} \right. \quad (11)$$

The maximum primary RMS current is then:

$$I_{pri\_rms\_max} = I_{pri\_rms}(0,0.01,t_{on\_90V},90,2.18\cdot10^{-3}) = 0.15\,A \quad (12)$$

The secondary winding RMS current:

$$I_{sec\_rms}(a,b,t_{on},V_{ac},L_p) = \left\| \begin{array}{l} t1 \leftarrow a \\ sum \leftarrow 0 \\ while(t1 < b) \\ \left\| \begin{array}{l} sum \leftarrow sum + \left\{ \dfrac{N^4 \cdot V_o^2 / L_p^2}{t_{on} + t_{off}(t_{on},V_{ac},t1+t_{on})} \int_0^{t_{off}(t_{on},V_{ac},t1+t_{on})} \left(\dfrac{V_{in}(V_{ac},t1+t_{on})\cdot t_{on}}{N\cdot V_o} - t\right)^2 \cdot dt \right\} \cdot \\ \left[t_{on} + t_{off}(t_{on},V_{ac},t1+t_{on})\right] \\ t1 \leftarrow t1 + t_{on} + t_{off}(t_{on},V_{ac},t1+t_{on}) \end{array} \right. \\ \sqrt{\dfrac{sum}{b-a}} \end{array} \right. \quad (13)$$

The maximum secondary winding RMS current is:

$$I_{sec\_rms\_max} = I_{sec\_rms}(0,0.01,t_{on\_90V},90,2.18\cdot10^{-3}) = 0.667\,A \quad (14)$$

The Transformer Core Selection

Select the transformer core based on output power for the entire operating frequency. Ferrite is common in flyback transformers. The core area product ($A_E \cdot A_W$)—which is the core magnetic cross-section area multiplied by the available window area for winding—typically provides an initial core-size estimate for a given application. The following provides a rough estimate of the required area product:

$$A_E \cdot A_W = \left(\frac{L_p \cdot I_{Pk\_max} \cdot I_{rms\_max}}{B_{max} \cdot K_u \cdot K_j} \right) cm^4 \quad (15)$$

Where:

- K_u is winding factor which is usually 0.2 to 0.3 for an off-line transformer,
- K_j is the current-density coefficient (typically 0.06 A/m^2 for ferrite core),
- I_{Pk_max} and I_{rms_max} are the maximum peak current and RMS current of the primary inductor, and
- B_{max} is the maximum-allowed flux density under normal operation—which is usually preset to the saturation flux density of the core material (0.3T to 0.4T).

So the estimated minimum core area product is 0.026 cm^4.

Refer to the manufacture's datasheet to select an appropriate core with sufficient margins. The more margins means transformer can use less winding turns and wider wires which can get higher efficiency. But also, the core shape should best meet the layout dimensions and cost consideration. For this case, choosing an RM6 core provides enough core area with relatively small size.

- A_E = 0.36 cm^2, A_W = 0.26 cm^2, $A_E \times A_W$=0.095 cm^4.
- The core magnetic path length: l_c=2.86 cm
- The relative permeability of the core material: $\mu_\gamma = 2400$

Primary and Secondary Winding Turns

The transformer's primary size requires a minimum number of turns to avoid saturating a given core size. The normal saturation specification is E-t, or the volt-second rating. The E-t rating is the maximum voltage, E, applied over t seconds (The E-t rating is identical to the product of inductance, L, and the peak current). Equation (16) estimates the minimum value of N_P to avoid the core saturation:

$$N_P = \frac{L_p \cdot I_{pk\_max}}{B_{max} \cdot A_E} \times 10^4 \quad (16)$$

Where:

L_p = the primary inductance of the transformer (H)

B_{max}= the maximum allowable flux density (T)

A_E= the effective cross sectional core area (cm^2)

I_{pk_max}= the maximum primary peak current (A)

Select B_{max} to be smaller than the saturation flux density, B_{sat}. B_{max} selection also requires taking the transformer's high-temperature characteristics into account because B_{sat} decreases as the temperature increases. B_{max} also influences the transformer's audible noise: a small B_{max} can reduce audible noise given a narrow window area. For PC40 material, the B_{max} is set to 0.27 to get N_P=115.

The number secondary windings is a function of the turn ratio, N, and primary turn count, N_P:

$$N_s = \frac{N_p}{N} = 23 \quad (17)$$

Wire Size

Once the number of windings have been determined, select the wire size to minimize the winding conduction loss and the leakage inductance. The winding loss depends on the RMS current value, and the wire length and cross section.

Determine the wire size from the winding's RMS current:

$$S_{pri} = \frac{I_{pri\_rms\_max}}{J} = 2.5 \cdot 10^{-2} (mm^2) \quad (18)$$

$$S_{sec} = \frac{I_{sec\_rms\_max}}{J} = 1 \cdot 10^{-1} (mm^2) \quad (19)$$

Where J is the current density of the wire, which is typically 6A/mm^2.

Due to the skin effect and proximity effect of the conductor, select a wire diameter less than 2×Δd (where Δd is the skin-effect depth):

$$\Delta d = \sqrt{\frac{1}{\pi \cdot f_{s\_min} \cdot \mu \cdot \sigma}} = 0.35(mm) \quad (20)$$

Where μ is the conductor's magnetic permeability, which is usually equal to the permeability of a vacuum for most conductors (i.e. $4\pi \times 10^{-7}$ H/m). σ is the wire's conductivity (typically 6×10^{7} S/m at 0° for copper, which increases with temperature).

If the requires wire diameter exceeds 2×Δd, use multiple strands of thinner wire or Litz wire to minimize the AC resistance. Select enough strands such that the effective cross sectional area meets the current density requirement.

In offline isolated applications, the whole system needs to pass the Hipot test, which requires taking the primary to secondary isolation distance into consideration. Small power systems typically use triple-insulated wire (TIW) as the secondary winding wire to enhance the isolation distance. Using TIW negates the need for a retaining wall and conserves the transformer window area.

This case uses 0.18mm×1 wire for the primary winding, 0.33mm×1 T.I.W for the secondary winding, so the wire area for the primary winding is S_1=2.54×10^{-2} mm^2, and for the secondary winding it is S_2=0.86×10^{-1} mm^2.

Auxiliary Winding Wire Size

The auxiliary winding's current requirement is relatively small because it primarily provides power to VCC and detects the current zero crossing for boundary-mode operation. The auxiliary winding's output DC voltage is proportion to the output LED voltage with a turn ratio of N_{aux}/N_s. Higher VCC voltage can help faster start up, but need considerate the VCC pin maximum voltage. Most applications, the VCC is recommended to set as high as 22V-23V. Given an LED output voltage of 20V, select N_{aux} as N_{aux}=23/20×N_s, so N_{aux}=26 for a 0.15mm wire.. If some cases need a higher VCC voltage to meet the start up time, connect a 27V Zener diode from VCC to GND to protect VCC pin from excessive voltage damage.

Window-Area Fill-Factor Calculation

After selecting appropriate wire sizes, check whether the core window area can accommodate the windings. Calculate each winding's required window area, respectively, then add the areas together—be sure to take the interwinding insulation and spaces into consideration. The fill factor—the winding area relative to the whole core window area—should be well below 1 due to these interwinding insulation and spaces between turns. Select a fill factor no greater than 20%.

$$\frac{N_p \cdot S_1 + N_s \cdot S_2 + N_{aux} \cdot S_3}{A_{W\_RM6}} = 0.206 \quad (21)$$

If the required window area exceeds the selected one, reduce either the wire size or use a larger core. However, reducing the wire size increases the transformer copper loss.

Air Gap

With a selected core and winding turns, the core air gap is approximately:

$$G = \mu_0 \cdot A_E \cdot \frac{N_P^2}{L_p} - \frac{l_c}{\mu_r} = 0.4\,(mm) \quad (22)$$

Where A_E is the cross sectional area of the selected core, μ_0 is the permeability of vacuum which equals $4\pi \times 10^{-7}$ H/m., L_p and N_P is the primary winding inductance and turns respectively, l_c is the core magnetic path length and μ_r is the relative magnetic permeability of the core material.

Instructions for Transformer Manufacturing

The coupling between the transformer primary side and the secondary side must be as tight as possible to minimize leakage inductance. This can be accomplished by interleaving the primary and secondary windings during transformer manufacture, as shown in Figure 17. Start with one half primary winding connected to the drain of the MOSFET first, followed by the auxiliary winding, and then the secondary winding, and last is the other half primary winding. This structure also can help keep the secondary winding far away from the drain dot to reduce parasitic capacitance to improve the CM EMI. To meet the safety requirements, separate the transformer's primary side and secondary side and keep a safe creepage distance of at least 6mm. Do not directly connect the auxiliary winding pin (AUX+) and the two secondary winding pins (W and B) to the transformer pins. Instead, use jumpers and connect externally, as per Figure18. To further improve EMI, especially for the CM EMI, a 0.025mm*6mm cooper is adhered to the core's periphery and connected to the primary GND (The E shown in Figure 18).

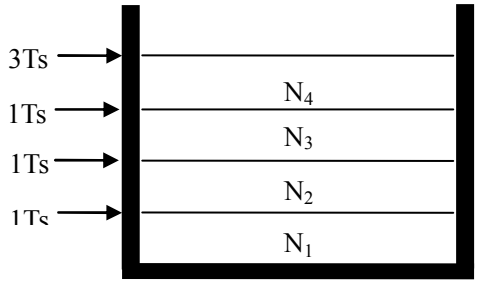


Figure 17: Transformer Winding Diagram

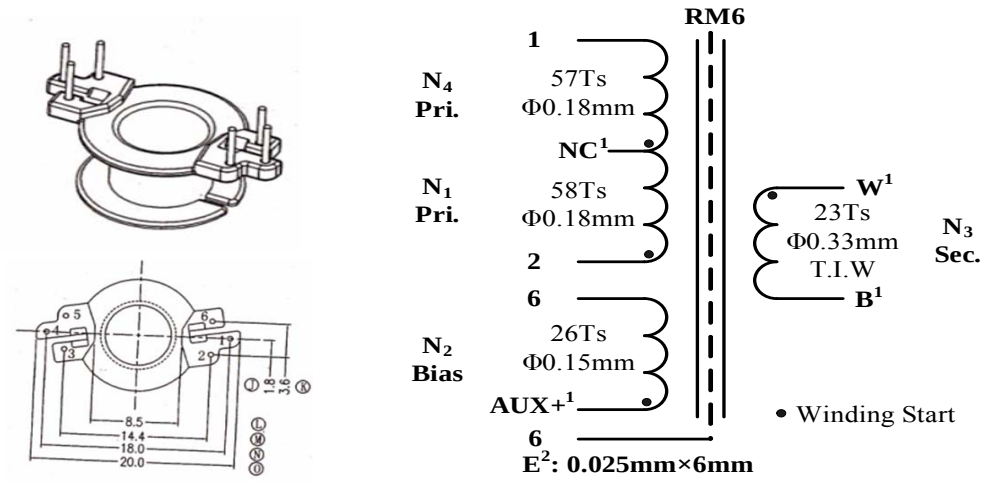


Figure 18: Transformer Pin Out and the Connection Diagram

E. INPUT EMI FILTER (L1, L2, L3, CX1, CY1, C2)

The input EMI filter is comprised of L1, L2, L3, CX1, with the Y-class capacitor, CY1, and input film capacitor, C2. The EMI filter has two stages with –80dB attenuation for the DM noise. Soldering the L2 and L3 inductors to the L and N lines, respective, also acts as a CM noise filter. Select component values to pass EMI test standards, as well as to account for the power factor. The input capacitance plays the primary role for the power factor, a small input capacitance increase the power factor.

F. INPUT BRIDGE (BD1)

The input bridge can use standard, slow-recovery, low-cost diodes. When selecting diodes, take into account these three items: the maximum input RMS current; the maximum input-line voltage; and thermal performance. The maximum input-line voltage occurs during surge conditions, where the surge voltage across the line may exceed 600V. This example uses MB6S as the BD, with a 600V, 0.5A rating.

G. INPUT CAPACITOR (C2)

The input capacitor, C2, mainly provides the transformer's switching frequency magnetizing current. The maximum current occurs at the peak of the input voltage. Limit the capacitor's maximum high-frequency voltage ripple to 10%, or the voltage ripple can cause the primary peak current to spike and worsen both the power loss and the EMI performance.

$$C2 > \frac{I_{pk\_max} - \sqrt{2} I_{pri\_rms\_max}}{2 \cdot \pi \cdot f_{s\_min} \cdot \sqrt{2} \cdot V_{ac\_min} \cdot 0.1} = 82nF \quad (23)$$

Input capacitor selection also requires taking into account the EMI filter, the power factor. A large capacitor improves EMI, but limits the power factor. This case uses a 100nF, 400V, CBB capacitor.

H. OUTPUT CAPACITOR (C8, C9)

The output voltage ripple has two components: the switching-frequency ripple associated with the flyback converter, and the low-frequency ripple associated with the input-line voltage (100Hz). Selecting the output bulk capacitor depends on the output current, the output voltage, the desired voltage ripple, and the LED current ripple. This case has a load of 6 LEDs in series, a 350mA output current, and a current ripple set within 60%. Since the LED impedance is not resistive, the output voltage ripple refers to the LED V-I characteristics as provided by the LED manufacturer to design the output voltage ripple within 3%.

The maximum RMS current of the output capacitor is:

$$I_{out\_cap\_rms\_max} = \sqrt{I_{sec\_rms\_max}^{2} - I_{o\_rms}^{2}} \quad (24)$$

Where I_{o_rms} is the output RMS current and $I_{sec\_rms\_max}$ is the maximum secondary RMS current from equation (14). Design the maximum RMS current to be smaller than the capacitor's RMS current specification.

The maximum switching voltage ripple occurs at the peak of the minimum-rated input line voltage, and the ripple (peak-to-peak) can be estimated by:

$$\Delta V_{o\_swtiching} = \frac{I_{o\_max} \cdot t_{off}(t_{on\_90V}, 90, 0.005)}{C_{out}} + (I_{sec\_pk\_max} - I_{o\_max}) \cdot R_{ESR} \quad (25)$$

Where I_{o_max} is the maximum instantaneous output LED current with a mean value of 350mA plus a 30% peak ripple; $t_{off}(t_{on\_90V}, 90, 0.005)$ is the turn-off time at the peak of the minimum-rated input line, R_{ESR} is the ESR of output capacitor (typically 0.03Ω per capacitor), and $I_{sec\_pk\_max}$ is the maximum peak current of the secondary winding.

Estimate the maximum low-frequency ripple (2x the line frequency, 100Hz) from the capacitor impedance and the peak capacitor current (I_{o_max}).

$$\Delta V_{o\_line} = I_{o\_max} \sqrt{\frac{1}{(2\pi \cdot 2f_{line} \cdot C_{out})^{2}} + R_{ESR}^{2}} \quad (26)$$

Based on this equation, the 100Hz low-frequency ripper dominates the output voltage ripple. Set $\Delta V_{o\_line} = 0.7V$ for C_{out}=600μF. Selecting two 330μF/35V bulk capacitors in parallel minimizes the ESR and distributes the capacitor RMS current value. Add a 30kΩ pre-load resistor to discharge the output voltage under open-load conditions.

I. RCD Snubber (R14, C6, D3)

The peak voltage across the MOSFET at turn-off includes the instantaneous input line voltage, the voltage reflected from the secondary side, and the voltage spike due to leakage inductance. The RCD snubber (shown in Figure 19) protects the MOSFET from over-voltage damage by absorbing the leakage inductance energy and clamping the drain voltage. The values of C1 and R2 depend on the leakage inductance energy dissipated by the RC network during each cycle. Figure 20 shows the primary MOSFET drain-source voltage ripple and the snubber capacitor at point A during the turn-off interval.

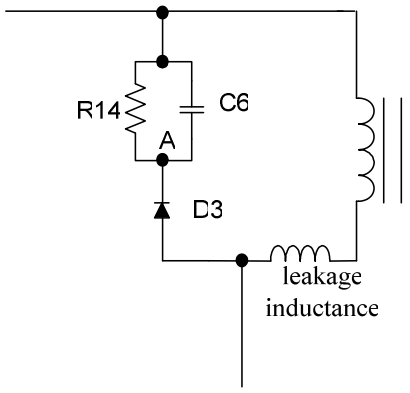


Figure 19: Primary-Side RCD Snubber

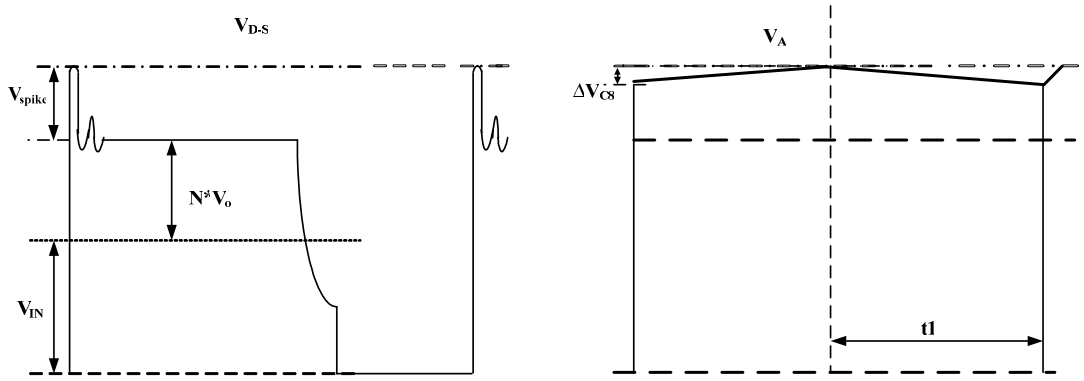


Figure 20: A Point Voltage with a High-Side MOSFET Drain Voltage and Snubber Capacitor

Estimate the energy stored in the leakage inductor at the maximum input voltage as:

$$E_{Lk\_max} = \frac{1}{2} \cdot L_{leakage} \cdot I_{pk\_V_{in\_max}}{}^2 \quad (27)$$

Where $I_{pk\_Vin\_max}$ is the peak current for the primary side at the maximum input voltage. Assume all the leakage inductance energy transfers to the snubber capacitor. The secondary relationship is:

$$E_{Lk\_max} = \frac{1}{2} \cdot C6 \cdot \left[(V_{in\_max} + N \cdot V_o + V_{spike})^2 - (V_{in\_max} + N \cdot V_o + V_{spike} - \Delta V_{C6})^2 \right] \quad (28)$$

Where V_{spike} is the spike voltage clamped by the RCD snubber, ΔV_{C6} is the snubber capacitor's voltage change caused by the leakage inductance.

Assuming $\Delta V_{C6} << V_{spike}$, and the $\frac{1}{4} \cdot 2\pi \cdot \sqrt{L_{leakage} \cdot C6} < T_{Vin\_max}$,

$$\Delta V_{C6} = V_{spkie} \cdot (1 - e^{-\frac{t1}{R14 \cdot C6}}) \quad (29)$$

Where t1 is the time $T_{Vin\_max} - \frac{1}{4} \cdot 2\pi \cdot \sqrt{L_{leakage} \cdot C6}$, and τ_{Vin_max} is the switching period at V_{in_max}.

To select R14, take into account the secondary-side reflecting voltage because it contributes to the snubber resistance after the MOSFET turns off. Select R14 to be large enough to reduce the reflecting voltage loss, but avoid contributing to a clamping voltage that exceeds the selected MOSFET based on equation (1).

Based on equations (6), (7), and (10), $I_{pk\_Vin\_max}$=0.345A, $T_{on\_Vin\_max}$=2.1μs, and T_{Vin_max}=10.8μs. The leakage inductance is estimated as 2% of the primary inductance, 40μH. Select the snubber parameters: C6=22nF, R14=100kΩ for V_{SPIKE}=57V and ΔV_{C6}=0.28V.

Select a snubber capacitor with a higher voltage rating than the spike voltage, and a diode voltage rating higher than V_{in_max} + V_{spike}—use a normal-recovery diode, such as a S1ML, which has better EMI performance than a fast-recovery diode. Given the difficulty in theoretically calculating the power dissipation of the snubber resistor R14, monitor the resistor's thermal performance during testing to determine the final appropriate value and power level.

J. VCC POWER SUPPLY (R4, R15, C3, D2,)

Page 10 shows the detailed VCC operation timing sequence. The C3 should be large enough to hold the VCC voltage not drop below UVLO threshold before the auxiliary winding can take charge of the

VCC power supply at start up. Usually, a >4.7uF ceramic cap is selected. The start resistor R4 with C3 determines the system start delay time, if a shorter delay time is required, select a smaller R4, but the power dissipation of the resistor and the charging current need to be taken care, too big charging current will make the VCC can not drop below UVLO threshold when fault condition happens, so the IC can not restart, here a 470kΩ resistor is selected. The resistor R15 is used to limit the charging current from the auxiliary winding, or the VCC may exceed the ABS value if the transformer leakage inductance is big. But the resistance can not be selected too big, or the power dissipation and the voltage drop between auxiliary winding and VCC will both increase. Usually, the resistor is selected from 100Ω~1kΩ. The voltage rating for the rectifying diode D2 should meet the following equation:

$$V_{D2} > VCC_{max} + \frac{N_{aux}}{N_p} \cdot V_{in\_max} + V_{aux\_negtive\_spike} \quad (30)$$

Where VCC_{max} is the maximum VCC voltage, in this case, VCC_{max}= 23V, N_{aux} and N_p are the auxiliary winding and primary winding turns, $V_{aux\_negtive\_spike}$ is the maximum negative spike on auxiliary winding, in this case, $V_{aux\_negtive\_spike}$= 40V, so D5 need a voltage rating higher than 130V. Here chosen 200V/0.2A diode BAV21W with 100Ω R15

K. ZCD AND OVP DETECTOR (R9, R10, D4)

Refer to information starting on page 14 for additional information.

The resistor divider, R9 and R10, sets the OVP threshold:

$$(V_{o\_ovp} \cdot \frac{N_{aux}}{N_s} - V_{D4} - V_{R15}) \cdot \frac{R9}{R10 + R9} = 5.1V \quad (31)$$

Where V_{o_ovp} is the output OVP voltage, N_{aux} is the number of transformer auxiliary winding turns, and N_s is the number of transformer secondary winding turns, V_{D4} is forward voltage of D4, V_{R15} is the voltage drop of R15. Given N_{aux}=26, N_s=23, V_{D4}=0.7V, V_{R15} can be estimated as about 2*2mA*100=0.4V, set V_{o_ovp}=25V for R10/R9=4.3. Consider R9 should be smaller than 3kΩ, select R9=2.2kΩ, get R10=9.53kΩ.

D4 is used to block the negative voltage of auxiliary winding when the MOSFET is turn on, the diode can use normal type, the voltage rating is same with equation (30). Please note, the diode with small junction capacitance is very useful to suppress the spike voltage at MOSFET turning off, or the high spike may exceed the ABS value CS/ZCD pin and bring potential danger. It is recommended the junction capacitance C_J should be small than 3pF, here chosen the BAV21W with 1.5pF C_J.

L. CURRENT SENSING (R11, R12, C1)

As described on page 6, approximate the current sensing resistor with the following equation:

$$R_s \approx \frac{V_{FB} \cdot N}{2 \cdot I_o} \quad (32)$$

Where N is the turn ratio of primary winding to secondary winding, V_{FB} is the feedback reference voltage (typically 0.414V), and R_s is the sense resistor.

Equation (32) describes R_S under ideal BCM operation, but in real applications, some factors also influence the output current, such as the IC's internal logic delay, the transformer inductance, and the ZCD detection delay. These factors make estimating the output current difficult, and why designing the current sensing resistor last allows for better fine-tuning for the required output current. In this case, the

sensing resistor is tuned to 1.8Ω in series with 1.1Ω. A bypass capacitor C1 is added from CS/ZCD pin to GND to absorb the high frequency noise to make the sample signal more precise.

M. MULT PIN RESISTOR DIVIDER (R5, R6, C4)

For the MULT pin resistor divider setting information, please refer to page 11. Here selecting the R5=6.2kΩ, R6=1MkΩ,, C4=2.2nF..

N. FEEDFORWARD RESISTOR (R7)

The resistor R7 is used to add Vin feedforward for CS/ZCD pin to help improve the line regulation, or the MOSFET turn off delay will make the line regulation bad. The value of R7 should be fine tuned, and related to some factors such as primary inductance, MOSFET type, etc. Here, after tuned, the R7 is selected as 43kΩ with <5mA output current variation in line regulation.

O. GATE DRIVER RESISTOR (R8)

Considering both for the EMI performance and the MOSFET switching speed, the gate driving resistor (R8) is selected as 20Ω.

P. LOOP COMPENSATION CAPACITOR (C5)

Please refer to page 13 for detailed selection information.

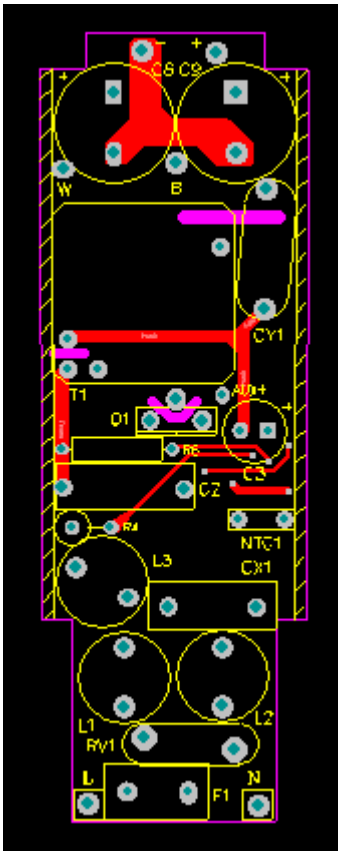
Here, considering both for the system start up time and PF, THD result, chosen C5=1uF.

Q. NTC THERMISTOR (NTC, C7)

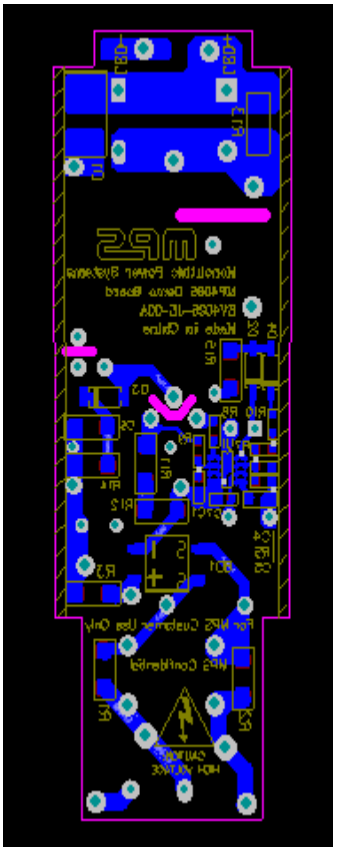
The output current adjusting happens when NTC voltage decrease lower than 1.2V, so calculation the corresponding resistance as R=1.2V/60uA=20kΩ. Refer to the thermistor datasheet to find the expected temperature when resistance is 20 kΩ. Here chosen 220kΩ Murata thermistor, the temp when resistance decreasing to 20 kΩ is about 80° C. A 2.2nF bypass capacitor is added beside the pin to absorb the high frequency noise.

R. LAYOUT GUIDELINE

- Design the main power flow path as short as possible using wide wires. Design the sense resistor GND return to directly connect to the input capacitor, C2. Use the largest-possible cooper pour for the power devices for good thermal performance.
- Separate the power GND and the analog GND, connect them together only at IC GND pin or other single point.
- Place the IC pin components as close as possible to the corresponding pins. Provide the ZCD pin bypass capacitor, NTC bypass capacitor and the COMP pin capacitor layout priority.
- Place the EMI filter inductor L1 and L2 right in parallel with each other.
- Isolate the primary side and the secondary side by at least 4mm to meet safety requirements and the Hipot test. Tune the transformer installation position to keep the primary side far away from secondary side.
- In order to pass the surge test, separate the input high voltage wire from other components and GND. It is better to connect R4, and R6 to the rectified input line for the DIP package.
- On the secondary side, place the rectifying diode as close as possible to the output filter capacitor, and use a short trace from the transformer output return pin to the return point of the output filter capacitor.



Top View



Bottom View

Figure 21: Board layout

S. BOM

Quantity	Designator	Value	Description	Package	Manufacturer	Manufactuer_P/N
1	BD1	MB6S	BRIDGE, 600V, 0.5A	SOIC-4	Taiwan Semiconductor	MB6S
1	C1	10pF/50V	Ceramic Cap,C0G,50V	0603	murata	GRM1885C1H100JA01
1	C2	100nF/400V	CBB, 104/400V	DIP	Panasonic	CBB 0.1μF/400V
1	C3	4.7μF/50V	Ceramic Cap,X7R,50V	1206	murata	GRM31CR71H475KA12L
1	C4	2.2nF/50V	Ceramic Cap,X7R,50V	0603	TDK	C1608X7R1H222K
1	C5	1μF/10V	Ceramic Cap,X7R,10V	0603	murata	GRM188R71A105KA61D
1	C6	22nF/630V	Ceramic Cap,X7R,630V	1206	TDK	C3216X7R2J223K
1	C7	2.2nF/50V	Ceramic Cap,X7R,50V	0603	TDK	C1608X7R1H222K
2	C8,C9	330μF/35V	Electrolytic Capacitor;35V;Electrolytic	DIP	Jianghai	CD263-35V330
1	CX1	22nF/275V	X Capacitor,275V	DIP	Caili	PX223K3IB19L270D9R
1	CY1	2.2nF	Y Capacitor,4000V	DIP	Hongke	JNK12E222MY02N
1	D1	MBRS3200T3G	Diodes,200V,3A	SMB	ON Semiconductor	MBRS3200T3G
2	D2,D4	BAV21W	Diodes,200V,0.2A	SOD-123	Diodes	BAV21W-7-F
1	D3	S1ML	Diodes,1000V,1A	SMA	Diodes	Taiwan Semiconductor
1	F1	250V/2A	SS-5-2A	DIP	COOPER BUSSMANN	SS-5-2A
3	L1,L2,l3	Inductor,1.5mH	Inductor,15mH/0.21A	DIP	TDK	TSL0808RRA-152KR21
1	Q1	ISU04N65A	650V/4A	TO-251	IPS	ISU04N65A
3	R1,R2,R3	5.1kΩ	RES,1%	1206	Yageo	RC1206FR-075K1L
1	R4	470k	DIP,0.5W RESISTOR	DIP	any	
1	R5	5.23kΩ	Film RES, 1%	0603	Yageo	RC0603FR-075K23L
1	R6	1MΩ	DIP,0.25W RESISTOR	DIP	any	
1	R7	43kΩ	Film RES,1%	0603	LION	RC0603FR-0743KL
1	R8	20Ω	Film RES, 1%	0603	Yageo	RC0603FR-0720RL
1	R9	2.2kΩ	Film RES, 1%	0603	Yageo	RC0603FR-072K2L
1	R10	9.53kΩ	Film RES, 1%	0603	Yageo	RC0603FR-079K53L
1	R11	1.8Ω	RES, 1%	1206	Yageo	RC1206FR-071R8L
1	R12	1.1Ω	Film RES, 1%	1206	Yageo	RC1206FR-071R1L
1	R13	30kΩ	Film RES, 1%	1206	Yageo	RC1206FR-0730KL
1	R14	100kΩ	Film RES,5%	1206	Yageo	RM12JTN104
1	R15	100Ω	Film RES, 1%	1206	Yageo	RC1206FR-07100RL
1	RV1	TVR10431KSY	430V/2500A	DIP	TKS	TVR10431KSY
1	T1	RM6	RM6, Np:Ns:Naux=115:23:26, Lp=2.18mH	RM6	EMEI	FX0314
1	U1	MP4027	MP4027GJ	SOT23-8	MPS	MP4027GJ
1	NTC	220kΩ	NTC Thermistor	0603	murata	NCP18WM224E03RB

5. EXPERIMENTAL RESULT

All measurements performed at room temperature

5.1 PERFORMANCE DATA

6LEDs

V_{IN}(VAC)	P_{IN}(W)	Vo(V)	I_{6LEDs}(A)	Po(W)	Efficiency	PF
90	8.12	19.71	0.347	6.84	84.23%	0.993
100	8.01	19.63	0.348	6.83	85.28%	0.991
110	7.97	19.63	0.348	6.83	85.71%	0.989
120	7.94	19.63	0.348	6.83	86.04%	0.987
135	7.92	19.62	0.348	6.83	86.21%	0.982
185	7.91	19.59	0.347	6.80	85.94%	0.962
200	7.93	19.59	0.347	6.80	85.72%	0.954
220	7.97	19.58	0.346	6.77	85.00%	0.94
230	7.98	19.58	0.346	6.77	84.90%	0.933
250	8.04	19.58	0.346	6.77	84.26%	0.917
265	8.09	19.58	0.346	6.77	83.74%	0.904

5LEDs

V_{IN}(VAC)	P_{IN}(W)	Vo(V)	I_{5LEDs}(A)	Po(W)	Efficiency	PF
90	6.81	16.39	0.35	5.74	84.24%	0.991
100	6.75	16.38	0.351	5.75	85.18%	0.989
110	6.72	16.38	0.351	5.75	85.56%	0.986
120	6.7	16.37	0.351	5.75	85.76%	0.983
135	6.69	16.37	0.351	5.75	85.89%	0.977
185	6.7	16.36	0.35	5.73	85.46%	0.952
200	6.72	16.34	0.35	5.72	85.10%	0.942
220	6.77	16.33	0.35	5.72	84.42%	0.925
230	6.79	16.32	0.349	5.70	83.88%	0.915
250	6.84	16.32	0.349	5.70	83.27%	0.895
265	6.88	16.32	0.349	5.70	82.79%	0.878

4LEDs

V_{IN}(VAC)	P_{IN}(W)	Vo(V)	I_{4LEDs}(A)	Po(W)	Efficiency	PF
90	5.6	13.27	0.353	4.68	83.65%	0.989
100	5.55	13.27	0.353	4.68	84.40%	0.986
110	5.53	13.27	0.353	4.68	84.71%	0.982
120	5.53	13.27	0.353	4.68	84.71%	0.979
135	5.53	13.27	0.353	4.68	84.71%	0.972
185	5.55	13.28	0.353	4.69	84.47%	0.935
200	5.6	13.27	0.353	4.68	83.65%	0.927
220	5.65	13.25	0.353	4.68	82.78%	0.906
230	5.66	13.25	0.353	4.68	82.64%	0.895
250	5.71	13.25	0.353	4.68	81.91%	0.871
265	5.78	13.26	0.353	4.68	80.98%	0.853

3LEDs

V_{IN}(VAC)	P_{IN}(W)	Vo(V)	I_{3LEDs}(A)	Po(W)	Efficiency	PF
90	4.29	9.84	0.356	3.50	81.66%	0.985
100	4.24	9.84	0.356	3.50	82.62%	0.98
110	4.22	9.84	0.356	3.50	83.01%	0.976
120	4.21	9.84	0.356	3.50	83.21%	0.97
135	4.21	9.84	0.356	3.50	83.21%	0.96
185	4.29	9.84	0.356	3.50	81.66%	0.918
200	4.31	9.84	0.356	3.50	81.28%	0.898
220	4.36	9.84	0.356	3.50	80.34%	0.873
230	4.39	9.84	0.357	3.51	80.02%	0.857
250	4.45	9.83	0.357	3.51	78.86%	0.828
265	4.51	9.84	0.357	3.51	77.89%	0.806

5.2 LINE AND LOAD REGULATION

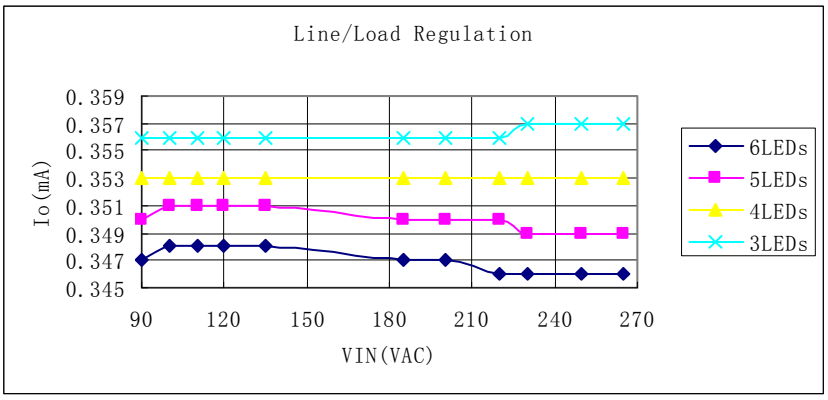


Figure 22: Line/Load Regulation

5.3 EFFICIENCY

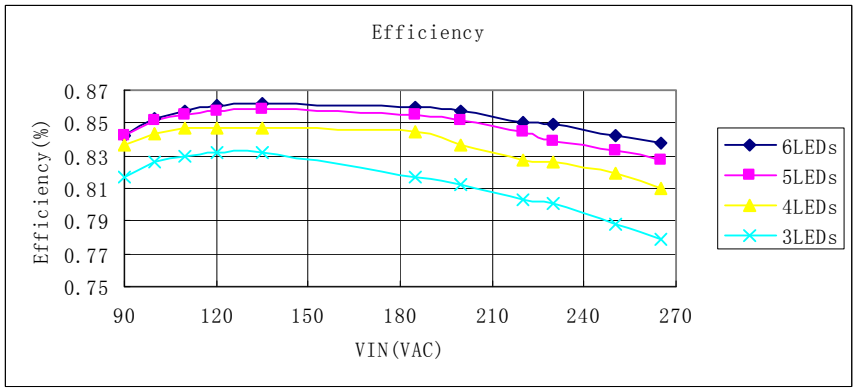
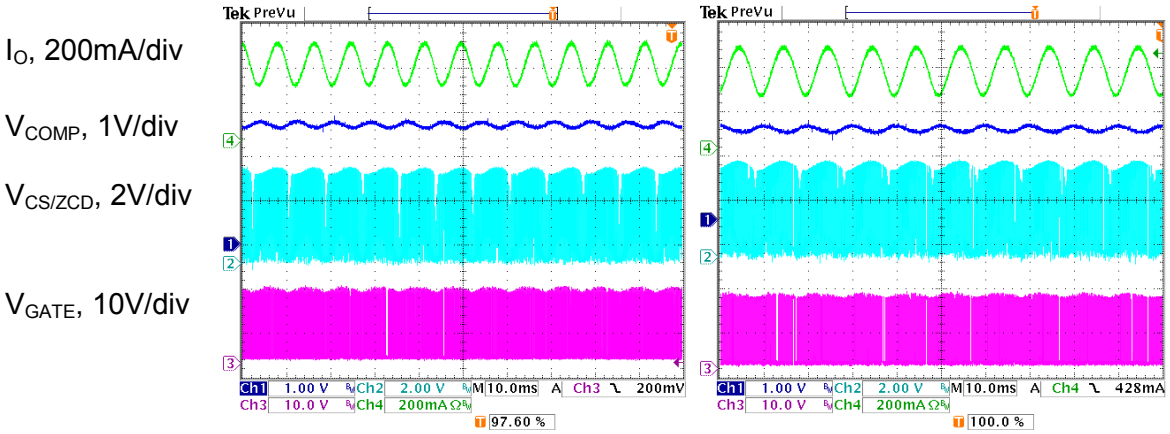


Figure 23: Efficiency

5.4 STEADY STATE



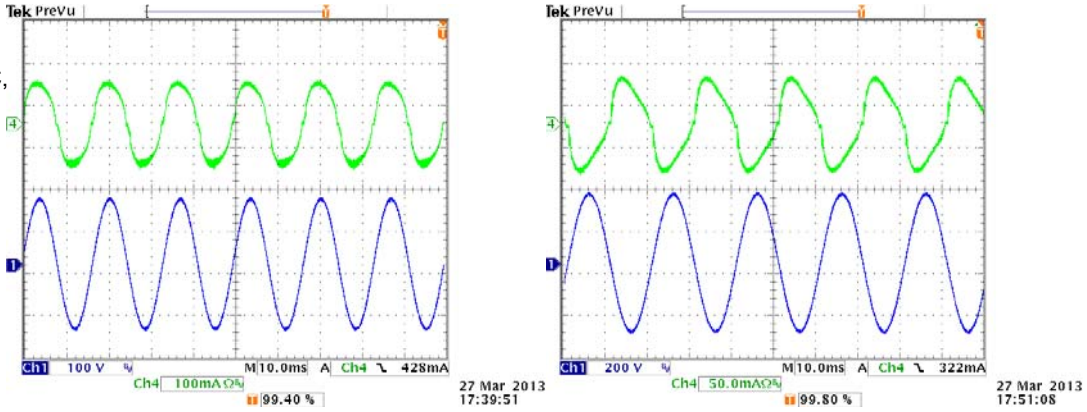
110VAC **230VAC**

Figure 24: 110/230VAC, Full Load, 10ms/div

5.5 INPUT VOLTAGE AND CURRENT

I_{IN}, 100mA/div-110VAC, 50mA/div-230VAC

V_{IN}, 100V/div-110VAC, 200V/div-230VAC



110VAC **230VAC**

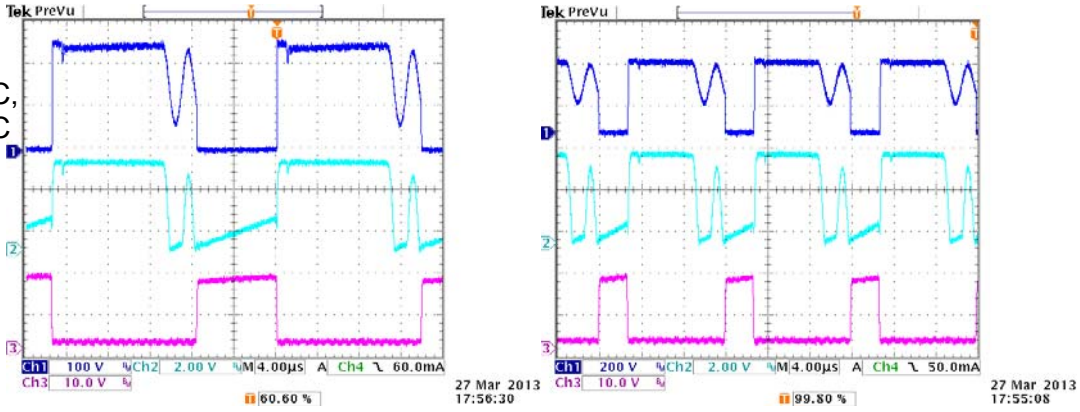
Figure 25: 110/230VAC, Full Load, 10ms/div

5.6 BOUNDARY CONDUCTION OPERATION

V_{DRAIN}, 100V/div-110VAC, 200V/div-230VAC

$V_{CS/ZCD}$, 2V/div

V_{GATE}, 10V/div



110VAC **230VAC**

Figure 26: 110/230VAC, Full Load, 4us/div

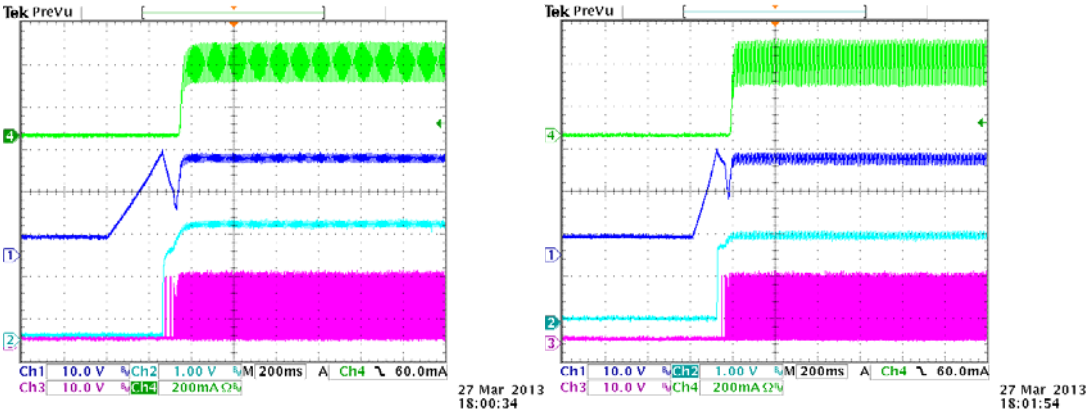
5.7 START UP

I_O, 200mA/div

V_{CC}, 10V/div

V_{COMP}, 1V/div

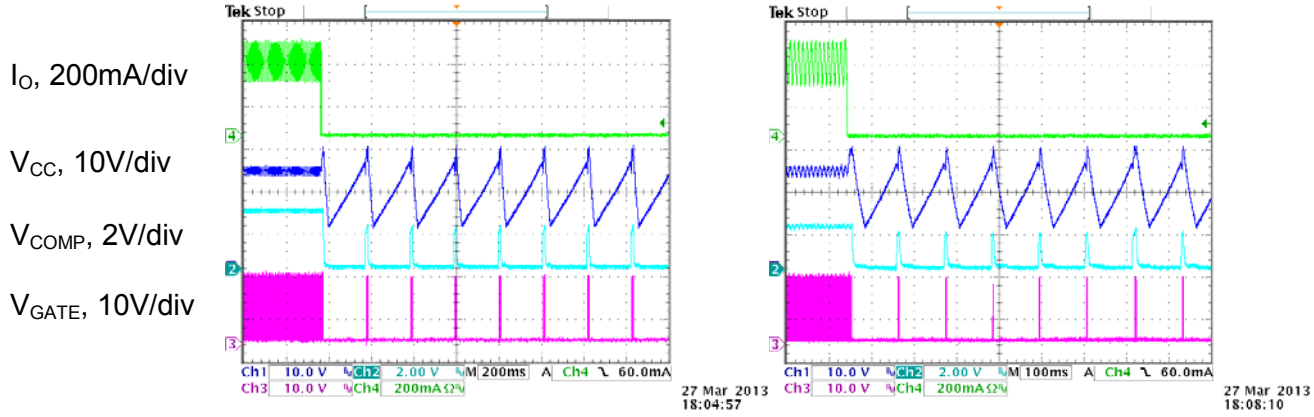
V_{GATE}, 10V/div



110VAC **230VAC**

Figure 27: 110/230VAC, Full Load, 200ms/div

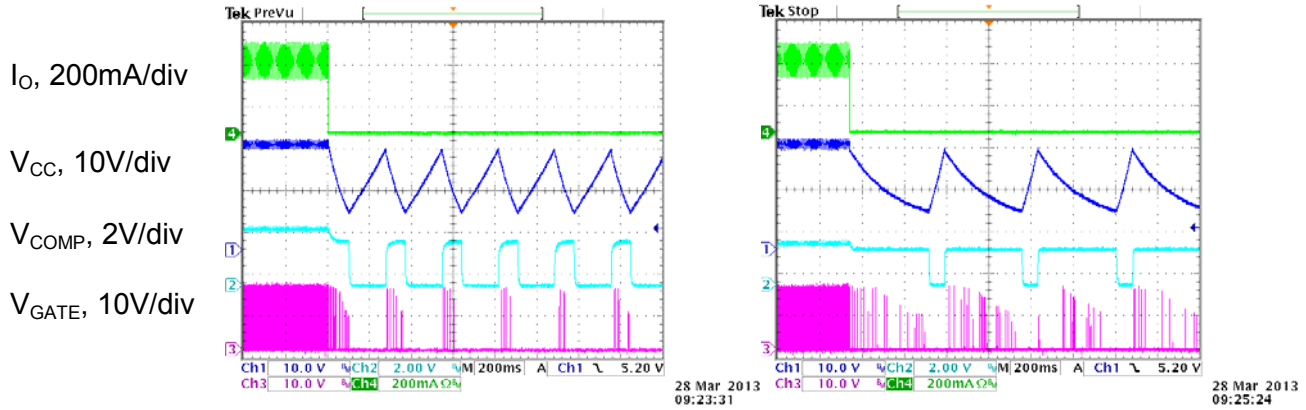
5.8 OVP (OPEN LOAD AT NORMAL OPRATION)



110VAC **230VAC**

Figure 28: 110/230VAC, Full Load, 200ms/div-110VAC, 100ms/div-230VAC

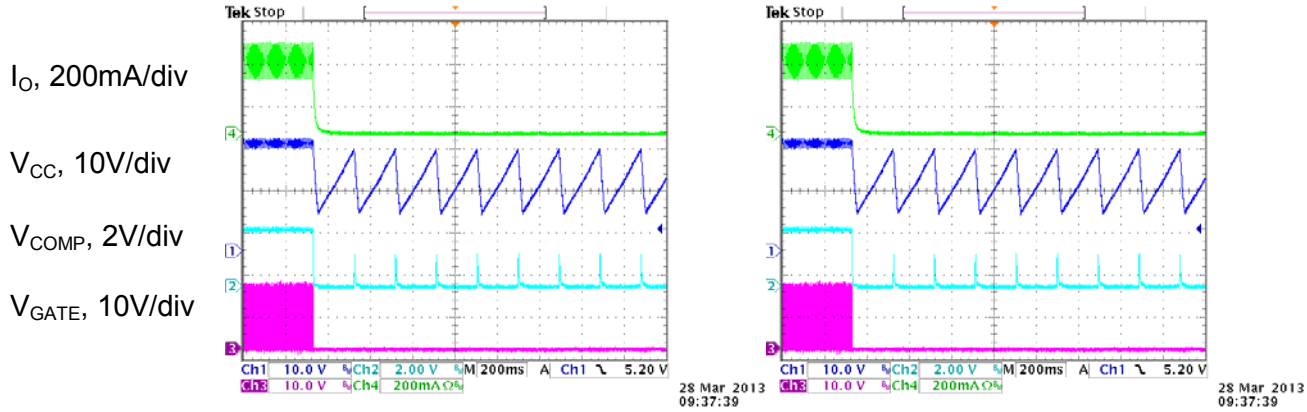
5.9 SCP (SHORT LED+ TO LED– AT NORMAL OPERATION)



110VAC **230VAC**

Figure 29: 110/230VAC, Full Load, 200ms/div

5.10 PRIMARY-SIDE OCP (SHORT PRIMARY WINDING AT NORMAL OPRATION)



110VAC **230VAC**

Figure 30: 110/230VAC, Full Load, 200ms/div

5.11 NTC CURVE

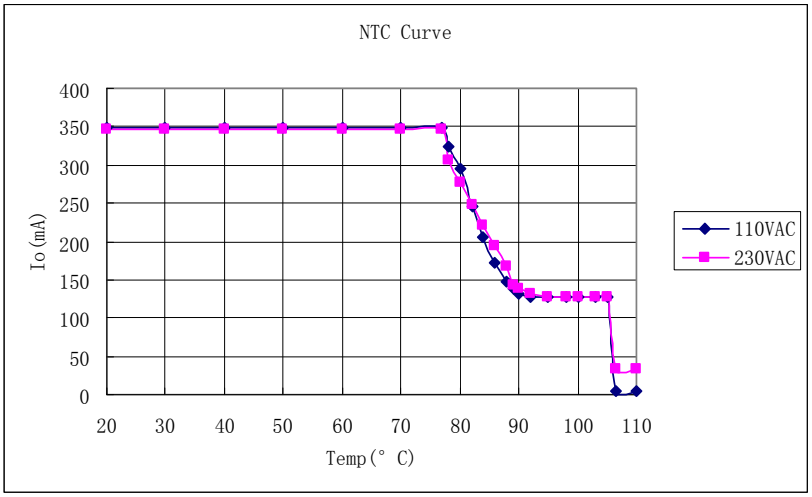
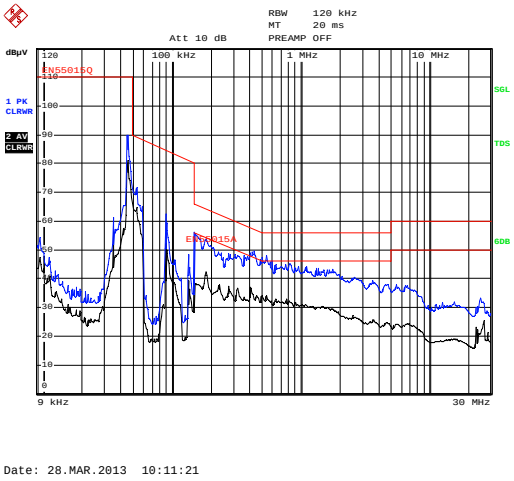
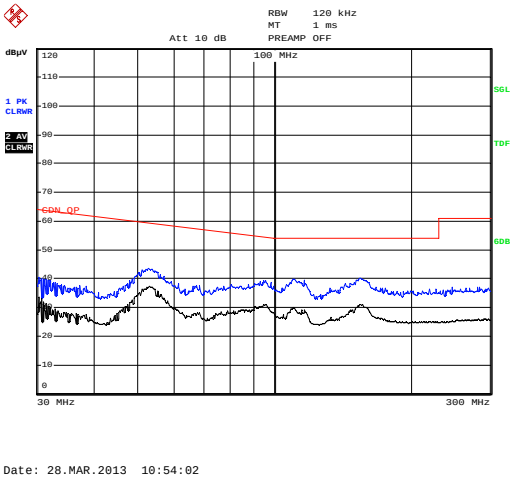


Figure 31: NTC Curve

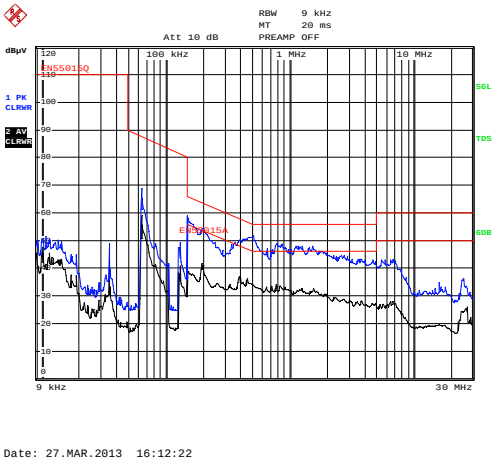
5.12 EMI PERFORMANCE

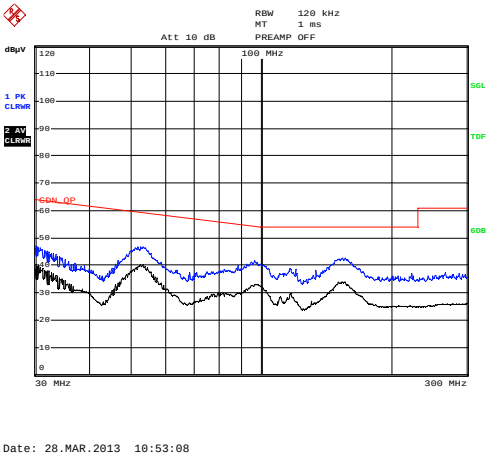




Conduction **CDN Test**

Figure 32: 110VAC EMI Performance





Conduction **CDN Test**

Figure 33: 230VAC EMI Performance

5.13 SURGE TEST

Line to Line 500V and Line to Power Earth 1kV surge testing was completed according to IEC61547. Input voltage was set at 230VAC/50Hz. Output was loaded at full load and operation was verified following each surge event.

Surge Level (V)	Input Voltage (VAC)	Injection Location	Injection Phase (°)	Test Result (Pass/Fail)
500	230	L to N	90	Pass
-500	230	L to N	270	Pass
1000	230	L to PE	90	Pass
-1000	230	L to PE	270	Pass
1000	230	N to PE	90	Pass
-1000	230	N to PE	270	Pass