PRODUCT RELIABILITY REPORT

Product: MP28313

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Monolithic Power Systems, Inc.

1. Device Information

Product:	MP28313
Package:	SOIC8
Process Technology:	BCD
Report Date:	12/18/2015

2. Summary of Test Results

Test	Test Condition	Lot# or Date Code	Test Results (S.S./Rej)	Comment
Temperature, Bias, and Operating Life	JESD22-A108, @+125°C for 1000 hours or equivalent	F580274.9 C888364.9A C888364.9B	80/0 80/0 80/0	
ESD: Human Body Model (HBM)	ANSI/ESDA/JEDEC JS-001	F288464.8	3/0	>2000V
ESD: Device Charged Model (CDM)	ANSI/ESDA/JEDEC JS-002	F288464.8	3/0	>750V
Latch-up	EIA/JESD78	F288464.8	6/0	>+/-100mA & >1.5Vccmax
Moisture/Reflow Sensitivity	J-STD-020	1211 1214 1216	300/0 300/0 300/0	MSL=2
High Temperature Storage Life	JESD22-A103, @150°C for 1000 hours	1211 1214 1216	50/0 50/0 50/0	
Temperature Cycling	JESD22-A104, from -65°C to 150°C for 1000 cycles or equivalent	1211 1214 1216	80/0 80/0 80/0	
Accelerated Moisture Resistance- Unbiased Autoclave	JESD22-A102, @121°C/100%RH for 168 hours or equivalent	1211 1214 1216	80/0 80/0 80/0	
Steady State Temperature Humidity Bias Life Test	JESD22-A101, @85°C/85%RH static bias at Vinmax for 1000 hours or equivalent	1128 1214 1452	80/0 80/0 80/0	

3. Failure Rate Calculation

Sample Size:	7210
Rejects:	0
Activation Energy (eV):	0.7
Equivalent Device Hours:	5.62×10^{8} Hours
Failure Rate (FIT@60%CL):	1.6 FIT
MTBF (years):	70,162 Years

Revision / Update History

Revision	Reason for Change	Date	Rel Engineer
1.0	Initial release	December 2015	Ramon Lei

Appendix: Description of Reliability Test and Failure Rate Calculation

High Temperature Operating Life Test

Purpose: This test is a worst-case life test that checks the integrity of the product. The high temperature testing is use for acceleration of any potential failures over time. The calculation for failure rate (FIT) using the operating ambient temperature is done using the Arrhenius equation.

Condition: 125C @ Vccmax

Pass Criteria: All units must pass the min/max limits of the datasheet.

ESD Test

Purpose: The purpose of the ESD test is to guarantee that the device can withstand electrostatic voltages during handling.

Condition: Human Body Model and Charged Device Model

Pass Criteria: ESD Testing on every pin. The device must be fully functional after testing and pass the min/max limits in the datasheet.

IC Latch-Up Test

Purpose: The purpose of this specification is to establish a method for determining IC latch-up characteristics and to define latch-up failure criteria. Latch-up characteristics are extremely important in determining product reliability and minimizing No Trouble Found (NTF) and Electrical Overstress (EOS) failures due to latch-up.

Condition: Voltage and current injection

Pass criteria: All pins with the exception of “no connect” pins and timing related pins, shall be latch-up tested. The device must be fully functional after testing and pass the min/max limits in the datasheet.

Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices

Purpose: The purpose of this standard is to identify the classification level of nonhermetic solid state surface mount devices (SMDs) that are sensitive to moisture-induced stress so that they can be properly packaged, stored, and handled to avoid damage during assembly solder reflow attachment and/or repair operations.

Condition: Bake + moisture sock + 3X reflow at 260C

Pass criteria: All units must pass the min/max limits of the datasheet

High Temperature Storage Life

Purpose: The test is typically used to determine the effects of time and temperature, under storage conditions, for thermally activated failure mechanisms and time-to-failure distributions of solid state electronic devices, including nonvolatile memory devices (data retention failure mechanisms).

Condition: Bake at 150C

Pass Criteria: All units must pass min/max limits of the datasheet

Accelerated Moisture Resistance- Unbiased Autoclave

Purpose: To check the performance of the device in humid environments. This test checks the integrity of the passivation, poor metal to plastic seal and contamination level during assembly and material compatibility.

Condition: 121C/15psig/100% RH (no bias)

Pass Criteria: All units must pass min/max limits of the datasheet

Temperature Cycle Test

Purpose: This test is used to evaluate the die attach integrity and bond integrity. This is similar to the Thermal Shock test, but can generate different failure modes due to the longer dwell time and gradual temperature change.

Condition: -65C to 150C

Pass Criteria: All units must pass min/max limits of the datasheet

Steady State Temperature Humidity Bias Life Test

Purpose: This is to check the performance of the device in humid environments. This test checks the integrity of the passivation, poor metal to plastic seal and contamination level during assembly and material compatibility.

Condition: 85%RH at 85C with Vin=Vinmax

Pass Criteria: All units must pass min/max limits of the datasheet

Highly Accelerated Temperature and Humidity Stress Test

Purpose: This is an equivalent test to Steady State Temperature Humidity Bias Life test with different (higher) temperature stress condition.

Condition: 85%RH at 130C with Vin=Vinmax

Pass Criteria: All units must pass min/max limits of the datasheet

Failure Rate Calculation

The failure rate for a technology is gauged by a Failures-In-Time (FIT) based upon accelerated stress data. The units for FIT are failures per billion device hours.

$$FITRate = \frac{(\chi^2 / 2) * 10^9}{stress * device\ hours}$$

The stress that enables FIT is High Temperature Operating Life (HTOL), which is a product level test. HTOL is accelerated by temperature and by voltage. The total number of failures in stress determines the chi-squared factor (a dimensionless number representing a 60% confidence level of statistics). The number of product units times the stress period (in hours) is the device-hours number. The Arrhenius equation uses the Activation Energy for the failure mode, as well as the stress temperature and the reporting temperature (usually 55C) to compute the HTOL temperature acceleration factor, AF(T). The accelerated stress device-hours is AF(T) times the device-hours number. For voltage stress, the voltage acceleration factor AF(V)= Exp(β(Vtest- Vuse)), Vtest = Stress Voltage (V). Vuse = Nominal Voltage (V). β = Voltage Acceleration Constant depending on a wafer process.

MTBF (Mean Time Between Failure) equals to 1/FIT.