NB681

28V, 6A, Low Iq, High Current Synchronous Buck Converter with 2-Bit VID

The Future of Analog IC Technology

DESCRIPTION

The NB681 is a fully integrated, high-frequency, synchronous, rectified, step-down, switch-mode converter with 2-bit VID, especially designed for IMVP8 applications—VCCIO, PRIMCORE, V1.0A, EDRAM, and EOPIO. It offers a very compact solution to achieve a 6A continuous output current and a 7.5A peak output current over a wide input supply range.

The NB681 operates at high efficiency over a wide output current load range based on MPS proprietary switching loss reduction technology and internal low Ron power MOSFETs.

Adaptive constant-on-time (COT) control mode provides fast transient response and eases loop stabilization. The DC auto-tune loop provides good load and line regulation.

To avoid audible noise, NB681 provides low-power mode for power loss saving during the low-power state and ultrasonic mode.

Full protection features include OC limit, OVP, UVP, and thermal shutdown.

The converter requires a minimal number of external components, and it is available in a QFN 2mm x 3 mm package.

FEATURES

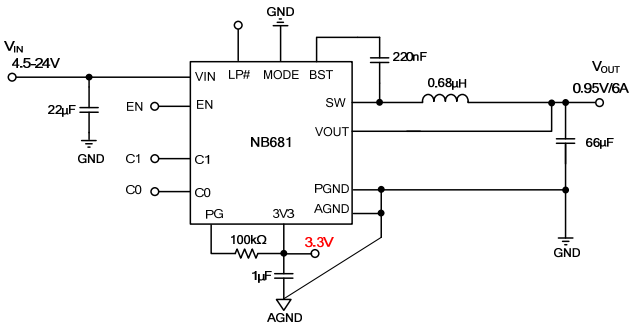
- Wide 4.5V to 28V Operating Input Range
- VCCIO/PRIMCORE/EDRAM/EOPIO/V1.0A Compatible for IMVP8
- Output Adjustable by 2-Bit VID
- Low-Power Mode
- 25μA Low Quiescent Current
- 6A Continous Output Current
- 7.5A Peak Output Current
- Selectable Ultrasonic Mode
- Adaptive COT for Fast Transient
- DC Auto-Tune Loop
- Stable with POSCAP and Ceramic Capacitors
- 1% Reference Voltage
- Internal Soft Start
- Output Discharge
- OCL, OVP, UVP, and Thermal Shutdown,
- Latch-Off Reset via EN or Power Cycle
- QFN 2mm x 3mm Package

APPLICATIONS

- Laptop Computers
- Tablet PCs
- Networking Systems
- Servers
- Personal Video Recorders
- Flat Panel Televisions and Monitors
- Distributed Power Systems

All MPS parts are lead-free, halogen-free, and adhere to the RoHS directive. For MPS green status, please visit the MPS website under Quality Assurance. “MPS” and “The Future of Analog IC Technology” are registered trademarks of Monolithic Power Systems, Inc.

TYPICAL APPLICATION



MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2017 MPS. All Rights Reserved.

ORDERING INFORMATION

Part Number*	Package	Top Marking
NB681GD	QFN-13 (2mm x 3mm)	*See Below*

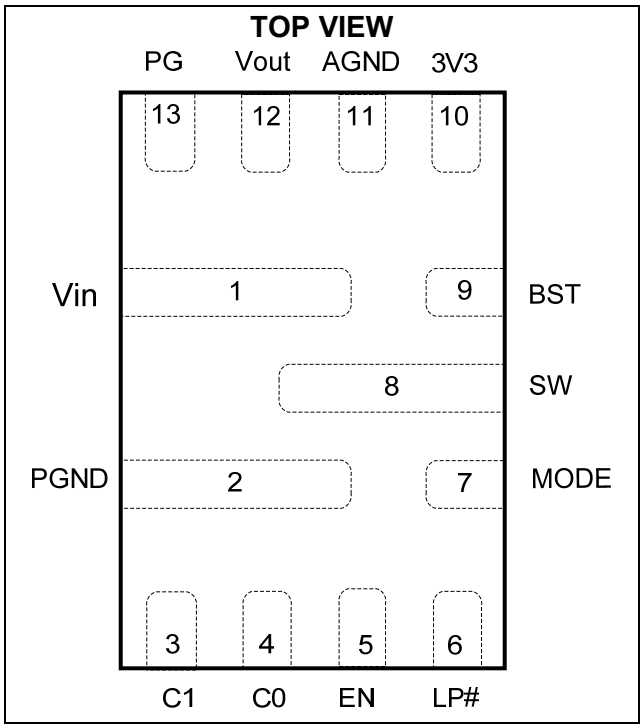
* For Tape & Reel, add suffix –Z (e.g. NB681GD–Z)

TOP MARKING

AKVY
LLL

AKV: Product code of NB681GD
Y: Year code
LLL: Lot number

PACKAGE REFERENCE



MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2017 MPS. All Rights Reserved.

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}) ..... 28 V
V_{SW} (DC).....-1 V to 26 V
V_{SW} (25 ns).....-3.6 V to 28 V
V_{BST} ..... V_{SW} +4.5 V
I_{EN}.....100 µA
All other pins .....-0.3 V to +4.5 V
Continuous power dissipation (T_A = +25°C) (2)
QFN-13 (2mm x 3mm)..... 1.8 W
Junction temperature .....150°C
Lead temperature .....260°C
Storage temperature..... -65°C to +150°C

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) .....4.5 V to 24 V
Supply voltage (V_{CC}) .....3.15 V to 3.5 V
Enable current (I_{EN}).....50 µA
Operating junction temp. (T_J). .. -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

QFN-13 (2mm x 3mm).....	70	15... °C/W

NOTES:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J(MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D(MAX)=(T_J(MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2017 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12 V, 3V3 = 3.3 V, T_J = 25°C, LP# = 1, C1 = 1, C0 = 0, Mode = 0, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Supply current						
3V3 supply current in normal mode	I_{3V3}	V_{EN} = 3.3 V,$V_{LP\#}$ = 3.3 V, V_{OUT} = 1 V		150		µA
3V3 supply current in LP# mode	$I_{3V3\ LP\#}$	V_{EN} = 3.3 V,$V_{LP\#}$ = 0		30		µA
3V3 shutdown current	$I_{3V3\ SDN}$	V_{EN} = 0 V			1	µA
MOSFET						
High-side switch on resistance	HS_{RDS-ON}			36		mΩ
Low-side switch on resistance	LS_{RDS-ON}			13		mΩ
Switch leakage	SW_{LKG}	V_{EN} = 0 V, V_{SW} = 0 V		0	1	µA
Current limit						
Low-side valley current limit	I_{LIMIT_LS}		7	7.6	8.3	A
Switching frequency and minimum off timer						
Switching frequency[5]	F_S	Default		750		kHz
Constant on timer	Ton	V_{IN} = 5 V, V_{OUT} = 1.2 V	250	330	400	ns
Minimum on time[5]	$T_{ON\ Min}$			50		ns
Minimum off time[5]	$T_{OFF\ Min}$			250		ns
Over-voltage and under-voltage protection						
OVP threshold	V_{OVP}	V_{FB}	120%	130%	135%	V_{REF}
UVP-1 threshold	V_{UVP}	V_{FB}	70%	75%	80%	V_{REF}
UVP-1 hold off timer[5]	T_{OC}	V_{OUT} = 60% V_{REF}		64		µs
UVP-2 threshold	V_{UVP}	V_{FB}	45%	50%	55%	V_{REF}
Reference and soft start						
Internal reference voltage	V_{REF}, MODE=0	LP# = 0[5]		0		mV
		LP# = 1, C1 = 0, C0 = 0		850		mV
		LP# = 1, C1 = 0, C0 = 1		875		mV
		LP# = 1, C1 = 1, C0 = 0	940	950	960	mV
		LP# = 1, C1 = 1, C0 = 1		975		mV
	V_{REF}, MODE=Float	LP# = 0		700		mV
		LP# = 1, C1 = 0, C0 = 0		850		mV
		LP# = 1, C1 = 0, C0 = 1		900		mV
		LP# = 1, C1 = 1, C0 = 0		950		mV
		LP# = 1, C1 = 1, C0 = 1		1000		mV
	V_{REF}, MODE=100k	LP# = 0[5]		0		mV
		LP# = 1, C1 = 0, C0 = 0		800		mV
		LP# =1, C1 = 0, C0 = 1		950		mV
		LP# = 1, C1 = 1, C0 = 0	990	1000	1010	mV
		LP# = 1, C1 = 1, C0 = 1		1050		mV

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2017 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12 V, 3V3 = 3.3 V, T_J = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Internal reference voltage	$V_{REF,}$ **MODE=150k**	LP# = 0[5]		0		mV
		LP# = 1, C1 = 0, C0 = 0		1000		mV
		LP# = 1, C1 = 0, C0 = 1		1075		mV
		LP# = 1, C1 = 1, C0 = 0		1150		mV
		LP# = 1, C1 = 1, C0 = 1		1200		mV
Soft-start time	T_{SS}	En to PG up	0.9	1.3	1.5	ms
VID change slew rate	SR_{VID}	MODE = Float or 150 k	5		10	mV/µs
		MODE = 100 k	25		35	mV/µs
		MODE = 0	10		20	mV/µs
VID change timer (EOPIO) [5]	$T_{VID\ EOPIO}$	MODE = 100 k			10	µs
LP# exit timer[5]	$T_{LP\#_exit}$	MODE = Float			45	µs
		MODE = 0/100 k/150 k			240	µs
MODE						
Mode source current	I_{MODE}		9	10	11.6	µA
Enable and UVLO						
EN UVLO rising threshold	$V_{EN\ H\ UVLO}$		1.1	1.2	1.3	V
EN hysteresis	$V_{EN\ HYS}$			100		mV
EN high limit @USM	$V_{EN\ H\ USM}$				1.6	V
EN low limit @Normal[5]	$V_{EN\ L\ Normal}$		2.3			V
Enable input current	I_{EN}	V_{EN} = 3.3 V		5		µA
		V_{EN} = 0 V		0		
VCC under-voltage lockout threshold rising	VCC_{Vth}		2.8	3.0	3.13	V
VCC under-voltage lockout threshold hysteresis	VCC_{HYS}			200		mV
VIN under-voltage lockout threshold rising	VIN_{VTH}			4.2	4.4	V
VIN under-voltage lockout threshold hysteresis	VIN_{HYS}			300		mV
LP# , C1, C0 logic						
Rising threshold	V_{LH}		0.39	0.6	0.79	V
Hysteresis	V_{LHYS}			100		mV
Input current	I_{LIN}	$V_{LP\#,C1,C0}$ = 3.3 V			1	µA
Power good						
PG when Vout risng (good)	$PG_{Rising(GOOD)}$	V_{FB} rising, percentage of V_{REF}		95		%
PG when Vout falling (fault)	$PG_{Falling(Fault)}$	V_{FB} falling, percentage of V_{REF}		90		
PG when Vout rising (fault)	$PG_{Rising(Fault)}$	V_{FB} rising, percentage of V_{REF}		115		
PG when Vout falling (good)	$PG_{Falling(Fault)}$	V_{FB} falling, percentage of V_{REF}		105		

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2017 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12 V, 3V3 = 3.3 V, T_J = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Power good low to high delay	PG_{Td}			5	11	µs
EN low to power good low delay	$PG_{Td\ EN\ low}$				1	µs
PG sink current capability	V_{PG}	Sink 4 mA			0.4	V
Thermal protection						
Thermal shutdown(5)	T_{SD}			145		°C
Thermal shutdown hysteresis(5)	$T_{SD\ HYS}$			25		°C

NOTE:

5) Guaranteed by design.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2017 MPS. All Rights Reserved.

PIN FUNCTIONS

PIN #	Name	Description
1	VIN	**Supply voltage input**. The NB681 operates from a +4.5 V to +24 V input rail. An input capacitor is needed to decouple the input rail. Use wide PCB traces and multiple vias to make the connection with at least two layers for the input trace.
2	PGND	**Power ground**. Use wide PCB traces and multiple vias to make the connection.
3, 4	C1, C0	**2-bit VID control input**. Set C1 and C0 with MODE to get different voltage references for different rails.
5	EN	**Enable.** Drive EN high to turn on the buck regulator; drive EN low to turn off the buck regulator. EN determines USM. If EN is within 1.2 V-1.7 V, it is in USM. If EN >2.3 V, it is in normal mode. For normal mode, it is recommended that EN rising finishes in <1 ms.
6	LP#	**Low-power mode control signal.** Pull LP# high in normal operation. Pull LP# low to enter low-power mode. Usually, LP# is controlled by the SLP#S0 of the system.
7	MODE	**Selection for VCCIO/PRIMCORE/EDRAM/EOPIO/V1.0 A applications with external 1% resistors.**
8	SW	**Switch output.** Connect SW to the inductor and bootstrap capacitor. SW is connected to VIN when the HS-FET is on; SW is connected to PGND when the LS-FET is on. Use wide and short PCB traces to make the connection. SW is noisy, so keep sensitive traces away from SW.
9	BST	**Bootstrap.** A >100 nF capacitor connected between SW and BST is required to form a floating supply across the high-side switch driver.
10	3V3	**External 3V3 VCC input for control and driver**. Place a 1 µF decoupling capacitor close to 3V3 and AGND.
11	AGND	**Signal logic ground.** Make a Kelvin connection to PGND near the VCC capacitor. AGND can be applied as a remote sense ground with proper setting.
12	VOUT	**Output sense input.** Connect the VOUT to the remote output capacitor with good GND decoupling. Keep the VOUT trace away from SW or other noisy nodes. It is recommended to use a >20 mil trace for the vout sense.
13	PG	**Power good output**. PG is an open-drain signal. PG is high if the output voltage is higher than 95 percent of the nominal voltage or lower than 105 percent of the nominal voltage.

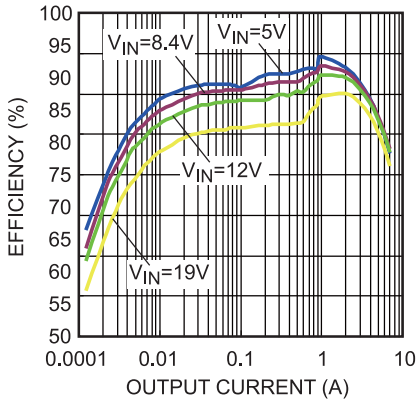
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2017 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS

NB681 V_{IN} = 12 V, V_{OUT} = 1 V, L = 1.0 µH/10 mΩ, R_{mode} = 100 kΩ, LP# = C1 = 1, C0 = 0, R_{bst} = 0, T_J = +25°C, C_{out} = 22 µF*3 unless otherwise noted.

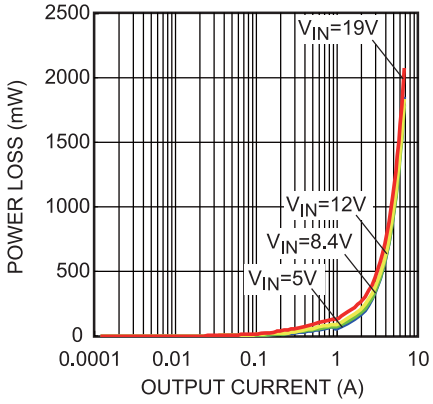
Efficiency vs. Load Current

V_{OUT}=1V



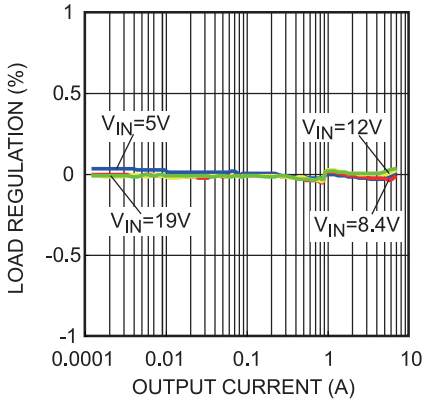
Power Loss

V_{OUT}=1V



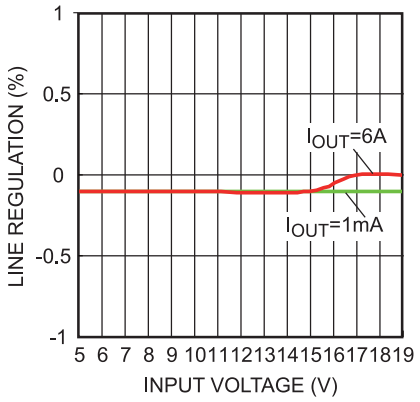
Load Regulation

V_{OUT}=1V



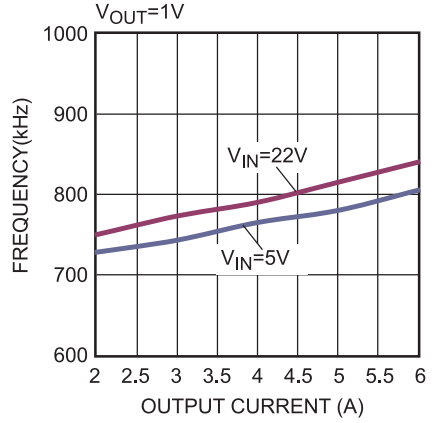
Line Regulation

V_{OUT}=1V



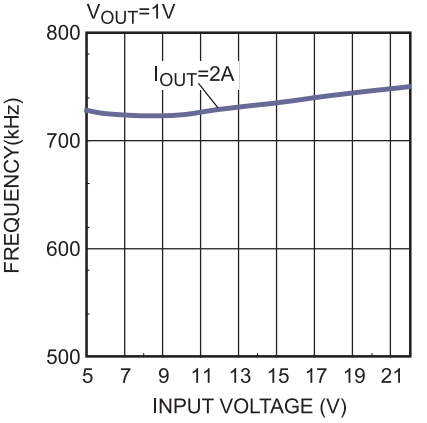
Switch Frequency vs. Output Current

V_{OUT}=1V



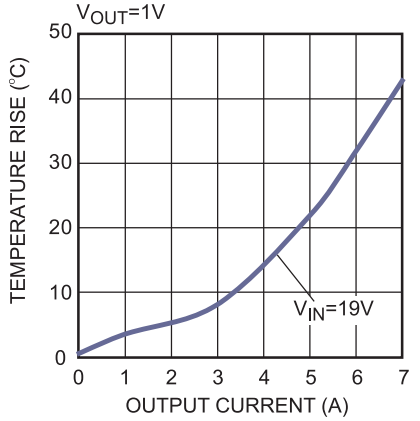
Switch Frequency vs. Input Voltage

V_{OUT}=1V



Temperature Rise vs. Load Current

V_{OUT}=1V

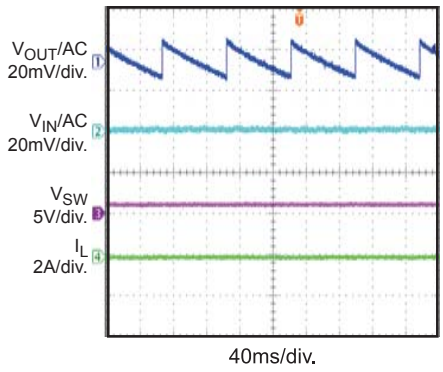


MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2017 MPS. All Rights Reserved.

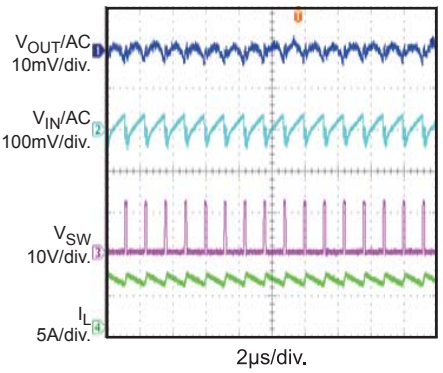
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

NB681 V_{IN} = 12 V, V_{OUT} = 1 V, L = 1.0 µH/10 mΩ, R_{mode} = 100 kΩ, LP# = C1 = 1, C0 = 0, Rbst = 0, T_J = +25°C, Cout = 22 µF*3 unless otherwise noted.

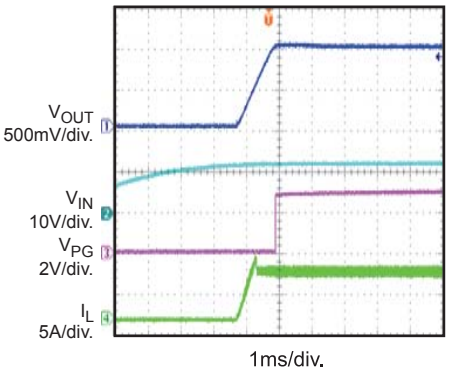
Input/Output Voltage Ripple
I_{OUT} = 0A



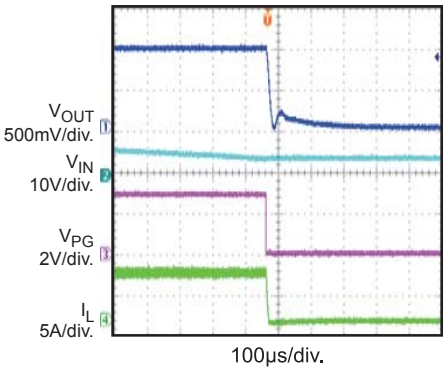
Input/Output Voltage Ripple
I_{OUT} = 6A



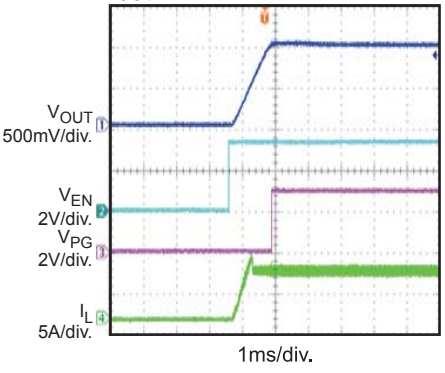
Power Good through V_{IN} Startup
I_{OUT} = 6A



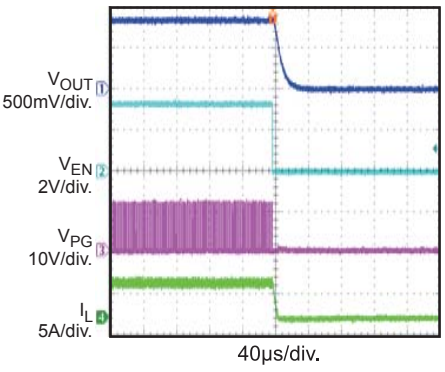
Power Good through V_{IN} Shutdown
I_{OUT} = 6A



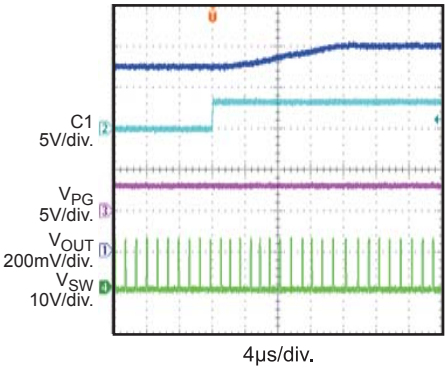
Power Good through EN Startup
I_{OUT} = 6A



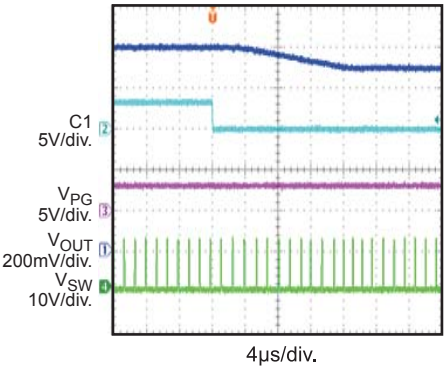
Power Good through EN Shutdown
I_{OUT} = 6A



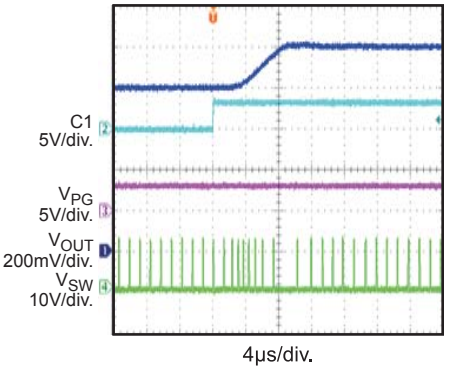
VID Transient
I_{OUT}=1A, C0=1, C1=0 to 1,
R_{MODE}=Float (VCCPRIMCORE)
V_{OUT}=0.9V-1V



VID Transient
I_{OUT}=1A, C0=1, C1=1 to 0,
R_{MODE}=Float (VCCPRIMCORE)
V_{OUT}=1V-0.9V



VID Transient
I_{OUT}=1A, C0=0, C1=0 to 1,
R_{MODE}=100k (EOPIO)
V_{OUT}=0.8V-1V



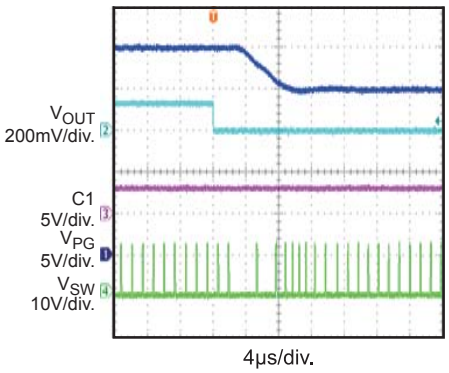
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2017 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

NB681 V_{IN} = 12 V, V_{OUT} = 1 V, L = 1.0 µH/10 mΩ, R_{mode} = 100 kΩ, LP# = C1 = 1, C0 = 0, Rbst = 0, T_J = +25°C, Cout = 22 µF*3 unless otherwise noted.

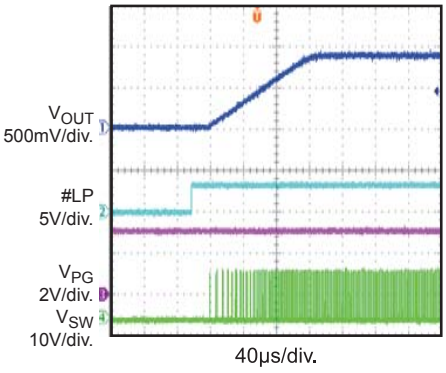
VID Transient

I_{OUT}=1A, C0=0, C1=1 to 0,
R_{MODE}=100k (EOPIO)
V_{OUT}=1V-0.8V



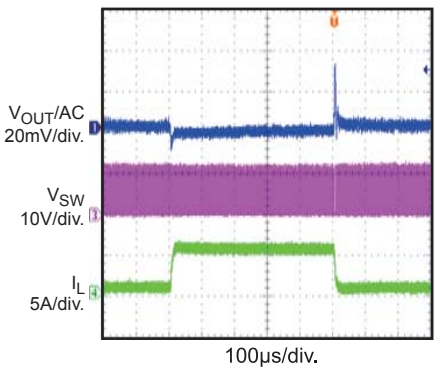
LP# Transient

I_{OUT}=3A, C1=1, C0=1,
LP#=0-1, R_{MODE}=0 (VCCIO)
V_{OUT}=0V-1V



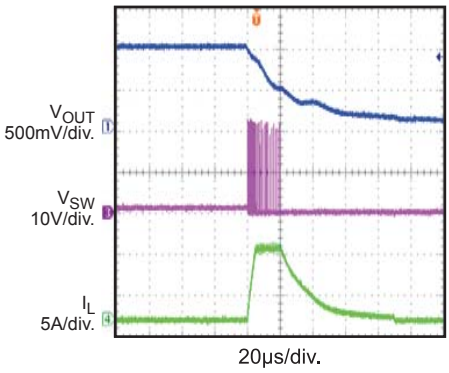
Load Transient

I_{OUT}=0.6A-5.4A @1.6A/µs



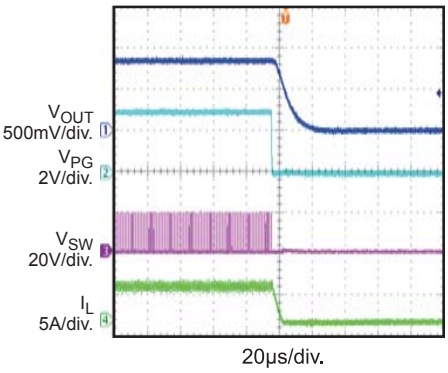
Short-Circuit Protection

V_{IN}=22V



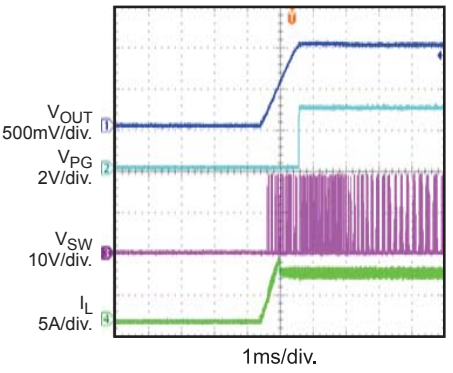
Thermal Shutdown

V_{IN}=19V, I_{OUT}=6A



Thermal Recovery

V_{IN}=19V, I_{OUT}=6A



MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2017 MPS. All Rights Reserved.

FUNCTIONAL BLOCK DIAGRAM

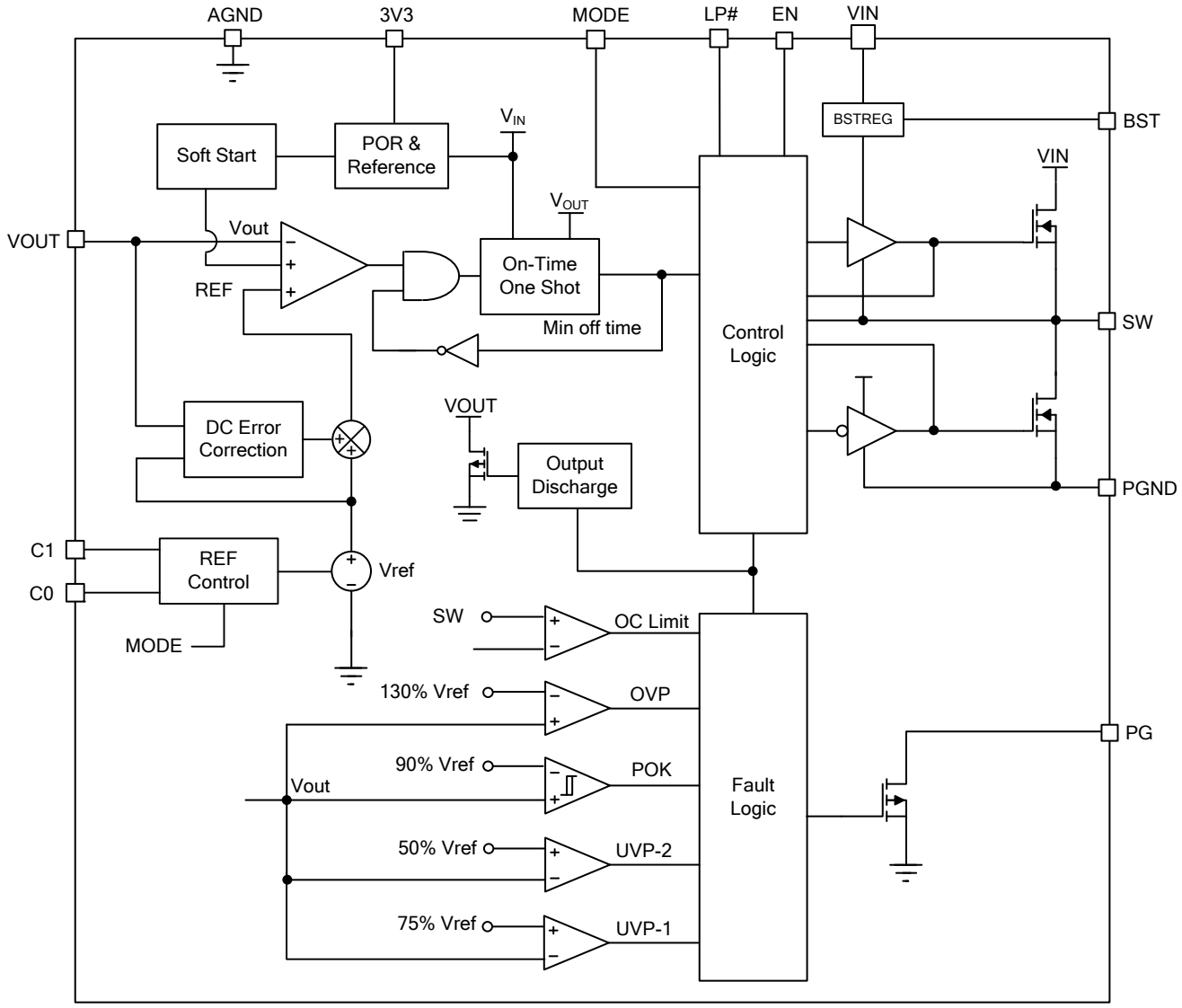


Figure 1—Functional block diagram

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2017 MPS. All Rights Reserved.

OPERATION

PWM Operation

The NB681 is a fully integrated, synchronous, rectified, step-down, switch-mode converter, especially designed for IMVP8 applications—VCCIO, PRIMCORE, EDRAM, EOPIO, and V1.0A. Constant-on-time (COT) control provides fast transient response and eases loop stabilization. At the beginning of each cycle, the high-side MOSFET (HS-FET) is turned on when the feedback voltage (V_{FB}) is below the reference voltage (V_{REF}), which indicates insufficient output voltage. The on period is determined by the output voltage and the input voltage to make the switching frequency fairly constant over the input voltage range.

After the on period elapses, the HS-FET is turned off or enters an off state. It is turned on again when V_{FB} drops below V_{REF}. By repeating operation this way, the converter regulates the output voltage. The integrated low-side MOSFET (LS-FET) is turned on when the HS-FET is in its off state to minimize the conduction loss. There is a dead short between the input and GND if both the HS-FET and the LS-FET are turned on at the same time (shoot-through). In order to avoid shoot-through, a dead time (DT) is generated internally between the HS-FET off and the LS-FET on period or the LS-FET off and the HS-FET on period.

Internal compensation is applied for COT control for stable operation even when ceramic capacitors are used as output capacitors. This internal compensation improves the jitter performance without affecting the line or load regulation.

CCM Operation

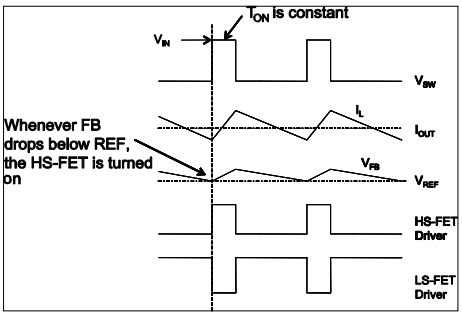


Figure 2—CCM mode operation

Continuous conduction mode (CCM) occurs when the output current is high, and the inductor current is always above zero amps (see Figure 2). When V_{FB} is below V_{REF}, the HS-FET is turned on for a fixed interval. When the HS-FET is turned off, the LS-FET is turned on until the next period.

In CCM operation, the switching frequency is fairly constant (PWM mode).

DCM Operation

When the load decreases, the inductor current will decrease as well. Once the inductor current reaches zero, the part transitions from CCM to discontinuous conduction mode (DCM).

DCM operation is shown in Figure 3. When V_{FB} is below V_{REF}, the HS-FET is turned on for a fixed interval, which is determined by the one-shot on timer. See Equation (1). When the HS-FET is turned off, the LS-FET is turned on until the inductor current reaches zero. In DCM operation, the V_{FB} does not reach V_{REF} when the inductor current approaches zero. The LS-FET driver turns into tri-state (high Z) when the inductor current reaches zero. A current modulator takes over the control of the LS-FET and limits the inductor current to less than -1 mA. Hence, the output capacitors discharge slowly to GND through the LS-FET. As a result, the efficiency at light-load is improved greatly. The HS-FET is not turned on as frequently during a light-load condition as it is during a heavy-load condition (skip mode).

At a light-load or no-load condition, the output drops very slowly, and the NB681 reduces the switching frequency naturally, achieving high efficiency at light load.

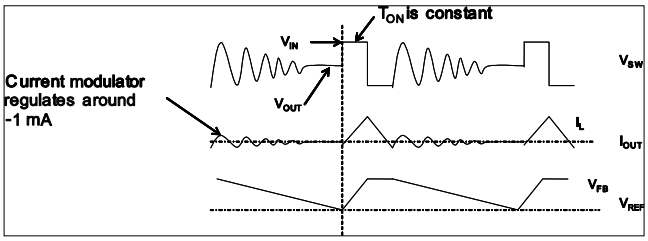


Figure 3—DCM operation

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2017 MPS. All Rights Reserved.

As the output current increases from the light-load condition, the time period within which the current modulator regulates becomes shorter. The HS-FET is turned on more frequently; the switching frequency increases accordingly. The output current reaches the critical level when the current modulator time is zero. The critical level of the output current is determined with Equation (1):

$$I_{OUT} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times L \times F_{SW} \times V_{IN}} \quad (1)$$

The device enters PWM mode once the output current exceeds the critical level. After that, the switching frequency stays fairly constant over the output current range.

DC Auto-Tune Loop

NB681 applies a DC auto-tune loop to balance the DC error between V_{FB} and V_{REF} by adjusting the comparator input REF to make V_{FB} always follow V_{REF}. This loop is quite slow, so it improves the load and line regulation without affecting the transient performance. The relationship between V_{FB},V_{REF}, and REF is shown in Figure 4.

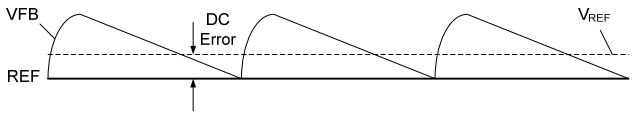


Figure 4—DC auto-tune loop operation

VCCIO/PRIMCORE/EDRAM/EOPIO/V1.0A MODE Select

NB681 combines mode selection to support different rails in IMVP8 including VCCIO, PRIMCORE, EDRAM, EOPIO, and V1.0A. These rails have different (normal) VID and different voltages in LPM, VID slew rate, and other features. By selecting a different resistor from MODE to GND, NB681 can be applied in different rails with proper features. Table 1 shows resistor settings on MODE to enter different rails.

Table 1—MODE selection for different rails

MODE	VR Rail	Resistor to GND (1% accuracy)
M1	VCCIO	0
M2	PRIMCORE	Float or > 230 K
M3	EDRAM/V1.0A/EOPIO	100 K
M4	Others	150 K

Low-Power Mode

To minmize power loss at light-load, NB681 enters low-power mode once LP# is set to low. NB681 is allowed to decay to the LPM target value with the assertion of LP#. When the VR enters LPM, it behaves in the following manner:

- PG remains high to all power good logic;
- VR stops switching;
- The output decays into the load (discharge circuitry is off) and decays to 0 V.

Once LP# changes from 0 V→1 V, NB681 exits LPM by ramping up Vout (with a proper delay and slew rate) to make sure the output is ready in 240 µs, including the delay time (Tdelay). The operation timing and slew rate of the LP# and Vout is shown in Figure 5.

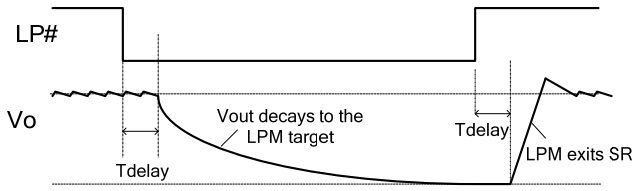


Figure 5—LPM voltage transition and timing

The LPM target value, slew rate, and PG state for different rails are listed in Table 2.

Table 2—Intel LPM specification for each rail

	PRIMCORE	VCCIO	EDRAM/ EOPIO	OTHER
LPM target(V)	0.7	0	0	0
LPM enter	Decay	Decay	Decay	Decay
LPM exit timer(µs)	45	240	240	240
PG during LPM	High	High	High	High

Control Bit Definitions (LP#, VID)

The control bit definitions including LP# and VIDx for different rails are shown in Table 3.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2017 MPS. All Rights Reserved.

Table 3—Control bit logics

	LP#	C1	C0	VOUT(V)
VCCIO	0	X	X	0
	1	0	0	0.85
	1	0	1	0.875
	1	1	0	0.95
	1	1	1	0.975
VCCPRIM _CORE	0	X	X	0.7
	1	0	0	0.85
	1	0	1	0.9
	1	1	0	0.95
	1	1	1	1.00
EDRAM/ EOPIO/ V1.0A	0	X	X	0
	1	0	0	0.8 (MSM)
	1	0	1	0.95
	1	1	0	1
	1	1	1	1.05
Others	0	X	X	0
	1	0	0	1.0
	1	0	1	1.075
	1	1	0	1.15
	1	1	1	1.2

Configuring the EN Control

EN is used to enable or disable the whole chip. Pull EN high to turn on the regulator and pull EN low to turn off the regulator. It is recommended to have EN rise from 0 V to over 2.3 V in less than 1 ms.

EN works with the LP# signal to control the output (see Table 4).

Table 4—EN/LP# control

EN	LP#	Output	PG
0	0	0 V, Off	Low
0	1	0 V, Off	Low
1	0	Normal turn on and fall to LP# target value after PG + 1 ms	Asserted when output reaches nominal voltage and remains high during LP# = 0
1	1	High	Remains asserted after SS

Soft Start (SS)

The NB681 employs a soft-start (SS) mechanism to ensure smooth output during power-up. When EN goes high, the internal reference voltage ramps up gradually; hence, the output voltage ramps up smoothly as well. Once the reference voltage reaches the target value, the soft start finishes, and the part enters steady-state operation.

If the output is pre-biased to a certain voltage during start-up, the IC disables the switching of both the high-side and low-side switches until the voltage on the internal reference exceeds the sensed output voltage at the internal FB node.

Power Good (PG)

The NB681 has power good (PG) output used to indicate whether the output voltage of the buck regulator is ready. PG is an open drain of a MOSFET. It should be connected to 3V3 or another voltage source through a resistor (e.g. 100 k). After the input voltage is applied, the MOSFET is turned on so that PG is pulled to GND before SS is ready. After the FB voltage reaches 95 percent of V_{REF}, PG is pulled high in less than 10 µs. When the FB voltage drops to 90 percent of V_{REF} (or rises higher than 115 percent of V_{REF}), PG is pulled low.

Note that when LP# goes from 1→0, PG stays high for all the power good logic.

Start-Up and Shutdown Sequence

Figure 6 shows the start-up and shutdown sequence including LP# and PG. To achieve a proper start up, it is recommended to turn on EN after VIN and VCC pass UVLO. During start-up, PG goes high immediately when Vout reaches its normal range. LP# mode is blanked until PG + 1 ms, meaning the NB681 is not able to enter LP# mode during the start-up period + 1 ms. Vout decays to the target LPM setting when LP# pulls low and is able to ramp up to its normal value in the Intel required timing. PG pulls low immediately after EN goes low.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2017 MPS. All Rights Reserved.

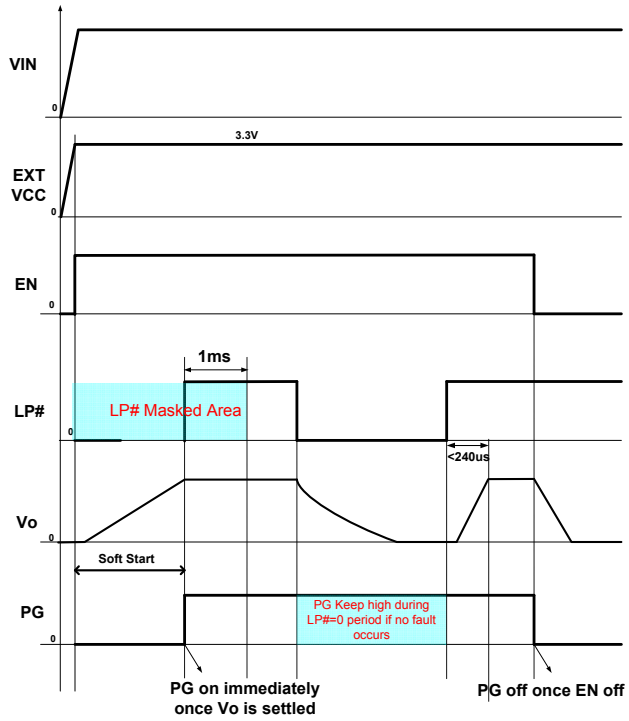


Figure 6—Power sequence and EN/PG logic

Ultrasonic Mode (USM)

Ultrasonic (USM) keeps the switching frequency above an audible frequency area during light-load or no-load conditions. Once the part detects both the HS-FET and the LS-FET are off (for about 32 µs), it forces PWM to initiate Ton, so the switching frequency will be out of audio range. To avoid Vout becoming too high, it shrinks Ton to control the Vout. If the part's FB is still too high after shrinking Ton to its minimum value, the output discharge function is activated, keeping Vout within a reasonable range. USM is selected by the voltage threshold on EN (see Table 5). To enter USM, set EN with two resistors as a divider (e.g., two 100 kΩ resistors) from 3.3 V logic to get 1.65 V.

Table—5 USM selection

Mode	Voltage on EN
USM	1.3 V < EN < 1.7 V
Normal operation	2.3 V < EN < 3.5 V

Over-Current Protection (OCP)

NB681 has cycle-by-cycle over current limiting control. The current-limit circuit employs a "valley" current-sensing algorithm. The part uses the Rds(on) of the LS-FET as a current-sensing element. If the magnitude of the current is above the current-limit threshold, the PWM is not allowed to initiate a new cycle even if FB is lower than REF. Figure 7 shows the detailed operation of the valley current limit.

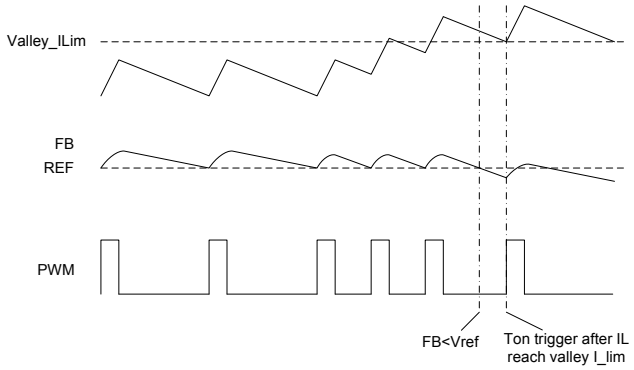


Figure 7—Valley current-limit operation

Since the comparison is done during the LS-FET on state, the OC trip level sets the valley level of the inductor current. The maximum load current at the over-current threshold (Ioc) can be calculated using Equation (2):

$$I_{OC} = I_limit + \frac{\Delta I_{inductor}}{2} \quad (2)$$

The OCL limits the inductor current and does not latch off. In an over-current condition, the current to the load exceeds the current to the output capacitor; thus the output voltage tends to fall off. Eventually, it ends up crossing the under-voltage protection (UVP) threshold and latches off. Fault latching can be re-set by EN going low or the power-cycling of VIN.

Over/Under-Voltage Protection (OVP/UVP)

NB681 monitors the output voltage to detect over and under voltage. When the feedback voltage becomes higher than 130 percent of the target voltage, the OVP comparator output goes high, and the circuit latches as the HS-FET driver turns off, and the LS-FET driver turns on, acting as a -2 A current source.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2017 MPS. All Rights Reserved.

To protect the part from damage, there is an absolute 3.6 V OVP on VOUT. Once Vout reaches this value, it latches off. The LS-FET behaves the same as at 130 percent OVP. This OVP is active even in LP# mode.

When the feedback voltage becomes lower than 75 percent of Vref, the UVP-1 comparator output goes high, and the part latches if the FB voltage stays in this range for about 64 µs (latching the HS-FET off and LS-FET on). The LS-FET remains on until the inductor current hits zero. During this period, the valley current limit helps control the inductor current.
When the feedback voltage drops below 50 percent of the Vref, the UVP-2 comparator output goes high, and the part latches off directly after the comparator and logic delay (latching the HS-FET off and the LS-FET on). The LS-FET remains on until the inductor current hits zero. Fault latching can be reset by EN going low or the power cycling of VIN or VCC.

UVLO Protection

The NB681 has two kinds of under-voltage lock-out protection: a 3 V VCC UVLO and a 4.2 V Vin UVLO. The part starts up only when both the VCC and Vin exceed their own UVLO. The part shuts down when either the VCC voltage is lower than the UVLO falling threshold voltage (2.8 V, typically), or the VIN is lower than the 3.9 V Vin falling threshold. Both UVLO protections are non-latch off.

Thermal Shutdown

Thermal shutdown is employed in the NB681. The junction temperature of the IC is monitored internally. If the junction temperature exceeds the threshold value (145ºC, typically), the converter shuts off. This is a non-latch protection. There is about 25ºC hysteresis. Once the junction temperature drops to about 120ºC, it initiates a SS.

Output Discharge

NB681 discharges the output when EN is low, or the controller is turned off by the protection functions UVP, OVP, UVLO, and thermal shutdown. The part discharges outputs using an internal MOSFET.

Remote Sense

For NB681 (where the remote sense is required), AGND acts as Remote Sen-, which is connected to the remote ground of the output capacitors. VOUT acts as Remote Sen+. The VCC capacitor connected between 3V3 and AGND is still required and should be placed very close to the IC. For additional details please see Figure 9 for the SCH with remote sense connection or refer to AN086 for remote sense details.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2017 MPS. All Rights Reserved.

APPLICATION INFORMATION

Input Capacitor

The input current to the step-down converter is discontinuous, and therefore requires a capacitor to supply the AC current to the step-down converter while maintaining the DC input voltage. Ceramic capacitors are recommended for best performance and should be placed as close to the V_{IN} pin as possible. Capacitors with X5R and X7R ceramic dielectrics are recommended because they are fairly stable with temperature fluctuations.

The capacitors must have a ripple current rating greater than the maximum input ripple current of the converter. The input ripple current can be estimated using Equation (3) and Equation (4):

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (3)$$

The worst-case condition occurs at V_{IN} = 2 V_{OUT}, where:

$$I_{CIN} = \frac{I_{OUT}}{2} \quad (4)$$

For simplification, choose the input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor value determines the input voltage ripple of the converter. If there is an input voltage ripple requirement in the system, choose the input capacitor that meets the specification.

The input voltage ripple can be estimated using Equation (5) and Equation (6):

$$\Delta V_{IN} = \frac{I_{OUT}}{F_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (5)$$

The worst-case condition occurs at V_{IN} = 2V_{OUT}, where:

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{F_{SW} \times C_{IN}} \quad (6)$$

Output Capacitor

An output capacitor is required to maintain the DC output voltage. Ceramic or POSCAP capacitors are recommended. The output voltage ripple can be estimated with Equation (7):

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times F_{SW} \times C_{OUT}}) \quad (7)$$

When using ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is caused mainly by the capacitance. For simplification, the output voltage ripple can be estimated by Equation (8):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times F_{SW}^{2} \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (8)$$

When using POSCAP capacitors, the ESR dominates the impedance at the switching frequency. The output ripple can be approximated with Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (9)$$

The maximum output capacitor limitation should be considered in design application. For a small soft-start time period (if the output capacitor value is too high), the output voltage cannot reach the design value during the soft-start time, causing it to fail to regulate. The maximum output capacitor value (C_{o_max}) can be limited approximately using Equation (10):

$$C_{O_MAX} = (I_{LIM_AVG} - I_{OUT}) \times T_{ss} / V_{OUT} \quad (10)$$

Where I_{LIM_AVG} is the average start-up current during the soft-start period (it can be equivalent to current limit value), and T_{ss} is the soft-start time.

Inductor

The inductor is necessary to supply constant current to the output load while being driven by the switched input voltage. A larger value inductor results in less ripple current, resulting in a lower output ripple voltage. However, a larger value inductor will have a larger physical footprint, a higher series resistance, and/or a lower saturation current. A good rule for determining the inductance value is to design the peak-to-peak ripple current in the inductor to be in the range of 30 percent to 50 percent of the maximum output current with the peak inductor current below the maximum switch current limit. The inductance value can be calculated by Equation (11):

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2017 MPS. All Rights Reserved.

$$L = \frac{V_{OUT}}{F_{SW} \times \Delta I_L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (11)$$

Where ΔI_L is the peak-to-peak inductor ripple current.

The inductor should not saturate under the maximum inductor peak current (including short current), so it is suggested to choose Isat >7.5 A.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2017 MPS. All Rights Reserved.

PCB LAYOUT GUIDELINES

Efficient PCB layout is critical for the performance of the IC. For best results, refer to Figure 8 and follow the guidelines below. For more information, refer to **AN087**.

1. Place the high-current paths (PGND, IN, and SW) very close to the device with short, direct, and wide traces. **A PGND trace under the IC is the number one priority.**
2. Place the input capacitors as close to IN and GND as possible on the same layer as the IC.
3. Place the decoupling capacitor as close to VCC and GND as possible. Keep the switching node (SW) short and away from the feedback network.
4. Keep the BST voltage path as short as possible with a > 50 mil trace.
5. Keep the IN and GND pads connected with a large copper plane to achieve better thermal performance. Add several vias with 10 mil drill/18 mil copper width close to the IN and GND pads to help thermal dissipation.
6. A 4-layer layout is recommended to achieve better thermal performance.
7. Use a >20 mil trace for the Vout sense for output discharge.

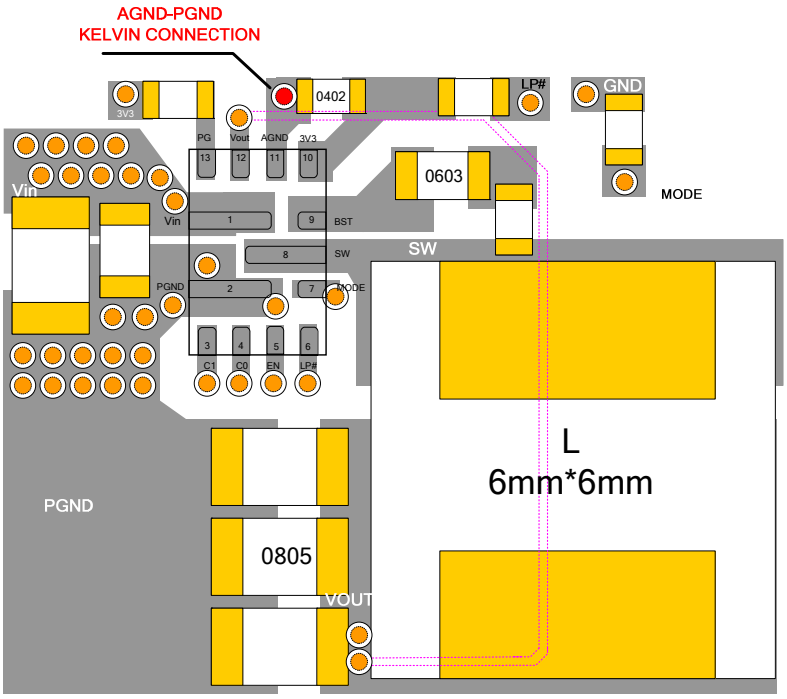


Figure 8—Recommended PCB layout

Recommend Design Example

Design examples are provided in Table 6.1 when ceramic capacitors are applied.

There is a resistor from the external 3.3 V power supply to 3V3 acting as the ripple noise filter of the 3.3 V power supply. It is recommend to have a resistor value from 0 Ω- 5.1Ω depending on the noise level. A 0402 size resistor will suffice if the 3.3 V voltage rises with SS > 100 µs. Otherwise, a larger size (e.g., 0603/0805) resistor is needed.

Table 6.1—Design example for different rails

V_{OUT} (V)	R_{Mode} (Ω)	Cout (F)	L (µH)
VCCIO	0	22 µ x 3	0.68~1
PRIMCORE	Float	22 µ x 3	0.68~1
EDRAM/ EOPIO/ V1.0A	100 K	22 µ x 3	0.68~1
Other	150 K	22 µ x 3	0.68~1

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2017 MPS. All Rights Reserved.

TYPICAL APPLICATION—FOR DIFFERENT RAILS

VCCIO

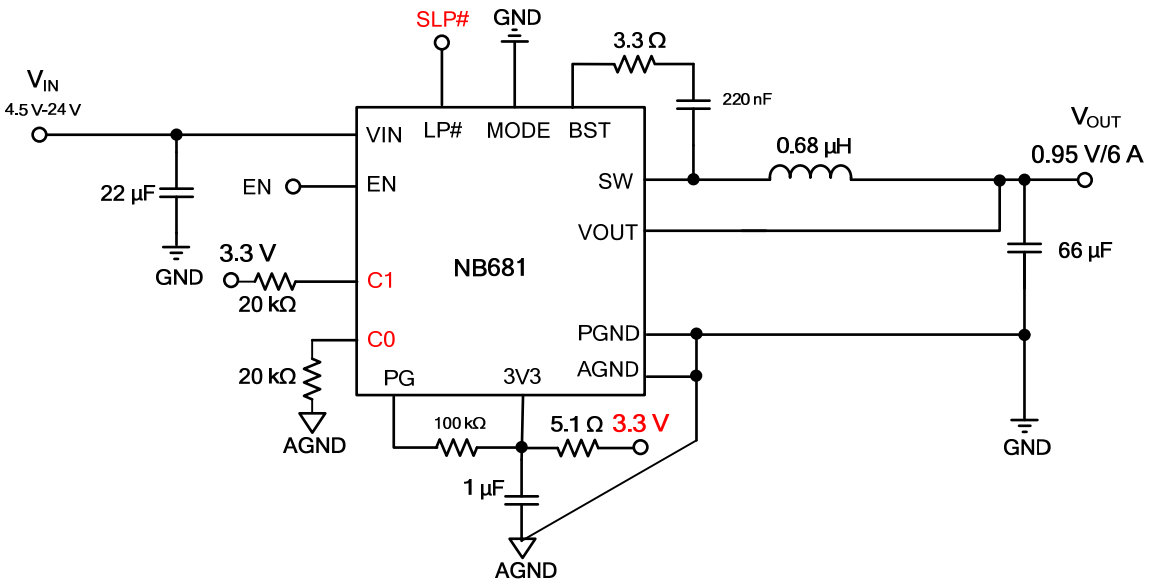


Figure 8.1— Typical application schematic for VCCIO, default 0.95 V (C1 and C0 can be pulled high or low directly without a resistor if Vout is fixed)

PRIMCORE

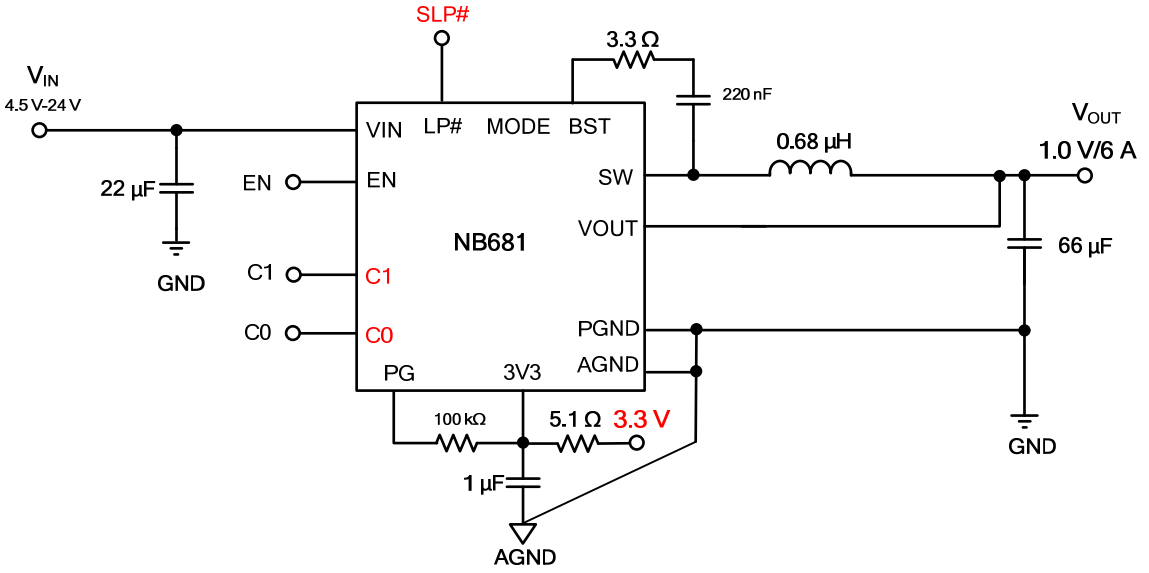


Figure 8.2— Typical application schematic for PRIMCORE, Vout adjusted by VID

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2017 MPS. All Rights Reserved.

TYPICAL APPLICATION—FOR DIFFERENT RAILS

EDRAM & V1.0A

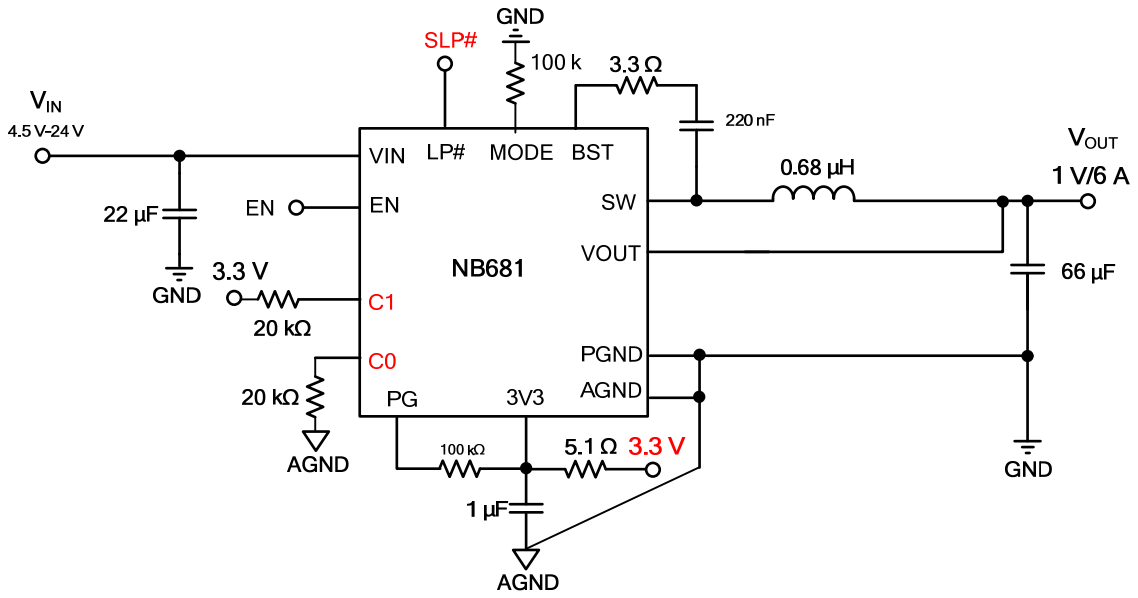


Figure 8.3— Typical application schematic for EDRAM and V1.0A, default 1 V, (C1 and C0 can be pulled high or low directly without a resistor if Vout is fixed)

EOPIO

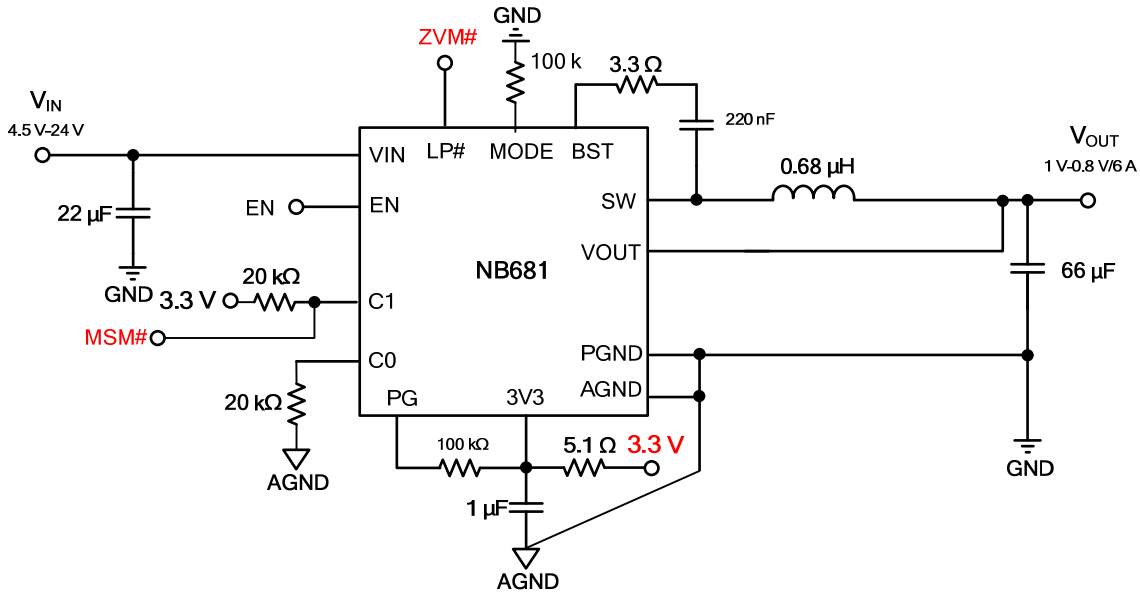
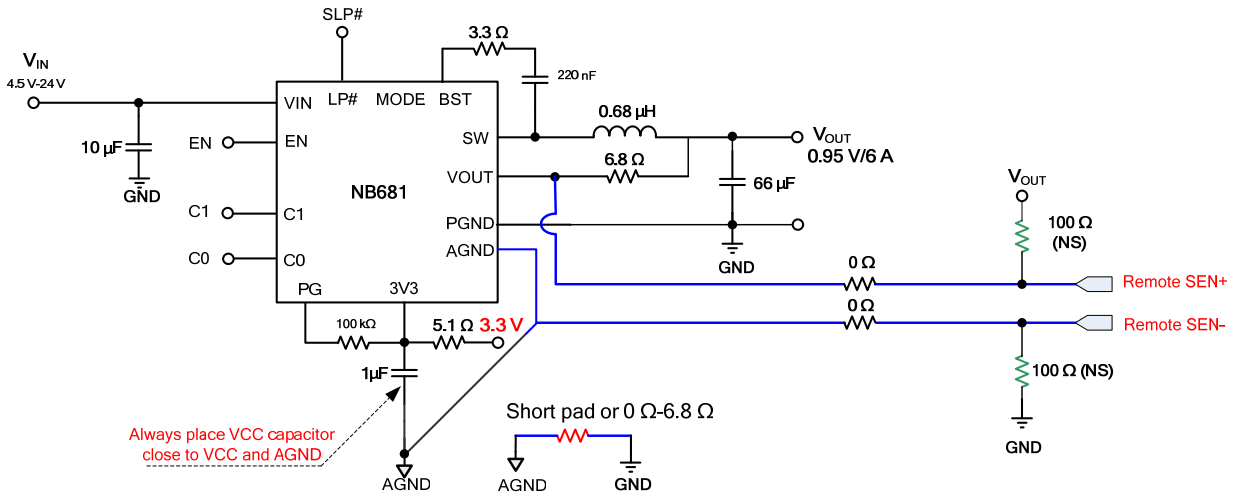


Figure 8.4— Typical application schematic for EOPIO

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2017 MPS. All Rights Reserved.

TYPICAL APPLICATION—WITH REMOTE SENSE

For more details on remote sense application, refer to AN086.

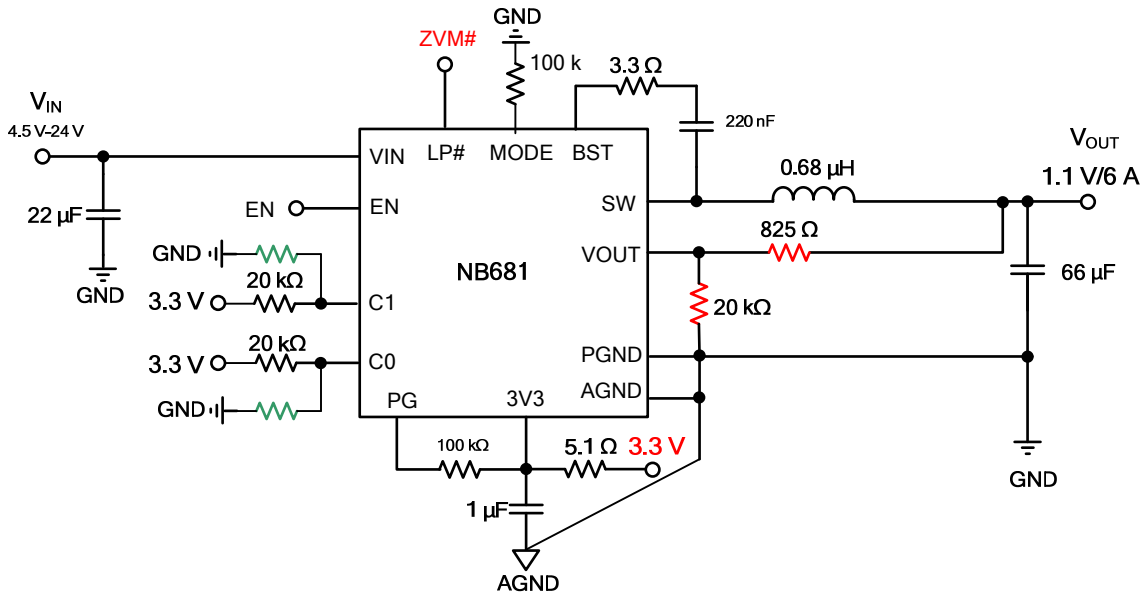


NOTE1: Ultrasonic mode is not effective if applied in this SCH, make sure EN rising finishes in 1 ms

Figure 9—Typical application schematic for NB681 remote sense application

TYPICAL APPLICATION—WITH VOUT OUT OF VID TABLE

The two red resistors on the Vout pin act as feedback resistors to adjust the Vout to the proper value. It is recommended to choose the closest VID value (which is lower than the target Vout) as Vref if there are no other limitations. Figure 10 shows the typical SCH with the Vout setting at 1.1 V.



NOTE 2: Ultrasonic mode is not effective if applied in this SCH, make sure EN rising finishes in 1 ms.

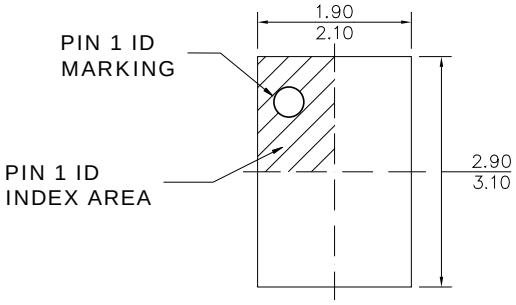
NOTE 3: It is not recommended to set Vout over 50 percent of the target Vref.

Figure 10—Typical application schematic for NB681 with Vout out of the VID Table

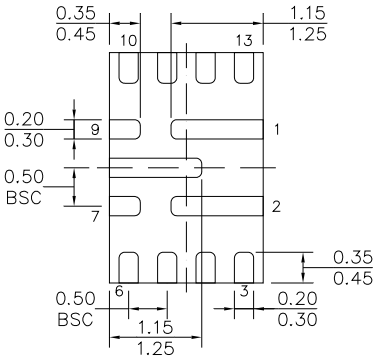
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2017 MPS. All Rights Reserved.

PACKAGE INFORMATION

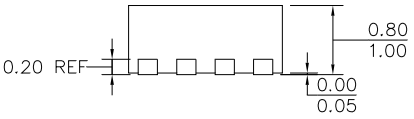
QFN-13 (2mm x 3mm)



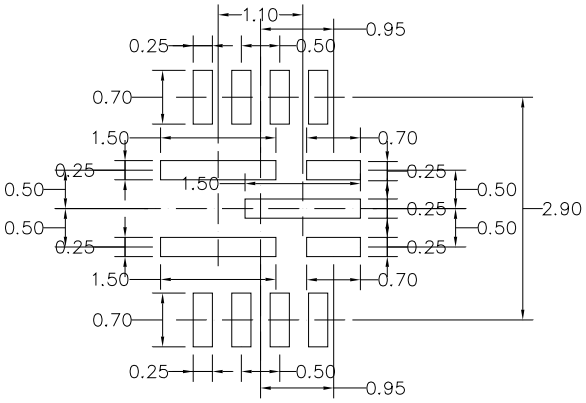
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

NOTICE: The information in this document is subject to change without notice. Users should warrant and guarantee that third party Intellectual Property rights are not infringed upon when integrating MPS products into any application. MPS will not assume any legal responsibility for any said applications.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2017 MPS. All Rights Reserved.