MPQ86970

50A, Monolithic Half-Bridge Intelli-Phase™ Solution in TLGA-41 (5mmx6mm) Package, AEC-Q100

DESCRIPTION

The MPQ86970 is a monolithic half-bridge Intelli-Phase™ DrMOS solution with built-in internal power MOSFETs and gate drivers. It can achieve up to 50A of continuous output current (I_{OUT}) across a wide input voltage (V_{IN}) range.

The integrated MOSFETs and drivers achieve high efficiency through an optimized dead time (DT) and reduced parasitic inductance.

This device is compatible with tri-state output controllers. It also includes a general-purpose current sensing and temperature sensing.

The MPQ86970 is ideal for autonomous driving applications where efficiency and compact size are at a premium. It is available in a TLGA-41 (5mmx6mm) package.

FEATURES

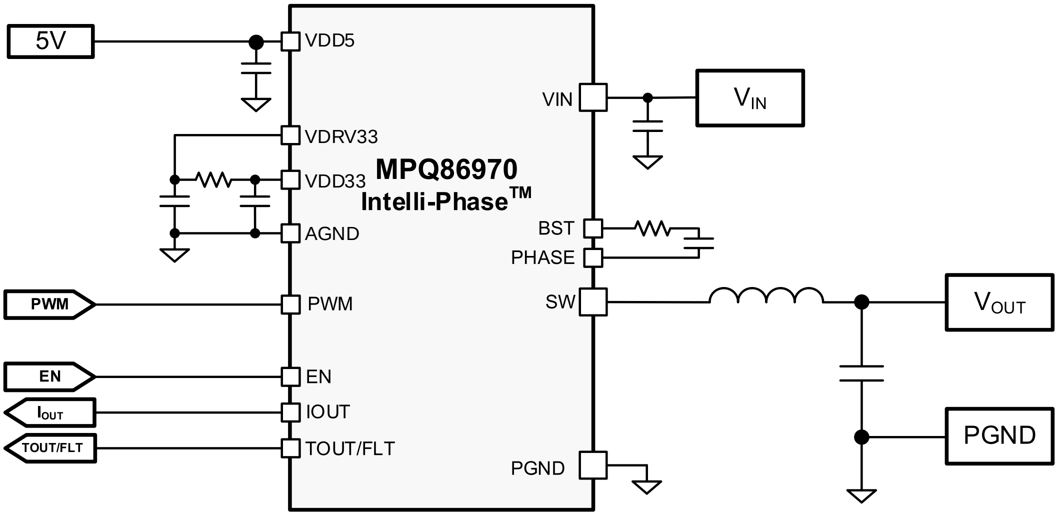
- Wide Operating Input Voltage (V_{IN}) Range
- 50A Output Current (I_{OUT})
- Accepts Tri-State Pulse-Width Modulation (PWM) Signal
- Built-In Switch for Bootstrap (BST) Charging
- Accu-Sense™ Current Sense
- Temperature Sense
- Current-Limit Protection with Fault Flag
- Over-Temperature Protection (OTP) with Fault Flag
- Catastrophic Protection with Fault Flag
- Designed for Multi-Phase Operation
- Available in an TLGA-41 (5mmx6mm) Package
- Available in AEC-Q100 Grade 1

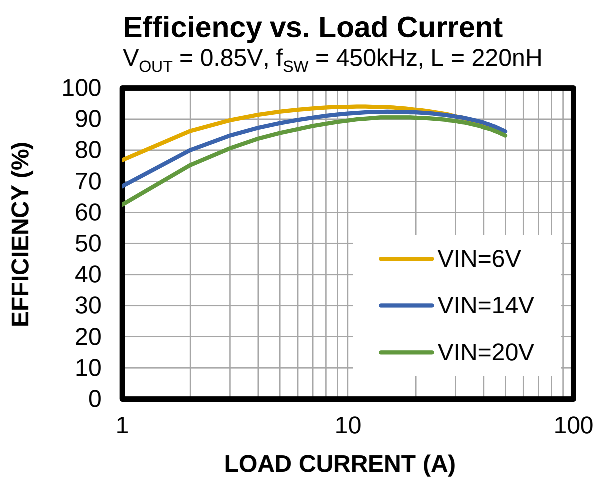
MPSafe™ QM — Developed for Functional Safety Applications: ISO 26262 Compliant

APPLICATIONS

- Autonomous Driving Systems-on-Chip (SoCs)
- Infotainment Systems

TYPICAL APPLICATION





ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MPQ86970GMJT-AEC1	TLGA-41 (5mmx6mm)	*See Below*	3

* For Tape & Reel, add suffix -Z (e.g. MPQ86970GMJT-AEC1-Z).

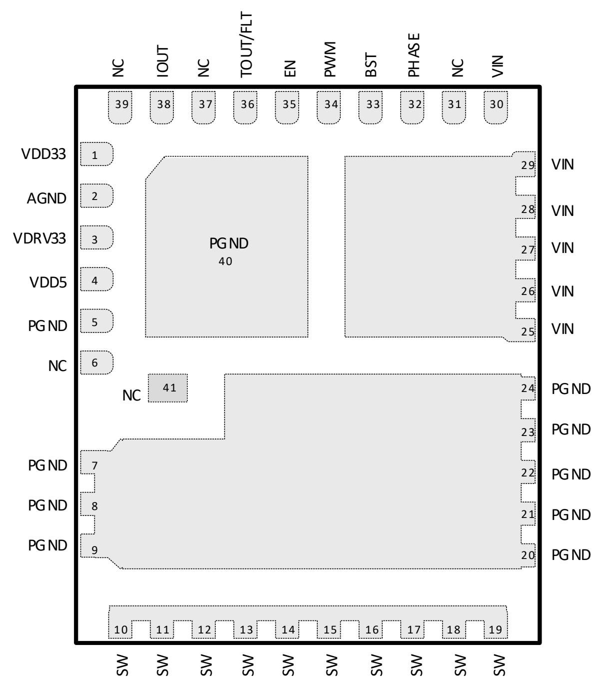
TOP MARKING

MPSYYWW
MP86970
LLLLLLL
T

MPS: MPS prefix
YY: Year code
WW: Week code
MP86970: Part number
LLLLLLL: Lot number
T: Thin package

PACKAGE REFERENCE

TOP VIEW



TLGA-41 (5mmx6mm)

PIN FUNCTIONS

Pin #	Name	Description
1	VDD33	**3.3V power supply for internal logic.** Connect the VDD33 pin to the VDRV33 pin through a 2.2Ω resistor. Decouple the VDD33 pin with a 1µF capacitor connected to AGND. Connect AGND and PGND at the VDD33 capacitor.
2	AGND	**Analog ground.**
3	VDRV33	**Internal LDO output for driver voltage.** Decouple the VDRV33 pin with a 1µF to 4.7µF ceramic capacitor.
4	VDD5	**5V power supply.** Connect the VDD5 pin to a 5V supply and decouple this pin with a 1µF to 4.7µF ceramic capacitor.
5, 7, 8, 9, 20, 21, 22, 23, 24, 40	PGND	**Power ground.**
6, 31, 37, 39, 41	NC	**No connection.**
10, 11, 12, 13, 14, 15, 16, 17, 18, 19	SW	**Phase node.**
25, 26, 27, 28, 29, 30	VIN	**Input supply voltage.** Place the input ceramic capacitor (C_{IN}) close to the device to support the switching current and minimize parasitic inductance.
32	PHASE	**Switch node for bootstrap capacitor connection.** The PHASE pin is internally connected to the SW pin.
33	BST	**Bootstrap.** The BST pin requires a 0.1µF to 0.47µF capacitor (C_{BST}) to drive the power MOSFET's gate above the supply voltage. Connect C_{BST} between the BST and PHASE pins to form a floating supply across the power MOSFET driver.
34	PWM	**Pulse width modulation input.** Float the PWM pin or drive PWM to a middle state to force SW into a high-impedance (Hi-Z) state.
35	EN	**Enable.** Pull the EN pin high to enable the device; pull EN low to disable it and force SW into a Hi-Z state.
36	TOUT/ FLT	**Single-pin temperature sense and fault reporting.** If a fault occurs, the TOUT/FLT pin is pulled up to the VDD33 pin's voltage (V_{DD33}).
38	IOUT	**Current-sense (CS) output.** Connect an external resistor to the IOUT pin to adjust the IOUT voltage (V_{IOUT}), which is proportional to the inductor current (I_L).

ABSOLUTE MAXIMUM RATINGS [1]

Input supply voltage (V_{IN}) (DC) 26V
V_{IN} (25ns) ....-3V to +28V
V_{SW}, V_{PHASE} (DC) ....-0.3V to +24V
V_{SW}, V_{PHASE} (25ns) ....-3V to +28V
V_{BST} (DC) .... V_{SW} + 4V
V_{BST} to V_{SW} (25ns) [2] 5V
V_{DD5} ....-0.3V to +6.5V
V_{DD33}, V_{DRV33} ....-0.3V to +4V
AGND, PGND ....-0.3V to +0.3V
Instantaneous current ($I_{INSTANTANEOUS}$) (20ms)…
………………………………………………… 65A
$I_{INSTANTANEOUS}$ (10µs) 100A
All other pins ....-0.3V to +4V
Junction temperature (T_J) ....150°C
Lead temperature ....260°C
Storage temperature .... -65°C to +150°C

ESD Ratings [3]

Human body model (HBM) ....Class 2
Charged-device model (CDM) .... Class C2b

Recommended Operating Conditions [4]

Input supply voltage (V_{IN})....................3V to 22V
VDD5 supply voltage (V_{DD5})............4.5V to 5.5V
VDRV33 supply voltage (V_{DRV33})........3V to 3.6V
Logic voltage (V_{DD33}) ....3V to 3.6V
Operating junction temp (T_J).... -40°C to +150°C

Thermal Resistance [5] θ_{JB} θ_{JC_TOP}

TLGA-41 (5mmx6mm) ……....1.8…..9.1…°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) For the AMR of a shorter pulse (<25ns), contact an MPS FAE for the related application note (AN164, “BST-SW Short Pulse Capability”).
3) Followed ANSI/ESDA/JEDEC JS-001 for HBM and ANSI/ESDA/JEDEC JS-002 for CDM.
4) The device is not guaranteed to function outside of its operating conditions.
5) Measured on a JESD51-7, 4-layer PCB.