MPQ86760

45A, Intelli-Phase™ Solution in TQFN-21 (4mmx5mm) Package, AEC-Q100 Qualified

DESCRIPTION

The MPQ86760 is a monolithic half-bridge with built-in internal power MOSFETs and gate drivers. It can achieve up to 45A of continuous output current (I_{OUT}) across a wide input voltage (V_{IN}) range.

The integrated MOSFETs and drivers achieve high efficiency through an optimized dead time (DT) and reduced parasitic inductance.

This device is compatible with tri-state output controllers. It also includes general-purpose current sensing and temperature sensing.

The MPQ86760 is ideal for autonomous driving applications where efficiency and compact size are at a premium. It is available in a TQFN-21 (4mmx5mm) package.

FEATURES

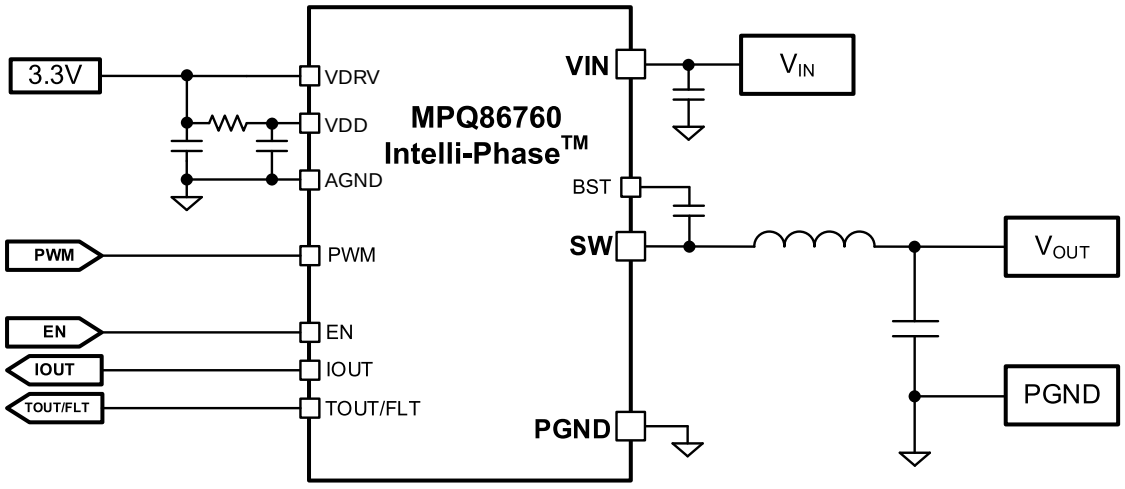
- Wide Operating Input Voltage (V_{IN}) Range
- 45A Output Current (I_{OUT})
- Accepts Tri-State Pulse-Width Modulation (PWM) Signal
- Built-In Switch for Bootstrap (BST)
- Accu-Sense™ Current Sense
- Temperature Sense
- Current-Limit Protection
- Over-Temperature Protection (OTP)
- Used for Multi-Phase Operation
- Available in a TQFN-21 (4mmx5mm) Package
- Available in AEC-Q100 Grade 1
- Developed for Functional Safety Applications: ISO 26262 Compliant

APPLICATIONS

- Autonomous Driving System-on-Chips (SoCs)
- Infotainment Systems

All MPS parts are lead-free, halogen-free, and adhere to the RoHS directive. For MPS green status, please visit the MPS website under Quality Assurance. “MPS”, the MPS logo, and “Simple, Easy Solutions” are trademarks of Monolithic Power Systems, Inc. or its subsidiaries.

TYPICAL APPLICATION



MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MPQ86760GVTE-AEC1	TQFN-21 (4mmx5mm)	*See Below*	1

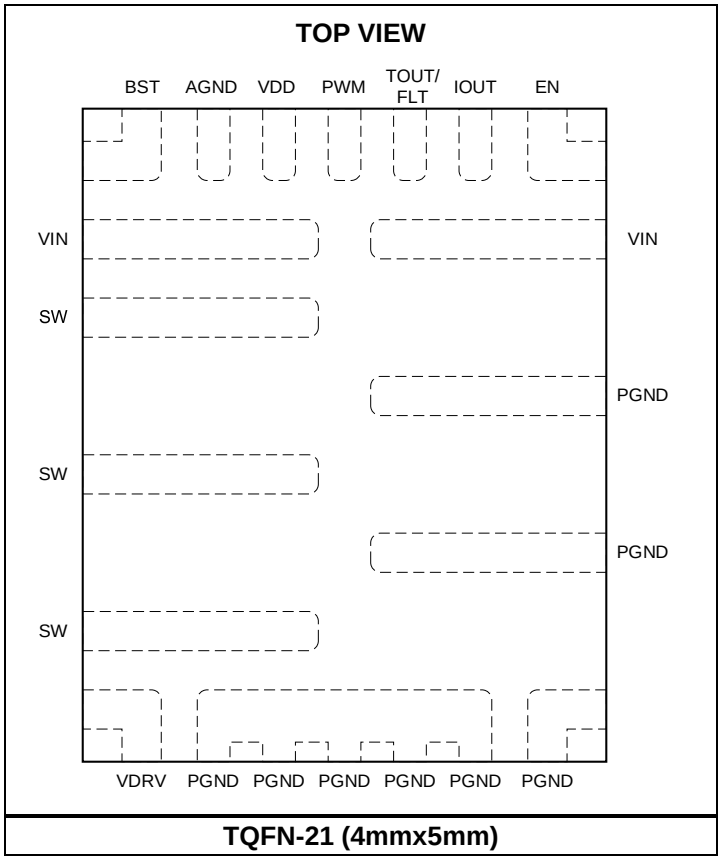
* For Tape & Reel, add suffix -Z (e.g. MPQ86760GVTE-AEC1-Z).

TOP MARKING

MPSYWW
M86760
LLLLLL
E

MPS: MPS prefix
Y: Year code
WW: Week code
M86760: Part number
LLLLLL: Lot number
E: Wettable flank

PACKAGE REFERENCE



TQFN-21 (4mmx5mm)

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

PIN FUNCTIONS

Pin #	Name	Description
1, 14	VIN	**Input supply voltage.** Place input ceramic capacitors (C_{IN}) close to the device to support the switching current and minimize parasitic inductance.
2, 3, 4	SW	**Phase node.**
5	VDRV	**Driver voltage.** Connect the VDRV pin to a 3.3V supply and decouple this pin with a 1µF to 4.7µF ceramic capacitor.
6, 7, 8, 9, 10, 11, 12, 13	PGND	**Power ground.**
15	EN	**Enable.** Pull the EN pin high to enable the device; pull it low to disable the device and place SW in a high-impedance (Hi-Z) state.
16	IOUT	**Current-sense output.** Use an external resistor to adjust the voltage so that it is proportional to the inductor current.
17	TOUT/FLT	**Single pin temperature sense and fault reporting.** If a fault occurs, the TOUT/FLT pin is pulled up to the VDD voltage (V_{DD}).
18	PWM	**Pulse-width modulation input.** Leave PWM floating or drive it to a middle state to put the SW pin in a Hi-Z state.
19	VDD	**3.3V power supply for internal logic.** Connect the VDD pin to a 3.3V external power supply through a 2.2Ω resistor. Decouple this pin with a 1µF capacitor connected to AGND. Connect AGND and PGND at the VDD pin's capacitor.
20	AGND	**Analog ground.**
21	BST	**Bootstrap.** The BST pin requires a 0.1µF to 0.22µF capacitor to drive the power switch's gate above the supply voltage. Place the capacitor between the SW and BST pins to form a floating supply across the power switch driver.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

ABSOLUTE MAXIMUM RATINGS (1)

Input voltage (V_{IN}) (DC).....8V
V_{IN} (25ns).....-3V to +10V
V_{SW} (DC).....-0.3V to +8V
V_{SW} (25ns).....-3V to +10V
V_{BST} to V_{SW} (DC).....4V
V_{BST} to V_{SW} (25ns) (2).....5V
V_{DD}, V_{DRV}.....-0.3V to +4V
AGND, PGND.....-0.3V to +0.3V
All other pins.....-0.3V to +4V
Instantaneous current ($I_{INSTANTANEOUS}$) (20ms).....
.....55A
Instantaneous current ($I_{INSTANTANEOUS}$) (10µs).....
.....90A
Junction temperature (T_J).....150°C
Lead temperature.....260°C
Storage temperature.....-65°C to +150°C

ESD Ratings (3)

Human body model (HBM).....Class 2
Charged-device model (CDM).....Class C2b

Recommended Operating Conditions (4)

Input voltage (V_{IN}).....3V to 6V
Supply voltage (V_{DRV}).....3V to 3.6V
Logic voltage (V_{DD}).....3V to 3.6V
Operating junction temp (T_J)....-40°C to +150°C

Thermal Resistance (5) θ_{JB} θ_{JC_TOP}

TQFN-21 (4mmx5mm) ……. 2.7.....15.4....°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) For the AMR of a shorter pulse (<25ns), contact an MPS FAE for the related application note.
3) Followed ANSI/ESDA/JEDEC JS-001 for HBM and ANSI/ESDA/JEDEC JS-002 for CDM.
4) The device is not guaranteed to function outside of its operating conditions.
5) Measured on a JESD51-7, 4-layer PCB.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS

V_{IN} = 5V, V_{DD} = V_{DRV} = EN = 3.3V, T_A = 25°C for typical value and T_A = -40°C to +150°C for max and min values, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input voltage (V_{IN}) under-voltage lockout (UVLO) rising threshold			2.3	2.6	2.98	V
V_{IN} UVLO threshold hysteresis				270		mV
VIN quiescent current in standby mode	I_{IN_STBY}	PWM = low, EN = low, V_{IN} = 6V, T_A = 25°C		0	1	µA
VIN quiescent current in active mode	$I_{IN_QUIESCENT}$	PWM = low, EN = high, V_{IN} = 6V, T_A = 25°C		20	40	µA
VDRV quiescent current	I_{VDRV}	PWM = low		250	400	µA
VDD quiescent current	I_{VDD}	PWM = low		3	4	mA
VDD voltage (V_{DD}) UVLO rising threshold			2.4	2.75	2.98	V
VDD voltage UVLO hysteresis				300		mV
VDRV voltage (V_{DRV}) UVLO rising threshold			2.4	2.75	2.98	V
VDRV voltage UVLO hysteresis				300		mV
High-side (HS) current limit		T_A = 25°C		90		A
Low-side (LS) current limit		T_A = 25°C		-25		A
LS off time at negative current limit (6)				120		ns
Dead time at SW rising (6)				3.5		ns
Dead time at SW falling (6)		Positive inductor current		10		ns
		Negative inductor current		20		ns
EN input high threshold voltage			2.3			V
EN input low threshold voltage					0.8	V
EN turn-on delay time (6)		V_{IN} = 5V, PWM = high		40		µs
PWM high to SW rising delay (6)	t_{RISING}			15		ns
PWM low to SW falling delay (6)	$t_{FALLING}$			15		ns
PWM tri-state to SW Hi-Z delay (6)	t_{LT}			40		ns
	t_{TL}			30		ns
	t_{HT}			40		ns
	t_{TH}			15		ns
Minimum PWM pulse width (6)				30		ns
IOUT sense gain				5		µA/A
IOUT sense gain accuracy (6)		20A ≤ I_{SW} ≤ 0A, V_{OUT} = 1.2V	-5	0	+5	%
IOUT sense offset		I_{SW} = 0A, V_{IOUT} = 1.2V	-10	0	+10	µA
		PWM = Hi-Z, V_{IOUT} = 1.2V	-2	0	+2	µA
TOUT/FLT sense gain (6)				8		mV/°C
TOUT/FLT voltage		T_J = 25°C		800		mV
Over-temperature (OT) fault latch-off (6)				170		°C
TOUT/FLT if a fault occurs		I_{FAULT} = 0.5mA	3	V_{DD}		V

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{DD} = V_{DRV} = EN = 3.3V, T_A = 25°C for typical value and T_A = -40°C to +150°C for max and min values, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
PWM resistance		Pull up, EN = high		5		kΩ
		Pull down		4		kΩ
PWM logic high voltage			2.3			V
PWM tri-state region			1.1		2	V
PWM logic low voltage					0.8	V

Note:

6) Guaranteed by design, not tested in production.

PWM TIMING CHART

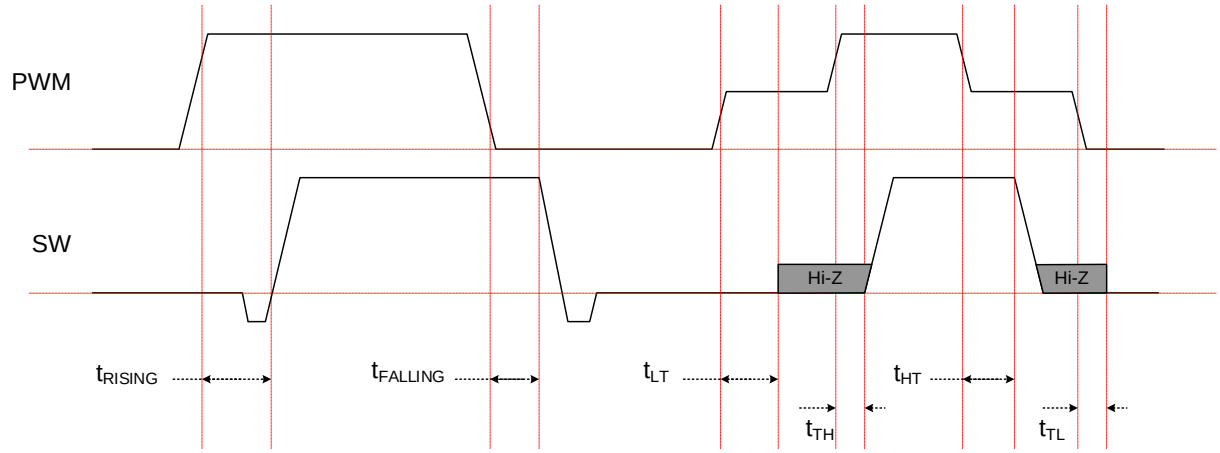


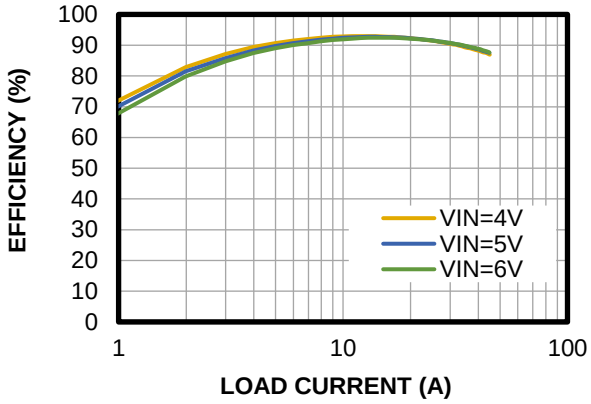
Figure 1: PWM Timing Chart

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

TYPICAL PERFORMANCE

Efficiency vs. Load Current

V_{OUT} = 0.75V, f_{SW} = 600kHz, L = 80nH



MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

FUNCTIONAL BLOCK DIAGRAM

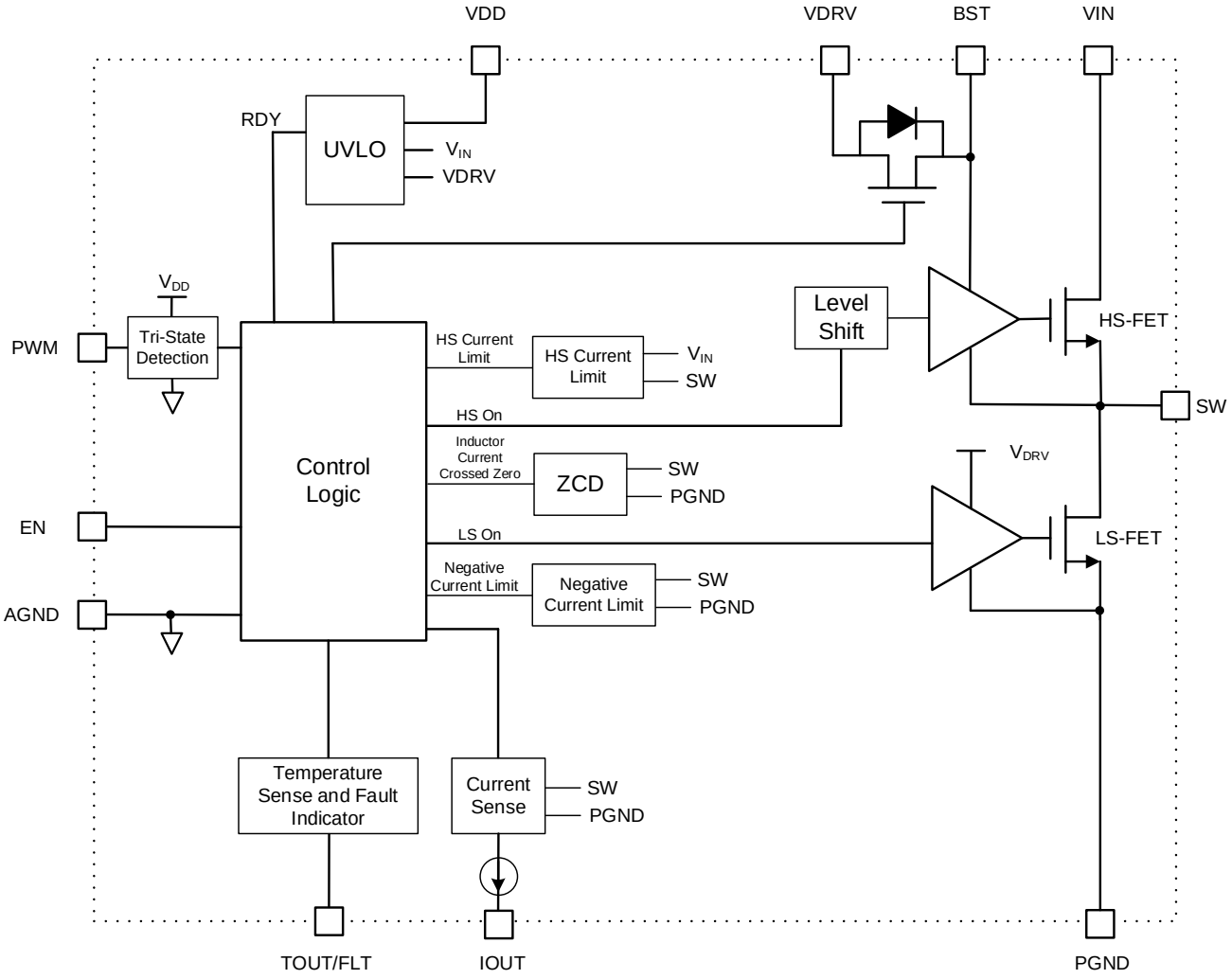


Figure 2: Functional Block Diagram

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

OPERATION

The MPQ86760 is a 45A, monolithic half-bridge driver with integrated MOSFETs. It is well-suited for multi-phase buck regulators. The VDD and VDRV pins are supplied by an external 3.3V. When the VIN, VDD, VDDRV, and VBST signals are sufficiently high, the device begins operating.

Pulse-Width Modulation (PWM)

The PWM input pin is capable of tri-state input. When the PWM input signal is within the tri-state threshold for 50ns (t_{HT} or t_{LT}), the high-side MOSFET (HS-FET) turns off immediately, and the low-side MOSFET (LS-FET) enters diode emulation mode. The LS-FET remains on until zero-current detection (ZCD).

The tri-state PWM input is enabled by forcing a middle-voltage PWM signal, or by floating the PWM input. The internal current source charges the signal to a middle voltage. See the PWM Timing Diagram on page 6 for the propagation delay definition from PWM to the SW node.

Standby Mode

When the EN pin is pulled low, the MPQ86760 enters standby mode. In standby mode, the device shuts down, and the IOUT and TOUT/FLT outputs are disabled. The fault latch cannot be reset by entering standby mode.

Diode Emulation Mode

When the PWM pin is in tri-state, the MPQ86760 enters diode emulation mode. The LS-FET turns on if the inductor current (I_L) is positive. The LS-FET turns off if the inductor current crosses the zero-current threshold. Diode emulation mode can be enabled by driving PWM to a middle state or floating PWM.

Current Sense

The current-sense pin (IOUT) is a bidirectional current source that is proportional to I_L. The current-sense gain is 5μA/A. Use a resistor to convert the current-sense gain into a volt-per-ampere gain to report I_L.

The IOUT output has two states (see Table 1). In standby mode, the IOUT circuit is disabled and requires 20μs to wake up and enter active mode.

Table 1: IOUT Output States

EN	IOUT
Low	Standby
High	Active

The IOUT voltage must be between 0.8V and 2V to obtain an accurate IOUT current output up to +450μA/-125μA (e.g. +90A/-25A). Generally, there is a resistor (R_{IOUT}) connected from IOUT to an external voltage capable of sinking a small current. This provides enough voltage to meet the required operating voltage range.

Figure 3 shows the typical circuit diagram of the IOUT connection to achieve a differential voltage source proportional to I_L.

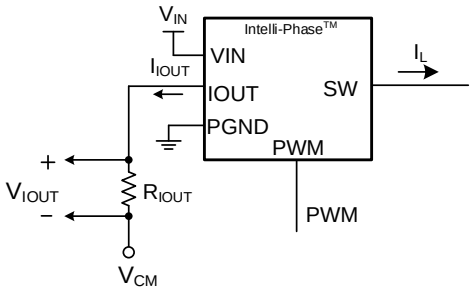


Figure 3: Typical Circuit Diagram for IOUT Pin Connection

To maintain V_{IOUT} within the operating range, calculate R_{IOUT} with Equation (1):

$$0.8V < I_{IOUT} \times R_{IOUT} + V_{CM} < 2.0V \quad (1)$$

Where V_{CM} is the reference voltage connected to R_{IOUT}.

The IOUT current (I_{IOUT}) can be calculated with Equation (2):

$$I_{IOUT} = G_{IOUT} \times I_L \quad (2)$$

Where G_{IOUT} is the current-sense gain.

V_{CM} can be obtained using a voltage divider from 3.3V (e.g. V_{DD}) (see Figure 4 on page 10). To minimize V_{CM} variation across I_{IOUT}, R_{IOUT} should exceed the equivalent resistance of R_1 in parallel with R_2 ($R_{IOUT} >> R_1 \parallel R_2$).

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

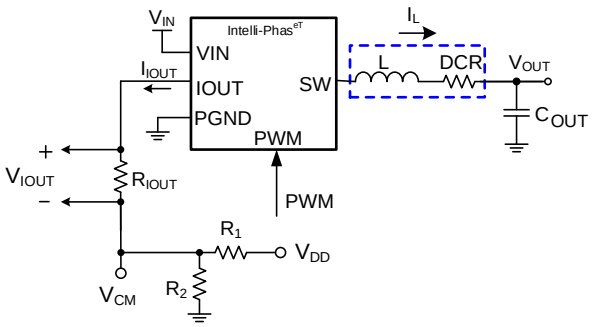


Figure 4: V_{CM} for IOUT Signal from V_{DD}

Positive and Negative Inductor Current Limit

If an over-current (OC) condition is detected on the HS-FET, the MPQ86760 immediately turns off the HS-FET and turns on the LS-FET.

If an OC condition is detected on the LS-FET, the MPQ86760 turns off the LS-FET and turns on the HS-FET for 120ns to limit the negative current.

Over-Temperature Protection (OTP)

If the junction temperature (T_J) reaches the over-temperature (OT) threshold, the HS-FET latches off, and TOUT/FLT is pulled to V_{DD}. The LS-FET turns on and stays on until ZCD.

Temperature-Sense Output with Fault Indication (TOUT/FLT)

The TOUT/FLT pin is a pin with dual functions, described below:

Junction Temperature (T_J) Sense

TOUT/FLT is a voltage output that is proportional to T_J when the MPQ86760 is in active mode. The temperature-sense gain is 8mV/°C, with a 600mV offset. For example, the voltage gain is 0.8V when T_J = 25°C, and 1.6V when T_J = 125°C.

Fault Indication

If an OT fault occurs (T_J reaches the OT threshold), TOUT/FLT is pulled to V_{DD} to report the fault event. Then the MPQ86760 latches off to turn off the HS-FET. The LS-FET turns on and remains on until I_L reaches 0A.

The fault latch cannot be reset by entering standby mode. The fault latch can only be released by cycling the power on VIN, VDD, and VDRV.

For multi-phase operation, the TOUT/FLT pins of all Intelli-Phase are connected together (see Figure 5).

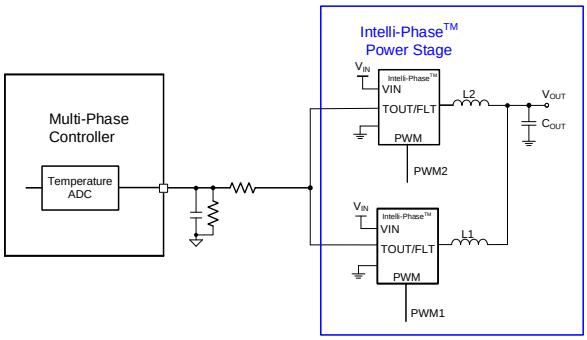


Figure 5: Multi-Phase Temperature Sense Utilization

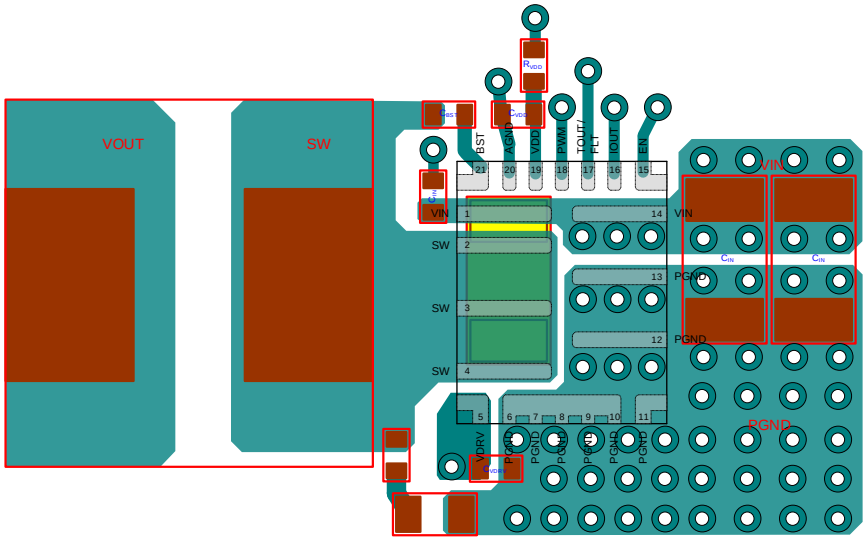
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

APPLICATION INFORMATION

PCB Layout Guidelines

The PCB layout is critical for stable and efficient operation. For the best results, refer to Figure 6 and follow the guidelines below.

1. Place the input MLCC capacitors as close to VIN and PGND as possible.
2. Add a 0.1µF to 1µF VIN capacitor next to pin 1.
3. Place the major MLCC capacitors on the same layer as the Intelli-Phase™.
4. Maximize the VIN and PGND copper plane to minimize parasitic impedance.
5. Place as many VIN and PGND vias as possible near the PGND plane to minimize parasitic impedance and thermal resistance.
6. Place the VDRV decoupling capacitor close to the VDRV pin. Ensure the VDRV capacitance exceeds the bootstrap (BST) capacitance. For example, use 1µF for the VDRV capacitor and 0.22µF for the BST capacitor.
7. Place the VDD decoupling capacitor close to the VDD pin.
8. Connect AGND and PGND at the point of the VDD capacitor's ground connection.
9. Place the BST capacitor as close to the BST and SW pins as possible.
10. Place an RC snubber circuit placeholder to tune the switching spike if needed.
11. Route the BST path with a trace width of 20mil or longer.
12. Use a 0.1µF to 1µF BST capacitor.
13. Route the IOUT signal with a 10mil trace width.
14. Route the IOUT signal trace away from high-current paths, such as SW and PWM.
15. Keep a 40mil distance between IOUT and any noisy signals.
16. Route the IOUT signal and the noisy signals in two different layers. Place a solid GND layer between these layers.
17. Route the PWM signal with a 10mil trace width.



Input Capacitor: 1206 Package (Top Side and Bottom Side) and 0402 Package (Top Side)
Inductor: 6.5mmx6.5mm
VDD/VDRV/BST Capacitor: 0402 Package
Via Size: 20/10mil

Figure 6: Recommended PCB Layout (Placement and Top Layer)

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

TYPICAL APPLICATION CIRCUIT

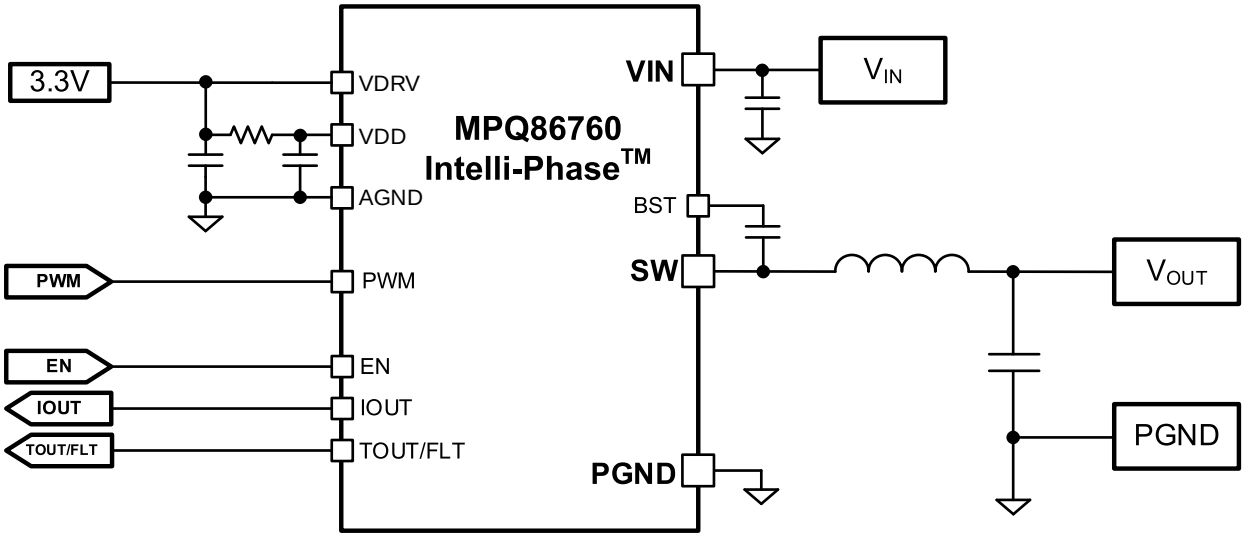
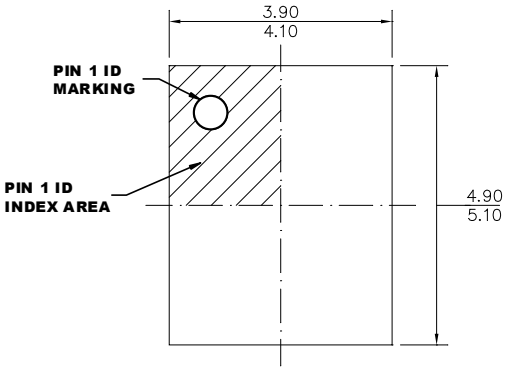


Figure 7: Typical Application Circuit

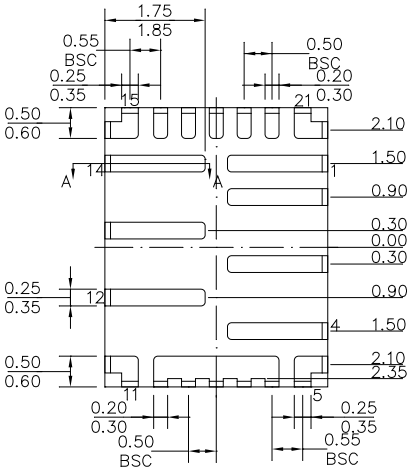
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

PACKAGE INFORMATION

TQFN-21 (4mmx5mm)

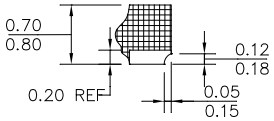


TOP VIEW

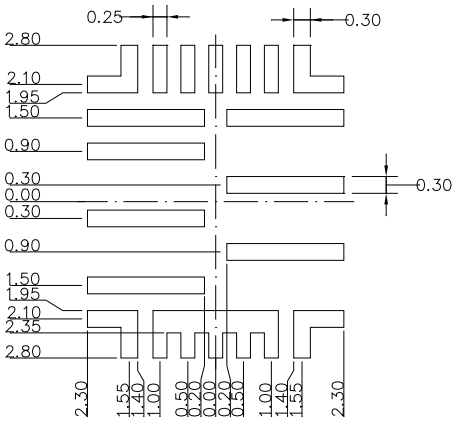


BOTTOM VIEW

SIDE VIEW



SECTION A-A



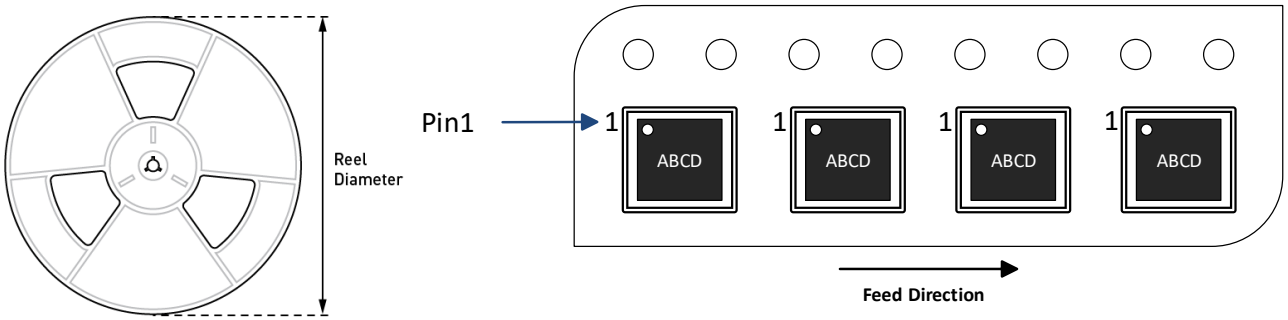
RECOMMENDED LAND PATTERN

NOTE:

1) THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ86760GVTE-AEC1-Z	TQFN-21 (4mmx5mm)	5000	N/A	N/A	13in	12mm	8mm

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	7/11/2024	Initial Release	-

Notice: The information in this document is subject to change without notice. Please contact MPS for current specifications. Users should warrant and guarantee that third-party Intellectual Property rights are not infringed upon when integrating MPS products into any application. MPS will not assume any legal responsibility for any said applications.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.