MPQ8633A

16V, 12A, Synchronous Step-Down Converter with Adjustable Current Limit, Programmable Frequency, and Voltage Tracking

DESCRIPTION

The MPQ8633A is a fully integrated, high-frequency, synchronous buck converter. It offers a very compact solution to achieve up to 12A output current over a wide input supply range with excellent load and line regulation. The MPQ8633A operates at high efficiency over a wide output current load range.

The MPQ8633A adopts internally compensated constant-on-time (COT) control mode that provides fast transient response and eases loop stabilization.

The operating frequency is set easily to 600kHz, 800kHz, or 1000kHz with the MODE configuration, allowing the MPQ8633A frequency to remain constant regardless of the input/output voltages.

The output voltage start-up ramp is controlled by an internal 1ms timer. It can be increased by adding a capacitor on TRK/REF. An open-drain power good(PGOOD) signal indicates the output is within its nominal voltage range. The PGOOD is clamped to around 0.7V with external pull-up voltage when the input supply fails to power the MPQ8633A.

Fully integrated protection features include over-current protection (OCP), over-voltage protection (OVP), under-voltage protection (UVP), and over-temperature protection (OTP).

The MPQ8633A requires a minimum number of readily available, standard, external components and is available in a QFN 3mm x 4mm package.

FEATURES

- Wide Input Voltage Range from 2.7V:
  - 2.7V to 16V with External 3.3V VCC Bias
  - 4 V to 16V with Internal Bias or External 3.3V VCC Bias
- Differential Output Voltage Remote Sense
- Programmable Accurate Current Limit Level
- 12A Output Current
- Low $R_{DS(ON)}$ Integrated Power MOSFETs
- Proprietary Switching Loss Reduction Technique
- Adaptive COT for Ultrafast Transient Response
- Stable with Zero ESR Output Capacitor
- 0.5% Reference Voltage over 0°C to +70°C Junction Temperature Range
- 1% Reference Voltage from -40°C to +125°C Junction Temperature Range
- Selectable Pulse Skip or Forced CCM Operation
- Excellent Load Regulation
- Output Voltage Tracking
- Output Voltage Discharge
- PGOOD Active Clamped Low Level during Power Failure
- Programmable Soft-Start Time from 1ms
- Pre-Bias Start-Up
- Selectable Switching Frequency from 600kHz, 800kHz, and 1000kHz
- Non-Latch OCP, UVP, UVLO, Thermal Shutdown, and Latch-Off for OVP.
- Output Adjustable from 0.6V to 90%*Vin, up to 5.5V Max.
- Available in a QFN 3mm x 4mm Package

APPLICATIONS

- Telecom and Networking Systems
- Server, Cloud-Computing, Storage
- Base Stations
- General Purpose Point-of-Load (PoL)
- 12V Distribution Power Systems
- High-end TV
- Game Consoles and Graphic Cards

All MPS parts are lead-free, halogen-free, and adhere to the RoHS directive. For MPS green status, please visit the MPS website under Quality Assurance.

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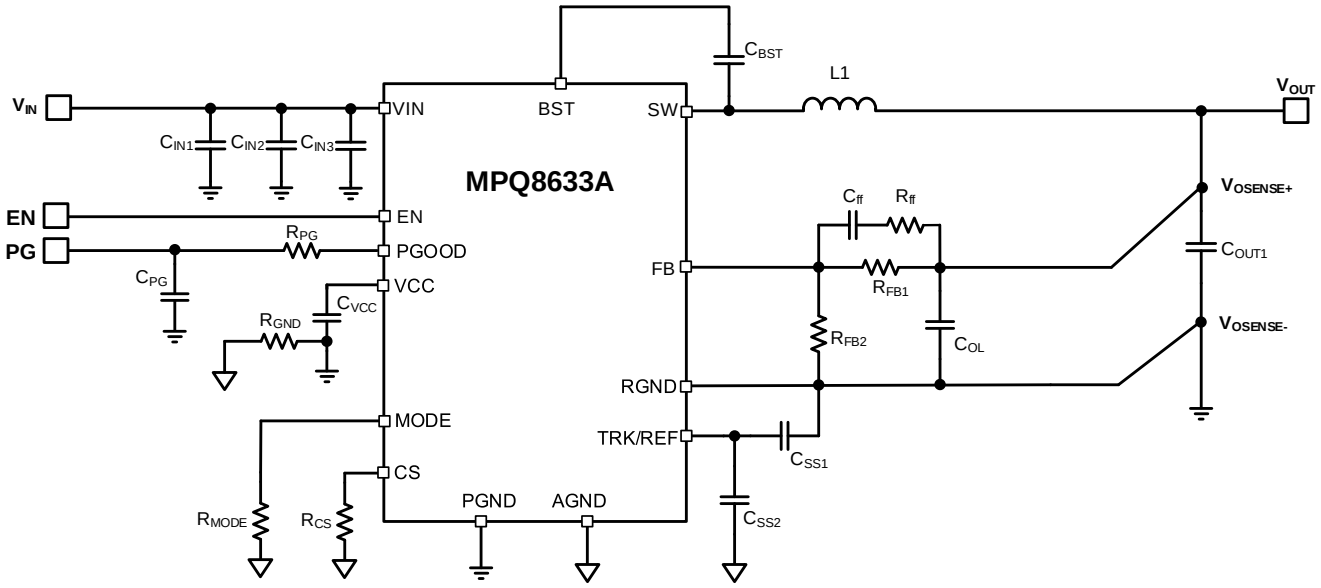
TYPICAL APPLICATION



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ORDERING INFORMATION

Part Number	Package	Top Marking
MPQ8633AGLE*	QFN-21 (3mm x 4mm)	*See Below*
MPQ8633AGL**	QFN-20 (3mm x 4mm)	*See Below*

* For Tape & Reel, add suffix –Z (e.g. MPQ8633AGLE–Z)

** For Tape & Reel, add suffix –Z (e.g. MPQ8633AGL–Z)

****MPQ8633AGL is not recommended for new design**

TOP MARKING (MPQ8633AGLE)

MPYW
8633
ALLL
E

MP: MPS prefix
Y: Year code
W: Week code
8633A: First five digits of the part number
LLL: Lot number
E: MPQ8633AGLE

TOP MARKING (MPQ8633AGL)

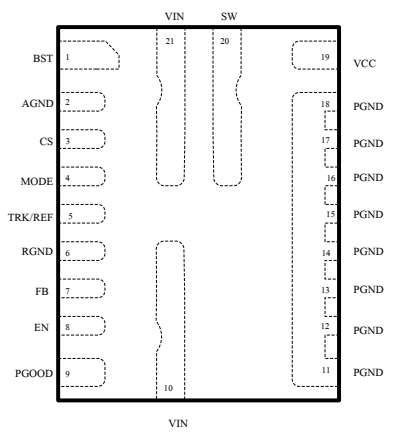
(Not recommended for new design)

MPYW
8633
ALLL

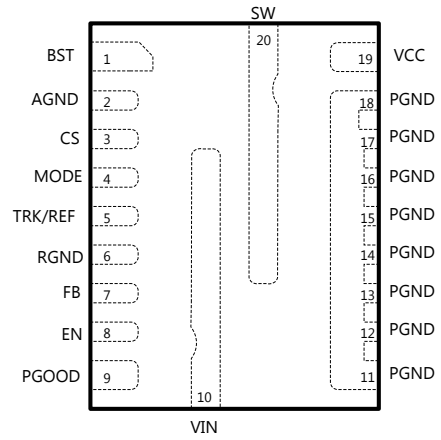
MP: MPS prefix
Y: Year code
W: Week code
8633A: First five digits of the part number
LLL: Lot number

PACKAGE REFERENCE

TOP VIEW QFN (3mm x 4mm)



(QFN-21)



(QFN-20)
(Not recommended for new design)

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ABSOLUTE MAXIMUM RATINGS [1]

Supply voltage (V_{IN}) 18V
V_{IN} - V_{SW} (DC) ..... -0.3V to +18.3V
V_{IN} - V_{SW} (25ns)..... -5V to +28V
V_{SW} (DC)..... -0.3V to +18.3V
V_{SW} (25ns) [2] ..... -5V to +25V
V_{BST} 22.3V
V_{BST} - V_{SW} (25ns) [2] 5V
V_{CC}, EN..... 4.5V
All other pins..... -0.3V to +4.3V
Junction temperature (T_J) ..... 170°C
Lead temperature ..... 260°C
Storage temperature..... -65°C to +170°C

Recommended Operating Conditions [3]

Supply voltage (V_{IN}) ..... 4V to 16V
Output voltage (V_{OUT})..... 0.6V to 5.5V
External VCC bias (V_{CC_EXT})..... 3.12V to 3.6V
Maximum output current (I_{OUT_MAX}) 12A
Maximum output current limit (I_{OC_MAX}) 16A
Maximum peak inductor current (I_{L_PEAK}) 18A
EN voltage (V_{EN}) 3.6V
Operating junction temp (T_J) .... -40°C to +125°C

Thermal Resistance [4]

	θ_{JB}	θ_{JC_TOP}
QFN (3mmx4mm)	9	21

°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) Measured by using differential oscilloscope probe.
3) The device is not guaranteed to function outside of its operating conditions.
4) Θ_{JB}: Thermal resistance from junction to board around PGND pin soldering point.
   Θ_{JC_TOP}: Thermal resistance from junction to top of package.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_J = -40°C to +125°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
SUPPLY CURRENT						
Supply current (shutdown)	I_{IN}	V_{EN} = 0V		0	10	μA
Supply current (quiescent)	I_{IN}	V_{EN} = 2V, V_{FB} = 0.62V		650	850	μA
MOSFET						
Switch leakage	SW_{LKG_HS}	V_{EN} = 0V, V_{SW} = 0V		0	10	μA
	SW_{LKG_LS}	V_{EN} = 0V, V_{SW} = 12V		0	30	
HS on-state resistance	$R_{DS_ON_HS}$	V_{EN} = 2V @ 25ºC		13.3		mΩ
LS on-state resistance	$R_{DS_ON_LS}$	V_{EN} = 2V @ 25ºC		3.8		mΩ
CURRENT LIMIT						
Current limit threshold	V_{LIM}		1.15	1.2	1.25	V
I_{CS} to I_{OUT} ratio	I_{CS}/I_{OUT}	I_{OUT} ≥2A	18	20	22	μA/A
Low-side negative current limit	I_{LIM_NEG}			-9		A
Negative current limit time-out[6]	t_{NCL_Timer}			200		ns
SWITCHING FREQUENCY						
Switching frequency[7]	f_{SW}	MODE = GND, I_{OUT} =0A, V_{OUT}=1V,	480	600	720	kHZ
		MODE = 30.1K, I_{OUT} =0A, V_{OUT}=1V,	680	800	920	kHZ
		MODE = 60.4K, I_{OUT} =0A, V_{OUT}=1V,	850	1000	1150	kHZ
Minimum on time [6]	T_{ON_MIN}	V_{FB} = 500mV			50	ns
Minimum off time [6]	T_{OFF_MIN}	V_{FB} = 500mV			180	ns
OVER-VOLTAGE AND UNDER-VOLTAGE PROTECTION						
OVP threshold	V_{OVP}		113%	116%	119%	V_{REF}
UVP threshold	V_{UVP}		77%	80%	83%	V_{REF}
FEEDBACK VOLTTAGE AND SOFT-START						
FEEDBACK voltage	V_{REF}	T_J = -40°C to +125°C	594	600	606	mV
		T_J = 0°C to +70°C	597	600	603	mV
TRK/REF sourcing current	I_{TRACK_Source}	$V_{TRK/REF}$ = 0V		42		μA
TRK/REF sinking current	I_{TRACK_Sink}	$V_{TRK/REF}$ = 1V		12		μA
Soft-start time	t_{SS}	C_{TRACK} = 1nF, T_J = 25°C	0.75	1	1.25	ms
ERROR AMPLIFIER						
Error amplifier offset	V_{OS}		-3	0	3	mV
Feedback current	I_{FB}	V_{FB} = REF		50	100	nA

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_J = -40°C to +125°C, unless otherwise noted.

ENABLE AND UVLO						
Enable input rising threshold	VIH_{EN}		1.17	1.22	1.27	V
Enable hysteresis	V_{EN-HYS}			200		mV
Enable input current	I_{EN}	V_{EN} = 2V		0		μA
Soft shutdown discharge FET	R_{ON_DISCH}			80	150	Ω
VIN UVLO						
VIN under-voltage lockout threshold rising	VIN_{Vth_Rise}	V_{CC} = 3.3V	2.1	2.4	2.7	V
VIN under-voltage lockout threshold falling	VIN_{Vth_Fall}		1.55	1.85	2.15	V
VCC REGULATOR						
VCC under-voltage lockout threshold rising	VCC_{Vth_Rise}		2.65	2.8	2.95	V
VCC under-voltage lockout threshold falling	VCC_{vth_Fall}		2.35	2.5	2.65	V
VCC regulator	V_{CC}		2.88	3.00	3.12	V
VCC load regulation		Icc = 25mA		0.5		%
POWER GOOD						
Power good high threshold	$PG_{Vth_Hi_Rise}$	FB from low to high	89.5%	92.5%	95.5%	V_{REF}
Power good low threshold	$PG_{Vth_Lo_Rise}$	FB from low to high	113%	116%	119%	V_{REF}
	$PG_{Vth_Lo_Fall}$	FB from high to low	77%	80%	83%	V_{REF}
Power good low to high delay	PG_{Td}	T_J = 25°C	0.63	0.9	1.17	ms
Power good sink current capability	V_{PG}	I_{PG} = 10mA			0.5	V
Power good leakage current	I_{PG_LEAK}	V_{PG} = 3.3V			3	μA
Power good low-level output voltage	V_{OL_100}	V_{IN} = 0V, Pull PGOOD up to 3.3V through a 100KΩ resistor @ 25°C.		650	800	mV
	V_{OL_10}	V_{IN} = 0V, Pull PGOOD up to 3.3V through a 10KΩ resistor @ 25°C.		750	900	mV
THERMAL PROTECTION						
Thermal shutdown [6]	T_{SD}			160		°C
Thermal shutdown hysteresis[6]				30		°C

NOTE:

5) Guaranteed by design.

6) Guaranteed by design over temperature..

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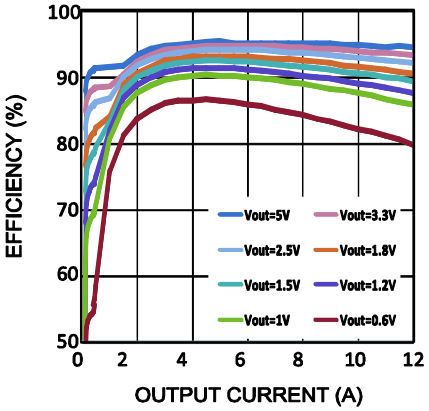
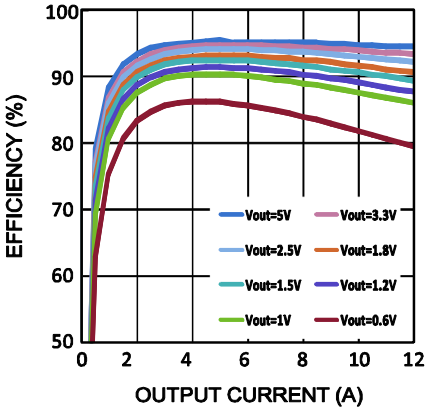
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, T_A = 25˚C, V_{OUT} = 1.2V, F_S = 800kHz unless otherwise noted.

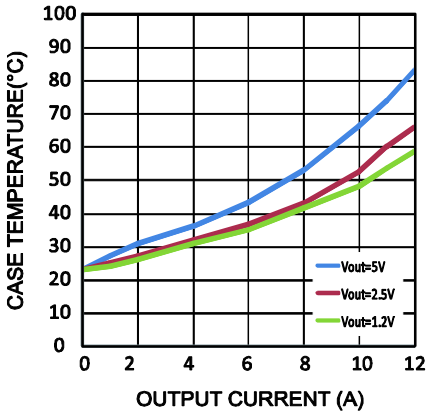
Efficiency
Pulse Skip, 1.1uH, 800kHz



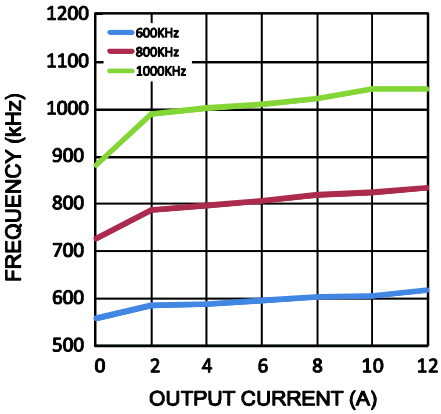
Efficiency
Forced CCM, 1.1uH, 800kHz



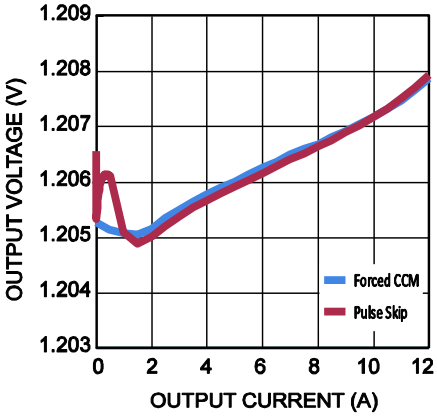
Thermal Results
800kHz, No air-flow



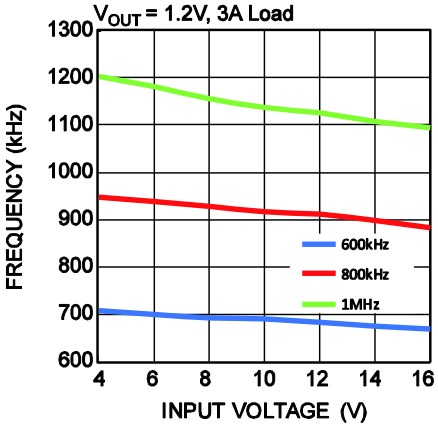
Switching Frequency vs. Output Current
Forced CCM



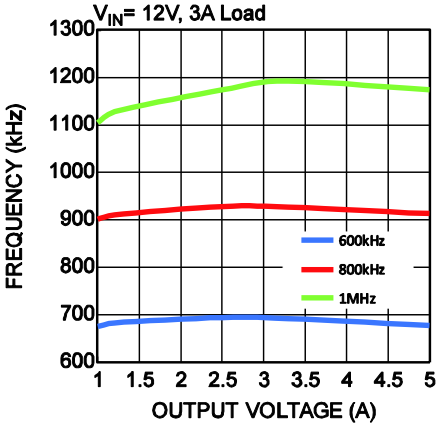
Output Voltage Load Regulation



Switching Frequency vs. Input Voltage
V_{OUT} = 1.2V, 3A Load



Switching Frequency vs. Input Voltage
V_{IN}= 12V, 3A Load



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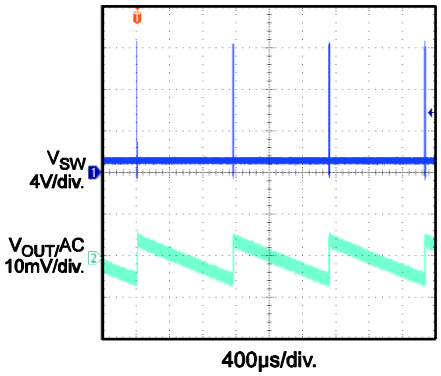
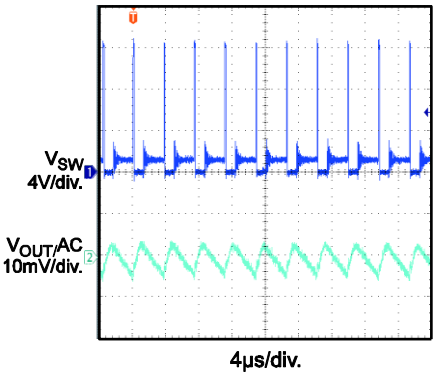
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_A = 25˚C, V_{OUT} = 1.2V, F_S = 800kHz unless otherwise noted.

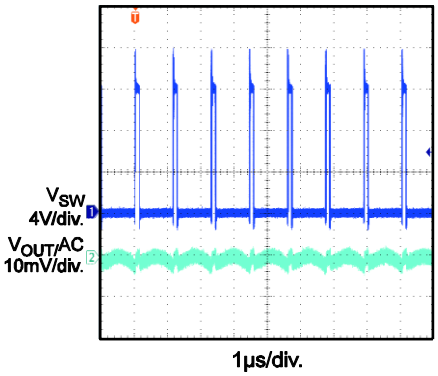
Steady State
I_{OUT} = 0A, Pulse Skip



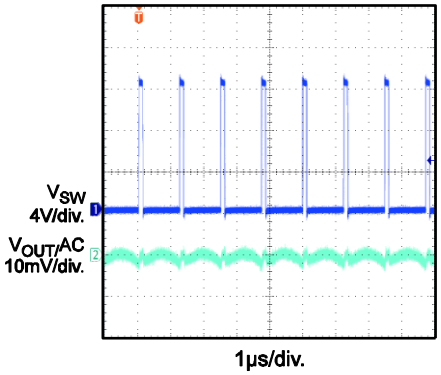
Steady State
I_{OUT} = 0.5A, Pulse Skip



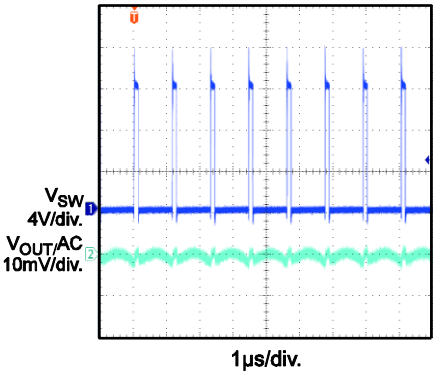
Steady State
I_{OUT} = 12A, Pulse Skip



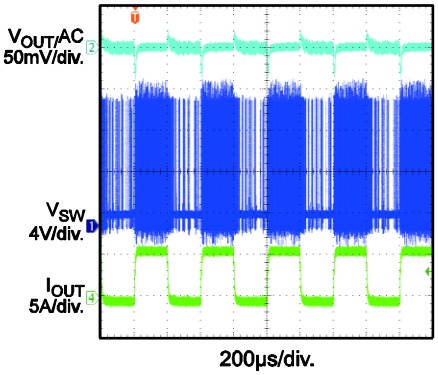
Steady State
I_{OUT} = 0A, Forced CCM



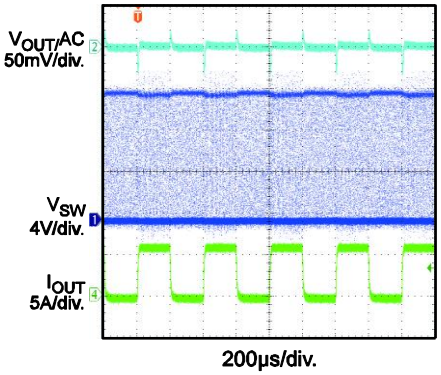
Steady State
I_{OUT} = 12A, Forced CCM



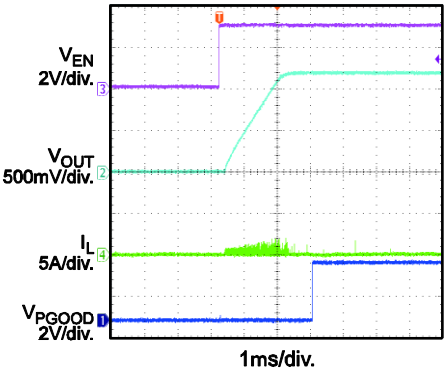
Load Transient
I_{OUT} = 0A-6A, Pulse Skip



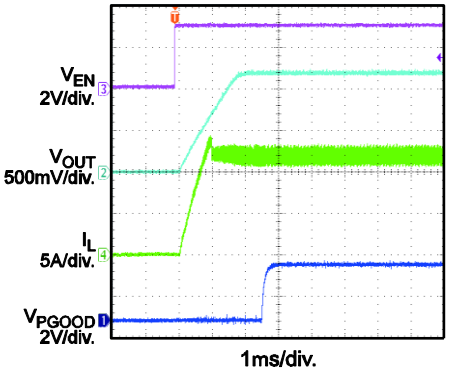
Load Transient
I_{OUT} = 0A-6A, Forced CCM



Power Up through EN
I_{OUT} = 0A, Pulse Skip



Power Up through EN
I_{OUT} = 12A, Pulse Skip



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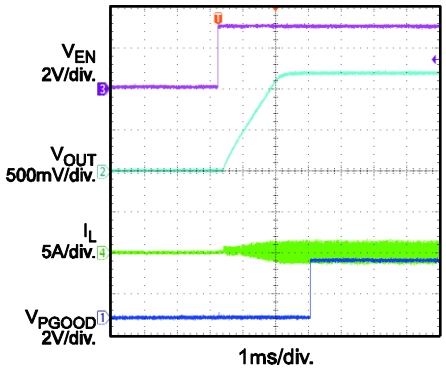
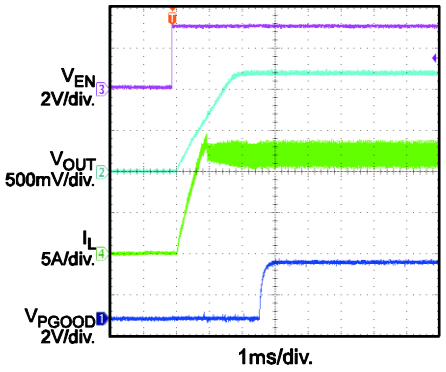
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_A = 25˚C, V_{OUT} = 1.2V, F_S = 800kHz unless otherwise noted.

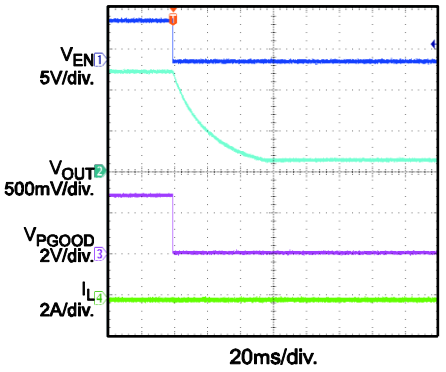
Power Up through EN
I_{OUT} = 0A, Forced CCM



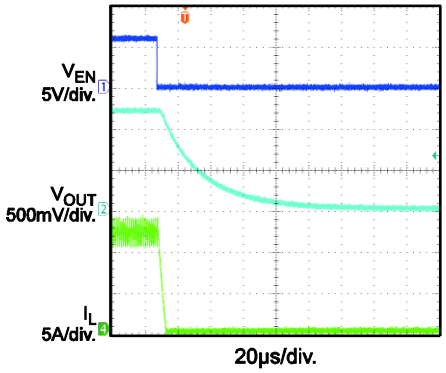
Power Up through EN
I_{OUT} = 12A, Forced CCM



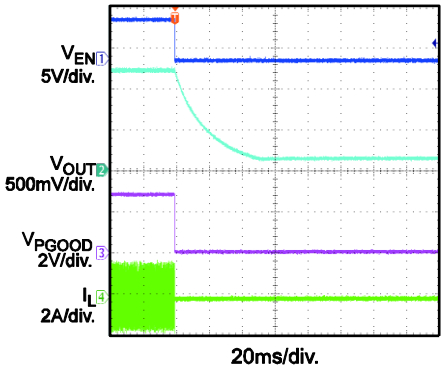
Power Down through EN
I_{OUT} = 0A, Pulse Skip



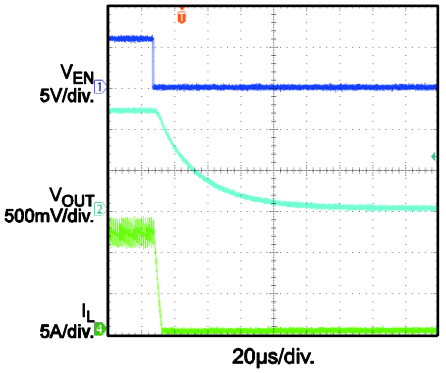
Power Down through EN
I_{OUT} = 12A, Pulse Skip



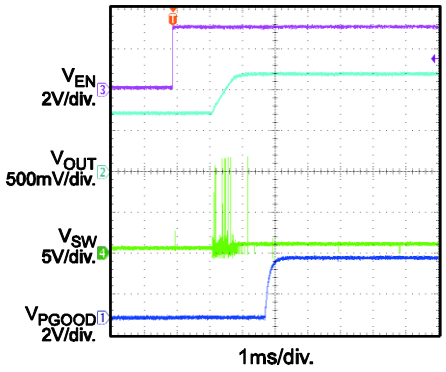
Power Down through EN
I_{OUT} = 0A, Forced CCM



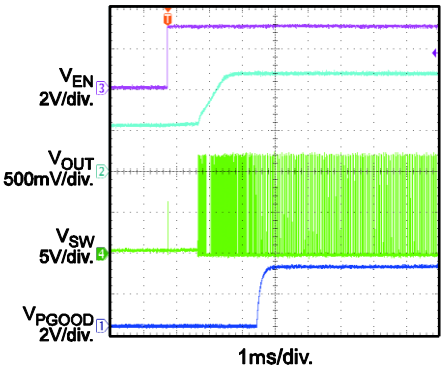
Power Down through EN
I_{OUT} = 12A, Forced CCM



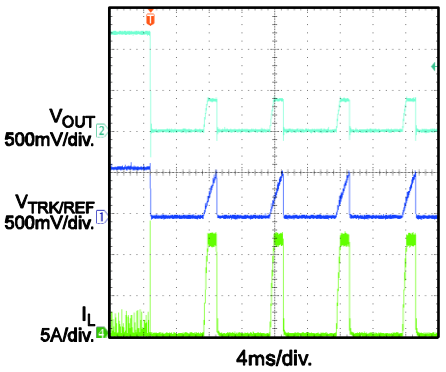
Pre-bias Start Up
Pulse Skip



Pre-bias Start Up
Forced CCM



Over-Current Protection Entry



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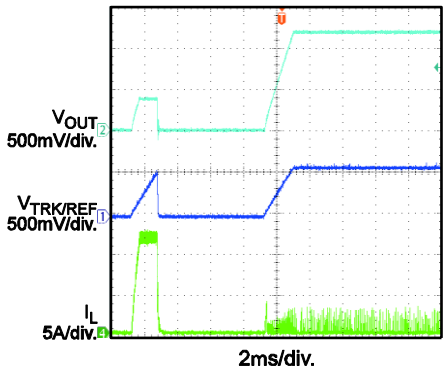
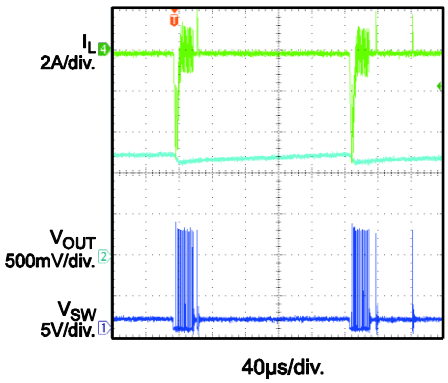
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_A = 25˚C, V_{OUT} = 1.2V, F_S = 800kHz unless otherwise noted.

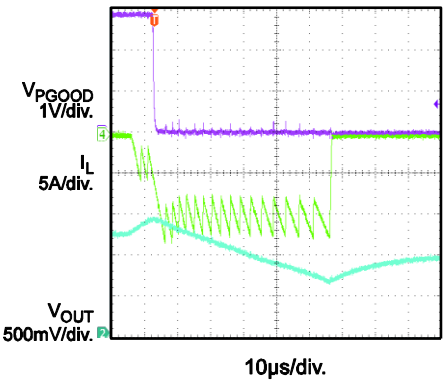
Over-Current Protection Recovery



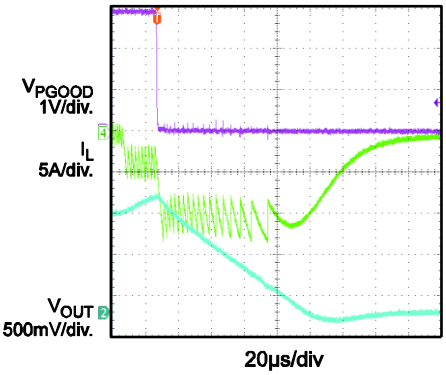
OSM Operation
Pulse Skip Mode



Over-voltage Protection
Pulse Skip Mode



Over-voltage Protection
Forced CCM



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PIN FUNCTIONS

MPQ8633A (QFN-21)

PIN #	Name	Description
1	BST	**Bootstrap**. A capacitor connected between SW and BS is required to form a floating supply across the high-side switch driver.
2	AGND	**Analog ground.** Select AGND as the control circuit reference point.
3	CS	**Current limit.** Connect a resistor to AGND to set the current limit trip point. See Equation 4 for additional details.
4	MODE	**Operation mode selection**. Program MODE to select CCM, pulse skip mode, and the operating switching frequency. See Table 1 for additional details.
5	TRK/REF	**External tracking voltage input.** The output voltage tracks this input signal. Decouple with a ceramic capacitor as close to TRK/REF as possible. X7R or X5R grade dielectric ceramic capacitors are recommended for their stable temperature characteristics. The capacitance of this capacitor determines the soft-start time. See Equation 2 and 3 for additional details.
6	RGND	**Differential remote sense negative input.** Connect this pin directly to the negative side of the voltage sense point. Short to GND if remote sense is not used.
7	FB	**Feedback (Differential remote sense positive input).** An external resistor divider from the output to RGND (tapped to FB) sets the output voltage. It is recommended to place the resistor divider as close to FB as possible. Vias should be avoided on the FB traces.
8	EN	**Enable**. EN is an input signal that turns the regulator on or off. Drive EN high to turn on the regulator, drive EN low to turn off the regulator. Connect EN to VIN through a pull-up resistor or a resistive voltage divider for automatic start-up. Do NOT float EN.
9	PGOOD	**Power good output.** This is an open-drain signal. A pull-up resistor (connected to a DC voltage) is required to indicate high if the output voltage is within regulation. There is about 1ms delay from FB ≥ 92.5% to PGOOD pull-high.
10, 21	VIN	**Input voltage.** VIN supplies power for the internal MOSFET and regulator. The input capacitors are needed to decouple the input rail. Use wide PCB traces to make the connection.
11-18	PGND	**System ground.** PGND is the reference ground of the regulated output voltage. For this reason, care must be taken in PCB layout. Use wide PCB traces to make the connection.
19	VCC	**Internal 3V LDO output.** The driver and control circuits are powered from this voltage. Decouple with a minimum 1μF ceramic capacitor as close to VCC as possible. X7R or X5R grade dielectric ceramic capacitors are recommended for their stable temperature characteristics.
20	SW	**Switch output.** Connect SW to the inductor and bootstrap capacitor. SW is driven up to the VIN voltage by the high-side switch during the on-time of the PWM duty cycle. The inductor current drives SW low during the off-time. Use wide PCB traces to make the connection.

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MPQ8633A (QFN20)

PIN #	Name	Description
1	BST	**Bootstrap**. A capacitor connected between SW and BS is required to form a floating supply across the high-side switch driver.
2	AGND	**Analog ground.** Select AGND as the control circuit reference point.
3	CS	**Current limit.** Connect a resistor to AGND to set the current limit trip point. See equation 4 for additional details.
4	MODE	**Operation mode selection**. Program MODE to select CCM, pulse skip mode, and the operating switching frequency. See Table 1 for additional details.
5	TRK/REF	**External tracking voltage input.** The output voltage tracks this input signal. Decouple with a ceramic capacitor as close to TRK/REF as possible. X7R or X5R grade dielectric ceramic capacitors are recommended for their stable temperature characteristics. The capacitance of this capacitor determines the soft-start time. See Equation 2 and 3 for additional details.
6	RGND	**Differential remote sense negative input.** Connect this pin directly to the negative side of the voltage sense point. Short to GND if remote sense is not used.
7	FB	**Feedback (Differential remote sense positive input).** An external resistor divider from the output to RGND (tapped to FB) sets the output voltage. It is recommended to place the resistor divider as close to FB as possible. Vias should be avoided on the FB traces.
8	EN	**Enable**. EN is a input signal that turns the regulator on or off. Drive EN high to turn on the regulator, drive EN low to turn off the regulator. Connect EN to VIN through a pull-up resistor or a resistive voltage divider for automatic start-up. Do NOT float EN.
9	PGOOD	**Power good output.** This is an open-drain signal. A pull-up resistor (connected to a DC voltage) is required to indicate high if the output voltage is within the regulation. There is about 1ms delay from FB ≥ 92.5% to PGOOD pull-high.
10	VIN	**Input voltage.** VIN supplies power for the internal MOSFET and regulator. The input capacitors are needed to decouple the input rail. Use wide PCB traces to make the connection.
11-18	PGND	**System ground.** PGND is the reference ground of the regulated output voltage. For this reason, care must be taken in PCB layout. Use wide PCB traces to make the connection.
19	VCC	**Internal 3V LDO output.** The driver and control circuits are powered from this voltage. Decouple with a minimum 1μF ceramic capacitor as close to VCC as possible. X7R or X5R grade dielectric ceramic capacitors are recommended for their stable temperature characteristics.
20	SW	**Switch output.** Connect SW to the inductor and bootstrap capacitor. SW is driven up to the V_{IN} voltage by the high-side switch during the on-time of the PWM duty cycle. The inductor current drives SW low during the off-time. Use wide PCB traces to make the connection.

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FUNCTIONAL BLOCK DIAGRAM

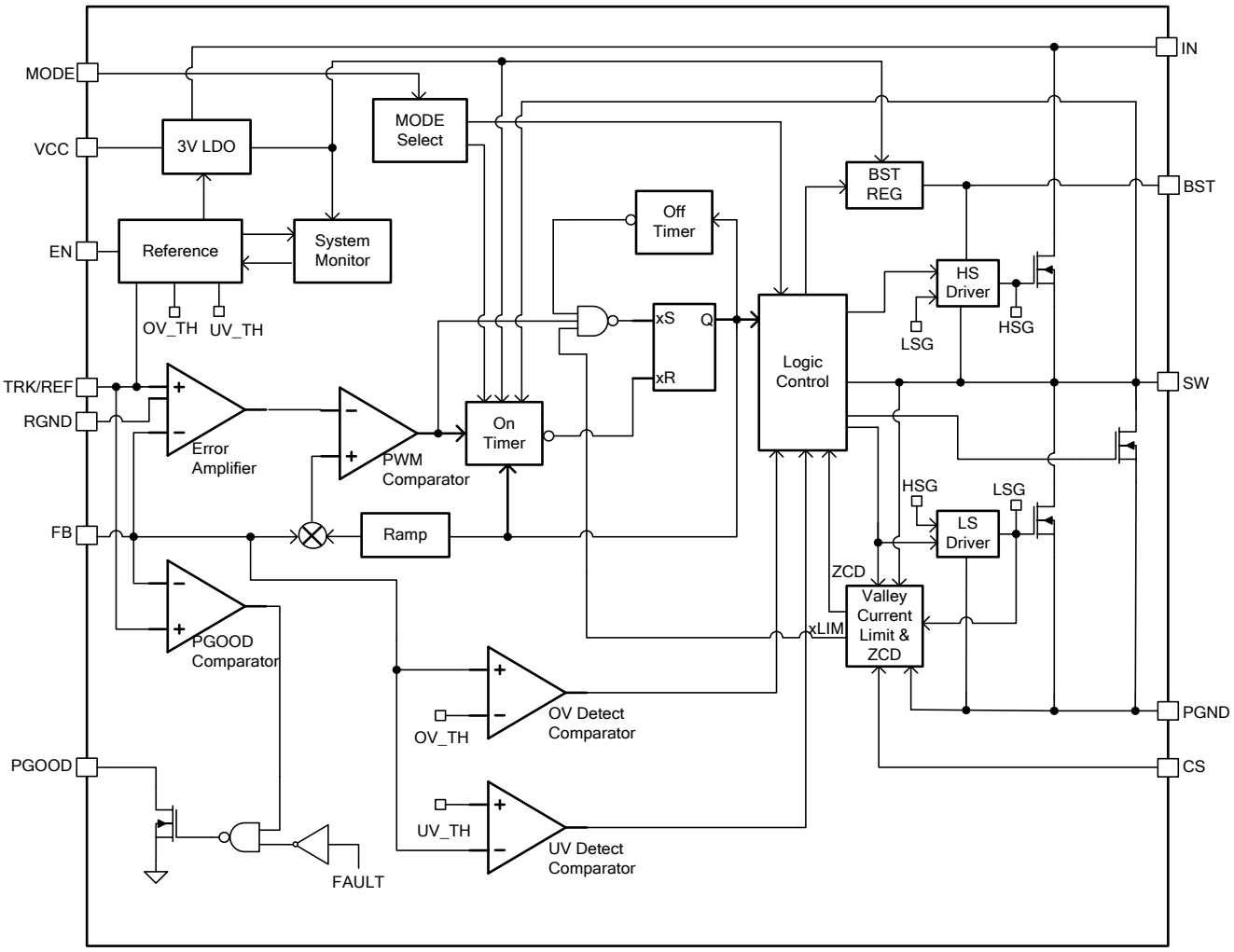

Figure 1—Functional block diagram

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OPERATION

COT Control

The MPQ8633A employs constant-on-time (COT) control to achieve fast load transient response. In Figure 2, it shows the details of the control stage of MPQ8633A.

The operational amplifier (AMP) corrects any error voltage between FB and VREF. With the help of AMP, MPQ8633A can provide excellent load regulation over the whole load range, no matter it operates in forced CCM or pulse skip mode.

The dedicated RGND pin helps to provide the feature of the differential output voltage remote sense. The pair of the remote sense trace should be kept in low impedance to achieve the best performance.

The MPQ8633A has internal RAMP compensation, so that it supports low ESR MLCC output capacitor solution. The adaptive internal RAMP is optimized so that the MPQ8633A is stable in the whole operating input/output voltage range with proper design of the output L/C filter.

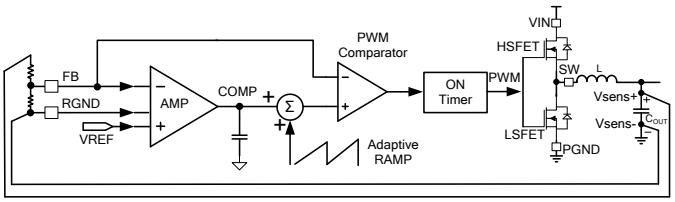

FIGURE 2—COT CONTROL

PWM Operation

In Figure 3, it shows how the PWM is generated. The AMP corrects any error between FB and REF, and generates a fairly smooth DC voltage (COMP). The internal RAMP is superimposed onto COMP. The superimposed COMP is compared with the FB signal. Whenever FB drops below the superimposed COMP, it turns on the integrated high-side MOSFET (HS-FET). The HS-FET keeps on for a fixed turn-on time. The fixed on time is determined by the input voltage, output voltage and selected switching frequency. After the on period elapses, the HS-FET turns off. It turns on again when FB drops below the superimposed COMP. By repeating this operation, the MPQ8633A regulates the output voltage. The integrated low-side MOSFET (LS-FET) turns on when the HS-FET is in its off state to minimize conduction loss. A dead short occurs between VIN and PGND if both the HS-FET and the LS-FET are turned on at the same time (shoot-through). In order to avoid shoot-through, a dead time (DT) is generated internally between the HS-FET off and the LS-FET on period or the LS-FET off and the HS-FET on period.

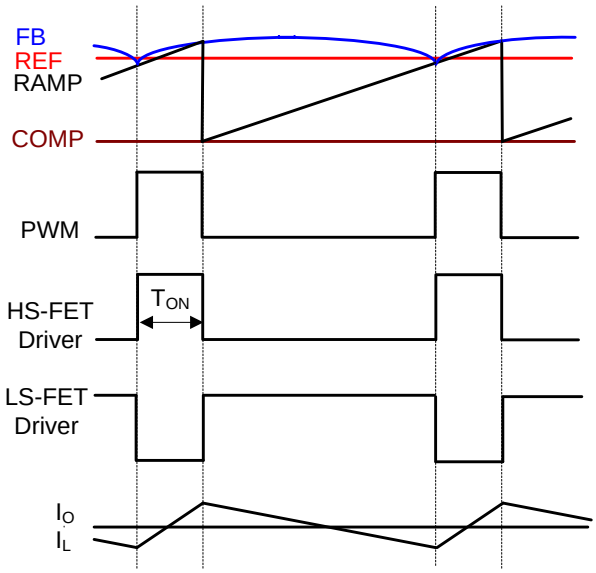

Figure 3—Heavy-load operation (PWM)

CCM Operation

Continuous conduction mode (CCM) occurs when the output current is high, and the inductor current is always above zero amps (see Figure 2). The MPQ8633A can also be configured to operate in forced CCM operation when the output current is low (See Mode Selection section for details).

In CCM operation, the switching frequency is fairly constant (PWM mode), hence the output ripple keeps almost the same throughout the whole load range.

Pulse Skip Operation

At light load condition, the MPQ8633A can be configured to work in pulse skip mode to optimize the efficiency. When the load decreases, the inductor current will decrease as

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well. Once the inductor current reaches zero, the part transitions from CCM to pulse skip mode if the MPQ8633A is configured so (see Mode Selection section for details).

Figure 4 shows pulse skip mode operation at light-load condition. When FB drops below superimposed COMP, the HS-FET turns on for a fixed interval. When the HS-FET turns off, the LS-FET turns on until the inductor current reaches zero. In pulse skip mode operation, the FB does not reach superimposed COMP when the inductor current approaches zero. The LS-FET driver turns into tri-state (high Z) when the inductor current hits zero. A current modulator takes over the control of the LS-FET and limits the inductor current to less than -1mA. Hence, the output capacitors discharge slowly to PGND through the LS-FET. At light load condition, the HS-FET is not turned on as frequently in pulse skip mode as it is in forced CCM. As a result, the efficiency in pulse skip mode is improved greatly, comparing with that in forced CCM operation.

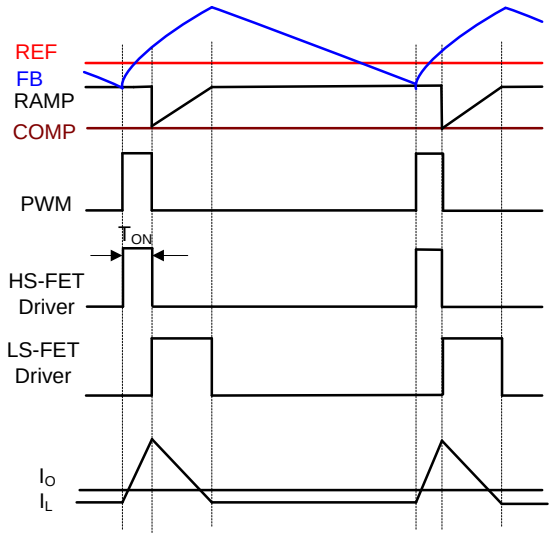

Figure 4—Pulse Skip at Light-load

As the output current increases from the light-load condition, the time period within which the current modulator regulates becomes shorter. The HS-FET is turned on more frequently. Hence, the switching frequency increases accordingly. The output current reaches the critical level when the current modulator time is zero. The critical level of the output current is determined with Equation (1):

$$I_{OUT} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times L \times F_{SW} \times V_{IN}} \quad (1)$$

Where F_{SW} is the switching frequency.

The part enters PWM mode once the output current exceeds the critical level. After that, the switching frequency stays fairly constant over the output current range.

The MPQ8633A can be configured to operate in forced CCM even in a light-load condition. See Table 1 for MODE configuration.

Mode Selection

The MPQ8633A provides both forced CCM operation and pulse skip mode operation in a light-load condition. The MPQ8633A has three options for switching frequency selection. Selecting the operation mode under light load condition and the switching frequency is done by choosing the resistance value of the resistor connected between MODE and AGND or VCC (see Table 1).

Table 1—MODE selection

MODE	Light-Load Mode	Switching Frequency
VCC	Pulse skip	600 KHz
243 kΩ (±20%) to GND	Pulse skip	800 KHz
121 kΩ (±20%) to GND	Pulse skip	1000 KHz
GND	Forced CCM	600 KHz
30.1 kΩ (±20%) to GND	Forced CCM	800 KHz
60.4 kΩ (±20%) to GND	Forced CCM	1000 KHz

Soft Start (SS)

The minimum soft-start time is limited at 1ms. It can be increased by adding a SS capacitor between TRK/REF and RGND.

The total SS capacitor value can be determined with Equation (2) and (3):

$$C_{SS}(nF) = \frac{t_{ss}(ms) \times 36\mu A}{0.6(V)} \quad (2)$$

$$C_{SS} = C_{SS1} + C_{SS2} \quad (3)$$

where C_{SS2} is recommended to be minimum of 22nF.

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Output Voltage Tracking and Reference

The MPQ8633A provides an analog input pin (TRK/REF) to track another power supply or accept external reference. When an external voltage signal is connected to TRK/REF, it acts as a reference for the MPQ8633A output voltage. The FB voltage follows this external voltage signal exactly; the soft-start settings are ignored. The TRK/REF input signal can be in the range of 0.3V to 1.4V. During the initial start-up, the TRK/REF needs to reach 600mV or above first to ensure proper operation. After that, it can be any value between 0.3V and 1.4V.

Pre-Bias Start-Up

The MPQ8633A has been designed for a monotonic start-up into pre-biased loads. If the output is pre-biased to a certain voltage during start-up, the IC disables switching for both the high-side and low-side MOSFETs until the voltage on the TRK/REF capacitor exceeds the sensed output voltage at FB. Before TRK/REF voltage reaches pre-biased FB level, if the BST voltage (from BST to SW) is lower than 2.3V, the LS-FET is turned on to allow the BST voltage to be charged through VCC. The LS-FET is turned on for very narrow pulses, so the drop in pre-biased level is negligible.

Output Voltage Discharge

When the MPQ8633A is disabled through EN, it enables the output voltage discharge mode. This causes both the HS-FET and the LS-FET to latch off. A discharge FET connected between SW and PGND is turned on to discharge the output voltage. The typical switch on resistance of this FET is about 80Ω. Once the FB voltage drops below 10%*REF, the discharge FET is turned off.

Current Sense and Over-Current Protection (OCP)

The MPQ8633A features an on-die current sense and a programmable positive current limit threshold.

The current limit is active when the MPQ8633A is enabled. During the LS-FET on state, the SW current (inductor current) is sensed and mirrored to CS with the ratio of G_{CS}. By using a resistor (R_{CS}) from CS to AGND, the V_{CS} voltage is proportional to the SW current cycle-by-cycle. The HS-FET is only allowed to turn on when the V_{CS} voltage is below the internal OCP voltage threshold V_{OCP} (during the LS-FET on state) to limit the SW valley current cycle-by-cycle.

Equation (4) calculates the current limit threshold setting from R_{CS}:

$$R_{CS}(\Omega) = \frac{V_{OCP}}{G_{CS} \times (I_{LIM} - \frac{(V_{IN} - V_O) \times V_O}{V_{IN}} \times \frac{1}{2 \times L \times f_s})} \quad (4)$$

Where,

V_{OCP} =1.2 V,

G_{CS} = 20 μA/A, and

I_{LIM} = the desired output current limit.

The OCP HICCUP is active 3ms after the MPQ8633A is enabled, Once OCP HICCUP is active, if the MPQ8633A detects over-current condition for consecutive 31 cycles, or if the FB drops below under-voltage protection (UVP) threshold, it enters HICCUP mode. In HICCUP mode, the MPQ8633A latches off the HSFET immediately, and latches off LSFET after ZCD is detected. Meanwhile, the TRK/REF capacitor is also discharged. After about 11ms, the MPQ8633A will try to soft start automatically. If the over-current condition still holds after 3ms of running, the MPQ8633A repeats this operation cycle until the over-current condition disappears, and the output voltage rises smoothly back to the regulation level.

Negative Inductor Current limit

When the LS-FET detects a -9A current, the part turns off the LS-FET for 200ns to limit the negative current.

Output Sinking Mode (OSM)

The MPQ8633A employs output sinking mode (OSM) to regulate the output voltage to the targeted value. When the FB voltage is higher than 104%*REF but is below the OVP threshold, it triggers OSM. During OSM operation, the LS- FET remains on until it hits the -5.5A negative current limit.

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Upon hitting -5.5A, the LS-FET is momentarily turned off for 200ns and is then turned on again. The MPQ8633A keeps this operation until the FB drops below 102%*REF. Once it does, the MPQ8633A exits OSM after 15 consecutive cycles of forced CCM.

Over-Voltage Protection (OVP)

The MPQ8633A monitors the output voltage by connecting FB to the tap of the output voltage feedback resistor divider to detect an over-voltage condition. This provides latch-off OVP mode.

If the FB voltage exceeds 116% of the REF voltage, it enters latch-off OVP mode. The HS-FET latches off and PGOOD latches low until power recycle of VCC or EN. Meanwhile, the LS-FET remains on until it hits the low-side negative current limit (NOCP). Once it hits NOCP, the LS-FET is momentarily turned off for 200ns and is then turned on again. The MPQ8633A keeps this operation to try to bring down the output voltage. When the FB voltage drops below 50% of the REF voltage, the LS-FET is turned off for pulse skip mode, and keeps turning on for forced CCM operation. If FB rises back to more than 116% of the REF voltage, the LS-FET turns on again with NOCP until FB drops back below 50% of the REF voltage. It needs power recycle of the EN or VIN to clear the OVP fault.

The OVP function is enabled after TRK/REF reaches 600mV.

Over-Temperature Protection (OTP)

The MPQ8633A has over-temperature protection (OTP). The IC monitors internally the junction temperature. If the junction temperature exceeds the threshold value (160ºC, typically), the converter shuts off and discharge the TRK/REF capacitors. This is a non-latch protection. There is about 30ºC hysteresis. Once the junction temperature drops to about 130ºC, it initiates a soft start.
The OTP function is effective once the MPQ8633A is enabled.

Output Voltage Setting and Remote Output Voltage Sensing

First, choose a value for R_{FB1}. Then R_{FB2} can be determined with Equation (5):

$$R_{FB2}(k\Omega) = \frac{V_{REF}}{V_O - V_{REF}} \times R_{FB1}(k\Omega) \quad (5)$$

To optimize the load transient response, a feed-forward capacitor (C_{FF}) is recommended in parallel with R_{FB1}. R_{FB1} and C_{FF} add an extra zero to the system, which improves loop response. R_{FB1} and C_{FF} are selected so that the zero formed by R_{FB1} and C_{FF} is between 5kHz and 40kHz. See Equation (6):

$$f_Z = \frac{1}{2\pi \times R_{FB1} \times C_{FF}} \quad (6)$$

Power Good (PGOOD)

The MPQ8633A has a power good (PGOOD) output. PGOOD is the open-drain of a MOSFET. Connect PGOOD to VCC or another external voltage source (less than 3.6V) through a pull-up resistor (10kΩ, typically). After applying the input voltage, the MOSFET turns on, so PGOOD is pulled to GND before TRK/REF is ready. After the FB voltage reaches 92.5% of the REF voltage, PGOOD is pulled high after a 0.8ms delay.

When the FB voltage drops to 80% of the REF voltage or exceeds 116% of the nominal REF voltage, PGOOD is latched low. PGOOD can only be pulled high again after a new SS.

If the input supply fails to power the MPQ8633A, PGOOD is clamped low even though PGOOD is tied to an external DC source through a pull-up resistor. The relationship between the PGOOD voltage and the pull-up current is shown in Figure 5 below:

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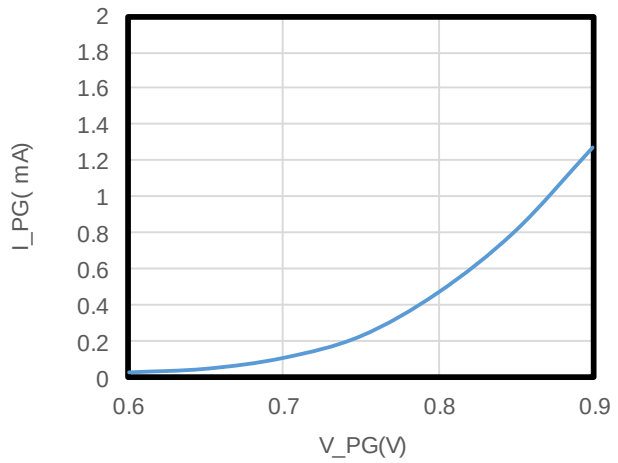

Figure 5—PGOOD clamped voltage v.s. pull-up current

EN Configuration

The MPQ8633A turns on when EN goes high, and it turns off when EN goes low. The EN pin can't be left floating for proper operation. It can be driven by an analog or digital control logic signal to enable/disable the MPQ8633A.

The MPQ8633A provides accurate EN thresholds, so a resistor divider from VIN to AGND can be used to program the input voltage at which the MPQ8633A is enabled.

This is highly recommended for the application where there is no dedicated EN control logic signal, to avoid possible UVLO bouncing during power up and power down. The resistor divider values can be determined by equation (7):

$$V_{IN_START}(V) = VIH_{EN} \times \frac{R_{UP} + R_{DOWN}}{R_{DOWN}} \quad (7)$$

VIH_{EN}=1.22V (typical)

R_{UP} and R_{DOWN} should be chosen that VEN doesn't exceed 3.6V when VIN reaches the maximum value.

The EN can also be directly connected to VIN through a pull-up resistor (R_{UP}). But the R_{UP} should be chosen that the maximum current going to EN is 50μA. A easy calculation of the RUP is given in equation (8):

$$R_{UP}(K\Omega) = \frac{V_{INMAX}(V)}{0.05(mA)} \quad (8)$$

Enable (EN) Thresholds

The MPQ8633A has two EN thresholds: the LDO EN rising threshold, and the EN input rising threshold. During start-up, once EN reaches the LDO EN rising threshold (typically 0.7V), the internal LDO is enabled, and VCC starts to increase. When EN reaches the EN input rising threshold, the part is enabled and starts to switch (see Figure 6).

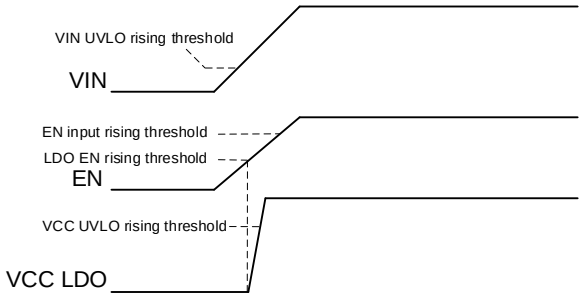

Figure 6—Start-Up Sequence with Internal LDO and Two EN Thresholds

Power Sequence with External VCC Bias

The MPQ8633A supports an external 3.3V VCC bias. When using the external VCC bias, it is recommended to apply the external VCC bias before reaching either the V_{IN} UVLO rising threshold or LDO EN rising threshold. If the external VCC bias is applied after reaching both the V_{IN} UVLO rising threshold and LDO EN rising threshold, then the LDO has an output and provides power to the load, which is supplied by the external VCC. Depending on the load condition of the external VCC, the LDO might be overloaded until the external VCC bias is applied. For the same reason, it is recommended to shut down the external VCC bias after reaching either the V_{IN} UVLO falling threshold or LDO EN falling threshold.

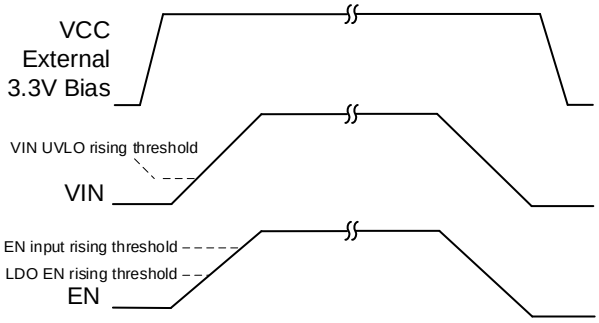

Figure 7—Start-Up Sequence with External VCC Bias

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APPLICATION INFORMATION

Input Capacitor

The input current to the step-down converter is discontinuous, and therefore, requires a capacitor to supply the AC current to the step-down converter while maintaining the DC input voltage. Use ceramic capacitors for best performance. During layout, place the input capacitors as close to VIN pin as possible.

The capacitance can vary significantly with temperature. Use capacitors with X5R and X7R ceramic dielectrics because they are fairly stable over a wide temperature range and they offer very low ESR.

The capacitors must have a ripple current rating that exceeds the converter's maximum input ripple current. Estimate the input ripple current with Equation (9) and Equation (10):

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (9)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, where:

$$I_{CIN} = \frac{I_{OUT}}{2} \quad (10)$$

For simplification, choose an input capacitor with an RMS current rating that exceeds half the maximum load current.The input capacitor value determines the converter input voltage ripple. If there is an input voltage ripple requirement in the system, select an input capacitor that meets the specification.

Estimate the input voltage ripple with Equation (11) and Equation (12):

$$\Delta V_{IN} = \frac{I_{OUT}}{F_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (11)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, where:

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{F_{SW} \times C_{IN}} \quad (12)$$

Output Capacitor

The output capacitor maintains the DC output voltage. Use POSCAP or ceramic capacitors. Estimate the output voltage ripple with Equation (13):

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times F_{SW} \times C_{OUT}}) \quad (13)$$

When using ceramic capacitors, the capacitance dominates the impedance at the switching frequency. The capacitance also dominates the output voltage ripple. For simplification, estimate the output voltage ripple with Equation (14):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times F_{SW}^{2} \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (14)$$

The ESR dominates the switching frequency impedance for the POSCAP capacitors. For simplification, the output ripple can be approximated with Equation (15):

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (15)$$

Inductor

The inductor supplies constant current to the output load while being driven by the switching input voltage. A larger value inductor results in less ripple current and lower output ripple voltage but has a larger physical size, a higher series resistance, and/or a lower saturation current. Generally, select an inductor value that allows the inductor peak-to-peak ripple current to be 30 percent to 40 percent of the maximum switch current limit. Also, design for a peak inductor current that is below the maximum switch current limit. Calculate the inductance value using Equation (16):

$$L = \frac{V_{OUT}}{F_{SW} \times \Delta I_{L}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (16)$$

Where ΔI_L is the peak-to-peak inductor ripple current.

Choose an inductor that will not saturate under the maximum inductor peak current. The peak inductor current can be calculated with Equation (17):

$$I_{LP} = I_{OUT} + \frac{V_{OUT}}{2 \times F_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (17)$$

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PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For optimal performance, refer to Figure 8 and Figure 9 and follow the guidelines below:

1. Place the input MLCC capacitors as close to the VIN and PGND pins as possible. The major MLCC capacitors should be placed on the same layer as the MPQ8633A. Maximize the VIN and PGND copper plane to minimize the parasitic impedance.
2. A 0402 capacitor with a minimum 1µF value is required. Place the capacitor on the right side of the IC. VIN is extended to the right side to connect the capacitor. At least two 20/10mil vias should be placed on the ground side of the capacitor to the inner solid ground plane.
3. Place PGND vias (as many as possible and as close to PGND as possible) to minimize both parasitic impedance and thermal resistance.
4. Place the VCC decoupling capacitor close to the device. Connect AGND and PGND at the point of the VCC capacitor's ground connection.
5. Place the BST capacitor as close to BST and SW as possible. Use traces with a width of 20mil or wider to route the path. It is recommended to use a 0.1µF to 1µF bootstrap capacitor.
6. Place the REF capacitor close to TRK/REF to RGND.
7. Place via at least 10mm away from the positive side of the first input decoupling capacitor close to the IC if it must be placed on the PGOOD pad.
8. Place C_{OL} between the output sense lines and close to the device. It is recommended to use a 1nF to 100nF capacitor.
9. Do not place vias on the V_{OSENSE}± trace.
10. Use a 10Ω to 49.9Ω for R_{PG}, and a 1nF C_{PG}.
11. The feedforward resistor (R_{ff}) is recommended to be 1/10 of the top feedback resistor (R_{FB1}).

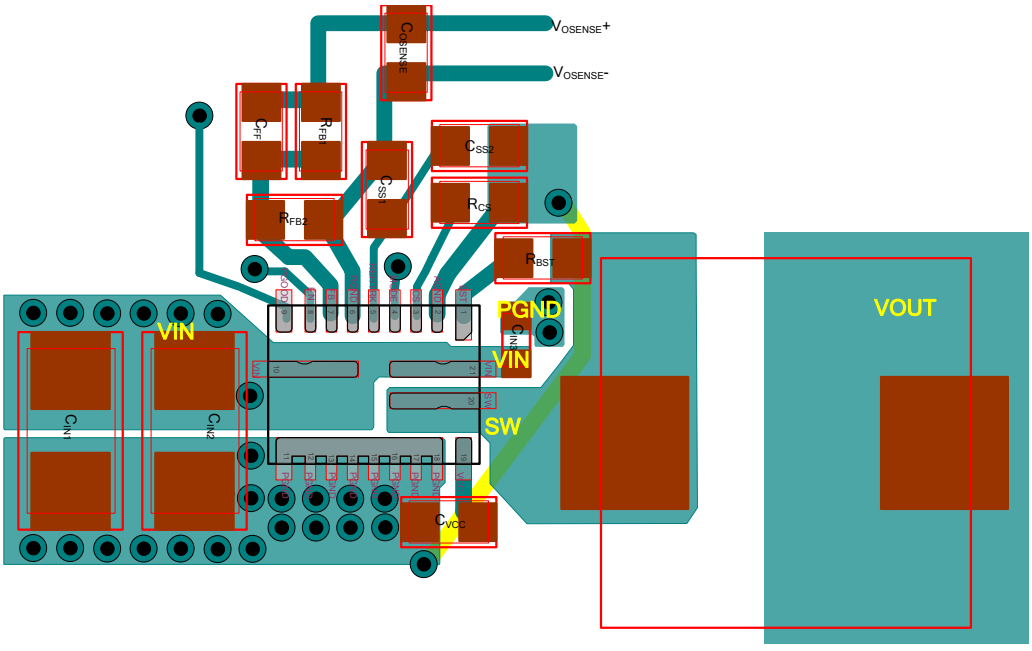

Figure 8—Recommended PCB layout (QFN-21)

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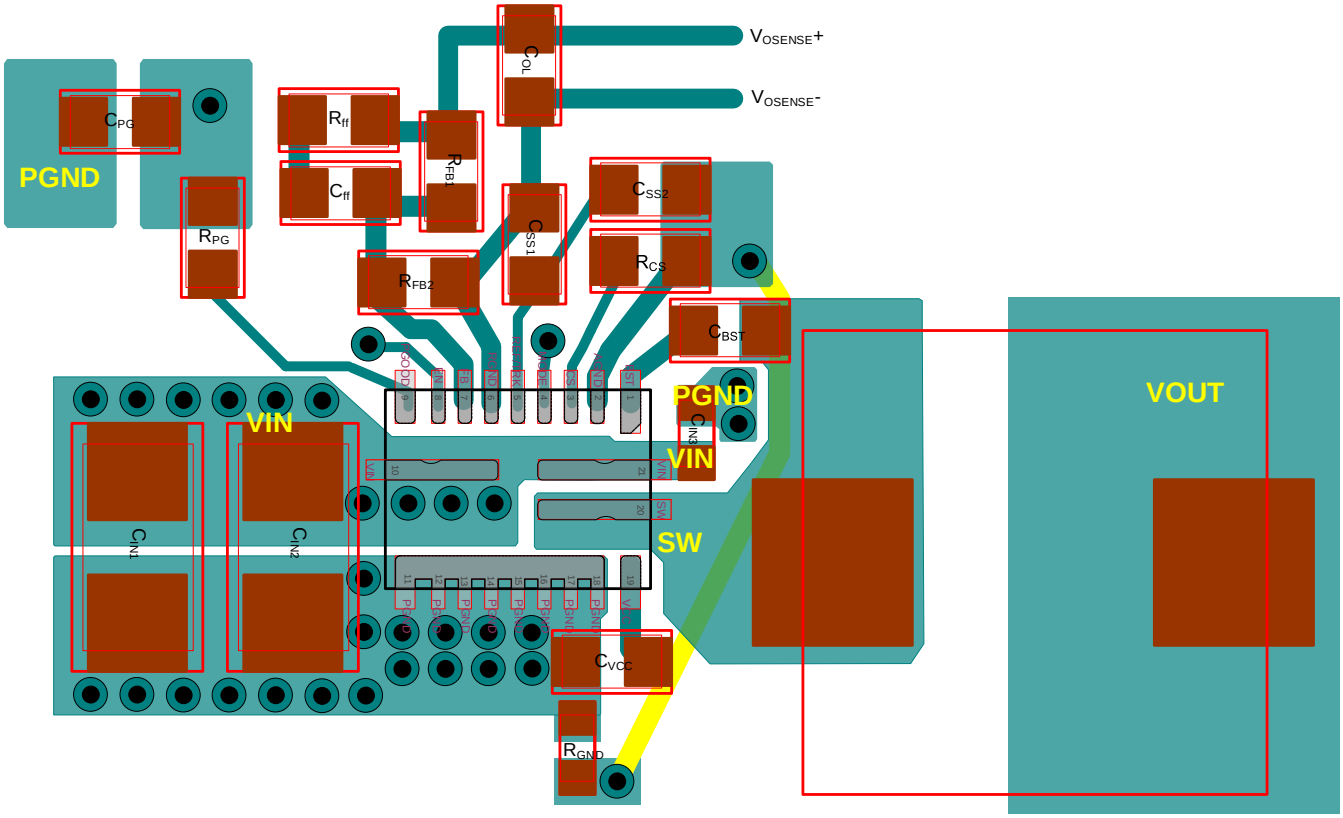

Figure 9—Recommended PCB layout (QFN-20)
(Not recommended for new design)

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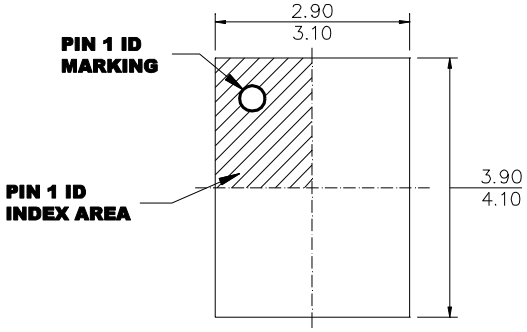
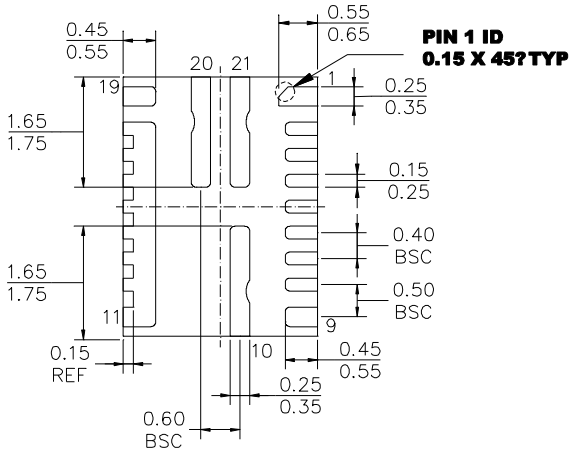
PACKAGE INFORMATION

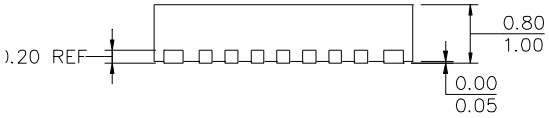
QFN-21 (3mm x 4mm)



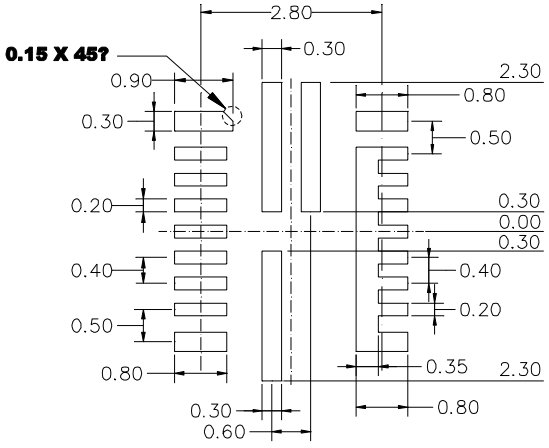
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) LAND PATTERN OF PIN1,9,10,11,19,20 AND 21 HAVE THE SAME WIDTH.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

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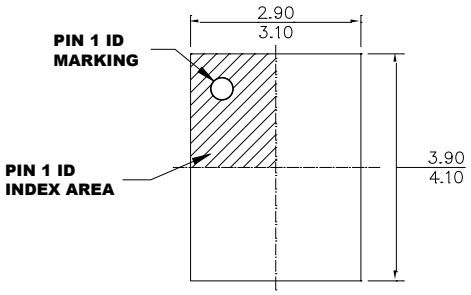
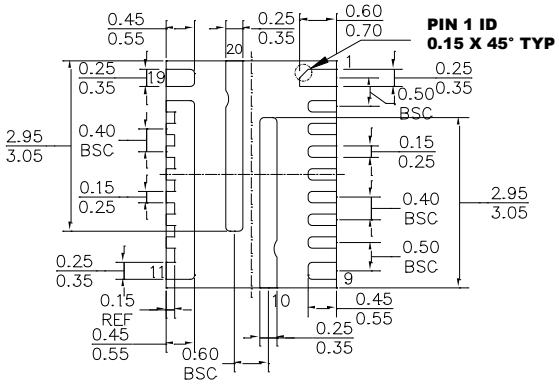
PACKAGE INFORMATION

QFN-20 (3mm x 4mm)

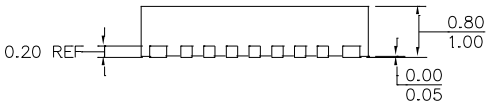
(Not recommended for new design)



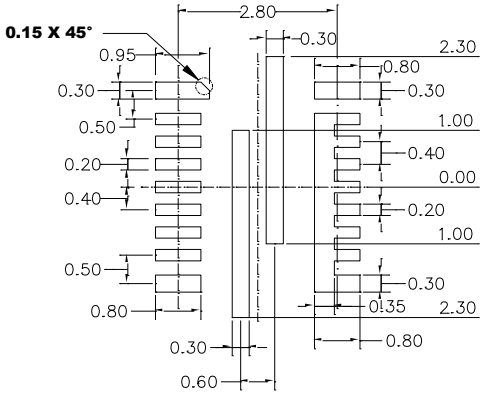
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

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REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	7/31/2015	Initial Release	-
1.01	06/29/2016	Updated the following sections in the Absolute Maximum Ratings section: • Updated V_{CC} to V_{CC}, EN • Deleted EN current (I_{EN}) and Continuous power dissipation • Recommended Operating Conditions: Added $V_{IN(DC)}$-$V_{SW(DC)}$ and $V_{IN(DC)}$; updated EN current (I_{EN}) to EN Voltage (V_{EN}) • Thermal Resistance: Updated the corresponding note from 5) to 4) • Updated the numbering of note 1a to note 2 • Removed the previous note 2, note 3, and note 4 • Added note 3, note 4, and 5	4
		Updated the numbering of note 5 to note 6	6
1.02	08/03/2016	Updated the Thermal Resistance in the Absolute Maximum Rating section	4
1.03	08/21/2017	Updated the Electrical Characteristics section	5–6
		Made overall copyedits.	All
1.04	03/02/2018	Made the following updates to the Electrical Characteristics section: • Power good low-level output voltage • PG clamped voltage vs current based on the spreadsheet	6
1.05	05/23/2018	Updated the GL package to NFRND	All
1.06	8/27/2019	Updated the Applications section and TPC1	1
		Added Equation (3)	14
		Updated the PCB Layout Guidelines section	20
1.1	3/26/2024	Updated the following sections in the Typical Application image: • PGOOD: Added R_{PG} and C_{PG} • VCC: Added R_{GND} • FB: Added R_{ff} • RGND: Added C_{OL} between R_{FB1} and RGND	2
		Updated the following sections in the Absolute Maximum Ratings section: • Updated V_{SW} (DC), V_{SW} (25ns), and V_{BST} • Deleted V_{SW} (25 ns) • Added V_{IN} - V_{SW} (DC), V_{IN} - V_{SW} (25ns), and V_{BST} - V_{SW} (25ns) • Recommended Operating Conditions: Deleted $V_{IN(DC)}$ - $V_{SW(DC)}$ and $V_{SW(DC)}$ • Thermal Resistance: Updated the corresponding note from 5) to 4) • Deleted note 4 • Made minor formatting edits and copyedits	4

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REVISION HISTORY *(continued)*

		Updated the f_Z range from between 20kHz and 60kHz to between 5kHz and 40kHz in the Output Voltage Setting and Remote Output Voltage Sensing section	17
		Added the Enable (EN) Thresholds and Power Sequence with External VCC Bias sections, as well as Figure 6 and Figure 7; made a minor formatting edit to the figure label for Figure 5	18
		Updated the figure numbering for Figure 8 (previously Figure 6) and Figure 9 (previously Figure 7)	20–21
		Updated step 8, and added step 9, step 10, and step 11 in the PCB Layout Guidelines section	20
		Updated the placement and top layer PCB in Figure 9	21

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