MPQ8632D-6, MPQ8632D-12

High Efficiency, 6A/12A, 18V Synchronous Step-down Converter

The Future of Analog IC Technology

END OF LIFE, REFER TO MPQ8632-6 OR MPQ8632-12

DESCRIPTION

The MPQ8632D-6/MPQ8632D-12 is a fully integrated high frequency synchronous rectified step-down switch mode converter. It offers a very compact solution to achieve 6A/12A output current over a wide input supply range with excellent load and line regulation. The MPQ8632D-6/MPQ8632D-12 operates at high efficiency over a wide output current load range.

The MPQ8632D-6/MPQ8632D-12 uses Constant-On-Time (COT) control mode to provide fast transient response and ease loop stabilization.

An external resistor programs the operating frequency from 200kHz to 1MHz and the frequency keeps nearly constant as input supply varies with the feedforward compensation.

The default under voltage lockout threshold is internally set at 4.1V, but a resistor network on the enable pin can increase this threshold. An open drain power good signal indicates that the output is within nominal voltage range.

The MPQ8632D-6/MPQ8632D-12 employs a programmable soft start and shut-down scheme. With the soft shut-down feature, it discharges the output voltage smoothly when the enable signal is deserted.

It has fully integrated protection features that include over-current protection, over-voltage protection and thermal shutdown.

The MPQ8632D-6/MPQ8632D-12 requires a minimal number of readily available standard external components and is available in a 3mm×4mm package.

FEATURES

- 2.5V to 18V Operating Input Range with External 5V Bias
- 4.5V to 18V Operating Input Range with Internal Bias
- 6A/12A Output Current
- Low R_{DS}(ON) Internal Power MOSFETs
- Proprietary Switching Loss Reduction Technique
- Adaptive COT for Ultrafast Transient Response
- 0.5% Reference Voltage Over 0°C to 70°C Junction Temperature Range
- Programmable Soft Start and Shut-down Time
- Pre-Bias Start up
- Programmable Switching Frequency from 200kHz to 1MHz
- Non-latch OCP, OVP and Thermal Shutdown
- Output Adjustable from 0.611V to 13V

APPLICATIONS

- Telecom and Networking Systems
- Base Stations
- Servers
- Personal Video Recorders
- Flat Panel Television and Monitors
- Distributed Power Systems

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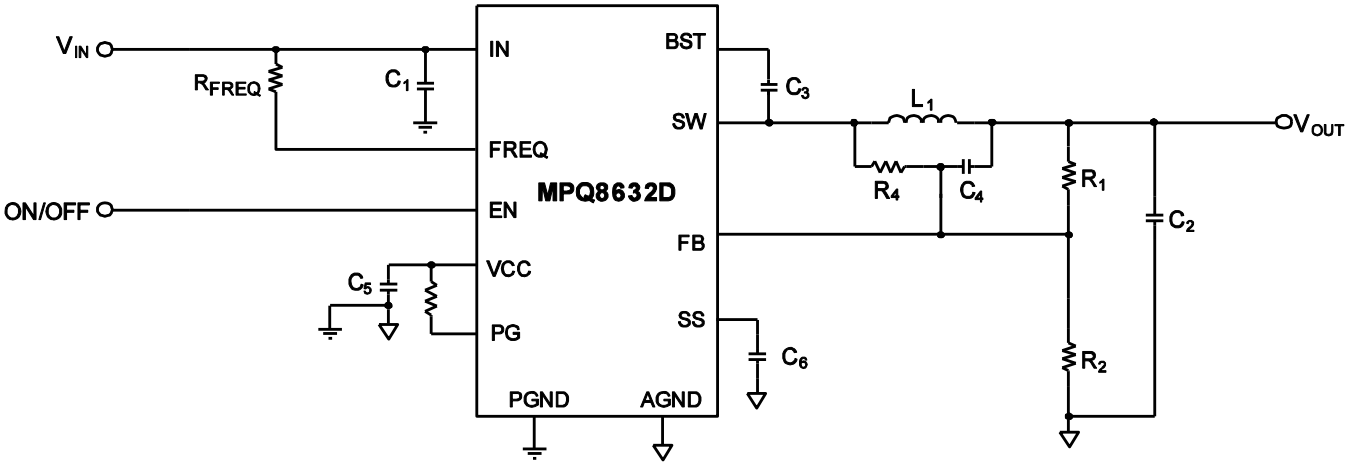
TYPICAL APPLICATION



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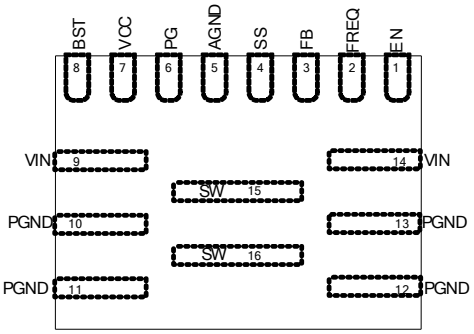
ORDERING INFORMATION

Part Number	Package	Top Marking
MPQ8632DGLE-6*	QFN(3X4mm)	MP8632D 6
MPQ8632DGLE-12	QFN(3X4mm)	MP8632D 12

***** For Tape & Reel, add suffix –Z (e.g. MPQ8632DGLE–6–Z)

PACKAGE REFERENCE

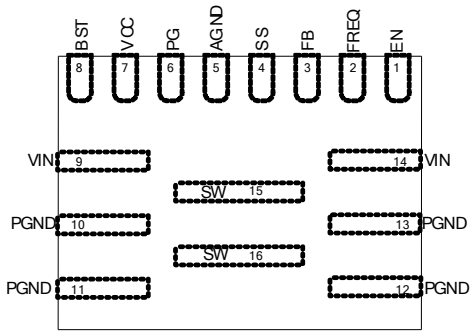
TOP VIEW



Part Number*	Package
MPQ8632DGLE-6	QFN (3x4mm)
Junction Temperature	**Top Marking**
–40°C to +125°C	MP8632D 6

***** For Tape & Reel, add suffix –Z (eg. MPQ8632DGLE-6–Z)

TOP VIEW



Part Number*	Package
MPQ8632DGLE-12	QFN (3x4mm)
Junction Temperature	**Top Marking**
–40°C to +125°C	MP8632D 12

***** For Tape & Reel, add suffix –Z (eg. MPQ8632DGLE-12–Z)

ABSOLUTE MAXIMUM RATINGS (1)

Supply Voltage V_{IN} 21V
V_{SW} ..... -0.3V to V_{IN} + 0.3V
V_{SW} (30ns) ..... -3V to V_{IN} + 3V
V_{BST} ..... V_{SW} + 6V
Enable Current I_{EN} (2) 2.5mA
All Other Pins ..... –0.3V to +6V
Continuous Power Dissipation (T_A=+25°) (3)
QFN3X4 ..... 2.7W
Junction Temperature ..... 150°C
Lead Temperature ..... 260°C
Storage Temperature ..... -65°C to +150°C

Recommended Operating Conditions (4)

Supply Voltage V_{IN} ..... 4.5V to 18V
Output Voltage V_{OUT} ..... 0.611V to 13V
Enable Current I_{EN} 1mA
Operating Junction Temp. (T_J). -40°C to +125°C

Thermal Resistance (5) θ_{JA} θ_{JC}

QFN (3x4mm) ..... 46 ..... 9 ..... °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) Refer to the section “Configuring the EN Control”.
3) The maximum allowable power dissipation is a function of the maximum junction temperature T_J(MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D(MAX)=(T_J(MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) The device is not guaranteed to function outside of its operating conditions.
5) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_J = -40°C to +125°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Supply Current						
Supply Current (Shutdown)	I_{IN}	V_{EN} = 0V		0	1	μA
Supply Current (Quiescent)	I_{IN}	V_{EN} = 2V, V_{FB} = 1V	700	860	1000	μA
MOSFET						
High-side Switch On Resistance	HS_{RDS-ON}	MPQ8632DGLE-6 T_J =25°C		28		mΩ
		MPQ8632DGLE-12 T_J =25°C		19.6		mΩ
Low-side Switch On Resistance	LS_{RDS-ON}	MPQ8632DGLE-6, T_J =25°C		15.8		mΩ
		MPQ8632DGLE-12,T_J=25°C		5.2		
Switch Leakage	SW_{LKG}	V_{EN} = 0V, V_{SW} = 0V or 12V		0	10	μA
Current Limit						
Low-side Valley Current Limit(6)	I_{LIMIT_VALLEY}	MPQ8632DGLE-6	6.5	7.5	8.5	A
		MPQ8632DGLE-12	12	15	18	
Low-side Negative Current Limit(6)	$I_{LIMIT_NEGATIVE}$		-4	-2.5	-1	A
Timer						
One-Shot On Time	T_{ON}	R_{FREQ}=453kΩ, V_{OUT}=1.2V		250		ns
Minimum On Time(6)	T_{ON_MIN}		20	30	40	ns
Minimum Off Time(6)	T_{OFF_MIN}		200	360	420	ns
Under-voltage Protection						
UVP Threshold(6)	V_{UVP}		47%	50%	53%	V_{FB}
Reference And Soft Start/Shut-down						
Reference Voltage	V_{REF}	T_J = 0°C to +70°C	608	611	614	mV
		T_J = 0°C to +125°C	605	611	617	mV
		T_J = -40°C to +125°C	602	611	620	mV
Feedback Current	I_{FB}	V_{FB} = 611mV		50	100	nA
Soft Start Charging Current	I_{SS}	V_{SS}=0V	16	20	25	μA
Soft Shut-down Discharging Current	I_{SD}	V_{SS}=0V	6	10	15	μA

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_J = -40°C to +125°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Enable And UVLO						
Enable Input Low Voltage	VIL_{EN}		1.1	1.3	1.5	V
Enable Hysteresis	V_{EN-HYS}			250		mV
Enable Input Current	I_{EN}	V_{EN} = 2V		0		μA
		V_{EN} = 0V		0		
VCC Regulator						
VCC Under Voltage Lockout Threshold Rising	VCC_{Vth}			3.8		V
VCC Under Voltage Lockout Threshold Hysteresis	VCC_{HYS}			500		mV
VCC Regulator	V_{CC}			4.8		V
VCC Load Regulation		Icc=5mA		0.5		%
Power Good						
Power Good High Threshold	$PG_{Vth-Hi-Rise}$	FB from low to high	86%	90%	94%	V_{FB}
	$PG_{Vth-Hi-Fall}$	FB from high to low		109%		V_{FB}
Power Good Low Threshold	$PG_{Vth-Lo-Rise}$	FB from low to high	116%	120%	124%	V_{FB}
	$PG_{Vth-Lo-Fall}$	FB from high to low		85%		V_{FB}
Power Good Lower to High Delay	PG_{Td}			2.5		ms
Power Good Sink Current Capability	I_{OL}	V_{OL}=600mV			12	mA
Power Good Leakage Current	I_{PG_LEAK}	V_{PG} = 3.3V		10		nA
Thermal Protection (6)						
Thermal Shutdown	T_{SD}		150			°C
Thermal Shutdown Hysteresis				25		°C

Note:

6) Guaranteed by design.

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PIN FUNCTIONS

MPQ8632D-6/MPQ8632D-12

PIN #	Name	Description
1	EN	Enable. Digital input that turns the regulator on or off. Drive EN high to turn on the regulator, drive it low to turn it off. Connect EN to IN through a pull-up resistor or a resistive voltage divider for automatic startup. Do not float this pin.
2	FREQ	Frequency Set. Require a resistor connected between FREQ and IN to set the switching frequency. The input voltage and the resistor connected to the FREQ pin determine the ON time. The connection to the IN pin provides line feed-forward and stabilizes the frequency during input voltage's variation.
3	FB	Feedback. Connect to the tap of an external resistor divider from the output to GND to set the output voltage. FB is also configured to realize over-voltage protection (OVP) by monitoring output voltage. MPQ8632D-6 and MPQ8632D-12 provide non-latch OVP mode. Please refer to the section "Over-Voltage-Protection (OVP)". Place the resistor divider as close to FB pin as possible. Avoid using vias on the FB traces.
4	SS	Soft Start/Shut-Down. Connect an external capacitor to program the soft start/shut-down time for the switch mode regulator. The soft start time is the half of the soft shut-down time.
5	AGND	Analog ground. The control circuit reference.
6	PG	Power Good. The output is an open drain signal. Require a 100kΩ typical pull-up resistor to a DC voltage to indicate high if the output voltage exceeds 90% of the nominal voltage. Recommend a 10nF capacitor from PG to GND when the PG pull up resistor is <100kΩ. There is a delay from FB ≥ 90% to PG goes high.
7	VCC	Internal 4.8V LDO Output. Power the driver and control circuits. 5V external bias can disable the internal LDO. Decouple with a ≥ 1μF ceramic capacitor as close to the pin as possible. For best results, use X7R or X5R dielectric ceramic capacitors for their stable temperature characteristics.
8	BST	Bootstrap. Require a capacitor connected between SW and BST pins to form a floating supply across the high-side switch driver.
9, 14	IN	Supply Voltage. Supply power to the internal MOSFET and regulator. The MPQ8632D-6/MPQ8632D-12 operates from a +2.5V to +18V input rail with 5V external bias and a +4.5V to +18V input rail with internal bias. Require an input decoupling capacitor. Connect using wide PCB traces and multiple vias.
10, 11, 12, 13	PGND	System Ground. Reference ground of the regulated output voltage. PCB layout requires extra care. Connect using wide PCB traces.
15, 16	SW	Switch Output. Connect to the inductor and bootstrap capacitor. The high-side switch drives the pin up to the V_{IN} during the PWM duty cycle's ON time. The inductor current drives the SW pin negative during the OFF-time. The low-side switch's ON-resistance and the internal Schottky diode clamp the negative voltage. Connect using wide PCB traces.

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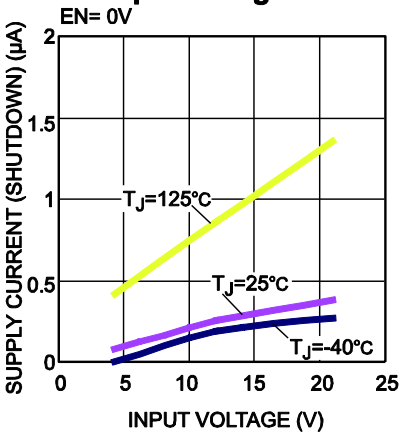
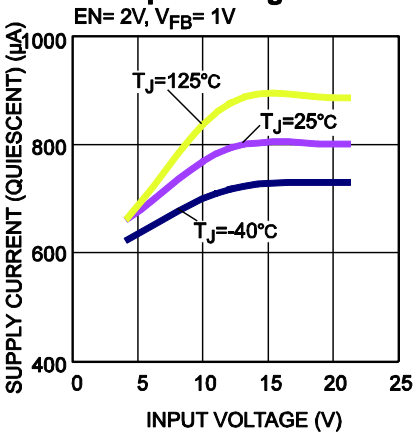
TYPICAL CHARACTERISTICS

MPQ8632DGLE-12, VIN = 12V, V_{OUT} = 1V, L = 1µH, T_A = 25ºC, unless otherwise noted.

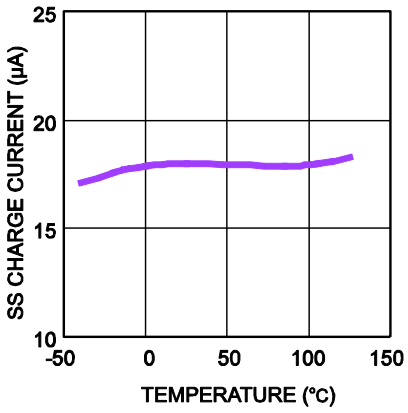
Supply Current (Shutdown) vs. Input Voltage



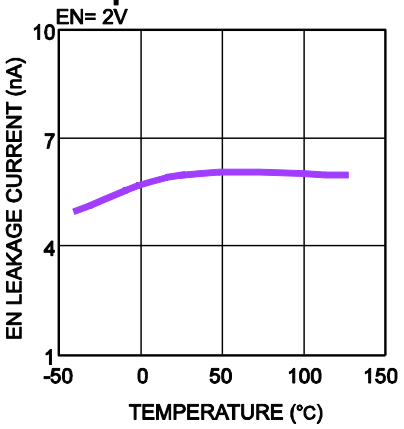
Supply Current (Quiescent) vs. Input Voltage



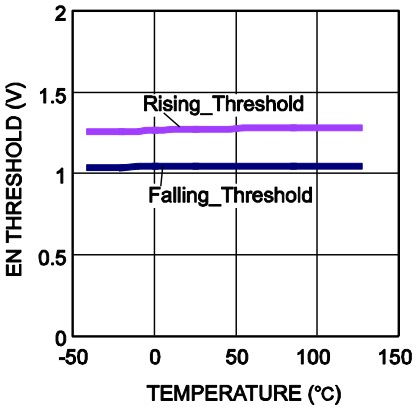
SS Charge Current vs. Temperature



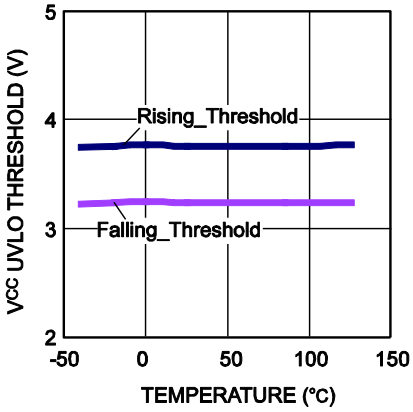
EN Leakage Current vs. Temperature



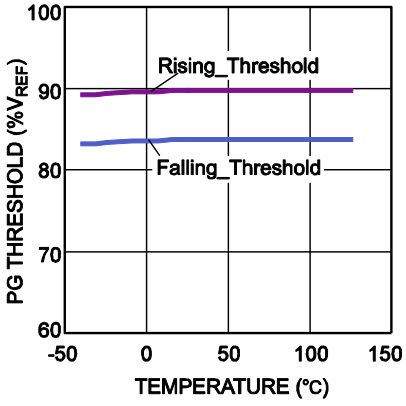
EN Threshold vs. Temperature



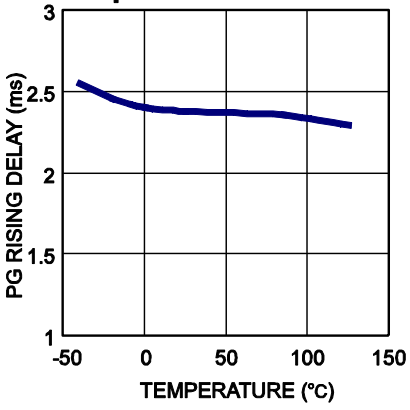
V_{CC} UVLO Threshold vs. Temperature



PG Threshold vs. Temperature



PG Rising Delay vs. Temperature



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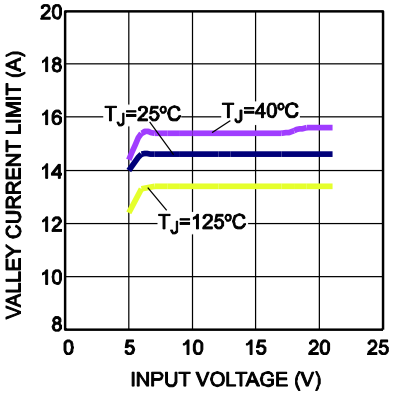
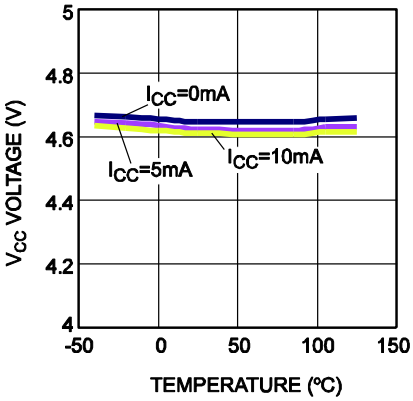
TYPICAL CHARACTERISTICS *(continued)*

MPQ8632DGLE-12, V_{IN} = 12V, V_{OUT} = 1V, L = 1µH, T_A = 25°C, unless otherwise noted.

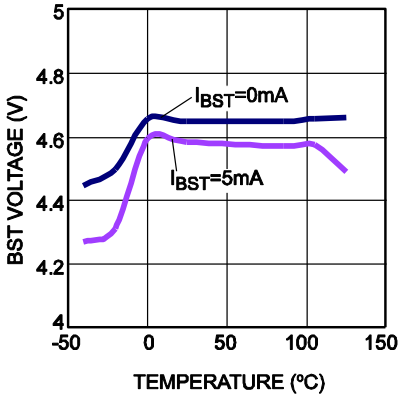
Valley Current Limit vs. Input Voltage



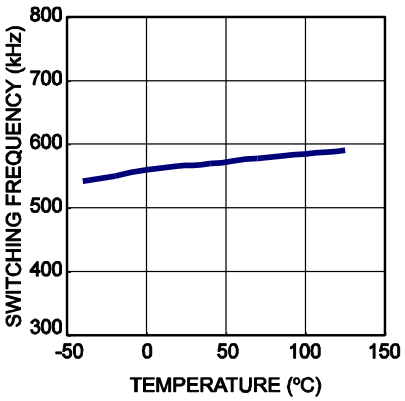
V_{CC} Voltage vs. Temperature



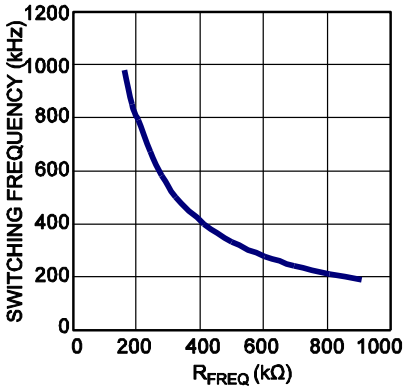
BST Voltage vs. Temperature



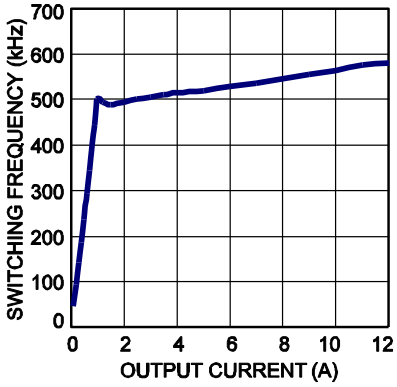
Switching Frequency vs. Temperature
I_{OUT}=6A, R_{FREQ}=332kΩ



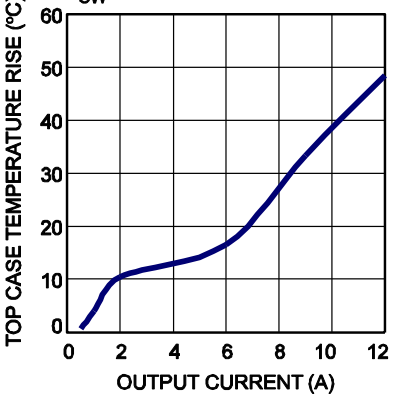
Switching Frequency vs. R_{FREQ}



Switching Frequency vs. Output Current
R_{FREQ}=332kΩ



Case Temperature Rise vs. Output Current
F_{SW}=500kHz



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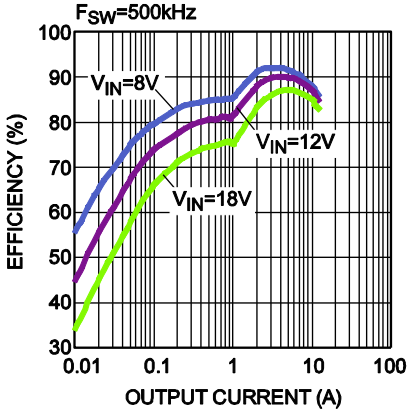
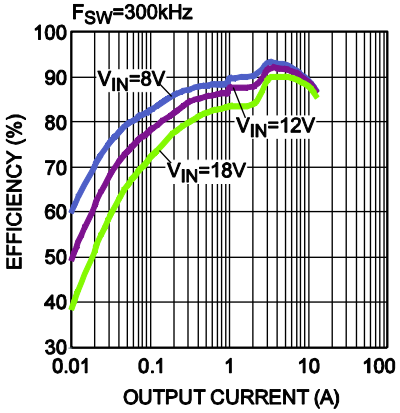
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

MPQ8632DGLE-12, V_{IN} = 12V, V_{OUT} = 1V, L = 1µH, T_A = 25ºC, unless otherwise noted.

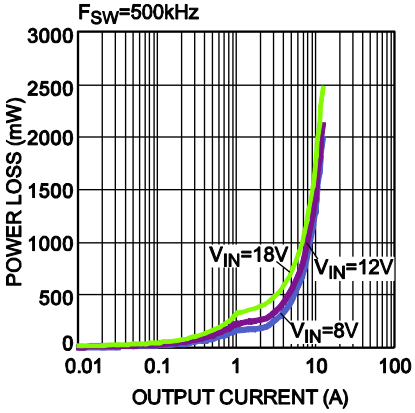
Efficiency vs. Output Current



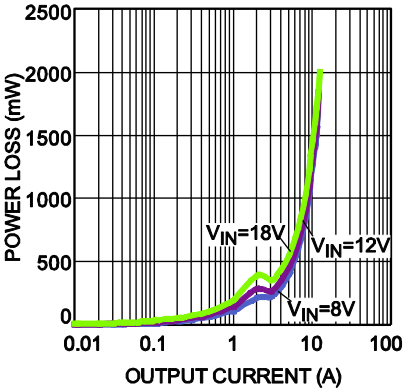
Efficiency vs. Output Current



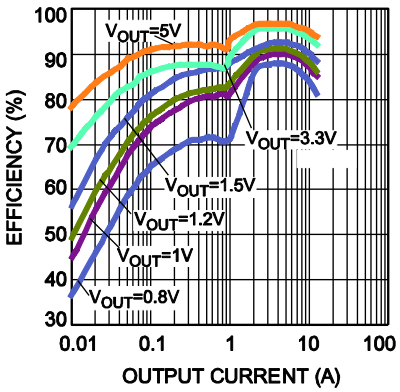
Power Loss vs. Output Current



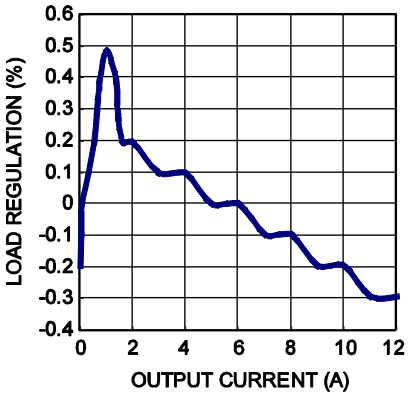
Power Loss vs. Output Current



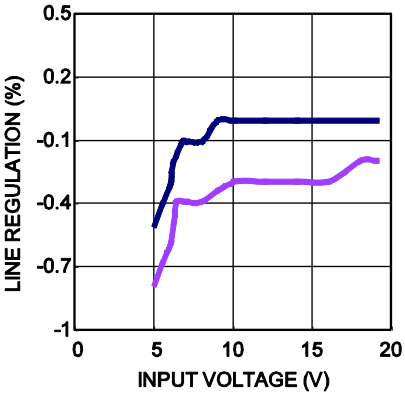
Efficiency vs. Output Current



Load Regulation vs. Output Current



Line Regulation vs. Input Voltage



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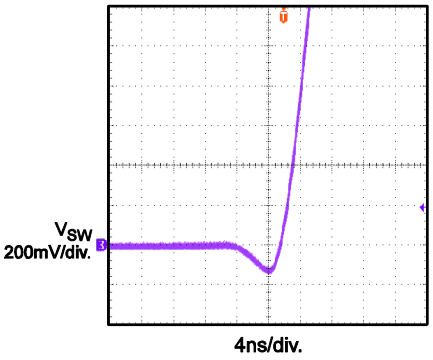
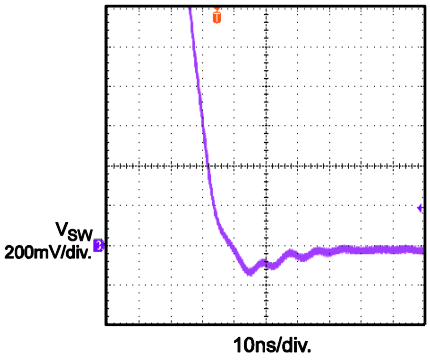
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

MPQ8632DGLE-12, V_{IN}=12V, V_{OUT} =1V, L=1µH, T_A=+25°C, unless otherwise noted.

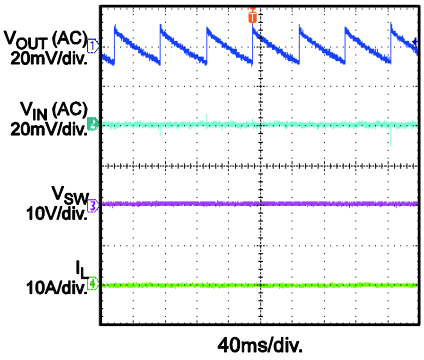
Dead Time (on)
I_{OUT} = 12A



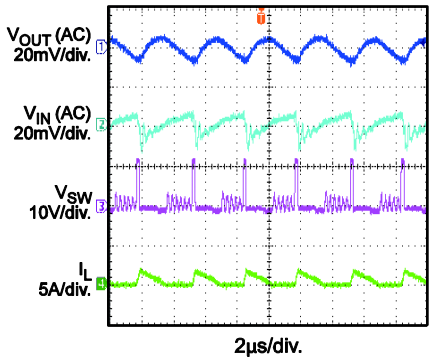
Dead Time (off)
I_{OUT} = 12A



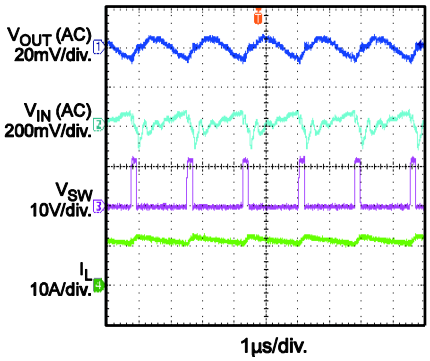
Input/Output Voltage Ripple
I_{OUT} = 0A



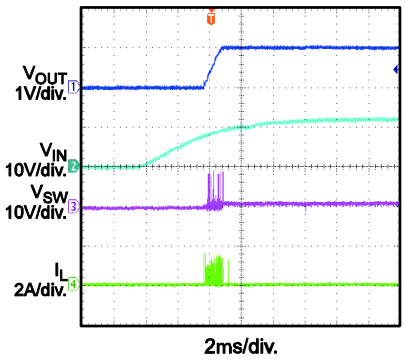
Input/Output Voltage Ripple
I_{OUT} = 0.5A



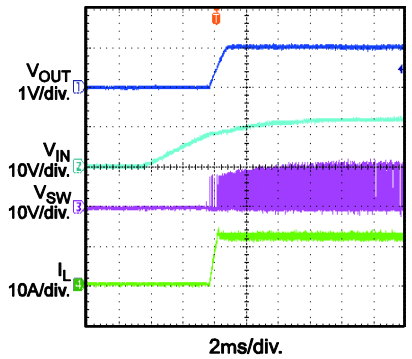
Input/Output Voltage Ripple
I_{OUT} = 12A



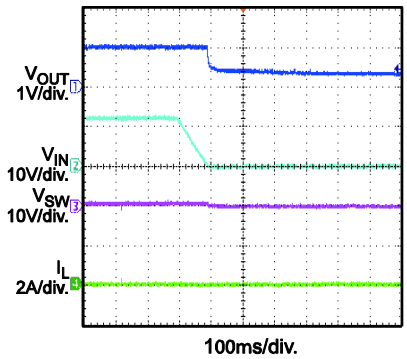
Start Up Through V_{IN}
I_{OUT} = 0A



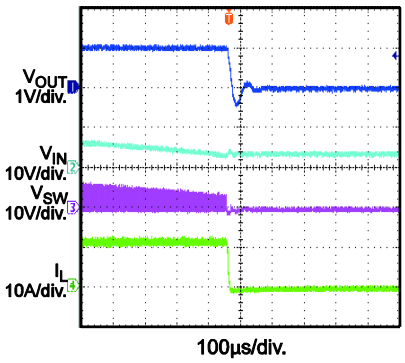
Start Up Through V_{IN}
I_{OUT} = 12A



Shutdown Through V_{IN}
I_{OUT} = 0A



Shutdown Through V_{IN}
I_{OUT} = 12A



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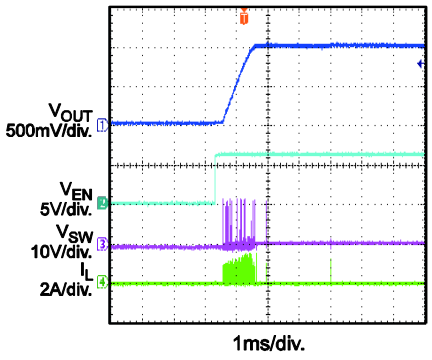
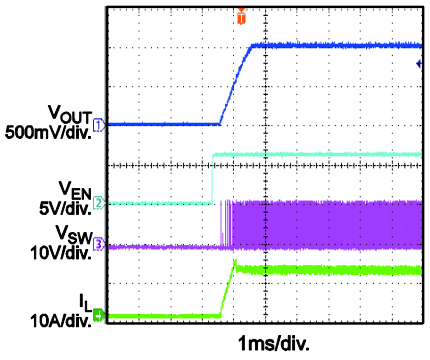
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

MPQ8632DGLE-12, V_{IN}=12V, V_{OUT} =1V, L=1µH, T_A=+25°C, unless otherwise noted.

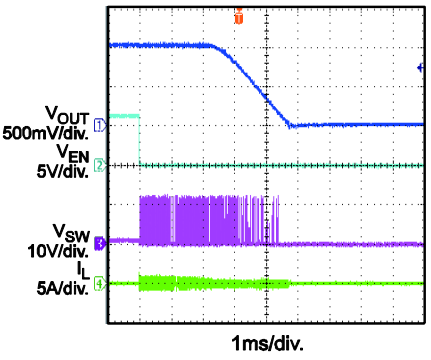
Start up Through EN
I_{OUT} = 0A



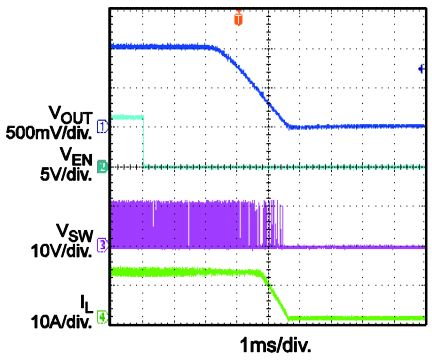
Start up Through EN
I_{OUT} = 12A



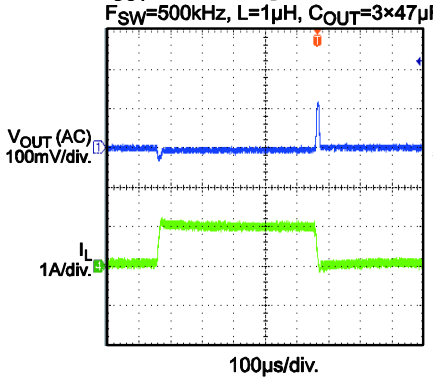
Shutdown Through EN
I_{OUT} = 0A



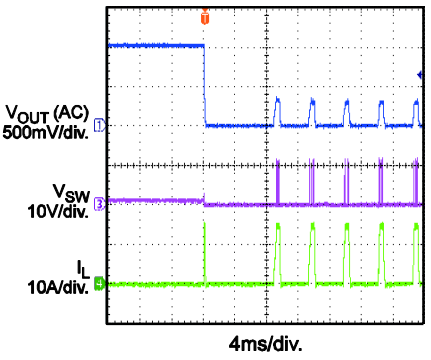
Shutdown Through EN
I_{OUT} = 12A



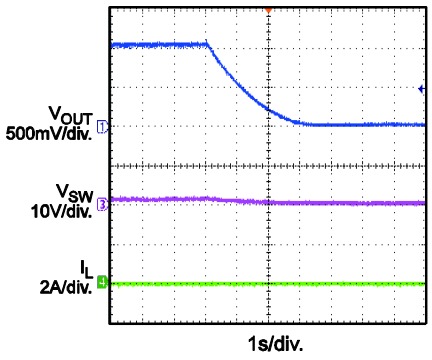
Transient
V_{IN} = 12V, V_{OUT} = 1V,
I_{OUT} = 1.2-10.8A @1.6A/µs,
F_{SW}=500kHz, L=1µH, C_{OUT}=3×47µF



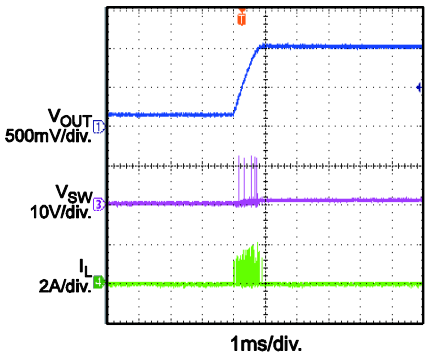
Short Circuit Protection



Thermal Shutdown
I_{OUT} = 0A



Thermal Recovery
I_{OUT} = 0A



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BLOCK DIAGRAM

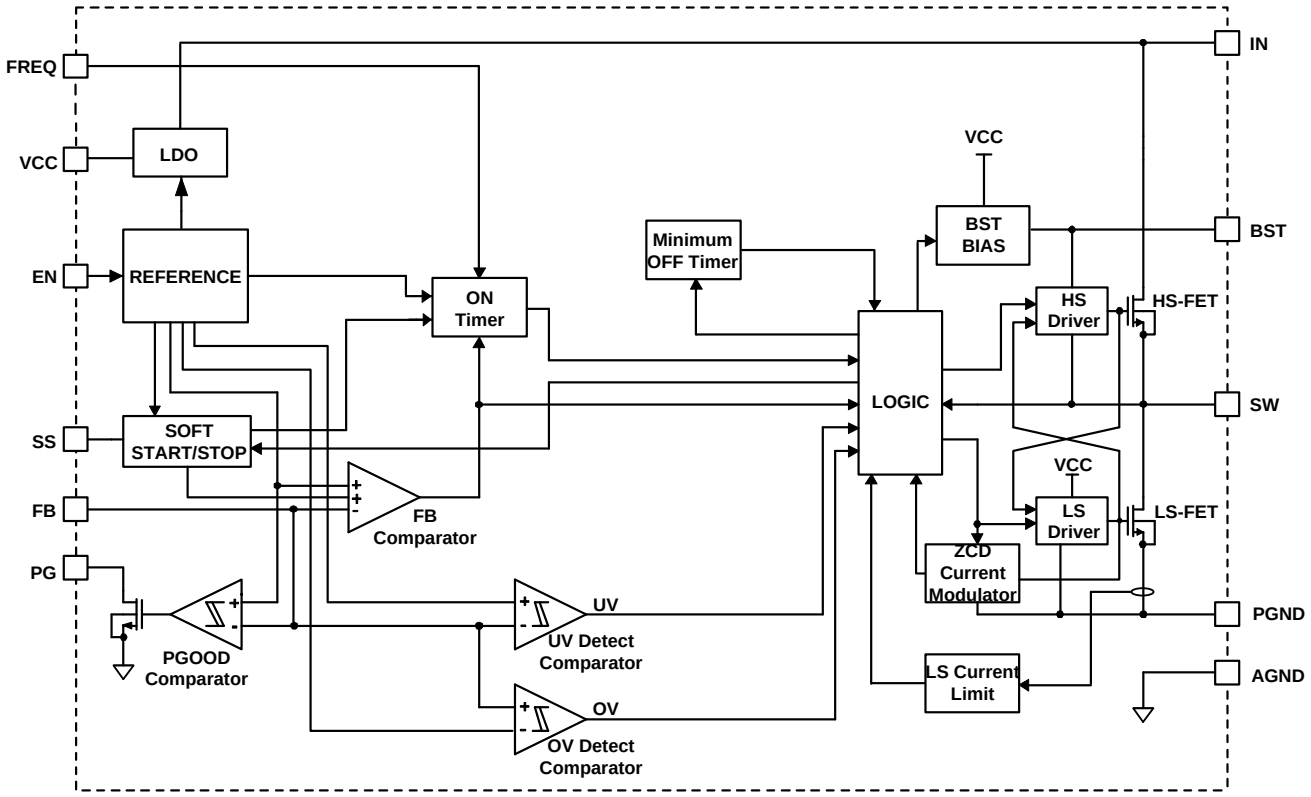

Figure 1—Functional Block Diagram

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OPERATION

PWM Operation

The MPQ8632D-6/MPQ8632D-12 is a fully integrated synchronous rectified step-down switch mode converter. It uses Constant-on-time (COT) control to provide a fast transient response and ease loop stabilization.

At the beginning of each cycle, the high-side MOSFET (HS-FET) turns ON when the feedback voltage (V_{FB}) drops below the reference voltage (V_{REF}), which indicates an insufficient output voltage. The input voltage and the frequency-set resistor determine the ON period as follows:

$$T_{ON}(ns) = \frac{6.1 \times R_{FREQ}(k\Omega)}{V_{IN}(V) - 0.4} \quad (1)$$

After the ON period elapses, the HS-FET turns off. It turns ON again when V_{FB} drops below V_{REF}. By repeating this operation, the converter regulates the output voltage. The integrated low-side MOSFET (LS-FET) turns on when the HS-FET is OFF to minimize the conduction loss. There is a dead short (or shoot-through) between input and GND if both HS-FET and LS-FET turn on at the same time. A dead-time (DT) internally generated between HS-FET OFF and LS-FETON, or LS-FET OFF and HS-FET ON avoids shoot-through.

Heavy-Load Operation

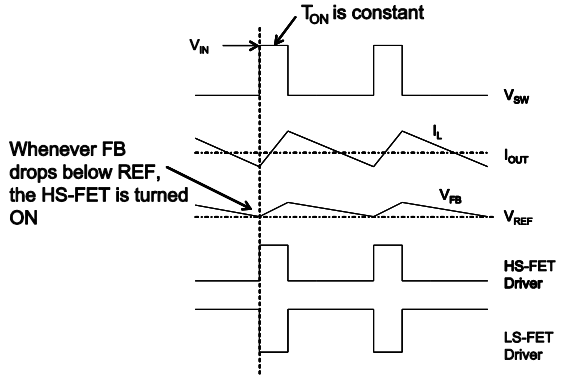

Figure 2—Heavy Load Operation

When the output current is high and the inductor current is always above zero amps, it is called continuous-conduction-mode (CCM). Figure 2 shows the CCM operation. When V_{FB} is below V_{REF}, HS-FET turns on for a fixed interval determined by the one- shot on-timer as per equation 1. When the HS-FET turns off, the LS-FET turns on until the next period.

In CCM operation, the switching frequency is fairly constant and is also called PWM mode.

Light-Load Operation

As the load decreases, the inductor current decreases too. When the inductor current touches zero, the operation is transited from continuous-conduction-mode (CCM) to discontinuous-conduction-mode (DCM).

Figure 3 shows the light load operation. When V_{FB} drops below V_{REF}, HS-FET turns on for a fixed interval determined by the one- shot on-timer as per equation 1. When the HS-FET turns off, the LS-FET turns on until the inductor current reaches zero. In DCM operation, the V_{FB} does not reach V_{REF} when the inductor current is approaching zero. The LS-FET driver turns into tri-state (high Z) whenever the inductor current reaches zero. A current modulator takes over the control of LS-FET and limits the inductor current less than -1mA. Hence, the output capacitors discharge slowly to GND through LS-FET. As a result, this mode improves greatly the light load efficiency. At light load condition, the HS-FET does not turns ON as frequently as at heavy load condition. This is called skip mode.

At light load or no load condition, the output drops very slowly and the MPQ8632D-6/MPQ8632D-12 reduces the switching frequency naturally and then achieves high efficiency at light load.

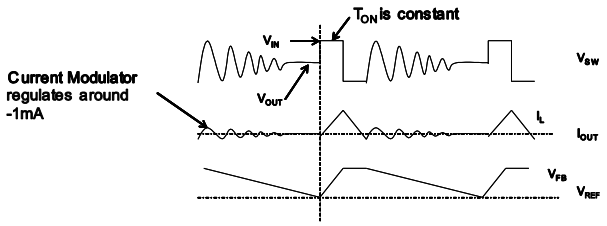

Figure 3—Light Load Operation

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As the output current increases from the light load condition, the current modulator regulates the operating period that becomes shorter. The HS-FET turns ON more frequently. Hence, the switching frequency increases correspondingly. The output current reaches the critical level when the current modulator time decreases to zero. Determine the critical output current level as follows:

$$I_{OUT} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times L \times F_{SW} \times V_{IN}} \quad (2)$$

Where F_{SW} is the switching frequency.

The IC turns into PWM mode once the output current exceeds the critical level. After that, the switching frequency stays fairly constant over the output current range.

Switching Frequency

Selecting the switching frequency requires trading off between efficiency and component size. Low frequency operation increases efficiency by reducing MOSFET switching losses, but requires larger inductor and capacitor values to minimize the output voltage ripple.

For MPQ8632D-6/MPQ8632D-12， set the on time using the FREQ pin to set the frequency for steady state operation at CCM.

The MPQ8632D-6/MPQ8632D-12 uses adaptive constant-on-time (COT) control, though the IC lacks a dedicated oscillator. Connect the FREQ pin to the IN pin through the resistor (R_{FREQ}) so that the input voltage is feed-forwarded to the one-shot on-time timer. When operating in steady state at CCM, the duty ratio stays at V_{OUT}/V_{IN}, so the switching frequency is fairly constant over the input voltage range. Set the switching frequency as follows:

$$F_{SW}(kHz) = \frac{10^6}{\frac{6.1 \times R_{FREQ}(k\Omega)}{V_{IN}(V) - 0.4} \times \frac{V_{IN}(V)}{V_{OUT}(V)} + T_{DELAY}(ns)} \quad (3)$$

Where T_{DELAY} is the comparator delay of about 5ns.

Typically, the MPQ8632D-6/MPQ8632D-12 is set to 200kHz to 1MHz applications. It is optimized to operate at high switching frequencies at high efficiency high switching frequencies allow for physically smaller LC filter components to reduce the PCB footprint.

Jitter and FB Ramp Slope

Figure 4 and Figure 5 show jitter occurring in both PWM mode and skip mode. When there is noise on the V_{FB} descending slope, the HS-FET ON time deviates from its intended point and produces jitter and influences system stability. The V_{FB} ripple's slope steepness dominates the noise immunity though its magnitude has no direct effect.

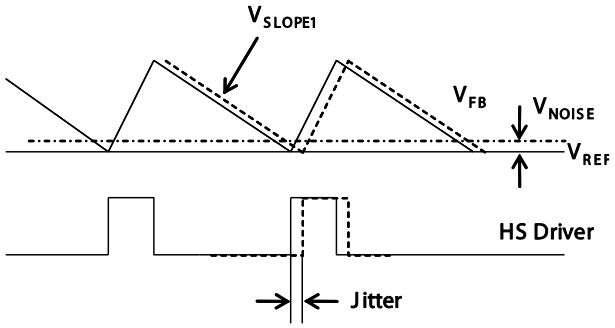

Figure 4—Jitter in PWM Mode

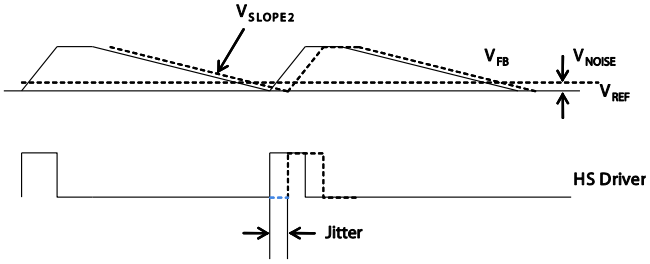

Figure 5—Jitter in Skip Mode

Ramp with a Large ESR Capacitor

Using POSCAPs or other large-ESR capacitors as the output capacitor results in the ESR ripple dominating the output ripple. The ESR also significantly influences the V_{FB} slope. Figure 6 shows the simplified equivalent circuit in PWM mode with the HS-FET off and without an external ramp circuit.

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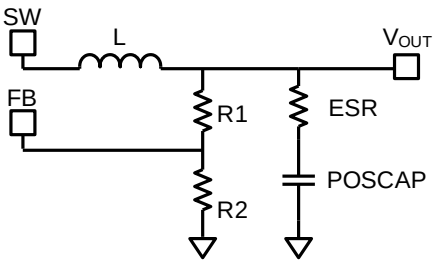

Figure 6—Simplified Circuit in PWM Mode without External Ramp Compensation

To realize the stability without an external ramp, usually select the ESR value as follows:

$$R_{ESR} \geq \frac{\frac{T_{SW}}{0.7\times\pi}+\frac{T_{ON}}{2}}{C_{OUT}} \quad (4)$$

Where T_{SW} is the switching period.

Ramp with a Small ESR Capacitor

Use an external ramp when using ceramic output capacitors, because the ESR ripple is not high enough to stabilize the system.

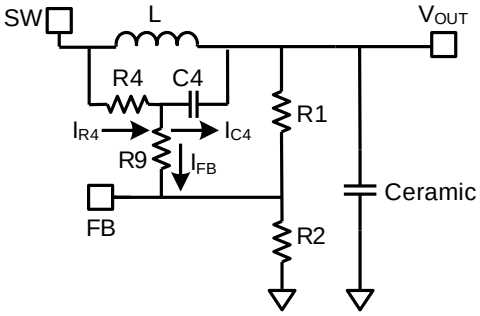

Figure 7—Simplified Circuit in PWM Mode with External Ramp Compensation

Figure 7 shows the simplified circuit in PWM mode with the HS-FET OFF and an external ramp compensation circuit (R4, C4). Design the external ramp based on the inductor ripple current. Select C4, R9, R1 and R2 to meet the following condition:

$$\frac{1}{2\pi\times F_{SW}\times C4} < \frac{1}{5}\times\left(\frac{R1\times R2}{R1+R2}+R9\right) \quad (5)$$

Where:

$$I_{R4} = I_{C4} + I_{FB} \approx I_{C4} \quad (6)$$

Then estimate the ramp on V_{FB} as:

$$V_{RAMP} = \frac{V_{IN}-V_{OUT}}{R4\times C4}\times T_{ON}\times\left(\frac{R1//R2}{R1//R2+R9}\right) \quad (7)$$

The V_{FB} ripple's descending slope then follows:

$$V_{SLOPE1} = \frac{V_{RAMP}}{T_{OFF}} = \frac{-V_{OUT}}{R4\times C4} \quad (8)$$

Equation 8 shows that if there is instability in PWM mode, reduce either R4 or C4. If C4 is irreducible due to equation 5 limitations, then reduce R4. For a stable PWM operation, design V_{slope1} based on equation 9.

$$-V_{SLOPE1} \geq \frac{\frac{T_{SW}}{0.7\times\pi}+\frac{T_{ON}}{2}-R_{ESR}\times C_{OUT}}{2\times L\times C_{OUT}}\times V_{OUT}+\frac{I_{OUT}\times 10^{-3}}{T_{SW}-T_{ON}} \quad (9)$$

Where I_{OUT} is the load current.

In skip mode, The V_{FB} ripple's descending slope is almost same whether the external ramp is used or not. Figure 8 shows the simplified circuit in skip mode when both the HS-FET and LS-FET are off.

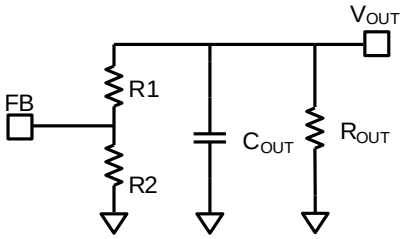

Figure 8—Simplified Circuit in skip Mode

Determine the V_{FB} ripple's descending slope in skip mode as follows:

$$V_{SLOPE2} = \frac{-V_{REF}}{[(R1+R2)//R_{OUT}]\times C_{OUT}} \quad (10)$$

Where R_{OUT} is the equivalent load resistor.
Figure 5 shows that V_{SLOPE2} in skip mode is lower than that is in PWM mode, so it is reasonable that the jitter in skip mode is larger To achieve less jitter during ultra light load condition, reduce R1 and R2, but that will decrease the light load efficiency.

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Configuring the EN Control

The regulator turns on when En goes high; conversely it turns off when EN goes low. Do not float the pin.

For automatic start-up, pull the EN pin up to input voltage through a resistive voltage divider. Choose the values of the pull-up resistor (R_{UP} from the IN pin to the EN pin) and the pull-down resistor (R_{DOWN} from the EN pin to GND) to determine the automatic start-up voltage:

$$V_{IN-START} = 1.5 \times \frac{(R_{UP} + R_{DOWN})}{R_{DOWN}} (V) \quad (11)$$

For example, for R_{UP}=100kΩ and R_{DOWN}=51kΩ, the $V_{IN-START}$ is set at 4.44V.

To reduce noise, add a 10nF ceramic capacitor from EN to GND.

An internal zener diode on the EN pin clamps the EN pin voltage to prevent run away. The maximum pull up current assuming the worst case 6V for the internal zener clamp should be less than 1mA.

Therefore, when driving EN with an external logic signal, use an EN voltage less than 6V. When connecting EN to IN through a pull-up resistor or a resistive voltage divider, select a resistance that ensures a maximum pull-up current less than 1mA.

If using a resistive voltage divider and V_{IN} exceeds 6V, then the minimum resistance for the pull-up resistor R_{UP} should meet:

$$\frac{V_{IN} - 6V}{R_{UP}} - \frac{6V}{R_{DOWN}} \leq 1mA \quad (12)$$

With only R_{UP} (the pull-down resistor, R_{DOWN}, is not connected), then the VCC UVLO threshold determines $V_{IN-START}$, so the minimum resistor value is:

$$R_{UP} \geq \frac{V_{IN} - 6V}{1mA} (\Omega) \quad (13)$$

A typical pull-up resistor is 100kΩ.

External VCC bias

An external 5V VCC bias can disable the internal LDO, in this case, Vin can be as low as 2.5V.

Soft Start/Stop

The MPQ8632D-6/MPQ8632D-12 employs a soft start/stop (SS) mechanism to ensure a smooth output during power-up and power shutdown. When the EN pin goes high, an internal current source (20μA) charges the SS capacitor. The SS capacitor voltage takes over the REF voltage to the PWM comparator. The output voltage smoothly ramps up with the SS voltage. Once the SS voltage reaches the REF voltage, it continues ramping up while V_{REF} takes over the control of the PWM comparator. At this point, soft start finishes and the device enters steady state operation.

When the EN pin becomes low, the SS capacitor voltage is discharged through a 10uA internal current source. Once the SS voltage reaches REF voltage, it takes over the control of the PWM comparator. The output voltage will decrease smoothly with SS voltage until zero level.

Determine the SS capacitor value as follows:

$$C_{SS}(nF) = \frac{T_{SS}(ms) \times I_{SS}(\mu A)}{V_{REF}(V)} \quad (14)$$

If the output capacitors are large, then avoid setting a short SS time otherwise it would risk hitting the current limit during SS. Use a minimum value of 4.7nF if the output capacitance value exceeds 330μF.

Pre-Bias Startup

The MPQ8632D-6/MPQ8632D-12 has been designed for monotonic startup into pre-biased loads. If the output is pre-biased to a certain voltage during startup, the IC will disable switching for both high-side and low-side switches until the voltage on the soft-start capacitor exceeds the sensed output voltage at the FB pin.

Power Good (PG)

The MPQ8632D-6/MPQ8632D-12 has a power-good (PG) output. The PG pin is the open drain of a MOSFET. Connect it to VCC or some other voltage source that measures less than 5.5V through a pull-up resistor (typically 100kΩ). Recommend a 10nF capacitor from PG to GND when the PG pull up resistor is <100kΩ. After VCC is ready, the MOSFET turns on so that the PG pin is pulled to GND before the SS is ready.

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After the FB voltage reaches 90% of the REF voltage, the PG pin is pulled high after a 2.5ms delay.

When the FB voltage drops to 85% of the REF voltage or exceeds 120% of the nominal REF voltage, the PG pin is pulled low.

If the input supply fails to power the MPQ8632D-6/MPQ8632D-12, the PG pin is also pulled low even though this pin is tied to an external DC source through a pull-up resistor (typically 100kΩ).

Over-Current Protection (OCP)

The MPQ8632D-6/MPQ8632D-12 features TWO current limit levels for over-current conditions: low-side valley current limit and low-side negative current limit.

Low-Side Valley Current Limit: The device monitors the inductor current during the LS-FET ON state. When ILIM=1 and at the end of the OFF time, the LS-FET sourcing current is compared to the internal positive-valley–current limit. If the valley current limit is less than the LS-FET sourcing current, the HS-FET remains OFF and the LS-FET remains ON for the next ON time. When the LS-FET sourcing current drops below the valley current limit, the HS-FET turns on again.

These parts enter OCP mode if the LS-FET sourcing valley current exceeds the valley current limit for about 40us. During OCP, the device tries to recover from the over-current fault with hiccup mode: the chip disables the output power stage, discharges the soft-start capacitor and then automatically retries soft-start. If the over-current condition still holds after soft-start ends, the device repeats this operation cycle until the over-current conditions disappear and then output rises back to regulation level. OCP offers non-latch protection.

Low-Side Negative Current Limit: If the sensed LS-FET negative current exceeds the negative current limit, the LS-FET turns off immediately and stays OFF for the remainder of the OFF period. In this situation, both MOSFETs are OFF until the end of a fixed interval. The HS-FET body diode conducts the inductor current for the fixed time.

Over -Voltage Protection (OVP)

The MPQ8632D-6/MPQ8632D-12 monitors the output voltage using the FB pin connected to the tap of a resistor divider to detect over-voltage. MPQ8632D-6 and MPQ8632D-12 provide non-latch OVP mode.

If the FB voltage exceeds the nominal REF voltage but remains lower than 120% of the REF voltage (0.611V), both MOSFETs are off.

If the FB voltage exceeds 120% of the REF voltage but remains below 130%, the LS-FET turns on while the HS-FET remains off. The LS-FET remains on until the FB voltage drops below 110% of the REF voltage or the low-side negative current limit is hit.

If the FB voltage exceeds 130% of the REF voltage, these parts enter a non-latch off mode. Once the FB voltage comes back to the reasonable value, they will exit this OVP mode and operate normally again.

UVLO protection

The MPQ8632D-6/MPQ8632D-12 has under-voltage lock-out protection (UVLO). When the VCC voltage exceeds the UVLO rising threshold voltage, the MPQ8632D-6/MPQ8632D-12 powers up. It shuts off when the VCC voltage falls below the UVLO falling threshold voltage. This is non-latch protection.

The MPQ8632D-6/MPQ8632D-12 is disabled when the VCC voltage falls below 3.3 V. If an application requires a higher UVLO threshold, use the two external resistors connected to the EN pin as shown in Figure 9 to adjust the startup input voltage. For best results, use the enable resistors to set the input voltage falling threshold (V_{STOP}) above 3.6 V. Set the rising threshold (V_{START}) to provide enough hysteresis to account for any input supply variations.

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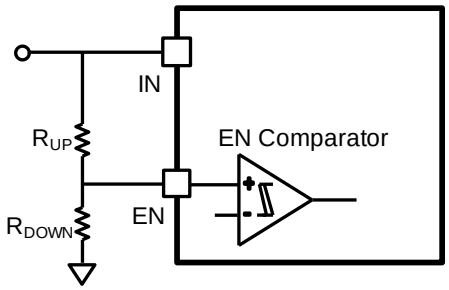

Figure 9—Adjustable UVLO Threshold

Thermal Shutdown

The MPQ8632D-6/MPQ8632D-12 has thermal shutdown protection. The IC internally monitors the junction temperature. If the junction temperature exceeds the threshold value (minimum 150ºC), the converter shuts off. This is a non-latch protection. There is about 25ºC hysteresis. Once the junction temperature drops to about 125ºC, it initiates a soft startup.

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APPLICATION INFORMATION

Setting the Output Voltage-Large ESR Capacitors

For applications that electrolytic capacitor or POS capacitor with a large ESR is set as output capacitors. The feedback resistors—R1 and R2 as shown in Figure 10—set the output voltage.

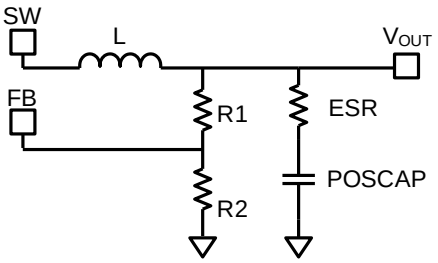

Figure10—Simplified POSCAP Circuit

First, choose a value for R2 that balances between high quiescent current loss (low R2) and high noise sensitivity on FB (high R2). A typical value falls within 5kΩ to 50kΩ, using a comparatively larger R2 when V_{OUT} is low, and a smaller R2 when V_{OUT} is high. Then calculate R1 as follows, which considers the output ripple:

$$R1 = \frac{V_{OUT} - \frac{1}{2} \times \Delta V_{OUT} - V_{REF}}{V_{REF}} \times R2 \quad (15)$$

Where ΔV_{OUT} is the output ripple determined by equation 24.

Setting the Output Voltage-Small ESR Capacitors

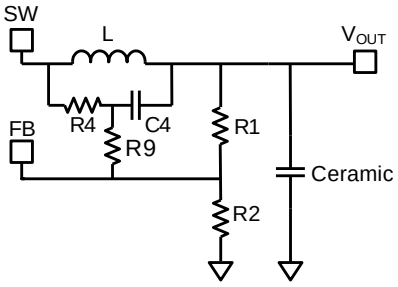

Figure11—Simplified Ceramic Capacitor Circuit

When using a low ESR ceramic capacitor on the output, add an external voltage ramp to the FB pin consisting of R4 and C4.The ramp voltage, V_{RAMP}, and the resistor divider influence the output voltage as shown in Figure 11. Calculate V_{RAMP} as shown in equation 7. Select R2 to balance between high quiescent current loss and FB noise sensitivity. Choose R2 within 5kΩ to 50kΩ, using a larger R2 when V_{OUT} is low, and a smaller R2 when V_{OUT} is high. Determine the value of R1 as follows:

$$R1 = \frac{R2}{\frac{V_{FB(AVG)}}{V_{OUT} - V_{FB(AVG)}} - \frac{R2}{R4 + R9}} \quad (16)$$

Where $V_{FB(AVG)}$ is the average FB voltage. $V_{FB(AVG)}$ varies with the V_{IN}, V_{OUT}, and load condition, where the load regulation is strictly related to the $V_{FB(AVG)}$. Also the line regulation is related to the $V_{FB(AVG)}$; improving the load or line regulation involves a lower V_{RAMP} that meets equation 9.

For PWM operation, estimate $V_{FB(AVG)}$ from equation 17.

$$V_{FB(AVG)} = V_{REF} + \frac{1}{2} \times V_{RAMP} \times \frac{R1 // R2}{R1 // R2 + R9} \quad (17)$$

Usually, R9 is 0Ω, though it can also be set following equation 18 for better noise immunity. It should also be less than 20% of R1//R2 to minimize its influence on V_{RAMP}.

$$R9 < \frac{1}{5} \times \frac{R1 \times R2}{R1 + R2} \quad (18)$$

Using equations 16 and 17 to calculate the output voltage can be complicated. To simplify the R1 calculation in equation 16, add a DC-blocking capacitor, C_{DC}, to filter the DC influence from R4 and R9. Figure 12 shows a simplified circuit with external ramp compensation and a DC-blocking capacitor. The addition of this capacitor, simplifies the R1 calculation as per equation 19 for PWM mode operation.

$$R1 = \frac{V_{OUT} - V_{REF} - \frac{1}{2} \times V_{RAMP}}{V_{REF} + \frac{1}{2} \times V_{RAMP}} \times R2 \quad (19)$$

For best results, select a C_{DC} Value at least 10× C4 for better DC blocking performance, but smaller than 0.47µF account for start-up performance. To use a larger C_{DC} for better FB noise immunity, reduce R1 and R2 to limit effects on system start-up. Note that even with Cdc, the load and line regulation are still related to V_{RAMP}.

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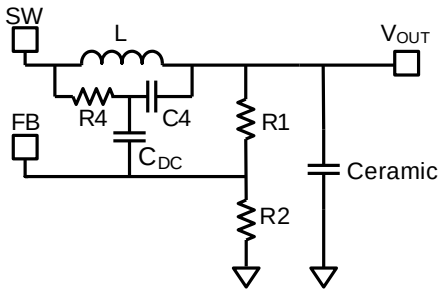

Figure12—Simplified Ceramic Capacitor Circuit with DC Blocking Capacitor

Input Capacitor

The input current to the step-down converter is discontinuous, and therefore, requires a capacitor to supply the AC current to the step-down converter while maintaining the DC input voltage. Use ceramic capacitors for best performance. During layout, Place the input capacitors as close to the IN pin as possible.

The capacitance can vary significantly with temperature. Use capacitors with X5R and X7R ceramic dielectrics because they are fairly stable over a wide temperature range.

The capacitors must also have a ripple current rating that exceeds the converter's maximum input ripple current. Estimate the input ripple current as follows:

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (20)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, where:

$$I_{CIN} = \frac{I_{OUT}}{2} \quad (21)$$

For simplification, choose an input capacitor with an RMS current rating that exceeds half the maximum load current.

The input capacitance value determines the converter input voltage ripple. Select a capacitor value that meets any input voltage ripple requirements.

Estimate the input voltage ripple as follows:

$$\Delta V_{IN} = \frac{I_{OUT}}{F_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (22)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, where:

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{F_{SW} \times C_{IN}} \quad (23)$$

Output Capacitor

The output capacitor maintains the DC output voltage. Use ceramic capacitors or POSCAPs. Estimate the output voltage ripple as:

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times F_{SW} \times C_{OUT}}) \quad (24)$$

When using ceramic capacitors, the capacitance dominates the impedance at the switching frequency. The capacitance also dominates the output voltage ripple. For simplification, estimate the output voltage ripple as:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times F_{SW}^2 \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (25)$$

The ESR only contributes minimally to the output voltage ripple, thus requiring an external ramp to stabilize the system. Design the external ramp with R4 and C4 as per equation 5, 8 and 9.

The ESR dominates the switching-frequency impedance for POSCAPs,. The ESR ramp voltage is high enough to stabilize the system. thus eliminating the need for an external ramp. Select a minimum ESR value around 12mΩ to ensure stable operation. For simplification, the output ripple can be approximated as:

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (26)$$

Inductor

The inductor supplies constant current to the output load while being driven by the switching input voltage. A larger value inductor results in less ripple current and lower output ripple voltage, but is larger physical size, has a higher series resistance, and/or lower saturation current. Generally, select an inductor value that allows the inductor peak-to-peak ripple current to 30% to 40% of the maximum switch current limit. Also, design for a peak inductor current that is below the maximum switch current limit. Calculate the inductance value as:

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$$L = \frac{V_{OUT}}{F_{SW} \times \Delta I_L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (27)$$

Where ΔI_L is the peak-to-peak inductor ripple current.

Choose an inductor that will not saturate under the maximum inductor peak current. The peak inductor current can be calculated as:

$$I_{LP} = I_{OUT} + \frac{V_{OUT}}{2 \times F_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (28)$$

Table 1 lists a few highly-recommended high-efficiency inductors.

Table 1—Inductor Selection Guide

Part Number	Manufacturer	Inductance (µH)	DCR (mΩ)	Current Rating (A)	Dimensions L x W x H (mm³)	Switching Frequency (kHz)
744325072	Wurth	0.72	1.35	35	10.2 x 10.5 x 4.7	500
FDU1250C-1R0M	TOKO	1	1.72	31.3	13.3 x 12.1 x 5	500
FDA1055-1R5M	TOKO	1.5	2.8	24	11.6 x 10.8 x 5.5	500
744325180	Wurth	1.8	3.5	18	10.2 x 10.5 x 4.7	500
FDA1055-2R2M	TOKO	2.2	3.94	20.6	11.6 x 10.8 x 5.5	500
FDA1055-3R3M	TOKO	3.3	5.92	15.6	11.6 x 10.8 x 5.5	500
HC7-3R9-R	Cooper	3.9	7.9	10.6	13.8 x 13 x 5.5	500

Typical Design Parameter Tables

The following tables include recommended component values for typical output voltages (1V, 2.5V, 3.3V) and switching frequency (500kHz). Refer to Tables 2-3 for design cases without external ramp compensation and Tables 4-5 for design cases with external ramp compensation. An external ramp is not needed when using high-ESR capacitors, such as electrolytic or POSCAPs. Use an external ramp when using low-ESR capacitors, such as ceramic capacitors. For cases not listed in this datasheet, an excel spreadsheet provided by local sales representatives can assist with the calculations.

Table 2—MPQ8632D-6, F_{SW}=500kHz, V_{IN}=12V

V_{OUT} (V)	L (µH)	R1 (kΩ)	R2 (kΩ)	R7 (kΩ)
1	1	13.3	20	357
2.5	2.2	63.4	20	887
3.3	3.3	91	20	1200

Table 3—MPQ8632D-12, F_{SW}=500kHz, V_{IN}=12V

V_{OUT} (V)	L (µH)	R1 (kΩ)	R2 (kΩ)	R7 (kΩ)
1	0.72	13.3	20	357
2.5	1.5	63.4	20	887
3.3	1.8	91	20	1200

Table 4—MPQ8632D-6, F_{SW}=500kHz, V_{IN}=12V

V_{OUT} (V)	L (µH)	R1 (kΩ)	R2 (kΩ)	R4 (kΩ)	C4 (pF)	R7 (kΩ)
1	1	13.7	20	750	220	357
2.5	2.2	66.5	20	1000	220	887
3.3	3.3	95.3	20	1200	220	1200

Table 5—MPQ8632D-12, F_{SW}=500kHz, V_{IN}=12V

V_{OUT} (V)	L (µH)	R1 (kΩ)	R2 (kΩ)	R4 (kΩ)	C4 (pF)	R7 (kΩ)
1	0.72	13.7	20	750	220	357
2.5	1.5	66.5	20	1000	220	887
3.3	1.8	95.3	20	1200	220	1200

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LAYOUT RECOMMENDATION

1. Place high current paths (GND, IN, and SW) very close to the device with short, direct and wide traces.
2. Two-layer IN copper layers are required to achieve better performance. Respectively put at least a decoupling capacitor on either side of the IC that has VIN pin and as close to the IN and GND pins as possible. Also, several vias with 18mil diameter and 8mil hole- size are recommended to be placed under the device and are required near input capacitors to help on the thermal dissipation, also reduce the parasitic inductance.
3. Put a decoupling capacitor as close to the VCC and AGND pins as possible.
4. Keep the switching node (SW) plane as small as possible and far away from the feedback network.
5. Place the external feedback resistors next to the FB pin. Make sure that there are no vias on the FB trace. The feedback resistors should refer to AGND instead of PGND.
6. Keep the BST voltage path (BST, C3, and SW) as short as possible.
7. Keep FREQ signal away from noise signals, like SW, BST and VIN plane and vias close to the MP8632D VIN pins. The VIN pin of frequency setting resistor (R_{FREQ}) should connect to a quiet VIN node before input decoupling capacitor.
8. Strongly recommend a four-layer layout to improve thermal performance.

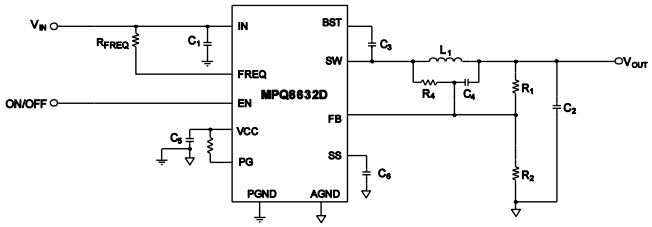
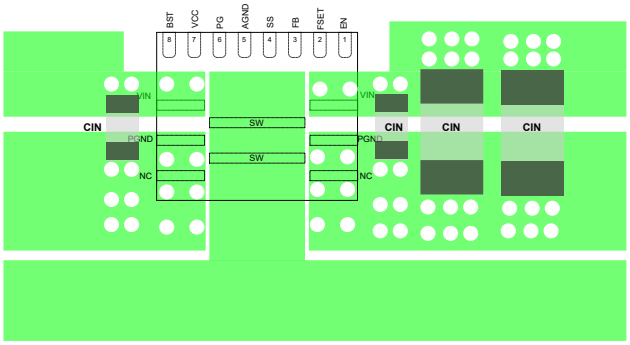


Figure 13—Schematic for PCB Layout Guide



Top Layer

Figure 14—PCB Layout Guide

Design Example

Below is a design example following the application guidelines for the specifications:

Table 6—Design Example

V_{IN}	4.5-18V
V_{OUT}	1V
F_{SW}	500kHz

The detailed application schematic is shown in Figure 14. The typical performance and circuit waveforms have been shown in the Typical Performance Characteristics section. For more device applications, please refer to the related Evaluation Board Datasheets.

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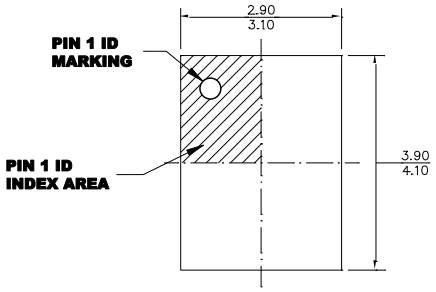
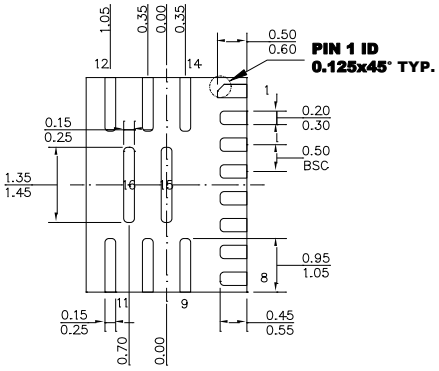
PACKAGE INFORMATION

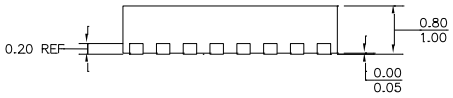
QFN(3X4mm)



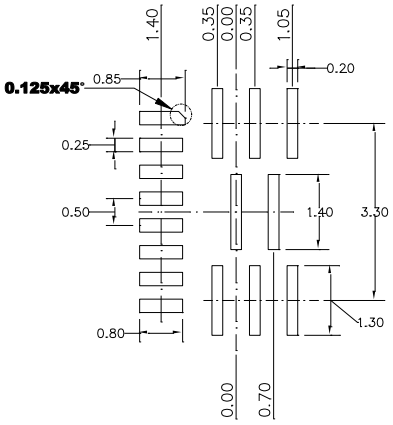
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

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