MPQ79700FS

MPSafe™ ASIL-D 12-Channel Power Sequencer, AEC-Q100 Qualified

DESCRIPTION

The MPQ79700FS is a 12-channel, functional safety power sequencer engineered to provide precise power sequencing and safety functions for automotive advanced driver assistance systems (ADAS) and autonomous driving platforms.

The device's configurability and flexibility enables design reuse across different applications and system-on-chip (SoC) generations.

The MPQ79700FS contains a crystal driver, a real-time clock (RTC) with an alarm function, a configurable watchdog that can be accessed through the I^2C interface, and active-low system reset and interrupt outputs.

Safety mechanisms such as built-in self-test (BIST) provide high diagnostic coverage, which help the system achieve its target ASIL rating.

The MPQ79700FS is available in a QFN-24 (4mmx4mm) package with wettable flanks.

FEATURES

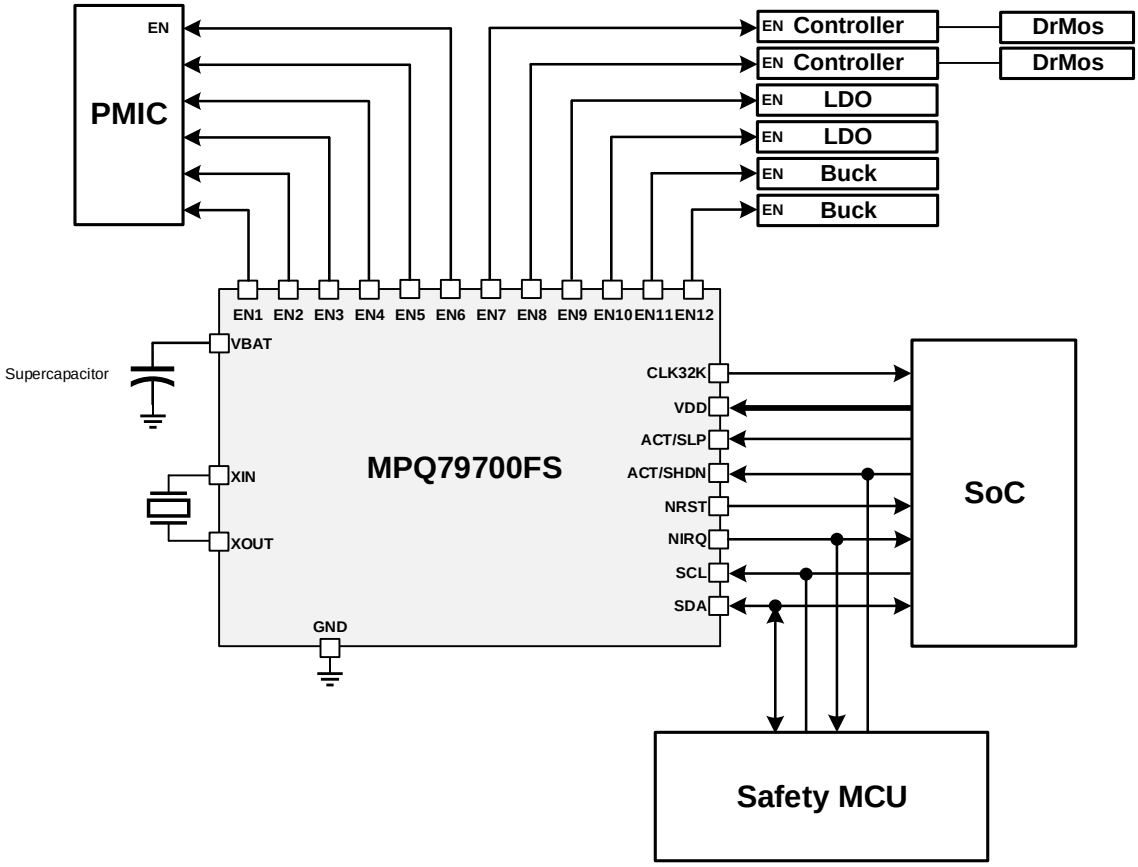
- Designed for Automotive ADAS and Autonomous Driving Platforms:
  - 2.7V to 5.5V Input Voltage (V_{IN}) Range
  - 12 Enable Outputs
  - Time-Slot Based Sequencing
  - System Reset Signal
  - System Interrupt Signal
- Mission-Critical Safety Features:
  - Write Protection on Safety Critical Registers
  - Advanced Diagnostics
  - Built-In Self-Test (BIST)
  - Window Watchdog
  - Over-Temperature Shutdown
  - Support Systems Up to ASIL-D
  - ISO26262 Functional Safety Compliant
- Application Flexibility with I^2C Interface:
  - Fast Mode I^2C Interface with CRC
  - One-Time Programmable (OTP) Memory
  - Configurable Parameters:
    - Sequence Order
    - I^2C Address
    - Watchdog Timing
    - Drive Mode for Enable Pins
    - Alternate Functions for Enable Pins
- Additional Features:
  - Backup Battery Input
  - 32kHz Crystal Oscillator Driver
  - Real-Time Clock (RTC)
  - Available in a QFN-24 (4mmx4mm) Package with a 0.5mm Pitch and Wettable Flanks
  - Available in AEC-Q100 Grade 1

MPSafe™ Developed for Functional Safety Applications: ISO26262 Compliant

APPLICATIONS

- Advanced Driver Assistance Systems
- Autonomous Driving Platforms
- Functional Safety Systems with Multiple Power Rails
- Industrial Robotics

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating***
MPQ79700FSGRE-xxxx-AEC1**	QFN-24 (4mmx4mm)	*See Below*	1

* For Tape & Reel, add suffix -Z (e.g. MPQ79700FSGRE-xxxx-AEC1-Z).

** "-xxxx" is the configuration code identifier for the register settings stored in the OTP register. Each "x" can be a hexadecimal value between 0 and F. The default code is the "-0000" version. Contact an MPS FAE to create this unique number.

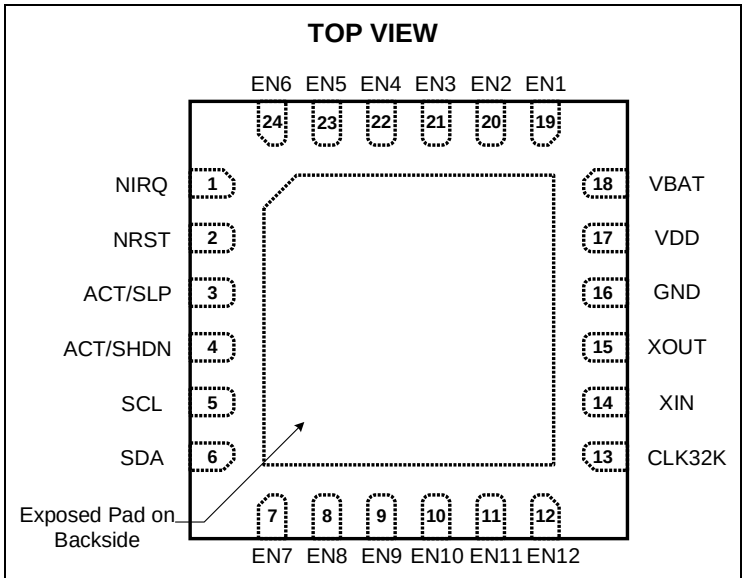
*** Moisture Sensitivity Level Rating

TOP MARKING

MPSYWW
M79700
LLLLLL
AE

MPS: MPS prefix
Y: Year code
WW: Week code
M79700: Part number
LLLLLL: Lot number
A: Part revision code
E: Wettable flank

PACKAGE REFERENCE



QFN-24 (4mmx4mm) with Wettable Flanks

PIN FUNCTIONS

Pin #	Name	Type	Description
1	NIRQ	Out, OD	**Interrupt.** The NIRQ pin is an active-low signal. If an event occurs that requires the device status to be read, this pin sends an interrupt output signal to the I²C. This pin is an open-drain status pin. Connect NIRQ to a voltage with a resistor (e.g. 10kΩ). It is recommended that this pull-up voltage not exceed the VDD voltage (V_{DD}). Connect this pin to GND if it is not used.
2	NRST	Out, OD	**Reset.** The NRST pin is an active-low signal, and it is the system reset output. This pin is an open-drain status pin. Connect NRST to a voltage with a resistor (e.g. 10kΩ). The pull-up voltage must not exceed V_{DD}. Connect this pin to GND if it is not used.
3	ACT/SLP	In	**Active/sleep.** The ACT/SLP pin is used in conjunction with the SLEEP entry/exit sequence control registers. Connect ACT/SLP directly to a voltage or use a resistor (e.g. 10kΩ). The ACT/SLP pin's logic high/low threshold is typically 0.75V/0.45V, respectively. The voltage on the ACT/SLP pin can exceed V_{DD}. If ACT/SLP is floating, an internal 100kΩ resistor pulls this pin low. When this pin goes from low (SLP) to high (ACT), the system exits SLEEP mode. When this pin goes from high (ACT) to low (SLP), the system enters SLEEP mode.
4	ACT/SHDN	In	**Active/shutdown.** The ACT/SHDN pin is the power sequencer control input. Connect ACT/SHDN directly to a voltage or use a resistor (e.g. 10kΩ). The ACT/SHDN pin's logic high/low threshold is typically 0.75V/0.45V, respectively. The voltage on the ACT/SHDN pin can exceed V_{DD}. If ACT/SHDN is floating, an internal 100kΩ resistor pulls this pin low. When this pin goes from low (SHDN) to high (ACT), the system starts up. When this pin goes from high (ACT) to low (SHDN), the system shuts down.
5	SCL	In, OD	**I²C bus serial clock input.** The SCL pin is an open-drain port. An external pull-up resistor is required to connect this pin to the I²C bus supply rail. SCL supports up to 1Mb/s of data transfer in fast-mode plus. If this pin is not used, connect it to the VDD pin through a resistor (e.g. 100kΩ).
6	SDA	In/Out, OD	**I²C bus serial data input/output.** The SDA pin is an open-drain port. An external pull-up resistor is required to connect this pin to the I²C bus supply rail. SDA supports up to 1Mb/s of data transfer in fast-mode plus. If this pin is not used, connect it to the VDD pin through a resistor (e.g. 100kΩ).
7, 8	EN7, EN8	Out, OD/PP	**Sequencer outputs 7 and 8.** The EN7 and EN8 pins have an optional output type: open drain or push-pull. Open drain: Connect this pin to a voltage with a resistor (e.g. 10kΩ), regardless of whether this pin is used. It is recommended that the pull-up voltage not exceed V_{DD}. Push-pull: No external pull-up resistor is required. Float this pin if it is not used.
9	EN9	Out, OD/PP	**Sequencer output 9 and general-purpose output 9.** The EN9 pin has an optional output type: open drain or push-pull. Open drain: Connect this pin to a voltage with a resistor (e.g. 10kΩ), regardless of whether this pin is used. It is recommended that the pull-up voltage not exceed V_{DD}. Push-pull: No external pull-up resistor is required. Float this pin if it is not used.

PIN FUNCTIONS *(continued)*

Pin #	Name	Type	Description
10	EN10	In/Out, OD/PP	**Sequencer output 10, general-purpose output 10, and emergency off input (active low).** The EN10 pin has multiple functions, and can be configured as either an output or input. Open-drain output: Connect this pin to a voltage with a resistor (e.g. 10kΩ), regardless of whether this pin is used. It is recommended that the pull-up voltage not exceed V_{DD}. Push-pull output: No external pull-up resistor is required. Float this pin if it is not used. Input: The emergency off (NEM_PD) function is enabled. Connect this pin to a voltage with a resistor (e.g. 10kΩ). It is recommended that the pull-up voltage not exceed V_{DD}. The EN10 pin's input logic high/low threshold is 0.84V/0.36V.
11	EN11	In/Out, OD/PP	**Sequencer output 11, general-purpose output 11, and reset input (active low).** The EN11 pin has multiple functions, and can be configured as either an output or input. Open-drain output: Connect this pin to a voltage with a resistor (e.g. 10kΩ), regardless of whether this pin is used. It is recommended that the pull-up voltage not exceed V_{DD}. Push-pull output: No external pull-up resistor is required. Float this pin if it is not used. Input: The reset input (NRST_IN) function is enabled. Connect this pin to a voltage with a resistor (e.g. 10kΩ). It is recommended that the pull-up voltage not exceed V_{DD}. The EN11 pin's input logic high/low threshold is 0.84V/0.36V.
12	EN12	In/Out, OD/PP	**Sequencer output 12, general-purpose output 12, power button (active low).** The EN12 pin has multiple functions, and can be configured as either an output or input. Open-drain output: Connect this pin to a voltage with a resistor (e.g. 10kΩ), regardless of whether this pin is used. It is recommended that the pull-up voltage not exceed V_{DD}. Push-pull output: No external pull-up resistor is required. Float this pin if it is not used. Input: The power button (NPWR_BTN) function is enabled. Connect this pin to a voltage with a resistor (e.g. 10kΩ). It is recommended that the pull-up voltage not exceed V_{DD}. The EN12 pin's input logic high/low threshold is 0.84V/0.36V.
13	CLK32K	Out, OD	**32.768kHz clock output.** The CLK32K pin is an open-drain status pin that outputs the 32.768kHz square wave signal. Connect CLK32K to a voltage with a resistor (e.g. 10kΩ). It is recommended that the pull-up voltage not exceed V_{DD}. Float this pin if it is not used.
14	XIN	In	**Crystal oscillator input.** The XIN pin can be selected for on-chip or external load capacitors. When the crystal driver is enabled, place a 32.768kHz, 12.5pF load capacitance crystal between the XIN and XOUT pins. If the chip is configured as an external load capacitor, use a C0G ceramic capacitor as the crystal load capacitor. Float this pin if it is not used.
15	XOUT	Out	**Crystal oscillator output.** The XOUT pin can be selected for on-chip or external load capacitors. When the crystal driver is enabled, place a 32.768kHz, 12.5pF load capacitance crystal between the XIN and XOUT pins. If the chip is configured as an external load capacitor, use a C0G ceramic capacitor as the crystal load capacitor. Float this pin if it is not used.

PIN FUNCTIONS *(continued)*

Pin #	Name	Type	Description
16	GND	Supply	**Ground.** Electrically connect the GND pin to the system ground plane with the shortest, lowest-impedance connection possible.
17	VDD	Supply	**Input supply voltage.** The VDD pin supplies power to the chip. Bypass VDD to GND with an external, low-ESR, 1µF to 10µF ceramic capacitor. Place the bypass capacitors as close to the chip as possible.
18	VBAT	Supply	**Backup battery input.** If there is an emergency and V_{DD} is off, the VBAT pin supplies power to part of the digital block to maintain the register data. Bypass VBAT to GND with an external, low-ESR, 1µF to 10µF ceramic capacitor. Place the bypass capacitors as close to the chip as possible. Float this pin if it is not used.
19, 20, 21, 22, 23, 24	EN1, EN2, EN3, EN4, EN5, EN6	Out, OD/PP	**Sequencer outputs 1–6.** The EN1–EN6 pins have an optional output: open drain or push-pull. Open drain: Connect this pin to a voltage with a resistor (e.g. 10kΩ), regardless of whether this pin is used. It is recommended that the pull-up voltage not exceed V_{DD}. Push-pull: No external pull-up resistor is required. Float this pin if it is not used.
PAD	Exposed pad	-	**Exposed pad.** This pad is not connected to internal circuit. Connect the pad to the GND plane to improve thermal performance.

ABSOLUTE MAXIMUM RATINGS (1)

All pins ..... -0.3V to +6V
Continuous power dissipation (T_A = 25°C) (2)
QFN-24 (4mmx4mm) 2W
Junction temperature ..... 150°C
Lead temperature ..... 260°C
Storage temperature ..... -65°C to +260°C

Electrostatic Discharge (ESD) Ratings

Human body model (HBM) ..... Class 2 (3)
Charged device model (CDM)..... Class C2b (4)

Recommended Operating Conditions

Supply voltage (V_{DD}) ..... 2.7V to 5.5V
Operating junction temp (T_J) .... -40°C to +150°C

Thermal Resistance (5) θ_{JA} θ_{JC} θ_{JB}

QFN-24 (4mmx4mm)……...62…4.8…32..°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can produce an excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) Per AEC-Q100-002.
4) Per AEC-Q100-011.
5) Measured on JESD51-7, 4-layer PCB. The values given in this table are only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

ELECTRICAL CHARACTERISTICS

Typical values are V_{DD} = 5V, T_J = 25°C, all voltages with respect to ground, unless otherwise noted. Minimum and maximum values are at V_{DD} = 5V, T_J = -40°C to +150°C, all voltages with respect to ground, guaranteed by characterization, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
VDD Supply						
Supply voltage	V_{DD}		2.7		5.5	V
VDD under-voltage lockout (UVLO) rising threshold	$UVLO_{VTH\_R}$	VDD power up from backup state (BACKUP)	2.4	2.6	2.7	V
VDD UVLO falling threshold	$UVLO_{VTH\_F}$		2.2	2.4	2.5	V
V_{IN} UVLO threshold hysteresis	$UVLO_{HYS}$			200		mV
VDD supply current (quiescent)	I_Q	Normal mode (internal clock activated), SHDN/ ACTIVE/SLEEP state, shutdown sequence complete		600	1000	µA
		Low-power mode (internal clock deactivated), SHDN state, shutdown sequence complete		74	200	
		Low-power mode (internal clock deactivated), ACTIVE/SLEEP state, shutdown sequence complete		120	250	
		During BIST execution			10	mA
VBAT Supply						
Backup battery supply voltage	V_{BAT}		1.85		5.5	V
Battery voltage UVLO	$UVLO_{BB}$	Falling		1.55	1.85	V
VBAT current in BACKUP mode	I_{BB}			12	50	µA
ACT/SHDN, ACT/SLP						
Input logic high	V_{IH}		0.84			V
Input logic low	V_{IL}				0.36	V
Enable input pull-down resistor	R_{PD}	Enable input pull-down to ensure safe state in case of open circuit on enable pin		100		kΩ
EN1–EN12 Pins (Configurable as Push-Pull or Open Drain)						
Output high	V_{OHEN}	Configured as push-pull, 1mA source current	V_{DD} - 0.3			V
Output low	V_{OLEN}	If configured as open drain, use 10kΩ external pull-up resistor to 1.8V			0.1	V
Output resistance	R_{ONEN}	Push		180		Ω
		Pull		160		Ω
Delay of ENx/CLK32K from trigger (6)	t_{SLOT1} + t_{SL_EN}	Sequence requiring NRST assertion		t_{NRST} + 2.5	t_{NRST} + 10	µs
		Sequence not requiring NRST assertion		2.5	10	µs
Intra-slot ENx delay (6)	t_{EN_EN}	In the same slot			1	µs
ENx delay from NRST in emergency shutdown (6)	t_{NRST_EN}	Sequence 2 and Sequence 9	200	400		ns

ELECTRICAL CHARACTERISTICS *(continued)*

Typical values are V_{DD} = 5V, T_J = 25°C, all voltages with respect to ground, unless otherwise noted. Minimum and maximum values are at V_{DD} = 5V, T_J = -40°C to +150°C, all voltages with respect to ground, guaranteed by characterization, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
EN1–EN12 Output Readback for Diagnostic						
Input logic high	V_{IHEN}	Push-pull only		0.75 x V_{DD}		V
Input logic low	V_{ILEN}	Push-pull and open-drain		0.4		V
ENx fault self-diagnose time (6)	t_{F_EN}	From EN_X short to GND (or VDD) fault to NIRQ assert		6	12	µs
EN10–EN12 (Configurable as Input: NEM_PD, NRST_IN, NPWR_BTN)						
Input logic high	V_{IHEN}	Configured as input	0.84			V
Input logic low	V_{ILEN}	Configured as input			0.36	V
NRST, NIRQ (Open Drain)						
Input logic low	V_{IL}			0.4		V
Output low	V_{OL}	With 10kΩ external pull-up resistor to 1.2V			0.1	V
		With 10kΩ external pull-up resistor to 1.8V			0.1	V
Shutdown trigger to NRST assertion latency	t_{NRST}	For controlled shutdown and V_{DD} UVLO			15	µs
Fault detection to NIRQ assertion latency	t_{NIRQ}	For all fault except F_OSC			15	µs
Built-In Self-Test (BIST)						
POR to ready with BIST	t_{CFG_WB}	Include BIST,OTP load			15	ms
POR to ready without BIST	t_{CFG_NB}	Include OTP load			2.5	ms
BIST time	t_{BIST}	AT_POR = 1 or AT_SHDN			12.5	ms
Crystal Driver and 32kHz Output (Open Drain)						
Operating voltage		V_{DD} > $UVLO_{VTH\_R}$		V_{DD}		V
		V_{DD} < $UVLO_{VTH\_F}$ and V_{BAT} > $UVLO_{BB}$		V_{BAT}		V
CLK32K output low	V_{OLCK}	With 4.7kΩ external pull-up resistor to 1.2V			0.1	V
		With 4.7kΩ external pull-up resistor to 1.8V			0.1	V
CLK32K output frequency	f_{32K}			32768		Hz
CLK32K output duty cycle	D_{32K}		40	50	60	%
CLK32K output rising time (7) (8)	t_{32K_R}	From 20% to 80% rising edge, with 4.7kΩ external pull-up resistor, 10pF load capacitance		400		ns
CLK32K output falling time (7) (8)	t_{32K_F}	From 80% to 20% falling edge, with 4.7kΩ external pull-up resistor, 10pF load capacitance		20		ns
Early boot CLK32K frequency accuracy	Acc_{EB32K}	<50ms after UVLO	-10		+10	%
Operating CLK32K frequency accuracy	Acc_{32K}	>1s after UVLO, T_A = 25°C	-100		+100	ppm
Start-up time	t_{32K_GOOD}	From $UVLO_{VTH\_R}$ to first cycle reaches early boot CLK32K			50	ms

ELECTRICAL CHARACTERISTICS *(continued)*

Typical values are V_{DD} = 5V, T_J = 25°C, all voltages with respect to ground, unless otherwise noted. Minimum and maximum values are at V_{DD} = 5V, T_J = -40°C to +150°C, all voltages with respect to ground, guaranteed by characterization, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Frequency fault	f_{FAULT}	f_{32K} > 32.768kHz		17		%
		f_{32K} < 32.768kHz		-16		
Fault detection time	t_{XTALF}	f_{32K} > 10kHz when fault detected			1	ms
Internal Oscillator Clock						
Internal oscillator clock frequency	f_{CKI}		2.375	2.5	2.625	MHz
Thermal Shutdown						
Thermal shutdown (7)	T_{SD}	T_J rising		175		°C
Thermal shutdown hysteresis (7)	T_{SD-HYS}			20		°C

Notes:

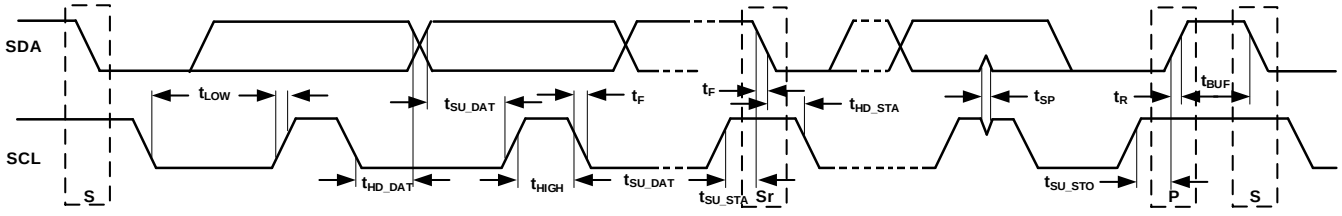
6) ENx represents any channel from EN1 to EN12.
7) Not tested in production. Guaranteed by design and characterization.
8) This value is mainly determined by external pull-up resistor, load capacitance, and the internal MOSFET's parasitic capacitance.

I²C INTERFACE ELECTRICAL CHARACTERISTICS

Typical values are V_{DD} = 5V, T_J = 25°C, all voltages with respect to ground, unless otherwise noted. Minimum and maximum values are at V_{DD} = 5V, T_J = -40°C to +150°C, all voltages with respect to ground, guaranteed by characterization, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
I²C Interface Specifications (Capable of 1.2V/1.8V and 3.3V Signaling)						
Input logic high	V_{IHI2C}	V_{IH} of 1.2V/1.8V, Reg 0xFA, bits[1:0] = 00b	0.84			V
		V_{IH} of 3.3V, Reg 0xFA, bits[1:0] = 10b	1.29			
Input logic low	V_{ILI2C}	V_{IL} of 1.2V/1.8V, Reg 0xFA, bits[1:0] = 00b			0.36	V
		V_{IL} of 3.3V, Reg 0xFA, bits[1:0] = 10b			0.76	
Output low	V_{OLI2C}	SDA with 10kΩ pull-up resistor, both for 1.2V/3.3V signaling			0.1	V
Input capacitance	C_{SDA} / C_{SDL}			5		pF
SCL clock frequency	f_{SCL}				1	MHz
SCL high time	t_{HIGH}		0.26			µs
SCL low time	t_{LOW}		0.5			µs
Data set-up time	t_{SU_DAT}		50			ns
Data hold time	t_{HD_DAT}		0			µs
Set-up time for repeated start condition	t_{SU_STA}		0.26			µs
Hold time for start	t_{HD_STA}		0.26			µs
Bus free time between a start and stop condition	t_{BUF}		0.5			µs
Set-up time for stop condition	t_{SU_STO}		0.26			µs
SCL and SDA rising time	t_R				120	ns
SCL and SDA falling time	t_F		20 x (V_{DD} / 5.5V)		120	ns
Suppressed spike pulse width	t_{SP}		0		50	ns
Capacitance bus for each bus line	C_B				550	pF

I²C-COMPATIBLE INTERFACE TIMING DIAGRAM

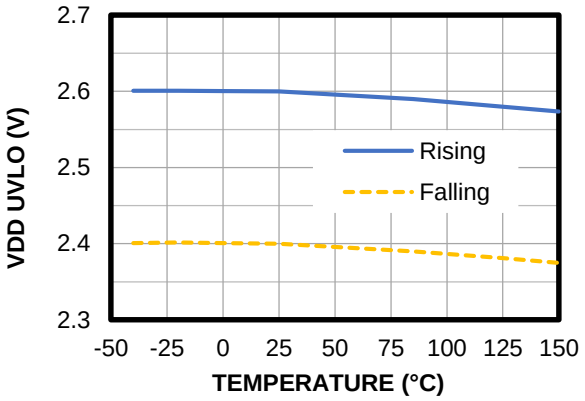


S = Start Condition
Sr = Repeated Start Condition
P = Stop Condition

TYPICAL CHARACTERISTICS

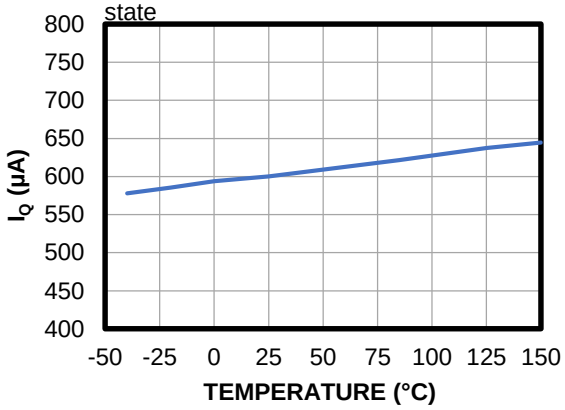
V_{DD} = 5V, T_J = -40°C to +150°C, unless otherwise noted.

VDD UVLO Threshold vs. Temperature



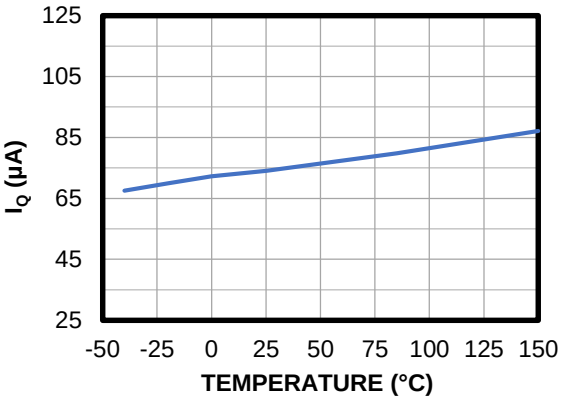
Quiescent Current vs. Temperature

Normal mode, SHDN/ACTIVE/SLEEP state



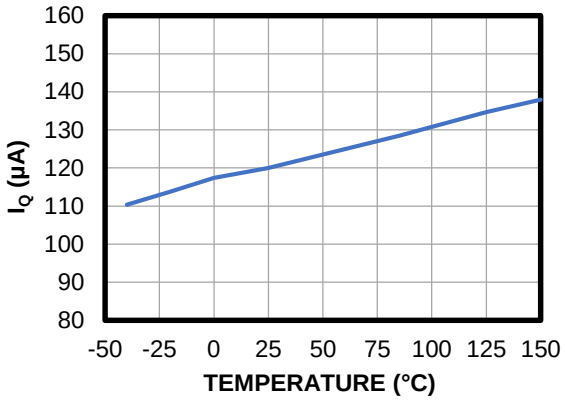
Quiescent Current vs. Temperature

Low power mode, SHDN state



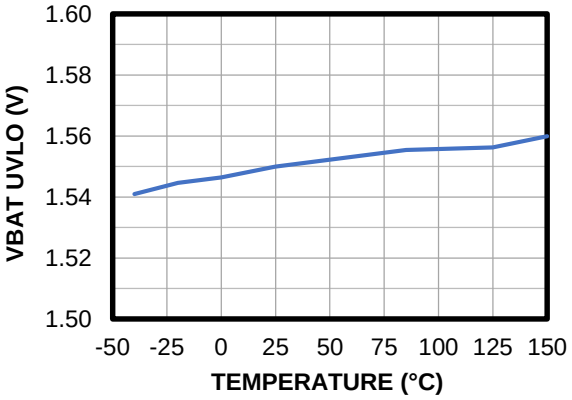
Quiescent Current vs. Temperature

Low power mode, ACTIVE/SLEEP state

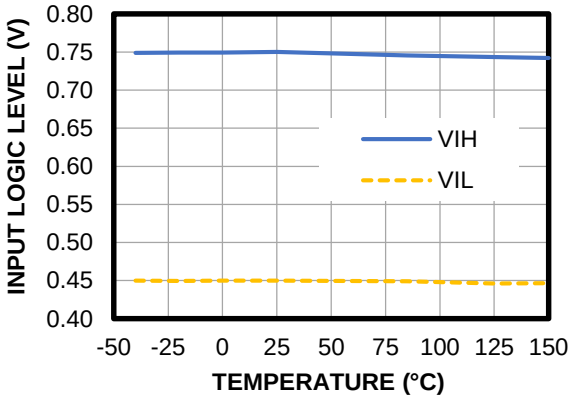


VBAT UVLO Threshold vs. Temperature

Falling



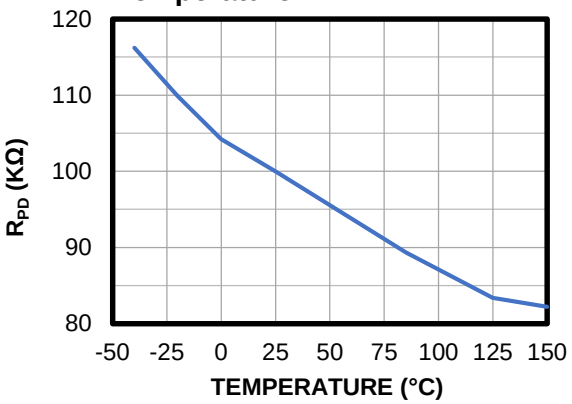
ACT/SHDN and ACT/SLP Input Logic Level vs. Temperature



TYPICAL CHARACTERISTICS *(continued)*

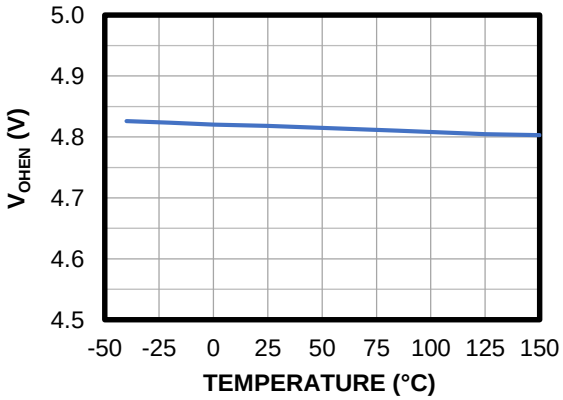
V_{DD} = 5V, T_J = -40°C to +150°C, unless otherwise noted.

ACT/SHDN and ACT/SLP Input Pulldown Resistor vs. Temperature



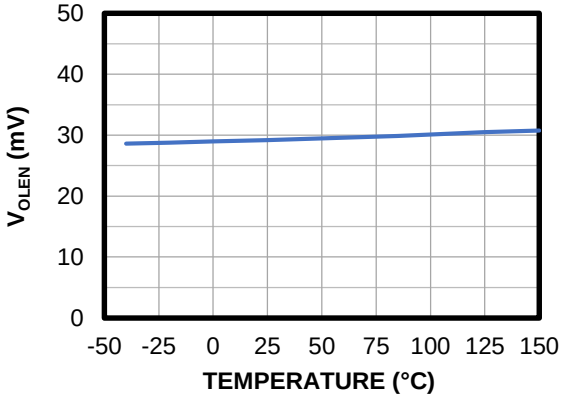
ENx Output High vs. Temperature

Push-pull, source 1mA load



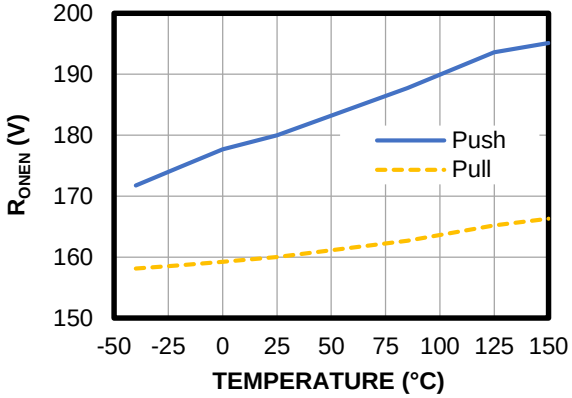
ENx Output Low vs. Temperature

Open-drain, 10kΩ pull up resistor to 1.8V



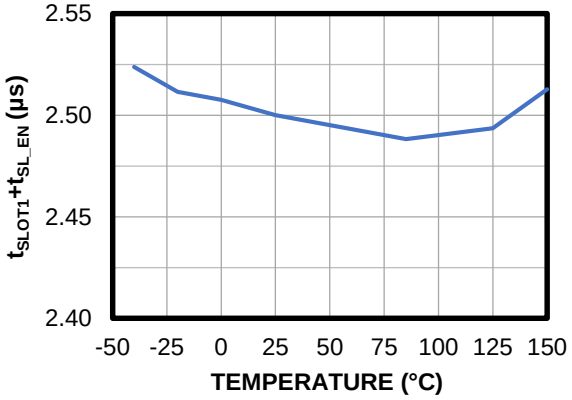
ENx Output Resistance vs. Temperature

Push-pull



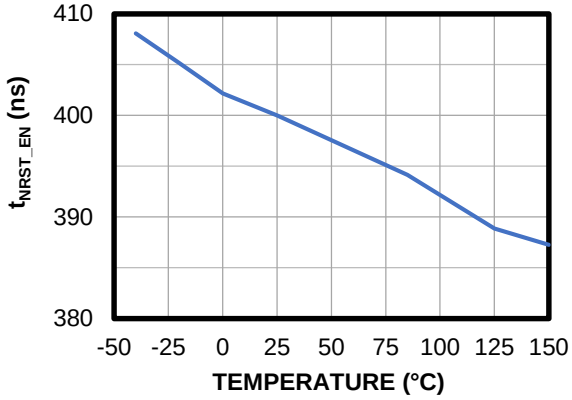
Delay of ENx/CLK32K from Trigger vs. Temperature

Sequence not requiring NRST assertion



t_{NRST_EN} vs. Temperature

In sequence 2 or sequence 9

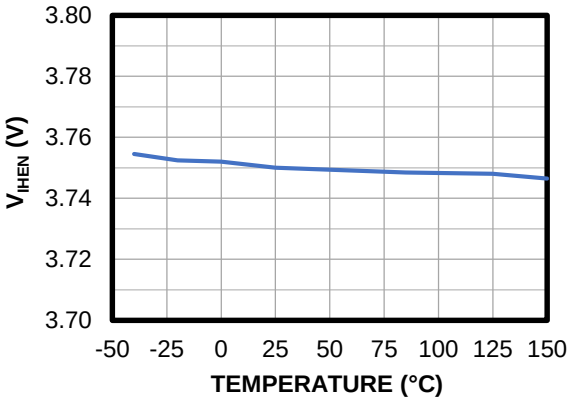


TYPICAL CHARACTERISTICS *(continued)*

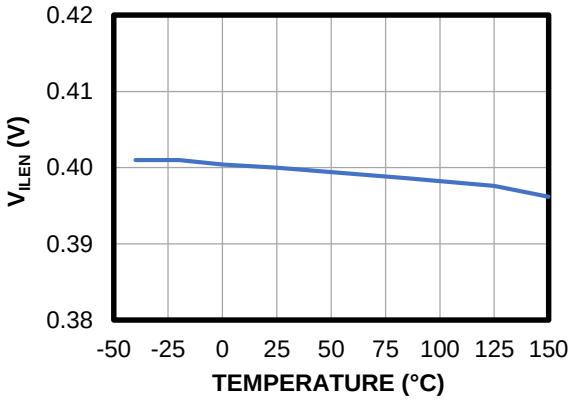
V_{DD} = 5V, T_J = -40°C to +150°C, unless otherwise noted.

ENx Input Logic High vs. Temperature

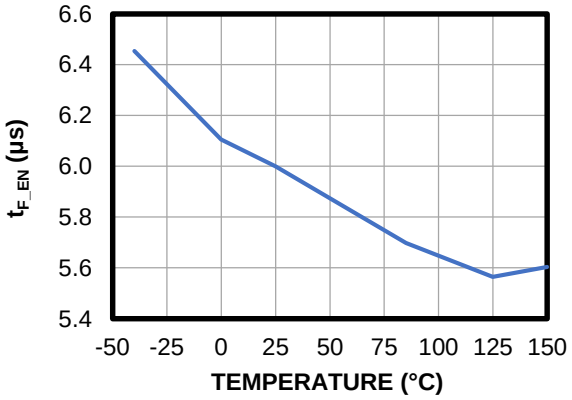
Push-pull, V_{DD} = 5V



ENx Input Logic Low vs. Temperature



ENx Fault Self-diagnose Time vs. Temperature

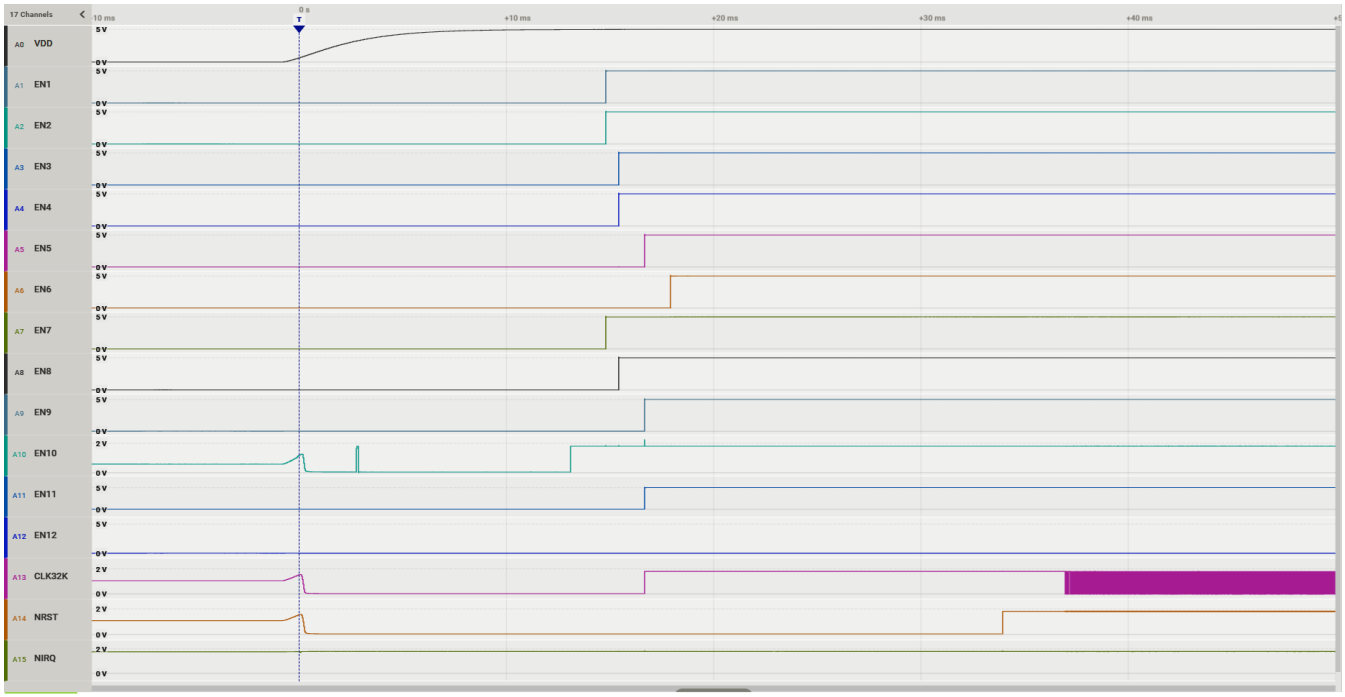


TYPICAL PERFORMANCE CHARACTERISTICS

V_{DD} = 5V, V_{PU} = 1.8V, V_{BAT} = 5V, default OTP configured as shown in the Register Map section on page 44, T_A = 25°C, unless otherwise noted.

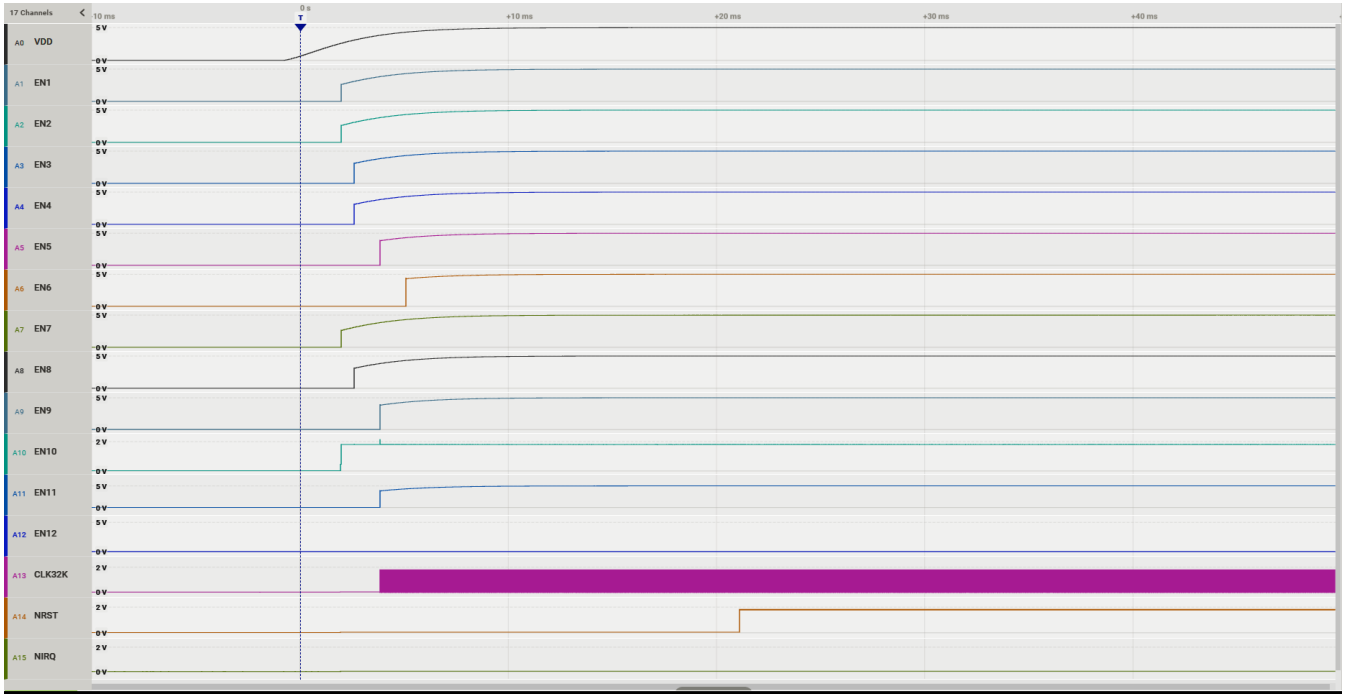
VDD Start-Up from OFF State with ACT/SHDN High

EN10 (NEM_PD) = high, ACT/SHDN = high



VDD Start-Up from BACKUP State with ACT/SHDN High

EN10 (NEM_PD) = high, ACT/SHDN = high



TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

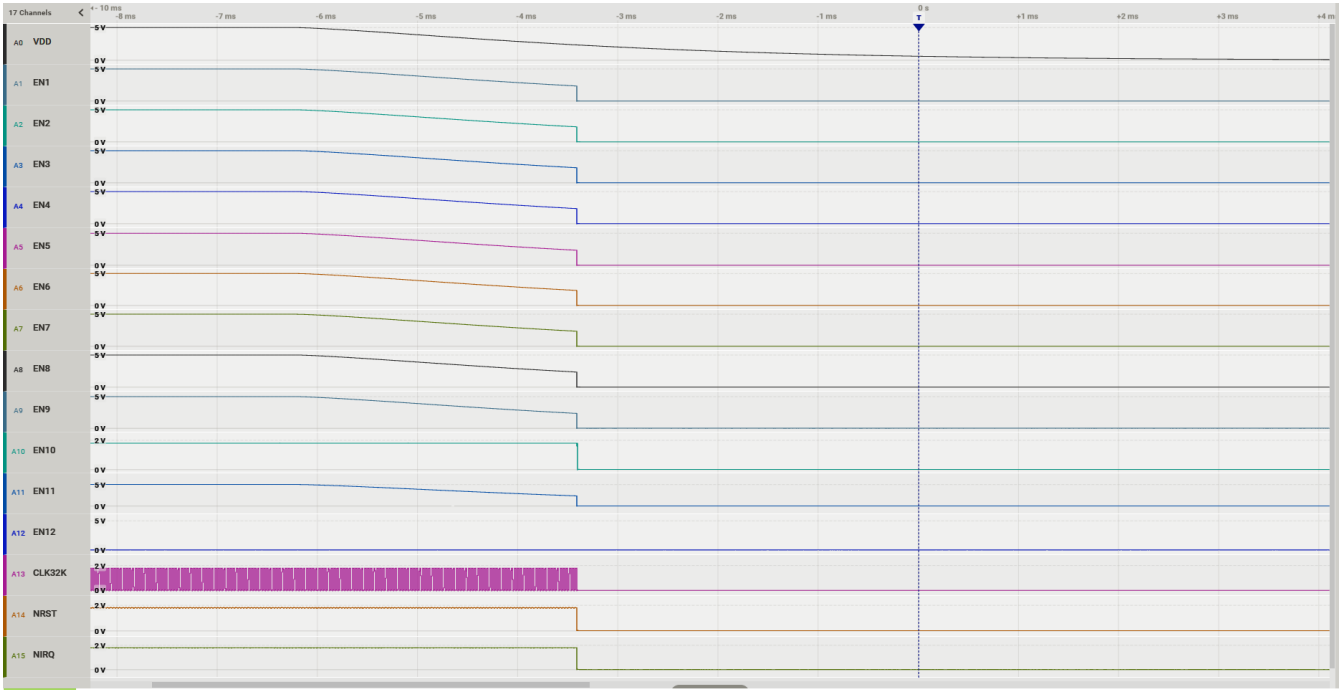
V_{DD} = 5V, V_{PU} = 1.8V, V_{BAT} = 5V, default OTP configured as shown in the Register Map section on page 44, T_A = 25°C, unless otherwise noted.

Sequence 1: Power Up from SHDN1 to ACTIVE by ACT/SHDN Control

EN10 (NEM_PD) = high

Sequence 2: VDD Emergency Power Down from ACTIVE to BACKUP

EN10 (NEM_PD) = high, ACT/SHDN = high



TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

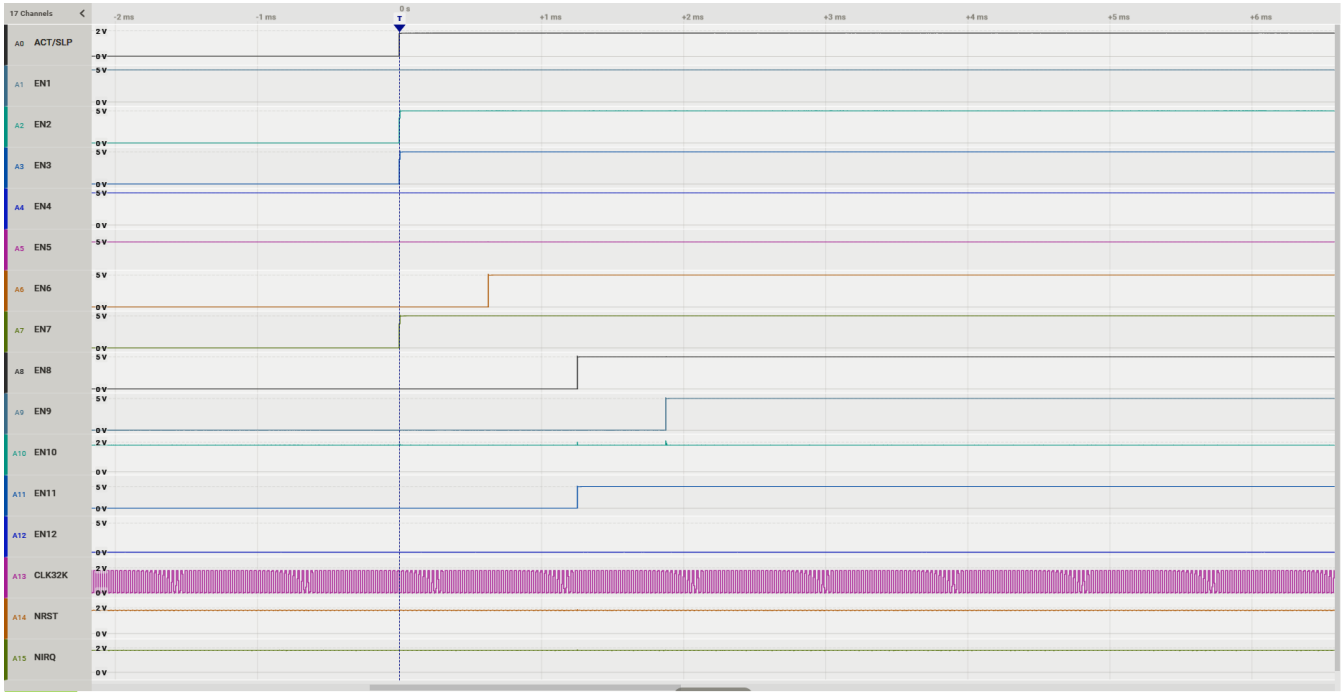
V_{DD} = 5V, V_{PU} = 1.8V, V_{BAT} = 5V, default OTP configured as shown in the Register Map section on page 44, T_A = 25°C, unless otherwise noted.

Sequence 3: SLEEP Entry via ACT/SLP Control

EN10 (NEM_PD) = high, ACT/SHDN = high, register 0x28, bit[2] = 0b

Sequence 4: SLEEP Exit via ACT/SLP Control

EN10 (NEM_PD) = high, ACT/SHDN = high, register 0x28, bit[2] = 0b

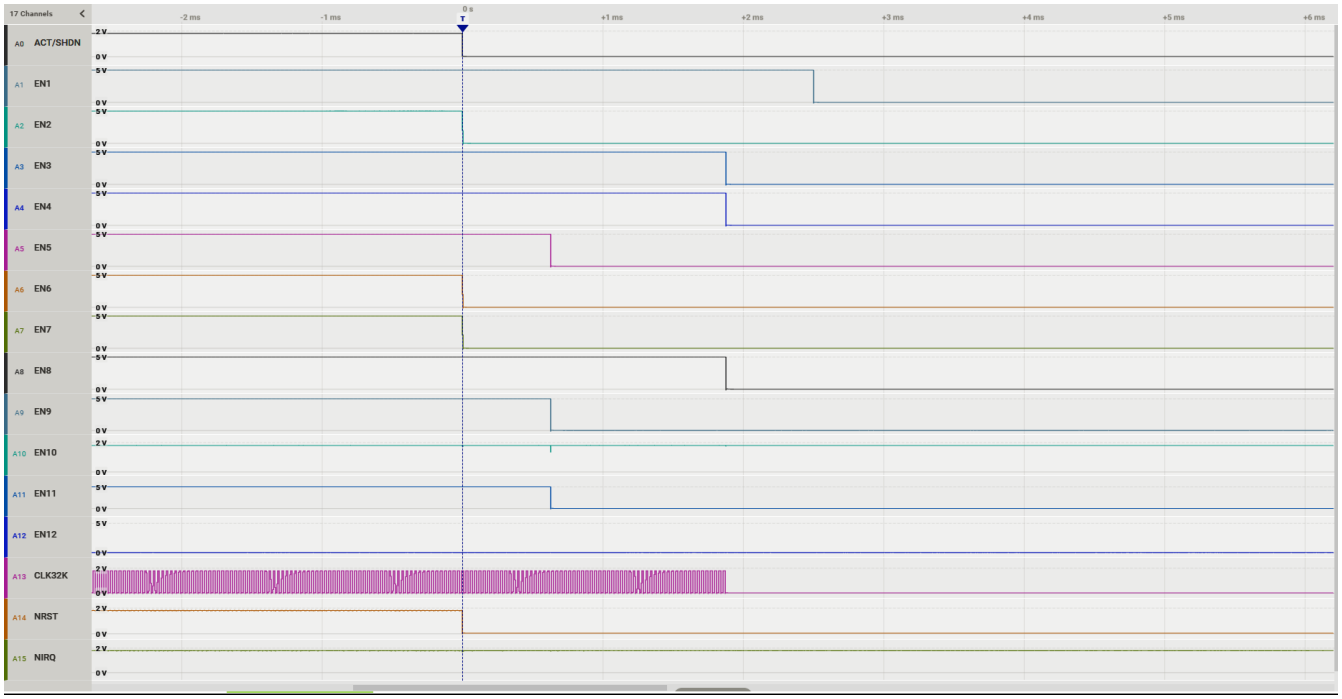


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{DD} = 5V, V_{PU} = 1.8V, V_{BAT} = 5V, default OTP configured as shown in the Register Map section on page 44, T_A = 25°C, unless otherwise noted.

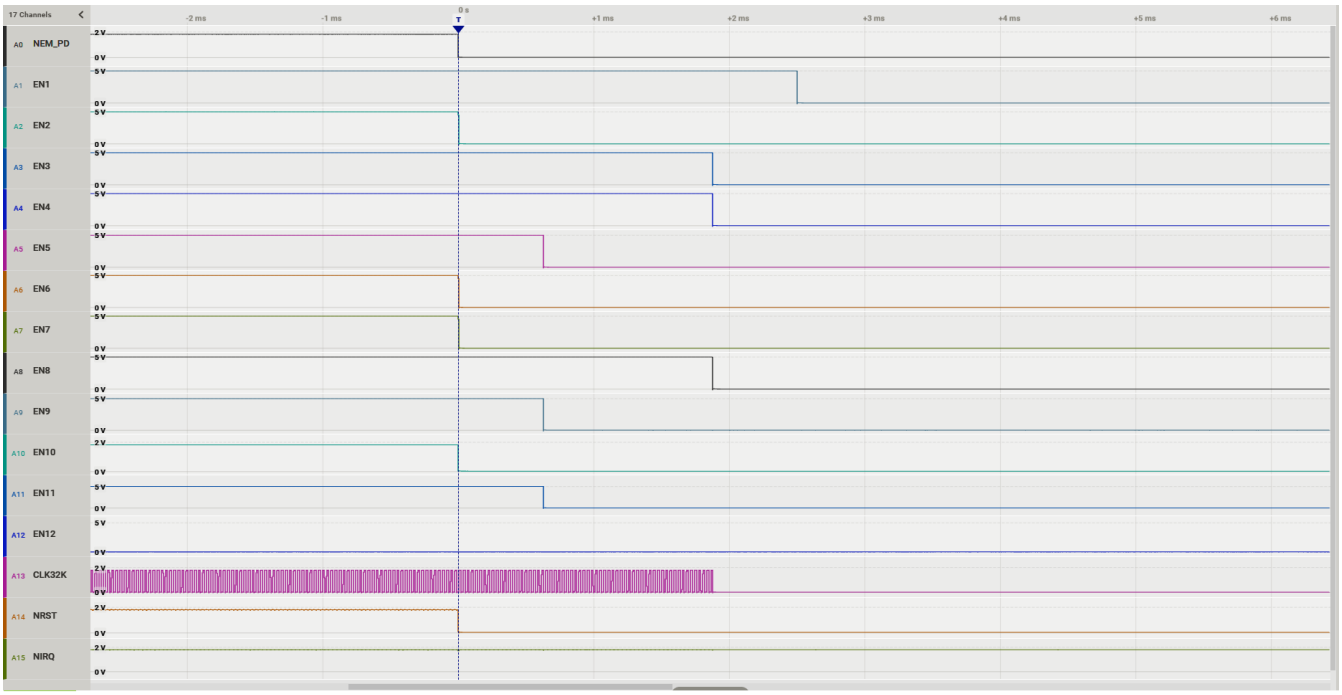
Sequence 5: Power Down from ACTIVE to SHDN1 via ACT/SHDN Control

EN10 (NEM_PD) = high



Sequence 5: Power Down from ACTIVE to SHDN2 via NEM_PD Assertion

ACT/SHDN = high

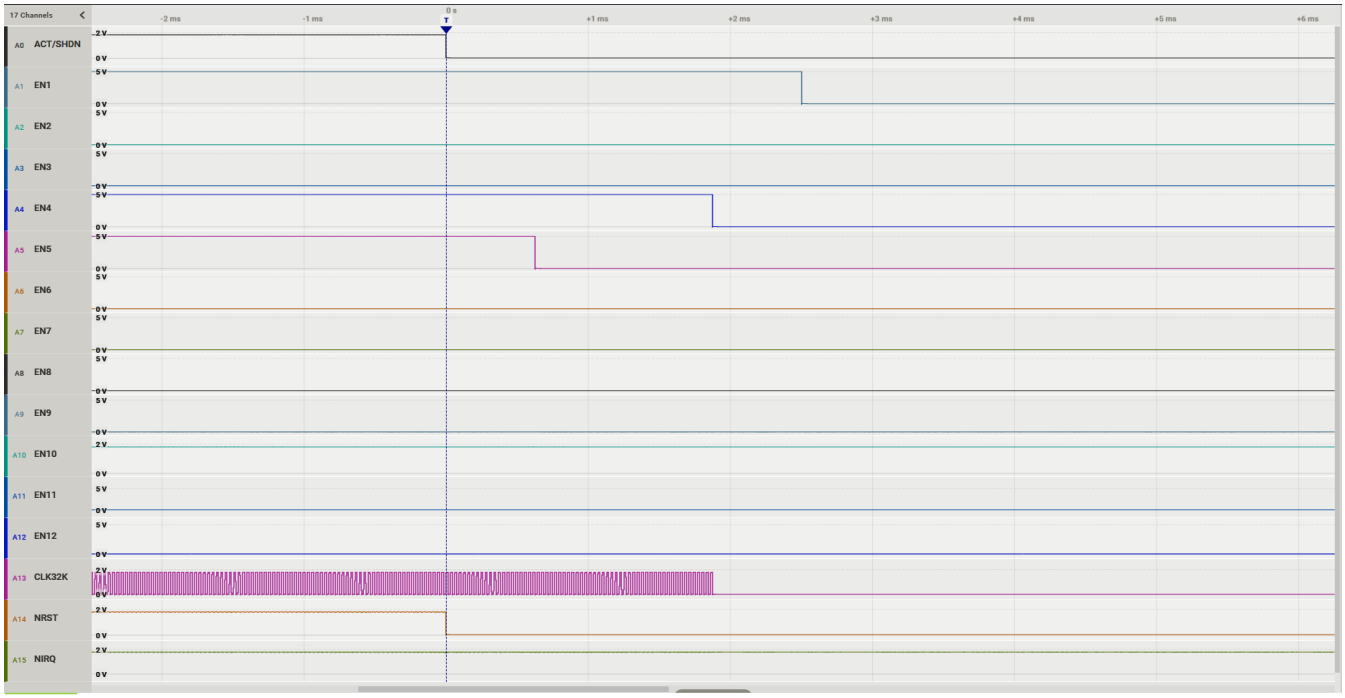


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{DD} = 5V, V_{PU} = 1.8V, V_{BAT} = 5V, default OTP configured as shown in the Register Map section on page 44, T_A = 25°C, unless otherwise noted.

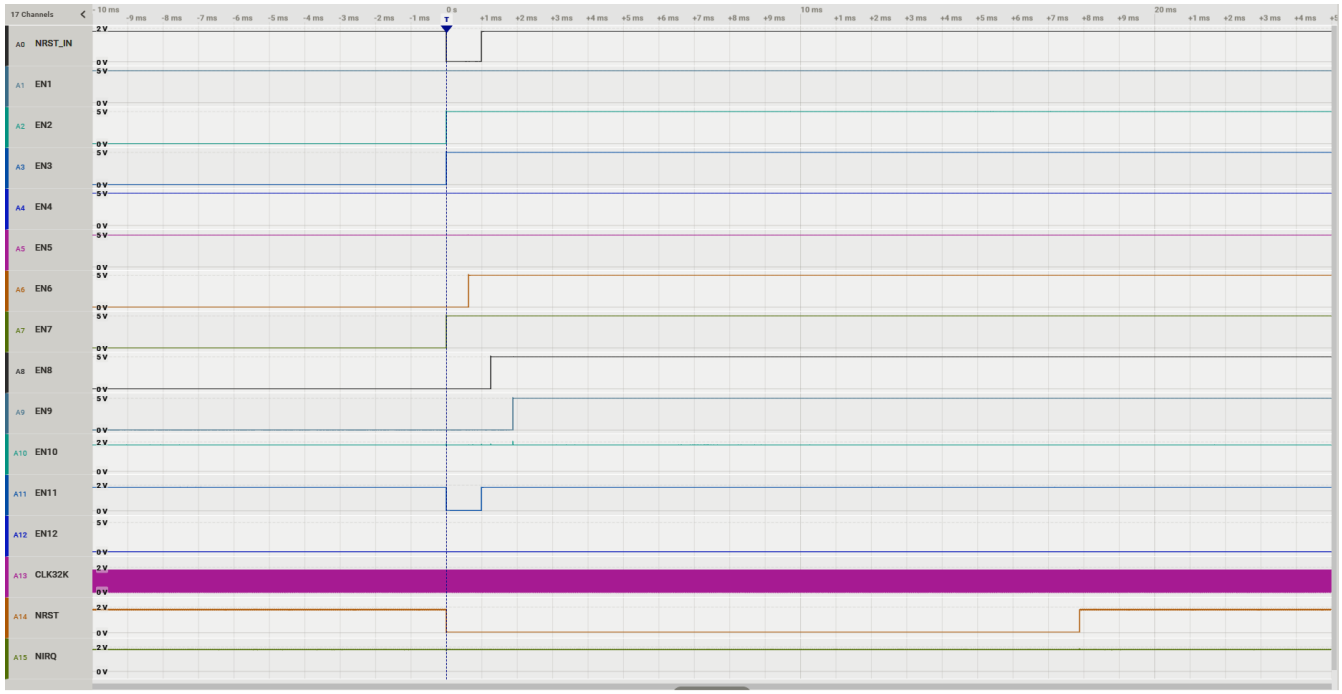
Sequence 6: Power Down from SLEEP to SHDN1 by ACT/SHDN Controlled

EN10 (NEM_PD) = high, ACT/SLP = low, register 0x28, bit[2] = 0b



Sequence 7: SLEEP Exit Due to NRST_IN Assertion

EN10 (NEM_PD) = high, EN11 configured via NRST_IN (registers 0x20, bit[2] = 1b, 0x21, bit[2] = 1b, 0x3D = 00h, 0x5D = 00h)

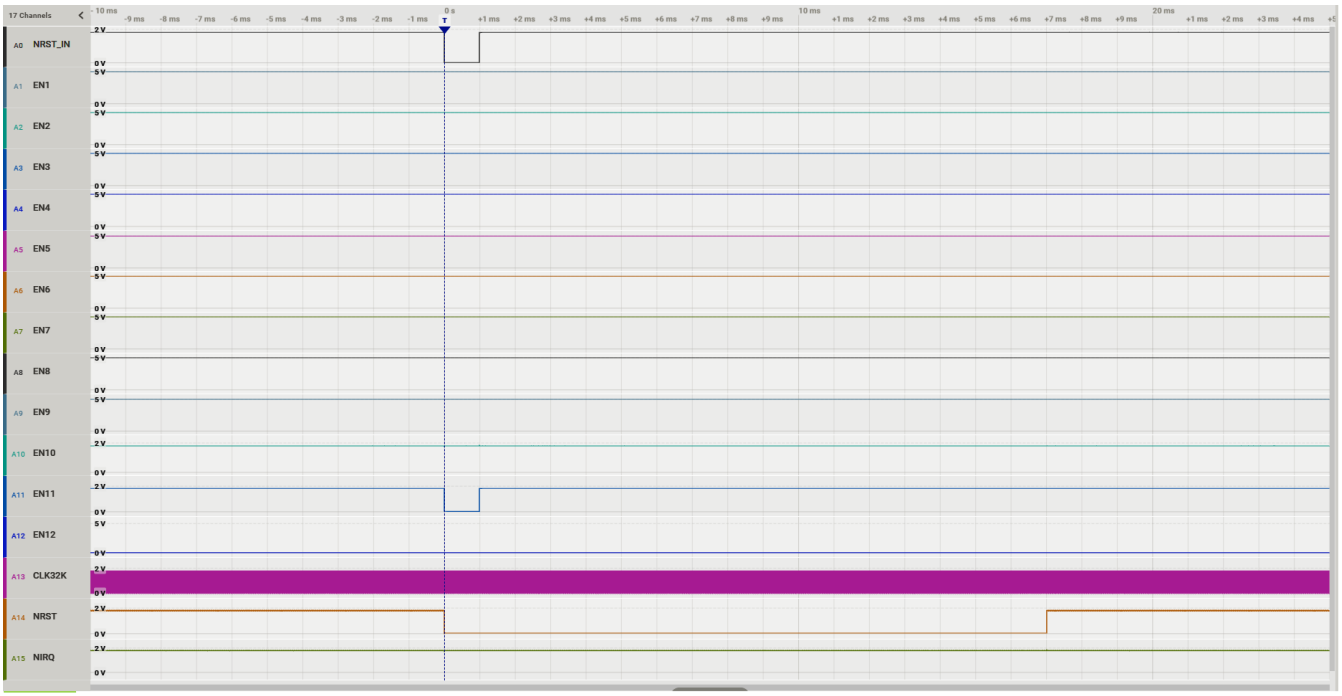


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{DD} = 5V, V_{PU} = 1.8V, V_{BAT} = 5V, default OTP configured as shown in the Register Map section on page 44, T_A = 25°C, unless otherwise noted.

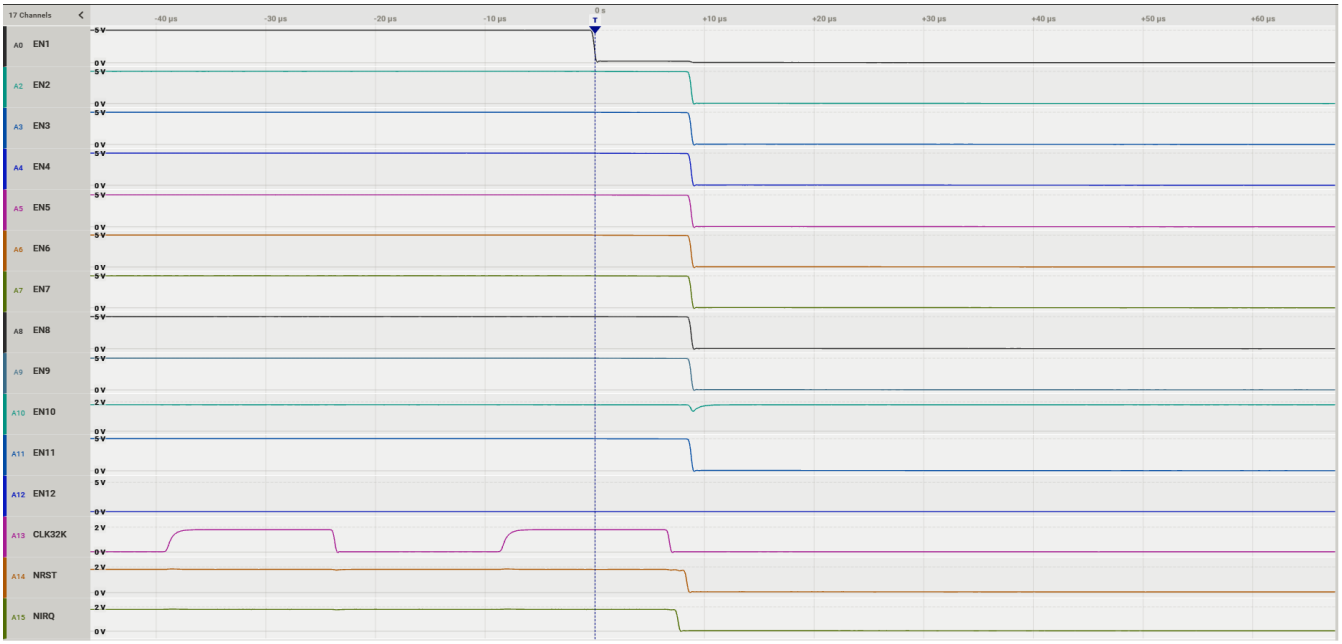
Sequence 8: Reset Due to NRST_IN Assertion

EN10 (NEM_PD) = high, EN11 configured as NRST_IN (registers 0x20, bit[2] = 1b, 0x21, bit[2] = 1b, 0x3D = 00h, 0x5D = 00h)



Sequence 9: FAILSAFE Power Down from ACTIVE via F_EN

EN10 (NEM_PD) = high, Pull EN1 to GND



FUNCTIONAL BLOCK DIAGRAM

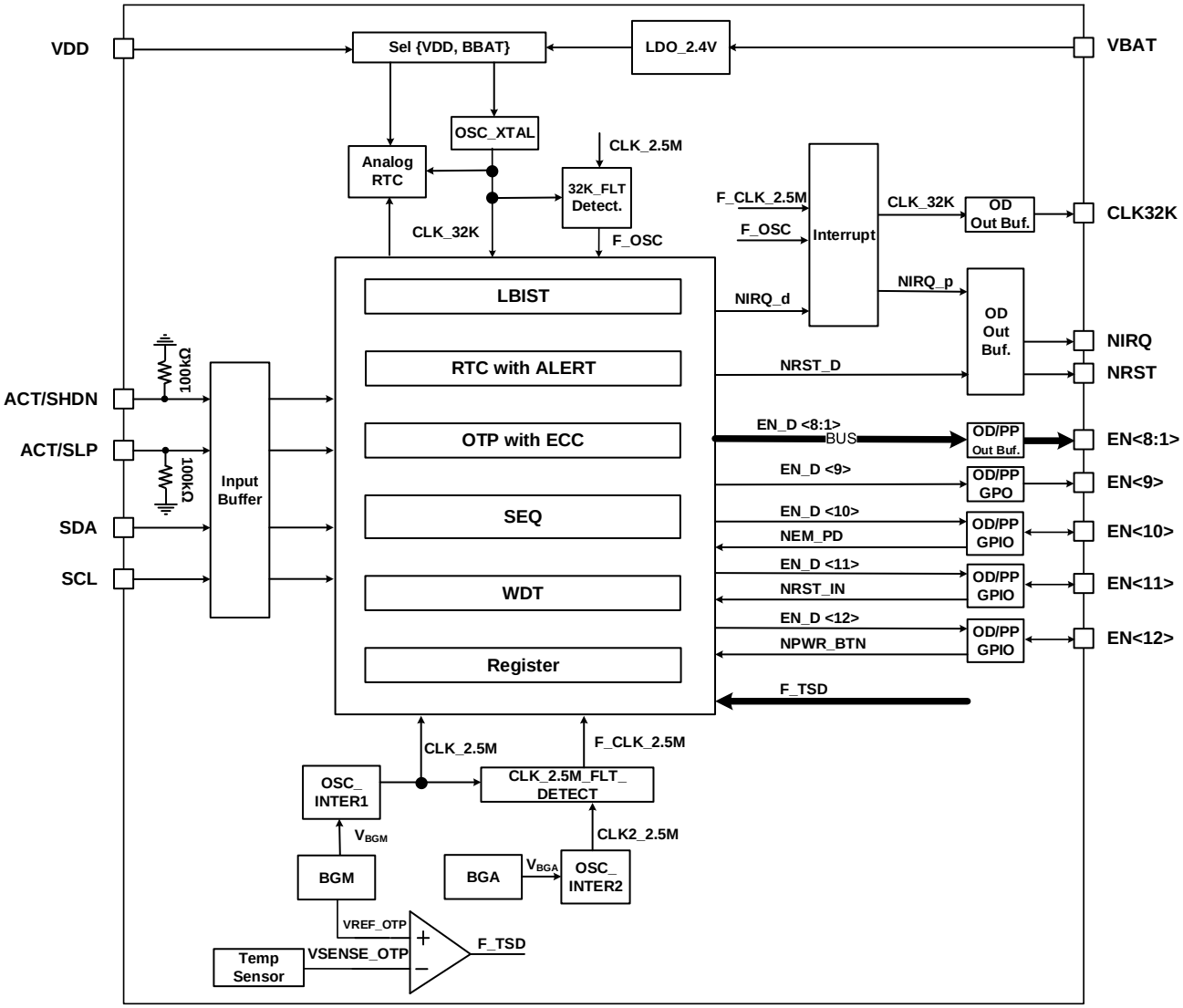


Figure 1: Functional Block Diagram

OPERATION

The MPQ79700FS is a 12-channel functional safety power sequencer engineered for automotive advanced driver assistance systems (ADAS) and autonomous driving platforms.

The device provides the essential control and sequencing for the entire platform. Its configurability and flexibility enable design reuse across different applications and system-on-chip (SoC) generations.

The MPQ79700FS contains a crystal driver, a real-time clock (RTC) with an alarm function, a configurable watchdog that can be accessed through the I^2C interface, and active-low system reset and interrupt outputs.

Built-in safety mechanisms such as built-in self-test (BIST) provide high diagnostic coverage, which helps the system achieve the target ASIL-D rating.

Input Supply Voltage and Backup Battery

The VDD supply is the power source for both the internal digital and analog circuits. In addition, a battery can be connected to the VBAT pin to act as a backup power supply. Under-voltage lockout (UVLO) is implemented both for VDD and VBAT to avoid the chip (or certain blocks) from operating at an insufficient supply voltage.

The MPQ79700FS starts up when the VDD voltage (V_{DD}) exceeds its UVLO rising threshold (typically 2.6V), regardless of whether the VBAT voltage (V_{BAT}) is above or below its UVLO threshold (typically 1.55V). When V_{DD} is below its UVLO falling threshold (typically 2.4V), the MPQ79700FS enters BACKUP state if V_{BAT} exceeds its UVLO threshold, or it enters OFF state if V_{BAT} is below its UVLO threshold.

See the Sequencer Operation section on page 23 and Figure 3 on page 24 for details regarding VDD/VBAT operation.

Pin Drive Mode

The MPQ79700FS provides two optional drive modes for the output pins (EN1 to EN12): push-pull (PP) and open-drain (OD) outputs, which can be set via registers EN_CFG1 and EN_CFG2 for each channel, respectively. If OD mode is selected, the ENx pin must be connected to a bus voltage (V_{BUS}) through a resistor (e.g. 10kΩ). V_{BUS} must not exceed V_{DD}. If PP mode is selected, no external resistor is required. In this scenario, the ENx output high level is almost equal to V_{DD}.

The CLK32K, NRST, NRIQ pins are open drain only. They must be connected to a bus voltage via a pull-up resistor (e.g. 10kΩ). In addition, voltage must not exceed V_{DD}.

Note that the EN10, EN11, and EN12 pins can be configured as input pins via registers EN_ALT_F and AF_IN_OUT. If configured as input pins, an input signal can be directly applied on the pins, even if they are in OD or PP mode. The input signal's high level cannot exceed V_{DD}.

Internal Clocks

The MPQ79700FS integrates one internal clock and one crystal oscillator driver (see Figure 2).

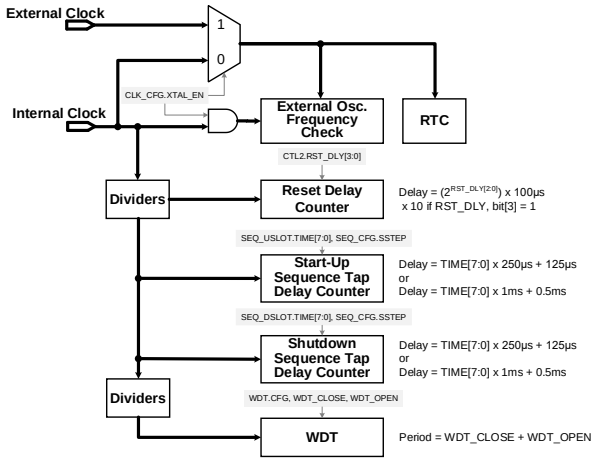


Figure 2: Clock Diagram

With an external crystal oscillator, the crystal oscillator driver generates the 32.768kHz reference clock for applications. The internal oscillator frequency is 2.5MHz with ±5% accuracy, and is used to monitor if the 32.768kHz crystal oscillator frequency is out of ±15% tolerance. Once the fault is detected, a flag is set in register INT_SRC1.F_OSC and NIRQ assert to alert host.

The CLK32K clock output and RTC use the crystal oscillator as the time base (in other words, they use the internal oscillator only if XTAL_EN = 0). The time base for the MPQ79700FS delays and the watchdog timer (WDT) depend on the internal clock.

Sequencer Operation

Once V_{DD} exceeds its under-voltage lockout (UVLO) threshold ($UVLO_{VTH\_R}$), the MPQ79700FS starts up. In addition to the primary voltage supply, a VBAT pin is also equipped; this pin is recommended to be connected with a battery as backup power. Both V_{BAT} and V_{DD} are implemented with UVLO to protect the device from turning on accidently.

While powering up the device, V_{DD} must be provided, regardless of the V_{BAT} level. In case of an emergency shutdown in which V_{DD} accidently drops below $UVLO_{VTH\_F}$, the critical functions continue operating if V_{BAT} exceeds its UVLO threshold ($UVLO_{BB}$).

When the device is on, BIST is optionally executed depending on the status of the AT_POR bit, which can only be set via the one-time programmable memory (OTP). Configuration is loaded from the OTP, and is assisted by the error correction code (ECC), supporting single-error correction (SEC) and double-error detection (DED). See the Built-In Self-Test (BIST) and Configuration Load section on page 26 for more details.

The I^2C interface becomes active afterwards. The OTP load and BIST results are reported in the TEST_STAT register. Once the start-up process is complete, the MPQ79700FS operates following a specific state machine (see Figure 3 on page 24).

Figure 3 on page 24 shows the MPQ79700FS's operation, indicating all the events and signals that trigger state changes. Note that states with a white background represent functional sequences that are executed while the device transitions between states. These sequences are run to completion and can be interrupted only by removing power (V_{DD}) or if a failsafe power down is triggered.

The inputs (ACT/SHDN, ACT/SLP, NEM_PD, NRST_IN, and NPWR_BTN) as well as the FORCE_SHDN bits are ignored while these sequences are executed. These inputs and bits are handled once the sequence is complete. The MPQ79700FS acts accordingly based on the state or value of these inputs/bits once sequencing completes.

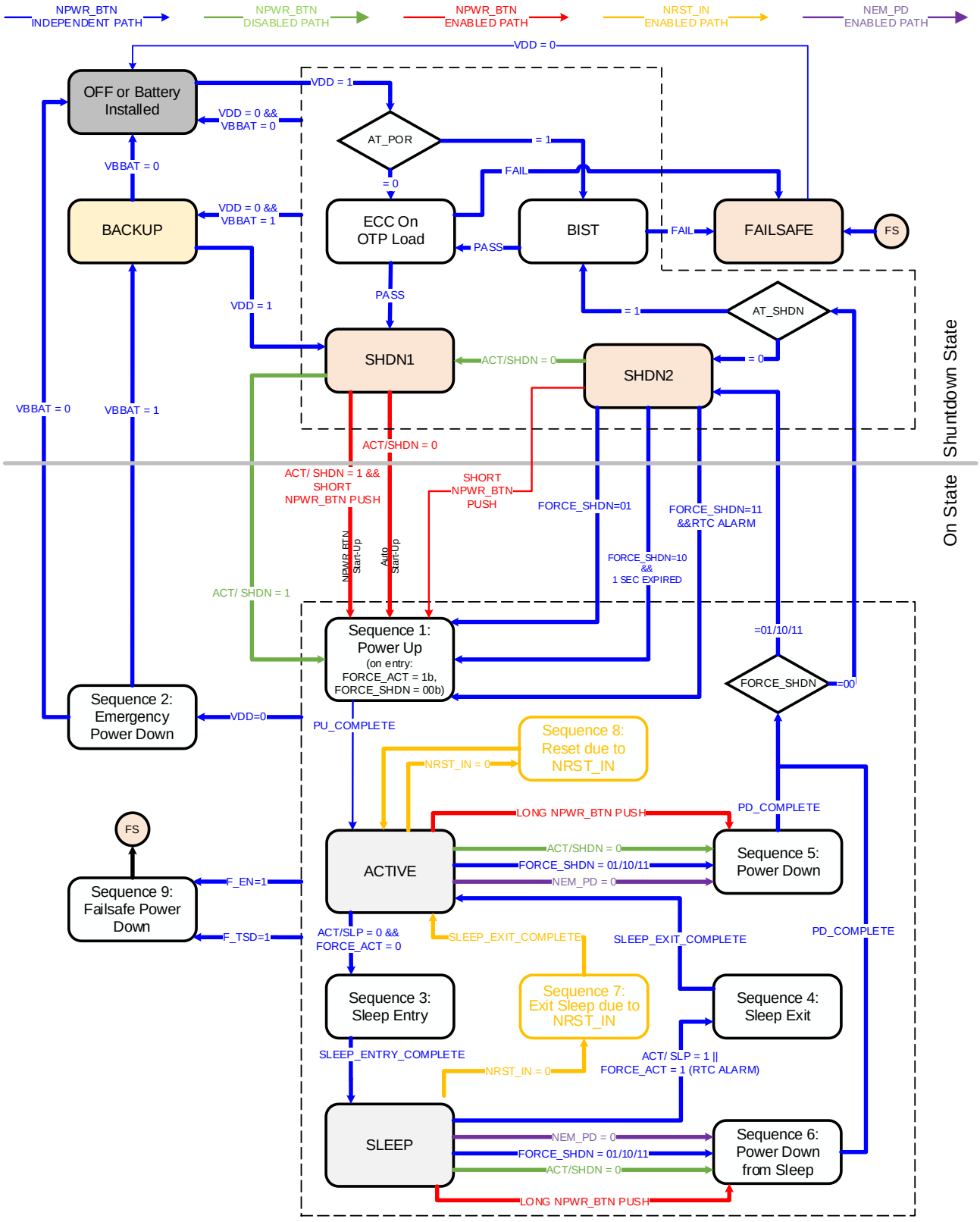


Figure 3: State Diagram

Table 1 describes the signals and registers bits that control the state transitions.

Table 1: State Diagram Control Signals

Signal	Functional Description
ACT/SHDN (pin 4) (or automatic power up sequence control if NPWR_BTN is enabled)	Active/shutdown. Hardware (HW) control for system power up/down from the SHDNx, ACTIVE, and SLEEP states. If ACT/SHDN = 1: Power up sequence command (ACT) If ACT/SHDN = 0: Power down sequence command (SHDN) If NPWR_BTN is enabled via registers EN_ALT_F and AF_IN_OUT, this pin controls the automatic power up sequence when power is applied to the MPQ79700FS (only while the device transitions from SHDN1 to Sequence 1). If ACT/SHDN = 1: Power up sequence requires an NPWR_BTN short push If ACT/SHDN = 0: Power up sequence is automatic when power is applied
ACT/SLP (pin 3)	Active/sleep. HW control to enter ACTIVE and SLEEP sequences. ACT/SLP = 1: Active state entry sequence command ACT/SLP = 0: Sleep state entry sequence command
NEM_PD (pin 10) (alternate function to EN10)	Emergency power down input. HW control for immediate shutdown. See the EN_ALT_F section on page 52 and the AF_IN_OUT section on page 53 for more details. NEM_PD is active low. When it asserts, the MPQ79700FS enters the power down sequence. This input can be optionally debounced (see the DEB_IN section on page 55 for more details).
NRST_IN (pin 11) (alternate function to EN11)	Reset input. HW reset input to force a system reset without power cycling. See the EN_ALT_F section on page 52 and the AF_IN_OUT section on page 53 for details on settings. NRST_IN is active low. When it asserts, the MPQ79700FS resets to the ACTIVE state and asserts the NRST output for the system. NRST de-asserts when NRST_IN de-asserts and RST_DLY has passed (see Figure 14 and Figure 15 on page 31). This input can be optionally debounced (see the DEB_IN section on page 55 for more details).
NPWR_BTN (pin 12) (alternate function to EN12)	Power button input. HW control for power up/down through a button. See the EN_ALT_F section on page 52 and the AF_IN_OUT section on page 53 for more details. NPWR_BTN is active low and it supports two assertion pulses: 1. A short pulse causes the MPQ79700FS to enter the power up sequence from the SHDNx state, or asserts NIRQ when in ACTIVE state. 2. A long pulse causes the MPQ79700FS to enter the power down sequence from the ACTIVE/SLEEP state. Note that a long pulse can be initiated while the MPQ79700FS is asleep, and a wake source (ACT/SLP or an RTC alarm) moves the MPQ79700FS to ACTIVE state. The timer that determines the long pulse should not be reset, and the long pulse detection and process should continue from the ACTIVE state. The short/long pulse is determined by a time setting in register LP_TTSHLD. This input can be optionally debounced (see the DEB_IN section on page 55 for more details).

FORCE_ACT (CTL_1 register, bit[2])	CTL_1, bit[2]. FORCE_ACT set by HW to mask/ignore ACT/SLP if three scenarios occur: 1. Power up from SHDNx state: The ACT/SLP signal may be driven by a system power domain controlled by the MPQ79700FS. Therefore, the ACT/SLP signal may be indeterminate during the power up sequence. By ignoring ACT/SLP during power up, the MPQ79700FS ensures that the signal is valid before performing a sleep entry sequence. 2. Wake from SLEEP on an RTC alarm: When RTC_WAKE is set, FORCE_ACT is set on the RTC alarm, forcing the device to exit the sleep sequence and enter ACTIVE state (see the Real-Time Clock (RTC) section on page 34 for more details). 3. Assertion of NRST_IN. If the NRST_IN pin is enabled (see Sequence 7 on page 32). FORCE_ACT is set when NRST_IN asserts in SLEEP state, forcing the device to exit the sleep sequence and enter ACTIVE state. Sequence 8 is also triggered by NRST_IN assertion, but note that FORCE_ACT is not set in sequence 8. Software on the I²C master device must clear the FORCE_ACT bit to resume normal hardware control over ACT/SLP.
FORCE_SHDN (CTL_1 register, bits[1:0])	CTL_1, bits[1:0]. FORCE_SHDN is used for SW and WDT control of the power down sequence. During a power-on reset (POR) or when ACT/SHDN = 0, FORCE_SHDN is cleared to 00b to indicate normal control by the ACT/SHDN pin (or NPWR_BTN, if enabled), the software may write values other than 00b to shut down and restart under varying conditions, as defined by FORCE_SHDN. WDT-based power down is controlled by WDT_CFG.PDMD, which is the value written to FORCE_SHDN if a watchdog timer violation occurs.

Built-In Self-Test (BIST) and Configuration Load

The MPQ79700FS provides BIST for the critical analog and logic functions. BIST is optionally executed when the device is powered on (depending on the AT_POR bit), and can be compiled online via the AT_SHDN bit (if FORCE_SHDN = 00b) manually after Sequence 5 and Sequence 6. If the power down is initiated by FORCE_SHDN being set to 01b, 10b, or 11b, then BIST is not executed.

BIST is applied to meet ASIL-D safety requirements. Instead of only being checked once during BIST, some safety items are periodically checked while operating. The real-time safety items that are checked are listed below:

- I²C protocol PEC: Data transferring through I²C is attached with a packet error checking (PEC) code. The slave device rejects receiving data unless the PEC matches the master device. PEC is an optional function related to EN_PEC and REQ_PEC (see page 57 for more details).
- NRST, NIRQ short to high check: Note that when NIRQ shorts to a high-level voltage, the device cannot indicate the fault by pulling down the NIRQ pin. The host must read F_NRSTIRQ for this information. This fault can be checked by forcing pin assertion via the FORCE_INT bit.
- Runtime volatile memory (VM) CRC: When no data is transferring, cyclic redundancy check (CRC) continues operating to detect accidental changes to the data. If a CRC fault is detected, the information is reported via F_RT_CRC.
- Thermal shutdown: The devices provides thermal shutdown protection. The fault is reported via the F_TSD bit. See the Sequence 9 section on page 33 for more details.
- Clock monitoring: The MPQ79700FS is implemented with a reference clock to cross-check with the internal clock to detect a clock error. See the Crystal Oscillator Driver and 32kHz Output section on page 33 for more details.

The V_{DD} start-up items that are checked are listed below:

- OTP ECC: While loading the configuration from the OTP, every 32 bytes of data is attached with a 7-bit ECC. A 1-bit error can be self-corrected by the ECC. A double error can only be detected. If either SEC or DED is executed, it is reported.
  - If SEC occurs, it is reported via the ECC_SEC bit while the start-up procedure continues normally.
  - If a DED condition occurs, the fault is reported via the F_ECC_DED bit and NIRQ is pulled down. Then the MPQ79700FS enters FAILSAFE state.
- VM BIST when loading data from the OTP.
- Analog BIST (ABIST): ABIST typically involves exercising diagnostic circuits in and out of fault scenarios by injecting currents or voltages into the diagnostic circuit. This ensures that the diagnostic circuit can switch to both fault and non-fault states. It is an analog circuit controlled by a digital circuit that verifies the correct functionality of analog safety mechanisms. During ABIST, the following parameters are tested: reference voltage monitoring, digital clock monitoring, CLK_32K clock monitoring, and if an output pin is stuck testing for faults
- Logic BIST (LBIST): The logic circuits are checked during LBIST. If an error is detected, NIRQ is pulled down and the error is reported via the F_BIST bit.

When the MPQ79700FS executes BIST, NIRQ de-asserts. Meanwhile, the NRST, CLK32K, and ENx pins are held low, the state transition is blocked, and the I^2C is inactive. Once BIST is complete, the I^2C is active again. If there is no failure, the device enters the SHDN1 state with the loaded OTP. If BIST fails (and/or a DED fault occurs), then NIRQ asserts and the device enters FAILSAFE state.

Backup State (BACKUP)

If V_{DD} drops, the MPQ79700FS can operate in BACKUP state if a battery is supplying power on VBAT (with a voltage exceeding $UVLO_{BB}$). Rather than be considered a normal state, this state should be considered a backup safety mechanism while facing emergency circumstances.

In the BACKUP state, only the battery supplies power to the device. Note that the device must have gone through a V_{DD} supplied state (and loaded configuration data) in order to enter this state. If there has not been a state where V_{DD} was supplied, then the MPQ79700FS remains in the OFF or battery installed state. The device only exits this state if there is a valid V_{DD} supply.

When the MPQ79700FS is in BACKUP state, the following pins are set to certain states:

- ENx = low (de-asserted)
- CLK32K = low (output disabled)
- NRST = low (asserted)
- ACT/SHDN and ACT/SLP inputs are ignored

The crystal oscillator and RTC remain active with Acc_{32k} accuracy, but the crystal oscillator fault monitor is not active. RTC_T[31:0], the interrupt, and the status registers are maintained and updated. Register configurations are maintained at their values from before the device entered the BACKUP state. The PROT1/2 registers are cleared. The I^2C interface and all remaining blocks are inactive.

After exiting the BACKUP state, the last configuration is active, and the device enters the SHDN1 state.

Failsafe State (FAILSAFE)

When in the FAILSAFE state, ENx, CLK32K, NRST, NIRQ are all held low, the ACT/SHDN and ACT/SLP inputs are ignored, and I^2C functionality remains active.

The MPQ79700FS enters the FAILSAFE state if any one of below faults occurred,

- F_EN or F_TSD
- F_ECC_DED or F_BIST

For more details, see Figure 21 on page 33 and Table 3 on page 38. The device cannot exit the FAILSAFE state by setting any register or pin state. To exit a FAILSAFE state, remove V_{DD} and ensure that the MPQ79700FS enters OFF state.

Output Sequencing

The MPQ79700FS can control the power up/down sequence for up to 12 channels. By outputting the enable signals of those channels, the MPQ79700FS can supply power to the system with a certain sequence and time tag. The sequence on/off events can be initiated by the hardware or software through ACT/SHDN, ACT/SLP, RTC wake, FORCE_SHDN, NPWR_BTN (if enabled), NEM_PD (if enabled), and NRST_IN (if enabled).

The device can output a power sequence per the loaded OTP configurations. In addition, the host can also initiate online changes for the following registers:

- SEQ_DSLOT: Sets the time slot between sequencing points for power down/sleep entry.
- PWR_EN1–12: Sets the power sequence for the 12 channels during power up/down. Set the channels that are not mapped with the allocated power up/down event to 0h.
- PWR_CLK32OE: Assigns the power up/down sequence for the 32kHz clock output's 1–15 time slots. Set the channels that are not mapped with the allocated power up/down event for CLK32 to 0h.
- SLP_EN1–12: Sets the power sequence for the 12 channels when entering or exiting SLEEP state. Set the channels that are not mapped with the allocated sleep entry/exit event to 0h.
- SLP_CLK32OE: Sets the sleep entry/exit sequence assignment for the 32.768kHz clock output's 1–15 time slots. Set the channels not mapped by CLK32 to 0h.

Figure 4 shows a power up event triggered by ACT/SHDN. Slot 1 refers to the earliest slot, while ENx (or CLK32K) toggles in the first time slot after the event is triggered. Figure 4 also indicates the definitions of the time delays in the Electrical Characteristics section on page 8.

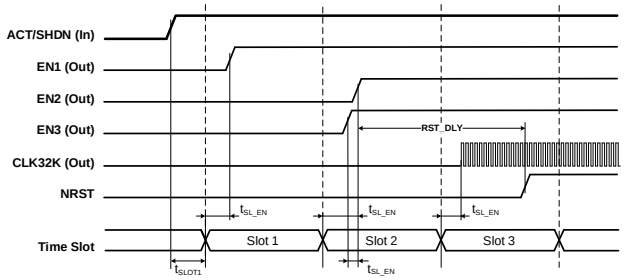


Figure 4: Output Sequencing Example

Transitioning Sequences

Figure 3 on page 24 shows nine sequences (power up, emergency power down, sleep entry, sleep exit, power down, power down from SLEEP, sleep exit due to NRST_IN, reset due to NRST_IN, FAILSAFE power down). These sequences are described below, with timing diagrams that show the main signals involved in each sequence.

Sequence 1 (Power Up)

When the system is activated, the MPQ79700FS conducts Sequence 1 and starts outputting power up enable signals on the voltage channels. This sequence is controlled by the ACT/SHDN pin when NPWR_BTN is not enabled (see Figure 5).

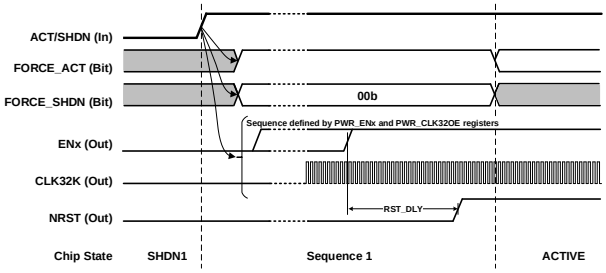


Figure 5: Sequence 1 (Controlled by the ACT/SHDN Pin)

When ACT/SHDN is high, the ENx/CLK32K output sequence starts. After the last ENx and CLK32K signals, NRST de-asserts after the delay time set by the RST_DLY[3:0] bits. The power up sequence is defined by the PWR_ENx and PWR_CLK32OE registers.

For applications that use a power button to turn the system on and off, a strap option is implemented in the MPQ79700FS. This option can be activated by enabling NPWR_BTN.

To enable the NPWR_BUTTON function, set EN_AF12 = 1b, AFIO12 =1b, PWR_EN12 = 00h and SLP_EN12 = 00h.

Note that under such circumstances, the maximum output signal drops down to 11 channels.

Figure 6 shows when NPWR_BTN short pushing triggers Sequence 1 from a SHDN1 state.

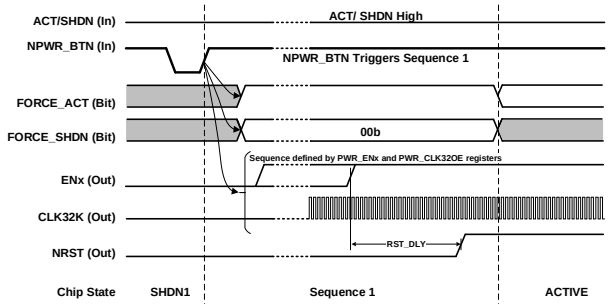


Figure 6: NPWR_BTN Short Pushing Triggers Sequence 1 from SHDN1

Figure 7 shows when V_{DD} triggers sequence 1 from OFF/BACKUP state when NPWR_BTN is enabled.

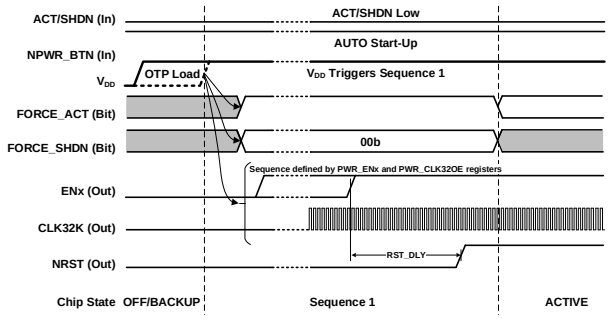


Figure 7: V_{DD} Triggers Sequence 1 from OFF/BACKUP with NPWR_BTN Enabled

Figure 8 shows when NPWR_BTN short pushing triggers Sequence 1 from SHDN2 state.

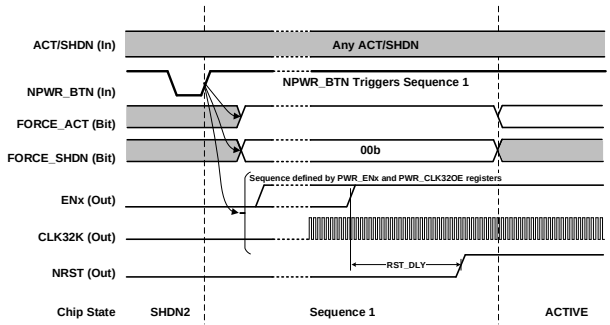


Figure 8: NPWR_BTN Short Pushing Triggers Sequence 1 from SHDN2

Figure 9 shows when SW triggers Sequence 1 from a SHDN2 state. This is during a SW power up/down when FORCE_SHDN is not set to 00b.

When NPWR_BTN is enabled, ACT/SHDN is used as the AUTO/BUTTON power up strap option. When ACT/SHDN is high, a short push on NPWR_BTN initiates the power up sequence. When ACT/SHDN is low, the power up sequence automatically starts once V_{DD} is valid. However, when operating in SHDN2 state, it is required a short push on NPWR_BTN to initiate the power up sequence, regardless of whether ACT/SHDN is high or low. It is recommended to short ACT/SHDN to VDD or GND, depending on the application.

Figure 6, Figure 7, and Figure 8 show the detailed behavior. When power up is triggered, the ENx and CLK32K output sequences start. After the last ENx and CLK32K signals, NRST de-asserts for the time set by the RST_DLY.

In addition to ACT/SHDN and NPWR_BTN control, the power up sequence can also be triggered via software. Write 01b, 10b, or 11b to register CTL_1. CTL_1, bits[1:0] (also known as FORCE_SHDN) force a power down sequence first. After a delay, the ACT/SHDN pin resumes its control to trigger the power up sequence. The delay time is based on the FORCE_SHDN bits.

Figure 9 shows the detailed behavior. When ACT/SHDN high, write 01b to FORCE_SHDN so that the ACT/SHDN pin control resumes immediately after the power down sequence completes, and when the next power up sequence is triggered.

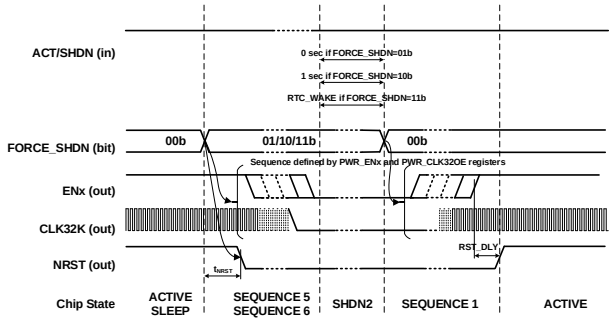


Figure 9: SW Triggers Sequence 1 from SHDN2 (FORCE_SHDN ≠ 00b)

Write 10b to FORCE_SHDN so that ACT/SHDN pin control resumes after a 1s delay.

Write 11b to FORCE_SHDN and enable RTC_PU. When an RTC alarm occurs at RTC_T = RTC_A, the ACT/SHDN pin control resumes.

Sequence 2 (Emergency Power Down)

If an emergency power down occurs (V_{DD} drops below its UVLO threshold while the device is in one of the on states from Figure 3 on page 24), Sequence 2 is initiated to protect the system.

If an emergency power down is detected, the MPQ79700FS asserts NRST and NIRQ before pulling ENx and CLK32K down. The device can use NRST assertion to reset the system, and NIRQ assertion can inform the host about the emergency. Figure 10 shows the details for Sequence 2. t_{NRST_EN} is typically 400ns, which is the time from when NRST asserts to when ENx and CLK32K are pulled down. NIRQ assertion occurs around the same time as NRST assertion.

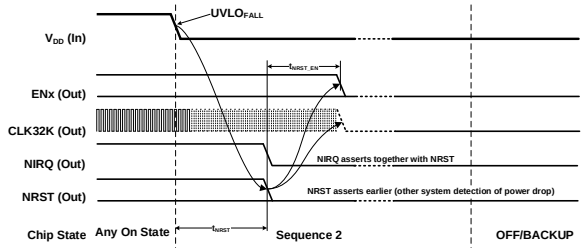


Figure 10: Sequence 2 (Emergency Power Down)

Note that if emergency power down is triggered while another sequence transition is underway, the other sequence transition is interrupted and Sequence 2 starts immediately.

Sequence 3 (Sleep Entry)

The MPQ79700FS can implement SLEEP state when several specific sleep channels are expected to be turned off according to the host. This sequence is triggered when both ACT/SLP is low and register FORCE_ACT = 0b. The sleep channels are pulled down in the order defined by SLP_ENx and SLP_CLK32OE. For non-sleep channels, set registers SLP_ENx and SLP_CLK32OE to 00h. The ENx and CLK32K outputs remains as it would in the previous status (see Figure 11).

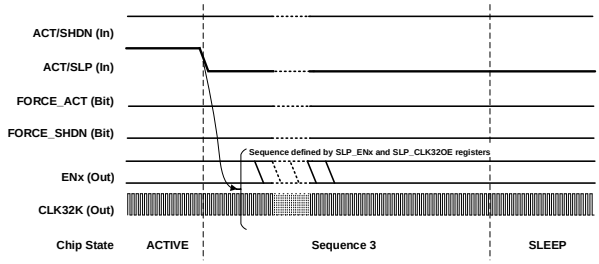


Figure 11: Sequence 3 (Sleep Entry)

If ACT/SLP is pulled low first, the sleep entry sequence also can be triggered by setting FORCE_ACT = 0b.

Sequence 4 (Sleep Exit)

Sequence 4 defines the device behavior when the system goes from SLEEP state to ACTIVE state. Either of the following conditions trigger Sequence 4:

- The ACT/SLP pin is set to high during SLEEP state
- The FORCE_ACT bit is set to 1b by an RTC alarm

This sequence starts by pulling up the ENx/CLK32K outputs to start up the sleep channels, based on the configurations in the SLP_ENx and SLP_CLK32OE registers.

If an RTC alarm triggers a wake-up, there are two methods to trigger Sequence 4:

1. The MPQ79700FS asserts an interrupt when there is an RTC alarm; then the sequence starts after the hosts sees the interrupt and pulls up ACT/SLP.
2. Set RTC_WAKE = 1b to enable the device to automatically exit SLEEP mode after an RTC alarm triggers a wake-up. An RTC alarm also forces the FORCE_ACT bit to 1b to avoid immediate sleep re-entry in case ACT/SLP is not driven high before Sequence 4 is complete. Note that the RTC_WAKE bit must be enabled before RTC_T = RTC_A; otherwise, an automatic exit is not triggered.

Figure 12 shows when Sequence 4 is triggered by ACT/SLP.

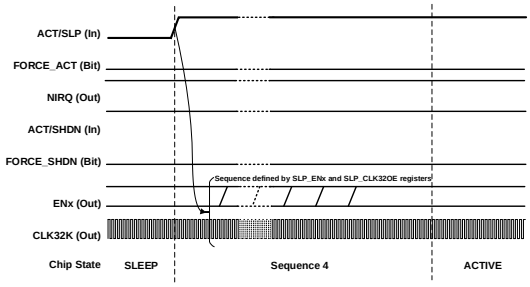


Figure 12: Sequence 4 (Sleep Exit Triggered by ACT/SLP)

Figure 13 on page 31 shows the sequence when Sequence 4 is triggered due to an RTC alarm and ACT/SLP sequencing.

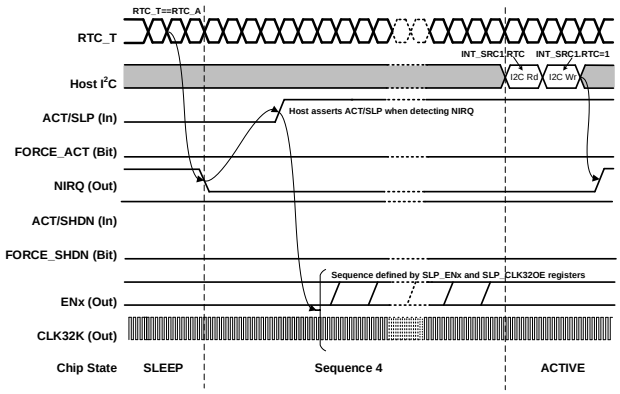


Figure 13: Sequence 4 (Sleep Exit Triggered by RTC, ACT/SLP Sequencing)

Figure 14 shows when Sequence 4 is triggered due to an RTC alarm and autonomous sequencing.

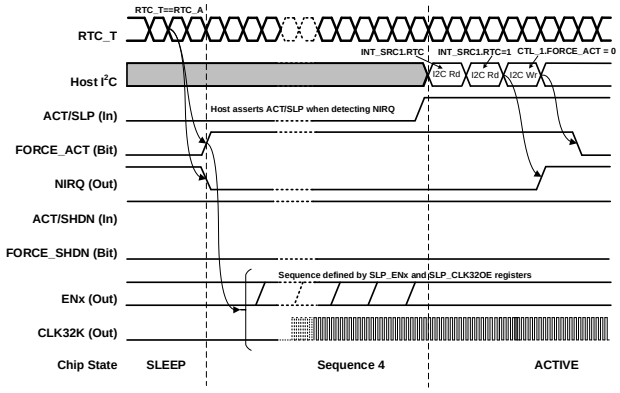


Figure 14: Sequence 4 (Sleep Exit Triggered by RTC, Autonomous Sequencing)

Sequence 5 and Sequence 6 (Power Down from ACTIVE and SLEEP States)

Sequence 5 is a power down sequence from ACTIVE state, while Sequence 6 is a power down sequence from SLEEP state. In both scenarios, NRST asserts in the first sequencing slot with a delay (t_{NRST}) after the power down sequence is triggered. After NRST assertion passes (t_{NRST_EN}), ENx and CLK32K de-assert based on the configurations in the PWR_ENx and PWR_CLK32OE registers. If NPWR_BTN is enabled, the long-press time (t_{LONG_PRESS}) is determined by the LP_TTSHLD register.

Figure 15 shows when the FORCE_SHDN bit triggers a power down.

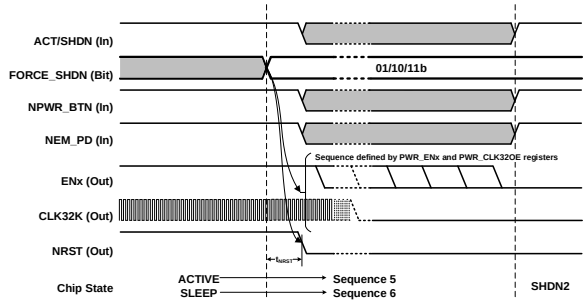


Figure 15: Sequence 5 and 6 (FORCE_SHDN Bit Triggers Power Down)

Figure 16 shows when ACT/SHDN triggers a power down.

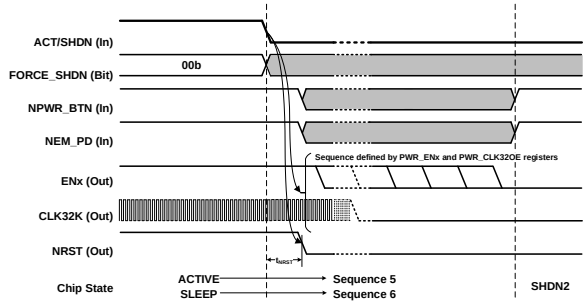


Figure 16: Sequence 5 and 6 (ACT/SHDN Triggers Power Down)

Figure 17 shows when NPWR_BTN triggers a power down.

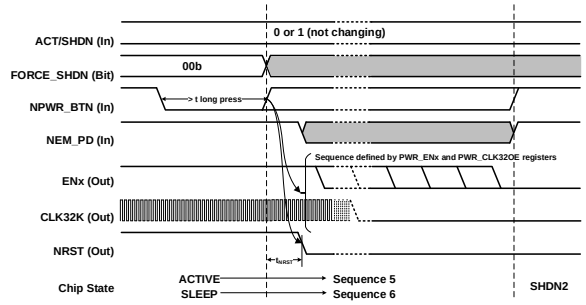


Figure 17: Sequence 5 and 6 (NPWR_BTN Triggers Power Down

Figure 18 shows when NEM_PD triggers a power down.

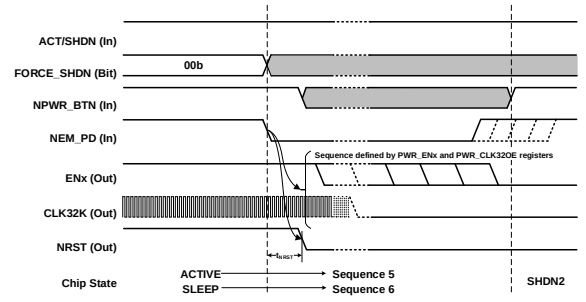


Figure 18: Sequence 5 and 6 (NEM_PD Triggers a Power Down

Power down from SLEEP state differs from power down from ACTIVE state, since certain ENx and CLK32K signals may have already de-asserted for SLEEP mode. When the device shuts down after a sleep sequence, the remaining ENx and CLK32K signals de-assert per the configurations in the PWR_ENx and PWR_CLK32OE registers.

Figure 18 on page 31 shows NEM_PD, which is an alternate function of EN10. When NEM_PD is pulled low, the power down sequence is triggered. To enable the NEM_PD function, set EN_AF10 = 1b, AFIO10 = 1b, PWR_EN10 = 00h, and SLP_EN10 = 00h.

The power down sequence also applies to shutdowns triggered by the WDT. See the Watchdog Timer (WDT) section on page 35 for more details.

Sequence 7 (Sleep Exit Due to NRST_IN)

NRST_IN is an alternate function of EN11. To enable the NRST_IN function, set registers EN_AF11 = 1b, AFIO11 = 1b, PWR_EN11 = 00h, and SLP_EN11 = 00h.

For applications where NRST_IN is enabled, NRST_IN assertion in SLEEP state can also trigger the MPQ79700FS to exit SLEEP state. If an emergency occurs, the MPQ79700FS can receive relevant information through NRST_IN.

After NRST_IN assertion (plus a debounce set via the DEB_IN register), the device asserts NRST immediately to ensure that there is a proper power state synchronization with the rest of the system. Meanwhile, a sequence to exit SLEEP mode is executed and the sleep channels are re-activated. If the emergency situation is averted, the host (or other devices, depending on the application) can de-assert NRST_IN to release NRST. The NRST signal de-asserts once the RST_DLY delay time has passed and the last ENx and NRST_IN signals have de-asserted.

NRST de-assertion follows the normal sequence-controlled behavior, but is gated by both RST_DLY and NRST_IN. This means that if NRST_IN is released after the ENx and CLK32K sequences are completed and RST_DLY has passed since the last sequenced ENx/CLK32K, then NRST de-asserts immediately once NRST_IN is released. If NRST_IN is released before RST_DLY has passed, then NRST remains asserted until RST_DLY has passed.

In Sequence 7, NRST_IN forces the FORCE_ACT bit to 1b to avoid immediate sleep re-entry, in case ACT/SLP is not driven high before this sequence completes.

Figure 19 shows the details for Sequence 7.

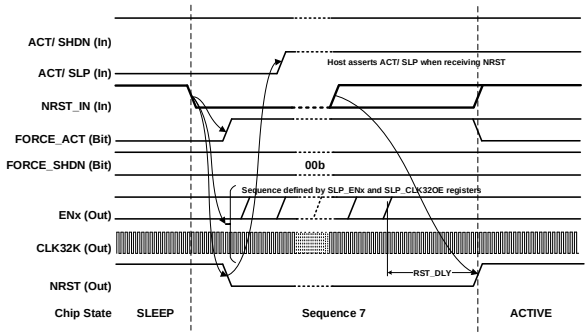


Figure 19: Sequence 7 (Sleep Exit Due to NRST_IN)

Sequence 7 can be applied in the event of a WDT-initiated reset. If WDTEN = 01b or 10b, NRST may assert if WDT violation occurs, then a sleep exit sequence is triggered. Note that this sequence is not applied when WDTEN = 11b, since NRST does not assert in this scenario.

Sequence 8 (Reset Due to NRST_IN)

For applications where NRST_IN is enabled, NRST_IN assertion in ACTIVE state can trigger the NRST output to be reset. NRST asserts at NRST_IN assertion (plus a debounce set via the DEB_IN register), then de-asserts after NRST_IN de-assertion (plus debounce) and the RST_DLY delay time has passed.

Figure 20 shows the details for Sequence 8. Unlike Sequence 7, if FORCE_ACT = 0b before Sequence 8, this sequence does not set FORCE_ACT to 1b.

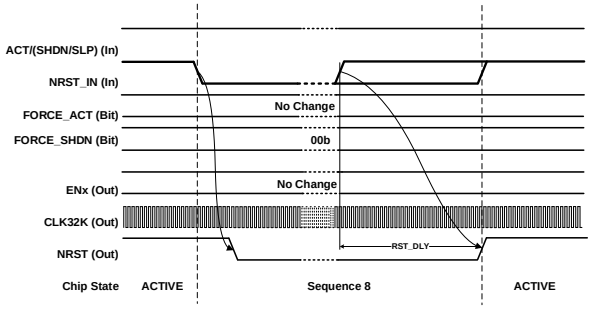


Figure 20: Sequence 8 (Reset Due to NRST_IN)

Sequence 8 can be applied in the event of a WDT-initiated reset. If WDTEN = 01b or 10b, NRST may assert if WDT violation occurs. Note that this sequence is not applied when WDTEN = 11b, since NRST does not assert in this scenario.

Sequence 9 (Failsafe Power Down)

F_TSD and F_EN faults cause the MPQ79700FS to enter FAILSAFE state (see the Faults Handling section on page 37 for more details). The transition to this state is similar to Sequence 2, though the trigger is a fault instead of V_{DD}. NRST and NIRQ assert, then ENx and CLK32K are pulled down. NRST assertion occurs a specific time (t_{NRST_EN}) before ENx and CLK32K are pulled down, while NIRQ asserts about 1µs before NRST (see Figure 21).

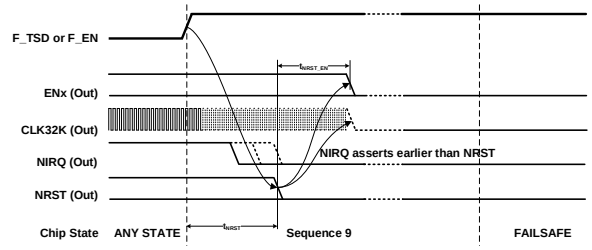


Figure 21: Sequence 9 (Failsafe Power Down)

Note that if F_TSD or F_EN are triggered while another sequence transition is underway, the executing sequence transition is interrupted and Sequence 9 starts immediately.

Crystal Oscillator Driver and 32kHz Output

The MPQ79700FS integrates a 32.768kHz crystal oscillator driver that can generate the reference clock for other devices in the system. Figure 22 shows the crystal oscillator block diagram. The crystal driver and RTC are powered by the VDD input (or the VBAT input if an emergency condition occurs).

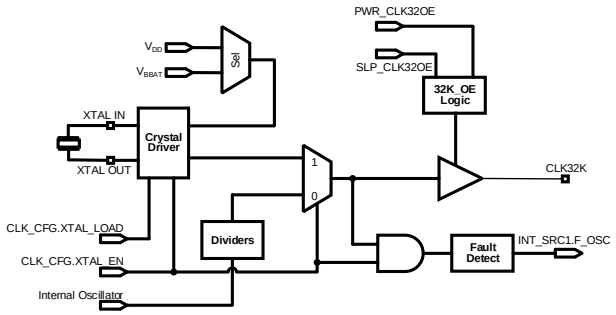


Figure 22: Crystal Oscillator Block Diagram

When the device is powered only by V_{BAT}, the CLK32K output buffer is disabled. The oscillator and RTC remain functional, and the status and configuration registers are maintained.

The crystal load capacitor can either be external capacitors or the MPQ79700FS's internal capacitors. To use the internal load capacitors, set the XTAL_LOAD bit to 1b; otherwise, set it 0b and use the external capacitors for the application. To activate the crystal driver circuit, set the XTAL_EN bits to 1b. These bits are configured via the OTP and are read-only once out of the MPS factory. The default internal capacitors are well-suited for crystals that require a load capacitance of 12.5pF. Contact an MPS FAE to set these registers and internal capacitors value.

The MPQ79700FS implements fault detect logic circuits for the oscillator frequency. If f_{32k} exceeds the f_{FAULT} limit, the device pulls NIRQ down to warn the host within a set time (t_{XTALF}). This fault is also reported via the F_OSC bit.

The output buffer is controlled by the configuration registers (PWR_CLK32OE and SLP_CLK32OE). PWR_CLK32OE determines when the clock output is disabled during the power up sequence and when it is disabled during the power down sequence. If the clock output should be disabled in SLEEP mode, the SLP_CLK32OE register determines when the clock should be enabled during sleep entry/exit.

The internal clock (rather than the crystal oscillator) drives the WDT and on/off sequencers, which ensures that the power up sequence is not delayed while the crystal oscillator stabilizes.

During V_{DD} start-up, if the following power up sequence completes before the crystal oscillator is stable (within the accuracy specified by Acc_{EB32k} in the Electrical Characteristics section on page 8) then the rising edge of NRST is not delayed while waiting for the crystal oscillator to stabilize.

If XTAL_EN = 0b (crystal oscillator disabled), the RTC and CLK32K outputs are driven by the internal oscillator. The WDT and on/off sequencers are driven by the internal oscillator.

See the Electrical Characteristics section on page 8 for relevant parameters values.

Real-Time Clock (RTC)

The MPQ79700FS includes a real-time clock (RTC) with a 32-bit time and alarm registers. The time counter is incremented once per second, counting up to about 136 years. Figure 23 shows the RTC block diagram.

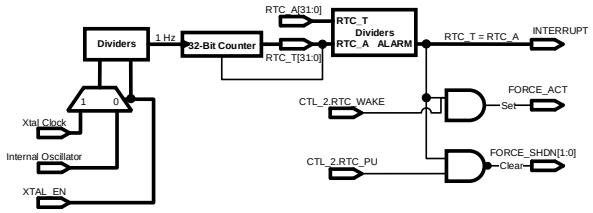


Figure 23: RTC Block Diagram

The RTC_T register is a 32-bit, read/write (R/W) register that is initialized with a POR value of 0x00000000. It is incremented once per second if all of the following conditions are met:

- The crystal oscillator or internal oscillator (depending on the XTAL_EN bit) is operational
- V_{DD} exceeds $UVLO_{VTH\_R}$
- RTC_T < 0xFFFFFFFF

If RTC_T = 0xFFFFFFFF, then RTC_T stops counting and maintains this value.

The RTC_A register is a 32-bit, R/W register that is initialized with a POR value of 0xFFFFFFFF. Set this register to the target value. When RTC_T = RTC_A, the alarm is executed. Note that the alarm is not triggered if the set RTC_A < RTC_T. If the MPQ79700FS enters a BACKUP state when RTC_T < RTC_A and RTC_T rises to be equal to RTC_A while in the BACKUP state, an RTC alarm is not triggered when the device exits the BACKUP state.

The RTC_T register is independent of RTC_A, and the RTC_T register's active counting is not affected by an RTC alarm or the RTC_A setting.

The device can take the following actions after an alarm is executed:

- Alarm disabled
- Assert NIRQ and the flag alarm status for a wake-up based on the external processor interrupt
- Autonomously wake up from SLEEP state
- Autonomously wake up from a shutdown state

Figure 23 shows the RTC configuration register bits (FORCE_ACT, FORCE_SHDN, RTC_WAKE, and RTC_PU). These actions are described in greater detail below:

1. Alarm disabled: If RTC_A = 0xFFFFFFFF, this can be considered a disabled alarm, unless RTC_T is manually set close to 0xFFFFFFFF (e.g. 0xFFFFFF00). This is because RTC_T needs to count to about 136 years from 0x00000000 to 0xFFFFFFFF, which is impossible in a real application.
2. Alarm to assert NIRQ for an interrupt-based wake-up: If the MPQ79700FS interrupts the host in applications where RTC_WAKE and RTC_PU are both cleared, the host asserts ACT/SLP or ACT/SHDN. If RTC_T = RTC_A, then an interrupt asserts and the RTC flag is set. The host processor reads INT_SRC1 to determine whether the RTC alarm is the source for the interrupt. In this scenario, FORCE_ACT is not set (see Figure 13 on page 31).
3. Autonomously wake up from SLEEP state: If RTC_T = RTC_A in applications where RTC_WAKE is set, an interrupt asserts and the RTC flag is set. Then the MPQ79700FS transitions from SLEEP to ACTIVE. FORCE_ACT is also set when the alarm triggers. As a result of the interrupt, the processor wakes up, determines cause of the interrupt, de-asserts ACT/SLP, and clears FORCE_ACT (see Figure 14 on page 31).
4. Autonomously wake from a shutdown state: If the processor sets FORCE_SHDN (CTL_1, bits[1:0]) to 11b in applications where RTC_PU is set, the MPQ79700FS is forced into SHDN2 mode until RTC_T = RTC_A. Then the MPQ79700FS transitions from SHDN2 to ACTIVE. In addition, the device can exit SHDN2 if ACT/SHDN is de-asserted and re-asserted by the system, or FORCE_SHDN is set to 01b or 10b.

Note the register access for the RTC_T and RTC_A registers. The RTC uses two 32-bit registers to keep time (RTC_T) and set alarms (RTC_A).

Access to these registers is limited by the I²C interface, and the 32-bit registers are split into four 8-bit I²C registers. See the Register Map section on page 44 for more details. RTC_T is split into registers 0x70~0x73, while RTC_A is split into registers 0x74~0x77. To complete a write/read operation for RTC_T (or RTC_A), write to all four related registers one by one and in order. The read/write operations cannot be atomic, as they always involve multiple registers accesses to complete the 32-bit value.

Since RTC_T is a 32-bit counting register, non-atomic operation can impede data coherency during register access. Data coherency refers to the data across the four 8-bit registers, and they belong to the same coherent state or instant.

While this is not an issue for the RTC itself as it counts the time, it requires careful handling when moving data as part of a host, when the host reads or writes the set of four 8-bit registers. The access operation (read or write) may become asynchronous with the time counting as the 32-bit register increments. This means that when the four 8-bit registers are accessed by the host, they may not be accurate, and the incorrect time may be written or read.

This can be illustrated with an example, showing a read operation while the RTC_T[31:0] increments from 767s to 768s:

1. RTC_T = 00000000 00000000 00000010 11111111 = **767**
2. Host starts the I²C read transaction:
   a. Start > MPQ79700FS address > Write > RTC_T[31:24] address
   b. Restart > MPQ79700FS address > Read > MPQ79700FS transmits RTC_T[31:24] data (00000000)
   c. MPQ79700FS transmits RTC_T[23:16] data (00000000)
   d. MPQ79700FS transmits RTC_T[15:8] data (00000010)
      Assume that now the RTC_T[31:0] increments to 00000000 00000000 00000011 00000000 = **768**
   e. MPQ79700FS transmits RTC_T[7:0] data (00000000)
   f. Stop
3. Recomposed I²C registers into 32-bit RTC data = 00000000 00000000 00000010 00000000
4. While the host was supposed to read 767, the poor data coherency means this value is read as 512.

To avoid the above scenario, the MPQ79700FS guarantees data coherency during a write/read by taking a snapshot (into the buffer registers) of the 32-bit RTC_T register when the RTC_T[31:24] address is written at the beginning of the I²C read transaction. This snapshot data is transmitted instead of the live data from the counting register.

Watchdog Timer (WDT)

The MPQ79700FS implements a watchdog timer (WDT) as a system failure detection mechanism to ensure that the host can continue updating data at certain durations. The WDT can interrupt, reset, or cycle the system power based on a configurable number of failures. The failure is based on a key register updating within the configurable update window. Figure 24 shows the watchdog timer clock block diagram.

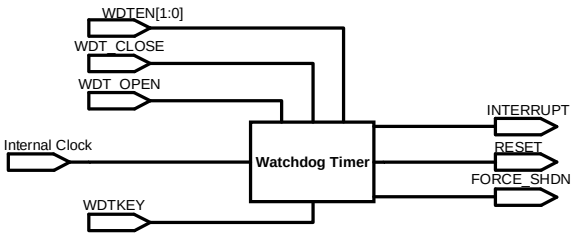


Figure 24: Watchdog Timer Clock Block Diagram

The watchdog timer is enabled by setting the WDTEN bits. These bits also define the tolerable numbers of watchdog violations (configurable up to three successive violations) and the device's action(s) if a violation is detected.

Table 2 shows the WDT configurations.

Table 2: Watchdog Timer Configuration

WDTEN[1:0]	Description
00b	Watchdog disabled.
01b	If there are successive violations: 1. Assert interrupt request (NIRQ). 2. Assert reset (NRST) according to Sequence 7 and Sequence 8. 3. Shut down according to PDMD (WDT_CFG, bits[1:0]).
10b	If there are successive violations: 1. Assert reset (NRST) according to Sequence 7 and Sequence 8. 2. Shut down according to PDMD (WDT_CFG, bits[1:0]).
11b	On the first violation: Shut down according to PDMD (WDT_CFG, bits[1:0]).

When the WDT is enabled, the beginning of the first closed window may be delayed by up to eight WDT periods, as configured by WDTDLY[2:0]. After the delay, the WDT counts the close window and open window; these durations can be set via the WDT_CLOSE and WDT_OPEN registers, with a range between 1ms and 864ms each. When NRST asserts, the WDT stops working. In this scenario, the host is not expected to service WDTKEY. The WDT resumes operation after NRST is de-asserted and WDTDLY is applied.

The WDT input signal is a new value that is written to the WDTKEY register via the I^2C. A valid WDT input signal writes any data that is different from current WDTKEY data (e.g. write 00h-01h-00h-01h cyclically, or write 00h-01h-02h-10h-22h, etc.).

It is expected to update WDTKEY during open windows. Otherwise, this is considered a violation. Examples include updating data during a close window (these cases are recorded in WDUV, which means updating has occurred too early), or not receiving any data until the open duration expires (these are recorded in WDEXP, which means updating has occurred too late).

Meanwhile, if a WDT violation occurs, the WDT flag is set.

A WDT period is the combination of a close window and an open window where the maximum WDT period can be up to 1.728s (when both the close and open windows are set to 864ms). Once WDTKEY receives valid data during open window, open window counting is reset and the next WDT period starts instead of counting the complete open duration.

When the WDT is enabled, it may be automatically disabled in SLEEP state (by clearing the WDT_CFG.SLP_EN bit) since the host may be also in SLEEP state and unable to keep updating the WDTKEY signal. This mechanism could be masked by setting the WDT_CFG.SLP_EN bit to 1b depending on the application. In SHDN1 and SHDN2 states, the WDT is automatically disabled (the stored setting WDT_CFG.WDTEN[1:0] is applied after exiting those states).

Figure 25 shows WDT operation without a violation.

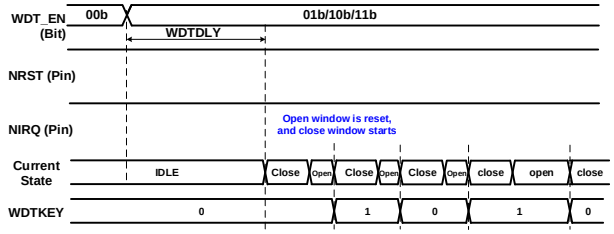


Figure 25: WDT Operation without a Violation

Figure 26 shows WDT operation when there are successive violations and WDTEN = 01b.

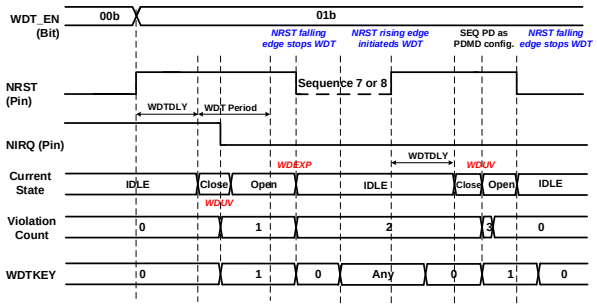


Figure 26: WDT Operation with Successive Violations (WDTEN = 01b)

Figure 27 on page 37 shows WDT operation when there are successive violations and WDTEN = 10b.

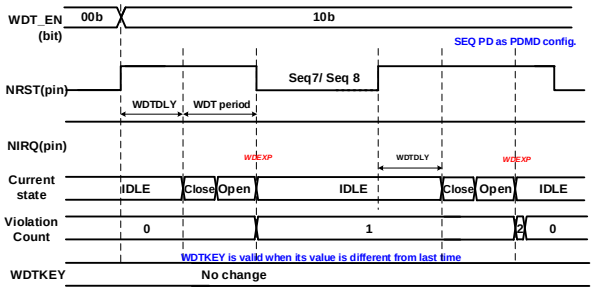


Figure 27: WDT Operation with Successive Violations (WDTEN = 10b)

Figure 28 shows WDT operation when there are successive violations and WDTEN = 11b.

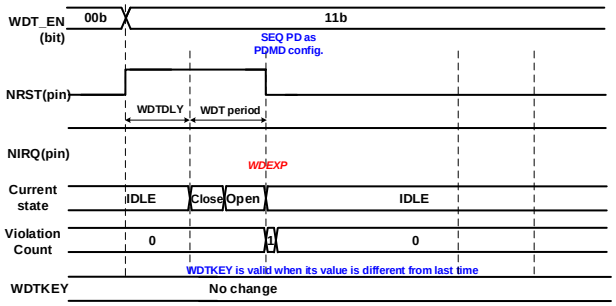


Figure 28: WDT Operation with Successive Violations (WDTEN = 11b)

Since the MPQ79700FS tolerates successive WDT violations, the number of violations are counted internally using either WDUV or WDEXP. They are allowed to count up to 3 violations (set via WDTEN). The WDT takes different actions according to the WDTEN settings: it may assert an interrupt, reset, or cycle the system's power.

To maintain proper WDT functionalities, the violation count should not trigger a reset when NRST asserts. If NRST asserts internally or externally, the WDT violation count is paused. It continues counting with the same number when NRST de-asserts and another close window starts. This means that the WDT violation counting function operates regardless of whether NRST asserts internally or externally.

The violation count is reset to 0 when the WDT is disabled, including if WDT is automatically disabled in SLEEP state (if SLP_EN = 0b) or SHDNx state. If the WDT reaches its maximum numbers of violations, the system shuts down according to WDTEN (see Table 2 on page 36).

Then the MPQ79700 accesses the shutdown state, WDT is disabled, and the violation count is reset. If the host clears the violation count when other devices cause a system reset, it can disable the WDT through the I²C when NRST is asserted, regardless of whether the assertion was an internal or external.

Faults Handling

The MPQ79700FS detects different faults, which are reported through the NIRQ interrupt pin (active low) and the INT_SRC1 and INT_SRC2 registers. Table 3 on page 38 describes each detected fault, and the actions taken by the MPQ79700FS in response.

In all cases, the host can clear the interrupt flag. This de-asserts NIRQ unless other flags are set. For the F_INTERNAL bits, it is sufficient to clear the relevant flag in the INT_SRC2 register.

Note that the interrupt flags can only be cleared by the host with a write-1-to-clear operation. Flags are not cleared automatically if the fault condition is removed.

One-Time Programmable (OTP) Memory

The MPQ79700FS provides an OTP memory to set custom default parameters.

MPS provides a GUI and I²C tool to configure the MPQ79700FS during the custom development process. To configure the MPQ79700FS for an application, contact an MPS FAE. The OTP can be written twice, meaning that there are two OTP pages.

Note that registers 0x20~0x24 (EN_ALT_F, AF_IN_OUT, EN_CFG1, EN_CFG2 and CLK_CFG) can only be written to and configured by MPS. Contact an MPS FAE if these registers must be updated.

Table 3: Faults Handling

Fault	Description	Actions
F_NRSTIRQ (INT_SRC1, bit[0])	The NRST and/or NIRQ pins cannot be pulled low (NRST/NIRQ is a short to high-level voltage; the external short-to-GND level cannot be determined). The NIRQ line can be tested by the host by forcing NIRQ low through the FORCE_INT bit.	1. Set the interrupt flag (F_NRSTIRQ). 2. If a fault occurs on NRST, pull NIRQ low to alert the host. 3. If a fault occurs on NIRQ, no further action is required. The host polls INT_SRC1 periodically. 4. If the host clears the interrupt but the fault is still detected, the MPQ79700FS sets it again.
F_OSC (INT_SRC1, bit[1])	Indicates whether crystal oscillator frequency is outside the f_{FAULT} range. This fault detection is only active if XTAL_EN = 1.	1. Set the interrupt flag (F_OSC). 2. Pull NIRQ low to alert the host. Note that the CLK32K output's enabled state is not affected.
F_EN (INT_SRC1, bit[2])	Indicates whether there is an enable output pin fault, including an unintended switch on/off, being stuck at on/off, and/or shorting to VDD or GND.	1. Set the interrupt flag (F_EN). 2. Pull NIRQ low to alert the host. 3. The device enters FAILSAFE state (Sequence 9). The I^2C stays active.
RTC (INT_SRC1, bit[3])	Indicates whether an RTC alarm was triggered. This alarm function is active only if RTC is configured for the function (see the Real-Time Clock (RTC) section on page 34).	1. Set the interrupt flag (RTC). 2. Pull NIRQ low to alert the host.
F_PEC (INT_SRC1, bit[4])	Indicates whether there was a packet error checking (PEC) fault during an I^2C transaction. The PEC fault detection is only active if EN_PEC = 1b.	1. The I^2C write transaction with an incorrect PEC does not complete and the write fails. 2. Set the interrupt flag (F_PEC). 3. Pull NIRQ low to alert the host.
WDT (INT_SRC1, bit[5])	Indicates whether a WDT violation has occurred since the last read. WDT fault detection is only active if WDTEN[1:0] is enabled.	1. Set the interrupt flag (WDT). 2. Pull NIRQ low to alert the host (if WDTEN[1:0] = 01b).
EM_PD (INT_SRC1, bit[6])	Indicates whether an emergency power down has occurred, such as if V_{DD} drops below its UVLO threshold while the device is in an on state (Sequence 2).	1. Set the interrupt flag (EM_PD). 2. Pull NIRQ low to alert the host. 3. Enter BACKUP or OFF state, depending on the VBAT status. 4. If going to BACKUP state, the interrupt flag is maintained and can be read once V_{DD} is restored.
F_INTERNAL (INT_SRC1, bit[7])	Indicates whether an internal fault has occurred.	1. Set the interrupt flag (F_INTERNAL). 2. Pull NIRQ low to alert the host. 3. Further action depends on the INT_SRC2 setting.
F_BPSP (INT_SRC2, bit[0])	Sends an alert for short pulse on NPWR_BTN. It is valid only if NPWR_BTN is enabled through the EN_AF12 and AFIO12 bits.	1. Set the interrupt flags (F_BPSP and F_INTERNAL). 2. Pull NIRQ low to alert the host.

F_ECC_DED (INT_SRC2, bit[1])	Indicates whether an ECC double-error was detected on the OTP configuration load.	1. Set the interrupt flags (F_ECC_DED and F_INTERNAL). 2. Pull NIRQ low to alert the host. 3. Enter FAILSAFE state. The I²C remains active.
F_TSD (INT_SRC2, bit[2])	Indicates whether a thermal shutdown fault was detected.	1. Set the interrupt flags (F_TSD and F_INTERNAL). 2. Pull NIRQ low to alert the host. 3. Enter FAILSAFE state (Sequence 9). The I²C remains active.
F_BIST (INT_SRC2, bit[4])	Indicates whether a BIST fault was detected.	1. Set the interrupt flags (F_BIST and F_INTERNAL). 2. Pull NIRQ low to alert the host. 3. Enter FAILSAFE state. The I²C remains active.
F_RT_CRC (INT_SRC2, bit[5])	Indicates whether a runtime register CRC fault was detected.	1. Set the interrupt flags (F_RT_CRC and F_INTERNAL). 2. Pull NIRQ low to alert the host.
F_BG (INT_OTHER, bit[0])	Indicates whether a fault has occurred because the bandgap reference voltage is outside of its ±10% tolerance window.	1. Set the interrupt flags (F_BG, F_OTHER, and F_INTERNAL). 2. Pull NIRQ low to alert the host.
F_2P5M (INT_OTHER, bit[1])	Indicates whether a fault has occurred because the 2.5MHz digital clock frequency is outside of its ±10% tolerance window.	1. Set the interrupt flags (F_2P5M, F_OTHER, and F_INTERNAL). 2. Pull NIRQ low to alert the host.

I²C INTERFACE

I²CSerial Interface Description

The I²C bus is a two-wire, bidirectional serial interface, consisting of a serial data line (SDA) and a serial clock line (SCL). The lines are externally pulled to a bus voltage when they are idle. When connected to the line, a master device generates the SCL signal and device address, and arranges the communication sequence. The MPQ79700FS works as a slave-only device, which supports up to 1Mb/s of bidirectional data transfer in fast-mode plus, thereby adding flexibility to the sequencer. The ENx sequence, RTC, WDT, and other sequencer parameters can be instantaneously controlled via the I²C interface.

Data Validity

One clock pulse is generated for each data bit transferred. The data on SDA must be stable during the clock's high period. The SDA line's high or low state can only change when the clock signal on the SCL line is low (see Figure 29).

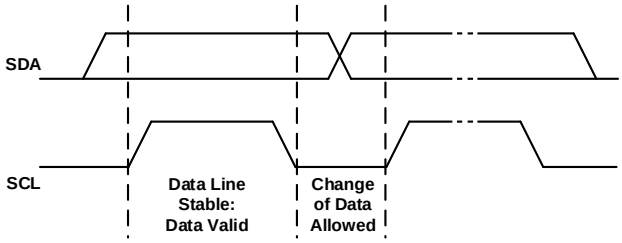


Figure 29: Bit Transfer on the I²C Bus

Start and Stop Commands

Start (S) and stop (P) commands are signaled by the master device, which signifies the beginning and the end of the I²C transfer. A start command is defined as the SDA signal transitioning from high to low while SCL is high. A stop command is defined as the SDA signal transitioning from low to high while SCL is high (see Figure 30).

Start and stop commands are always generated by the master. The bus is considered busy after a start command. The bus is considered free again after a delay following a stop command. The bus stays busy if a repeated start (Sr) command is generated instead of a stop command. Start and repeated start commands are functionally identical.

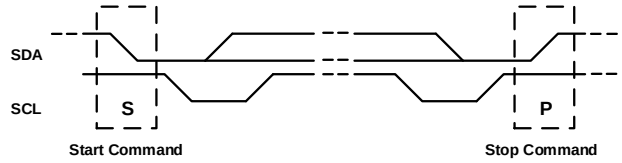


Figure 30: Start and Stop Conditions

Transfer Data

Every byte put on SDA must be 8 bits long. Each byte must be followed by an acknowledge (ACK) bit. The acknowledge-related clock pulse is generated by the master. The transmitter releases the SDA line (high) during the acknowledge clock pulse. The receiver must pull down the SDA line during the acknowledge clock pulse, so that it remains stable (low) during the high period of the clock pulse.

Figure 31 shows the data transfer format. After the start command, a slave address is sent. This address is 7 bits long, followed by an 8th data direction bit. The data direction bit determines whether the transmission is a read (R) or write (W). A 0 indicates a write transmission, and a 1 indicates a read (a request for data). A data transfer is always terminated by a stop command generated by the master. However, if the master still wishes to communicate on the bus, it can generate a repeated start command and address another slave without first generating a stop command.

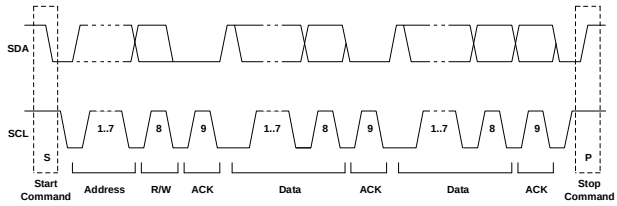


Figure 31: A Complete Data Transfer

Write Sequence

The MPQ79700FS I²C supports single and sequential byte writing. If enabled by EN_PEC, single-byte writes have an appended packet error checking (PEC) byte. PEC is not supported on a sequential write. Figure 32 and Figure 33 on page 41 show the write sequence. The typical MPQ79700FS single-byte write sequence requires a start command from the master, a valid slave address, a register index byte, and a corresponding data byte for a single data update.

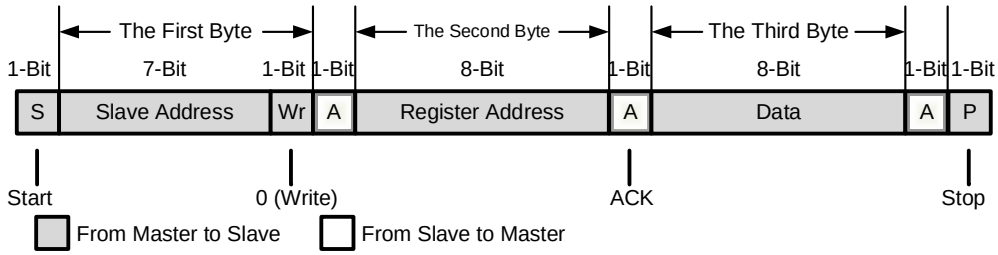


Figure 32: Write Sequence (Single Byte)

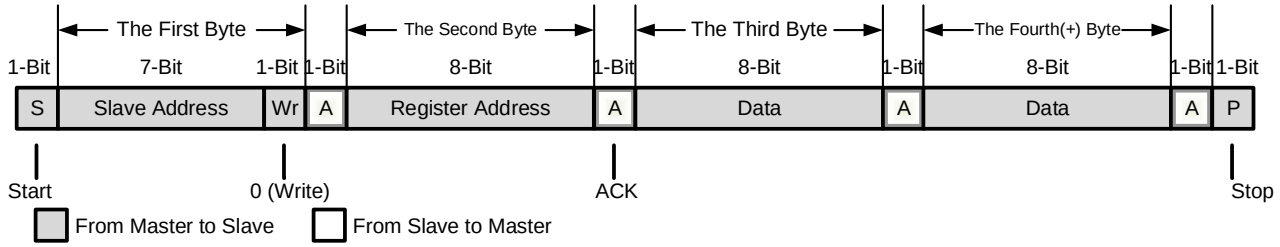


Figure 33: Write Sequence (Sequential Bytes)

After receiving each byte, the MPQ79700FS acknowledges by pulling SDA low during the high period of a single clock pulse. A valid I²C address selects the MPQ79700FS. The MPQ79700FS then performs an update on the falling edge of the LSB byte.

Read Sequence

The MPQ79700FS I²C supports both single and sequential byte reading. If enabled by EN_PEC, single-byte reads can be appended with a PEC byte. PEC is not supported on a sequential read.

Figure 34 and Figure 35 show the write sequence. The typical MPQ79700FS single-byte read sequence is 4 bytes long. It begins with a start command from the master, followed by a valid slave address and a register index byte. Unlike a write sequence, a start command from the master comes again. The bus direction then turns around with the rebroadcast of the slave address, with bit 1 indicating a read cycle. The following 4th byte contains the data being returned by the MPQ79700FS. That byte value in the data byte reflects the value of the register index being queried before.

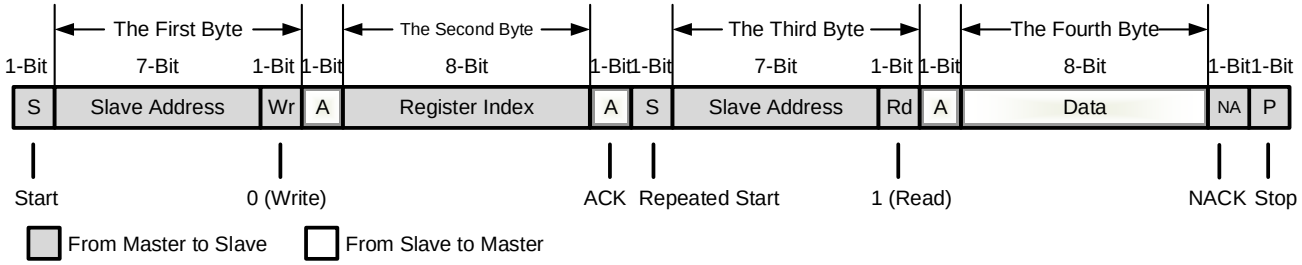


Figure 34: Read Sequence (Single Byte)

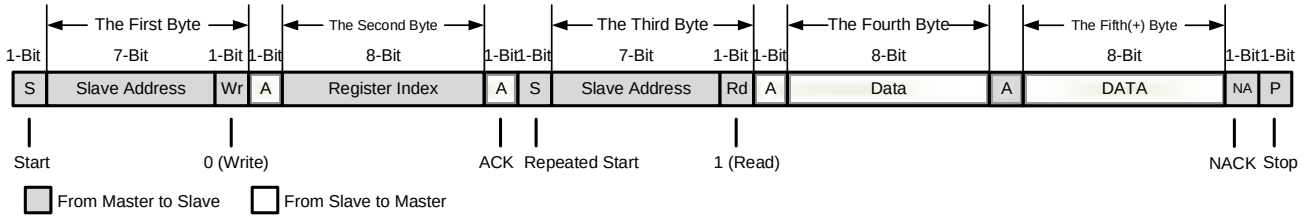


Figure 35: Read Sequence (Sequential Byte)

Chip Address

The MPQ79700FS supports 127 different addresses (00h~7Fh), which can be preset in register 0xF9 via the I²C bus.

When the master sends the address as an 8-bit value, the 7-bit address should be followed by an 8th data direction bit.

Packet Error Checking (PEC)

The MPQ79700FS supports PEC following the SMBus implementation. Refer to System Management Bus Specification version 3.0, sections 6.4 and 6.5 for more details (specifically, refer to section 6.4.1.3 for details on slave implementation). The specification uses a CRC-8, represented by the polynomial $C(x) = x^8 + x^2 + x + 1$.

As described in the SMBus specification, the PEC calculation includes all bytes in the transmission, such as the address, command, and data. The PEC calculation does not include ACK or not acknowledge (NACK) bits, or start, stop, or repeated start commands. This means that the PEC is computed across the entire message from the first start command.

According to SMBus specifications (section 6.4.1), the SMBus must accommodate any mixture of devices that support PEC and devices that do not. For this reason, a device that acts as a slave and supports PEC must always be prepared to perform the slave transfer with or without PEC, verify the correctness of PEC if present, and only process the message if PEC is correct.

The I²C master can implement an optional exception for transfers without PEC when PEC is enabled. Such exceptions are controlled by the REQ_PEC bit.

If PEC is enabled by EN_PEC and the PEC byte is present in the write transaction, then the master must NACK and assert NIRQ if the PEC byte is incorrect.

If PEC is enabled by EN_PEC, and the PEC byte is not present in the write transaction:

- If REQ_PEC = 0, the device behaves as described by the SMBus specification and do not assert NIRQ.
- If REQ_PEC = 1, the device treats the missing PEC as an incorrect PEC, and asserts NIRQ.

Figure 36 and Figure 37 show the write and read operation with CTL_2.EN_PEC enabled. In order for PEC calculations (from the start to stop commands). Assume that these transactions are complete as depicted and are not followed by a repeated start command.

Note that when PEC is enabled, the register address auto-increment is disabled. This removes the sequential writes and reads.

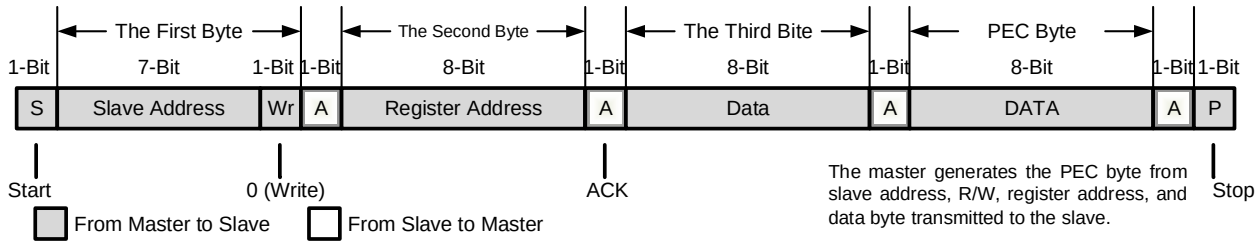


Figure 36: Write Sequence with PEC

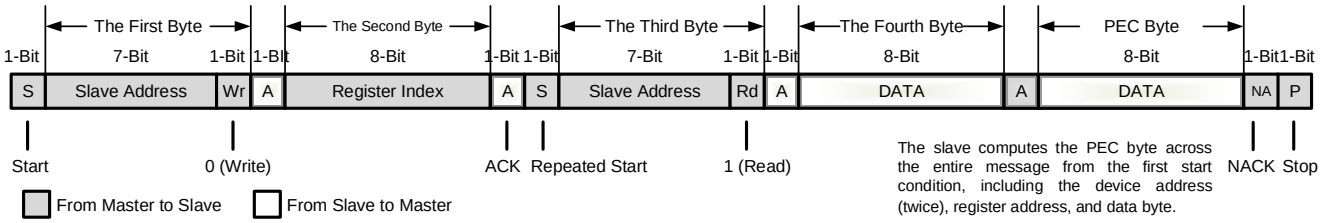


Figure 37: Read Sequence with PEC

Table 6 shows the transactional I²C behavior.

Table 6: I²C Transactions Behavior

#	I²C Transaction	Expected Behavior
1	Single-byte write to a valid register with valid data.	Normal condition. Acknowledge the register address byte and data byte. Write byte to register.
2	Single-byte write to an invalid register.	Acknowledge the register address byte and data byte. Ignore the data byte.
3	Single-byte write to protect a register (as per PROT1/2).	Acknowledge the register address byte and data byte. Ignore the data byte.
4	Single-byte write to a valid register with invalid data.	Acknowledge the register address byte and data byte. Ignore the data byte.
5	Single-byte write to a valid register with valid data, but an invalid PEC byte.	Acknowledge the register address byte and data byte. Do not acknowledge the PEC byte + interrupt. Ignore the data byte.
6	Single-byte read from a valid register.	Normal condition. Acknowledge the register address byte. Data is returned.
7	Single-byte read from an invalid register.	Acknowledge the register address byte. 0x00 data is returned.
8	Single-byte read from a protected register (as per PROT1/2).	Normal condition. Acknowledge the register address byte. Data is returned.
9	Single-byte read from a valid register with an invalid PEC byte.	The master must handle an invalid PEC byte for reads.
10	Multi-byte write starting at a valid address and ending at a valid address.	Normal condition. Acknowledge the register address byte and data bytes. Write bytes to registers.
11	Multi-byte write starting at valid address and crossing into an invalid or protected address.	Acknowledge the register address byte and data bytes. Write bytes to valid registers. Ignore data bytes for invalid or protected registers.
12	Multi-byte write starting at a valid address, crossing into an invalid or protected address, then back to valid address.	Acknowledge the register address byte and data bytes. Write bytes to valid registers. Ignore data bytes for invalid or protected registers.
13	Multi-byte read starting at a valid address and ending at a valid address.	Normal condition. Acknowledge the register address byte. Data is returned.
14	Multi-byte read starting at a valid address and crossing into an invalid register.	Acknowledge the register address byte. Data is returned for valid addresses. 0x00 is returned for invalid addresses.
15	Multi-byte read starting at a valid address, crossing into an invalid register, then back to a valid address.	Acknowledge the register address byte. Data is returned for valid addresses. 0x00 is returned for invalid addresses.

REGISTER MAP

Add.	Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Default (9)	Group
0x00~0x0F: Device Information												
0x00	DEVICE_ID	R	DEV_ID[7:0]								09	-
0x01	DEVICE_REV	R	DEV_REV[7:0]								81	-
0x02 … 0x0F	RESERVED	-	RESERVED									-
0x10~0x1F: Interrupts and Status Registers												
0x10	INT_SRC1	RW1C	F_INTERNAL	EM_PD	WDT	F_PEC	RTC	F_EN	F_OSC	F_NRSTIRQ	-	-
0x11	INT_SRC2	RW1C	F_OTHER	RESERVED	F_RT_CRC	F_BIST	F_LDO	F_TSD	F_ECC_DED	F_PBSP	-	-
0x12	INT_OTHER	RW1C	RESERVED						F_2P5M	F_BG	-	-
0x13	CTL_STAT	R	RESERVED		ST_NIRQ	ST_NRST	ST_ACTSLP	ST_ACTSHDN	ST_DEV[1:0]		-	-
0x14	EN_STDR1	R	RESERVED				STDR_EN12	STDR_EN11	STDR_EN10	STDR_EN9	-	-
0x15	EN_STDR2	R	STDR_EN8	STDR_EN7	STDR_EN6	STDR_EN5	STDR_EN4	STDR_EN3	STDR_EN2	STDR_EN1	-	-
0x16	EN_STRD1	R	RESERVED				STRD_EN12	STRD_EN11	STRD_EN10	STRD_EN9	-	-
0x17	EN_STRD2	R	STRD_EN8	STRD_EN7	STRD_EN6	STRD_EN5	STRD_EN4	STRD_EN3	STRD_EN2	STRD_EN1	-	-
0x18	WDT_STAT	R	RESERVED				OPEN	RESERVED	WDUV	WDEXP	-	-
0x19	TEST_STAT	R	RESERVED	BIST_C	ECC_SEC	RESERVED	BIST_VM	BIST_OTP	BIST_L	BIST_A	-	-
0x1A	LAST_RST	R	NRST_IN	WDT_RST	LP_NPWR_BTN	NEM_PD	ACTSHDN	WDT_SHDN	FORCE_SHDN[1:0]		-	-
0x1B … 0x1F	RESERVED	-	RESERVED								-	-
0x20~0x2F: Configuration Registers												
0x20	EN_ALT_F	R	RESERVED				EN_AF12	EN_AF11	EN_AF10	EN_AF9	0x02	-
0x21	AF_IN_OUT	R	RESERVED				AFIO12	AFIO11	AFIO10	AFIO9	0x02	-
0x22	EN_CFG1	R	RESERVED				PP_EN12	PP_EN11	PP_EN10	PP_EN9	0x0F	-
0x23	EN_CFG2	R	PP_EN8	PP_EN7	PP_EN6	PP_EN5	PP_EN4	PP_EN3	PP_EN2	PP_EN1	0xFF	-
0x24	CLK_CFG	R	XTAL_LOAD	XTAL_EN	RESERVED						0xC0	-
0x25	GP_OUT	R/W	RESERVED				GPO12	GPO11	GPO10	GPO9	0x00	WRK
0x26	DEB_IN	R/W	DEBOUNCE[3:0]				EN_DEB12	EN_DEB11	EN_DEB10	RESERVED	0x00	CTL
0x27	LP_TTSHLD	R/W	LP_TIME_TSHLD[7:0]								0x00	CTL
0x28	CTL_1	R/W	RESERVED				FORCE_INT	FORCE_ACT	FORCE_SHDN[1:0]		0x04	WRK
0x29	CTL_2	R/W	RST_DLY[3:0]				RTC_WAKE	RTC_PU	REQ_PEC	EN_PEC	0xC3	CTL

REGISTER MAP *(continued)*

Add.	Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Default (9)	Group
0x2A	TEST_CFG	R/W	RESERVED					AT_SHDN	AT_POR[1:0]		0x03	CTL
0x2B	IEN_OTHER	R/W	RESERVED						IEN_F_2P5M	IEN_F_BG	0x00	CTL
0x2C … 0x2F	RESERVED	-	RESERVED								-	-
0x30~0x6F: Sequencing Registers												
0x30	SEQ_CFG	R/W	RESERVED							SSTEP	0x00	SEQC
0x31	SEQ_USLOT	R/W	TIME[7:0]								0x02	SEQC
0x32	SEQ_DSLOT	R/W	TIME[7:0]								0x02	SEQC
0x33	PWR_EN1	R/W	PU[3:0]				PD[3:0]				0x15	SEQP
0x34	PWR_EN2	R/W	PU[3:0]				PD[3:0]				0x11	SEQP
0x35	PWR_EN3	R/W	PU[3:0]				PD[3:0]				0x24	SEQP
0x36	PWR_EN4	R/W	PU[3:0]				PD[3:0]				0x24	SEQP
0x37	PWR_EN5	R/W	PU[3:0]				PD[3:0]				0x42	SEQP
0x38	PWR_EN6	R/W	PU[3:0]				PD[3:0]				0x61	SEQP
0x39	PWR_EN7	R/W	PU[3:0]				PD[3:0]				0x11	SEQP
0x3A	PWR_EN8	R/W	PU[3:0]				PD[3:0]				0x24	SEQP
0x3B	PWR_EN9	R/W	PU[3:0]				PD[3:0]				0x42	SEQP
0x3C	PWR_EN10	R/W	PU[3:0]				PD[3:0]				0x00	SEQP
0x3D	PWR_EN11	R/W	PU[3:0]				PD[3:0]				0x42	SEQP
0x3E	PWR_EN12	R/W	PU[3:0]				PD[3:0]				0x00	SEQP
0x3F	PWR_CLK32OE	R/W	PU[3:0]				PD[3:0]				0x44	SEQP
0x40 … 0x4F	RESERVED		RESERVED								-	-
0x50 … 0x52	RESERVED		RESERVED								-	-
0x53	SLP_EN1	R/W	SLP_EXIT[3:0]				SLP_ENTRY[3:0]				0x00	SEQS
0x54	SLP_EN2	R/W	SLP_EXIT[3:0]				SLP_ENTRY[3:0]				0x13	SEQS
0x55	SLP_EN3	R/W	SLP_EXIT[3:0]				SLP_ENTRY[3:0]				0x12	SEQS
0x56	SLP_EN4	R/W	SLP_EXIT[3:0]				SLP_ENTRY[3:0]				0x00	SEQS
0x57	SLP_EN5	R/W	SLP_EXIT[3:0]				SLP_ENTRY[3:0]				0x00	SEQS
0x58	SLP_EN6	R/W	SLP_EXIT[3:0]				SLP_ENTRY[3:0]				0x21	SEQS
0x59	SLP_EN7	R/W	SLP_EXIT[3:0]				SLP_ENTRY[3:0]				0x13	SEQS
0x5A	SLP_EN8	R/W	SLP_EXIT[3:0]				SLP_ENTRY[3:0]				0x32	SEQS
0x5B	SLP_EN9	R/W	SLP_EXIT[3:0]				SLP_ENTRY[3:0]				0x41	SEQS

REGISTER MAP *(continued)*

Add.	Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Default (9)	Group
0x5C	SLP_EN10	R/W	SLP_EXIT[3:0]				SLP_ENTRY[3:0]				0x00	SEQS
0x5D	SLP_EN11	R/W	SLP_EXIT[3:0]				SLP_ENTRY[3:0]				0x31	SEQS
0x5E	SLP_EN12	R/W	SLP_EXIT[3:0]				SLP_ENTRY[3:0]				0x00	SEQS
0x5F	SLP_CLK32OE	R/W	SLP_EXIT[3:0]				SLP_ENTRY[3:0]				0x00	SEQS
0x60 … 0x6F	RESERVED		RESERVED								-	-
0x70~0x7F: Real-Time Clock (RTC) Registers												
0x70	RTC_T3	R/W	RTC_T[31:24]								0x00	RTC
0x71	RTC_T2	R/W	RTC_T[23:16]								0x00	RTC
0x72	RTC_T1	R/W	RTC_T[15:8]								0x00	RTC
0x73	RTC_T0	R/W	RTC_T[7:0]								0x00	RTC
0x74	RTC_A3	R/W	RTC_A[31:24]								0xFF	RTC
0x75	RTC_A2	R/W	RTC_A[23:16]								0xFF	RTC
0x76	RTC_A1	R/W	RTC_A[15:8]								0xFF	RTC
0x77	RTC_A0	R/W	RTC_A[7:0]								0xFF	RTC
0x78 … 0x7F	RESERVED		RESERVED								-	-
0x80~0x8F: Watchdog Timer (WDT) Registers												
0x80	WDT_CFG	R/W	WDTEN[1:0]		SLP_EN	WDTDLY[2:0]			PDMD[1:0]		0x00	WDT
0x81	WDT_CLOSE	R/W	CLOSE[7:0]								0x00	WDT
0x82	WDT_OPEN	R/W	OPEN[7:0]								0x00	WDT
0x83	WDTKEY	R/W	KEY[7:0]								0x00	- (10)
0x84 … 0x8F	RESERVED		RESERVED								-	-
0x90 … 0xEF	RESERVED		RESERVED								-	-
0xF0~0xFF: Protection Registers												
0xF0	PROT1	R/W	RESERVED	WRK	SEQS	SEQP	SEQC	WDT	RTC	CTL	0x00	-
0xF1	PROT2	R/W	RESERVED	WRK	SEQS	SEQP	SEQC	WDT	RTC	CTL	0x00	-
0xF2 … 0xF8	RESERVED		RESERVED								-	-
0xF9	I2CADDR	R	RESERVED	ADDR_OTP[6:0]							0x3C	-
0xFA	DEV_CFG	R	RESERVED						SOC_IF[1:0]		0x02	-
0xFB … 0xFF	RESERVED		RESERVED								-	-

Notes:

9) Initial configurations for the MPQ79700FS-0000 registers. The default value can be redefined if the OTP function is available.
10) Although the WDTKEY register belongs to the watchdog function, it is excluded from the WDT protection group as it must remain writeable even though the other WDT protection group registers may be set to read-only.

REGISTER DESCRIPTION

DEVICE_ID (0x00)

Access: Read-only

The DEVICE_ID command returns device information.

Bits	Name	Description
D[7:0]	DEV_ID	Returns device information.

DEVICE_REV (0x01)

Access: Read-only

The DEVICE_REV command returns the revision information.

Bits	Name	Description
D[7:0]	DEV_REV	Returns the revision information.

INT_SRC1 (0x10)

Access: Read and write 1 to clear the bit. Writing 0 to a bit has no effect; writing 1 to a bit that is already set to 0 has no effect.

The INT_SRC1 command indicates the interrupt source. If F_INTERNAL is set, see the INT_SRC2 register on page 48 for more details on the fault. The INT_SRC1 register indicates why NIRQ is asserted. When the host processor receives a NIRQ signal, it may read this register to determine the source of the interrupt. If this register is cleared, then MPQ79700FS does not assert NIRQ.

Bits	Name	Description
D[7]	F_INTERNAL	Indicates whether an internal fault occurred (ORed value for all bits in INT_SRC2). This bit is cleared by clearing the bits in INT_SRC2. If the fault condition in INT_SRC2 is removed, write 1 to clear both this bit and the bits in in INT_SRC2. 0: No internal fault has been detected 1: An internal fault has been detected. Additional details are flagged in the INT_SRC2 register
D[6]	EM_PD	Indicates whether emergency power down has occurred. Write 1 to clear the bit. This bit is set again at the next emergency power down. 0: No emergency power down has occurred 1: An emergency shutdown has occurred (e.g. Sequence 2, V_{DD} dropped below the UVLO threshold while the device was in an on state)
D[5]	WDT	This bit is valid only if WDTEN[1:0] is enabled. Write 1 to clear the bit. The bit is set again at the next WDT violation. 0: No WDT violation has occurred (or WDTEN[1:0] = 00b) 1: A WDT violation has occurred
D[4]	F_PEC	Indicates whether a PEC error has occurred. This bit is valid only if EN_PEC is enabled. Write 1 to clear the bit. The bit is set again at the next PEC error. 0: No PEC error has occurred (or EN_PEC = 0) 1: A PEC error has occurred
D[3]	RTC	Write 1 to clear the bit. The bit sets again at the next RTC alarm. 0: An RTC alarm has not been triggered (or the alarm function is disabled) 1: An RTC alarm has been triggered
D[2]	F_EN	Indicates whether an enable pin output fault has occurred. If the fault has been removed, write 1 to clear the bit. 0: No short-to-high or low-level voltage has been detected 1: A short-to-high or low-level voltage has been detected

D[1]	F_OSC	Indicates whether a crystal oscillator fault has been detected. If the fault has been removed, write 1 to clear the bit. 0: No fault has been detected on the crystal oscillator (or XTAL_EN = 0 (disabled)) 1: A fault detected has been detected on the crystal oscillator; the frequency is outside its ±10% tolerance window
D[0]	F_NRSTIRQ	Indicates whether a fault has been detected on the reset pin (NRST) or interrupt pin (NIRQ). If the fault has been removed, write 1 to clear the bit. 0: No fault has been detected on NRST or NIRQ 1: A low-resistance path to high-level voltage has been detected on either NRST or NIRQ (note that an external short to low-level voltage cannot be determined)

INT_SRC2 (0x11)

Access: Read and write 1 to clear the bit. Writing 0 to a bit has no effect; writing 1 to a bit that is already set to 0 has no effect.

The INT_SRC2 command indicates the interrupt source register for internal errors.

Bits	Name	Description
D[7]	F_OTHER	Indicates whether another internal fault has been detected. The details are reported in INT_OTHER. This bit is cleared by clearing the bits in INT_OTHER. If the fault condition in INT_OTHER is removed, write 1 to clear both this bit and the bits in INT_OTHER. This bit represents the ORed value of all bits in INT_OTHER. 0: No fault has been reported in INT_OTHER 1: A fault has been reported in INT_OTHER
D[6]	RESERVED	Reserved.
D[5]	F_RT_CRC	Indicates whether there is a runtime register CRC fault. Write 1 to clear this bit. If a fault is detected, the bit is set again during the next register's CRC check. 0 : No register CRC fault has been detected 1: A register CRC fault has been detected
D[4]	F_BIST	Indicates whether a BIST fault has occurred. Note that clearing this bit does not clear the results in the TEST_STAT register. Write 1 to clear this bit. If a fault is detected, the bit is set again during next BIST execution. 0: No BIST fault has been detected 1: A BIST fault has been detected
D[3]	RESERVED	Reserved.
D[2]	F_TSD	Indicates whether thermal shutdown has occurred. If the fault has been removed, write 1 to clear the bit. 0: No thermal shutdown has occurred 1: Thermal shutdown has occurred since last reading
D[1]	F_ECC_DED	Indicates whether ECC DED occurred on the OTP configuration load. Write 1 to clear this bit. If a fault is detected, this bit is set during the next OTP configuration load. 0: No ECC-DED has occurred while loading the OTP 1: ECC-DED has occurred while loading the OTP
D[0]	F_PBSP	Indicates whether a NPWR_BTN shot pulse has occurred. This bit is valid only if NPWR_BTN is enabled via the EN_AF12 and AFIO12 bits. Write 1 to clear this bit. If a short pulse is detected on NPWR_BTN, this bit is set again. 0: No short pulse on NPWR_BTN (or NPWR_BTN is not enabled) has been detected 1: A short pulse has been detected on NPWR_BTN

INT_OTHER (0x12)

Access: Read and write 1 to clear the bit. Writing 0 to a bit has no effect; writing 1 to a bit that is already set to 0 has no effect.

The INT_OTHER command indicates the other internal interrupt statuses.

Bits	Name	Description
D[7:2]	RESERVED	Reserved.
D[1]	F_2P5M	Indicates whether an internal 2.5MHz digital clock fault has occurred. If the fault has been removed, write 1 to clear the bit. 0: No clock fault has been detected 1: A clock fault has been detected; the clock frequency is outside its ±10% tolerance window
D[0]	F_BG	Indicates whether a bandgap reference voltage fault has occurred. If the fault has been removed, write 1 to clear the bit. 0: No bandgap fault has been detected 1: A bandgap fault has been detected; the bandgap reference voltage is outside its ±10% tolerance window

CTL_STAT (0x13)

Access: Read-only

The CTL_STATE command indicates the MPQ79700FS's control pin states and internal state.

Bits	Name	Description
D[7:6]	RESERVED	Reserved.
D[5]	ST_NIRQ	Indicates the current state of the NIRQ output. 0: The NIRQ pin asserts low 1: The NIRQ pin does not assert low
D[4]	ST_NRST	Indicates the current state of the NRST output. 0: The NRST pin asserts low 1: The NRST pin does not assert low
D[3]	ST_ACTSLP	Indicates the current state of the ACT/SLP input. 0: The ACT/SLP pin driven low (SLP) 1: The ACT/SLP pin driven high (ACT)
D[2]	ST_ACTSHDN	Indicates the current state of the ACT/SHDN input. 0: The ACT/SHDN pin is driven low (SHDN) 1: The ACT/SHDN pin is driven high (ACT)
D[1:0]	ST_DEV[1:0]	Indicates the device's current operating state. 00b: SHDNx, power up, power down 01b: SLEEP, sleep entry, sleep exit 10b: Invalid combination 11b: ACTIVE

EN_STDR1 (0x14)

Access: Read-only

The EN_STDR1 command indicates the current drive status of the ENx pins (internal digital logic output).

Bits	Name	Description
D[7:4]	RESERVED	Reserved.

D[3]	STDR_EN12	Indicates the current drive state of ENx. 0: The sequencer is driving ENx low 1: The sequencer is driving ENx high or allowing it to float
D[2]	STDR_EN11	
D[1]	STDR_EN10	
D[0]	STDR_EN9	

EN_STDR2 (0x15)

Access: Read-only

The EN_STDR2 command indicates the current drive status of the ENx pins (internal digital logic output).

Bits	Name	Description
D[7]	STDR_EN8	Indicates the current drive state of ENx. 0: The sequencer is driving ENx low 1: The sequencer is driving ENx high or allowing it to float
D[6]	STDR_EN7	
D[5]	STDR_EN6	
D[4]	STDR_EN5	
D[3]	STDR_EN4	
D[2]	STDR_EN3	
D[1]	STDR_EN2	
D[0]	STDR_EN1	

EN_STRD1 (0x16)

Access: Read-only

The EN_STRD1 command indicates the current read status of the ENx pins (external analog output).

Bits	Name	Description
D[7:4]	RESERVED	Reserved.
D[3]	STRD_EN12	Indicates the sequencer's current read state for ENx. 0: ENx is low 1: ENx is high or floating
D[2]	STRD_EN11	
D[1]	STRD_EN10	
D[0]	STRD_EN9	

EN_STRD2 (0x17)

Access: Read-only

The EN_STRD2 command indicates the current read status of the ENx pins (external analog output).

Bits	Field Name	Description
D[7]	STRD_EN8	Indicates the sequencer's current read state for ENx. 0: ENx is low 1: ENx is high or floating
D[6]	STRD_EN7	
D[5]	STRD_EN6	
D[4]	STRD_EN5	
D[3]	STRD_EN4	
D[2]	STRD_EN3	
D[1]	STRD_EN2	
D[0]	STRD_EN1	

WDT_STAT (0x18)

Access: Read-only

The WDT_STAT command indicates the WDT status.

Bits	Name	Description
D[7:4]	RESERVED	Reserved.
D[3]	OPEN	Indicates whether the WDTKEY is updated in open or close window. 0: Close 1: Open
D[2]	RESERVED	Reserved.
D[1]	WDUV	Indicates whether a watchdog update violation has been detected. It is cleared after being read. 0: No violation has been detected 1: The watchdog updated too early
D[0]	WDEXP	Indicates whether the watchdog close timer expired without updating WDKEY. It is cleared after being read. 0: WDT has not expired 1: WDT expired

TEST_STAT (0x19)

Access: Read-only

The TEST_STAT command returns the internal self-test and ECC statuses.

Bits	Name	Description
D[7]	RESERVED	Reserved.
D[6]	BIST_C	Indicates the BIST state. 0: BIST is running (or has not been executed since last POR). Check the TEST_CFG register 1: BIST is complete
D[5]	ECC_SEC	Returns the status of the ECC SEC during an OTP configuration load. 0: No error correction has been applied 1: SEC has been applied
D[4]	RESERVED	Reserved.
D[3]	BIST_VM	Returns the status of the VM test output from BIST. 0: The volatile memory test passed 1: The volatile memory test failed
D[2]	BIST_OTP	Returns the status of the OTP test output from BIST. 0: The OTP test passed 1: The OTP test failed
D[1]	BIST_L	Returns the status of the logic test output from BIST. 0: The logic test passed 1: The logic test failed
D[0]	BIST_A	Returns the status of the analog test output from BIST. 0: The analog test passed 1: The analog test failed

LAST_RST (0x1A)

Access: Read-only

The LAST_RST command returns the reason of the last NRST assertion or shutdown. NRST assertion and shutdown occur in Sequence 2, Sequence 5, Sequence 6, Sequence 7, and Sequence 8. The register is maintained as long as V_{DD} and/or V_{BAT} is present. The register is overwritten with new relevant data during the next NRST assertion or shutdown.

If an emergency power down (Sequence 2) occurs, it is recorded in EM_PD register bit and the LAST_RST register is cleared. It is recommended that the host reads INT_SRC1 when it first starts up.

Bits	Field Name	Description
D[7]	NRST_IN	Indicates whether NRST asserted due to NRST_IN (if enabled via the EN_ALT_F and AF_IN_OUT registers). 0: NRST_IN did not cause the last NRST assertion 1: NRST_IN caused the last NRST assertion
D[6]	WDT_RST	Indicates whether NRST asserted due to the WDT (see the WDT_CFG register on page 61). 0: WDT did not cause the last NRST assertion 1: WDT caused the last NRST assertion
D[5]	LP_NPWR_BTN	Indicates whether NRST assertion or shutdown was due to NPWR_BTN (if enabled via the EN_ALT_F and AF_IN_OUT registers). 0: NPWR_BTN long-press is not the cause for the last NRST assertion or shutdown 1: A NPWR_BTN long-press caused the last NRST assertion or shutdown
D[4]	NEM_PD	Indicates whether NRST assertion or shutdown was due to NEM_PD (if enabled via the EN_ALT_F and AF_IN_OUT registers). 0: NEM_PD did not cause the last NRST/shutdown 1: NEM_PD caused the last NRST/shutdown
D[3]	ACTSHDN	Indicates whether NRST assertion or shutdown was due to ACT/SHDN asserting low (shutdown). 0: ACT/SHDN going low did not cause the last NRST shutdown 1: ACT/SHDN going low caused the last NRST shutdown
D[2]	WDT_SHDN	Indicates whether NRST assertion or shutdown is due to WDT. If this bit is set, FORCE_SHDN[1:0] does not contain the PDMD[1:0] value. 0: WDT did not cause the last NRST shutdown 1: WDT caused the last NRST shutdown
D[1:0]	FORCE_SHDN [1:0]	Indicates whether NRST assertion or shutdown is due to FORCE_SHDN[1:0] ≠ 00b. The value is the same as the FORCE_SHDN[1:0] that initiated the last NRST assertion or shutdown. Note that if the WDT_SHDN bit is set, this bit field is always 00b.

EN_ALT_F (0x20)

Access: Read-only, once loaded from the OTP

The EN_ALT_F command enables alternate functions for the sequencing pins (EN9–EN12) (the function is selected via the AF_IN_OUT register). The alternate function can be enabled only if the corresponding PU/PD/SLP_EXIT/SLP_ENTRY registers fields are all set to 00h. If any of those bit fields are non-zero, the corresponding pin is locked to its ENx sequencing function.

Contact an MPS FAE if this register must be updated.

Bits	Field Name	Description
D[7:4]	RESERVED	Reserved.

D[3]	EN_AF12	Enables the alternate function for EN12. 0: Disabled 1: Enabled (GPO12 or NPWR_BTN)
D[2]	EN_AF11	Enables the alternate function for EN11. 0: Disabled 1: Enabled (GPO11 or NRST_IN)
D[1]	EN_AF10	Enables the alternate function for EN10. 0: Disabled 1: Enabled (GPO10 or NEM_PD)
D[0]	EN_AF9	Enables the alternate function for EN9. 0: Disabled 1: Enabled (GPO9)

AF_IN_OUT (0x21)

Access: Read-only, once loaded from the OTP

The AF_IN_OUT command sets the alternate functions for the sequencing pins (EN9–EN12) (enabled via the EN_ALT_F register).

Contact an MPS FAE if this register must be updated.

Bits	Field Name	Description
D[7:4]	RESERVED	Reserved.
D[3]	AFIO12	Selects the alternate function of EN12: 0: General-purpose output (GPO), GPO12 1: NPWR_BTN (power button input)
D[2]	AFIO11	Selects the alternate function of EN11: 0: GPO11 1: NRST_IN (reset input)
D[1]	AFIO10	Selects the alternate function of EN10: 0: GPO10 1: NEM_PD (emergency shutdown input)
D[0]	AFIO9	Selects the alternate function of EN9. EN9 can only be selected as GPO9 through EN_ALT_F, bit[0], and does not have an alternate function. 0: GPO9 1: Invalid

EN_CFG1 (0x22)

Access: Read-only, once loaded from the OTP

The EN_CFG1 command sets the drive mode configuration for EN9–EN12.

Contact an MPS FAE if this register must be updated.

Bits	Name	Description
D[7:4]	RESERVED	Reserved.
D[3]	PP_EN[12]	Configures the ENx pin's output type. 0: Open drain 1: Push-pull
D[2]	PP_EN[11]	
D[1]	PP_EN[10]	
D[0]	PP_EN[9]	

EN_CFG2 (0x23)

Access: Read-only once loaded from the OTP

The EN_CFG2 command sets the drive mode configuration for EN1–EN8.

Contact an MPS FAE if this register must be updated.

Bits	Field Name	Description
D[7]	PP_EN8	Configures the ENx pin's output type. 0: Open-drain 1: Push-pull
D[6]	PP_EN7	
D[5]	PP_EN6	
D[4]	PP_EN5	
D[3]	PP_EN4	
D[2]	PP_EN3	
D[1]	PP_EN2	
D[0]	PP_EN1	

EN_CFG2 (0x24)

Access: Read-only, once loaded from the OTP

The EN_CFG2 command configures the crystal oscillator.

Contact an MPS FAE if this register must be updated.

Bits	Name	Description
D[7]	XTAL_LOAD	Sets the crystal oscillator load's capacitance: 0: External 1: Internal (default for crystal oscillator that requires 12.5pF load capacitor)
D[6]	XTAL_EN	Enables the crystal oscillator. 0: Disabled 1: Enabled
D[5:0]	RESERVED	Reserved.

GP_OUT (0x25)

Access: Read/write. Read-only if the CTL group is protected.

The GP_OUT command sets the general-purpose output state for the sequencing pins (EN9–EN12). The GPO function is enabled via the AF_IN_OUT and EN_ALT_F registers.

Bits	Field Name	Description
D[7:4]	RESERVED	Reserved.
D[3]	GPO12	EN12 general-purpose output. Only used when both PWR_EN12 and SLP_EN12 are clear (register 0x3E = 00h and register 0x5E = 00h). 0: The EN12 pin is low 1: The EN12 pin is high
D[2]	GPO11	EN11 general-purpose output. Only used when both PWR_EN11 and SLP_EN11 are clear (register 0x3D = 00h, and register 0x5D = 00h). 0: The EN11 pin is low 1: The EN11 pin is high

D[1]	GPO10	EN10 general-purpose output. Only used when both PWR_EN10 and SLP_EN10 are clear (register 0x3C = 00h and register 0x5C = 00h). 0: The EN10 pin is low 1: The EN10 pin is high
D[0]	GPO9	EN9 general-purpose output. Only used when both PWR_EN9 and SLP_EN9 are clear (register 0x3B = 00h and register 0x5B = 00h). 0: The EN9 pin is low 1: The EN9 pin is high

DEB_IN (0x26)

Access: Read/write. Read-only if the CTL group is protected.

The DEB_IN command sets the debounce configuration for the alternate function input pins.

Bits	Name	Description
D[7:4]	DEBOUNCE[3:0]	Sets the debounce value for alternate function pins, calculated with the following equation: Debounce time = 5 x (DEBOUNCE[3:0] +1)ms 0000b: 5ms 0001b: 10ms … 1111b: 80ms Note that this debounce time is both valid for the input signal's rising and falling edges.
D[3]	EN_DEB12	Enables the debounce for the ENx pin. 0: Disabled 1: Enabled
D[2]	EN_DEB11	
D[1]	EN_DEB10	
D[0]	RESERVED	Reserved.

LP_TTSHLD (0x27)

Access: Read/write. Read-only if the CTL group is protected.

The LP_TTSHLD command configures the NPWR_BTN long-press threshold.

Bits	Field Name	Description
D[7:0]	LP_TIME_TSHLD	If NPWR_BTN is enabled, this value is in 100ms increments, and determines the minimum duration of the NPWR_BTN pulse to be detected as a long-press (a shorter press is a short-press). The press time threshold can be calculated with the following equation: LP_TIME_TSHLD = 100 x (LP_TTSHLD [7:0] +1) ms 00h: 100ms 01h: 200ms ... FEh: 25.5s FFh: 25.6s

CTL_1 (0x28)

Access: Read/write. Read-only if the CTL group is protected.

The CTL_1 command configures the interrupt and state SW control.

Bits	Field Name	Description
D[7:4]	RESERVED	Reserved.
D[3]	FORCE_INT (11)	Forces the NIRQ pin low. 0: The NIRQ pin controlled by the INT_SRCx register fault 1: Forces the NIRQ pin low

D[2]	FORCE_ACT	Forces the sequencer to ACTIVE state. FORCE_ACT is automatically set by HW when entering Sequence 1. As the sequencer performs the power up sequence, ACT/SLP may be undefined. FORCE_ACT being set prevents a bad ACT/SLP level from causing an unexpected transition into SLEEP state. I²C commands can clear this bit, but cannot set it. 0: ACT/SLP pin controls sleep entry/exit. Cleared only by I²C writes 1: ACT/SLP is ignored. Set only by the HW
D[1:0]	FORCE_ SHDN[1:0]	Sets the sequencer's shutdown state response. If NPWR_BTN disabled (EN_AF12 = 0b): 00b: Normal ACT/SHDN pin control 01b: Force a power down sequence, then resume normal ACT/SHDN pin control immediately 10b: Force a power down sequence, then resume normal ACT/SHDN pin control after a 1 second delay 11b: Force a power down sequence, then resume normal ACT/SHDN pin control when ACT/SHDN is low or when an RTC alarm occurs (per the configurations in CTL_2, RTC_T, and RTC_A) If NPWR_BTN is enabled (EN_AF12 = 1b): 00b: Normal NPWR_BTN pin control 01b: Force a power down sequence, then move to Sequence 1 immediately (proceed as if ACT/SHDN is high 10b: Force a power down sequence, then move to Sequence 1 after 1 second (proceed as if ACT/SHDN is high). If NPWR_BTN is pressed before the 1 second expires, then move to Sequence 1 11b: Force a power down sequence, then move to Sequence 1 when an RTC alarm occurs as (per the configurations in CTL_2, RTC_T, and RTC_A) (proceed as if ACT/SHDN is high). If NPWR_BTN is pressed before the RTC alarm, then move to Sequence 1

Note:

11) FORCE_INT is used by the software to periodically check for an internal or external short to high level voltage on the NIRQ pin.

CTL_2 (0x29)

Access: Read/write. Read-only if the CTL group is protected.

The CTL_2 command sets miscellaneous configurations.

Bits	Field Name	Description
D[7:4]	RST_DLY[3:0]	Configures the power up sequence. After the last sequenced ENx/CLK32K assertion, NRST remains asserted until RST_DLY[3:0]. For the power down sequence, NRST asserts within t_{NRST} while ACT/SHDN is low. 0000b: 0.1ms 1000b: 1ms 0001b: 0.2ms 1001b: 2ms 0010b: 0.4ms 1010b: 4ms 0011b: 0.8ms 1011b: 8ms 0100b: 1.6ms 1100b: 16ms 0101b: 3.2ms 1101b: 32ms 0110b: 6.4ms 1110b: 64ms 0111b: 12.8ms 1111b: 128ms

D[3]	RTC_WAKE	Enables the autonomous RTC wake-up alarm. If RTC_T = RTC_A, a wake-up event is generated and sets the RTC bits. If this bit is enabled, then FORCE_ACT is set to 1, which triggers an automatic exit from the SLEEP state to the ACTIVE state. This bit must be enabled before RTC_T = RTC_A; otherwise, the automatic exit from the SLEEP state is not triggered. 0: Disabled (FORCE_ACT = 0 on an RTC alarm) 1: Enabled (FORCE_ACT = 1 on an RTC alarm)
D[2]	RTC_PU	Enables autonomous RTC power up from SHDN2 to ACTIVE. If RTC_T = RTC_A, a power up event is generated. This bit must be enabled before RTC_T = RTC_A; otherwise, the power up event is not triggered. 0: Disabled 1: Enabled
D[1]	REQ_PEC	Requires a PEC byte (valid only if EN_PEC is set to 1). 0: A missing PEC byte is treated as a good PEC 1: A missing PEC byte is treated as a bad PEC and triggers a fault
D[0]	EN_PEC	Enables PEC. When enabled, it disables support for the register address auto-increment. 0: Disabled. Ignore the REQ_PEC bit setting, and allow multi-byte sequential I^2C writes and reads 1: Enabled. Multi-byte sequential I^2C writes and reads are not supported

TEST_CFG (0x2A)

Access: Read/write. Read-only if the CTL group is protected.

The TEST_CFG command configures built-in self-test (BIST) execution. See the Built-In Self-Test (BIST) and Configuration Load section on page 26 for more information.

Bits	Name	Description
D[7:3]	RESERVED	Reserved.
D[2]	AT_SHDN	Runs BIST when the device ready after t_{CFG_WB}. This bit cannot be set via the OTP. It always defaults to 0 when loading configurations from the OTP. 0: Do not run BIST when exiting Sequence 5 or Sequence 6 1: Run BIST when exiting Sequence 5 or Sequence 6 if FORCE_SHDN[1:0] = 00b
D[1:0]	AT_POR[1:0]	Runs BIST during POR. The device is ready after t_{CFG_WB}. Set to 11b to enable AT_POR; setting these bits to 01b and 10b is not recommended. 00b: If there a valid OTP configuration, skip BIST at POR 01b: If there is a corrupt OTP configuration, run BIST at POR 10b: If there is a corrupt OTP configuration, run BIST at POR 11b: If a valid OTP configuration, run BIST at POR

IEN_OTHER (0x2B)

Access: Read/write. Read-only if the CTL group is protected.

The IEN_OTHER command enables certain functions for the INT_OTHER register.

Bits	Name	Description
D[7:2]	RESERVED	Reserved.
D[1]	IEN_F_2P5M	Enables the 2.5MHz internal clock fault interrupt. 0: Disabled 1: Enabled
D[0]	IEN_F_BG	Enables the internal bandgap reference interrupt. 0: Disabled 1: Enabled

SEQ_CFG (0x30)

Access: Read/write. Read-only if the SEQ group is protected.

The SEQ_CFG command configures sequencing.

Bits	Name	Description
D[7:1]	RESERVED	Reserved.
D[0]	SSTEP	Selects the sequencing time slot step size (t_{SSTEP}) for SEQ_USLOT and SEQ_DSLOT: 0b: 250µs 1b: 1000µs

SEQ_USLOT (0x31)

Access: Read/write. Read-only if the SEQ group is protected.

The SEQ_USLOT command configures the time slot for power up and exiting SLEEP mode.

Bits	Name	Description
D[7:0]	TIME[7:0]	Sets the time slot between the sequencing points for power up and exiting SLEEP mode, calculated with the following question: t_{USLOT} = TIME[7:0] x t_{SSTEP} + t_{SMIN} Where t_{SSTEP} is set by SSTEP and t_{SMIN} = t_{SSTEP} / 2. If SSTEP = 0b:

Parameter	Symbol	Min (-6%)	Typ	Max (+6%)	Units
Slot step size	t_{SSTEP}	235	250	265	µs
Min slot time (0x00)	t_{SMIN}	117.5	125	132.5	µs
Max slot time (0xFF)	t_{SMAX}	60042.5	63875	67707.5	µs

If SSTEP = 1b:

Parameter	Symbol	Min (-6%)	Typ	Max (+6%)	Units
Slot step size	t_{SSTEP}	940	1000	1060	µs
Min slot time (0x00)	t_{SMIN}	470	500	530	µs
Max slot time (0xFF)	t_{SMAX}	240170	255500	270830	µs

SEQ_DSLOT (0x32)

Access: Read/write. Read-only if SEQ group is protected.

The SEQ_DSLOT command configures the times slot for power down and entering SLEEP mode.

Bits	Field Name	Description
D[7:0]	TIME[7:0]	Sets the time slot between the sequencing points for power down and entering SLEEP mode, calculated with the following equation: t_{DSLOT} = TIME[7:0] x t_{SSTEP} + t_{SMIN} Where t_{SSTEP} is set by SSTEP and t_{SMIN} = t_{SSTEP} / 2. See the SEQ_USLOT register above for more details.

PWR_EN1~PWR_EN12 (0x33~0x3E)

Twelve 8-bit registers.

Access: Read/write. Read-only if the SEQ group is protected.

The PWR_EN1~PWR_EN12 command sets the power up and power down definition by the EN1–EN12 assignments to one of fifteen time slots. Slot 1 is the earliest slot that can be selected, and it indicates that the ENx pin toggles in the first time slot after the triggering event. See the Output Sequencing section on page 28 for more details.

Bits	Name	Description
D[7:4]	PU[3:0]	Sets the power up sequence for ENx. 0h: The ENx pin is not mapped to sequence. ENx maintains its previous state, unless entering BACKUP or FAILSAFE (ENx is pulled low in these states) 1h: The ENx pin is mapped to first time slot (first to power up) Fh: The ENx pin is mapped to last time slot (last to power up)
D[3:0]	PD[3:0]	Sets the power down sequence for ENx. 0h: The ENx pin is not mapped to the sequence. ENx maintains its previous state, unless entering BACKUP or FAILSAFE (ENx is pulled low in these states) 1h: The ENx pin is mapped to first time slot (first to shut down) Fh: The ENx pin is mapped to last time slot (last to shut down)

PWR_CLK32OE (0x3F)

Access: Read/write. Read-only if the SEQ group is protected.

The PWR_CLK32OE command sets the power up and power down sequence assignment of the 32kHz clock output to one of fifteen time slots.

Bits	Name	Description
D[7:4]	PU[3:0]	0h: CLK32 is not mapped to the power up sequence. CLK32 maintains its previous state, unless entering BACKUP or FAILSAFE (CLK32 is pulled low in these states) 1h: Enable CLK32 at the first power up time slot Fh: Enable CLK32 at the last power up time slot
D[3:0]	PD[3:0]	0h: CLK32 is not mapped to the power down sequence. CLK32 maintains its previous state, unless entering BACKUP or FAILSAFE (CLK32 is pulled low in these states) 1h: Disable CLK32 at the first power down time slot Fh: Disable CLK32 at the last power down time slot

SLP_EN1~SLP_EN12 (0x53~0x5E)

Twelve 8-bit registers.

Access: Read/write. Read-only if the SEQ group is protected.

The SLP_EN1~SLP_EN12 command sets the sleep exit/entry sequence definition by the EN1–EN12 assignments to one of fifteen time slots. Slot 1 is the earliest slot that can be selected, and it indicates that the ENx pin toggles in the first time slot after the triggering event. See Output Sequencing section on page 28 for more details.

Bits	Name	Description
D[7:4]	SLP_EXIT[3:0]	Sets the exit sleep sequence for ENx. 0h: The ENx pin is not mapped to sequence. ENx maintains its previous state, unless entering BACKUP or FAILSAFE (ENx is pulled low in these states) 1h: The ENx pin is mapped to first time slot (first to power up) Fh: The ENx pin is mapped to last time slot (last to power up)

D[3:0]	SLP_ENTRY[3:0]	Sets the enter sleep sequence for ENx. 0h: The ENx pin is not mapped to sequence. ENx maintains its previous state, unless entering BACKUP or FAILSAFE (ENx is pulled low in these states) 1h: The ENx pin is mapped to first time slot (first to power up) Fh: The ENx pin is mapped to last time slot (last to power up)

SLP_CLK32OE

Access: Read/write. Read-only if the SEQ group is protected.

The SLP_CLK32OE command sets the sleep exit/entry sequence assignment for the 32kHz clock output to one of fifteen time slots.

Bits	Name	Description
D[7:4]	SLP_EXIT[3:0]	0h: CLK32 is not mapped to the sleep exit sequence. CLK32 maintains its previous state, unless entering BACKUP or FAILSAFE (CLK32 is pulled low in these states). 1h: Enable CLK32 at the first sleep exit time slot Fh: Enable CLK32 at the last sleep exit time slot
D[3:0]	SLP_ENTRY[3:0]	0h: CLK32 is not mapped to the sleep entry sequence. CLK32 maintains its previous state, unless entering BACKUP or FAILSAFE (CLK32 is pulled low in these states). 1h: Disable CLK32 at the first sleep entry time slot Fh: Disable CLK32 at the last sleep entry time slot

RTC_T[31:0] (0x70~0x73)

Four 8-bit registers.

Access: Read/write. Read-only if the RTC group is protected.

The RTC_T[31:0] command sets the RTC time. RTC_T3 the first to be accessed, while RTC_T0 is the last. Set or read the RTC_T value from RTC_T3 to RTC_T0 in sequence. For data coherency, see the Real-Time Clock (RTC) on page 34 for more details.

Bits	Field Name	Description
D[31:24]	RTC_T3	Register address 0x70. RTC time byte 3.
D[23:16]	RTC_T2	Register address 0x71. RTC time byte 2.
D[15:8]	RTC_T1	Register address 0x72. RTC time byte 1.
D[7:0]	RTC_T0	Register address 0x73. RTC time byte 0.

RTC_A[31:0] (0x74~0x77)

Four 8-bit registers.

Access: Read/Write. Read-only if RTC group is protected.

The RTC_A[31:0] command sets the RTC alarm. RTC_A3 is the first to be accessed, while RTC_A0 is the last. Set or read the RTC_A value from RTC_A3 to RTC_A0 in sequence. For data coherency, see the Real-Time Clock (RTC) on page 34 for more details.

Bits	Field Name	Description
D[31:24]	RTC_A3	Register address 0x74. RTC alarm byte 3.
D[23:16]	RTC_A2	Register address 0x75. RTC alarm byte 2.
D[15:8]	RTC_A1	Register address 0x76. RTC alarm byte 1.
D[7:0]	RTC_A0	Register address 0x77. RTC alarm byte 0.

WDT_CFG (0x80)

Access: Read/write. Read-only if the WDT group is protected.

The WDT_CFG command configures the watchdog.

Bits	Name	Description
D[7:6]	WDTEN[1:0]	Enables the watchdog. 00b: Disabled 01b: On successive violations, first interrupt (NIRQ assertion), reset (NRST assertion), then shut down according to PDMD 10b: On successive violations, first reset (NRST assertion) then shut down according to PDMD 11b: Shut down according to PDMD if the watchdog violation occurs
D[5]	SLP_EN	Automatically disables the watchdog in SLEEP mode. 0: Disabled 1: Enabled
D[4:2]	WDTDLY[2:0]	Sets the delay, in the number of WDT periods (WDT_CLOSE + WDT_OPEN), from the de-assertion of NRST (if exiting the SHDN1 or SHDN2 states), the value written to WDTEN[1:0], or from the exit SLEEP state (if WDT_CFG, bit[5] = 1b), to the first close window. 000b: 1 WDT period 001b: 2 WDT periods … 111b: 8 WDT periods
D[1:0]	PDMD[1:0]	Power down mode for WDT forced shutdown. Value written to FORCE_SHDN[1:0] on WDT shutdown event. The WDT shutdown event occurs regardless of the ACT/SHDN state at the time of the WDT violation. The PDMD value is written to FORCE_SHDN[1:0] while executing Sequence 5 or Sequence 6, and determines the behavior once the SHDN2 state is entered.

WDT_CLOSE (0x81)

Access: Read/write. Read-only if the WDT group is protected.

The WDT_CLOSE command configures the watchdog's close window.

Bits	Field Name	Description
D[7:0]	CLOSE[7:0]	Sets the watchdog's close window duration. 00h~1Fh: CLOSE[7:0] + 1ms 20h~3Fh: (CLOSE[7:0] - 32) x 2 + 34ms 40h~FFh: (CLOSE[7:0] - 64) x 4 + 100ms The LSB increments values are listed below:

1ms (00h~1Fh)	2ms (20h~Fh)	4ms (40h~FFh)
00h: 1ms	20h: 34ms	40h: 100ms
01h: 2ms	21h: 36ms	41h: 104ms
02h: 3ms	22h: 38ms	42h: 108ms
...	...	...
1Eh: 31ms	3Eh: 94ms	FEh: 860ms
1Fh: 32ms	3Fh: 96ms	FFh: 864ms

WDT_OPEN (0x82)

Access: Read/write. Read-only if the WDT group is protected.

The WDT_OPEN command configures the watchdog's open window.

Bits	Field Name	Description
D[7:0]	OPEN[7:0]	Sets the watchdog's open window duration. 00h~1Fh: OPEN [7:0] + 1ms 20h~3Fh: (OPEN [7:0] - 32) x 2 + 34ms 40h~FFh: (OPEN [7:0] - 64) x 4 + 100ms The LSB increments values are listed below:

1ms (00h~1Fh)	2ms (20h~Fh)	4ms (40h~FFh)
00h: 1ms	20h: 34ms	40h: 100ms
01h: 2ms	21h: 36ms	41h: 104ms
02h: 3ms	22h: 38ms	42h: 108ms
...	...	...
1Eh: 31ms	3Eh: 94ms	FEh: 860ms
1Fh: 32ms	3Fh: 96ms	FFh: 864ms

WDTKEY (0x83)

Access: Read/write

The WDTKEY command sets the watchdog reset key.

Bits	Name	Description
D[7:0]	KEY[7:0]	Watchdog key register. Writing any value that is different from the last time is valid for the watchdog input.

PROT1, PROT2 (0xF0, 0xF1)

Access: Read/write

For security, these registers have a POR value = 0x00, and each bit in each register becomes read-only once set. If any bit is set to 1, it cannot be cleared to 0 by the host. These bits can only be cleared (and allow writing different protecting registers configurations) by cycling the power on VDD (entering BACKUP or OFF state), or by executing BIST when exiting Sequence 5 or Sequence 6 (AT_SHDN = 1b).

The PROTx command selects the protection. To write-protect a register group, the host must set the relevant bit in both the PROT1and PROT2 registers.

Bits	Field Name	Description
D[7]	RESERVED	Reserved.
D[6]	WRK	0: The working registers are writeable 1: Writes to the working registers are ignored
D[5]	SEQS	0: The sleep sequence registers are writeable 1: Writes to the sleep sequence registers are ignored
D[4]	SEQP	0: The power down sequence registers are writeable 1: Writes to the power sequence registers are ignored
D[3]	SEQC	0: The sequence slot configuration registers are writeable 1: Writes to the sequence slot configuration registers are ignored
D[2]	WDT	0: The WDT registers are writeable 1: Writes to WDT registers are ignored
D[1]	RTC	0: The RTC registers are writeable 1: Writes to the RTC registers are ignored

D[0]	CTL	0: The control registers are writeable 1: Writes to the control registers are ignored

I2CADDR (0xF9)

Access: Read-only

The I2CADDR command returns the I²C address.

Bits	Name	Description
D[7]	RESERVED	Reserved.
D[6:0]	ADDR_OTP[6:0]	Returns the I²C slave device address, set via the OTP.

DEV_CFG (0xFA)

Access: Read-only

The DEV_CFG command configures the device options.

Bits	Field Name	Description
D[7:2]	RESERVED	Reserved.
D[1:0]	SOC_IF[1:0]	Sets the I²C interface level (includes the I²C pins, SCL/SDA). 00b: 1.2V/1.8V, with V_{IL} / V_{IH} = 0.36V / 0.84V 01b: Reserved 10b: 3.3V, with V_{IL} / V_{IH} = 0.76V / 1.29V 11b: Reserved

APPLICATION INFORMATION

Figure 38 shows the MPQ79700FS's typical application circuit.

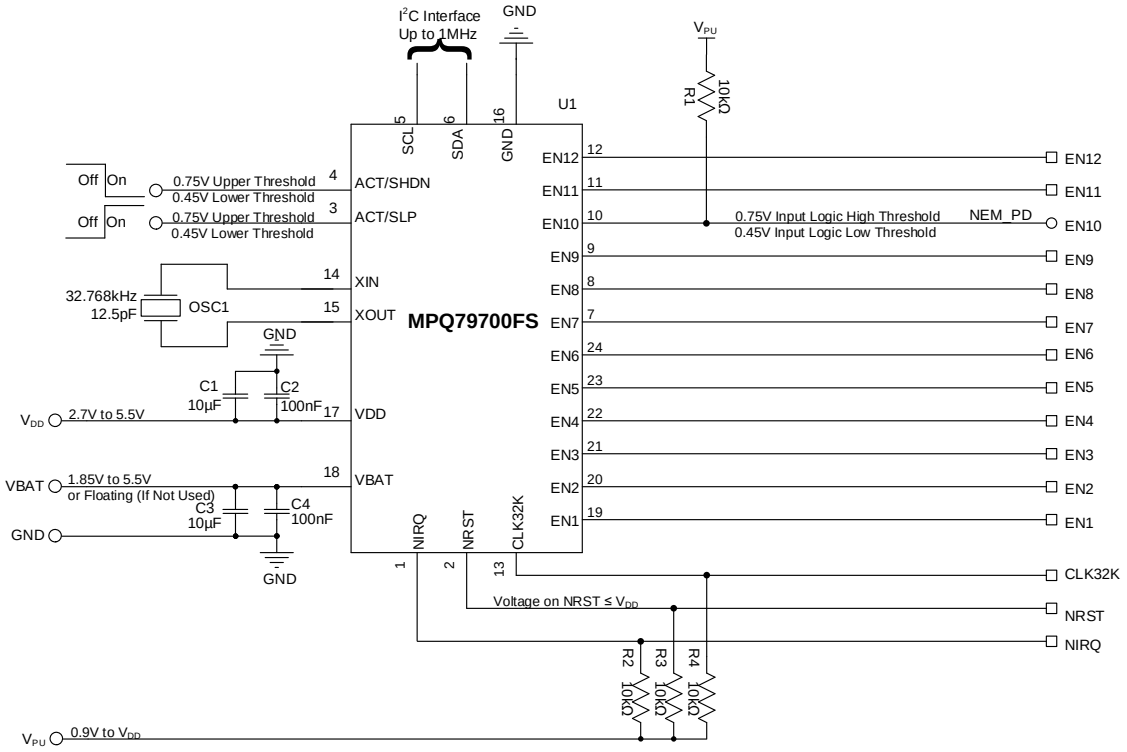


Figure 38: ENx Configured as Push-Pull (NEM_PD [EN10) Input Enabled)

Table 7 shows the design guide index based on Figure 38.

Table 7: Design Guide Index

Pin #	Name	Components	Design Guide Index
1	NIRQ	R2	Setting the Interrupt Signal Output (NIRQ, Pin 1)
2	NRST	R3	Setting the Reset Signal Output (NRST, Pin 2)
3	ACT/SLP	-	Setting the ACT/SLP Control Signal Input (ACT/SLP, Pin 3)
4	ACT/ SHDN	-	Setting the ACT/SHDN Control Signal Input (ACT/SLP, Pin 3)
5	SCL	-	Setting the I²C Interface (SCL, Pin 5; SDA, Pin 6)
6	SDA	-	
7, 8, 9, 11, 12, 19–24	EN1–EN9, EN11, EN12	-	Setting the Enable Signals Outputs (EN1–EN6, Pins 19–24; EN7–EN9, Pins 7–9; EN11–EN12, Pins 11–12)
10	EN10	R1	Setting the Alternate Function (NEM_PD) Signal Input (EN10, Pin 10)
13	CLK32K	R4	Setting the 32.768kHz Square Wave Output (CLK32K, Pin 13)
14	XIN	OSC1	Setting the 32.768kHz Crystal Oscillator Connection (XIN, Pin 14; XOUT, Pin 15)
15	XOUT		
16	GND	-	Setting the GND Connection (GND, Pins 16)
17	VDD	C1, C2	Selecting the Input Capacitors for VDD (VDD, Pin 17)
18	VBAT	C3, C4	Selecting the Input Capacitors for VBAT (VBAT, Pin 18)

Interrupt and Reset Indicator (NIRQ, Pin1; NRST, Pin 12)

Both the NIRQ and NRST pins are separately connected to the open drain of an internal MOSFET. For status indication, they should be connected to a voltage source through an external pull-up resistor.

The pull-up voltage on NIRQ is between 0.9V and 5.5V. It is recommended to stay below V_{DD}.

The pull-up voltage on NRST is between 0.9V and V_{DD}, and must not exceed V_{DD}.

The R_{PU} resistance (R2 and R3) value is recommended to be between 4.7kΩ and 100kΩ.

Float NIRQ (or NRST) if it is not used.

ACT/SLP and ACT/SHDN Input Control (ACT/SLP, Pin 3; ACT/SHDN, Pin 4)

The ACT/SLP and ACT/SHDN pins are digital control pins.

Drive ACT/SHDN above its 0.75V logic-high threshold to enter ACTIVE state (if the NPWR_BTN function is disabled). The ENx and CLK32K signals then start up in the order configured by the corresponding registers. Drive ACT/SHDN below its 0.45V logic-low threshold to enter a shutdown state (if the NPWR_BTN function is disabled). The ENx and CLK32K signals then shut down in the order configured by the corresponding registers.

The ACT/SLP pin has the same 0.75V logic high and 0.45V logic low thresholds as the ACT/SHDN pin. During ACTIVE state when ACT/SLP control is enabled (register 0x28, bit[2] = 0), drive ACT/SLP above or below its logic-high/low threshold exit or enter the SLEEP state. The ENx and CLK32K signals transition in the order configured by the corresponding registers.

Both ACT/SHDN and ACT/SLP do not require an external pull-up resistor to be connected to the signal source. The signal source voltage level can be either above or below V_{DD}, without a backdrive current from ACT/SHDN and ACT/SLP to VDD. An internal 100kΩ resistor is separately connected from ACT/SHDN and ACT/SLP to GND. ACT/SHDN and ACT/SLP are pulled low when they are floating.

ACT/SHDN or ACT/SLP can be connected to a voltage source through an external pull-up resistor. Figure 39 shows the internal circuit for the ACT/SHDN and ACT/SLP pins.

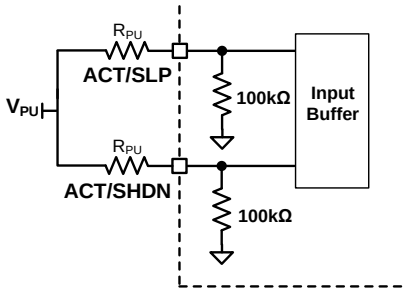


Figure 39: ACT/SHDN and ACT/SLP Pin Circuit

The pull-up resistance (R_{PU}) range can be calculated with Equation (1) and Equation (2):

$$R_{PU} < \frac{100k\Omega}{\frac{V_{PU\_H}}{0.75V} - 1} \quad (1)$$

$$R_{PU} > \frac{100k\Omega}{\frac{V_{PU\_L}}{0.45V} - 1} \quad (2)$$

Where V_{PU_H} and V_{PU_L} are the high and low voltage levels of V_{PU}, respectively.

I²C Interface (SCL, Pin 5; SDA, Pin 6)

The MPQ79700FS works as a slave-only device. It supports up to 1Mbs of bidirectional data transfer in fast-mode plus, which adds flexibility to the power sequencer application and provides advanced diagnoses. See the I²C Interface section on page 40 for more details.

If the I²C interface is not used, it is recommended to connect these pins to the VDD pin through a resistor (e.g. 100kΩ).

Setting the Enable Signals Outputs (EN1–EN6, Pins 19–24; EN7–EN9, Pins 7–9; EN11–EN12, Pins 11–12)

The MPQ79700FS's output pins can be set as open-drain or push-pull types via registers 0x22 and 0x23. Figure 40 on page 66 shows the ENx pin's internal circuit.

If the ENx output is configured as push-pull, it does not require an external pull-up resistor to connect ENx to a voltage source. The ENx output is driven by V_{DD} internally. If the output is high, M1 is on, M2 is off, and the ENx voltage (V_{ENx}) is close to V_{DD}. If the output is low, M1 is off, M2 is on, and V_{ENx} is close to 0V.

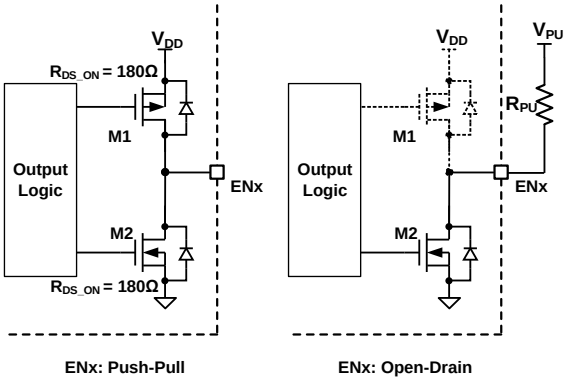


Figure 40: ENx Pin Circuit (Output)

If the ENx output is configured as an open drain, use an external pull-up resistor to connect ENx to a voltage source. In this scenario, M1 is always off while M2 turns on/off to output low or high. If the output is high, V_{ENx} is close to V_{PU}. If the output is low, V_{ENx} is close to 0V. It is recommended that the V_{PU} not exceed V_{DD}. Otherwise, the M1 body diode may conduct. This clamps the ENx high level to about V_{DD} + 0.7V, where 0.7V is the body diode's forward voltage.

However, if V_{PU} does not turn off after V_{DD}, there must be a backwards current flowing into ENx in the BACKUP state, where V_{DD} is 0V. A high-value R_{PU} can reduce the backwards current. It is recommended that R_{PU} be between 4.7kΩ and 100kΩ.

Figure 38 on page 64 shows EN10 configured as an open drain, while the other ENx outputs are configured as push-pull types. The other ENx outputs can connect directly to drive the enable input of a subsequent IC. However, although configured as push-pull, the ENx pins can be connected to a voltage source through an external pull-up resistor. In this scenario, the ENx output's high level can be estimated with Equation (3):

$$V_{OHEN} = V_{DD} \times \frac{180}{180 + R_{PU}} + V_{PU} \times \frac{R_{PU}}{180 + R_{PU}} \quad (3)$$

Where V_{PU} is the external voltage source, and R_{PU} is the pull-up resistance.

Setting the Alternate Function Signal Input (EN10, Pin 10)

The EN10 pin can be set as an input or output via the 0x20 and 0x21 registers. Figure 41 shows the ENx pins internal circuit as input.

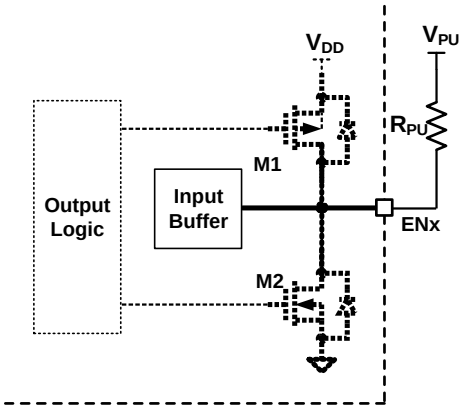


Figure 41: ENx Pin Circuit (Input)

When EN10 is configured as an input, M1 and M2 are always off, regardless of whether EN10 is set to push-pull or open drain. Connect EN10 to a voltage source through an external pull-up resistor. Otherwise, F_EN may be triggered during BIST.

The pull-up resistance for R1 is recommended to be between 4.7kΩ and 100kΩ, and V_{PU} should not exceed V_{DD}.

EN11 and EN12 can also be configured as inputs. Although EN10 (or EN11/EN12) is configured as an input, it is still driven low when entering BACKUP state, since the chip stops operating and the analog circuits force all ENx pins low in BACKUP state.

Setting the 32.768kHz Square Wave Output (CLK32K, Pin 13)

The CLK32K pin is connected to the open drain of an internal MOSFET. For status indication, it should also be connected to a voltage source through an external pull-up resistor.

The pull-up resistance for R4 is recommended to be between 4.7kΩ and 100kΩ.

Float CLK32K if it is not used.

Setting the 32.768kHz Crystal Oscillator Connection (XIN, Pin 14; XOUT, Pin 15)

If the crystal driver is enabled via register 0x24, the CLK32K pin outputs a square wave that is generated by the crystal. In addition, the user can select on-chip internal load capacitors or external load capacitors for the crystal via register 0x24.

Place a 32.768kHz crystal between the XIN and XOUT pins. Crystals of different frequencies are not supported. If an external load capacitor is selected, it is recommended to use the C0G ceramic capacitor as the crystal load's capacitor, and the capacitance is referred to the crystal's requirement. The MPQ79700FS's default internal capacitor is designed for a 12.5pF load capacitor. If the internal load capacitor is selected, use a 32.768kHz crystal with a load capacitor of 12.5pF. Contact an MPS FAE if an internal load capacitor is selected when the crystal load capacitor is not 12.5pF.

Float the XIN and XOUT pins if the crystal driver is not used.

Setting the GND Connection (GND1, Pins 16)

See the PCB Layout Guidelines section on page 68 for more details.

Selecting the Input Capacitors for VDD (VDD, Pin 17)

The VDD capacitor is recommended to be between 1µF and 10µF. It is strongly recommended to use an additional, lower-value capacitor (e.g. 0.1µF) with a small package size (0603) to absorb high-frequency switching noise. Place these capacitors as close to VDD and GND as possible.

Selecting the Input Capacitors for VBAT (VBAT, Pin 18)

For the VBAT capacitor, follow the same selection criteria as the VDD capacitor. It is recommended to use a 1µF to 10µF ceramic capacitor and an additional, lower-value capacitor (e.g. 0.1µF) with a small package size (0603). Place these capacitors as close to VBAT and GND as possible.

Setting Low-Power Mode (LPM)

During normal operation, the MPQ79700FS's quiescent current (I_Q) is typically 600µA. If a lower I_Q is required for the application, low-power mode (LPM) can be implemented to reduce I_Q to about 74µA in SHDNx state or 120µA in ACTIVE/SLEEP state.

In LPM, the internal clock is off at steady states (SHDNx, ACTIVE, SLEEP). However, since the internal clock is off, F_OSC detection is also invalid. There is a tradeoff between low I_Q and the F_OSC detection function.

If LPM is required, contact an MPS FAE for more details.

Power Up/Down Sequence when FORCE_SHDN = 01b

When ACT/SHDN high and FORCE_SHDN = 01b, the ACT/SHDN pin control resumes immediately after a power down sequence is completed, then a power up sequence is triggered. If one ENx is configured for power down in the last slot while starting up in Slot 1, this ENx pin follows a particular behavior (see Figure 42).

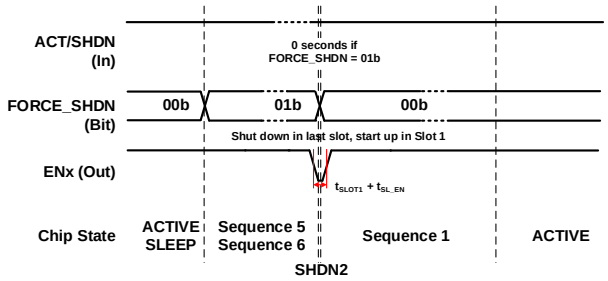


Figure 42: Power up/down when FORCE_SHDN = 01b

ENx has a low pulse that is as long as t_{SLOT1} + t_{SL_EN}. t_{SLOT1} + t_{SL_EN} is typically about 2.5µs. 2.5µs is short enough that it may be deglitched by the enable input of a subsequent IC.

To avoid a short pulse in this situation, it is recommended to not configure ENx to the last slot while starting up slot 1.

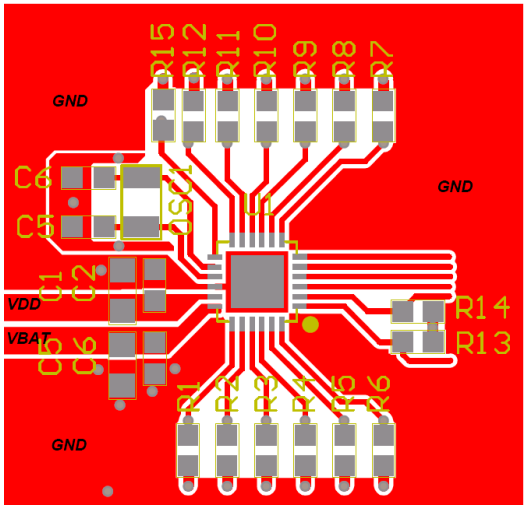
PCB Layout Guidelines (12)

Efficient PCB layout (especially for crystal oscillator placement) is critical for stable operation. A 4-layer layout is recommended. For the best results, refer to Figure 43 and follow the guidelines below:

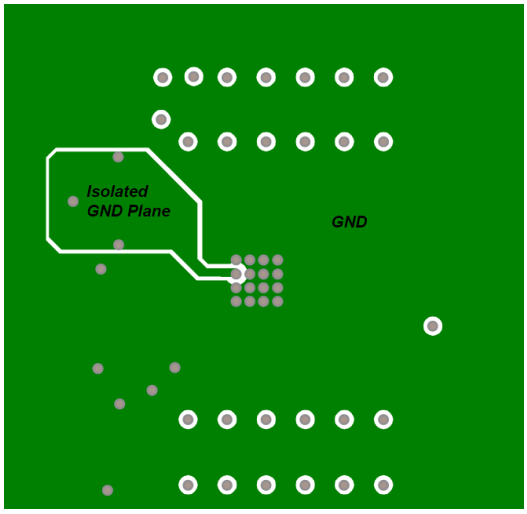
1. Place the ceramic input capacitor, especially the small package size (0603) bypass capacitor, as close to the VDD/VBAT and GND pins as possible to minimize high-frequency noise.
2. Use a large ground plane to connect directly to GND. If the bottom layer is a ground plane, add vias near GND.
3. Place the crystal oscillator as close to the XIN and XOUT pins as possible.
4. Place the crystal oscillator's load capacitors symmetrically and as close to the XIN/XOUT and GND pins as possible.
5. Place an isolated ground plane under the crystal oscillator area. This isolated ground is connected at one point to GND layer.
6. Use multiple vias to connect the power planes to the internal layers.

Notes:

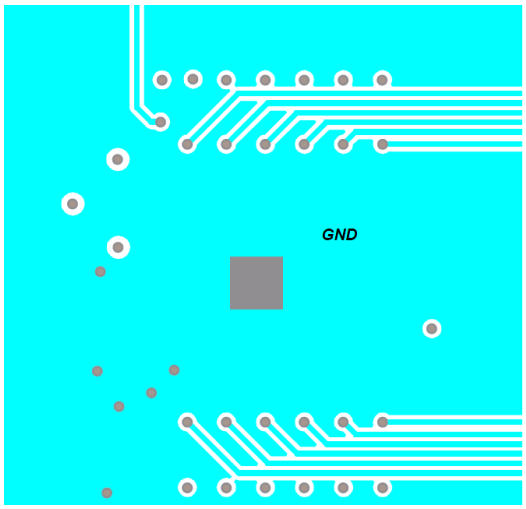
12) The recommended PCB layout is based on the typical application circuit (see Figure 45 on page 69).



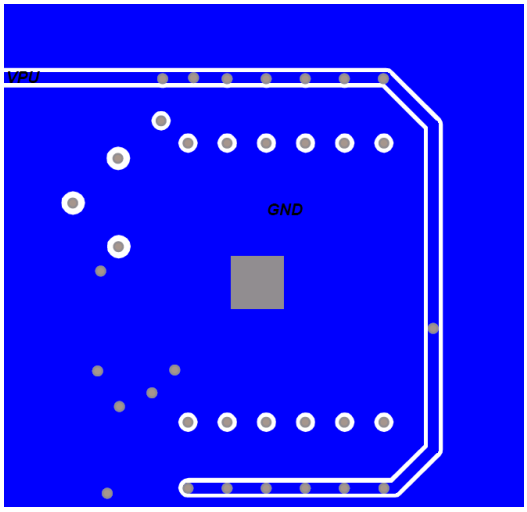
Top Layer



Inner Layer 1



Inner Layer 2



Bottom Layer

Figure 43: Recommended PCB Layout

TYPICAL APPLICATION CIRCUITS

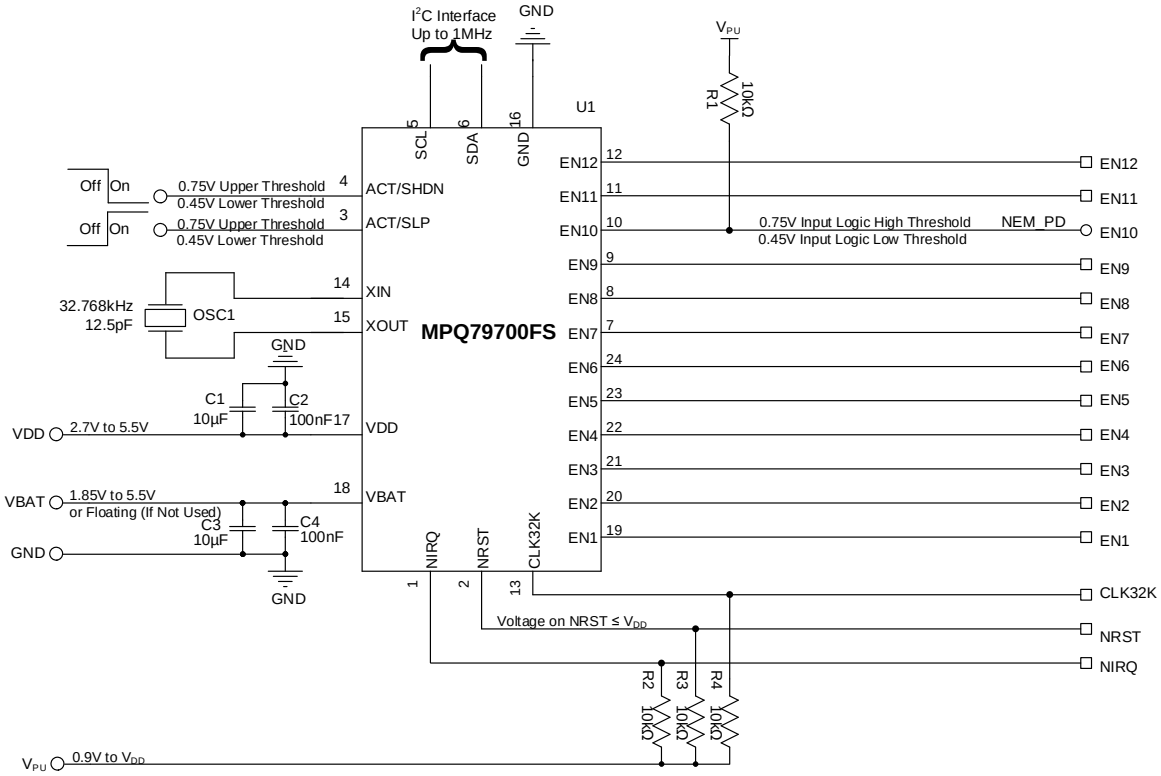


Figure 44: ENx Configured as Push-Pull (Internal Load Capacitor for Crystal Oscillator and NEM_PD are Enabled)

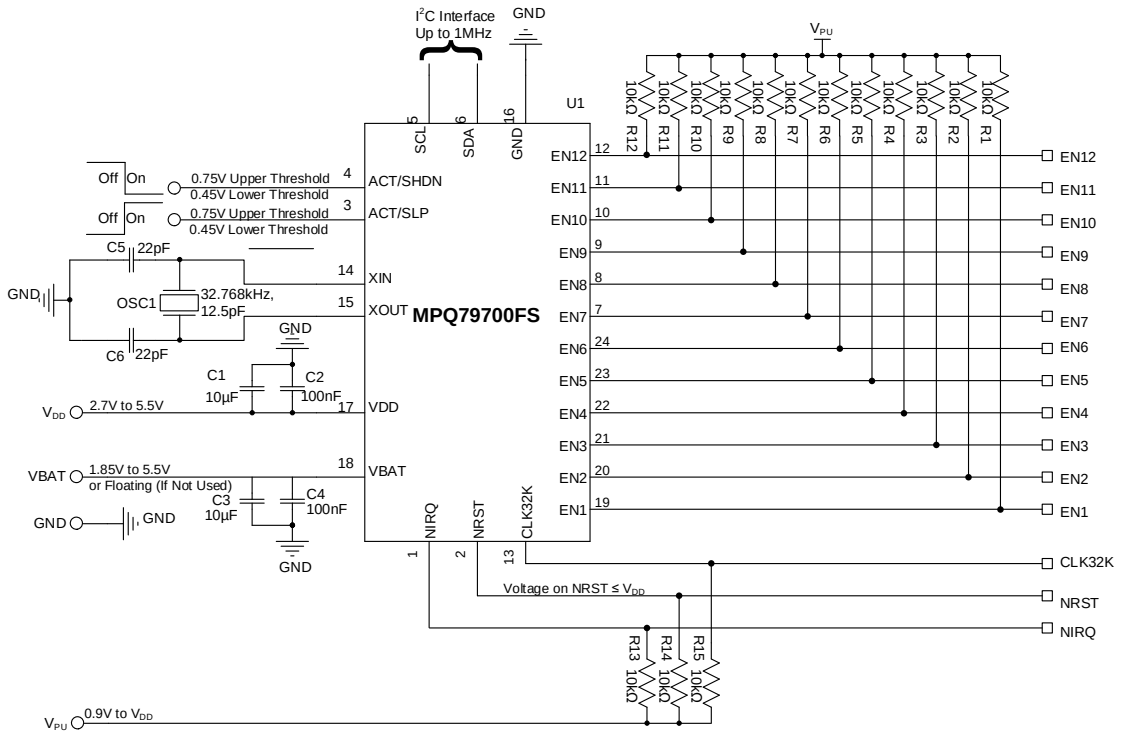
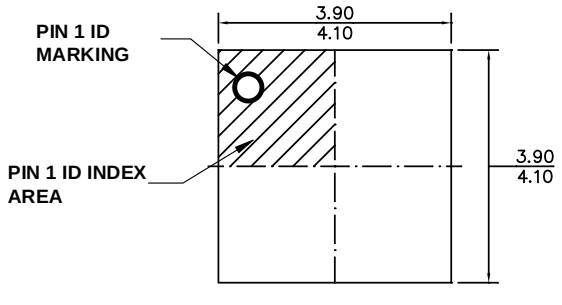


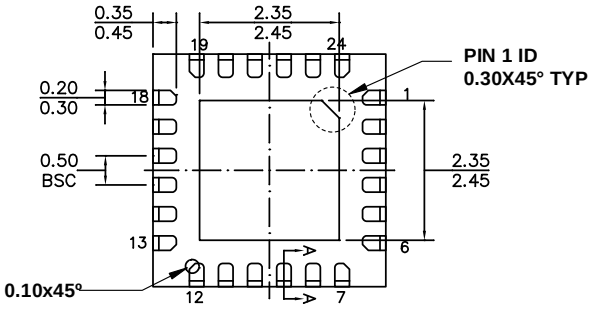
Figure 45: ENx Configured as Open Drain (External Load Capacitor for Crystal Oscillator)

PACKAGE INFORMATION

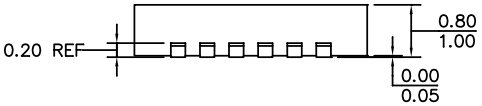
QFN-24 (4mmx4mm)
Wettable Flank



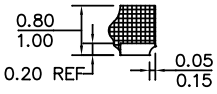
TOP VIEW



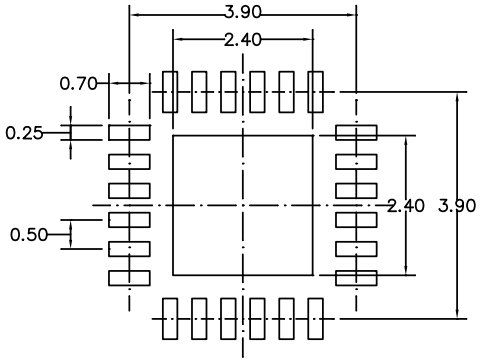
BOTTOM VIEW



SIDE VIEW



SECTION A-A

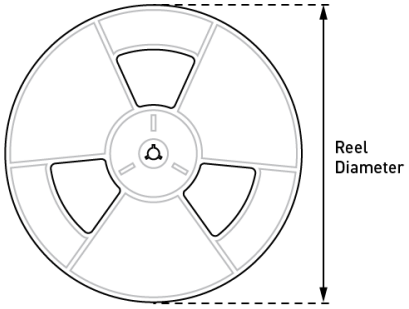


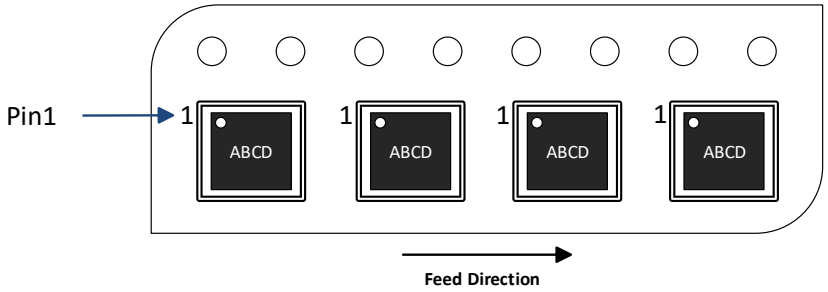
RECOMMENDED LAND PATTERN

NOTE:

1) THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION





Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ79700FSGRE-xxxx-AEC1-Z	QFN-24 (4mmx4mm)	5000	N/A	N/A	13in	12mm	8mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	6/3/2022	Initial Release	-