MPQ7225A

16-Channel, Current Sink LED Driver with Adaptive Feedback Control (AFC), AEC-Q100 Qualified

DESCRIPTION

The MPQ7225A is a 16-channel, current sink LED driver. Each channel is rated for up to 200mA of current, and 16 ICs can be cascaded together to create a 256-channel solution.

The MPQ7225A is optimized for animated or dynamic lighting applications. It employs 12-bit pulse-width modulation (PWM) dimming and 6-bit analog dimming register per channel, with individual control of each channel. The MPQ7225A is designed to function across distanced PCBs with a robust, high-speed, CAN-compatible differential interface.

The MPQ7225A features adaptive feedback control (AFC) to maximize system efficiency. The output voltage of the pre-regulator (e.g. buck voltage regulator) is adjusted in real time so that the voltage across the channels is kept to a minimum (300mV headroom at 200mA).

Frequency spread spectrum (FSS) optimizes EMC performance. The LED current's ramping rate and the phase shift between channels can be digitally configured as well.

The MPQ7225A can aid a system design for functional safety with failsafe (/FS) indicator. It also features an enhanced LED open/short protection scheme (hiccup and latch modes). Additional protection features include ISET pin open/short protection and thermal shutdown. If a fault condition occurs, then the fault indicator pulls low and the matching fault register is set.

The MPQ7225A is available in a QFN-32 (5mmx6mm) package, and is AEC-Q100 qualified.

FEATURES

- Scalability:
    - 16 Channels, 200mA (Max) per Channel
    - Cascade Up to 16 ICs /256 Channels
    - Pin-Configurable Device Address
- Designed for Automotive Applications:
    - Supports Up to 2.5V Cold Crank
    - -40°C to +150°C Operating Junction Temperature (T_J)

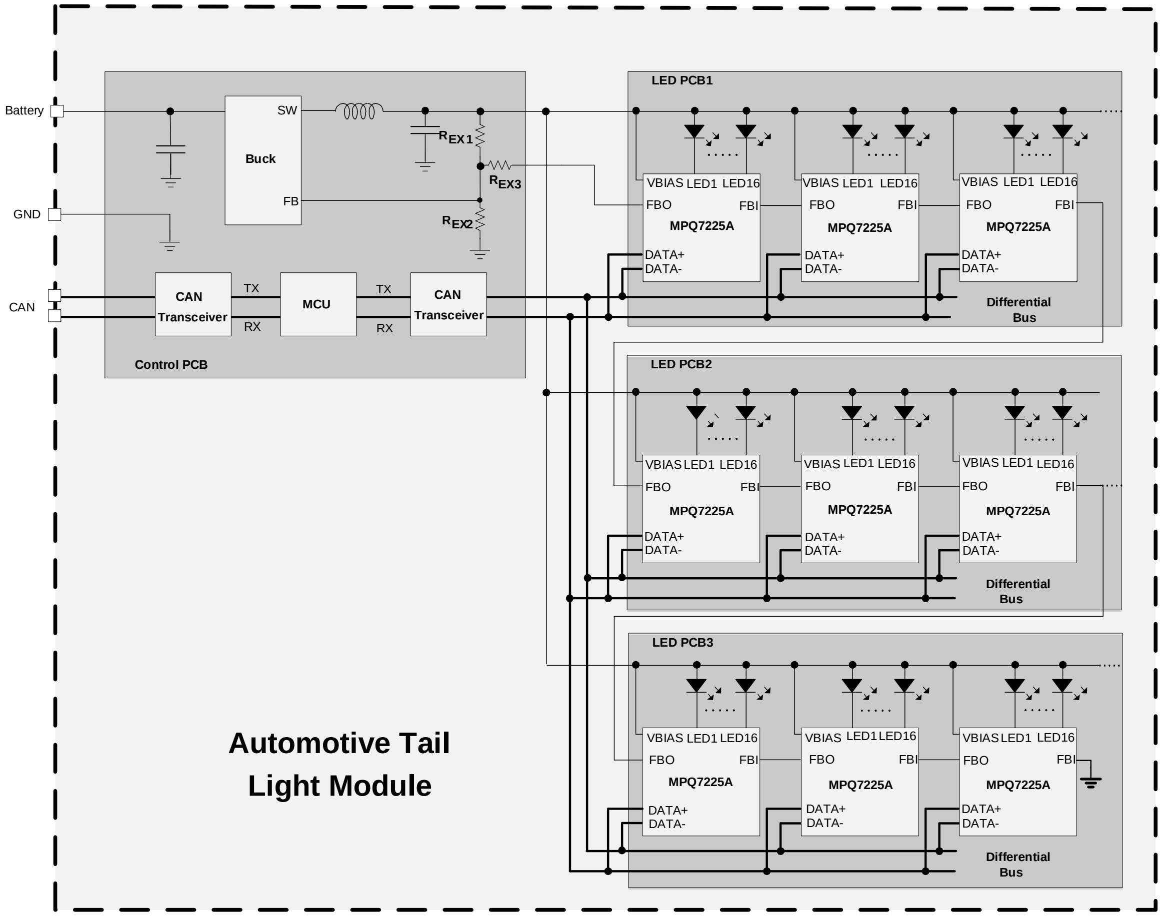
FEATURES *(continued)*

- Cooler Thermals and Optimized Efficiency:
    - Adaptive Feedback Control (AFC) Dynamically Optimizes Pre-Regulator Output (300mV Headroom at 200mA)
    - Headroom Optimization for Multiple ICs
- Robust Communication:
    - 2Mbps CAN Compatible Differential Interface
    - 12-Bit Pulse-Width Modulation (PWM) Dimming or 6-Bit Analog Dimming for Each Channel
- Optimized EMI/EMC:
    - Configurable Phase Shift and Slew Rate
    - Frequency Spread Spectrum (FSS) (Internal Clock)
    - Selectable PWM Dimming Frequency
    - CISPR25 Class 5 Compliant
- Additional Features:
    - Functional Safety Document Available to Support System in Achieving ASIL Requirements
    - Failsafe (/FS) Pin and Fault Registers for System Protection and Diagnostics
        - LED Short (to GND and Battery)
        - LED Open
        - Thermal Warning and Shutdown
        - ISET Pin Open/Short
- One-Time Programmable (OTP) Memory
- Available in a QFN-32 (5mmx6mm) Package with Wettable Flanks
- Available in AEC-Q100 Grade 1

APPLICATIONS

- Dynamic/Animated Tail Lights
- Adaptive Matrix Headlights
- Daytime Running Lights (DRLs)
- Turn Signals
- Puddle Lights

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating**
MPQ7225AGQJE-xxxx-AEC1***, ****	QFN-32 (5mmx6mm)	*See Below*	2

* For Tape & Reel, add suffix -Z (e.g. MPQ7225AGQJE-xxxx-AEC1-Z).

** Moisture Sensitivity Level Rating

*** “xxxx” is the configuration code identifier for the register settings stored in the OTP register. Each “x” can be a hexadecimal value between 0 and F. The default code is “0000”. Contact an MPS FAE to create this unique number.

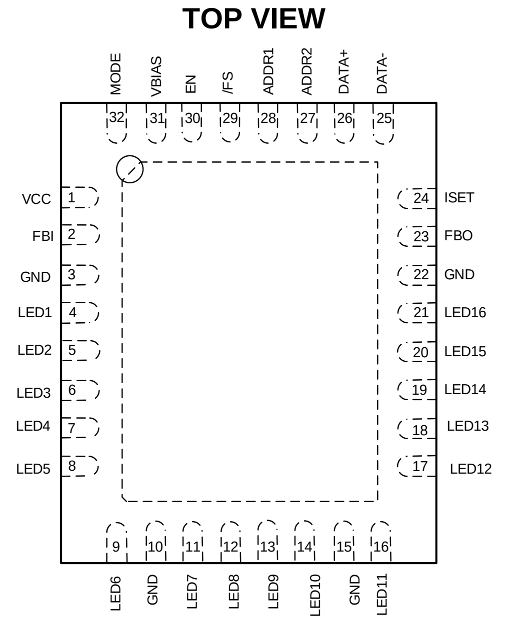
****Wettable flank

TOP MARKING

MPSYYWW
MP7225A
LLLLLLL
E

MPS: MPS prefix
YY: Year code
WW: Week code
MP7225A: Part number
LLLLLLL: Lot number
E: Wettable flank

PACKAGE REFERENCE



QFN-32 (5mmx6mm)

PIN FUNCTIONS

Pin #	Name	Description
1	VCC	**Internal bias supply.** The VCC pin is powered by VBIAS, and supplies power to the internal control circuit and gate drivers. Place a ≥10µF decoupling capacitor between VCC and ground, close to VCC. VCC requires power from an external source if V_{BIAS} is below 3.5V.
2	FBI	**Feedback input.** The FBI pin indicates the current sink headroom information input between multiple MPQ7225A devices. Connect FBI to GND if it is not used.
3, 10, 15, 22	GND	**Ground.** GND is the reference ground of the power device, and requires careful consideration during PCB layout.
4, 5, 6, 7, 8, 9, 11, 12, 13, 14, 16, 17, 18, 19, 20, 21	LED1–LED16	**LED channel 1–16 current inputs**. Connect the cathodes of LED channels 1–16 to these pins. Connect any unused LEDx pins to GND, and disable LEDx through the CHx_EN (0x03) register.
23	FBO	**Feedback output.** Connect the FBO pin to the DC/DC converter's feedback pin through a resistor divider network. FBO provides the current sink headroom information output between multiple MPQ7225A devices. Float this pin if adaptive feedback control (AFC) is not used.
24	ISET	**LED current set.** Connect an external resistor from ISET to GND to set the average LED current (I_{LED}). I_{LED} for each channel (mA) = 600 / R_{ISET} (kΩ). If the ISET pin is shorted to ground or an open condition is detected, the device latches off and asserts the /FS pin.
25	DATA-	**Differential interface (negative).**
26	DATA+	**Differential interface (positive).**
27	ADDR2	**Address setting.** Configure the device's address by connecting this pin to VCC/GND or to GND with a 35kΩ resistor (with ±10% range). For more details, see the Device Address section on page 27.
28	ADDR1	**Address setting.** Configure the device's address by connecting this pin to VCC/GND or to GND with a 35kΩ resistor (with ±10% range). For more details, see the Device Address section on page 27.
29	/FS	**Failsafe output.** The /FS pin is an active-low, open-drain output. /FS pulls low if any of the following occur: LED short, LED open, thermal shutdown, ISET pin open, or ISET pin short. The /FS pin can support a continuous connection to VBIAS or VCC through a pull-up resistor. Float this pin if it is not used.
30	EN	**Enable input.** Pull EN above 2.2V to enable the part; pull EN below 0.8V to shut down the part. The EN pin can be pulled directly to VBIAS through a resistor.
31	VBIAS	**Bias supply.** The MPQ7225A operates from a 2.5V to 18V input rail. A capacitor (C_{IN}) is required, and must be placed close to VBIAS to decouple the input rail.
32	MODE	**Mode selection.** The MODE pin is the master/slave mode selection pin. Tie MODE to GND to configure the device in master mode, or tie MODE to VCC to configure the device in slave mode. If AFC is not used, connect all devices' MODE pins to GND.
-	Exposed pad	**Exposure thermal pad.** The exposed pad has no internal electrical connection to GND. Connect the exposed pad to the external GND plane on the board for optimal thermal performance.

ABSOLUTE MAXIMUM RATINGS (1)

V_{VBIAS}	-0.3V to +20V
V_{LEDx}	-0.3V to +20V
FBO, EN, /FS	-0.3V to +20V
DATA+, DATA-	-0.3V to +18V
All other pins	-0.3V to +4V
Continuous power dissipation (T_A = 25°C) (2) (6)	
QFN-32 (5mmx6mm)	5.9W
Junction temperature (T_J)	150°C
Lead temperature	260°C
Storage temperature	-65°C to +150°C

ESD Ratings

Human body model (HBM)	Class 2 (3)
Charged-device model (CDM)	Class C2b (4)

Recommended Operating Conditions

VCC (if externally supplied)	3.2V to 3.5V
VBIAS voltage (V_{VBIAS})	2.5V to 18V
LED current (I_{LED})	200mA/ch
Operating junction temperature (T_J)	-40°C to +150°C

Thermal Resistance	***θ_{JA}***	***θ_{JC}***	
QFN-32 (5mmx6mm)			
JESD51-7	23.8	1.4	°C/W (5)
EVQ7225A-QJ-00A	21.2	0.93	°C/W(6)

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) Per AEC-Q100-002.
4) Per AEC-Q100-011.
5) Measured on a JESD51-7, 4-layer PCB. The values given in this table are only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application. The value of θ_{JC} shows the thermal resistance from junction-to-case bottom.
6) Measured on a standard EVB for the MPQ7225A: 83.5mmx83.5mm size, 4-layer PCB, 2oz. The value of θ_{JC} shows the thermal resistance from junction-to-case top.

ELECTRICAL CHARACTERISTICS

V_{BIAS} = 6.5V, T_J = -40°C to +150°C, typical values are at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply Voltage						
BIAS supply current	I_{BIAS}	Disabled, EN pin is low (shutdown)		0.5	2.5	µA
		Enabled, no LED load (EN pin is high, EN_ANA bit = 0, quiescent current [I_Q]), VCC supplied externally, V_{BIAS} = 6.5V		0.6	1	mA
		Enabled, no LED load (EN pin is high, EN_ANA bit = 0, I_Q), VCC supplied externally, V_{BIAS} = 14V		1.4	2.1	mA
		Enabled, no LED load (EN pin is high, EN_ANA bit = 0, I_Q), VCC supplied internally, V_{BIAS} = 6.5V		7	12	mA
		Enabled, no LED load (EN pin is high, EN_ANA bit = 0, I_Q), VCC supplied internally, V_{BIAS} = 14V		8	13	mA
VBIAS under-voltage lockout (UVLO) threshold	V_{BIAS_UVLO}	Rising edge		1.8		V
		Falling edge		1.6		V
VCC supply current	I_{CC}	Only required if VCC is supplied externally Disabled, EN pin is low (shutdown), V_{CC} = 3.5V		0.05	60	µA
		V_{CC} = 3.5V, enabled, no LED load (EN pin is high, I_Q)		6.5	13	mA
		V_{CC} = 3.5V, 16 LED channels are enabled (EN pin is high, EN_ANA bit = 1, PWM = 100%, R_{ISET} = 6.04kΩ, I_{LED} = 100mA)		12	20	mA
Internal VCC regulator voltage	V_{CC}	I_{VCC} = 0mA	3.1	3.3	3.5	V
VCC supply UVLO threshold	V_{CC_UVLO}	Rising edge	2.8	3	3.2	V
		Falling edge	2.6	2.8	3.0	V
EN threshold	V_{EN_R}	V_{EN} - V_{GND}	2.2			V
	V_{EN_F}	V_{EN} - V_{GND}			0.8	V
LED Current						
LED current (channel output to ideal current error)	I_{LED}	R_{ISET} = 3.01kΩ, T_J = 25°C	194.35	199.34	204.32	mA
		R_{ISET} = 3.01kΩ, T_J = -40°C to +150°C	189.37	199.34	209.3	mA
		R_{ISET} = 6.04kΩ, T_J = 25°C	96.85	99.34	101.82	mA
		R_{ISET} = 6.04kΩ, T_J = -40°C to +150°C	94.37	99.34	104.3	mA
LEDx current sink headroom voltage	V_{LEDx}	I_{LED} = 200mA		300	400	mV
		I_{LED} = 100mA		150	250	
		I_{LED} = 50mA		75	125	
ISET voltage	V_{ISET}	R_{ISET} = 3.01kΩ (or I_{ISET} = 200µA)	0.57	0.60	0.63	V

ELECTRICAL CHARACTERISTICS *(continued)*

V_{BIAS} = 6.5V, T_J = -40°C to +150°C, typical values are at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Channel output leakage current	I_{LKG}	PWM = 0% (single channel), T_J = -40°C to +150°C			2	μA
		PWM = 0% (all 16 channels), T_J = -40°C to +150°C			32	μA
Channel-to-channel current error	I_{EER_CC}	I_{ERR_CC} = (I_{OUTI} - I_{AVE}) / I_{AVE} x 100%, 100mA, 200mA	-5%		+5%	
Dimming						
PWM frequency	f_{PWM}	Default setting	225	250	275	Hz
PWM frequency range		Configuration range	250		1000	Hz
PWM duty slew rate	t_{PWM}	12-bit resolution, f_{PWM} = 250Hz	0.8	1	1.2	μs
Phase shift delay	t_{DELAY}	PHASE_SHIFT[1:0] = 11	16	20	24	μs
LED current slew rate in PWM dimming		SLEW_RATE[1:0] = 01, rising edge, R_{ISET} = 6.04kΩ	2	5	10	μs
		SLEW_RATE[1:0] = 11, rising edge, R_{ISET} = 6.04kΩ	8	20	32	μs
Protection (Selectable Latch or Hiccup Mode)						
Short LED string protection threshold	V_{LED_S}	LED_SHORT_THR[1:0] = 00	1.8	2.1	2.3	V
Short LED string protection time	t_{LED_S}	V_{LEDx} > V_{LED_S}	3.6	4	4.4	ms
Open LED string protection threshold	V_{LED_O}	LED on, real-time monitoring (cover pin short-to-GND)	50	100	150	mV
Open LED string protection time	t_{LED_O}	V_{LEDx} < V_{LED_O} (100mV)	3.6	4	4.4	ms
ISET current threshold for pin short (/FS, latch)	I_{ISET_STH}		0.7	1	1.3	mA
ISET current threshold for pin open (/FS, latch)	I_{ISET_OTH}		2	4.5	7	μA
Thermal warning threshold (7)	T_{WARN}		135	150	165	°C
Thermal warning hysteresis (7)	T_{WARN_HYS}			20		°C
Thermal shutdown threshold (7)	T_{SD}		155	170	185	°C
Thermal shutdown hysteresis (7)	T_{SD_HYS}			20		°C
/FS (Open Drain)						
Failsafe low output level	V_{FS_OL}	I_{FS_OL} = 2mA, active	0.15	0.33	0.5	V
Failsafe input current leakage	I_{FS_LKG}	Inactive			1	μA
Failsafe assert deglitch time	t_{FS-TD}		5	20	40	μs

DIGITAL INTERFACE CHARACTERISTICS

V_{BIAS} = 6.5V, T_J = -40°C to +150°C, typical values are at T_J = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Driver						
Bus output voltage (recessive)	$V_{O(R)}$	R_L = 180Ω	1.15	1.65	2.15	V
Bus output voltage (DATA+) (dominant)	$V_{O(D+)}$	R_L = 180Ω, see Figure 1 on page 9	2.35	2.55	2.85	V
Bus output voltage (DATA-) (dominant)	$V_{O(D-)}$	R_L = 180Ω, see Figure 1 on page 9	0.5	0.85	1.15	V
Differential output voltage (dominant)	$V_{OD(D)}$	R_L = 180Ω, V_{CC} = 3.3V	1.4	1.7	2.35	V
Output symmetry (dominant or recessive)	V_{SYM}	V_{CC} = 3.3V, $V_{O(DATA+)}$ + $V_{O(DATA-)}$	2.97	3.4	3.63	V
Differential output rising time (7)	t_R	R_L = 180Ω, C_L = 50pF, V_{CC} = 3.3V, see Figure 2 on page 9	2	5	15	ns
Differential output falling time (7)	t_F	R_L = 180Ω, C_L = 50pF, V_{CC} = 3.3V, see Figure 2 on page 9	20	25	35	ns
Propagation delay time (low-to-high level) (7)	$t_{P(L2H)D}$	R_L = 180Ω, C_L = 50pF, V_{CC} = 3.3V, see Figure 2 on page 9	2	7	15	ns
Propagation delay time (high-to-low level) (7)	$t_{P(H2L)D}$	R_L = 180Ω, C_L = 50pF, V_{CC} = 3.3V, see Figure 2 on page 9	10	22	40	ns
Receiver						
Input resistance (DATA+/-)	R_{IN}	V_{CC} = 3.3V, R_{IN} = △V(DATA+) / △I(DATA+)	14	30	58	kΩ
Differential threshold voltage for RX going negative	V_{RXTH-}	V_{CC} = 3.3V	0.7	1.1	1.5	V
Differential threshold voltage for RX going positive	V_{RXTH+}	V_{CC} = 3.3V	0.3	0.7	1.1	V
Propagation delay time (low-to-high level) (7)	$t_{P(L2H)R}$	R_L = 180Ω, C_L = 50pF, V_{CC} = 3.3V, see Figure 3 on page 9	3	13	30	ns
Propagation delay time (high-to-low level) (7)	$t_{P(H2L)R}$	R_L = 180Ω, C_L = 50pF, V_{CC} = 3.3V, see Figure 3 on page 9	5	18	35	ns
Input capacitance to ground (7)	C_{IN}			20		pF

Notes:

7) Not tested in production. Guaranteed by design and characterization.

TIMING DIAGRAMS

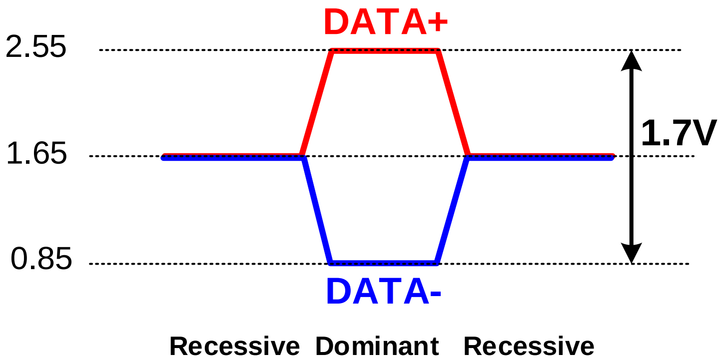


Figure 1: Differential Interface Timing

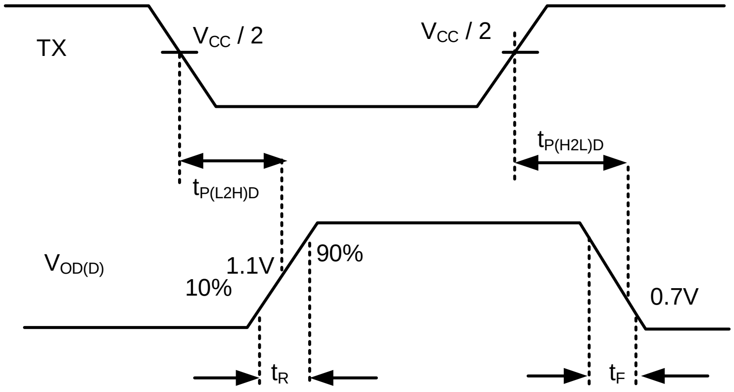


Figure 2: Driver Interface Timing

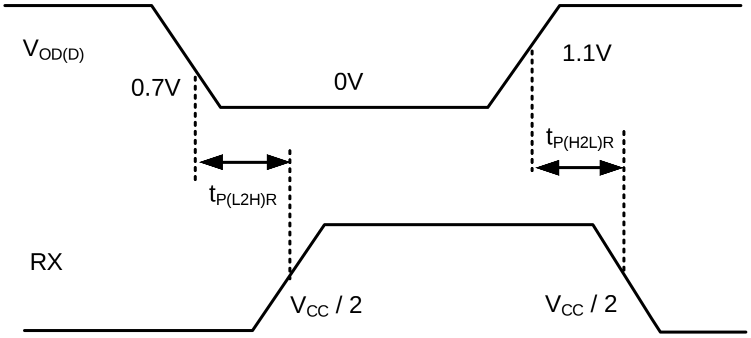
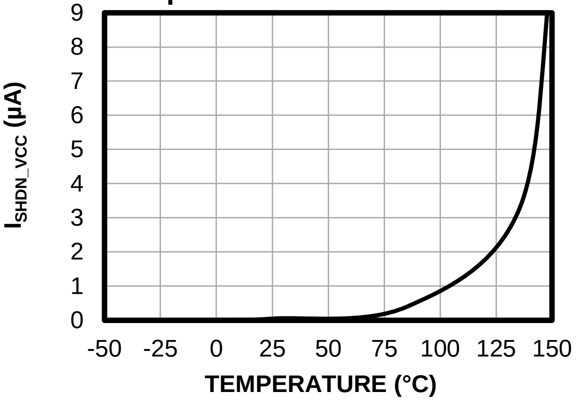


Figure 3: Receiver Interface Timing

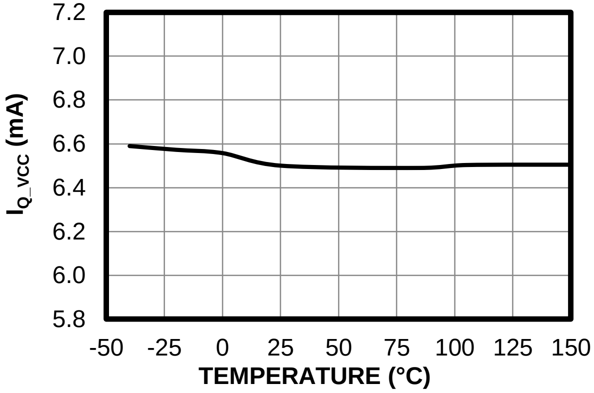
TYPICAL CHARACTERISTICS

V_{BIAS} = 6.5V, T_J = -40°C to +150°C, unless otherwise noted.

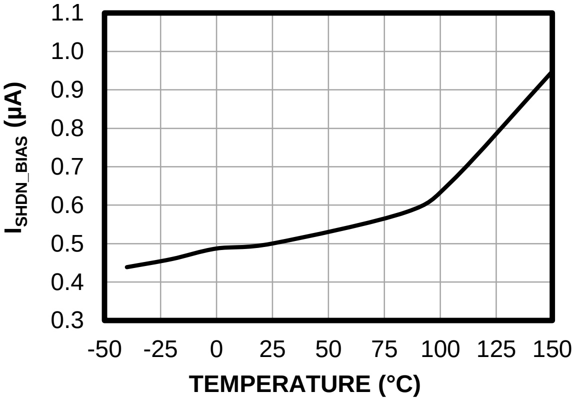
VCC Shutdown Current vs. Temperature



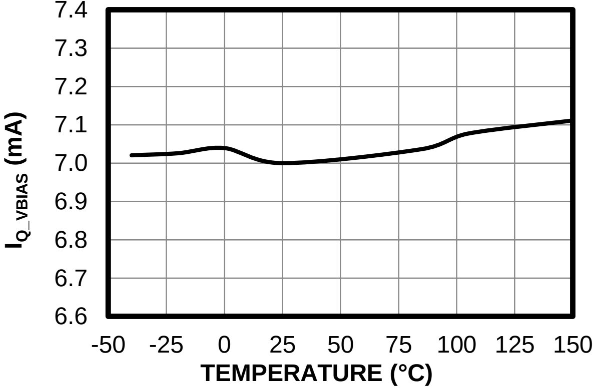
VCC Quiescent Current vs. Temperature



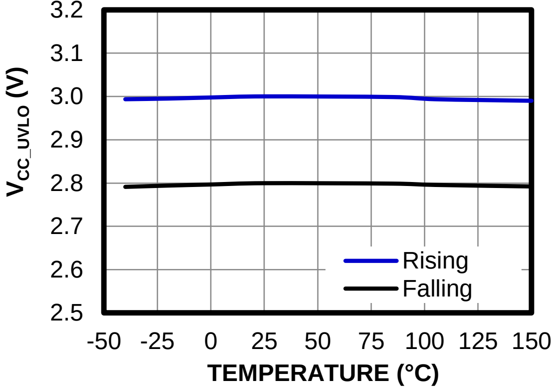
VBIAS Shutdown Current vs. Temperature



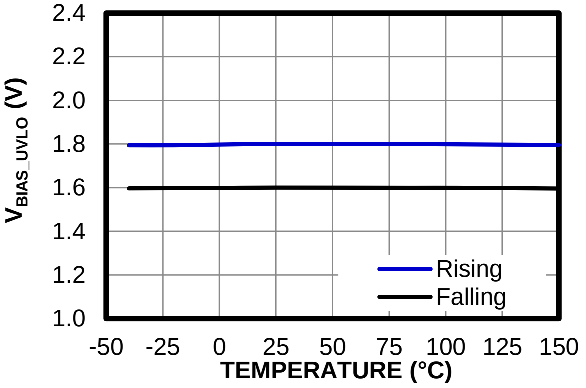
VBIAS Quiescent Current vs. Temperature



V_{CC} UVLO Threshold vs. Temperature



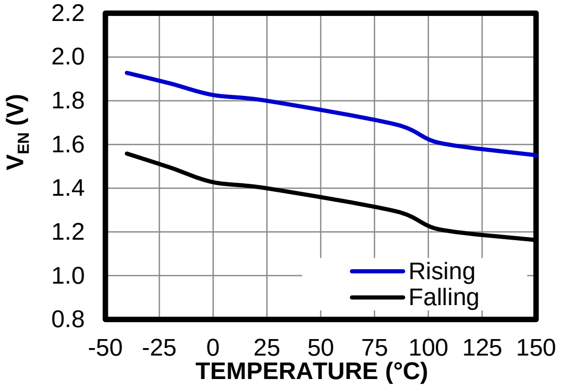
VBIAS UVLO Threshold vs. Temperature



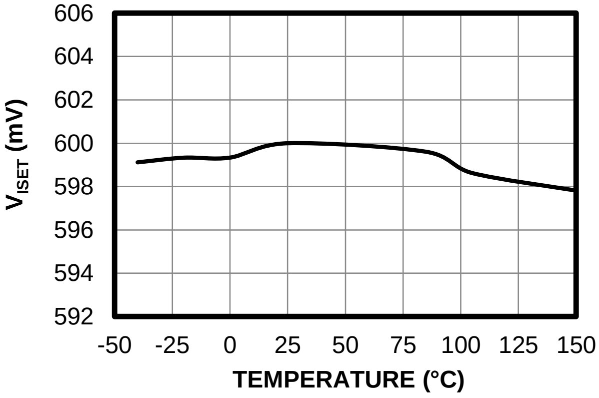
TYPICAL CHARACTERISTICS *(continued)*

V_{BIAS} = 6.5V, T_J = -40°C to +150°C, unless otherwise noted.

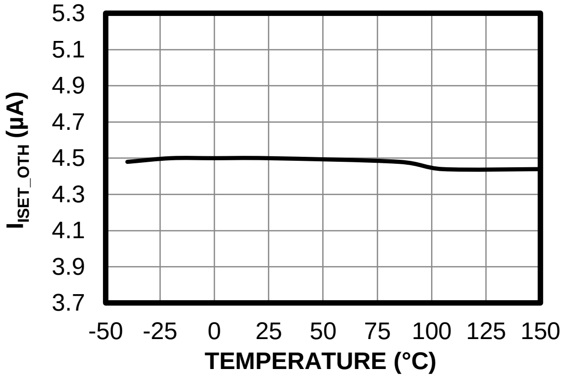
EN UVLO Threshold vs. Temperature



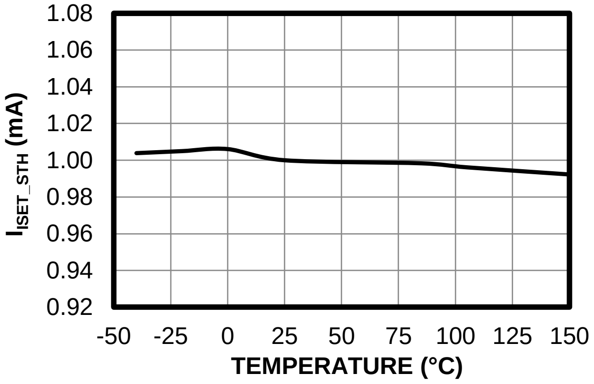
ISET Voltage vs. Temperature



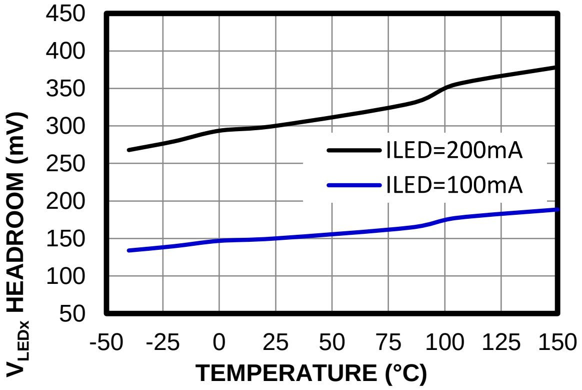
ISET Open Threshold vs. Temperature



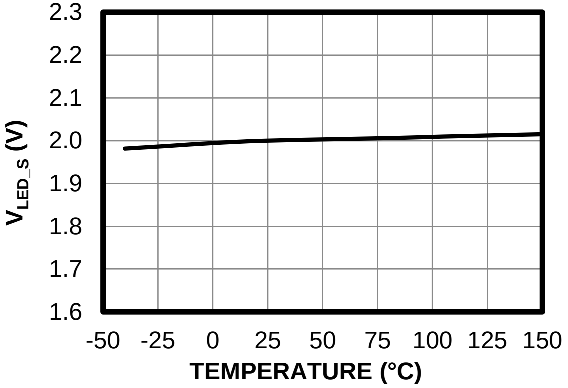
ISET Short Threshold vs. Temperature



V_{LEDx} Headroom vs. Temperature

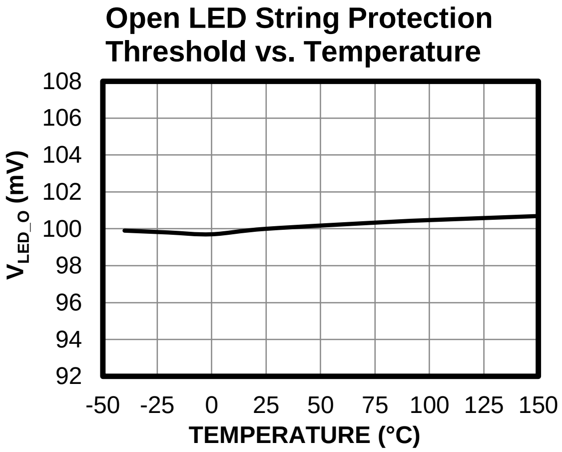


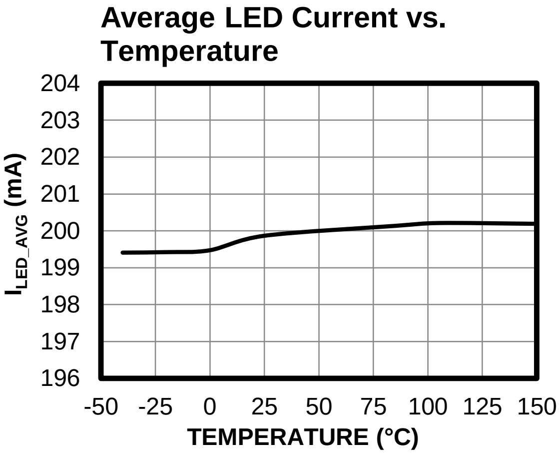
Short LED String Protection Threshold vs. Temperature



TYPICAL CHARACTERISTICS *(continued)*

V_{BIAS} = 6.5V, T_J = -40°C to +150°C, unless otherwise noted.



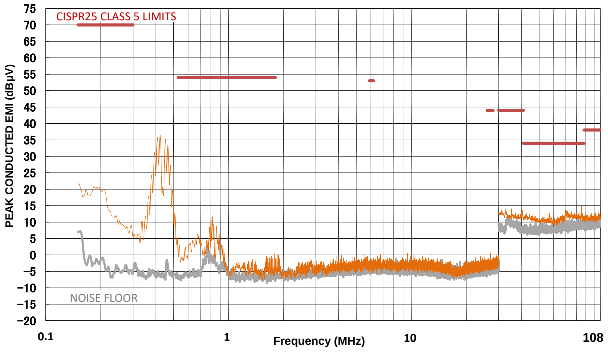


TYPICAL PERFORMANCE CHARACTERISTICS

2 LEDs in series (V_{LED} = 6V), I_{LED}/channel = 200mA, T_A = 25°C, unless otherwise noted. (8)

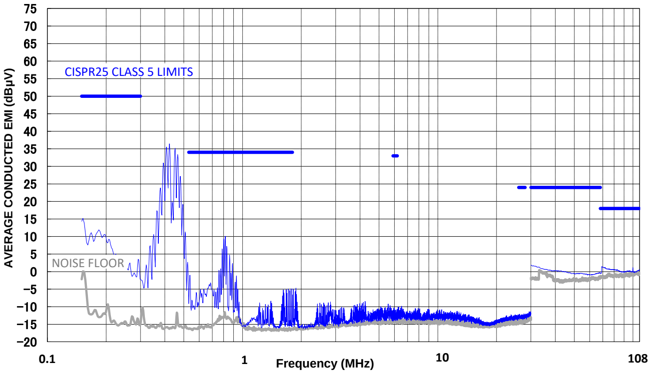
CISPR25 Class 5 Peak Conducted Emissions

150kHz to 108MHz



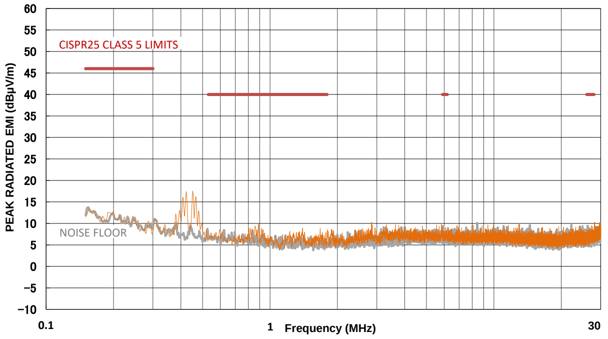
CISPR25 Class 5 Average Conducted Emissions

150kHz to 108MHz



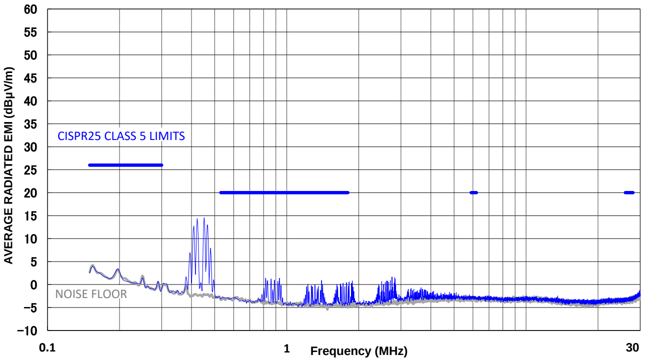
CISPR25 Class 5 Peak Radiated Emissions

150kHz to 30MHz



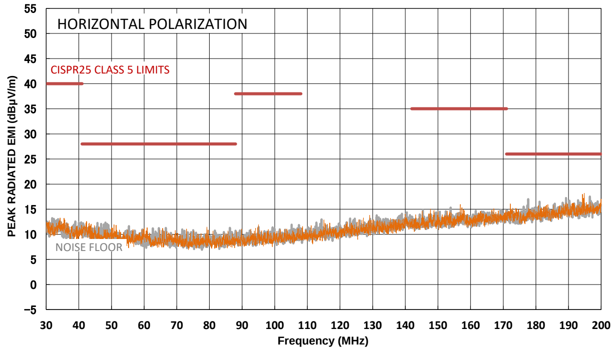
CISPR25 Class 5 Average Radiated Emissions

150kHz to 30MHz



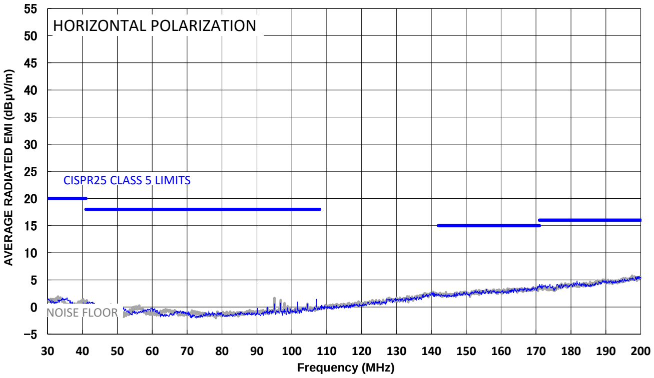
CISPR25 Class 5 Peak Radiated Emissions

Horizontal, 30MHz to 200MHz



CISPR25 Class 5 Average Radiated Emissions

Horizontal, 30MHz to 200MHz

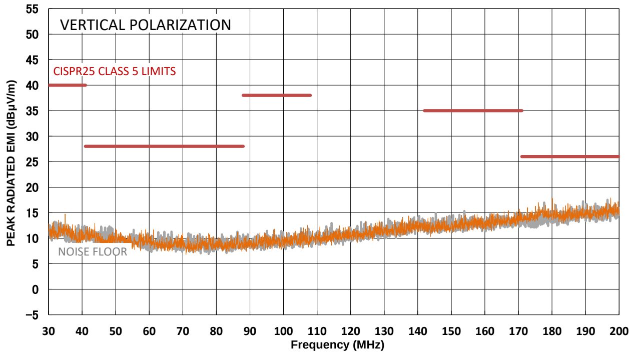


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

2 LEDs in series (V_{LED} = 6V), I_{LED}/channel = 200mA, T_A = 25°C, unless otherwise noted. (8)

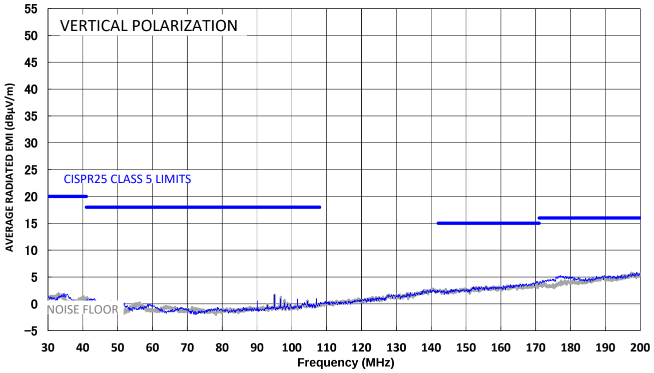
CISPR25 Class 5 Peak Radiated Emissions

Vertical, 30MHz to 200MHz



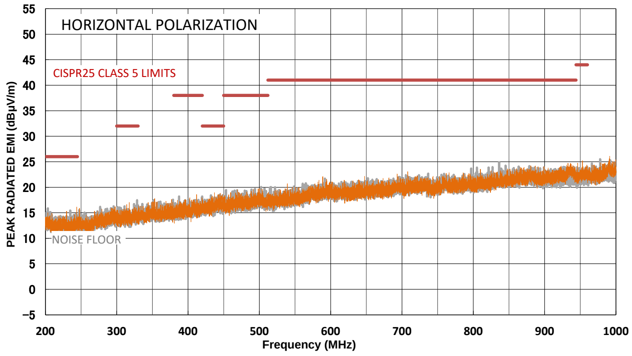
CISPR25 Class 5 Average Radiated Emissions

Vertical, 30MHz to 200MHz



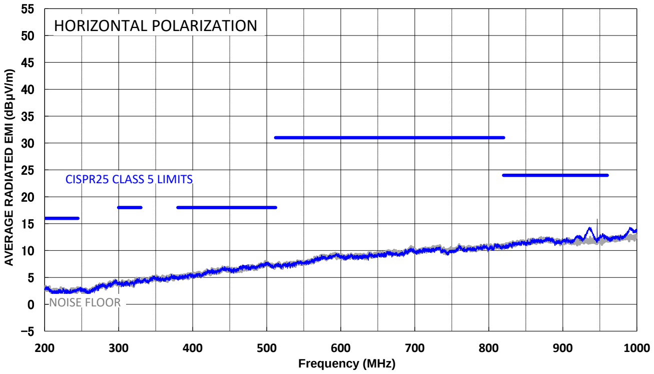
CISPR25 Class 5 Peak Radiated Emissions

Horizontal, 200MHz to 1GHz



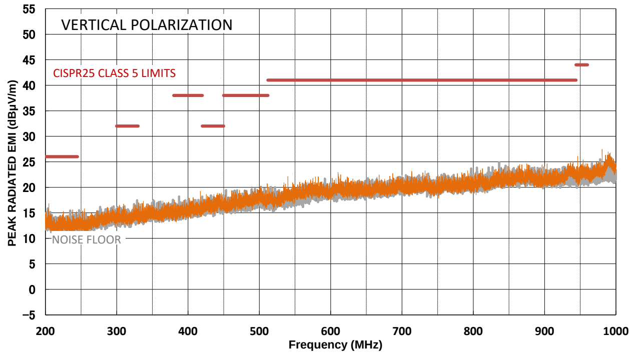
CISPR25 Class 5 Average Radiated Emissions

Horizontal, 200MHz to 1GHz



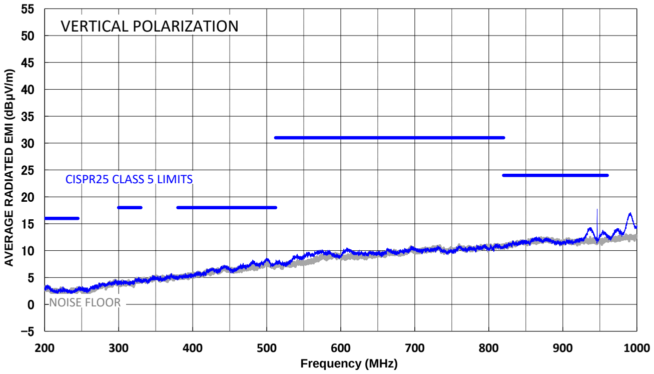
CISPR25 Class 5 Peak Radiated Emissions

Vertical, 200MHz to 1GHz



CISPR25 Class 5 Average Radiated Emissions

Vertical, 200MHz to 1GHz



Notes:

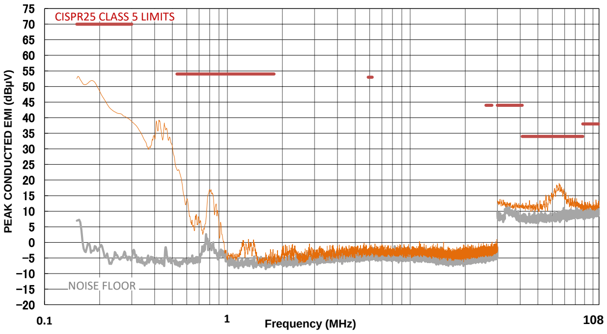
8) The EMC test results are based on the typical application circuit with EMI filters (see Figure 23 on page 44).

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

2 LEDs in series (V_{LED} = 6V), I_{LED}/channel = 200mA, T_A = 25°C, unless otherwise noted. (9)

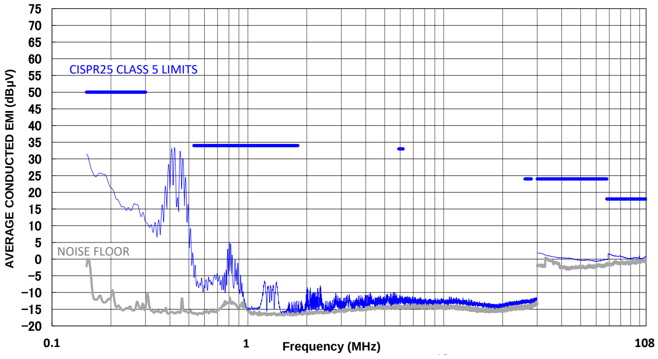
CISPR25 Class 5 Peak Conducted Emissions

150kHz to 108MHz



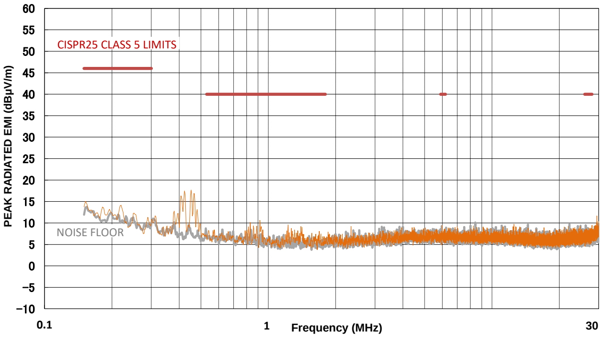
CISPR25 Class 5 Average Conducted Emissions

150kHz to 108MHz



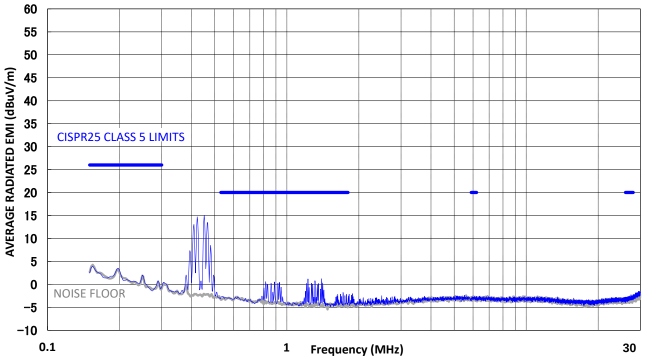
CISPR25 Class 5 Peak Radiated Emissions

150kHz to 30MHz



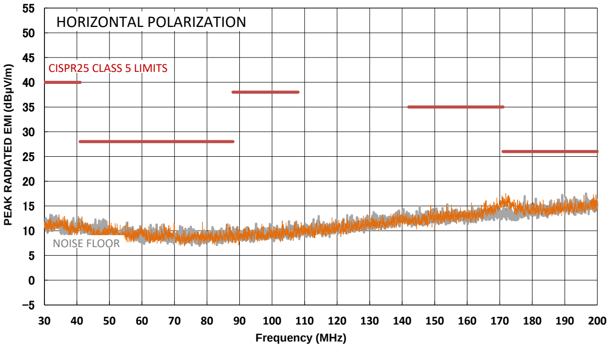
CISPR25 Class 5 Average Radiated Emissions

150kHz to 30MHz



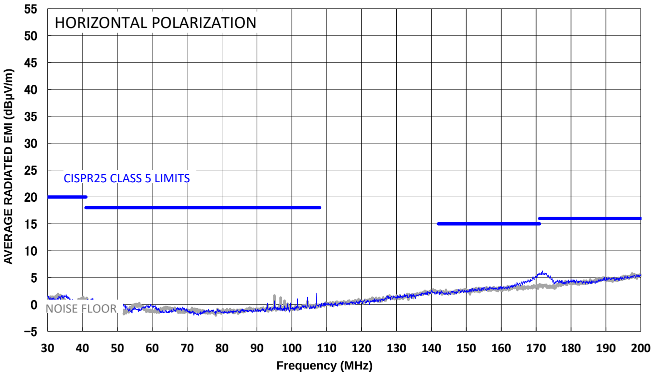
CISPR25 Class 5 Peak Radiated Emissions

Horizontal, 30MHz to 200MHz



CISPR25 Class 5 Average Radiated Emissions

Horizontal, 30MHz to 200MHz

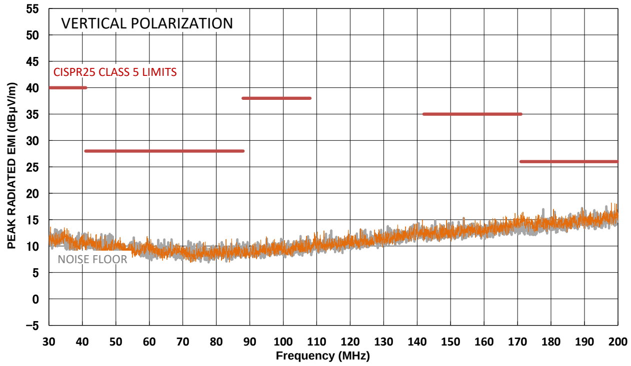


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

2 LEDs in series (V_{LED} = 6V), I_{LED}/channel = 200mA, T_A = 25°C, unless otherwise noted. (9)

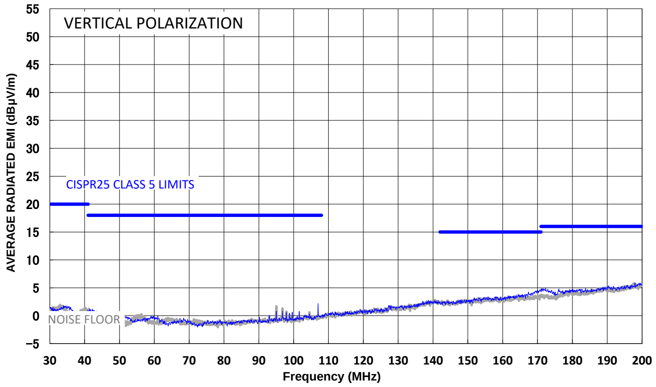
CISPR25 Class 5 Peak Radiated Emissions

Vertical, 30MHz to 200MHz



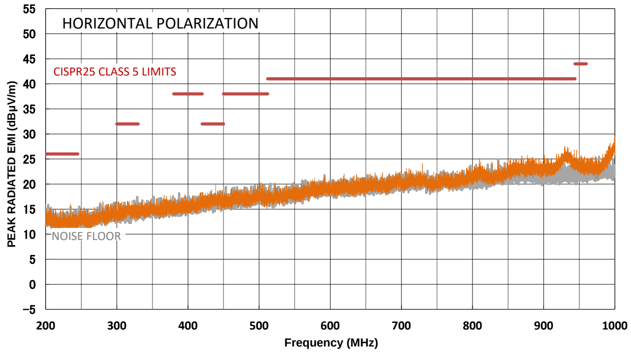
CISPR25 Class 5 Average Radiated Emissions

Vertical, 30MHz to 200MHz



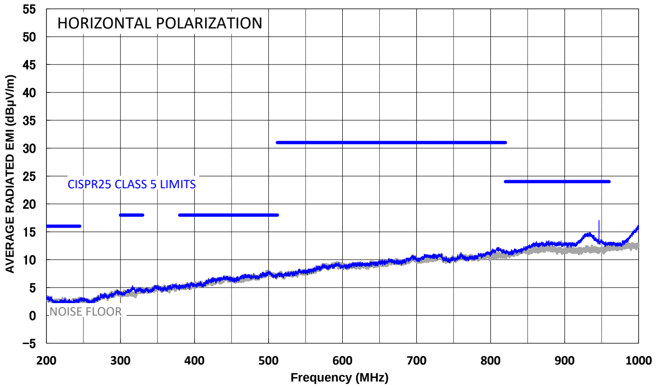
CISPR25 Class 5 Peak Radiated Emissions

Horizontal, 200MHz to 1GHz



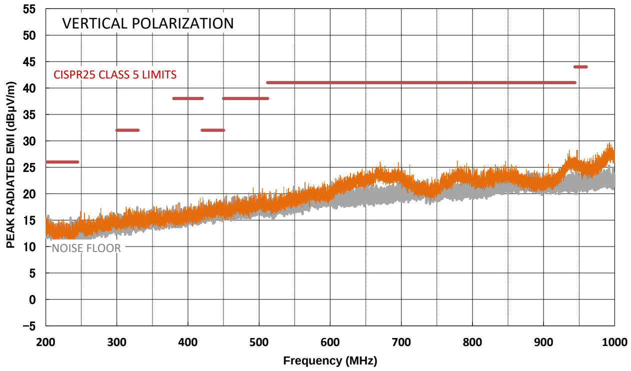
CISPR25 Class 5 Average Radiated Emissions

Horizontal, 200MHz to 1GHz



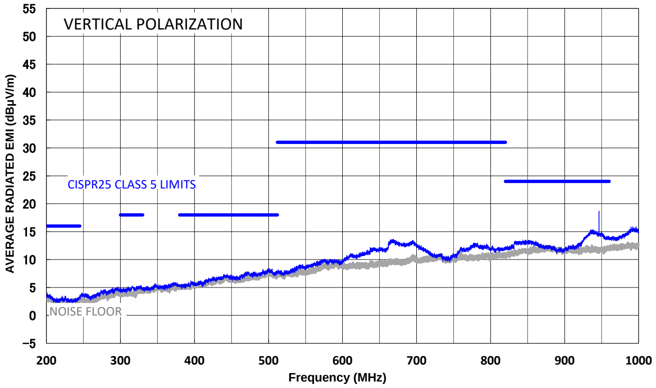
CISPR25 Class 5 Peak Radiated Emissions

Vertical, 200MHz to 1GHz



CISPR25 Class 5 Average Radiated Emissions

Vertical, 200MHz to 1GHz



Notes:

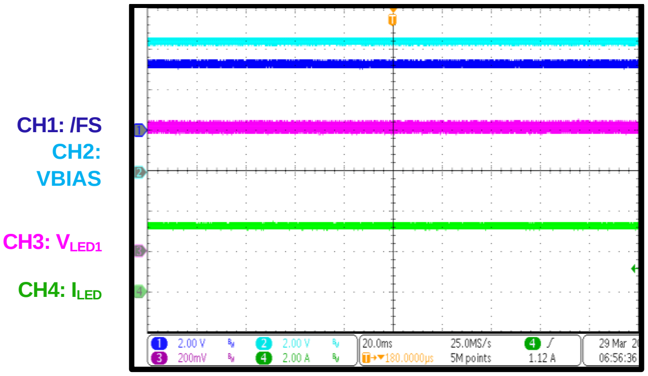
9) The EMC test results are based on the typical application circuit with EMI filters (see Figure 23 on page 44). The configurations are as follows: f_{PWM} = 250Hz, duty cycle = 50%, phase shift = 1µs, slew rate = 5µs.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

2 LEDs in series (V_{LED} = 6V), I_{LED}/channel = 200mA, T_A = 25°C, unless otherwise noted.

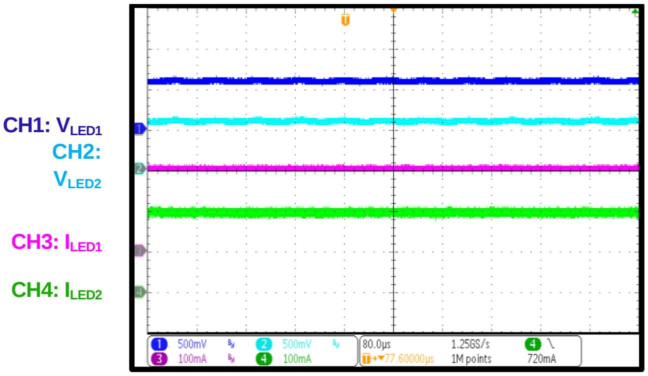
Steady State

2 LEDs in series (V_{LED} = 6V), I_{LED} = 0.2A/ch



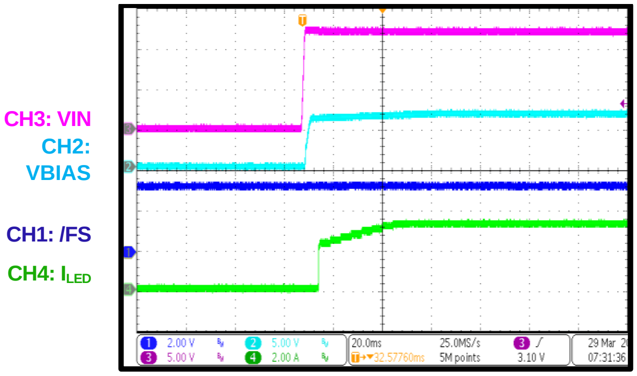
Steady State

2 LEDs in series (V_{LED} = 6V), I_{LED} = 0.2A/ch



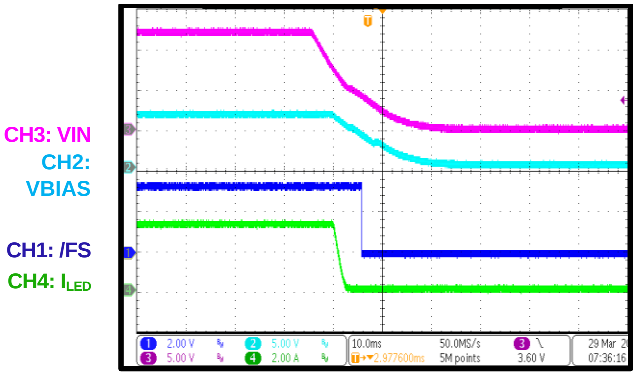
Pre-Buck Start-Up

MPQ7225A EN on to MPQ7225A VCC on to buck VIN on



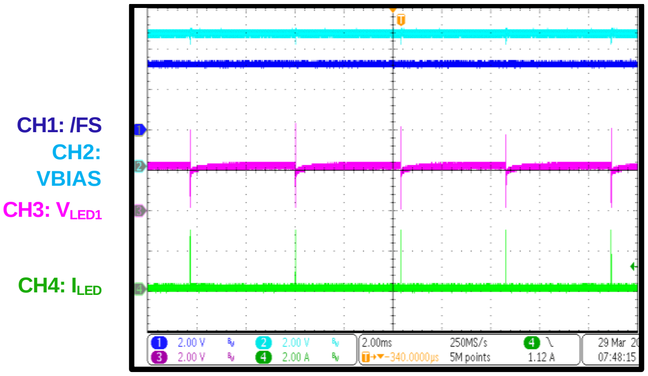
Pre-Buck Shutdown

MPQ7225A EN off to MPQ7225A VCC off to buck VIN off



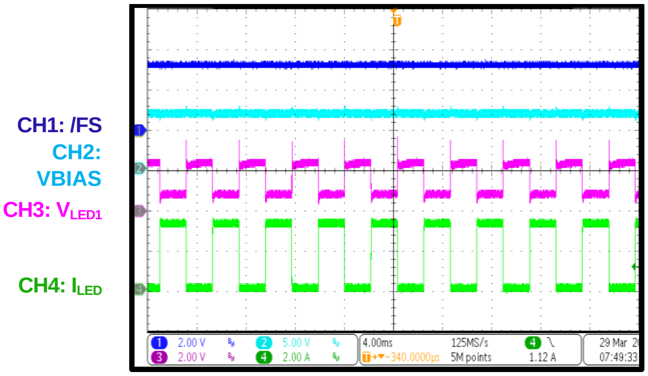
PWM Dimming

f_{PWM} = 250Hz, duty cycle = 0.2%



PWM Dimming

f_{PWM} = 250Hz, duty cycle = 50%

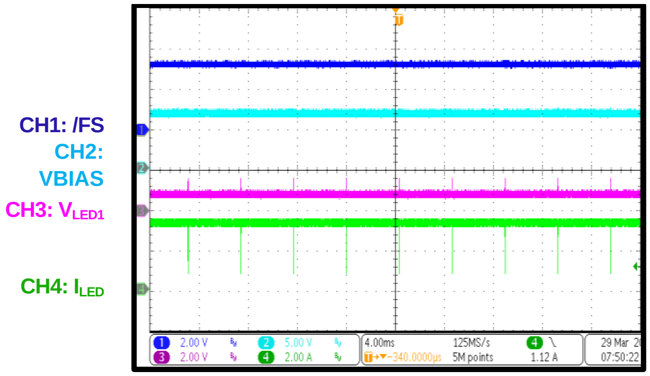


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

2 LEDs in series (V_{LED} = 6V), I_{LED}/channel = 200mA, T_A = 25°C, unless otherwise noted.

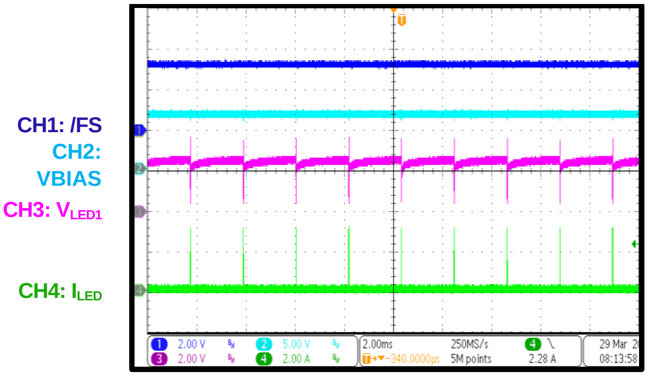
PWM Dimming

f_{PWM} = 250Hz, duty cycle = 99.9%



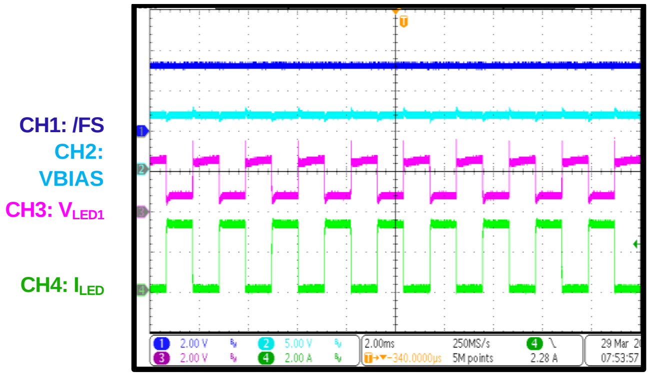
PWM Dimming

f_{PWM} = 500Hz, duty cycle = 0.3%



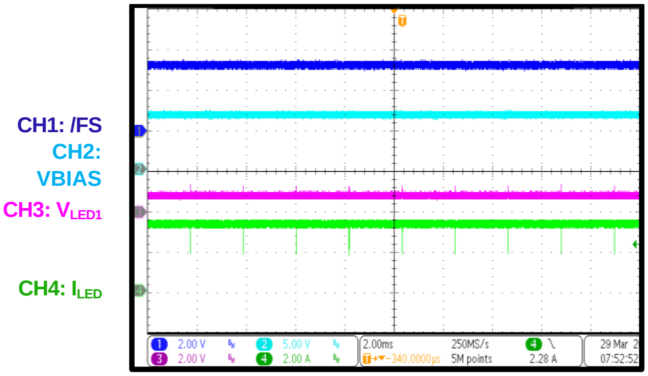
PWM Dimming

f_{PWM} = 500Hz, duty cycle = 50%



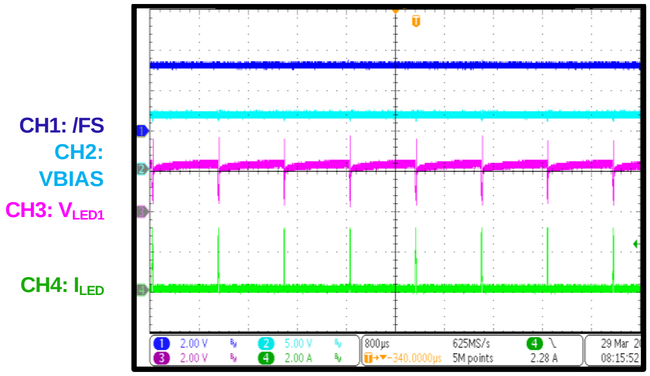
PWM Dimming

f_{PWM} = 500Hz, duty cycle = 99.9%



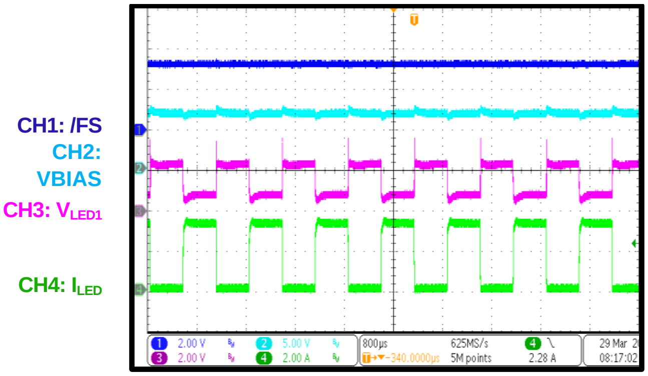
PWM Dimming

f_{PWM} = 1kHz, duty cycle = 0.5%



PWM Dimming

f_{PWM} = 1kHz, duty cycle = 50%

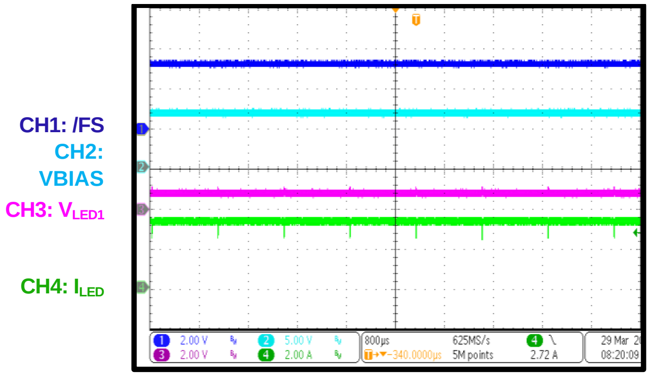


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

2 LEDs in series (V_{LED} = 6V), I_{LED}/channel = 200mA, T_A = 25°C, unless otherwise noted.

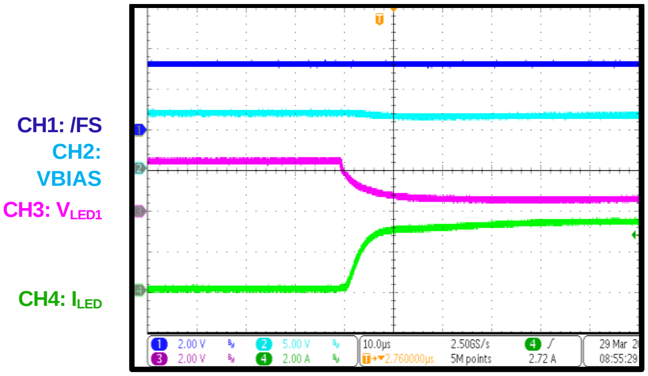
PWM Dimming

f_{PWM} = 1kHz, duty cycle = 99.9%



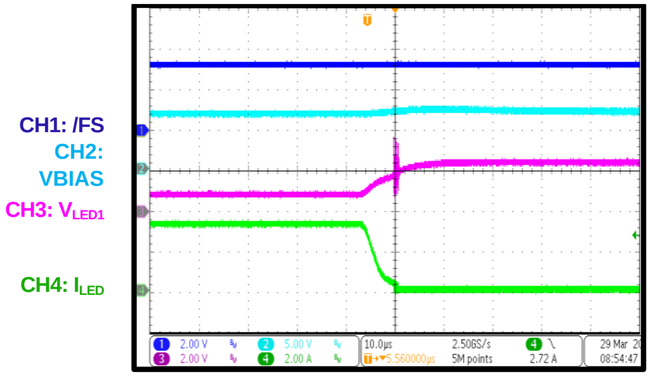
PWM Dimming Slew Rate

f_{PWM} = 1kHz, slew rate = 5µs



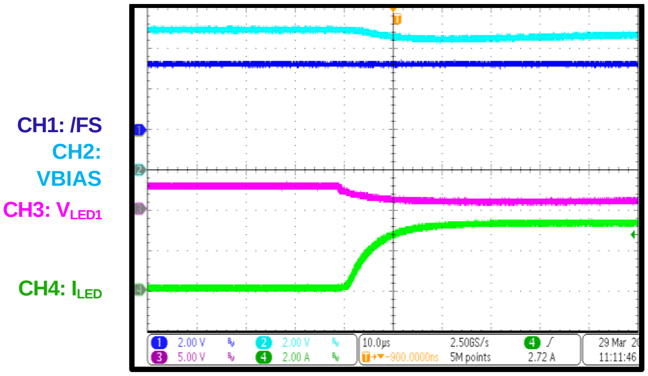
PWM Dimming Slew Rate

f_{PWM} = 1kHz, slew rate = 5µs



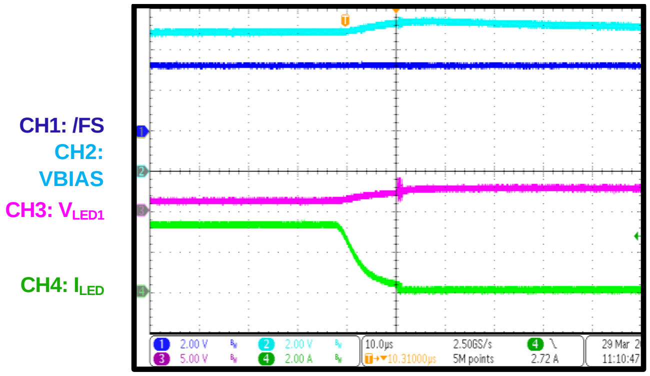
PWM Dimming Slew Rate

f_{PWM} = 1kHz, slew rate = 10µs



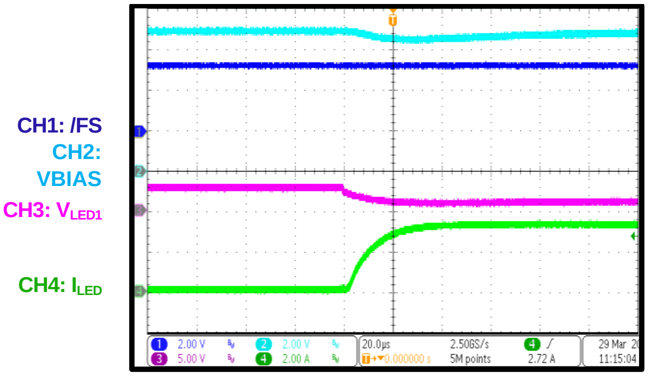
PWM Dimming Slew Rate

f_{PWM} = 1kHz, slew rate = 10µs



PWM Dimming Slew Rate

f_{PWM} = 1kHz, slew rate = 20µs

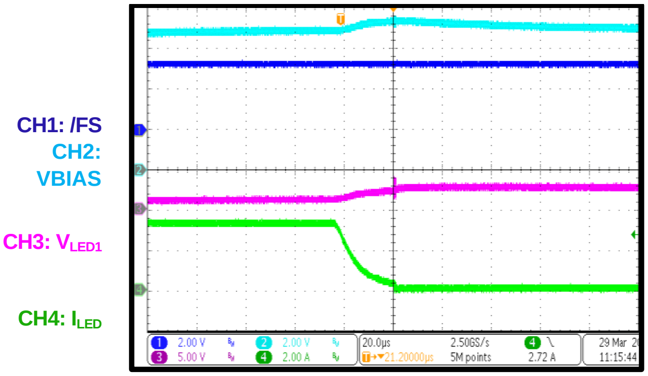


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

2 LEDs in series (V_{LED} = 6V), I_{LED}/channel = 200mA, T_A = 25°C, unless otherwise noted.

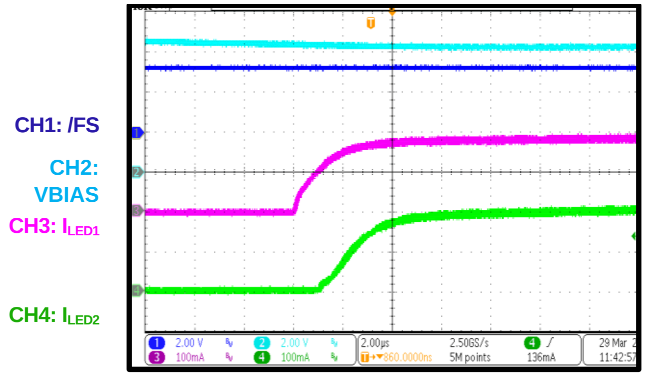
PWM Dimming Slew Rate

f_{PWM} = 1kHz, slew rate = 20µs



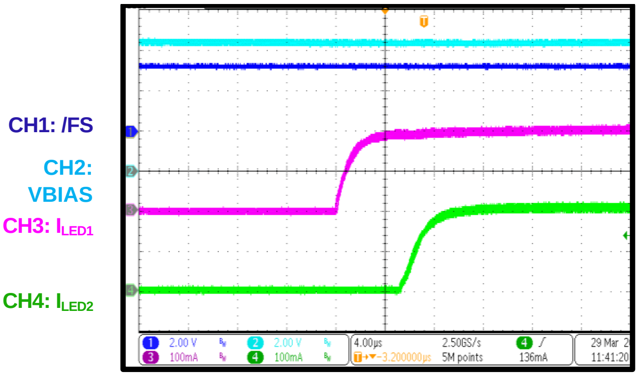
PWM Dimming Phase Shift

No slew rate, phase shift = 1µs



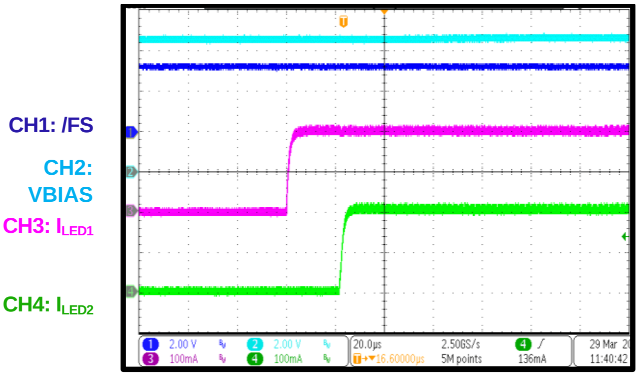
PWM Dimming Phase Shift

No slew rate, phase shift = 5µs



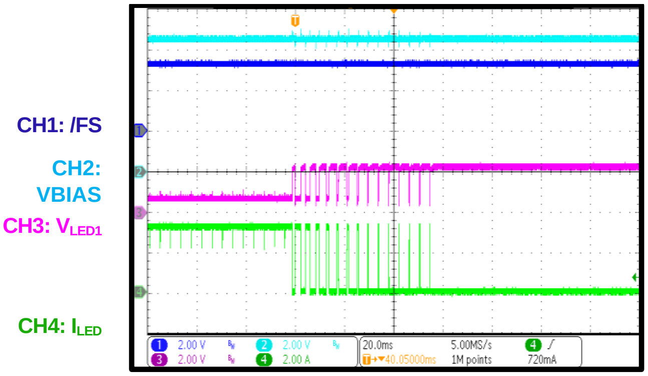
PWM Dimming Phase Shift

No slew rate, phase shift = 20µs



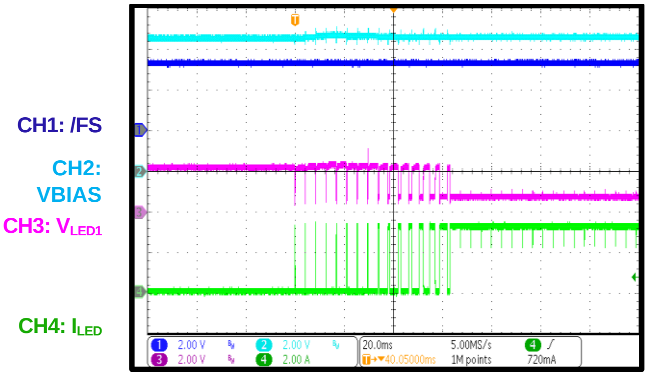
PWM Dimming to Auto-Dimming

f_{PWM} = 250Hz, normal speed,
duty cycle = 0% to 99.9%



PWM Dimming to Auto-Dimming

f_{PWM} = 250Hz, normal speed,
duty cycle = 99.9% to 0%

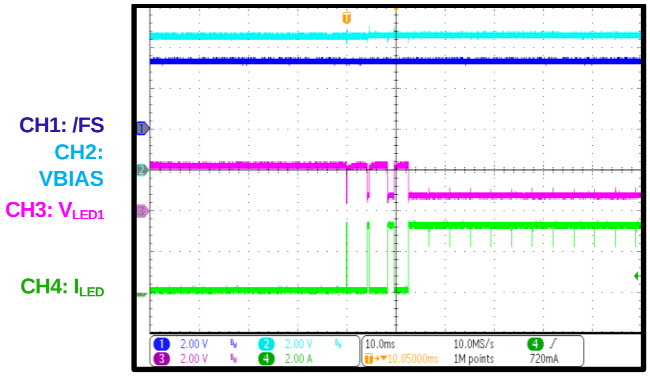


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

2 LEDs in series (V_{LED} = 6V), I_{LED}/channel = 200mA, T_A = 25°C, unless otherwise noted.

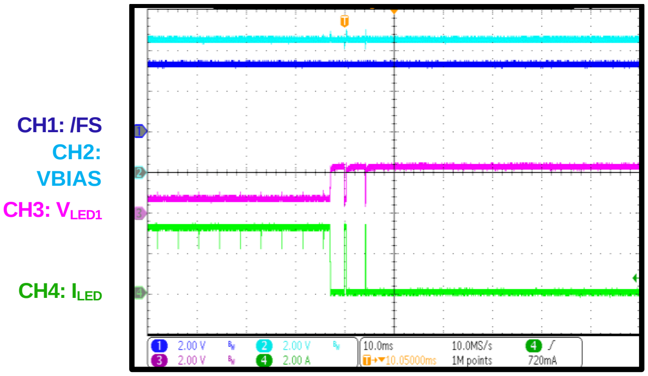
PWM Dimming to Auto-Dimming

f_{PWM} = 250Hz, 4 times normal speed,
duty cycle = 0% to 99.9%



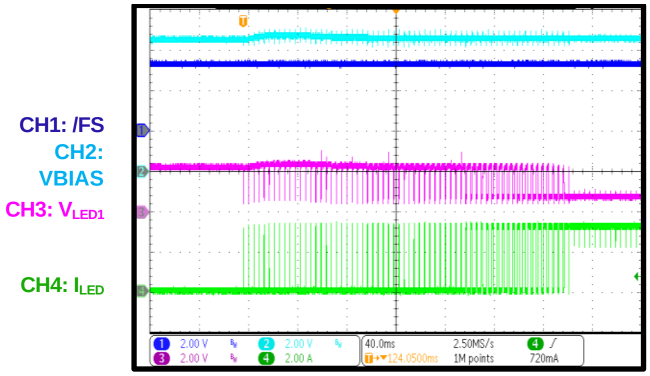
PWM Dimming to Auto-Dimming

f_{PWM} = 250Hz, 4 times normal speed,
duty cycle = 99.9% to 0%



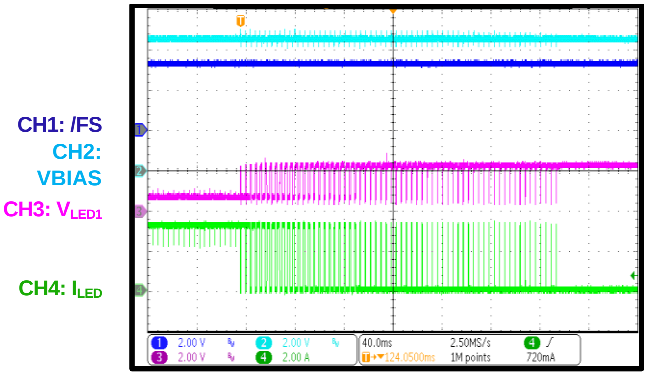
PWM Dimming to Auto-Dimming

f_{PWM} = 250Hz, 1/4 normal speed,
duty cycle = 0% to 99.9%

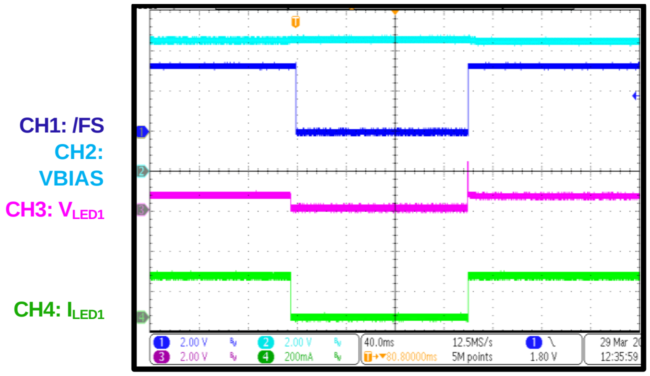


PWM Dimming to Auto-Dimming

f_{PWM} = 250Hz, 1/4 normal speed,
duty cycle = 99.9% to 0%

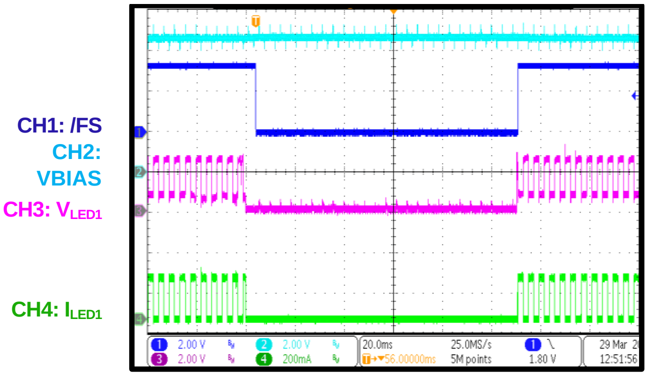


LED Open Entry/Recovery with /FS Non-Latch



LED Open Entry/Recovery with /FS Non-Latch

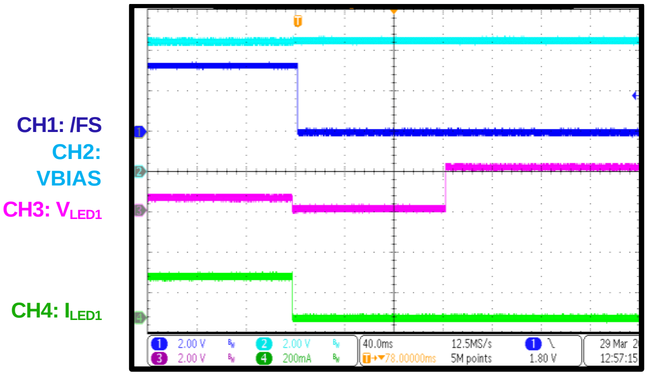
f_{PWM} = 250Hz, duty cycle = 50%



TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

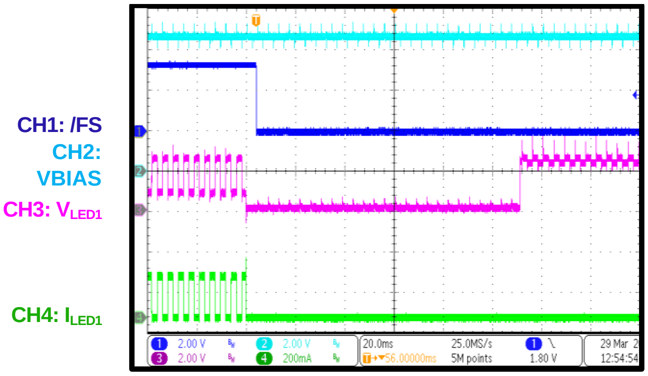
2 LEDs in series (V_{LED} = 6V), I_{LED}/channel = 200mA, T_A = 25°C, unless otherwise noted.

LED Open Entry/Recovery with /FS Latch

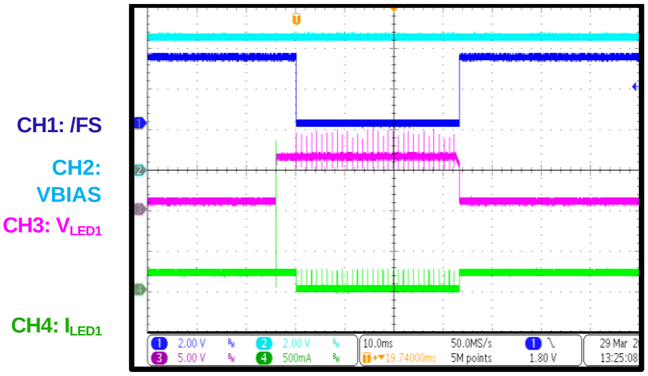


LED Open Entry/Recovery with /FS Latch

f_{PWM} = 250Hz, duty cycle = 50%

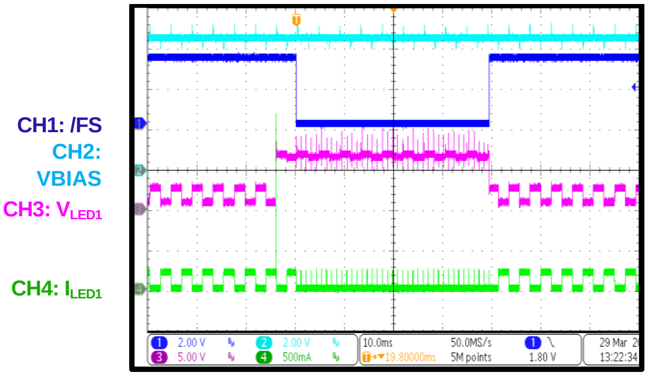


LED Short Entry/Recovery with /FS Non-Latch

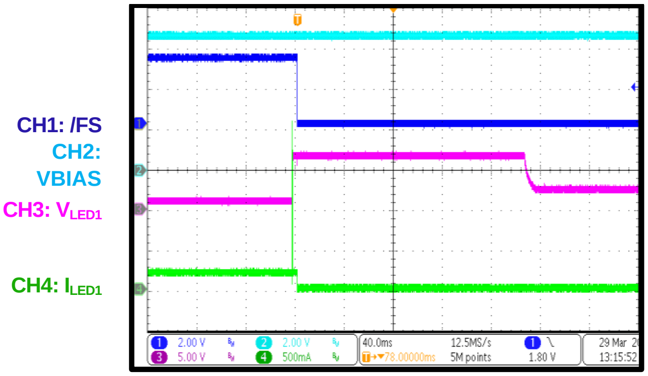


LED Short Entry/Recovery with /FS Non-Latch

f_{PWM} = 250Hz, duty cycle = 50%

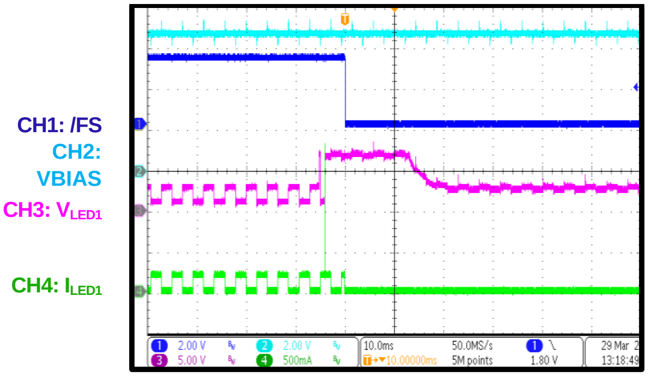


LED Short Entry/Recovery with /FS Latch



LED Short Entry/Recovery with /FS Latch

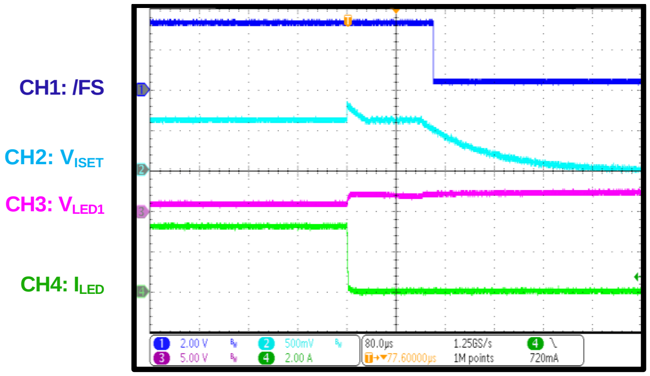
f_{PWM} = 250Hz, duty cycle = 50%



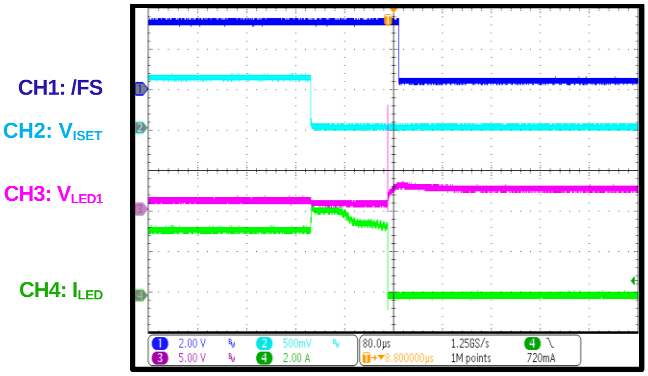
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

2 LEDs in series (V_{LED} = 6V), I_{LED}/channel = 200mA, T_A = 25°C, unless otherwise noted.

ISET Pin Open Protection



ISET Pin Short Protection



FUNCTIONAL BLOCK DIAGRAM

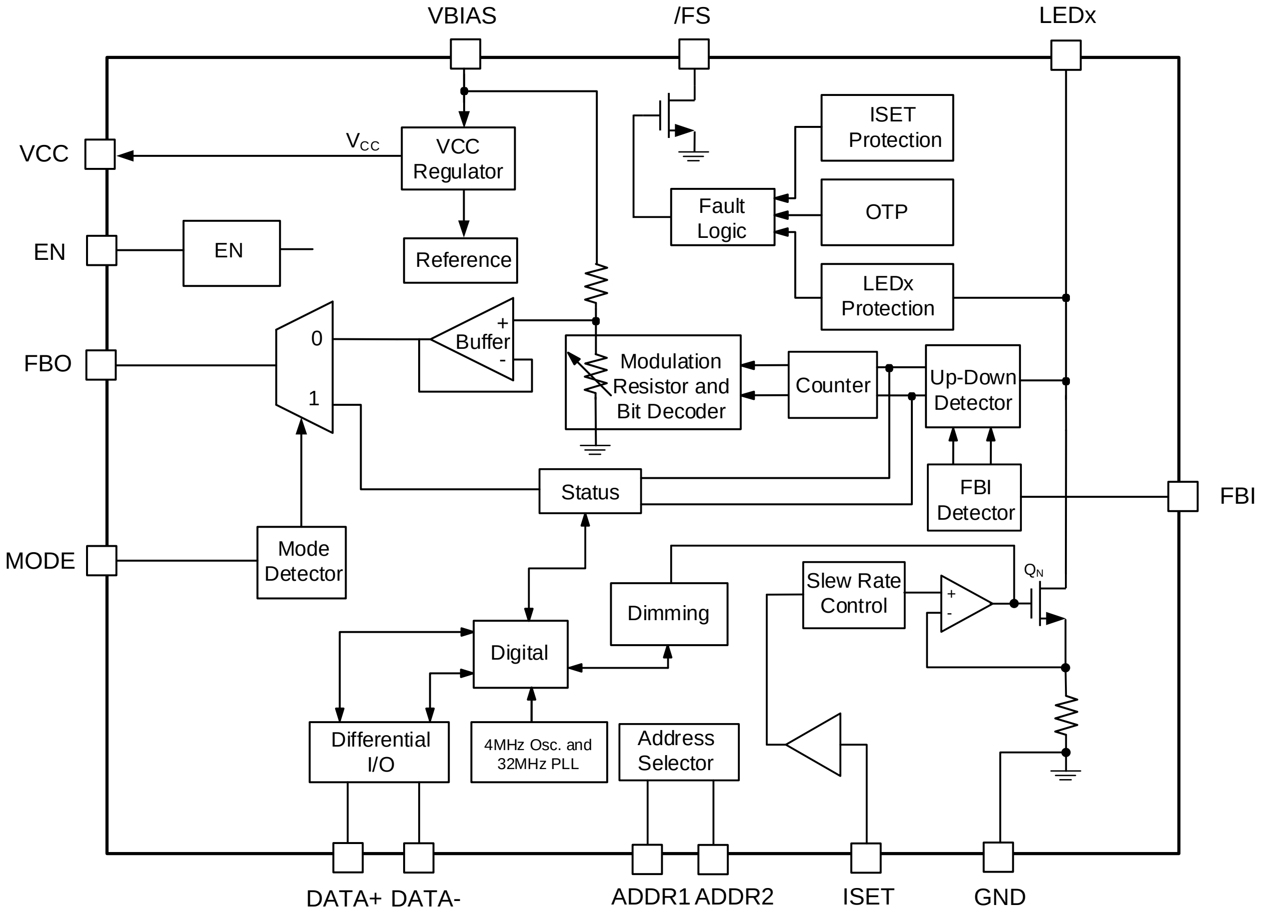


Figure 4: Functional Block Diagram

OPERATION

LED Current Sinks

The current sink regulators (16 channels) embedded in the MPQ7225A can be individually configured to provide up to 200mA of current for each channel. These 16 specialized current sinks are accurate to within ±5% for currents at 200mA across the full temperature range, with a string-to-string difference of ±5%.

Pre-Regulator Adaptive Feedback Control (AFC)

The MPQ7225A features adaptive feedback control (AFC) for the external pre-regulator. The output voltage of the pre-regulator (e.g. the buck) is always self-adjusted based on the LED string with the lowest headroom voltage. This minimizes the LEDx pin voltage (V_{LEDx}) and maintains the target LED current (I_{LED}) for the 16 channels. Overall efficiency is maximized when the MPQ7225A's current sinks operate with the minimum headroom voltage.

The number of used LED outputs is automatically detected, and only the active LED outputs are monitored for AFC. If any LED strings are not used, they can be disabled via the one-time programmable (OTP) memory using CHx_EN (0x03).

V_{LEDx} is periodically monitored by the control loop. If any of the LED outputs fall below the low-band threshold (0.45V), the external pre-regulator's output voltage increases. If all LED outputs exceed the high-band threshold (0.55V), the external pre-regulator's output decreases.

V_{LEDx} should remain between the low band and high band. The band can be configured via register 0x27 based on I_{LED}. The high-band voltage can be set between 0.25V and 0.6V, while the low-band voltage can be set between 0.2V and 0.55V. If 150mA < I_{LED} ≤ 200mA, it is recommended to set the overall band between 0.45V and 0.55V. If I_{LED} ≤ 150mA, it is recommended to set the overall band between 0.3V and 0.4V to improve efficiency.

The initial VBIAS voltage (V_{BIAS}) can also be configured via the OTP. The internal divider resistor (R1 and R2) defines both the minimum and maximum adaptive V_{BIAS} levels (see Figure 7 on page 26).

Choose the maximum V_{BIAS} based on the maximum LED string voltage specification. Before the LED drivers are active, the initial pre-regulator output voltage exceeds the maximum LED string voltage by about 0.3V.

One of the MPQ7225A's key benefits is that its dropout information can be transferred to the DC/DC converter's feedback pin via the FBO pin to optimize system efficiency in real time. This information sharing is also available between multiple MPQ7225A devices via the FBI and FBO pins. The channel with the lowest V_{LEDx} uses its V_{LEDx} to determine the DC/DC converter's power supply output. AFC also works if multiple MPQ7225A devices are connected in parallel.

Figure 5 shows the thermal image when V_{BIAS} is set with AFC.

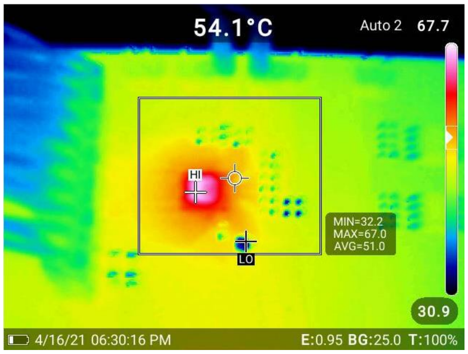


Figure 5: V_{BIAS} with AFC

Figure 6 shows the thermal image when V_{BIAS} has a fixed voltage (V_{LEDx} = 1V) without AFC.

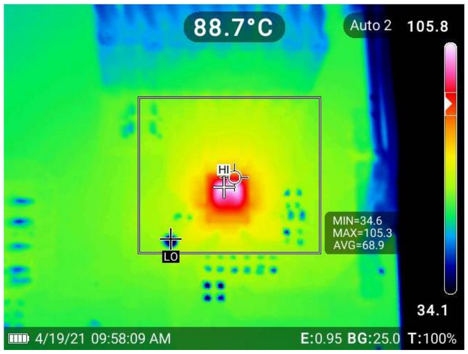


Figure 6: V_{BIAS} without AFC

AFC improves thermal performance and efficiency. When I_{LED} = 200mA, the temperature deviation is about 38.3°C.

If AFC is not used, float the MPQ7225A's FBO and MODE pins, and connect the FBI pin to GND.

Multiple Devices

The MPQ7225A can also support several devices in parallel by setting the part to master mode or slave mode through the MODE pin. If the MODE pin is connected to GND, the part is configured as the master. The slave device's FBO pin should be connected to the master device's FBI pin. If the MODE pin is connected to VCC, the part is configured as a slave device. The master device's FBO pin is connected to the pre-regulator's FB resistor divider (see Figure 7). Only the master device can directly adjust V_{BIAS}; the slave device can only deliver the V_{BIAS} information to master device through the FBI pin.

For the master device, the FBI pin voltage (V_{FBI}) and V_{LEDx} determine how to adjust V_{BIAS}. If the high band is set to 0.55V and the low band is set to 0.45V, and 0.75V < V_{FBI} < 1.2V (or any of the master devices' V_{LEDx} < 0.45V), then the chip decreases R2. This decreases the FBO voltage (V_{FBO}), which regulates V_{BIAS} to be high via the pre-regulator. If V_{FBI} < 0.3V and all the masters' V_{LEDx} > 0.55V, then the chip increases R2. This increases V_{FBO}, which regulates V_{BIAS} be to low via the pre-regulator. For other conditions, V_{BIAS} is maintained as normal.

Refer to the FBI detector. When 0.75V < V_{FBI} < 1.2V, UP_S = 1, and DOWN_S = 0, this means that V_{BIAS} is not sufficient for the slave device, so V_{BIAS} must be increased for the slave device. When V_{FBI} < 0.3V, DOWN_S = 1, and UP_S = 0, this means that V_{BIAS} is too high for the slave device, so V_{BIAS} must be decreased. When 0.3V < V_{FBI} < 0.75V, UP_S = 0, and DOWN_S = 0, this means that V_{BIAS} must stay the same for the slave device.

For any slave device, if V_{LEDx} < 0.45V, or 0.75 < V_{FBI} < 1.2V, then V_{FBO} = 1V (V_{BIAS} is not sufficient; increase V_{BIAS} for the slave device). If all V_{LEDx} > 0.55V and V_{FBI} < 0.3V, then V_{FBO} = 0V (V_{BIAS} is too high; decrease V_{BIAS} for the slave device); for other conditions, V_{FBO} = 0.5V (maintain V_{BIAS} for the slave device).

In summary, if V_{LEDx} < 0.45V, then V_{BIAS} increases; does V_{BIAS} decreases only when each V_{LEDx} > 0.55V. For other conditions, V_{BIAS} stays the same. Table 1 summarizes these relationships.

Table 1: Relationship between FBI, FBO, V_{BIAS}, and V_{LEDx}

Slave Device			
Condition	Any V_{LEDx} < 0.45 or 0.75 < V_{FBI} < 1.2V	All V_{LEDx} > 0.55V and V_{FBI} < 0.3V	Other condition
V_{FBO}	1V	0V	0.5V
Master Device			
Condition	Any V_{LEDx} < 0.45 or 0.75 < V_{FBI} < 1.2V	All V_{LEDx} > 0.55V and V_{FBI} < 0.3V	Other condition
V_{FBO}	Decreases	Increases	Stays the same
V_{BIAS}	Increases	Decreases	Stays the same

Figure 7 shows how to set up master and slave modes for the MPQ7225A.

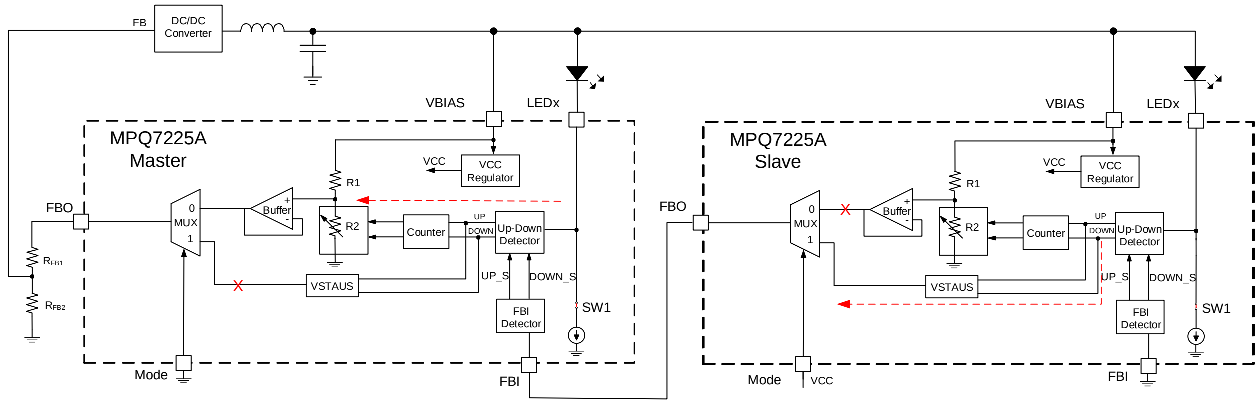


Figure 7: Master and Slave Mode Set-Up

Device Address

The device address is configured via ADDR1, ADDR2, and the SADDR_PAGE bit. A total of 16 different addresses can be configured (see Table 2).

Table 2: Address Setting

ADDR2	ADDR1	SADDR_PAGE	Bits[3:0]
Connect to VCC	Connect to VCC	0	0000
Connect to VCC	Connect R = 35kΩ to GND	0	0001
Connect to VCC	Connect to GND	0	0010
Connect R = 35kΩ to GND	Connect to VCC	0	0011
Connect R = 35kΩ to GND	Connect R = 35kΩ to GND	0	0100
Connect R = 35kΩ to GND	Connect to GND	0	0101
Connect to GND	Connect to VCC	0	0110
Connect to GND	Connect R = 35kΩ to GND	0	0111
Connect to GND	Connect to GND	0	1000
Connect to GND	Connect to GND	1	1000
Connect to VCC	Connect to VCC	1	1000
Connect to VCC	Connect R = 35kΩ to GND	1	1001
Connect to VCC	Connect to GND	1	1010
Connect R = 35kΩ to GND	Connect to VCC	1	1011
Connect R = 35kΩ to GND	Connect R = 35kΩ to GND	1	1100
Connect R = 35kΩ to GND	Connect to GND	1	1101
Connect to GND	Connect to VCC	1	1110
Connect to GND	Connect R = 35kΩ to GND	1	1111

At start-up, the IC checks the address first. Once the address is checked, the address is maintained during operation unless there is a power-on reset (POR). Note that the 35kΩ resistor must be within the ±10% range. If SADDR_PAGE is set to 0 via the OTP, the solution can support a maximum of 9 devices in one system. To use more than 9 devices, set SADDR_PAGE to 1.

Enable (EN) and Start-Up

The EN pin can connected to VBIAS through a resistor, or it can be controlled by the MCU's I/O pin. Pull EN above 2.2V to enable the part; pull EN below 0.8V to disable the part.

If using VBIAS to power VCC, V_{CC} does not rise until V_{BIAS} and EN are higher than UVLO. Then the internal logic circuits, including the differential interface, are active. The start-up sequence is as follows:

1. V_{BIAS} and EN pull high. Make sure the V_{BIAS} reach to the target value in 5ms.
2. V_{CC} exceeds its UVLO threshold.
3. The internal logic circuits are active and provide the output to the LEDs.

Each channel can be enabled or disabled individually by setting the corresponding ChxEN bit (register address: 0x03) to "disabled."

Figure 8 shows the start-up sequence. This sequence is described in greater detail below.

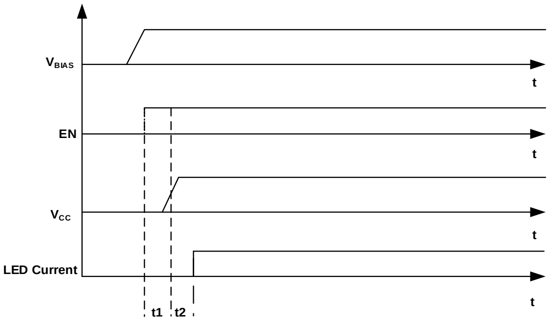


Figure 8: Start-Up Sequence

t1: The rising time from EN going high to $V_{CC} > V_{CC\_UVLO}$ is about 200µs, which is based on the 10µF VCC capacitor.

t2: The delay time from V_{CC} rising to when the internal logic is ready is about 5.5ms.

If V_{BIAS} < 3.5V, then another external LDO is required to power VCC. Set the external LDO voltage to 3.3V, with a current ability > (n20mA + 50mA), where *n* is the number of MPQ7225A devices in the system.

If using a buck converter as the MPQ7225A's pre-regulator, the FBO pin must be connected to the pre-regulator's FB pin through a divider network. In this scenario, start-up should follow the sequence below:

1. Power the MPQ7225A's VCC pin with an external 3.3V LDO.
2. The MPQ7225A's EN pin goes high.
3. The pre-regulator starts up.

Figure 9 shows this start-up sequence. This sequence is described in greater detail below.

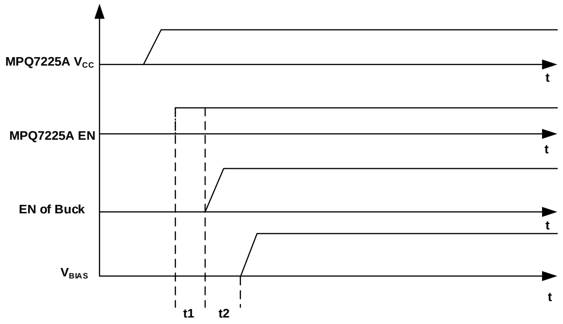


Figure 9: Start-Up Sequence

t1: The IC requires 500µs to load the OTP. It is recommended to wait longer than 500µs to initially start up the MPQ7225A or the buck converter.

t2: This time period is based on the buck's start-up delay.

If VBIAS is disconnected from the pre-regulator or the FBO pin is disconnected from the FB divider, then the pre-regulator works at a maximum duty cycle, and the pre-regulator's output voltage is regulated to its input voltage. Then all LEDx pins detect an LED short after 4ms, and all LEDx pins shut off.

If AFC is not used, then V_{BIAS} can be set to a fixed voltage. V_{BIAS} must exceed the maximum V_{LEDx} by at least 0.4V.

LED Current Setting

The LED currents of all channels are set by an external resistor at the ISET pin, calculated with Equation (1):

$$I_{LED}(mA) = \frac{600}{R_{ISET}(k\Omega)} \quad (1)$$

The nominal ISET voltage (V_{ISET}) is 0.6V. When the ISET current exceeds a specific value, it is detected as a pin short to ground. The ISET current threshold for short detection is 1mA (corresponding to a 0.6kΩ resistor, or a 1000mA I_{LED}). When the ISET current is below 5µA (corresponding to a 120kΩ resistor or 5mA I_{LED}), an ISET open condition is detected.

If an open or short condition is detected, the device latches off and asserts the /FS pin.

EMI Reduction

The MPQ7225A features three EMI reduction methods.

The first method requires configuring the LED current's rising/falling slew rates during pulse-width modulation (PWM) dimming, as this can sufficiently optimize EMI performance. The LED current rising/falling slew rates are controlled via register 0x01, bits[13:12]. The slew rates can be set to no slew rate, 5µs, 10µs, and 20µs. The default value is 5µs.

The second method requires configuring the LED current's phase-shift function. This function is controlled via register 0x01, bits[11:10]. When phase-shift is enabled, the channel x + 1 (where x = 1, 2...13) LED current phase shift is 1µs, 5µs, or 20µs after channel x's LED current rising edge.

The third EMI reduction method is frequency spread spectrum (FSS). FSS reduces EMI noise around the internal clock frequency and its harmonic frequencies. This method deliberately spreads the frequency of the clock waveform and widens the bandwidth of the switching waveform, which ultimately reduces its EMI spectral density. FSS modulates the internal clock frequency within ±10% from the central frequency, with a 15.6kHz modulation frequency (f_M) (see Figure 10). FSS can be disabled via register 0x01, bit[0].

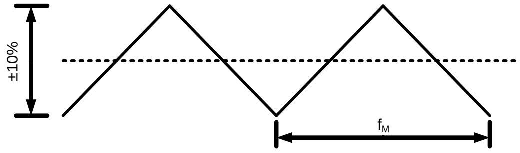


Figure 10: Frequency Spread Spectrum

Pulse-Width Modulation (PWM) Dimming

During PWM dimming, the LED current is chopped. This means that the LED current amplitude stays the same, while the LED current duty cycle varies with the PWM dimming register.

The PWM dimming duty cycle is set via PWM dimming registers 0x07~0x26, bits[11:0].

The duty cycle (D) can be estimated with Equation (2):

$$D = \frac{PWMx}{2^{12} - 1} = \frac{PWMx}{4095} \tag{2}$$

Where PWMx is the PWM dimming register for channel x (x = 1, 2...16).

When PWMx, bits[11:0] = 0x000, the corresponding LED channel current is 0. The PWM dimming frequency can be set via register 0x01, bits[9:8]. The dimming frequency can be set to 250Hz, 500Hz, or 1kHz. Ensure that the minimum dimming on time > 10µs.

The PWM dimming frequency and PWM dimming duty cycle can be changed on the fly.

Automatic Logarithmic Dimming

To reduce the burden on the communication bus, the MPQ7225A provides embedded, automatic logarithmic dimming based on a fixed 64-point lookup table. Assume there are a total of 64 steps between when the duty cycle = 1% and when the duty cycle = 100%. For a fixed constant (*k* = 1.075), the logarithmic curve can be fixed, so the duty cycle value for the 64 points can be calculated via software and solidified in digital circuitry. The duty cycle for Duty *x* is equal to (*k* x Duty (*x* - 1)), where *k* = 1.075 and the initial duty cycle is 1%.

Figure 11 shows the logarithmic dimming curve.

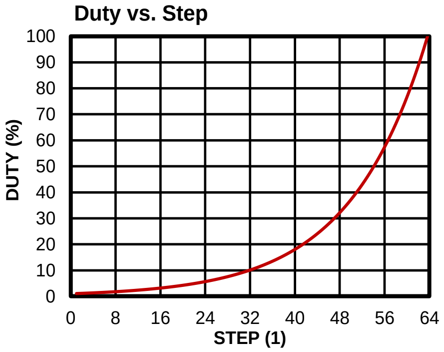


Figure 11: Logarithmic Dimming Curve

If the configurable cycle duty is not equal to the duty cycle on the curve, one more step is required to change the configured duty cycle.

The automatic logarithmic dimming speed can be set via register 0x02, bits[10:8]. The speed can be set to 4, 8, 16, 32, or 64 points, with a default of 16 points.

Figure 12 shows an example of the logarithmic dimming curve when the duty cycle changes. In this example, the duty cycle follows the sequence below:

- The duty cycle is configured from 0% to 80%
- The duty cycle is reduced to 30%
- The duty cycle is increased to 60%
- The duty cycle is decreased to 15%
- The duty cycle is increased to 50%

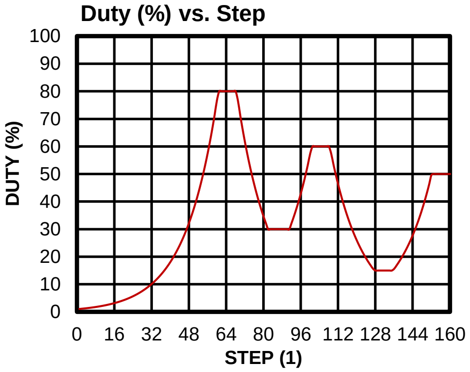


Figure 12: Logarithmic Dimming Curve with Continuous Duty Cycle Changes

Analog Dimming

During analog dimming, the LED current amplitude changes when the analog dimming register changes. Change the value of the analog dimming register for the corresponding channel via 0x17~0x26, bits[5:0]. The initial value of the analog dimming register is 0x20, though it can be set from 0x00 to 0x3F. When the register increases by 1 bit, the LED current amplitude increases by 0.5%. When the register decreases by 1 bit, the LED current amplitude decreases by 0.5%. I_{LED} can be adjusted to be between 84% and 115.5% of its normal value.

Global Dimming Function

When global dimming is disabled, the MPQ7225A can execute both analog dimming and PWM dimming for each channel independently. When global dimming is enabled, the dimming duty cycle and amplitude for each channel follows channel 1. This means that it is possible to adjust the LED current for each channel by only adjusting channel 1.

Phase Shift

The MPQ7225A can set the channel-by-channel current phase-shift function. This function is enabled via register 0x01, bits[13:12]. When phase-shift is enabled, the channel x + 1 (x = 1, 2...13) LED current phase shift is 1µs, 5µs, or 20µs after channel x's LED current rising edge.

Diagnostic and Fault Indications

The MPQ7225A supports a variety of diagnostic features, including the following:

- LED short protection
- LED open protection
- ISET pin open/short protection
- Thermal warning and shutdown

The /FS pin is an active-low open drain that is pulled high to an external voltage source via a 100kΩ resistor. If a protection is triggered, the corresponding fault bit in the register is set.

The LATCH_EN bit determines the channel behavior and pin behavior. Fault channels should latch off or set to hiccup mode if LED open or short protection occurs (not including V_{CC} UVLO, ISET pin open/short protection, thermal warning, and thermal shutdown). The integrated failsafe flag register indicates which channel triggered the protection; if any channel triggers a protection, the related register bit is set to 1.

If LATCH_EN = 1 (latch-off mode) and a fault is triggered, the fault channel remains off until POR or until EN turns off to reset the channel. Meanwhile, the other channels operate normally. Since the fault register is R1C (the register is cleared after being read once), the fault is not flagged again — even if the fault is present — unless VCC or EN is reset.

If LATCH_EN = 0 (hiccup mode), the fault channel tries to conduct for 32µs within every 1ms to detect whether the fault has been cleared. Once the fault condition is removed, the /FS pin is released high and the fault flag must be read by the MCU to be cleared . The fault bit and /FS pin cannot be reset until the fault condition is removed. VCC, EN, or EN_BIT can also reset the fault.

V_{CC} Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. V_{CC} UVLO does not trigger the /FS pin. If V_{CC} UVLO is triggered, the IC stops working and all the registers are reset.

LED Open Protection

The MPQ7225A features integrated LED open diagnostics. If V_{LEDx} drops below V_{LED_O} (about 100mV) for longer than 4ms, an open-load condition is detected. If there is an open load on one of the outputs, then the output turns off, the corresponding open fault bit (CHx_OPEN, where x = 1, 2...16) is set, and /FS is pulled low.

If LATCH_EN = 1 (latch-off mode), the fault channel remains off until POR or until EN turns off to reset the channel. Meanwhile, the other channels operate normally. /FS is released high once the fault bit is read-cleared by the MCU.

If LATCH_EN = 0 (hiccup mode), the LED open channel is not latched, and the fault channel tries to conduct for 32µs within every 1ms to detect whether the fault has been cleared. Once the open-load condition is no longer present, the channel turns on again and /FS releases high. The LED open bit remains set until it is read-cleared by the MCU and the open-load condition removed. The open fault bit and /FS pin cannot be reset until the open-load condition is removed.

LED Short Protection

During an LED short condition, V_{BIAS} - V_{LEDX} drops to low. If V_{LEDx} exceeds V_{LED_S} for 4ms, then LED short protection is triggered. The shorted channel turns off, the corresponding fault bit (CHx_SHORT) is set, and /FS is pulled low.

If LATCH_EN = 1 (latch-off mode), the fault channel remains off until VCC or EN go low to reset the channel. Meanwhile, the other channels operate normally. /FS is released high once the fault bit is read-cleared by the MCU.

If LATCH_EN = 0 (hiccup mode), the LED short channel is not latched, and the fault channel tries to conduct for 32µs within every 1ms to detect whether the fault has been cleared. Just as with an LED open fault, the short fault bit and /FS pin cannot be reset until the short condition is removed.

The LED short protection threshold can be configured via LED_SHORT_THR, bits[1:0].

There are four potential thresholds:

- If LED_SHORT_THR = 00, the threshold is 2V
- If LED_SHORT_THR = 01, the threshold is 3V
- If LED_SHORT_THR = 10, the threshold is 4V
- If LED_SHORT_THR = 11, the threshold is 5V

ISET Pin Open/Short Protection

The MPQ7225A implements a current monitor for the ISET resistor to provide open and short fault diagnostics and protection. The device monitors the current (I_{ISET}) flowing out of the ISET pin. If I_{ISET} exceeds I_{ISET_STH} (1mA), a short condition asserts. If I_{ISET} falls below I_{ISET_OTH} (5µA), an ISET pin open condition asserts.

ISET open or short protection is a latch-off protection. If an open or short condition is detected, the ISET_PIN_OPEN or ISET_PIN_SHORT bit is set, respectively. Then the MPQ7225A latches off and asserts /FS.

The fault bit can be cleared by the MCU, POR, or an EN reset. However, the /FS pin does not release high until POR or until EN goes high.

Thermal Warning

If the temperature exceeds 150°C, the OT_WARN bit is set and /FS asserts. The MPQ7225A continues working. /FS releases high once the thermal warning condition is removed. The fault bit remains set until it is cleared by the MCU, POR, or an EN reset.

Thermal warning can be individually masked via OT_WARN_MASK to prevent the /FS open-drain output from pulling low. Even if the fault is masked, the fault status can still be flagged by the registers.

Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. If the die temperature exceeds 170°C, all output channels turn off, the OT_STD bit is set, and /FS asserts. /FS releases high once the MPQ7225A recovers from thermal shutdown. The fault bit remains set until it is cleared by the MCU, POR, or an EN reset.

Thermal protection is a non-latch protection. Once the temperature drops 20°C below the thermal shutdown threshold, the MPQ7225A recovers, and the channels turn on using the previous settings without reinitializion.

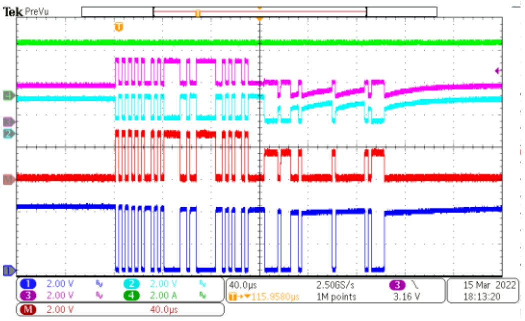
Differential Interface

The MPQ7225A is designed to operate with a differential interface for automotive lighting applications. By using the differential interface, the onboard MCU controls the settings and timings through a CAN transceiver.

The integrated differential interface is compatible with most CAN transceivers. It can communicate with other CAN transceivers by connecting the DATA+ and DATA- pins to the CAN bus. The interface features a high-speed receiver and transmitter capable of operating up to 2Mbps.

The differential interface is supplied by a 3.3V V_{CC} to maintain driver symmetry; the typical output common-mode voltage is 1.65V in the dominant state. The internal common-mode reference is V_{CC} / 2 = 1.65V to match the dominant state's common-mode output voltage. The transmitter converts a single-ended input (TXD) from the external CAN transceiver to differential outputs for the bus lines (DATA+ and DATA-).

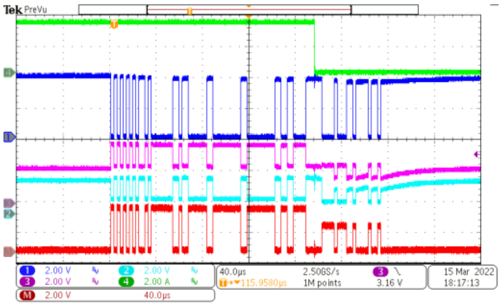
The receiver reads differential inputs from the bus lines (DATA+ and DATA-) and transfers this data as a single-ended output (RXD) to the internal digital circuitry. The receiver consists of a comparator that senses the voltage difference (V_{DIFF}) = (DATA+, DATA-) with respect to an internal 1.1V threshold. If V_{DIFF} exceeds 1.1V, a low logic is present at RXD. If V_{DIFF} falls below 0.7V, a high logic is present. The receiver always echoes the CAN bus data. Figure 13 shows the differential interface with a read command.



CH1: RX, CH2: DATA-, CH3: DATA+, CH4: I_{LED}

Figure 13: Differential Interface with Read CMD

Figure 14 shows the differential interface with a write command.



CH1: RX, **CH2: DATA-**, **CH3: DATA+**, **CH4: I_{LED}**

Figure 14: Differential Interface with Write CMD

Communication Protocol

The differential interface is a CAN-based protocol supported by most MCUs. Each frame contains multiple bytes, starting with a synchronization byte. The synchronization byte allows LED drivers to synchronize to the master MCU's frequency, which reduces costs on high-precision oscillators that are commonly used in CAN interfaces. The differential interface can support communication baud rates between 150kbps and 2Mbps.

The protocol supports the master and slave with a star-connected topology. The differential interface supports both write and readback commands (CMD).

Table 3 describes the frame structure of a typical 1-byte write action. When the MCU writes data to the MPQ7225A, the MPQ7225A's internal RX receives data from DATA+ and DATA- with a SYNC byte, DEV_ADDR, REG_ADDR, DATA, and CRC. Once the MPQ7225A verifies the cyclic redundancy check (CRC), it sends back a status byte and a CRC byte from TX to DATA+ and DATA-. Since the register is 16 bits long, it is transferred with the 8-bit LSB first, following by the 8-bit MSB.

Table 3: Write Frame

ST + 8-Bit + SP	ST + 8-Bit + SP	ST + 8-Bit + SP	ST + 8-Bit + SP	ST + 8-Bit + SP	ST + 8-Bit + SP	ST + 8-Bit + SP	ST + 8-Bit + SP
Sync Byte	Device address byte	Register address byte	DATA[0]	DATA[n]	CRC byte	Status byte	CRC byte

Figure 15 shows a write command with status feedback.

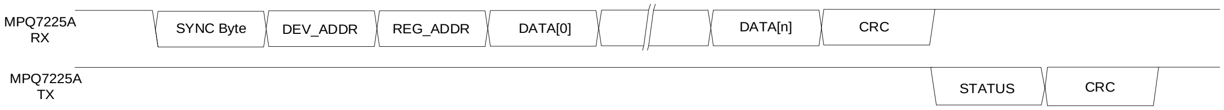


Figure 15: Write Command with Status Feedback

Table 4 describes the frame structure of a typical readback action. The master write frame consists of SYNC, DEV_ADDR, REG_ADDR, DATA, and CRC bytes. Once the MPQ7225A verifies the CRC, the MPQ7225A immediately feeds back the status byte and CRC byte to the MCU through DATA+ and DATA-. The CRC calculation does not include the sync bits.

Table 4: Read Frame

ST + 8-Bit + SP	ST + 8-Bit + SP	ST + 8-Bit + SP	ST + 8-Bit + SP	ST + 8-Bit + SP	ST + 8-Bit + SP	ST + 8-Bit + SP	ST + 8-Bit + SP
Sync Byte	Device address byte	Register address byte	CRC byte	Status byte	DATA[0]	DATA[n]	CRC byte

Figure 16 shows a read command with status feedback.

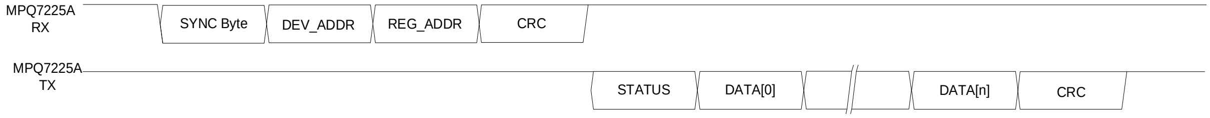


Figure 16: Read Command with Status Feedback

Synchronization Byte

The first byte transmitted from the MCU to the MPQ7225A is 01010101 (see Table 5). The MCU sends the clock signal to the MPQ7225A by outputting a 01010101 binary code in the first frame. The slave device adaptively uses the same clock to communicate with the MCU through the same internal, high-frequency clock. To avoid clock drift over time, the synchronization byte is always required for each new instruction transaction. This approach improves communication reliability and saves the cost of an external crystal oscillator.

Table 5: Synchronization Bytes

D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	1

Figure 17 shows the timing diagram for synchronization frame and device address frame.

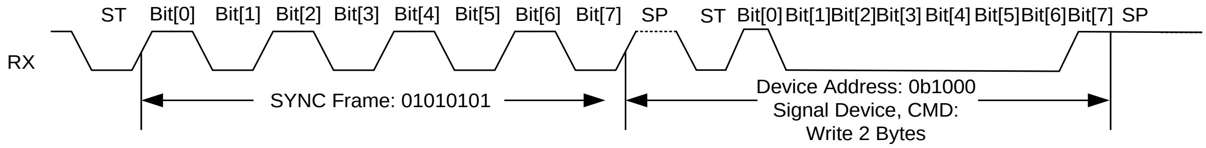


Figure 17: Synchronization Byte

Device Address Byte

The device address byte follows the synchronization byte (see Table 6).

Table 6: Device Address Byte

Bits	Bit Name	Description
D[7:4]	DEV_ADDR	Sets the device address.
D3	BROADCAST	Sets the broadcast mode. 1: Broadcast mode 0: Single-device only. Broadcast only accepts write commands
D[2:0]	CMD	Sets the command mode. Since this register is 2 bytes, the MPQ7225A can only support ⩾ 2 bytes. 000: Write 1 byte of data 001: Write 2 bytes of data 010: Write 4 bytes of data 011: Write 8 bytes of data 100: Read 1 byte of data 101: Read 2 bytes of data 110: Read 4 bytes of data 111: Read 8 bytes of data

Register Address Byte

As a read or write start address, the REG_ADDR frame follows the device address frame. There are a total of 8 bits of binary code in the register address byte (see Table 7). The register value can range and 0x00 and 0x33, with a 16-bit width.

Table 7: Register Address Byte

Bits	Bit Name	Description
D[7:0]	REG_ADDR	Sets the REG_ADDR register address.

Data Byte

For the data bytes, the data frame follows the register address byte. The MPQ7225A supports single data byte or multiple data byte writing in a one-time data transaction. The number of data bytes is defined in the device address byte (see Table 5). There are total of four options: 1, 2, 4, or 8 data bytes.

Status Byte

If no LED short or open condition is detected, then D5 and D4 are set to 0, and D3 is set to 1 to indicate that /FS is high (see Table 8).

Table 8: Status Byte

D7	D6	D5	D4	D3	D2	D1	D0
1	0	CH_SHORT	CH_OPEN	FS_PIN_STATUS	0	0	0

CRC Byte

The CRC code algorithm for multiple bytes of binary data is based on the polynomial $x^8 + x^5 + x^4 + 1$. The CRC code contains an 8-bit binary code, and the initial value is 0xFF. The poly value is 0x31, and the XOR value is 0x00. The CRC calculation does not include the sync bits.

REGISTER MAP WITHOUT OTP (10) (11)

Reg.	R/W	Addr.	Default	D[15]	D[14]	D[13]	D[12]	D[11]	D[10]	D[9]	D[8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
General Settings and Enable																			
SIL_REV	R	0x00	0x0001	RESERVED												SIL_REV			
DEV_CFG_1	R/W	0x01	0x0200	LED_SHORT_THR		SLEW_RATE		PHASE_SHIFT		PWM_FREQ		RESERVED						GLOBAL_DIM	FSS_EN
DEV_CFG_2	R/W	0x02	0x6003	CH_FS_MASK	LATCH_EN	CRC_EN	AUTO_DIM_MODE	AUTO_DIM_HOLD	AUTO_DIM_SPEED			OT_WARN_FS_MASK	RESERVED					MOD_EN	EN_ANA
CH_EN	R/W	0x03	0xFFFF	CH16_EN	CH15_EN	CH14_EN	CH13_EN	CH12_EN	CH11_EN	CH10_EN	CH9_EN	CH8_EN	CH7_EN	CH6_EN	CH5_EN	CH4_EN	CH3_EN	CH2_EN	CH1_EN
Diagnostics																			
DIAG_STAT_1	R1C	0x04	0x0000	CH16_OPEN	CH15_OPEN	CH14_OPEN	CH13_OPEN	CH12_OPEN	CH11_OPEN	CH10_OPEN	CH9_OPEN	CH8_OPEN	CH7_OPEN	CH6_OPEN	CH5_OPEN	CH4_OPEN	CH3_OPEN	CH2_OPEN	CH1_OPEN
DIAG_STAT_2	R1C	0x05	0x0000	CH16_SHORT	CH15_SHORT	CH14_SHORT	CH13_SHORT	CH12_SHORT	CH11_SHORT	CH10_SHORT	CH9_SHORT	CH8_SHORT	CH7_SHORT	CH6_SHORT	CH5_SHORT	CH4_SHORT	CH3_SHORT	CH2_SHORT	CH1_SHORT
DIAG_STAT_3	R1C	0x06	0x0000	RESERVED	OT_WARN	ISET_PIN_SHORT	ISET_PIN_OPEN	RESERVED	OT_SD	RESERVED									
Dimming and Additional Configurations																			
CH1_PWM	W/R	0x07	0x0FFF	RESERVED				PWM_DIM_1											
CH2_PWM	W/R	0x08	0x0FFF	RESERVED				PWM_DIM_2											
CH3_PWM	W/R	0x09	0x0FFF	RESERVED				PWM_DIM_3											
CH4_PWM	W/R	0x0A	0x0FFF	RESERVED				PWM_DIM_4											
CH5_PWM	W/R	0x0B	0x0FFF	RESERVED				PWM_DIM_5											
CH6_PWM	W/R	0x0C	0x0FFF	RESERVED				PWM_DIM_6											
CH7_PWM	W/R	0x0D	0x0FFF	RESERVED				PWM_DIM_7											
CH8_PWM	W/R	0x0E	0x0FFF	RESERVED				PWM_DIM_8											
CH9_PWM	W/R	0x0F	0x0FFF	RESERVED				PWM_DIM_9											
CH10_PWM	W/R	0x10	0x0FFF	RESERVED				PWM_DIM_10											
CH11_PWM	W/R	0x11	0x0FFF	RESERVED				PWM_DIM_11											
CH12_PWM	W/R	0x12	0x0FFF	RESERVED				PWM_DIM_12											
CH13_PWM	W/R	0x13	0x0FFF	RESERVED				PWM_DIM_13											
CH14_PWM	W/R	0x14	0xFFF	RESERVED				PWM_DIM_14											
CH15_PWM	W/R	0x15	0x0FFF	RESERVED				PWM_DIM_15											
CH16_PWM	W/R	0x16	0x0FFF	RESERVED				PWM_DIM_16											
CH1_ANA_DIM	W/R	0x17	0x0020	RESERVED										ANA_DIM_1					
CH2_ANA_DIM	W/R	0x18	0x0020	RESERVED										ANA_DIM_2					
CH3_ANA_DIM	W/R	0x19	0x0020	RESERVED										ANA_DIM_3					
CH4_ANA_DIM	W/R	0x1A	0x0020	RESERVED										ANA_DIM_4					
CH5_ANA_DIM	W/R	0x1B	0x0020	RESERVED										ANA_DIM_5					
CH6_ANA_DIM	W/R	0x1C	0x0020	RESERVED										ANA_DIM_6					
CH7_ANA_DIM	W/R	0x1D	0x0020	RESERVED										ANA_DIM_7					
CH8_ANA_DIM	W/R	0x1E	0x0020	RESERVED										ANA_DIM_8					
CH9_ANA_DIM	W/R	0x1F	0x0020	RESERVED										ANA_DIM_9					
CH10_ANA_DIM	W/R	0x20	0x0020	RESERVED										ANA_DIM_10					
CH11_ANA_DIM	W/R	0x21	0x0020	RESERVED										ANA_DIM_11					
CH12_ANA_DIM	W/R	0x22	0x0020	RESERVED										ANA_DIM_12					
CH13_ANA_DIM	W/R	0x23	0x0020	RESERVED										ANA_DIM_13					
CH14_ANA_DIM	W/R	0x24	0x0020	RESERVED										ANA_DIM_14					
CH15_ANA_DIM	W/R	0x25	0x0020	RESERVED										ANA_DIM_15					
CH16_ANA_DIM	W/R	0x26	0x0020	RESERVED										ANA_DIM_16					
PRE-VBIAS	R	0x27	0x5454	PRE-VBIAS_VOLT								REAL_VBIAS_VOLT							
DROP_BAND	R	0x28	0x25B9	RESERVED								LOW_BAND			HIGH_BAND			RESERVED	
SUFFIX_CODE	R	0x32	0x0000	RESERVED								SUFFIX_CODE							
SADDR_PAGE	R	0x33	0x0000	RESERVED										SADDR_PAGE	RESERVED				

Notes:

10) Commands in white that are not RESERVED or SIL_REV are read-only.
11) Commands in gray can be OTP read and written.

REGISTER DESCRIPTION

SIL_REV (0x00)

POR: Load from the OTP.

The SIL_REV command provides readout data and returns the silicon information.

Bits	Access	Bit Name	Default	Description
D[15:8]	RSV	RESERVED	0x00	Reserved. Always reads as 0.
D[7:4]	RSV	RESERVED	0x0	Reserved. Always reads as 0.
D[3:0]	R	SIL_REV	0x1	Returns the silicon revision information.

DEV_CFG_1 (0x01)

POR: Load from the OTP.

The DEV_CFG_1 command configures the LED short threshold, PWM dimming frequency, LED current slew rate, and phase shift during PWM dimming. It also enables global dimming and frequency spread spectrum control.

Bits	Access	Bit Name	Default	Description
D[15:14]	R/W	LED_SHORT_TH	00	Sets the LED short threshold. 00: 2V 01: 3V 10: 4V 11: 5V
D[13:12]	R/W	SLEW_RATE	00	Controls the dimming slew rate. 00: No slew rate 01: 5µs 10: 10µs 11: 20µs
D[11:10]	R/W	PHASE_SHIFT	00	Controls the PWM dimming phase shift. 00: No phase shift between channels 01: The rising edge of channel x + 1 is 1µs after channel x 10: The rising edge of channel x + 1 is 5µs after channel x 11: The rising edge of channel x + 1 is 20µs after channel x
D[9:8]	R/W	PWM_FREQ	10	Sets the LED channel PWM dimming frequency. The PWM frequency can be changed on the fly. 00: 1kHz 01: 500Hz 10: 250Hz 11: 1kHz
D[7:2]	RSV	RESERVED	0	Reserved.
D1	R/W	GLOBAL_DIM	0	When global dimming is enabled, all channels share dimming settings with channel 1. This allows users to adjust the LED current of all channels by only changing channel 1. 0: Disable global dimming 1: Enable global dimming
D0	R/W	FSS_EN	0	Enables frequency spread spectrum (FSS). 0: Disabled 1: Enabled

DEV_CFG_2 (0x02)

POR: Load from the OTP.

The DEV_CFG_2 command configures the LED open/short fault mask and protection behavior, the thermal warning fault mask, automatic dimming parameters, logarithmic automatic dimming, AFC, and the analog dimming circuit.

Bits	Access	Bit Name	Default	Description
D15	R/W	CH_FS_ MASK	0	Enables the /FS mask for LED channel diagnostics. 0: Disabled. /FS pulls down if there is a fault error flag or any channel experiences a short/open 1: Enabled. /FS does not pull down if there is a fault error flag or any channel experiences a short/open
D14	R/W	LATCH_EN	1	Sets the fault protection mode. If a fault is detected on a channel, the related channel latches off or enters hiccup mode while the other channels work normally. 0: Hiccup mode 1: Latch-off mode
D13	RSV	CRC_EN	1	Reserved.
D12	R/W	AUTO_DIM_ MODE	0	Sets the logarithmic automatic dimming mode. 0: Manual mode. The PWM dimming duty cycle changes for the next PWM dimming cycle 1: Automatic diming mode (logarithmic dimming). The duty cycle changes according to the fixed exponential curve with a certain speed setting
D11	R/W	AUTO_DIM_ HOLD	0	0: Normal operation. The dimming duty cycles changes to the setting value 1: Stop all the ongoing automatic dimming ramping, and remain at the current dimming value on the curve
D[10:8]	R/W	AUTO_DIM_ SPEED	000	Sets the automatic dimming speed for the 64-point logarithmic curve. 000: Normal speed. Jump 4 points per PWM cycle (0% to 100% in 16 PWM cycles) 001: 2x speed. Jump 8 points per PWM cycle (0% to 100% in 8 PWM cycles) 010:4x speed. Jump 16 points per PWM cycle (0% to 100% in 4 PWM cycles) 011: 1/2x speed. Jump 2 points per PWM cycle (0% to 100% in 32 PWM cycles) 100: 1/4x speed, jump 1 points per PWM cycle (0% to 100% in 64 PWM cycles) Others: Reserved, or similar to selecting 000
D7	R/W	OT_WARN_ FS_MASK	0	Sets the over-temperature (OT) warning diagnostic mask control. 0: An OT warning signal pulls down the /FS pin 1: An OT warning signal does not pull down the /FS pin
D[6:2]	RSV	RESERVED	0	Reserved.
D1	R/W	MOD_EN	1	0: AFC is disabled. Disable the up-down counter and maintain the current modulation bit 1: AFC is enabled. Enable the up-down counter
D0	R/W	EN_ANA	1	0: The analog circuit is disabled. When disabled, the device shuts down 1: The analog circuit is enabled. When enabled, the device turns on

CH_EN (0x03)

POR: Load from the OTP.

The CH_EN command enables channels 1–16.

Bits	Access	Bit Name	Default	Description
D[15:0]	R/W	CHx_EN	0xFFFF	Channel enable bits. Bits[15:0] control channel 16 to channel 1, respectively. If any channel is not used, set the related bit to 0. 0: Disabled 1: Enabled

DIAG_STAT_1 (0x04)

POR: N/A

The DIAG_STAT_1 command reports the channel LEDx open statuses. If any bit is set to 1, this means the related channel is open. If the register is read one time, the open flag resets to 0.

Bits	Access	Bit Name	Default	Description
D[15:0]	R1C	CHx_OPEN	0x0000	Channel x open protection fault flag. Bits[15:0] control channel 16 to channel 1, respectively. If any channel is not used, set the related bit to 0. 0: No open fault has been detected 1: An open fault has been detected. After being read, /FS is reset with the fault flag reset if the mode is set to latch-off mode; if the mode is set to hiccup mode, the fault flag and /FS pin are not reset until the fault is removed

DIAG_STAT_2 (0x05)

POR: N/A

The DIAG_STAT_2 command reports the channel LEDx short statuses. If the bit is set to 1, the related channel is experiencing a short condition. If the register is read one time, the open flag resets to 0.

Bits	Access	Bit Name	Default	Description
D[15:0]	R1C	CHx_SHORT	0x0000	Channel x short protection fault flag. Bits[15:0] control channel 16 to channel 1, respectively. If any channel is not used, set the related bit to 0. 0: No short fault has been detected 1: A short fault has been detected. After being read, /FS is reset with the fault flag reset if the mode is set to latch-off mode; if the mode is set to hiccup mode, the fault flag and /FS pin are not reset until the fault is removed

DIAG_STAT_3 (0x06)

POR: N/A

The DIAG_STAT_3 command reports an over-temperature (OT) warning, ISET pin short/open fault, and thermal shutdown status. If a bit is set to 1, the related protection is triggered; when the register is read one time, the related flag resets to 0.

Bits	Access	Bit Name	Default	Description
D15	RSV	RESERVED	0	Reserved.
D14	R1C	OT_WARN	0	Over temperature (OT) warning status. 0: No OT warning is present 1: There is an OT warning. After being read, the fault flag is reset. When the temperature recovers, /FS returns to high

D13	R1C	ISET_PIN_SHORT	0	ISET pin short flag. 0: No short condition has been detected on the ISET pin 1: A short condition has been detected on the ISET pin. After being read, the fault flag is reset. Only VCC or EN can reset the /FS pin
D12	R1C	ISET_PIN_OPEN	0	ISET pin open flag. 0: No open condition has been detected on the ISET pin 1: An open condition has been detected on the ISET pin. After being read, the fault flag is reset. Only VCC or EN can reset the /FS pin
D11	RSV	RESERVED	0	Reserved.
D10	R1C	OT_SD	0	Returns the OT shutdown status. 0: No OT shutdown has occurred 1: OT shutdown has occurred. After being read, the fault flag is reset. When the temperature recovers, /FS pulls high
D[9:0]	RSV	RESERVED	0	Reserved.

CHx_PWM (0x07~0x16)

POR: Load from the OTP.

The CHx_DIM command controls the PWM dimming duty cycle for all channels (channels 1–16). Register 0x07 corresponds to channel 1, while register 0x16 corresponds to channel 16.

Bits	Access	Bit Name	Default	Description
D[15:12]	RSV	RESERVED	0	Reserved.
D[11:0]	R/W	PWM_DIM	0xFFF	Sets PWM dimming for the corresponding channel.

CHx_ANA_DIM (0x17~0x26)

POR: Load from the OTP.

The CHx_ANA_DIM command controls the analog dimming range for all channels (channels 1–16). Register 0x17 corresponds to channel 1, while register 0x26 corresponds to channel 16.

Bits	Access	Bit Name	Default	Description
D[15:6]	RSV	RESERVED	0	Reserved.
D[5:0]	R/W	ANA_DIM	0x20	Sets analog dimming for the corresponding channel. The register value can be set from 0x00 to 0x3F.

VBIAS_VOLT (0x27)

POR: Load from the OTP.

The VBIAS_VOLT command sets the pre-V_{BIAS} voltage. It can only be changed via the OTP.

<table>
<tr><th>Bits</th><th>Access</th><th>Bit Name</th><th>Default</th><th>Description</th></tr>
<tr><td>D[15:8]</td><td>R</td><td>PRE-VBIAS</td><td>0x54</td><td>Sets the pre-V_{BIAS} voltage. When the register value increases by 1, V_{BIAS} increases by 0.05V, and the V_{FBO} = 1.2V.
<table>
<tr><th>V_{BIAS} (V)</th><th>Bits[15:8] (Dec)</th><th>Bits[15:8] (Hex)</th></tr>
<tr><td>2.5</td><td>14</td><td>0E</td></tr>
<tr><td>2.55</td><td>15</td><td>0F</td></tr>
<tr><td>…</td><td>…</td><td>…</td></tr>
<tr><td>13.95</td><td>243</td><td>F3</td></tr>
<tr><td>14</td><td>244</td><td>F4</td></tr>
</table>
</td></tr>
<tr><td>D[7:0]</td><td>R</td><td>REAL_VBIAS</td><td>0xxx</td><td>Returns the real value of the V_{BIAS} counter. This value is automatically adjusted after the MPQ7225A starts up.</td></tr>
</table>

DROP_BAND (0x28)

Default: 0x25B9

POR: Load from the OTP.

The DROP_BAND command controls the LED voltage (V_{LEDx}) for the AFC band, including the low band and the high band. It can only be changed via the OTP.

<table>
<tr><th>Bits</th><th>Access</th><th>Bit Name</th><th>Default</th><th>Description</th></tr>
<tr><td>D[15:8]</td><td>RSV</td><td>RESERVED</td><td>0x25</td><td>Reserved.</td></tr>
<tr><td>D[7:5]</td><td>R</td><td>LOW_BAND</td><td>0b101</td><td>Sets the low-band value for AFC.
<table>
<tr><th>Bits[7:5]</th><th>Low-Band Value</th><th>Bits[7:5]</th><th>Low-Band Value</th></tr>
<tr><td>000</td><td>0.2V</td><td>100</td><td>0.4</td></tr>
<tr><td>001</td><td>0.25V</td><td>101</td><td>0.45</td></tr>
<tr><td>010</td><td>0.3V</td><td>110</td><td>0.5</td></tr>
<tr><td>011</td><td>0.35V</td><td>111</td><td>0.55</td></tr>
</table></td></tr>
<tr><td>D[4:2]</td><td>R</td><td>HIGH_BAND</td><td>0b110</td><td>Sets the high-band value for AFC.
<table>
<tr><th>Bits[4:2]</th><th>High-Band Value</th><th>Bits[4:2]</th><th>High-Band Value</th></tr>
<tr><td>000</td><td>0.25V</td><td>100</td><td>0.45</td></tr>
<tr><td>001</td><td>0.3V</td><td>101</td><td>0.5</td></tr>
<tr><td>010</td><td>0.35V</td><td>110</td><td>0.55</td></tr>
<tr><td>011</td><td>0.4</td><td>111</td><td>0.6</td></tr>
</table></td></tr>
<tr><td>D[1:0]</td><td>RSV</td><td>RESERVED</td><td>0b01</td><td>Reserved.</td></tr>
</table>

SUFFIX_CODE (0x32)

POR: Load from the OTP.

The SUFFIX_CODE command returns the code information. It can only be changed via the OTP.

Bits	Access	Bit Name	Default	Description
D[15:8]	RSV	RESERVED	0x00	Reserved.
D[7:0]	R	SUFFIX_ CODE	0x00	Returns the suffix code information. It can also be used to store the code information, though this can only be changed via the OTP.

SADDR_PAGE (0x33)

Default: 0x0000. Read-only after OTP.

POR: Load from the OTP

The SADDR_PAGE command controls the device address. It can only be changed via the OTP, and is read-only after OTP.

Bits	Access	Bit Name	Default	Description
D[15:7]	RSV	RESERVED	0x00	Reserved.
D6	R	SADDR_ PAGE	0	Information register. Can be set to 0 or 1 via the OTP to support different device addresses.
D[5:0]	RSV	RESERVED	0x00	Reserved.

APPLICATION INFORMATION

AFC Network Connection

The FBI, FBO, and MODE pins are related to AFC. If AFC is not used, float the FBO pin, then connect FBI and MODE to GND (see Figure 18).

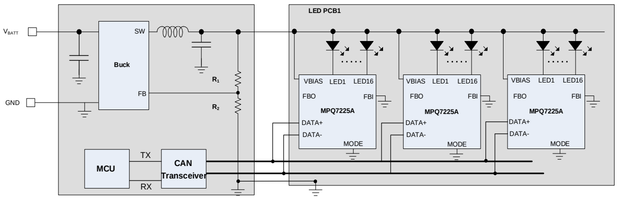


Figure 18: Application Circuit without AFC

V_{BIAS} can be set by the DC/DC converter's feedback voltage, calculated with Equation (3):

$$VBIAS = V_{FB}(1+\frac{R_1}{R_2}) \tag{3}$$

Consider the maximum LED voltage and ensure that (V_{BIAS} - V_{LED}) exceeds the headroom of each V_{LEDx}.

When using AFC, connect the FBI pin of the last slave device or single chip to GND; otherwise, connect FBI to the FBO pin of the next MPQ7225A for the current sink headroom information (see Figure 19).

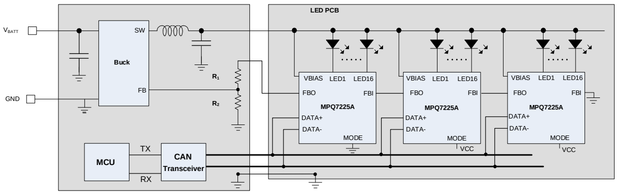


Figure 19: Application Circuit with AFC and a Connected FBO

For example, slave 2's FBI pin should connected to slave 3's FBO pin. For the master device, the FBO pin is the feedback output, and it should be connected to the DC/DC converter's feedback pin through a resistor divider network.

If the MPQ7225A and DC/DC converter are on the same board, or there is a connected FBO wire condition, the resistor network can be connected following Figure 18. Then the FB resistors can be estimated with Equation (4):

$$V_{FBO} = V_{FB}(1+\frac{R_1}{R_2}) \tag{4}$$

Where V_{FB} is the feedback reference voltage of the DC/DC converter (e.g. for the MPQ4323C, it is 0.8V), and FBO can between 0.6V and 2.2V. If V_{FBO} = 1.2V and R_2 = 80.6kΩ, then R_1 is 40.2kΩ.

The pre-V_{BIAS} voltage is set via the OTP, internal modulator, and resistors (R_1 and R_2) (see Figure 20).

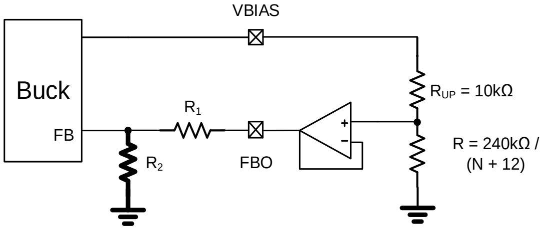


Figure 20: AFC Modulator Network

In Figure 20, N can be adjusted from 14 to 244 via OTP register 0x27. The pre-V_{BIAS} voltage should match the V_{LED}, or the device may detect an LED open or short when the LED is on. So if V_{FBO} = 1.2V and N = 100 (0x6464), then pre-V_{BIAS} should be set to 6.8V.

N automatically adjusts when V_{LED} changes after the device starts operating. If V_{FB} = 0.8V, R_2 = 80.6kΩ, and R_1 = 40.2kΩ, then V_{FBO} is about 1.2V, and V_{BIAS} can be adjusted between 2.5V and 14V with an N change between 14 and 244. See the VBIAS_VOLT (0x27) section on page 39 for more details.

If the MPQ7225A and DC/DC converter are not on the same PCB, there must be an FBO line between the converter and the MPQ7225A. If the FBO line is open, V_{BIAS} is regulated to the battery voltage (V_{BATT}), then an LED short is triggered.

A resistor network can be used to prevent V_{BIAS} from regulating to V_{BATT} when the FBO line is open.

Figure 21 shows the AFC modulator network.

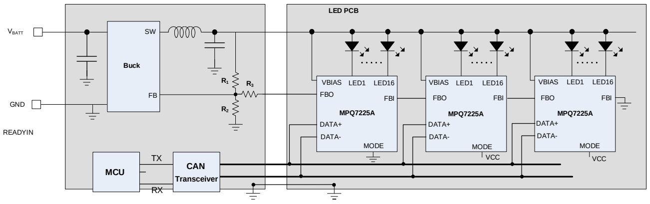


Figure 21: AFC Modulator Network

V_{BIAS} can be calculated with Equation (5):

$$V_{BIAS}=\frac{V_{FB}\times(R_1+R_3)+\frac{V_{FB}}{R2}\times R_1\times R_3}{R_1\times\frac{\frac{240}{N+12}}{10+\frac{240}{N+12}}+R_3} \quad (5)$$

When R3 is disconnected, V_{BIAS_O} can be estimated with Equation (6):

$$V_{BIAS\_O}=V_{FB}\times(1+\frac{R_1}{R_2}) \quad (6)$$

Figure 22 shows the AFC network with FBO open protection.

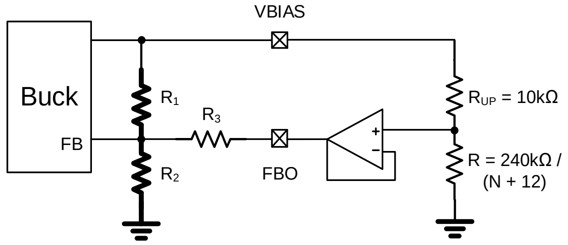


Figure 22: AFC Modulator Network with FBO Open Protection

For example, if the MPQ7225A has 2 LEDs in series (V_{LED} = 6.3V), set V_{BIAS_O} = 7.1V when FBO is open. If the DC/DC converter's V_{FB} is 0.8V (based on Equation (6)), select R_1 = 100kΩ so that R_2 = 12.7kΩ. If N is set to 100 via the OTP, set R_3 = 100kΩ. Then the pre-V_{BIAS} voltage is 6.71V based on Equation (5). When N changes from 14 to 244, V_{BIAS} changes from 5.9V to 7.6V, so consider the pre-V_{BIAS} value set via the OTP as well as resistor selection when making this connection. The connection shown in Figure 21 on page 41 minimizes the V_{BIAS} range.

Selecting the VBIAS Capacitor

The VBIAS pin is the bias supply. The MPQ7225A operates from an input voltage (V_{IN}) between 2.5V and 18V. A capacitor (C_{IN}) is required to decouple the VBIAS line's voltage noise. For example, if using the MPQ4323 output as the V_{BIAS} for the MPQ7225A, a decoupling capacitance is required for the MPQ7225A's VBIAS: 2 x 22µF, 2 x 10µF, and 0.1µF. Place the 22µF capacitors close to the MPQ4323. Place the 10µF capacitors close the LEDs, and place the 0.1µF capacitor close to the MPQ7225A's VBIAS pin.

Selecting the VCC Capacitor and Current Capability

The VCC is pin is the internal bias power supply. An internal LDO from VBIAS generates the 3.3V VCC. VCC supplies power to the internal control circuit and gate drivers. A ≥10µF decoupling capacitor should be placed from VCC to ground. VCC requires power from the external LDO if V_{BIAS} cannot sufficiently power VCC. The external LDO should be between 3.1V and 3.5V, with a 50mA + 20mA current ability. When there are multiple devices in parallel, the external DC source current ability should be ((50mA + *n* x 20mA)), where the *n* is the number of devices.

LED Current Setting

Set the LED currents of all channels with an external resistor at ISET pin, calculated with Equation (7):

$$I_{SET}(mA)=\frac{600}{R_{ISET}(k\Omega)} \quad (7)$$

Certain ISET resistances are recommended (see Table 10).

Table 10: Resistor Selection

I_{LED} (mA)	R_{ISET} (kΩ)
200	3.01
100	6.04
50	12.1

I_{LED} can be adjusted via analog dimming and PWM dimming. For more details, see the Pulse-Width Modulation (PWM) Dimming section on page 28 and the Analog Dimming section on page 29.

MODE Pin Configuration

If AFC is disabled, connect the MODE pin to GND. If AFC is enabled and the part is the master device, connect MODE to GND; if it is a slave device, connect MODE to VCC.

EN Pin

If the EN pin is not used to control the MPQ7225A on/off function, EN can be directly connected to VBIAS through a 10kΩ resistor. When EN pulls low, VCC shuts down and all the registers are reset.

ADDR1 and ADDR2 Pin

The ADDR1 and ADDR2 pins set the device address. They must be connected to VCC and GND, or connected to GND through a 35kΩ resistor (within a ±10% range).

ESD Protection Design

Electrostatic discharge (ESD) is the release of static electricity when two objects come into contact. If any of the MPQ7225A's pins are connected to another board through a connector with a line, those pin(s) may suffer from ESD issues. Generally, the LEDx, DATA+, DATA-, and FBO pins are most likely to be connected to another board through a line. For the LEDx pin, it is recommended to place a ≤100nF capacitor in parallel with VLEDx to protect against ESD if the LED load and MPQ7225A are not on the same board. For the DATA+ and DATA- pins, it is recommended that the total capacitance be ≤100pF and that an ESD diode be placed in parallel with DATA+ and DATA- to protect against ESD in real-world application. For the ESD diode, the recommended maximum peak repetitive reverse voltage (V_{RRM}) is 5V, and should always be below 18V.

PCB Layout Guidelines for BCI/EMC

Consider the bulk current injection (BCI), as FBO has a maximum current capability of 5mA for anti-interference. To improve BCI and EMC results, refer to Figure 23 on page 44 and follow the guidelines below:

1. For the buck converter (e.g. the MPQ4323C), place the symmetric input capacitors as close to VIN and GND as possible.
2. For the buck converter, ensure that the high-current paths at GND and VIN have short, direct, and wide traces.
3. For the buck converter, place the VCC capacitor as close to VCC and GND as possible.
4. For the buck converter, route SW and BST away from sensitive analog areas, such as FB.
5. For the MPQ7225A, place the feedback resistors close to the chip to ensure that the trace connected to FB is as short as possible.
6. For the MPQ7225A, place the capacitors as close to the input as possible.
7. For the MPQ7225A, add a small capacitor as close to the IC pins as possible to improve anti-interference abilities.
8. For the MPQ7225A, a large GND polygon is necessary to improve anti-interference abilities and heat dissipation.

2-Layer Layout Guidelines

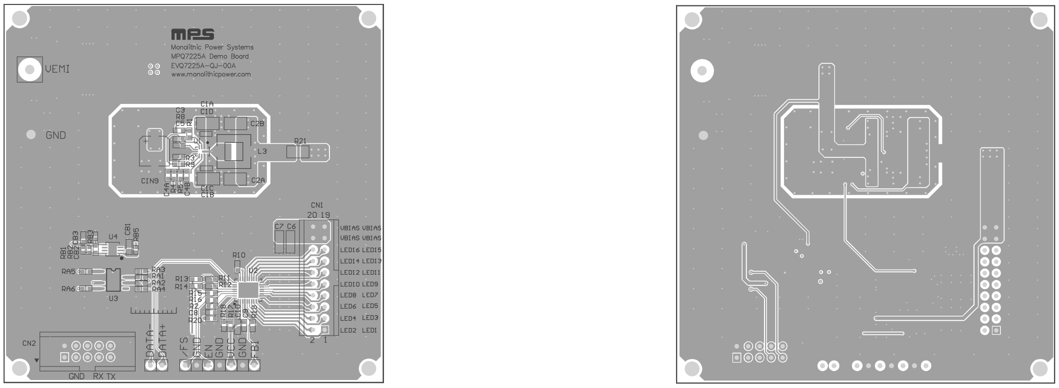
For a 2-layer PCB layout, follow the steps below:

1. The top layer should include the power, signal, and GND.
2. Cover GND in all areas except for the signal and power path.
3. The bottom layer should only include the GND polygon to shield noise interference, unless there is not enough PCB space.

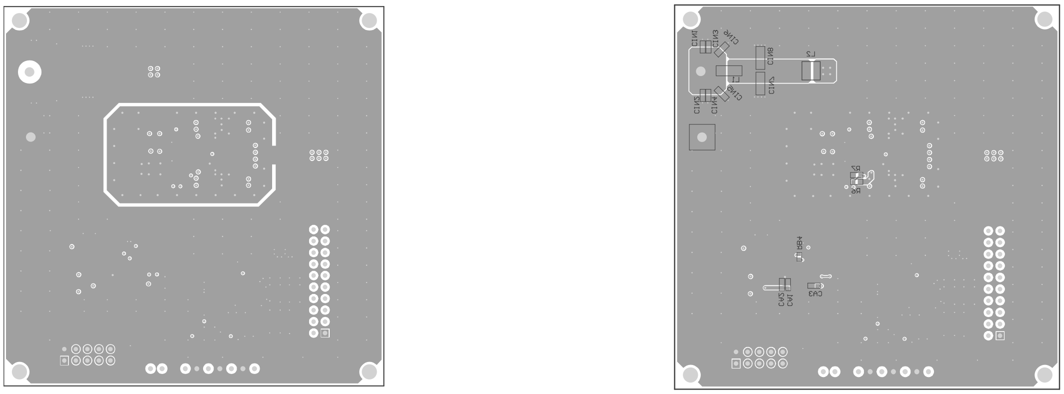
4-Layer Layout Guidelines

For a 4-layer PCB layout, follow the steps below:

1. The top layer should include the power, signal, and GND.
2. Cover GND in all areas on the top layer except for the signal and power path.
3. The second layer should only include GND to shield noise interference on the top layer.
4. The third layer should include the power, signal, and GND.
5. Cover GND in all areas on the third layer except for the signal path.
6. Cover GND in all areas on the bottom layer except for the signal and power path.



Top Layer **Mid-Layer 2**



Mid-Layer 1 **Bottom Layer**

Figure 23: Recommended PCB Layout

Note:

12) The recommended PCB layout is based on Figure 24 on page 45.

TYPICAL APPLICATION CIRCUIT

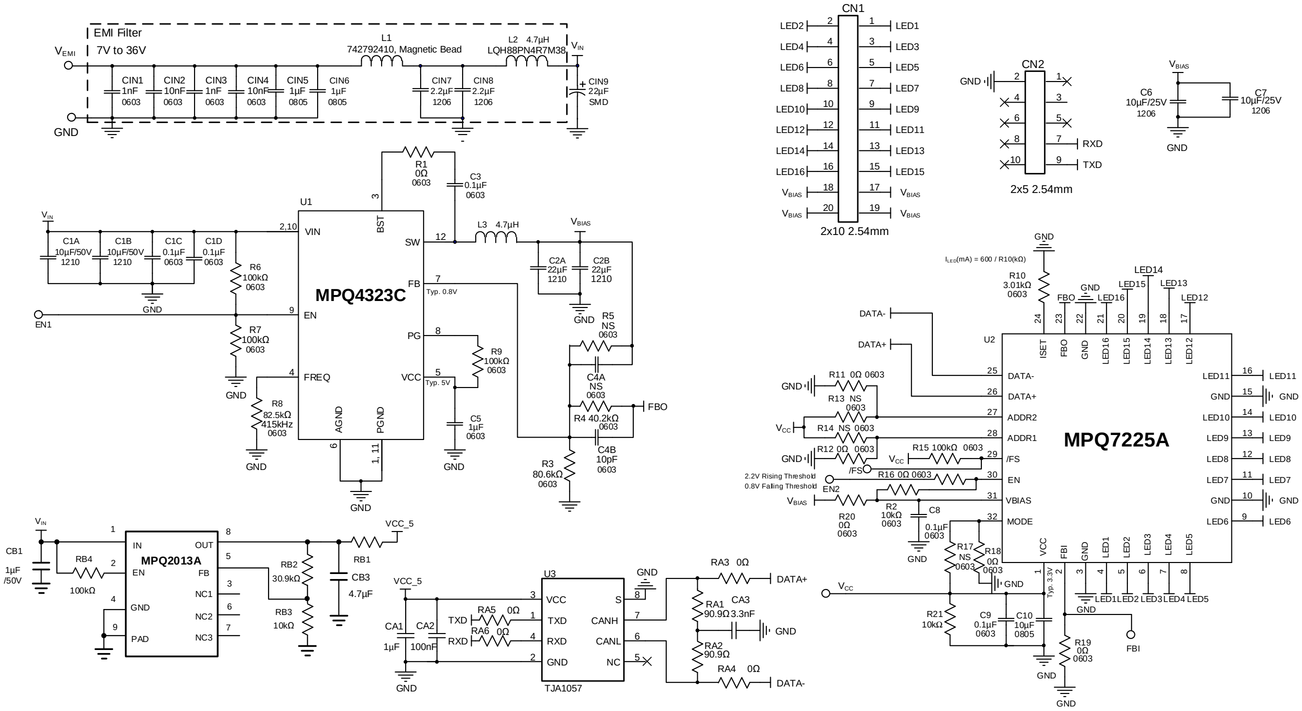
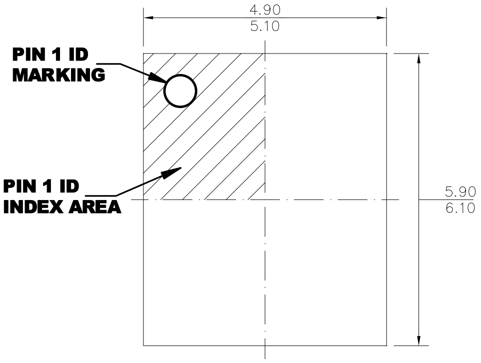


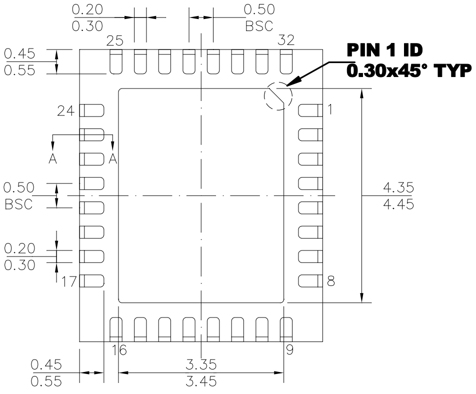
Figure 24: Typical Application Circuit (I_{LED} = 200mA/Channel)

PACKAGE INFORMATION

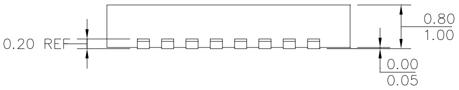
QFN-32 (5mmx6mm)
Wettable Flank



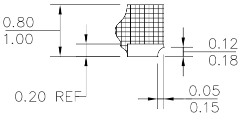
TOP VIEW



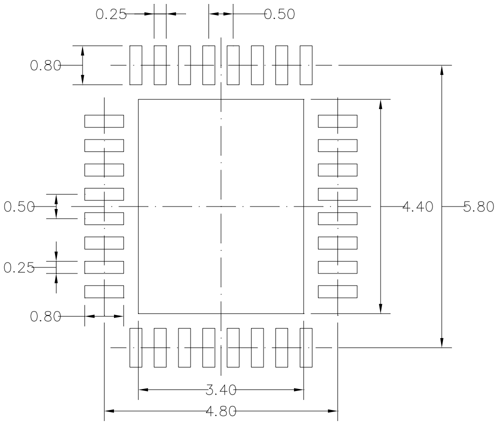
BOTTOM VIEW



SIDE VIEW



SECTION A-A

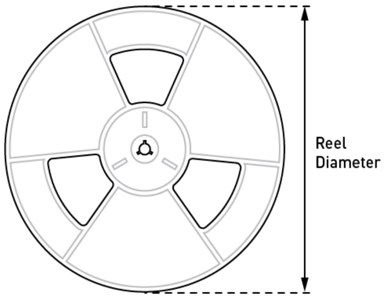


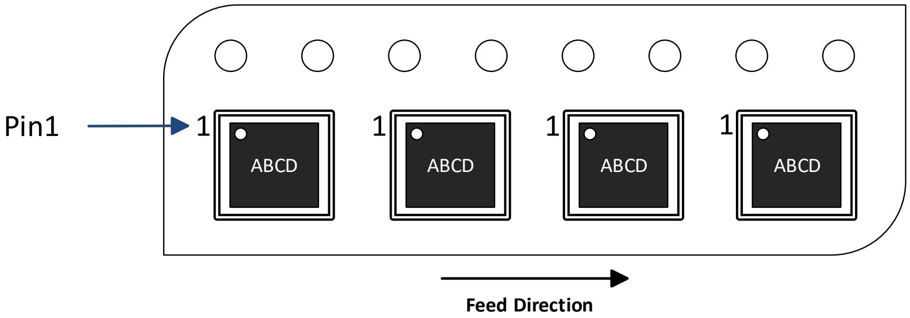
RECOMMENDED LAND PATTERN

NOTE:

1) THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
4) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
5) JEDEC REFERENCE IS MO-220.
6) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION





Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ7225AGQJE -xxxx-AEC1-Z	QFN-32 (5mmx6mm)	5000	N/A	N/A	13in	12mm	8mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	8/15/2023	Initial Release	-

Notice: The information in this document is subject to change without notice. Please contact MPS for current specifications. Users should warrant and guarantee that third-party Intellectual Property rights are not infringed upon when integrating MPS products into any application. MPS will not assume any legal responsibility for any said applications.