

### DESCRIPTION

The MPQ6619 is an H-bridge motor driver that operates from a 2.7V to 28V supply voltage ( $V_{IN}$ ) and achieves an output current ( $I_{OUT}$ ) of up to 5A. The MPQ6619 is ideally suited to drive a brushed DC motor.

The MPQ6619 features a configurable current limit. Full protection features include over-current protection (OCP), input over-voltage protection (OVP), under-voltage lockout (UVLO), and over-temperature protection (OTP).

The MPQ6619 is available in a QFN-19 (4mmx4mm) package, and is AEC-Q100 qualified.

### FEATURES

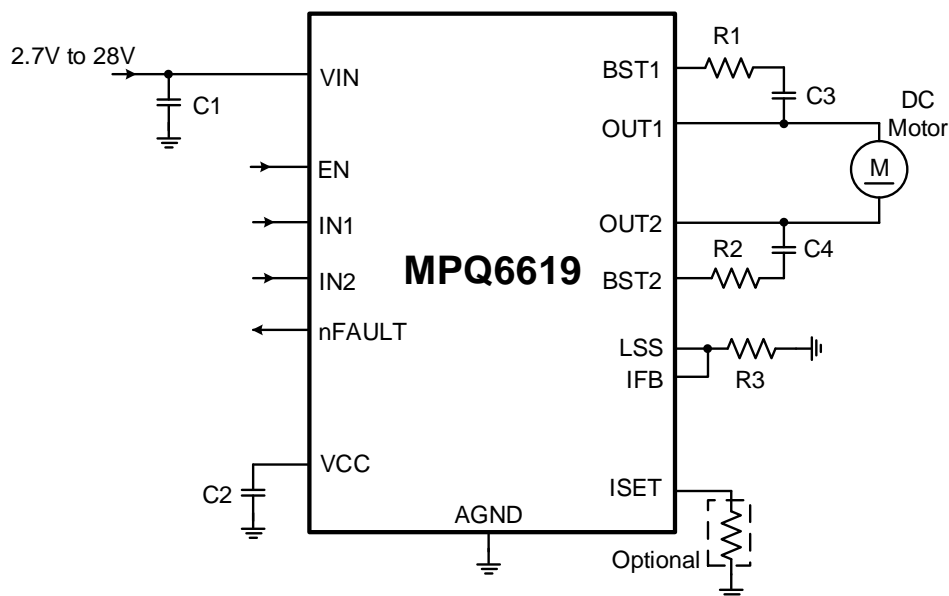
- Wide 2.7V to 28V Operating Supply Voltage ( $V_{IN}$ ) Range
- Up to 5A Peak of Output Current ( $I_{OUT}$ )
- Internal H-Bridge Driver
- Configurable Current Limit
- 65m $\Omega$  On Resistance ( $R_{DS(ON)}$ ) for Each Half-Bridge MOSFET
- 100% Duty Cycle H-Bridge Operation
- 1 $\mu$ A Shutdown Mode Current
- Over-Current Protection (OCP)
- Input Over-Voltage Protection (OVP)
- Under-Voltage Lockout (UVLO)
- Over-Temperature Protection (OTP)
- Fault Indication Output
- Available in a QFN-19 (4mmx4mm) Package
- Available in AEC-Q100 Grade 1

### APPLICATIONS

- DC Motors
- Solenoid/Actuators

All MPS parts are lead-free, halogen-free, and adhere to the RoHS directive. For MPS green status, please visit the MPS website under Quality Assurance. "MPS", the MPS logo, and "Simple, Easy Solutions" are trademarks of Monolithic Power Systems, Inc. or its subsidiaries.

### TYPICAL APPLICATION



### ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MPQ6619GRE-AEC1	QFN-19 (4mmx4mm)	See Below	1

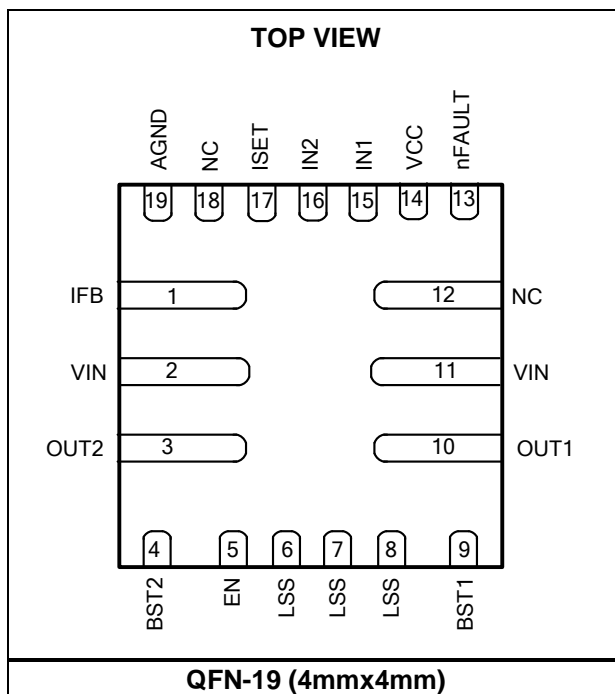
\* For Tape & Reel, add suffix -Z (e.g. MPQ6619GRE-AEC1-Z).

### TOP MARKING

**MPSYWW**  
**MP6619**  
**LLLLLL**  
**E**

MPS: MPS prefix  
 Y: Year code  
 WW: Week code  
 MP6619: Part number  
 LLLLLL: Lot number  
 E: Wettable flank

### PACKAGE REFERENCE



## PIN FUNCTIONS

Pin #	Name	Description
1	IFB	<b>Current-sense (CS) signal feedback.</b> Connect the IFB and LSS pins together.
2, 11	VIN	<b>Input supply voltage.</b>
3	OUT2	<b>Output terminal 2.</b>
4	BST2	<b>Bootstrap (BST) pin for the OUT2 high-side MOSFET (HS-FET) gate driver.</b> Connect a capacitor between the BST2 and OUT2 pins.
5	EN	<b>IC enable.</b> The EN pin is pulled down internally.
6, 7, 8	LSS	<b>Low-side (LS) source connection.</b> For CS, connect a CS resistor between the LSS pin and power ground.
9	BST1	<b>OUT1 HS-FET gate driver.</b> Connect a capacitor between the BST1 and OUT1 pins.
10	OUT1	<b>Output terminal 1.</b>
12, 18	NC	<b>No connection.</b> Float this pin or connect it to AGND.
13	nFAULT	<b>Fault indication output.</b> The nFAULT pin is pulled active low for fault conditions.
14	VCC	<b>5V LDO output for internal driver and logic.</b>
15	IN1	<b>Output 1 control input.</b> The IN1 pin is pulled down internally.
16	IN2	<b>Output 2 control input.</b> The IN2 pin is pulled down internally.
17	ISET	<b>Current trip voltage setting.</b> Connect a resistor from the ISET pin to GND.
19	AGND	<b>Internal logic ground.</b>

### ABSOLUTE MAXIMUM RATINGS <sup>(1)</sup>

Input supply voltage ( $V_{IN}$ )	35V
$V_{OUTX}$	-0.3V to $V_{IN} + 0.3V$
$V_{BST1}$	$V_{OUT1} + 6V$
$V_{BST2}$	$V_{OUT2} + 6V$
LSS	-0.3V to +0.3V
All other pins	-0.3V to +6V
Continuous power dissipation ( $T_A = 25^\circ C$ ) <sup>(2)</sup>	
QFN-19 (4mmx4mm)	2.8W
Junction temperature ( $T_J$ )	150°C
Lead temperature	260°C
Storage temperature	-65°C to +150°C

### ESD Ratings

Human body model (HBM)	$\pm 1.8kV$
Charged-device model (CDM)	$\pm 2kV$

### Recommended Operating Conditions <sup>(3)</sup>

Input supply voltage ( $V_{IN}$ )	2.7V to 28V
Operating junction temp ( $T_J$ )	-40°C to +125°C

<b>Thermal Resistance <sup>(4)</sup></b>	$\theta_{JA}$	$\theta_{JC}$
QFN-19 (4mmx4mm)	44	9

#### Notes:

- Exceeding these ratings may damage the device.
- The maximum allowable power dissipation is a function of the maximum junction temperature  $T_J$  (MAX), the junction-to-ambient thermal resistance  $\theta_{JA}$ , and the ambient temperature  $T_A$ . The maximum allowable continuous power dissipation at any ambient temperature is calculated by  $P_D$  (MAX) =  $(T_J$  (MAX) -  $T_A$ ) /  $\theta_{JA}$ . Exceeding the maximum allowable power dissipation can produce an excessive die temperature, which may cause the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- The device is not guaranteed to function outside of its operation conditions.
- Measured on a JESD51-7, 4-layer PCB.

## ELECTRICAL CHARACTERISTICS

$V_{IN} = 13.5V$ ,  $T_J = -40^{\circ}C$  to  $+125^{\circ}C$ , unless otherwise noted.

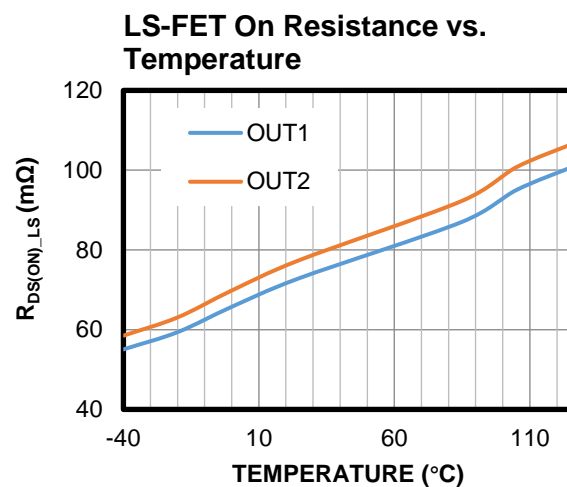
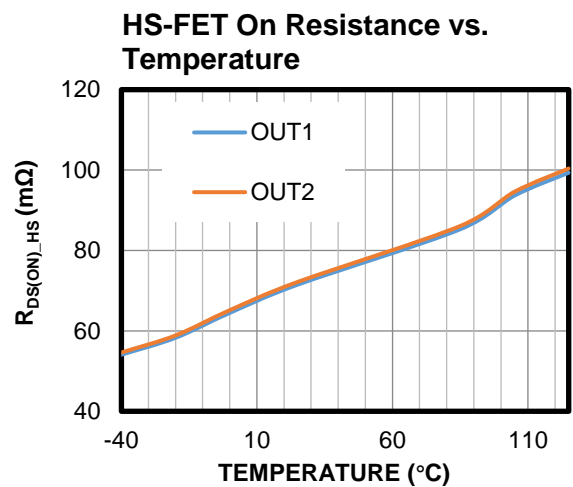
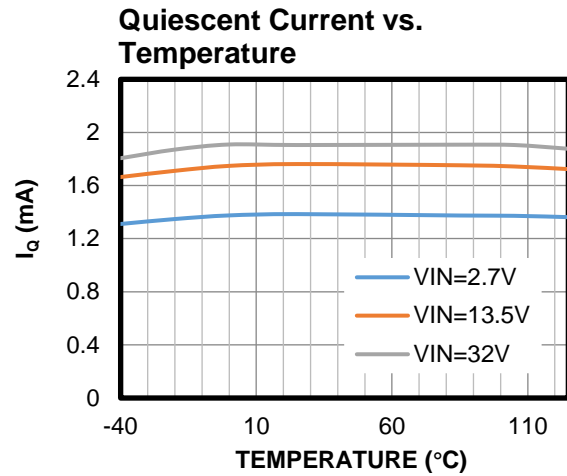
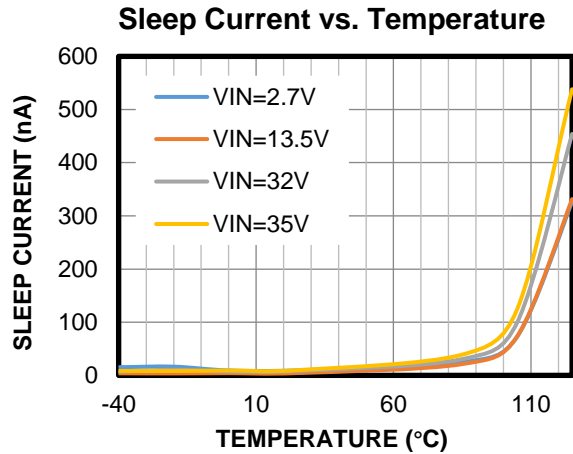
Parameters	Symbol	Condition	Min	Typ	Max	Units
<b>Input Supply Voltage</b>						
Input supply voltage ( $V_{IN}$ ) operating range	$V_{IN}$		2.7		28	V
Turn-on threshold	$V_{IN\_ON}$	$V_{IN}$ rising edge		2.5	2.65	V
Turn-on hysteretic voltage	$V_{IN\_HYS}$			0.15		V
<b>IC Supply</b>						
Shutdown current	$I_{IN\_SD}$	EN = 0			1	$\mu A$
Quiescent current	$I_Q$	EN = 1, no load current		1.6	2.2	mA
VCC regulator voltage	$V_{CC}$	$V_{IN} > 5.2V$	4.5	5	5.5	V
VCC regulator drop output voltage		$V_{IN} < 5V$ , 20mA load		100		mV
<b>Logic</b>						
Logic high threshold	$V_{IH}$				1.5	V
Logic low threshold	$V_{IL}$		0.4			V
IC start-up delay	$t_{DELAY}$	EN active to switching		230	350	$\mu s$
<b>Current Control</b>						
Current trip voltage	$V_{ITRIP}$	$V_{ITRIP} = 200mV$	180	200	225	mV
		$V_{ITRIP} = 100mV$	85	100	120	mV
Off time	$t_{ITRIP}$	After $I_{TRIP}$		1		ms
<b>Switching Frequency</b>						
IN1/IN2 PWM frequency	$f_{PWM}$				200	kHz
<b>Power MOSFET</b>						
High-side MOSFET (HS-FET) on resistance	$R_{DS(ON)\_HS}$	$T_J = 25^{\circ}C$	42	65	93	m $\Omega$
		$T_J = -40^{\circ}C$ to $+125^{\circ}C$			135	m $\Omega$
Low-side MOSFET (LS-FET) on resistance	$R_{DS(ON)\_LS}$	$T_J = 25^{\circ}C$	42	65	93	m $\Omega$
		$T_J = -40^{\circ}C$ to $+125^{\circ}C$			140	m $\Omega$
Minimum on time	$t_{MIN\_ON}$			200		ns
<b>Bootstrap (BST) for High-Side (HS) Driver</b>						
Forward voltage for BST charge	$V_{FBST}$			0.5		V
BST under-voltage lockout (UVLO) threshold	$V_{BST\_UVLO}$	Rising edge		2		V
<b>Protections</b>						
Over-current (OC) retry time	$t_{OCP}$		0.8	1		ms
OC threshold	$I_{OCP}$		6.5	10		A
Input over-voltage (OV) threshold	$V_{INOV}$		29	31	33	V
Thermal shutdown <sup>(5)</sup>	$T_{SD}$			150		$^{\circ}C$
Thermal shutdown hysteresis <sup>(5)</sup>	$T_{SD\_HY}$			20		$^{\circ}C$

**Note:**

5) Not tested in production.

## TYPICAL CHARACTERISTICS

$V_{IN} = 13.5V$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

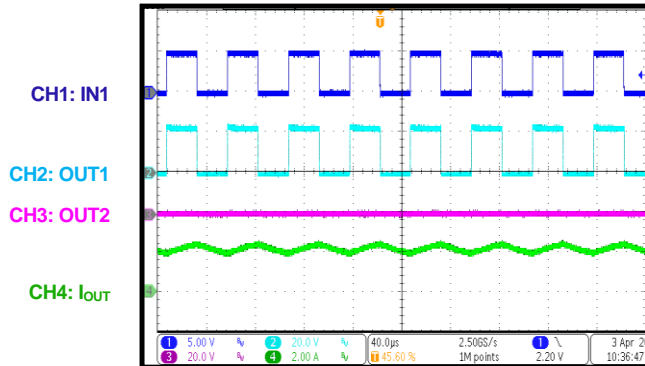


## TYPICAL PERFORMANCE CHARACTERISTICS

$V_{IN} = 24V$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

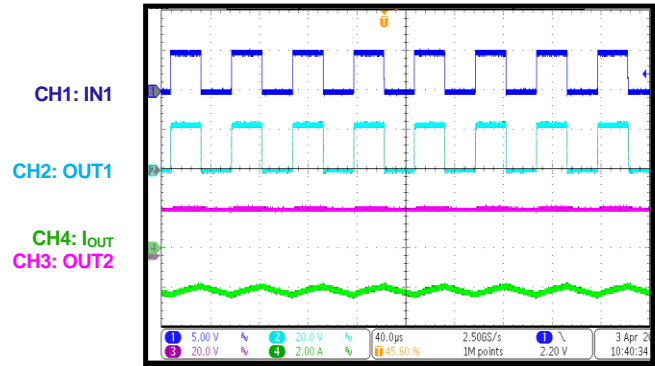
### Normal Operation

$V_{IN} = 24V$ ,  $IN1 = 20kHz/50\%$ ,  $IN2 = low$ ,  
load =  $5\Omega + 700\mu H$



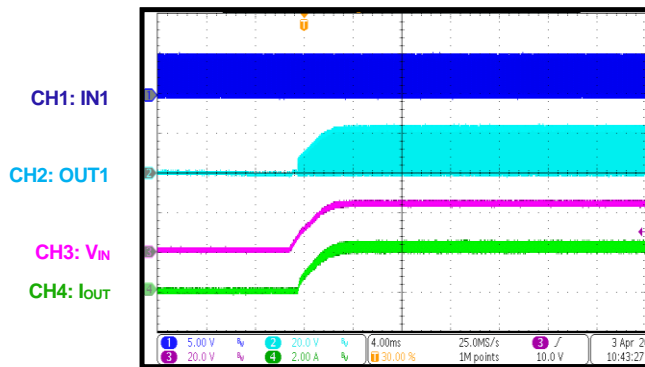
### Normal Operation

$V_{IN} = 24V$ ,  $IN1 = 20kHz/50\%$ ,  $IN2 = high$ ,  
load =  $5\Omega + 700\mu H$



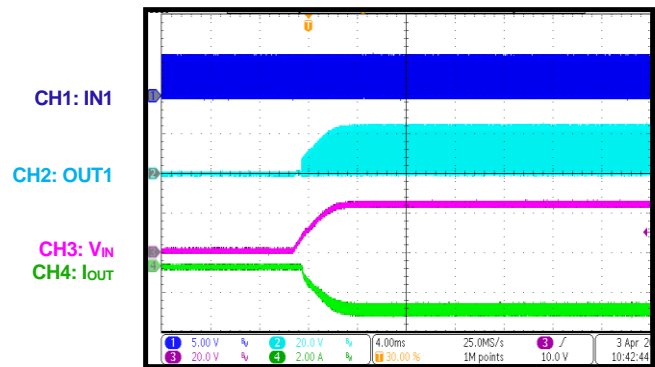
### Start-Up through VIN

$V_{IN} = 24V$ ,  $IN1 = 20kHz/50\%$ ,  $IN2 = low$ ,  
load =  $5\Omega + 700\mu H$



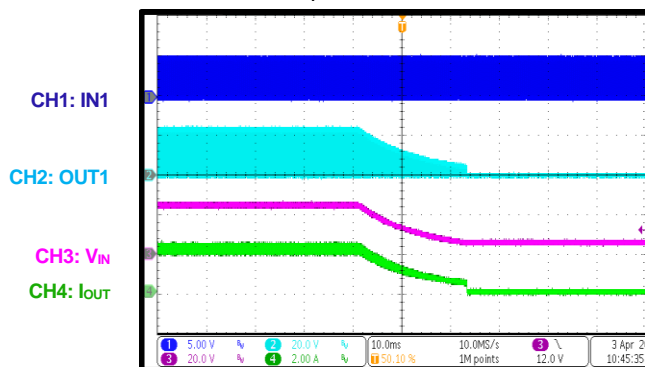
### Start-Up through VIN

$V_{IN} = 24V$ ,  $IN1 = 20kHz/50\%$ ,  $IN2 = high$ ,  
load =  $5\Omega + 700\mu H$



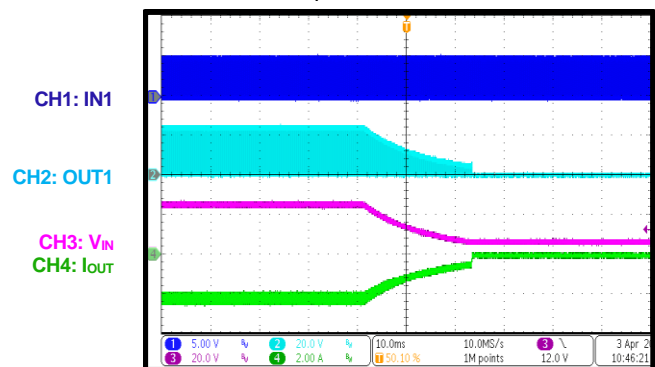
### Shutdown through VIN

$V_{IN} = 24V$ ,  $IN1 = 20kHz/50\%$ ,  $IN2 = low$ ,  
load =  $5\Omega + 700\mu H$

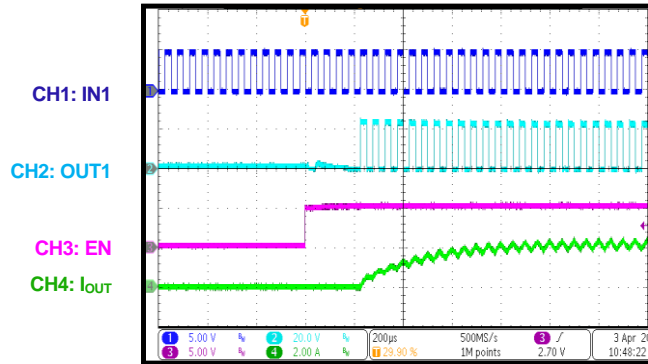
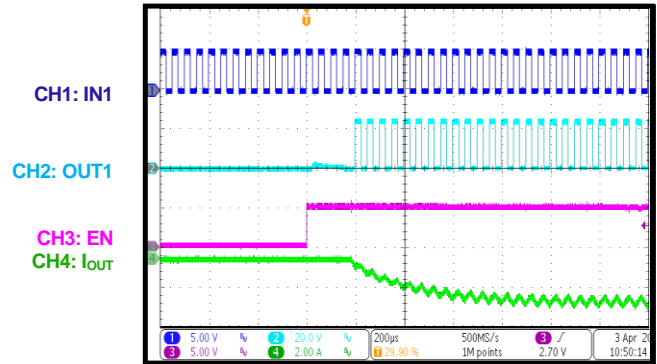
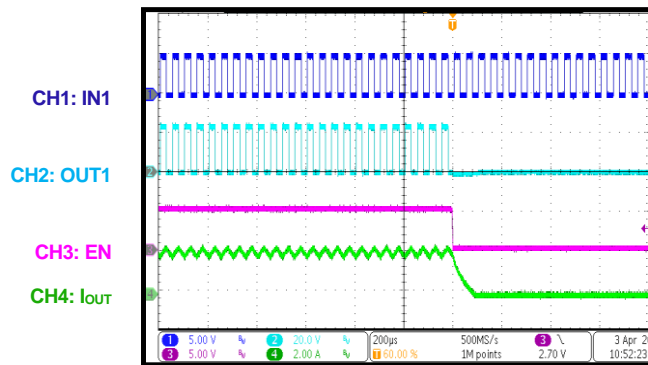
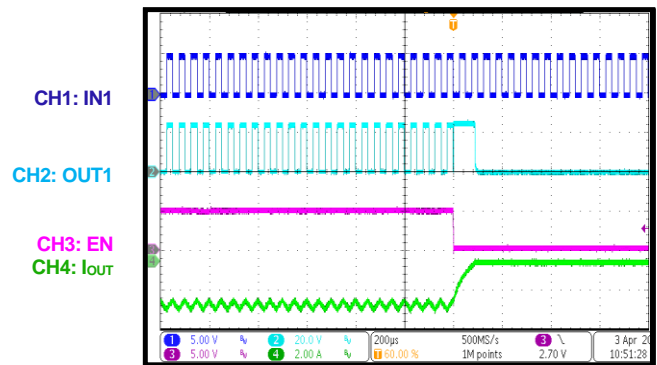


### Shutdown through VIN

$V_{IN} = 24V$ ,  $IN1 = 20kHz/50\%$ ,  $IN2 = high$ ,  
load =  $5\Omega + 700\mu H$



**TYPICAL PERFORMANCE CHARACTERISTICS (continued)**
 $V_{IN} = 24V$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

**IC Enabled**
 $V_{IN} = 24V$ ,  $IN1 = 20kHz/50\%$ ,  $IN2 = low$ ,  
load =  $5\Omega + 700\mu H$ 

**IC Enabled**
 $V_{IN} = 24V$ ,  $IN1 = 20kHz/50\%$ ,  $IN2 = high$ ,  
load =  $5\Omega + 700\mu H$ 

**IC Disabled**
 $V_{IN} = 24V$ ,  $IN1 = 20kHz/50\%$ ,  $IN2 = low$ ,  
load =  $5\Omega + 700\mu H$ 

**IC Disabled**
 $V_{IN} = 24V$ ,  $IN1 = 20kHz/50\%$ ,  $IN2 = high$ ,  
load =  $5\Omega + 700\mu H$ 


# FUNCTIONAL BLOCK DIAGRAM

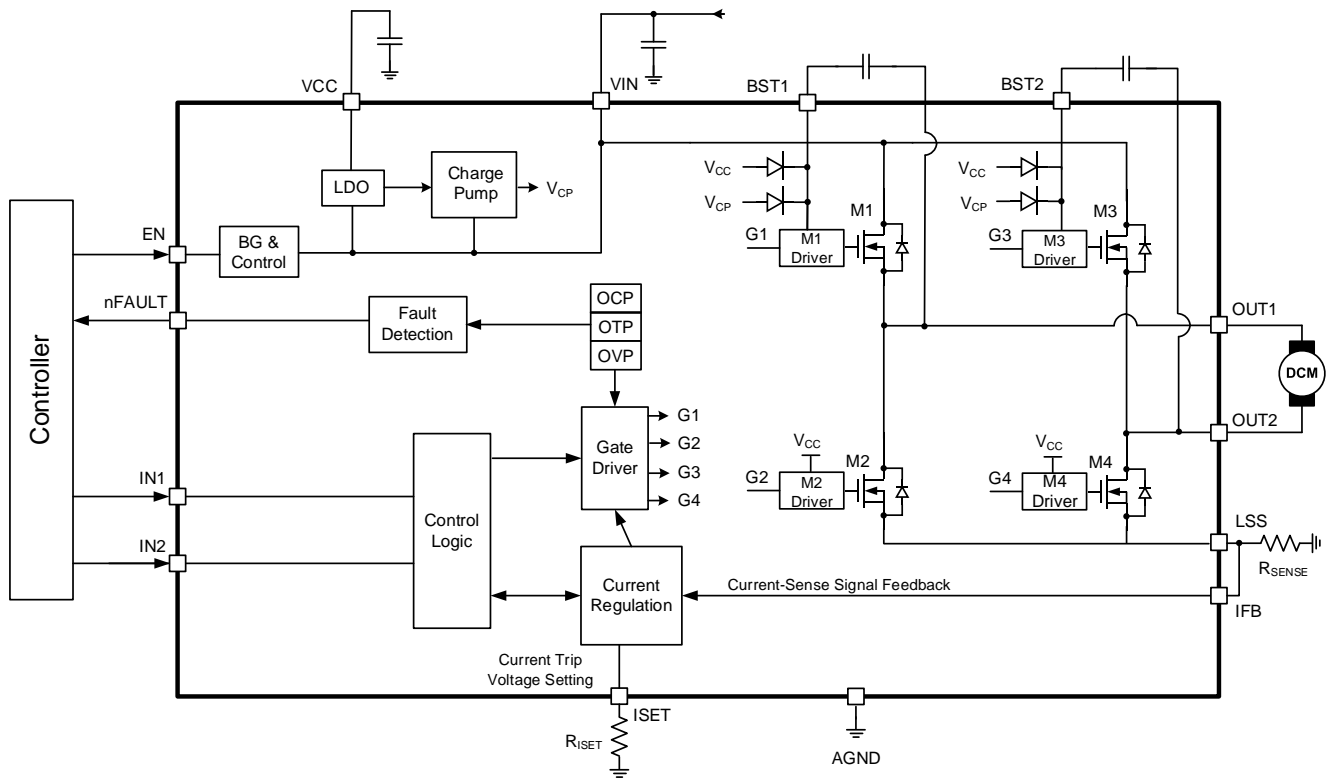


Figure 1: Functional Block Diagram

## OPERATION

The MPQ6619 is an H-bridge motor driver that operates from a 2.7V to 28V supply voltage ( $V_{IN}$ ) and achieves an output current ( $I_{OUT}$ ) of up to 5A. The MPQ6619 is ideal for driving a brushed DC motor.

### Input Logic

The MPQ6619 controls each half-bridge independently via the EN, IN1, and IN2 pins. Table 1 shows the input logic truth table for each pin.

**Table 1: Input Logic Truth Table**

EN	INx	OUTx
0	-	Z
1	0	L
1	1	H

### Shutdown Mode

If EN is pulled low, the MPQ6619 shuts down. In shutdown mode, all circuits and blocks are disabled, and the MPQ6619 consumes less than 1 $\mu$ A of shutdown current. To avoid mistripping, the EN pin has a 150ns deglitch time.

### Current Limit

The MPQ6619 has a configurable current limit. An external current-sense resistor ( $R_{SENSE}$ ) senses  $I_{OUT}$  flowing through the two low-side MOSFETs (LS-FETs). If  $I_{OUT}$  reaches the current trip threshold, a current limit condition is triggered. The entire H-bridge switches to a high-impedance (Hi-Z) state and all MOSFETs turn off. After a fixed off time ( $t_{TRIP}$ ), the MOSFETs are re-enabled and the cycle repeats.

The current limit is triggered when the IFB pin voltage ( $V_{IFB}$ ) reaches the current trip voltage ( $V_{ITRIP}$ ). For example, if  $I_{OUT}$  reaches 5A, a 40m $\Omega$   $R_{SENSE}$  is connected between the LSS pin and ground, and  $V_{ITRIP}$  is 200mV, then  $V_{IFB}$  reaches 200mV and a current trip occurs.

### Current Trip Voltage Setting

The current trip threshold is set via a resistor connected between ISET and GND ( $R_{ISET}$ ). When ISET is floating,  $V_{ITRIP}$  is set to 200mV by default. If  $R_{ISET}$  is connected between ISET and GND,  $V_{ITRIP}$  can fall below 200mV to reduce power loss on  $R_{SENSE}$ . The relationship between  $V_{ITRIP}$  and  $R_{ISET}$  can be calculated with Equation (1):

$$V_{ITRIP} = 0.2 \times \frac{40}{R_{ISET} \text{ (k}\Omega\text{)}} \quad (1)$$

For example, if  $R_{ISET}$  is 80k $\Omega$ ,  $V_{ITRIP}$  is 100mV. For improved accuracy, a 40k $\Omega$  to 80k $\Omega$  resistance is recommended to achieve a 200mV to 100mV  $V_{ITRIP}$ .

### Start-Up Sequence

When the IC starts up for the first time, there is a 0.3ms delay to detect whether a resistor is available on ISET. During this time, the IC is not switching.

### VCC LDO Regulator

The IC employs a low-dropout (LDO) regulator to provide a constant voltage (5V) at VCC. The VCC voltage ( $V_{CC}$ ) is the internal power supply for the logic and driver circuits. When  $V_{IN}$  drops,  $V_{CC}$  also drops. If  $V_{CC}$  falls below 4.8V, the IC triggers a power reset sequence and shuts down. Once  $V_{CC}$  exceeds 5.1V, the IC restarts and resumes normal operation.

### High-Side MOSFET (HS-FET) Driver

The two high-side MOSFETs (HS-FETs) (M1 and M3) are N-channel MOSFETs. When the HS-FETs turn on, they require a bootstrap (BST) supply voltage ( $V_{BSTx}$ ) across the BST1 and BST2 pins.  $V_{BSTx}$  is generated via the internal charge pump and a 5V  $V_{CC}$ . This allows the IC to operate at 100% duty cycle and provide sufficient driver voltage for the HS-FETs.

### Over-Current Protection (OCP)

OCP limits the current through each MOSFET by reducing the gate driver voltage to the MOSFET. If the MOSFET current exceeds the OCP threshold ( $I_{OCP}$ ) for longer than the OCP deglitch time, all MOSFETs in the H-bridge are disabled and nFAULT is pulled low. After an OCP retry time ( $t_{OCP}$ ), the driver restarts automatically.

### Input Over-Voltage Protection (OVP)

During the freewheeling time, the energy stored in the load current is delivered to the input side.

If  $V_{IN}$  and  $I_{OUT}$  are high enough, the energy sent back to the input side causes  $V_{IN}$  to increase. To avoid IC damage due to a high voltage spike, the IC employs  $V_{IN}$  protection.

If voltage applied to the VIN pin exceeds the OVP threshold, the H-bridge output is disabled and nFAULT is pulled low. Once  $V_{IN}$  drops to a safe level, the protection releases.

**Junction Over-Temperature Protection (OTP)**

If the die temperature exceeds safe limits (typically 150°C), all H-bridge MOSFETs are disabled and nFAULT is pulled low. Once the die temperature drops to a safe level (typically 130°C), the MPQ6619 restarts and resumes normal operation.

**Fault Indication Output (nFAULT)**

If any of the protection circuits are triggered, the nFAULT pin is pulled active low. These fault conditions include current limit trip, OCP, OTP, and OVP. The nFAULT pin is an open-drain output and requires an external pull-up resistor. Once the fault condition is removed, nFAULT is pulled inactive high via a pull-up resistor.

**Enable (EN) and Disable**

To enable the MPQ6619, EN is pulled high and the high-level signal time must exceed about 10 $\mu$ s. To shut down the IC, pull EN to logic low and set the low-level signal above 100ns.

## APPLICATION INFORMATION

### Selecting the Input Capacitor

The input capacitor ( $C_{IN}$ ) reduces the input supply surge current and switching noise. To prevent high-frequency switching current from passing through to the input, the  $C_{IN}$  impedance should be less than the input source impedance at the switching frequency ( $f_{SW}$ ). Ceramic capacitors with X5R or X7R dielectrics are recommended for their low ESR and small temperature coefficients. A higher-value capacitor is recommended for reducing  $V_{IN}$  ripple and noise.

For most applications, two 22 $\mu$ F ceramic capacitors in parallel are sufficient. It is recommended to connect one capacitor to each  $V_{IN}$  pin.

### Setting the Output Current limit

If a resistor is connected between the ISET and GND pins, the output current ( $I_{OUT}$ ) limit can be calculated with Equation (2):

$$I_{OUT} = 0.2 \times \frac{40}{R_{ISET} \text{ (k}\Omega\text{)}} \times \frac{1}{R_{SENSE} \text{ (}\Omega\text{)}} \quad (2)$$

If ISET is floating, then  $I_{OUT}$  limit can be calculated with Equation (3):

$$I_{OUT} = \frac{0.2}{R_{SENSE} \text{ (}\Omega\text{)}} \quad (3)$$

### Setting the Current-Sense Resistor

The current-sense resistor ( $R_{SENSE}$ ) power loss ( $P_{LOSS\_RIFB}$ ) can be calculated with Equation (4):

$$P_{LOSS\_RIFB} = \frac{V_{ITRIP}^2}{R_{SENSE} \text{ (}\Omega\text{)}} \quad (4)$$

To guarantee a current reference, it is recommended for the nominated  $R_{SENSE}$  power rating to be twice the calculated power loss with at least a 1% accuracy resistor.

### PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For the best results, refer to Figure 2 and follow the guidelines below:

1. Place the input capacitor ( $C_{IN}$ ) as close to the  $V_{IN}$ , VCC, and GND pins as possible.
2. Use a wide copper plane for the input, output, and GND connections to improve thermal performance.
3. Place as many GND vias as possible near the output and  $C_{IN}$  to improve thermal performance.
4. Keep the  $R_{SENSE}$  loop as short as possible.
5. Route the current-sense feedback signal far away from noise sources.

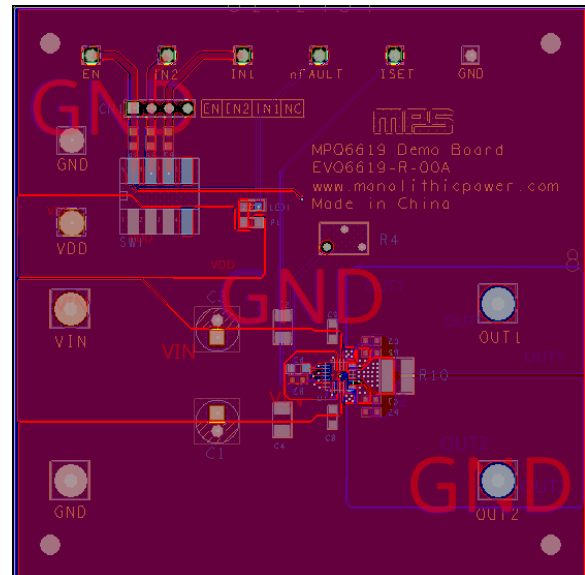


Figure 2: Recommended PCB Layout

### TYPICAL APPLICATION CIRCUIT

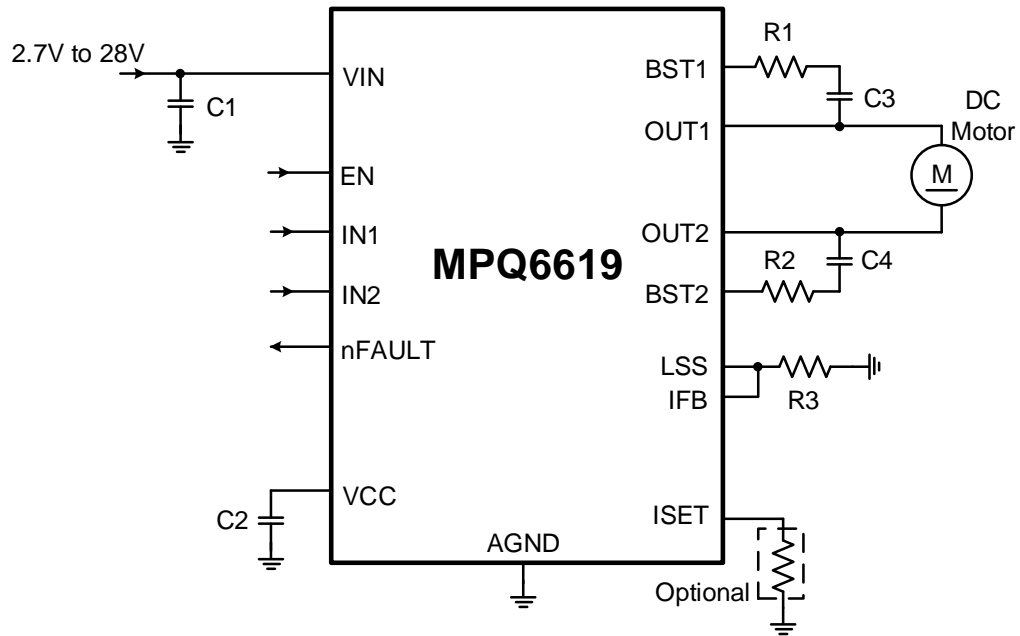
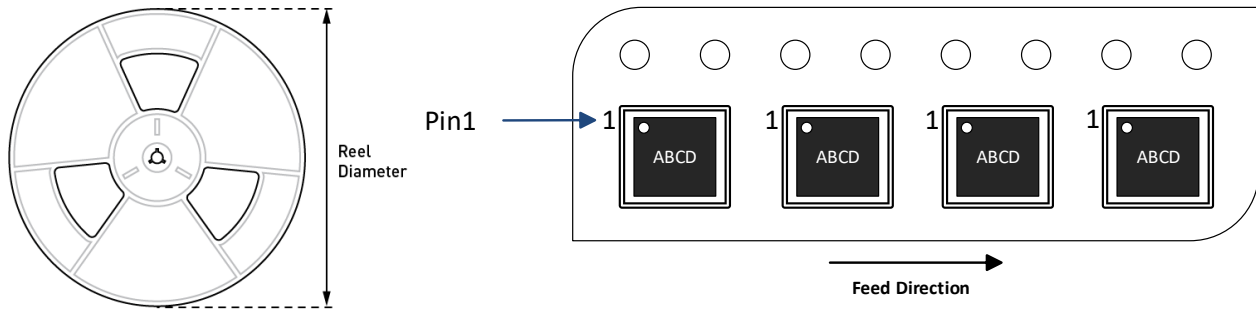


Figure 3: Typical Application Circuit



### CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ6619GRE-AEC1-Z	QFN-19 (4mmx4mm)	5000	N/A	N/A	13in	12mm	8mm

## REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	2/14/2025	Initial Release	-

**Notice:** The information in this document is subject to change without notice. Please contact MPS for current specifications. Users should warrant and guarantee that third-party Intellectual Property rights are not infringed upon when integrating MPS products into any application. MPS will not assume any legal responsibility for any said applications.