MPQ5862

16V, 1.5A, 90mΩ $R_{DS(ON)}$, Dual-Channel, High-Side Switch, AEC-Q100 Qualified

DESCRIPTION

The MPQ5862 is a dual-channel, smart, high-side power switch for a nominal current up to 1.5A per channel. The device covers a 5V to 16V input voltage (V_{INx}, where x = A or B) range. With a separate power supply design, the device supports two different input power rails. A back-to-back MOSFET configuration achieves up to 26V short-to-battery protection.

With a small 90mΩ on resistance ($R_{DS(ON)}$), the MPQ5862 provides a highly efficient, compact solution for camera load switch applications.

The device supports a configurable, high-accuracy current limit via the I^2C interface to clamp the inrush current under short-circuit conditions, which improves system reliability. A selectable start-up slew rate helps reduce the inrush current during start-up. In addition, a fast-off function can quickly turn off the device if the channel current increases sharply.

The MPQ5862 communicates to the MCU via the I^2C interface. The device supports up to 6 addresses set via an external resistor.

With the help of an internal analog-to-digital converter (ADC), the channel currents, supply voltages, reference voltage, and output voltages can be obtained without additional external circuitry. Full diagnostics and protection features are integrated, including input over-voltage (OV) and under-voltage (UV) detection, output OV detection for each channel, open-load and short-to-battery detection, over-current protection (OCP), short-circuit protection (SCP) with fast-off, and over-temperature protection (OTP) shutdown. Average/peak current detection improves diagnostic reliability in driver monitoring systems (DMS). The fault status can be reported via both the FT pin and I^2C interface.

The MPQ5862 provides well-developed monitoring and diagnostics via the internal ADC. Related safety documentation is also provided to aid functional safety design. The MPQ5862 is available in a tiny TQFN-17 (3mmx4mm) package, and is available in AEC-Q100 Grade 1.

FEATURES

- Designed for Automotive Applications
  - 5V to 16V Input Voltage (V_{INx}) Range
  - 26V Short-to-Battery Protection with Back-to-Back MOSFET
  - Available in AEC-Q100 Grade 1
- Cooler Thermals
  - 90mΩ On Resistance ($R_{DS(ON)}$) for Channels
- Reduces Board Size
  - Available in a TQFN-17 (3mmx4mm) Package with Wettable Flanks
- High-Accuracy Current-Sense Capability
  - ±3% at 2A
- Extends Vehicle Battery Life
  - Low 5μA Standby Current
- Vast Flexibility
  - Separate Power Supply Design Supports Two Power Rails
  - Configurable Current Limit and Soft Start
- Full Diagnostics and Protections with I^2C Interface
  - Fault Reporting via the FT Pin and I^2C
  - I^2C Supports 6 Addresses
  - V_{INx} OV/UV, Output Voltage (V_{OUTx}) OV Detection
  - Open-Load and Short-to-Battery Detection
  - Peak and Real-Time Current Sensing
  - SCP and OTP for Each Channel
  - Compliant with AEC-Q100-012 Test Grade 1
- Functional Safety System Design Capable
  - MPSafe™ Compatible – Functional Safety Supporting Document Available

MPSafe™ Fusa Compatible

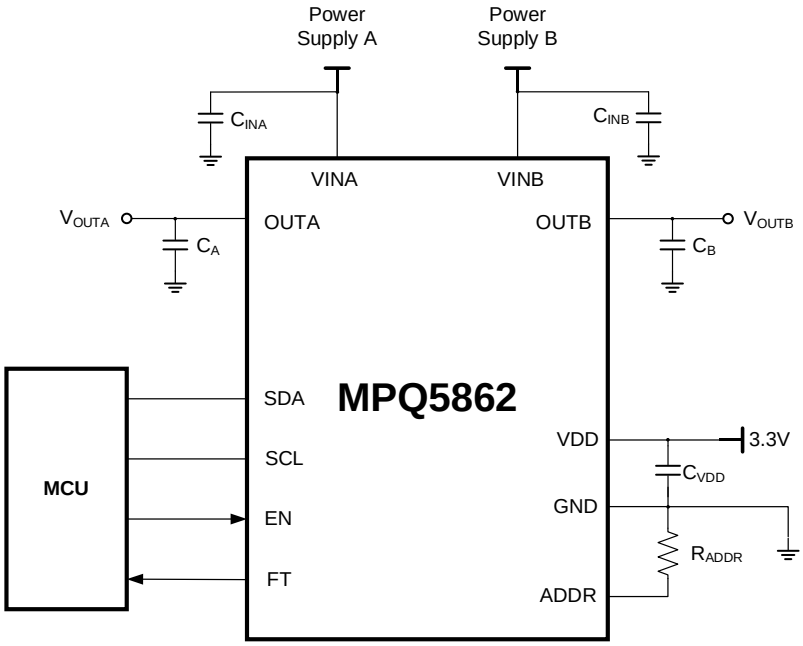
APPLICATIONS

- Cameras and Radars in Infotainment and ADAS Systems
- General Resistive and Capacitive Loads

All MPS parts are lead-free, halogen-free, and adhere to the RoHS directive. For MPS green status, please visit the MPS website under Quality Assurance. “MPS”, the MPS logo, and “Simple, Easy Solutions” are trademarks of Monolithic Power Systems, Inc. or its subsidiaries.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

TYPICAL APPLICATION



MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating**
MPQ5862GLTE-xxxx-AEC1***,****	TQFN-17 (3mmx4mm)	*See Below*	1

* For Tape & Reel, add suffix -Z (e.g. MPQ5862GLTE-xxxx-AEC1-Z).

** Moisture Sensitivity Level Rating

*** Wettable Flank

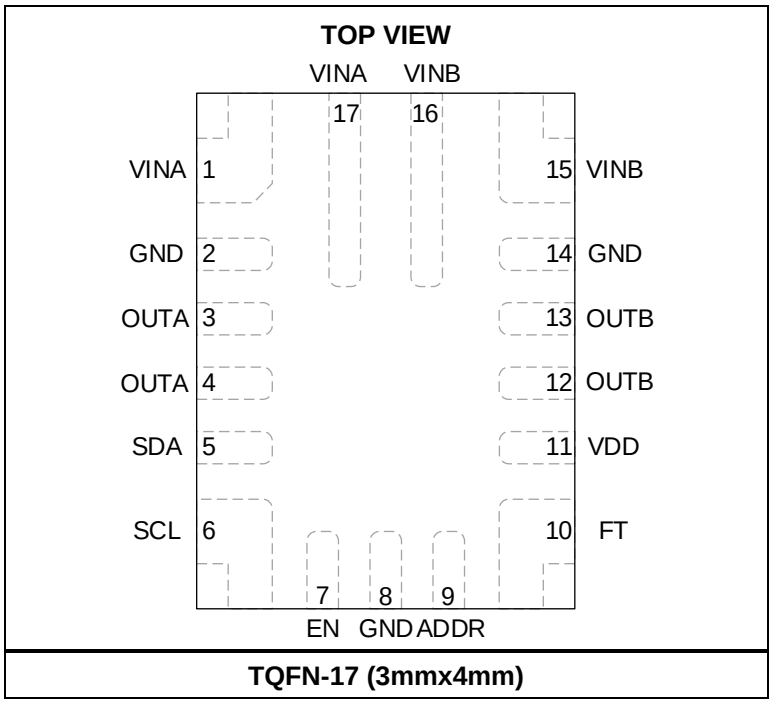
**** “xxxx” is the configuration code identifier for the register settings stored in the OTP register. Each “x” can be a hexadecimal value between 0 and F. The default device uses the “0000” code. Contact an MPS FAE to create this unique number.

TOP MARKING

MPYW
5862
LLL
E

MP: MPS prefix
Y: Year code
W: Week code
5862: Part number
LLL: Lot number
E: Wettable Flank

PACKAGE REFERENCE



TQFN-17 (3mmx4mm)

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

PIN FUNCTIONS

Pin #	Name	Description
1, 17	VINA	**Power supply A.** The VINA pins supply power to OUTA. Connect a minimum 1µF ceramic capacitor from VINA to GND.
2, 8, 14	GND	**Device ground.** Connect the GND pins together during PCB layout.
3, 4	OUTA	**Channel A load output.** Connect a 100nF ceramic capacitor from OUTA to GND.
5	SDA	**I^2C data input/output (I/O).**
6	SCL	**I^2C clock input.**
7	EN	**Enable.** Pull EN above the specified threshold (1.2V) to enable the chip. Pull EN below the threshold (0.9V) to shut down the chip. There is a 500kΩ pull-down resistor internally connected to the EN pin.
9	ADDR	**Address setting.** Connect a resistor from ADDR to GND to set the pin address. See Table 1 on page 19 for more details.
10	FT	**Fault output.** The FT pin's output is an open drain. If this pin is used, pull it up to an external power source through a pull-up resistor. When the device is enabled, this pin pulls low if a fault condition is detected. Float this pin if it is not used.
11	VDD	**Analog supply bypass.** Connect the VDD pin to a 3.3V power rail to supply the internal analog-to-digital converter (ADC) and logic circuit. Connect the VDD pin to GND with a 1µF bypass capacitor.
12, 13	OUTB	**Channel B load output.** Connect a 100nF ceramic capacitor from OUTB to GND.
15, 16	VINB	**Power supply B.** The VINB pins supply power to OUTB. Connect a minimum 1µF ceramic capacitor from VINB to GND. The VINA and VINB pins can be connected to different power supplies. If there is only one power rail, connect the VINB pins to the VINA pins.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

ABSOLUTE MAXIMUM RATINGS (1)

VINA/B, OUTA/B…….. -0.3V to +26.5V (2)
VINA/B to OUTA/B.....-26V to +26.5V (2)
EN.....-0.3V to +20V
All other pins.....-0.3V to +5V
Continuous power dissipation (3) (7) 4.5W
Junction temperature (T_J) .....150°C
Lead temperature .....260°C
Storage temperature..... -65°C to +150°C

ESD Ratings

Human body model (HBM) …….. Class 2 (4)
Charged-device model (CDM) …….Class C2b (5)

Recommended Operating Conditions

Supply voltage (V_{INx}).....5V to 16V
Nominal DC load current.....0A to 1.5A
Operating junction temp (T_J)…. -40°C to +150°C

Thermal Resistance θ_{JA} θ_{JC}

TQFN-17 (3mmx4mm) (6) …..68.7….6.4.…°C/W
EVQ5862-LT-00A (7) ……27.9…..……°C/W

Ψ_{JT}

TQFN-17 (3mmx4mm) (6)…..……...1.0…..°C/W
EVQ5862-LT-00A (7)…….....1.8.....°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) Absolute maximum ratings are rated under room temperature, unless otherwise noted. Exceeding these ratings may damage the device.
3) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) Per AEC-Q100-002.
5) Per AEC-Q100-011.
6) Obtained based on a JESD51-7, 4-layer PCB. The values given are only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application, and the value of θ_{Jc} shows the thermal resistor from junction-to-case bottom. The value of Ψ_{JT} shows the characterization parameter from junction-to-case top.
7) Measured on an MPS standard EVB, 2oz. copper thickness, 4-layer PCB. The value of Ψ_{JT} shows the characterization parameter from junction-to-case top.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS

V_{INA} = V_{INB} = 12V, V_{DD} = 3.3V, T_J = -40°C to +150°C, typical values are at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Operating and Supply Voltage						
VINA voltage (V_{INA})/VINB voltage (V_{INB}) over-voltage (OV) rising threshold	V_{INOV_R}		16	17	18	V
V_{INx} OV hysteresis	V_{OV_HYS}			0.5		V
V_{INx} under-voltage (UV) falling threshold	$V_{IN_UV_F}$	V_{INA} or V_{INB} < $V_{IN_UV_F}$, OUTA or OUTB shutdown		2.8	3.8	V
V_{INx} UV hysteresis	$V_{IN_UV_HYS}$			0.3		V
Recommended VDD voltage (V_{DD}) range	V_{DD_REC}		3		3.6	V
V_{DD} UV falling threshold	V_{DDUV_F}	V_{DD} < V_{DDUV_F}, device shutdown		2.6	2.9	V
V_{DD} UV hysteresis	V_{DDUV_HYS}			0.2		V
Operating Current						
Standby current	I_{STBY}	V_{INA} = V_{INB} = 12V, V_{EN} = 0V, T_J = 25°C		5	10	µA
		V_{INA} = V_{INB} = 12V, V_{EN} = 0V, T_J = -40°C to +150°C			28	µA
VINx quiescent current	$I_{Q\text{-}VINx}$	V_{INA} = 12V, V_{INB} = 0V (or V_{INA} = 0V, V_{INB} = 12V), V_{EN} = 2V		600	800	µA
VDD quiescent current	$I_{Q\text{-}VDD}$	V_{INA} = 12V, V_{INB} = 0V (or V_{INA} = 0V, V_{INB} = 12V), V_{EN} = 2V		1100	1600	µA
MOSFET Parameters						
Channel on resistance	$R_{DS(ON)}$	T_J = 25°C		90	110	mΩ
		T_J = -40°C to +150°C			200	mΩ
EN and FT						
EN logic high voltage	V_{EN_H}		1.0	1.2	1.4	V
EN logic low voltage	V_{EN_L}		0.7	0.9	1.1	V
EN voltage hysteresis	V_{EN_HYS}			300		mV
FT logic low voltage	V_{FT_L}	I_{FT} = 1mA			0.2	V
EN pull-down resistor	R_{EN_PU}			500		kΩ
Current Limit						
Current limit (8)	I_{LIMIT}		2.04	2.4	2.76	A
			1.53	1.8	2.07	
			0.935	1.1	1.265	
			0.35	0.5	0.65	
Soft short-circuit deglitch time	t_{SSC_DE}	Current limit triggered, channel shutdown after t_{SSC_DE}		0.5		ms
Short circuit recovery delay	t_{SC_RST}	Output short circuit shutdown, channel automatically recovers after this delay		300		ms

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS *(continued)*

V_{INA} = V_{INB} = 12V, V_{DD} = 3.3V, T_J = -40°C to +150°C, typical values are at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Diagnostics and Protections						
OUTx (OUTA or OUTB) OV threshold	V_{OOV_STD}	V_{OUTx} - V_{INx} > V_{OOV_STD}, channel shutdown	0.05	0.15	0.25	V
OUTx OV hysteresis	V_{OOV_HYS}			50		mV
OUTx OV deglitch time	t_{OOV_DE}			10		µs
Thermal shutdown threshold (9)	T_{SD}	T_J > T_{SD}, device shutdown		175		°C
Thermal shutdown hysteresis (9)	T_{SD_HYS}			25		°C
Thermal warning threshold (9)	T_{WR}	T_J > T_{WR}, thermal warning is detected via the I^2C interface		140		°C
Thermal warning hysteresis (9)	T_{WR_HYS}			25		°C
Analog-to-Digital Converter (ADC) Configuration						
Normal supply range	V_{DD_ADC}	ADC accuracy is ensured	3	3.3	3.6	V
Parameter-Sensing Accuracy (including ADC Error)						
V_{INx} and V_{OUTx} reading accuracy	ΔV/V		-3.5%		+3.5%	
VDD voltage (V_{DD}) reading accuracy	$\Delta V_{DD}/V_{DD}$		-4%		+4%	
OUTA, OUTB current reading accuracy	ΔI/I	I_{OUT} = 2A, T_J = 25°C	-3%		+3%	
		I_{OUT} = 2A, T_J = -40°C to +150°C	-6.25%		+6.25%	
		I_{OUT} = 600mA, T_J = 25°C	-5%		+5%	
		I_{OUT} = 600mA, T_J = -40°C to +150°C	-8.25%		+8.25%	
		I_{OUT} = 200mA, T_J = 25°C	-10%		+10%	
		I_{OUT} = 200mA, T_J = -40°C to +150°C	-20%		+20%	
		I_{OUT} = 60mA, T_J = -40°C to +150°C	-67%		+67%	

Notes:

8) Write to the relevant register to update this parameter.
9) Derived from bench characterization; not tested in production.

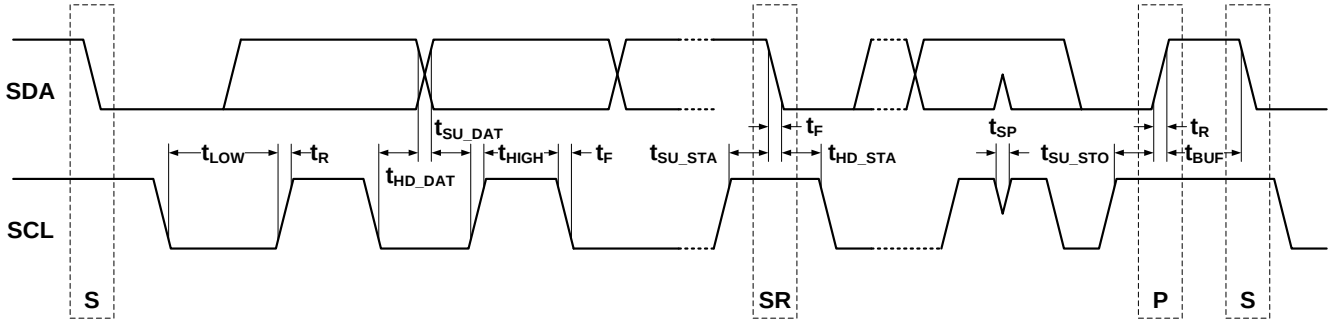
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS *(continued)*

V_{INA} = V_{INB} = 12V, V_{DD} = 3.3V, T_J = -40°C to +150°C, typical values are at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
I²C Configurations (9)						
Input logic high	V_{IH}		1.3			V
Input logic low	V_{IL}				0.5	V
Output logic low	V_{OL}				0.1	V
SCL clock frequency	f_{SCL}				1	MHz
SCL high time	t_{HIGH}		0.26			µs
SCL low time	t_{LOW}		0.5			µs
Data set-up time	t_{SU_DAT}		50			ns
Data hold time	t_{HD_DAT}		0			µs
Repeated start set-up time	t_{SU_STA}		0.26			µs
Repeated start hold time	t_{HD_STA}		0.26			µs
Bus free time between a stop and start command	t_{BUF}		0.5			µs
Stop set-up time	t_{SU_STO}		0.26			µs
SCL and SDA rise time	t_R				120	ns
SCL and SDA fall time	t_F		20 x (V_{DD} / 5.5V)		120	ns
Pulse width for suppressed spike	t_{SP}		0		50	ns
Capacitance for each bus line	C_B				550	pF

I²C-COMPATIBLE INTERFACE TIMING DIAGRAM



S: Start Command

SR: Repeated Start Command

P: Stop Command

Figure 1: I²C-Compatible Interface Timing Diagram

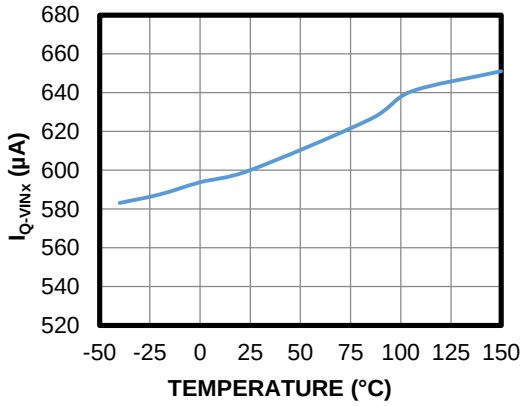
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

TYPICAL CHARACTERISTICS

V_{INA} = V_{INB} = 12V, V_{DD} = 3.3V, unless otherwise noted.

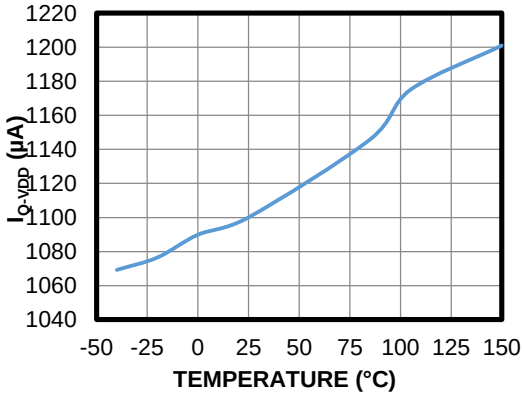
VINx Quiescent Current vs. Temperature

V_{INA} = 12V, V_{INB} = 0V, EN = 0V



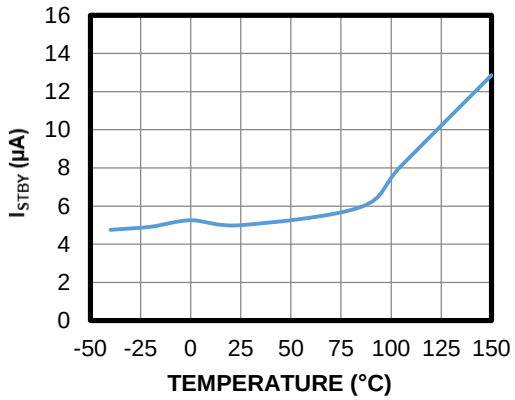
VDD Quiescent Current vs. Temperature

V_{INA} = 12V, V_{INB} = 0V, EN = 0V

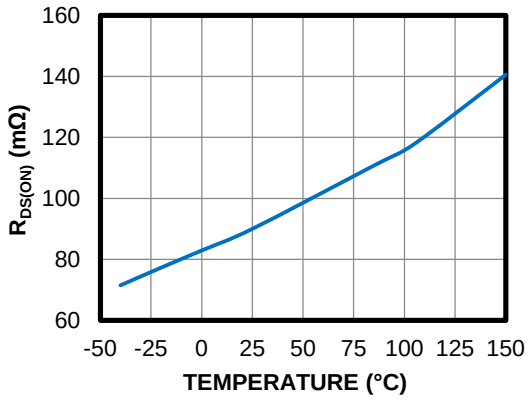


Standby Current vs. Temperature

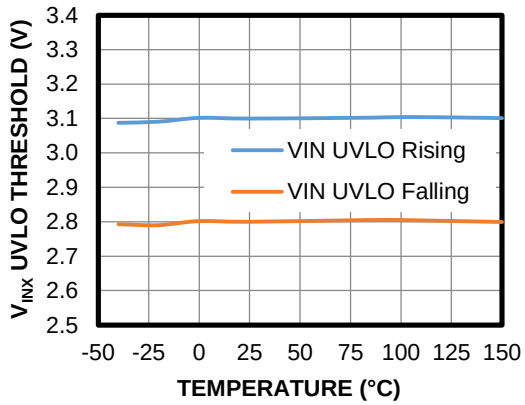
EN = 0V



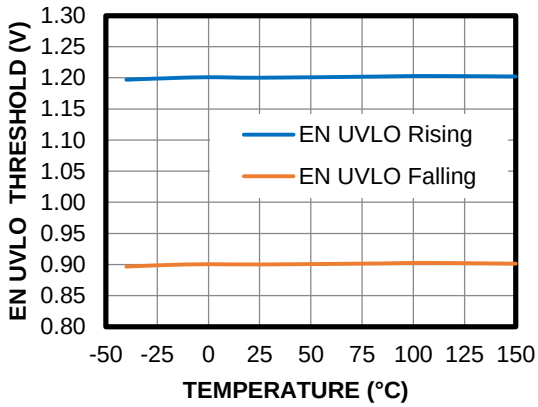
On Resistance vs. Temperature



V_{INx} UVLO Threshold vs. Temperature



EN UVLO Threshold vs. Temperature

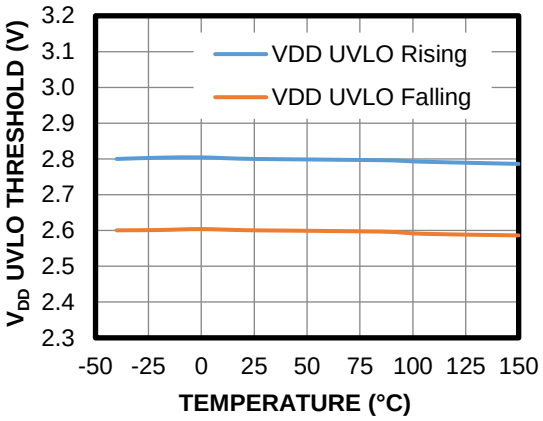


MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

TYPICAL CHARACTERISTICS *(continued)*

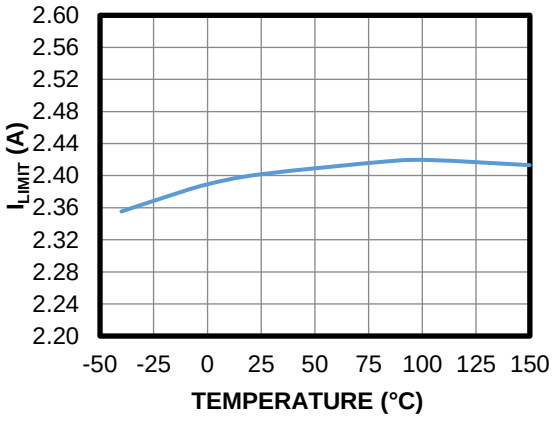
V_{INA} = V_{INB} = 12V, V_{DD} = 3.3V, unless otherwise noted.

V_{DD} UVLO Threshold vs. Temperature



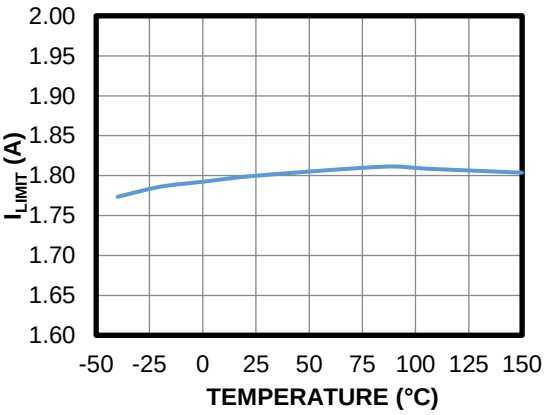
Current Limit vs. Temperature

OUTA current limit = 2.4A



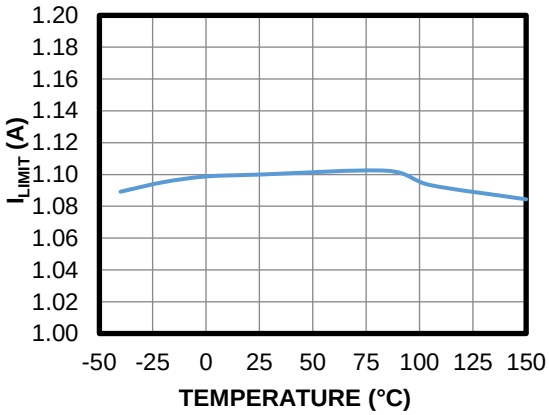
Current Limit vs. Temperature

OUTA current limit = 1.8A



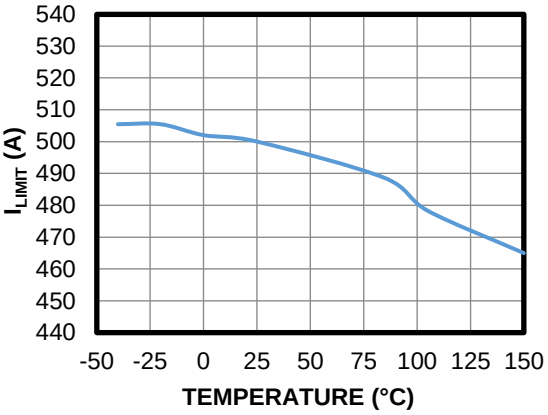
Current Limit vs. Temperature

OUTA current limit = 1.1A

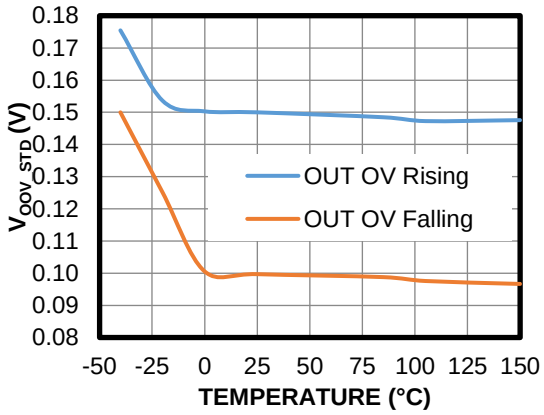


Current Limit vs. Temperature

OUTA current limit = 0.5A



OUTx Over-Voltage Threshold vs. Temperature



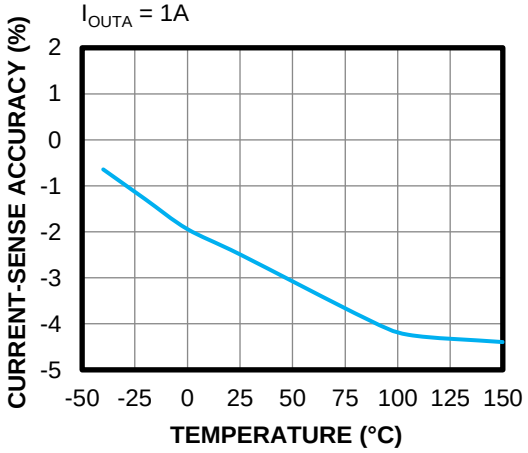
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

TYPICAL CHARACTERISTICS *(continued)*

V_{INA} = V_{INB} = 12V, V_{DD} = 3.3V, unless otherwise noted.

Current-Sense Accuracy vs. Temperature

I_{OUTA} = 1A

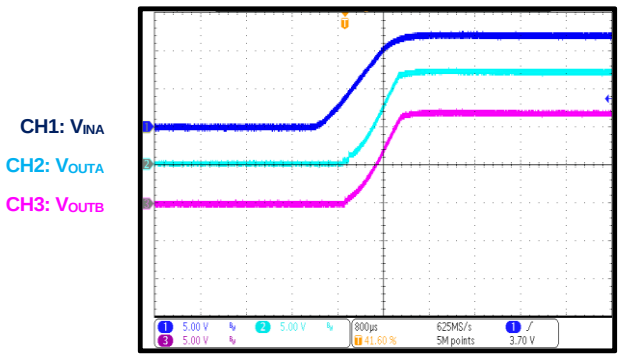


MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

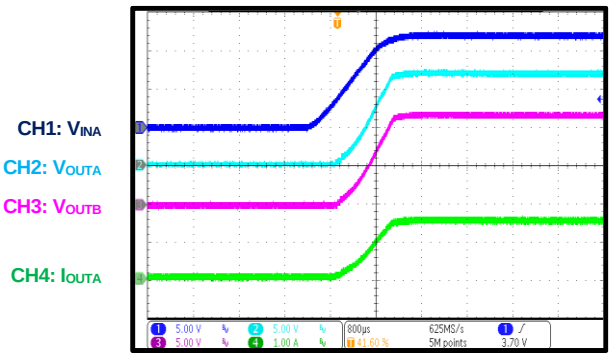
TYPICAL PERFORMANCE CHARACTERISTICS

V_{INA} = V_{INB} = 12V, V_{DD} = 3.3V, unless otherwise noted.

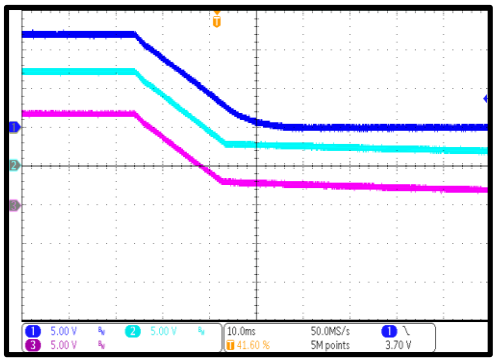
Start-Up through VINx
I_{OUTx} = 0A



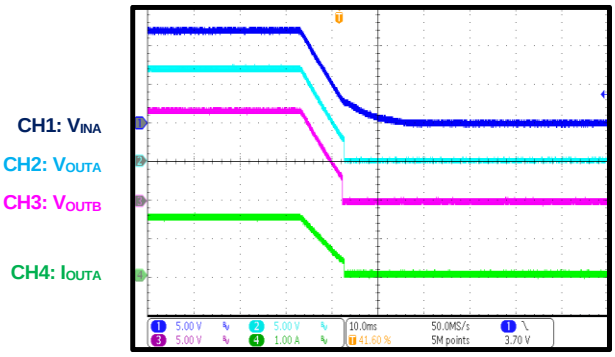
Start-Up through VINx
I_{OUTx} = 1.5A



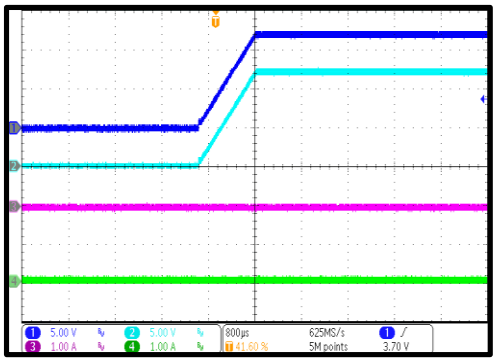
Shutdown through VINx
I_{OUTx} = 0A



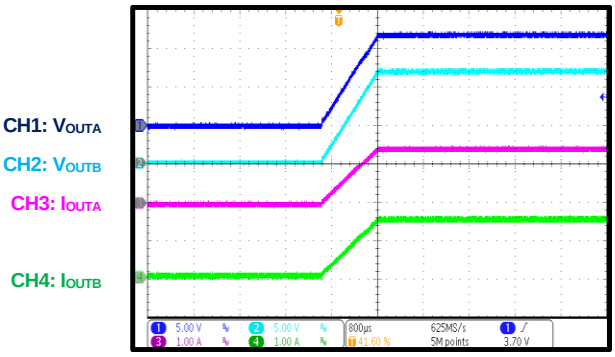
Shutdown through VINx
I_{OUTx} = 1.5A



Start-Up through EN Channel
I_{OUTx} = 0A



Start-Up through EN Channel
I_{OUTx} = 1.5A



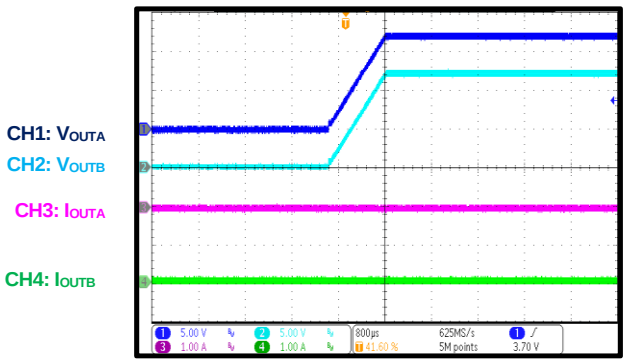
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{INA} = V_{INB} = 12V, V_{DD} = 3.3V, unless otherwise noted.

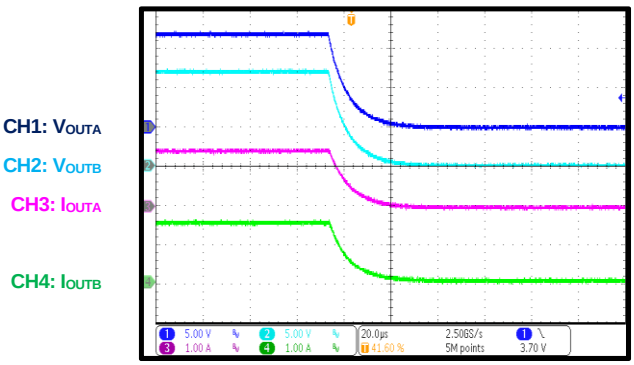
Shutdown through EN Channel

I_{OUTx} = 0A



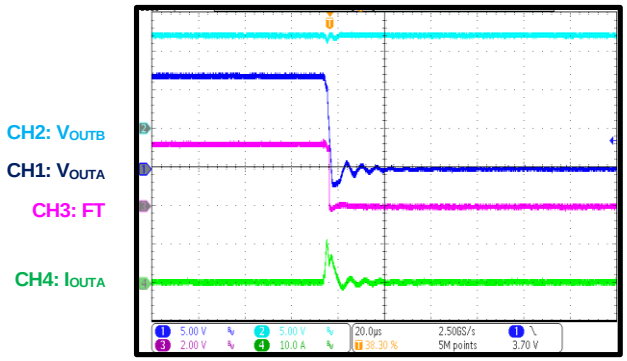
Shutdown through EN Channel

I_{OUTx} = 1.5A



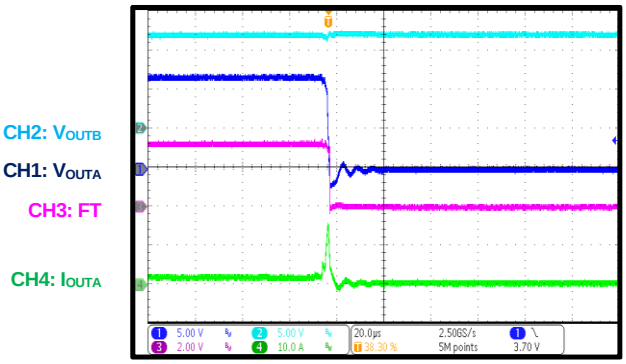
OUTA Short-Circuit Protection

I_{OUTx} = 0A



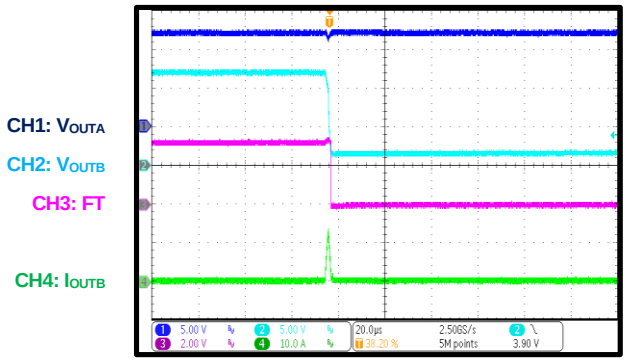
OUTA Short-Circuit Protection

I_{OUTx} = 1.5A



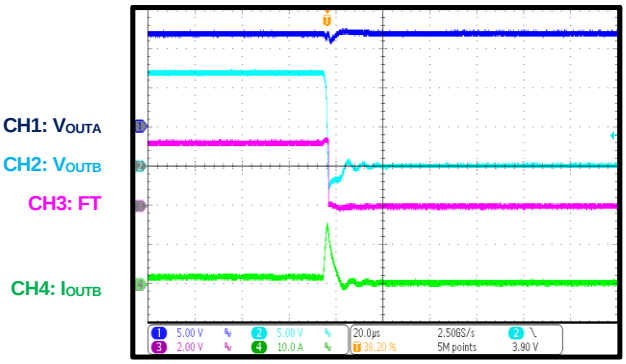
OUTB Short-Circuit Protection

I_{OUTx} = 0A



OUTB Short-Circuit Protection

I_{OUTx} = 1.5A



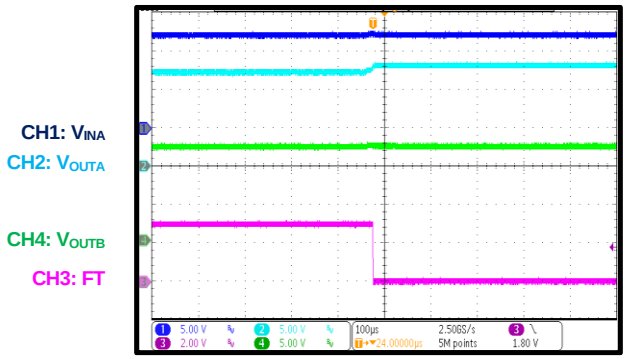
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{INA} = V_{INB} = 12V, V_{DD} = 3.3V, unless otherwise noted.

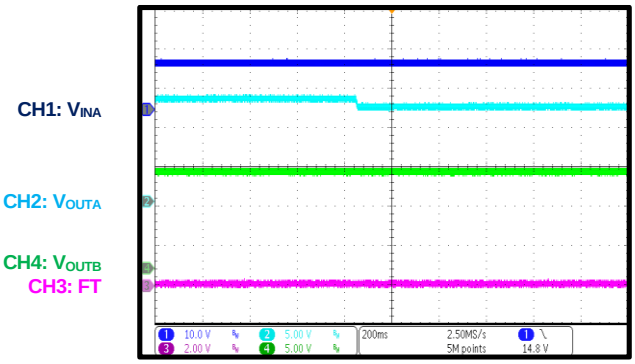
V_{OUTx} Over-Voltage Protection Entry

I_{OUTx} = 0A, V_{OUTA} OVP to 13V



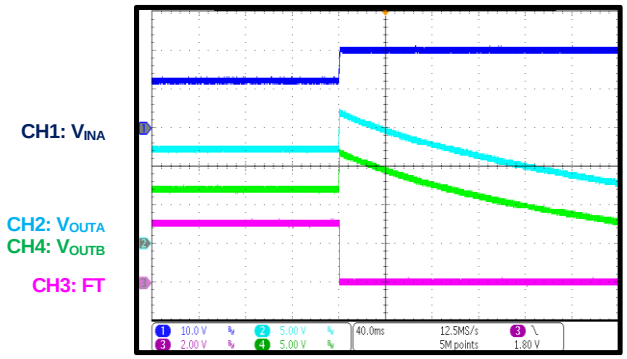
V_{OUTx} Over-Voltage Protection Recovery

I_{OUTx} = 0A, V_{OUTA} OVP to 13V



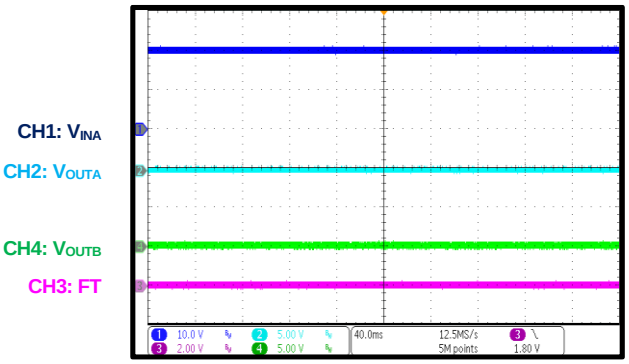
V_{INx} Over-Voltage Protection Entry

I_{OUTx} = 0A, V_{INA} and V_{INB} OVP to 20V



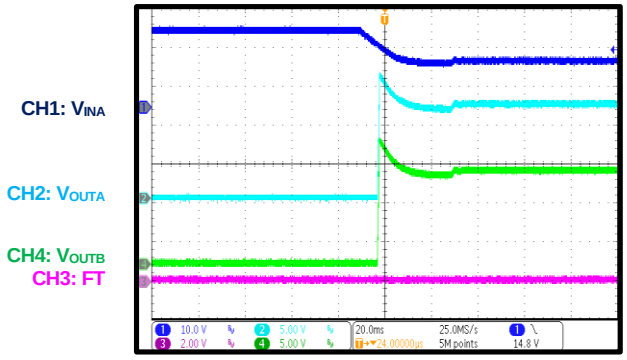
V_{INx} Over-Voltage Protection Steady State

I_{OUTx} = 0A, V_{INA} and V_{INB} OVP to 20V



V_{INx} Over-Voltage Protection Recovery

I_{OUTx} = 0A, V_{INA} and V_{INB} OVP to 20V



MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

FUNCTIONAL BLOCK DIAGRAM

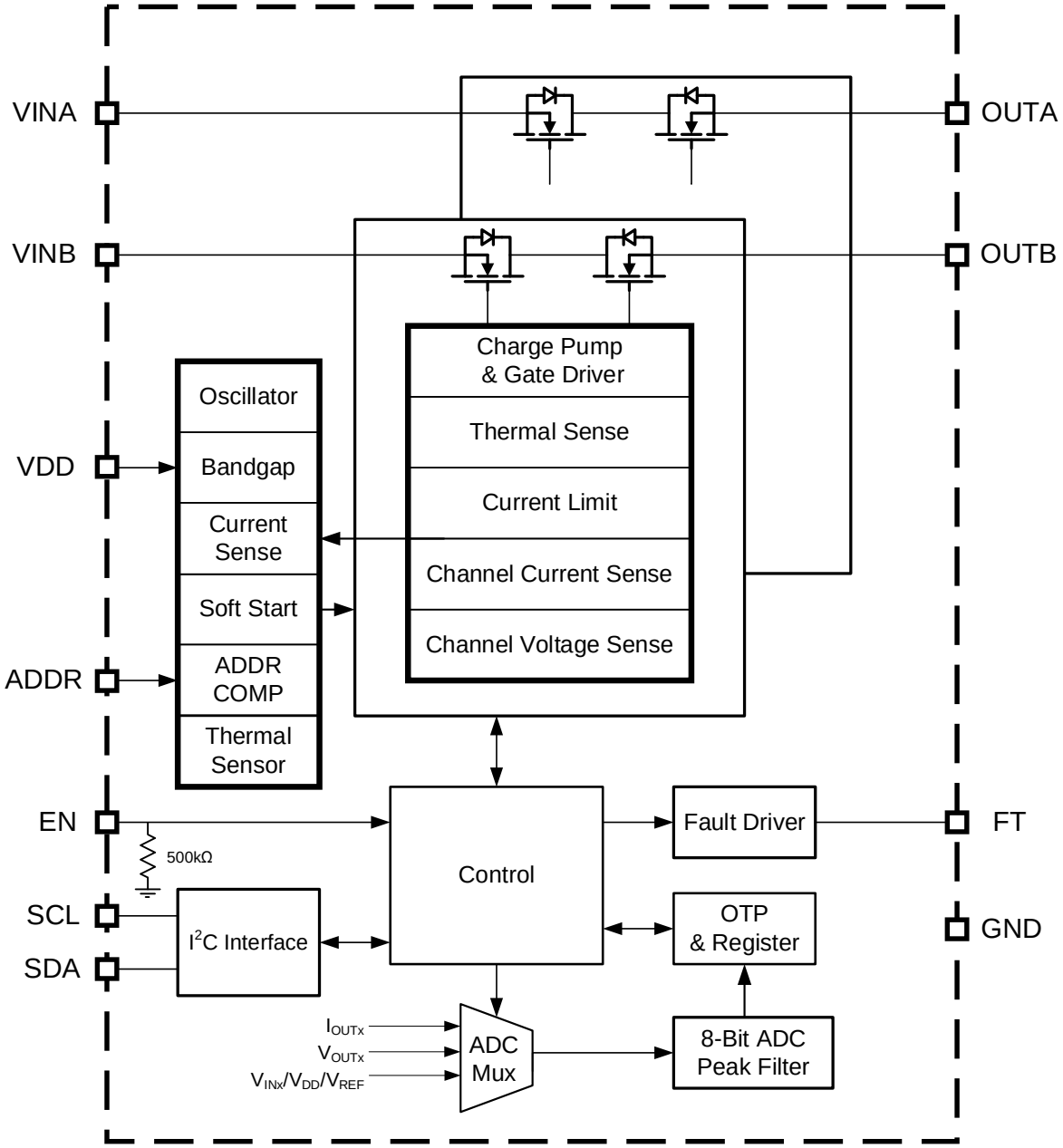


Figure 2: Functional Block Diagram

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

OPERATION

Separate Power Supplies

With a separate power supply design, the MPQ5862 supports two different power rails. OUTA is supplied by VINA, and OUTB is supplied by VINB.

When there is only one power rail, it is recommended to connect the VINA pins to the VINB pins.

Configurable Current Limit

The device has a configurable current limit (I_{LIMIT}), which can be set via I^2C. The default channel I_{LIMIT} is 2.4A, and the current limit options for the two channels are 2.4A, 1.8A, 1.1A, and 0.5A. A high-accuracy I_{LIMIT} can be configured via the I^2C to improve the device's reliability and provide protection from short-circuit or start-up conditions. In addition, this function allows the part to be used in low-current applications. The current limit during start-up and the recovery from over-current (OC) shutdown is only half of the set I_{LIMIT}.

When the load current reaches the set I_{LIMIT}, the output current (I_{OUT}) is regulated at the set limit. If this condition lasts for longer than 0.5ms, the channel shuts down to protect the load, and the device reports the fault via the I^2C and FT pin. If I_{OUT} increases sharply, the channel shuts down immediately (within 1µs) to protect the device.

Adjustable Start-Up Slew Rate

The start-up time can be set via the I^2C to reduce the inrush current during start-up. The options for the start-up time are 0.5ms, 1ms, 4ms, and 8ms. The default time is 1ms.

Internal 8-Bit Analog-to-Digital Converter (ADC)

An integrated, 8-bit analog-to-digital converter (ADC) provides thorough voltage and current information relevant to the device. This information includes the channel currents, input voltages (V_{INx}), reference voltage (V_{REF}), and output voltages (V_{OUTx}).

The ADC's operation mode can be set to continuously sense and update the registers. When the I^2C is triggered to save the quiescent current (I_Q), the operation mode can be set to only sense and update the registers once.

The MPQ5862 can also detect the peak channel current to provide a flexible diagnostic function for applications such as driver monitoring systems (DMS) (see Figure 3).

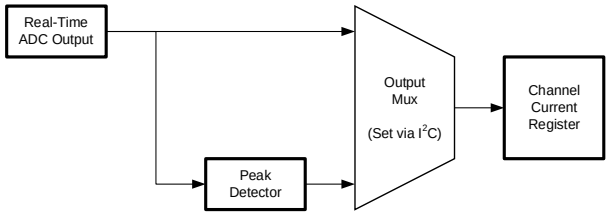


Figure 3: Current Information Options

Protections and Diagnostic Functions

The MPQ5862 provides comprehensive and flexible protection and diagnostic functions. The fault status can be reported via both the FT pin and the I^2C interface. The fault reporting function can be partially masked via the register setting (see the Register Map section starting on page 20 for more details).

The various protections and diagnostics are described below.

V_{INx} Over-Voltage Protection (OVP)

The device monitors the input voltages (V_{INx}, referring to both V_{INA} and V_{INB}) to protect the load and the device when V_{INx} exceeds V_{INOV_R} (typically 17V). If an over-voltage (OV) condition is detected while in the on state ($V_{INx} > V_{INOV_R}$), the corresponding output channel (OUTA or OUTB) shuts down and the FT pin asserts. When V_{Inx} falls below V_{INOV_RST} (typically 16.5V), the corresponding channel turns back on.

The FT pin's reporting feature can be masked via register FT_PIN_MASK_CONTROL (00h), bit[5]. When all the channels are off, V_{INx} over-voltage protection (OVP) can be enabled via register FT_PIN_MASK_CONTROL (00h), bit[7].

While in an off state (EN pin is low), the device can still report V_{INx} and whether there is an OV condition; if there is an OV condition, the corresponding channel(s) cannot turn on.

If the fault status has been removed, write 1 to register FT_PIN_MASK_CONTROL (00h), bit[0] to clear the fault register and de-assert the FT pin.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

V_{INx} Under-Voltage Protection (UVP)

While in the on state, if V_{INx} falls below the under-voltage (UV) threshold (V_{INUV_F}), then the corresponding output channel(s) turn off, and the status can be detected via the I^2C or FT pin. The FT pin's reporting feature can be masked via register FT_PIN_MASK_CONTROL (00h), bit[4].

While in the off state, if V_{INx} falls below V_{INUV_F}, the corresponding channel(s) cannot turn on.

Once the fault status has been removed, write 1 to register FT_PIN_MASK_CONTROL (00h), bit[0] to clear the fault register and de-assert the FT pin.

Short-to-GND and Over-Current Protection

The MPQ5862 features latch-off mode for short-to-GND and over-current protection (OCP). If I_{OUT} exceeds the current limit for longer than 0.5ms, the channel shuts down to protect the load, and the device reports the fault via the I^2C and FT pin. If I_{OUT} increases sharply, the channel shuts down immediately (within 1µs).

If short-to-GND or current-limit protection occurs, the part latches off. To recover from this state, the device must clear the fault register and the FT pin by cycling the power on VINA or VINB, or by reasserting the EN pin.

If the current limit is set high and a long coaxial cable is used in application, it is recommended to add an external diode from the GND pin to the OUT pins (OUTA and OUTB) to prevent the OUT pins from falling below -0.3V when the device is off. A 1N4148 diode is recommended.

Open-Load Detection

While in the on state, the microcontroller (MCU) detects open loads by reading the channel currents reported via the I^2C interface.

Short-to-Battery Detection (OUTx OVP)

The device monitors the output voltage on each channel (V_{OUTA} and V_{OUTB}). If V_{OUTx} exceeds the corresponding input voltage by about 0.15V (typically), the device turns off the channel and a fault is reported via the FT pin and I^2C register. If V_{OUTx} returns to the normal range, the device turns the channel back on automatically. The FT report feature can be masked via register FT_PIN_MASK_CONTROL (00h), bit[3].

Once the fault status has been removed, write 1 to register FT_PIN_MASK_CONTROL (00h), bit[0] to clear the fault register and de-assert the FT pin.

Thermal Protection

Thermal shutdown is implemented to prevent the chip from thermal runaway. The MPQ5862 has separate thermal protection for each channel. If the junction temperature (T_J) of one channel rises to the thermal shutdown threshold (T_{SD}, typically 175°C), the part shuts down and the FT pin is pulled down to report the fault. Once T_J falls to its lower threshold (typically 150°C), the device recovers automatically. Other channels are not impacted when a different channel experiences thermal protection. If a channel's temperature exceeds its lower threshold while in the off state, the corresponding channel(s) cannot turn on.

Once the fault status has been removed, write 1 to register FT_PIN_MASK_CONTROL (00h), bit[0] to clear the fault register and de-assert the FT pin.

If T_J of one channel exceeds the warning threshold (T_{WR}, typically 140°C), the device reports the thermal warning status via the I^2C until T_J falls to its lower threshold (typically 115°C). Meanwhile, the FT pin does not assert, and the other channels are not impacted.

AEC Q100-012 Test Grade A Certification

Short-circuit reliability is critical for smart high-side power switch devices. The AEC-Q100-012 standard is used to determine the reliability of the devices when operating under a continuous short-circuit condition. Different grade levels are specified according to the pass cycles.

This device is qualified with the highest level (Grade A), which 1 million times short-to-GND certification.

The applicable test modes are listed below:

1. Cold repetitive short-circuit test – long pulse
2. Cold repetitive short-circuit test – short pulse
3. Hot repetitive short-circuit test (continuous)

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

I²C INTERFACE

I²C Serial Interface Description

The I²C bus is a two-wire, bidirectional serial interface, consisting of a serial data line (SDA) and a serial clock line (SCL). The lines are externally pulled to V_{BUS} when they are idle. When connected to the line, a master device generates the SCL signal and device address, and arranges the communication sequence. The MPQ5862 works as a slave-only device, which supports up to 1Mbps of bidirectional data transfer in fast-mode, adding flexibility to the power supply solution. V_{OUTx}, the transition slew rate, and other converter parameters can be instantaneously controlled via I²C interface.

Data Validity

One clock pulse is generated for each data bit transferred. The data on SDA must be stable during the clock's high period. The SDA line's high or low state can only change when the clock signal on the SCL line is low (see Figure 4).

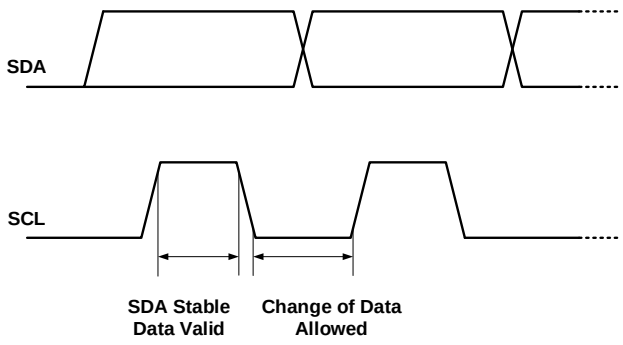


Figure 4: Bit Transfer on the I²C Bus

Start and Stop Commands

Start (S) and stop (P) commands are signaled by the master device, which signifies the beginning and the end of the I²C transfer. A start command is defined as the SDA signal transitioning from high to low while SCL is high. A stop command is defined as the SDA signal transitioning from low to high while SCL is high (see Figure 5).

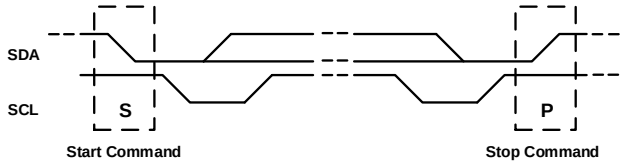


Figure 5: Start and Stop Commands

Data Transfer

Every byte put on SDA must be 8 bits long. Each byte must be followed by an acknowledge (ACK) bit. The acknowledge-related clock pulse is generated by the master. The transmitter releases the SDA line (high) during the acknowledge clock pulse. The receiver must pull down the SDA line during the acknowledge clock pulse, so that it remains stable (low) during the high period of the clock pulse.

Figure 6 shows the data transfer format. After the start command, a slave address is sent. This address is 7 bits long, followed by an 8th data direction bit. The data direction bit determines whether the transmission is a read (R) or write (W). A 0 indicates a write transmission, and a 1 indicates a read (a request for data). A data transfer is always terminated by a stop command, which is generated by the master device. However, if the master device still wishes to communicate on the bus, it can generate a repeated start (Sr) command and address another slave device without first generating a stop command.

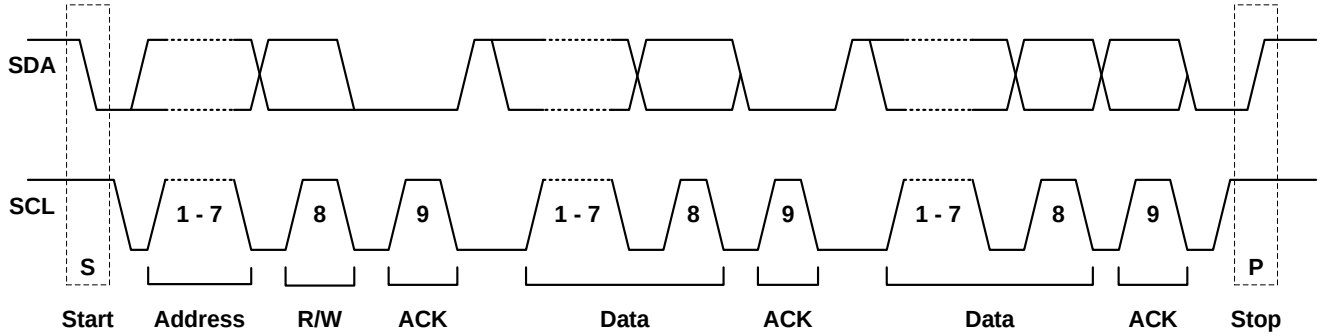


Figure 6: A Complete Data Transfer

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

Write Sequence

A typical MPQ5862 write sequence requires a start command from the master device, a valid slave address, a register index byte, and a corresponding data byte (see Figure 7).

After receiving each byte, the MPQ5862 acknowledges by pulling SDA low during the high period of a single clock pulse.

Read Sequence

A typical MPQ5862 read sequence requires a start command from the master device, followed by a valid slave address and a register index byte. Unlike with a write sequence, a start command from the master comes again (see Figure 8). The bus direction then turns around with the rebroadcast of the slave address, with bit 1 indicating a read cycle. The following 4th byte contains the data being returned by the MPQ5862. The value in this data byte reflects the value of the register index that was queried before.

Device Address

The MPQ5862's 7-bit address is set via a resistor connected between ADDR and GND. In this scenario, the I^2C address is based on the ADDR pin's voltage.

To ensure the resistance is effective within its lifetime, it is required to use a 1% accuracy resistor. The MPQ5862 checks the I^2C address during start-up. Once the I^2C address is determined, the address cannot be changed during operation unless the IC's power is reset.

Table 1 shows the recommended resistances, associated effective voltage range, and I^2C addresses.

Table 1: I^2C Address Setting

Recommended R_{ADDR}	I^2C R/W
Tie to GND	0x70
3.65kΩ	0x73
5.62kΩ	0x74
8.06kΩ	0x75
11.0kΩ	0x76
Float	0x77

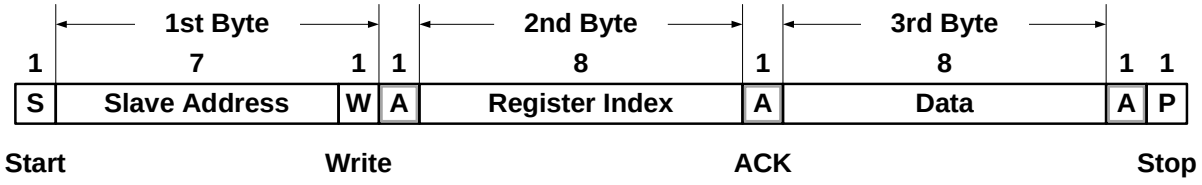


Figure 7: Write Sequence

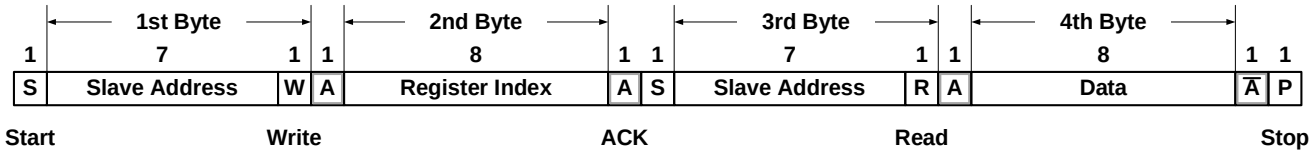


Figure 8: Read Sequence

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

REGISTER MAP

Table 2 and Table 3 show the MPQ5862's register description and register map. The registers are described in greater detail on the following pages.

Table 2: Register Description

Address	Register Description	Type	Power-On Reset
0x00	FT_PIN_MASK_CONTROL	R/W	0x82
0x01	GLOBAL_AND_CHANNEL_CONTROL	R/W	0xA0
0x02	CHANNEL_CURRENT_LIMIT_SETUP	R/W	0x00
0x03	CHANNEL_SOFT_ START_SETUP	R/W	0x55
0x04	ADC_CONTROL	R/W	0x00
0x05	GLOBAL_STATE_REPORT	R	0x00
0x06	CHANNEL_STATE_REPORT_I	R	0x00
0x07	CHANNEL_STATE_REPORT_II	R	0x00
0x08	ADC1	R	0x00
0x09	ADC2	R	0x00
0x0A	ADC3	R	0x00
0x0B	ADC4	R	0x00
0x0C	ADC5	R	0x00
0x0E	ADC6	R	0x00
0x14	ADC7	R	0x00
0x15	ADC8	R	0x00

Table 3: Register Mapping

Addr.	D7	D6	D5	D4	D3	D2	D1	D0
0x00	VINOVEN	RESERVED	VINOVM	VINUVM	OUTOVM	RESERVED	RESERVED	FTCLR
0x01	RESERVED				BEN	RESERVED	AEN	RESERVED
0x02	RESERVED		BCL		RESERVED		ACL	
0x03	RESERVED		BSS		RESERVED		ASS	
0x04	ADCCOV	ADCMD	PAPK	PBPK	RESERVED			
0x05	VINAOV	VINAUV	VINBOV	VINBUV	RESERVED			
0x06	ASC		BSC		AOT		BOT	
0x07	AOV		BOV		ACF		BCF	
0x08	ADC1							
0x09	ADC2							
0x0A	ADC3							
0x0B	ADC4							
0x0C	ADC5							
0x0E	ADC6							
0x14	ADC7							
0x15	ADC8							

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

FT_PIN_MASK_CONTROL (00h)

The FT_PIN_MASK_CONTROL command enables V_{INx} detection, OUT OV detection and masks the FT pin's reporting feature.

Bits	Access	Bit Name	Reset	Description
7	R/W	VINOVEN	1	This bit can only be set when all channels are off. 0: V_{INx} OV detection is disabled 1: V_{INx} OV detection is enabled; the part shuts down if $V_{INA/B}$ exceeds the threshold
6	R/W	RESERVED	0	Reserved.
5	R/W	VINOVM	0	0: The FT pin reports a V_{INx} OV condition 1: The FT pin does not report a V_{INx} OV condition
4	R/W	VINUVM	0	0: The FT pin reports a V_{INx} under-voltage (UV) condition 1: The FT pin does not report a V_{INx} UV condition
3	R/W	OUTOVM	0	0: The FT pin reports an OUT OV condition 1: The FT pin does not report an OUT OV condition
2:1	R/W	RESERVED	0	Reserved.
0	R/W	FTCLR	0	0: Normal operation 1: Write to clear the faults in all registers

GLOBAL_AND_CHANNEL_CONTROL (01h)

The GLOBAL_AND_CHANNEL_CONTROL command enables the channels.

Bits	Access	Bit Name	Reset	Description
7:4	R/W	RESERVED	1010	Reserved.
3	R/W	BEN	0	Enables channel B individually. Both the device EN and the channel's EN signal must be high to enable the channel. 0: Disabled 1: Enabled
2	R/W	RESERVED	0	Reserved.
1	R/W	AEN	0	Enables channel A individually. Both the device EN and the channel's EN signal must be high to enable the channel. 0: Disabled 1: Enabled
0	R/W	RESERVED	0	Reserved.

CHANNEL_CURRENT_LIMIT_SETUP (02h)

The CHANNEL_CURRENT_LIMIT_SETUP command sets the current limit (I_{LIMIT}) for each channel.

Bits	Access	Bit Name	Reset	Description
7:6	R/W	RESERVED	00	Reserved.
5:4	R/W	BCL	00	Sets the channel B I_{LIMIT}. 00: 2.4A 01: 1.8A 10: 1.1A 11: 0.5A
3:2	R/W	RESERVED	00	Reserved.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

1:0	**R/W**	**ACL**	**00**	**Sets the channel A I_{LIMIT}.** **00: 2.4A** **01: 1.8A** **10: 1.1A** **11: 0.5A**

CHANNEL_SOFT_ START_SETUP (03h)

The CHANNEL_SOFT_ START_SETUP command sets the soft-start time (t_{SS}) for each channel.

Bits	Access	Bit Name	Reset	Description
7:6	R/W	RESERVED	01	Reserved.
5:4	R/W	BSS	01	Sets the channel B t_{SS}. 00: 0.5ms 01: 1ms 10: 4ms 11: 8ms
3:2	R/W	RESERVED	01	Reserved.
1:0	R/W	ASS	01	Sets the channel A t_{SS}. 00: 0.5ms 01: 1ms 10: 4ms 11: 8ms

ADC_CONTROL (04h)

The ADC_CONTROL command controls the operation mode of the analog-to-digital converter (ADC); it can be set to continuously sense and update the registers, or to sense and update only once when the I^2C is triggered. This command can also set peak current detection to the past 1s or the real-time current for each channel.

Bits	Access	Bit Name	Reset	Description
7	R/W	ADCCOV	0	If ADCMD is set to 1, the user can set this pin to let the ADC convert for one cycle. Once the conversion is finished, this bit is set to 0 automatically, and the data in the I^2C registers (ADC1~ADC8) are valid for reading. 0: ADC conversion is complete; ready for I^2C reading 1: Start ADC conversion
6	R/W	ADCMD	0	0: Continuously update ADC1~ADC8 if VDD and EN are ready 1: The ADC starts conversion only when the I^2C sets ADCCOV to 1
5	R/W	PAPK	0	Selects whether the ADC reads the currents in parallel. 0: The ADC reads the channel's real-time current (A or B) 1: The ADC reads the channel's peak current (A or B) of the past 1s (the data is valid only when ADCCOV is set to 0)
4	R/W	PBPK	0	
3:0	R/W	RESERVED	0000	Reserved.

GLOBAL_STATE_REPORT (05h)

The GLOBAL_STATE_REPORT command reports the global state for over-voltage (OV) and under-voltage (UV) conditions; if the FT pin asserts, the relevant bit is read as 1.

Bits	Access	Bit Name	Reset	Description
7	R	VINAOV	0	0: No V_{INA} OV condition has been detected 1: A V_{INA} OV condition has been detected

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

6	**R**	**VINAUV**	**0**	**0: No V_{INA} UV condition has been detected 1: A V_{INA} UV condition has been detected**
5	R	VINBOV	0	0: No V_{INB} OV condition has been detected 1: A V_{INB} OV condition has been detected
4	R	VINBUV	0	0: No V_{INB} UV condition has been detected 1: A V_{INB} UV condition has been detected
3:0	R	RESERVED	0000	Reserved.

CHANNEL_STATE_REPORT_I (06h)

The CHANNEL_STATE_REPORT_I command reports the short-to-GND, over-current (OC), and over-temperature (OT) status for each channel.

Bits	Access	Bit Name	Reset	Description
7:6	R	ASC	00	Reports whether channel A is experiencing a short-to-GND or OCP fault. 00: No output short-to-GND or OCP fault has been detected 11: An output short-to-GND or OCP fault has been detected
5:4	R	BSC	00	Reports whether channel B is experiencing a short-to-GND or OCP fault. 00: No output short-to-GND or OCP fault has been detected 11: An output short-to-GND or OCP fault has been detected
3:2	R	AOT	00	00: No OT condition has been detected on channel A 11: An OT condition has been detected on channel A
1:0	R	BOT	00	00: No OT condition has been detected on channel B 11: An OT condition has been detected on channel B

CHANNEL_STATE_REPORT_II (07h)

The CHANNEL_STATE_REPORT_ II command reports whether an output over-voltage (OV) condition or thermal warning has occurred for each channel.

Bits	Access	Bit Name	Reset	Description
7:6	R	AOV	00	Indicates whether an output OV condition has been detected on the channel. 00: No output OV condition has been detected on the channel 11: An output OV condition has been detected on the channel
5:4	R	BOV	00	
3:2	R	ACF	00	Indicates whether a thermal warning has occurred. 00: No thermal warning has been detected 11: Thermal warning has been detected
1:0	R	BCF	00	

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

ADC1~ADC8 (08h~15h)

The ADC1~ADC8 commands read the following for all channels (A and B): V_{INx}, V_{REF}, and V_{OUTx}.

Bits	Access	Bit Name	Reset	Description
7:0	R	ADC1~ADC8	0000 0000	V_{INx} and V_{OUTx}: 75mV/LSB. V_{DD}: 20.8mV/LSB. V_{REF}: 5mV/LSB. Channel A and channel B current: 10mA/LSB. ADC1~ADC4: Returns the values for V_{INA}, V_{INB}, V_{DD}, and V_{REF}, respectively ADC5: V_{OUTA} ADC6: V_{OUTB} ADC7: Channel A current (real-time or peak) ADC8: Channel B current (real-time or peak)

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

APPLICATION INFORMATION

Functional Safety Compliance

As a functional safety compliant device, the MPQ5862 monitors its input/output voltages and channel currents. Contact an MPS FSE to obtain the related functional safety documentation. A multiple-pin design is applied for several pins (VINA, VINB and GND); this means that a single-point failure does not impact the device's operation, which improves device reliability.

Power-Over-Coaxial Cable

One of the MPQ5862's key applications is intended to be protecting power lines that supply remote cameras across a coaxial cable with concurrent data transmission. Figure 9 shows a system architecture diagram example.

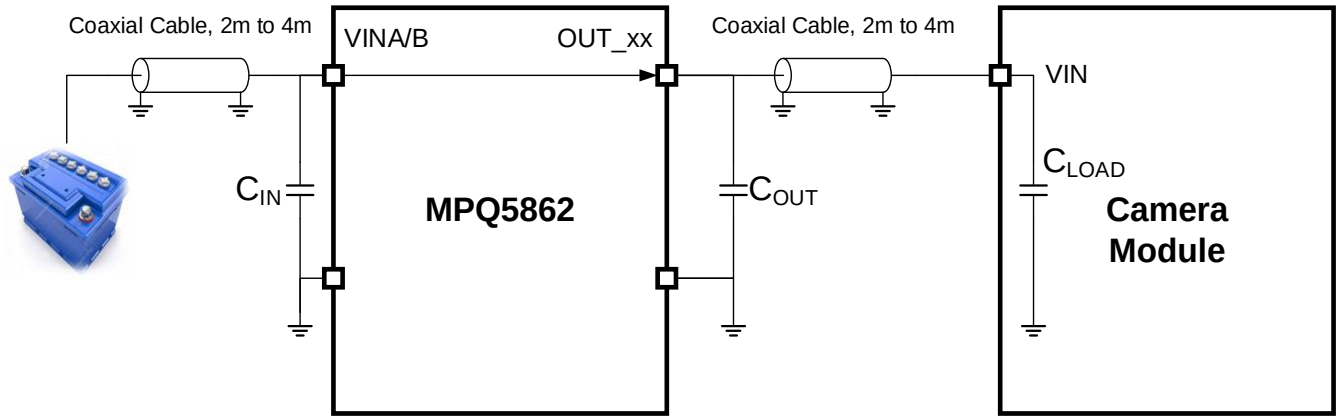


Figure 9: System Architecture Diagram Example

Figure 10 shows a typical application circuit for the MPQ5862.

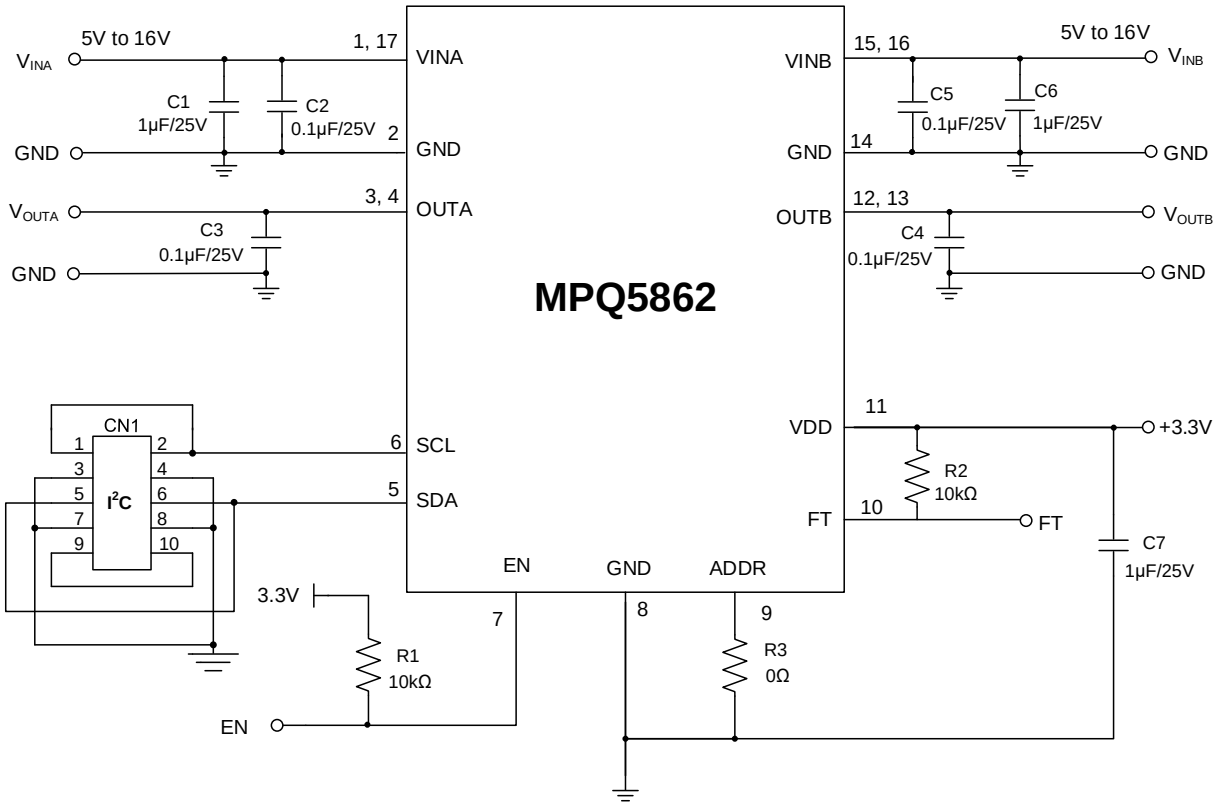


Figure 10: Typical Application Circuit

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

Table 4 shows the design guide index.

Table 4: Design Guide Index

Pin #	Pin Name	Component	Design Guide Index
1, 17	VINA	C1, C2	Selecting the Input Capacitors (VINA, Pins 1 and 17; VINB, Pins 15 and 16)
2, 8, 14	GND	-	Ground Connection (GND, Pins 2, 8, and 14)
3, 4	OUTA	C3	Selecting the Output Capacitor (OUTA, Pins 3 and 4; OUTB, Pins 12 and 13)
5	SDA	-	Digital Interface (SDA, Pin 5; SCL, Pin 6)
6	SCL	-	Digital Interface (SDA, Pin 5; SCL, Pin 6)
7	EN	R1	Enable (EN, Pin 7)
9	ADDR	R3	Selecting the I^2C Address (ADDR, Pin 9)
10	FT	R2	Fault Indicator (FT, Pin 10)
11	VDD	C5	Analog Supply Bypass (VDD, Pin 11)
12, 13	OUTB	C4	Selecting the Output Capacitor (OUTA, Pins 3 and 4; OUTB, Pins 12 and 13)
15, 16	VINB	C7, C8	Selecting the Input Capacitors (VINA, Pins 1 and 17; VINB, Pins 15 and 16)

Selecting the Input Capacitors (VINA, Pins 1 and 17; VINB, Pins 15 and 16)

For the best performance, it is recommended to use 1µF (or greater) ceramic capacitors with X5R or X7R dielectrics due to their low ESR and small temperature coefficients.

It is recommended to use another, lower-value capacitor (e.g. 0.1µF) with a small package size (e.g. 0603) to absorb high-frequency switching noise. Place the lower-value capacitor as close to the VINA, VINB, and GND pins as possible.

Selecting the Output Capacitor (OUTA, Pins 3 and 4; OUTB, Pins 12 and 13)

For the best performance, it is recommended to use a 0.1µF capacitor with a small package size (e.g. 0603) to absorb high-frequency switching noise. Place the capacitor as close to the OUTA, OUTB, and GND pins as possible.

Ground Connection (GND, Pins 2, 8 and 14)

See the PCB Layout Guidelines section on page 27 for more details.

Digital Interface (SDA, Pin 5; SCL, Pin 6)

The MPQ5862 works as a slave-only device that supports standard mode (100kbps), fast mode (400kbps), and fast-plus mode (1Mbps) bidirectional data transfer, adding flexibility to the power supply solution. The SCL and SDA lines are externally pulled to a bus voltage with a resistor (e.g. 1kΩ).

Enable (EN, Pin 7)

EN is a digital control pin that turns the device on and off. When the EN pin voltage exceeds 1.2V, the MPQ5862 turns on. To turn on the device, connect EN to a 3.3V power supply via a pull-up resistor (R1, which is recommended to be about 10kΩ.

Setting the I^2C Address (ADDR, Pin 9)

See Table 1 on page 19 for more details to set R3.

Fault Indicator (FT, Pin 10)

The FT pin is an open-drain output. If using the FT pin, connect it to a 3.3V power supply via a pull-up resistor (R2, which is recommended to be about 10kΩ). FT asserts low if a fault occurs.

Analog Supply Bypass (VDD, Pin 11)

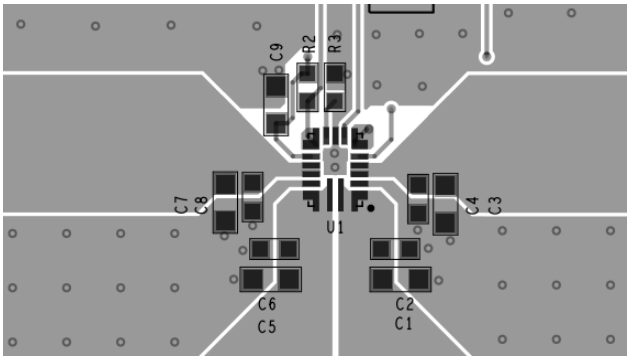
Connect the VDD pin to a 3.3V power rail to supply the internal ADC and logic circuit. Connect this pin to GND with a 1µF bypass capacitor (C5).

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

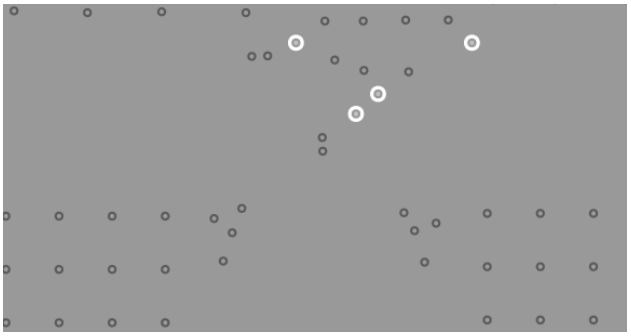
PCB Layout Guidelines (10)

Efficient PCB layout, especially input capacitor placement, is critical for stable operation. A 4-layer layout is strongly recommended to improve thermal performance. For the best results, refer to Figure 11 and follow the guidelines below:

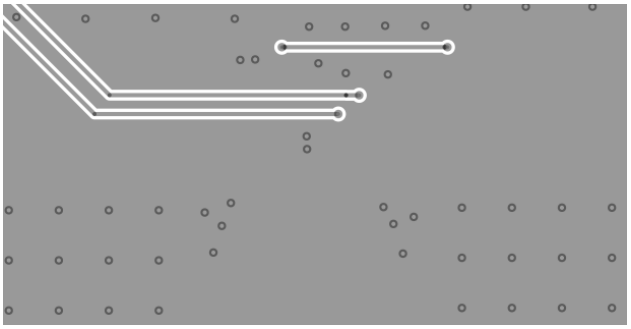
1. Use a large ground plane to connect the GND pin directly to ground.
2. Place the ceramic input capacitor, especially the small package size (0603) input and output bypass capacitors, as close to the VINA, VINB, OUTA, OUTB, and GND pins as possible to minimize noise.
3. Place the VDD capacitor as close to the VDD and GND pins as possible.
4. Use multiple vias to connect the power planes to the internal layers.



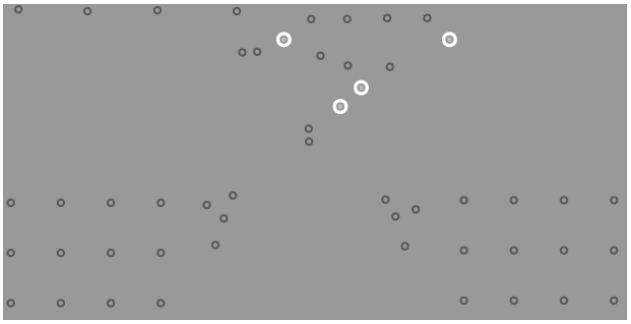
Top Layer



Mid-Layer 1



Mid-Layer 2



Bottom Layer

Figure 11: Recommended PCB Layout

Note:

10) The recommended PCB layout is based on Figure 12 on page 28.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

TYPICAL APPLICATION CIRCUIT

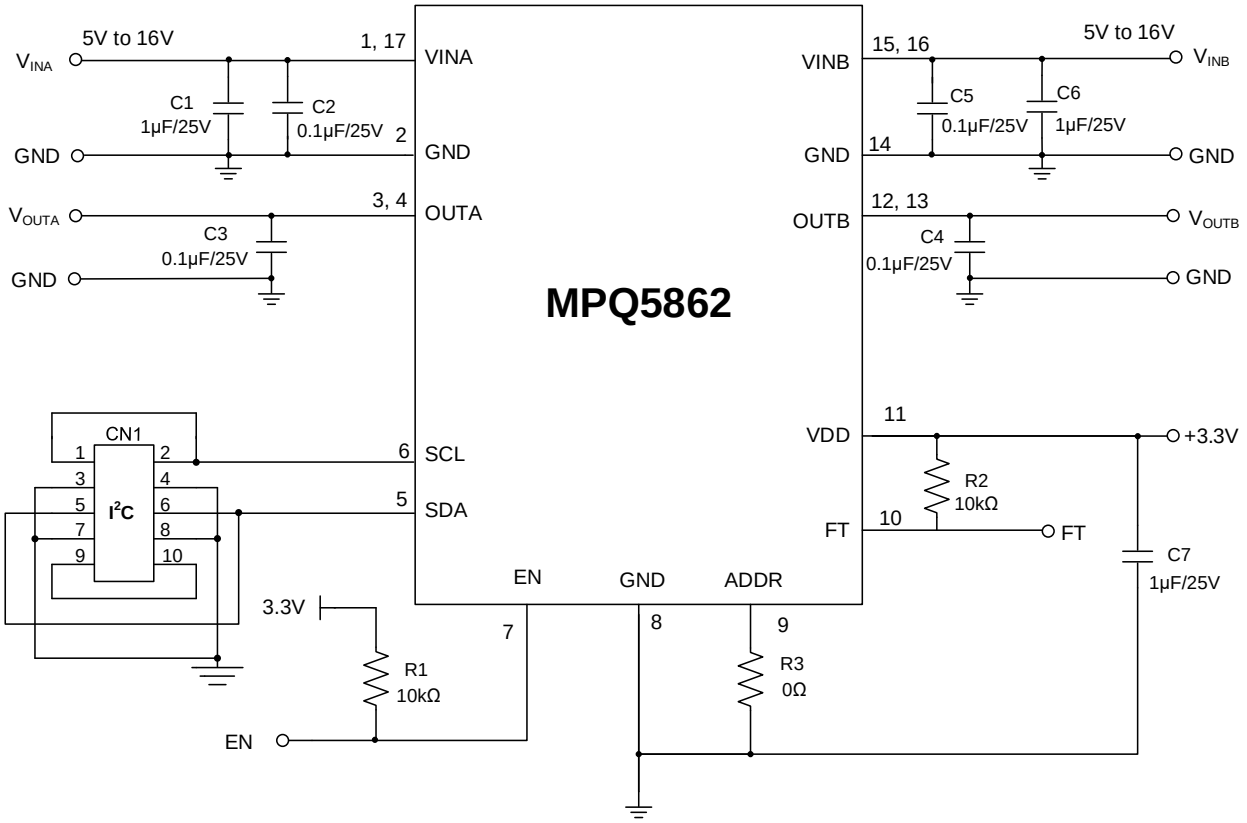
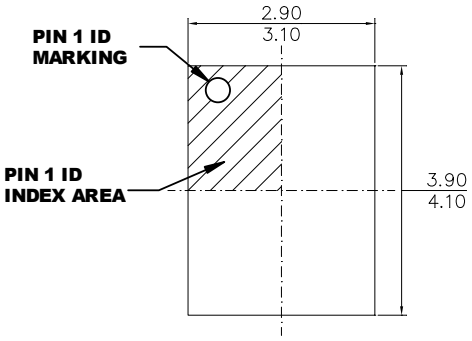


Figure 12: Typical Application Circuit

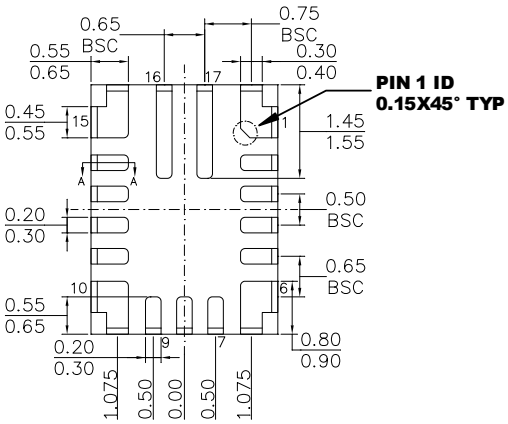
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

PACKAGE INFORMATION

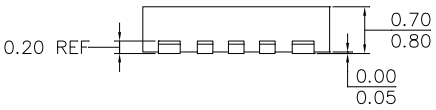
TQFN-17 (3mmx4mm)
Wettable Flank



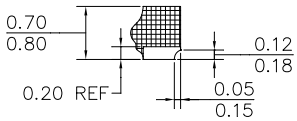
TOP VIEW



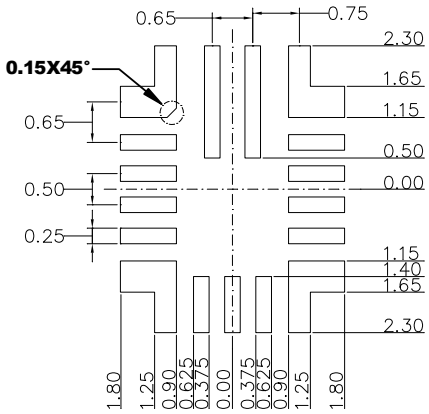
BOTTOM VIEW



SIDE VIEW



SECTION A-A



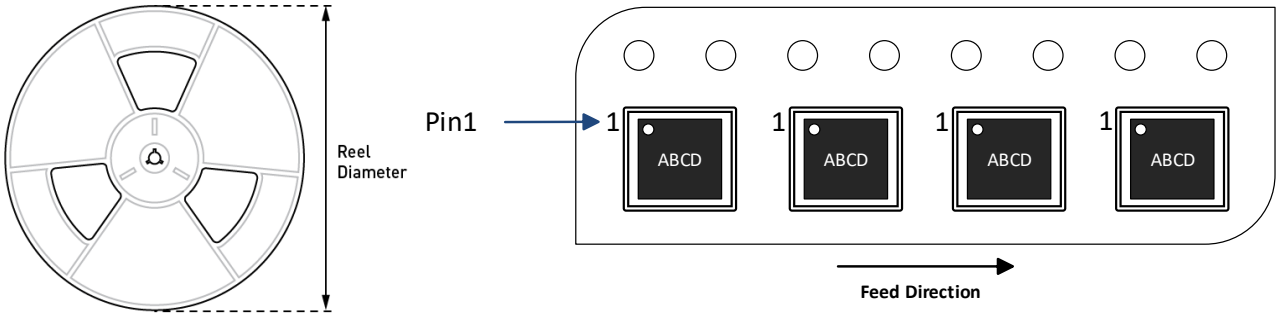
RECOMMENDED LAND PATTERN

NOTE:

1) THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ5862GLTE-xxxx-AEC1-Z	TQFN-17 (3mmx4mm)	5000	N/A	N/A	13in	12mm	8mm

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	3/12/2025	Initial Release	-

Notice: The information in this document is subject to change without notice. Please contact MPS for current specifications. Users should warrant and guarantee that third-party Intellectual Property rights are not infringed upon when integrating MPS products into any application. MPS will not assume any legal responsibility for any said applications.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.