MPQ4485

36V, 6A, Step-Down Converter with Dual USB Charging Ports Supporting Type-C 5V @ 3A DFP Mode and BC1.2 CDP Mode for Automotive, AEC-Q100 Qualified

The Future of Analog IC Technology

DESCRIPTION

The MPQ4485 integrates a monolithic, step-down, switch-mode converter with two USB current-limit switches and charging port identification circuitry. The MPQ4485 achieves 6A of output current with excellent load and line regulation over a wide input supply range.

The output of the USB switch is current-limited. USB1 supports DCP schemes for battery charging specification (BC1.2), divider mode, 1.2V/1.2V mode, and USB Type-C 5V @ 3A DFP mode, eliminating the need for outside user interaction. USB2 supports DCP and CDP schemes.

Full protection features include hiccup current limiting, output over-voltage protection (OVP), and thermal shutdown.

The MPQ4485 requires a minimal number of readily available, standard, external components and is available in a QFN-26 (5mmx5mm) package.

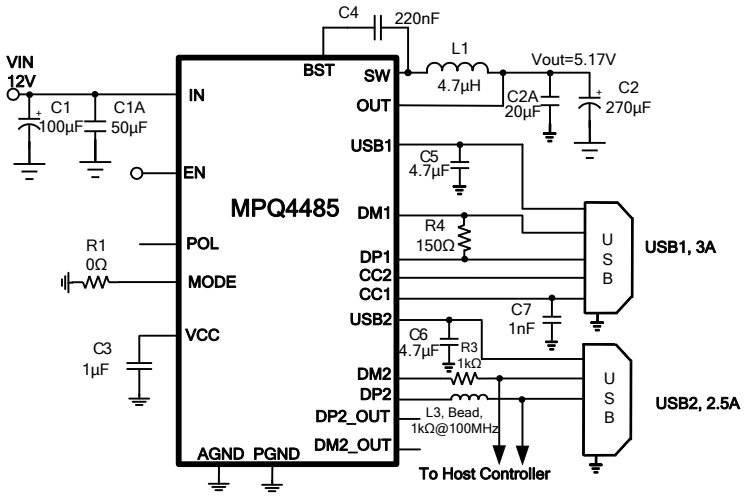
FEATURES

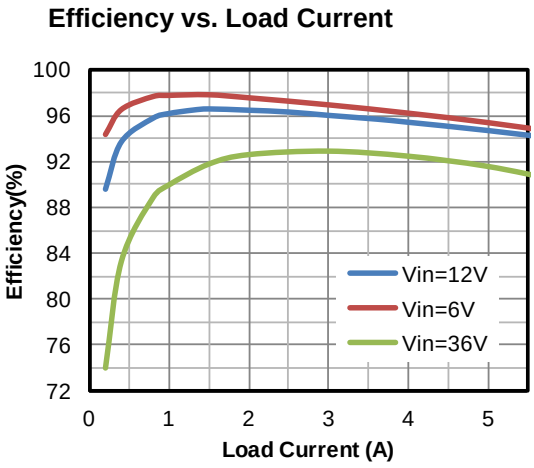
- Wide 6V to 36V Operating Input Voltage Range
- Fixed 5.17V Output Voltage
- 90mV Line Drop Compensation
- Accurate USB1/USB2 Output Current Limit
- 18mΩ/15mΩ Low $R_{DS(ON)}$ Internal Buck Power MOSFETs
- 18mΩ/18mΩ Low $R_{DS(ON)}$ Internal USB1/USB2 Power MOSFETs
- 450kHz Switching Frequency
- Forced CCM Operation
- Load Shedding versus Temperature for MPQ4485GU-LS-AEC1
- USB Output Over-Voltage Protection (OVP)
- Fast Over-Current Response for USB Switch
- Hiccup Current Limit
- Supports DCP Schemes for BC1.2, Divider Mode, and 1.2V/1.2V Mode
- USB1 Supports USB Type-C 5V @ 3A Mode, USB2 Supports CDP Mode
- ±8kV HBM ESD Rating for USB, DP, DM, DP_OUT, and DM_OUT
- Available in a QFN-26 (5mmx5mm) Package
- Available in AEC-Q100 Grade 1

APPLICATIONS

- USB Charging Downstream Port (CDP)
- USB Dedicated Charging Ports (DCP)
- USB Type-C Charging Port

TYPICAL APPLICATION





ORDERING INFORMATION

Part Number	Package	Top Marking
MPQ4485GU-AEC1*	QFN-26 (5mmx5mm)	*See Below*
MPQ4485GU-LS-AEC1**		

* For Tape & Reel, add suffix –Z (e.g. MPQ4485GU-AEC1–Z)
** For Tape & Reel, add suffix –Z (e.g. MPQ4485GU-LS-AEC1–Z)

DEVICE COMPARISON INFORMATION

Part Number	Load Shedding versus Temperature
MPQ4485GU-AEC1	No
MPQ4485GU-LS-AEC1	Yes

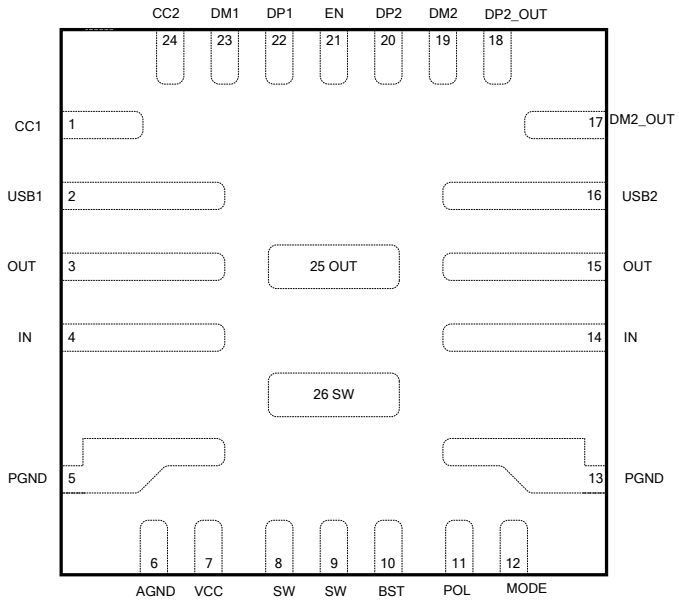
TOP MARKING

MPSYYWW
MP4485
LLLLLLL

MPS: MPS prefix
YY: Year code
WW: Week code
MP4485: Product code
LLLLLLL: Lot number

PACKAGE REFERENCE

TOP VIEW



QFN-26 (5mmx5mm)

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}) ..... -0.4V to +40V
V_{SW} .....-0.3V (-5V for <10ns) to V_{IN} + 0.3V (43V for <10ns)
V_{BST} .....V_{SW} + 5.5V
V_{EN} .....-0.3V to +10V (2)
V_{OUT}, V_{USB} .....-0.3V to +6.5V
All other pins..... -0.3V to +5.5V
Continuous power dissipation (T_A = +25°C) (3)
QFN-26 (5mmx5mm).....6.25W
Junction temperature .....150°C
Lead temperature .....260°C
Storage temperature..... -65°C to +150°C

Recommended Operating Conditions (4)

Operation input voltage range..... 6V to 36V
Output current.....3A for USB1, 2.5A for USB2
Operating junction temp. (TJ)... -40°C to +125°C

Thermal Resistance θ_{JA} θ_{JC}

QFN-26 (5mmx5mm)		
JESD51-7 (5)	44	9 °C/W
50mmx50mm 4-Layer PCB	20	2 °C/W

NOTES:

1) Absolute maximum ratings are rated under room temperature unless otherwise noted. Exceeding these ratings may damage the device.
2) For details on EN's ABS max rating, please refer to the EN Control section on page 13.
3) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage. Measured on a 4-layer PCB (50mmx50mm).
4) The device is not guaranteed to function outside of its operating conditions.
5) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, V_{EN} = 5V, CC1 to ground with 5.1kΩ resistor, T_J = -40°C to +125°C (6), typical value is tested at T_J = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply current (shutdown)	I_{IN}	V_{EN} = 0V		13	18	μA
Supply current (quiescent)	I_Q	No switching		1		mA
EN rising threshold	V_{EN_Rising}		-3%	1.235	+3%	V
EN hysteresis	V_{EN_HYS}			230		mV
EN pull-up current	I_{EN}		4	8	12	μA
Thermal shutdown (7)	T_{STD}			165		°C
Thermal hysteresis (7)	T_{STD_HYS}			20		°C
VCC regulator	V_{CC}		4.3	4.6	4.9	V
VCC load regulation	V_{CC_LOG}	I_{CC} = 50mA		1	3	%
Step-Down Converter						
V_{IN} under-voltage lockout threshold rising	V_{IN_UVLO}		4.6	5	5.4	V
V_{IN} under-voltage lockout threshold hysteresis	V_{UVLO_HYS}			700		mV
HS switch on resistance	R_{DSON_HS}			18	40	mΩ
LS switch on resistance	R_{DSON_LS}			15	30	mΩ
Output voltage	V_{OUT}	T_J = +25°C	-1%	5.17	+1%	V
		T_J = -40°C to+125°C	-2%	5.17	+2%	
Output over-voltage protection	V_{OVP_R}		5.45	5.85	6.25	V
Output OVP recovery	V_{OVP_F}		5.3	5.7	6.1	V
Output to ground resistance	R_{FB}	T_J = +25°C	100	160	220	kΩ
Low-side current limit	I_{LS_LIMIT}			-2		A
Switch leakage	SW_{LKG}	V_{EN} = 0V, V_{SW} = 36V or 0V, T_J = +25°C			1	μA
		V_{EN} = 0V, V_{SW} = 36V or 0V, T_J = -40°C to +125°C			5	
High-side current limit	I_{LIMIT}	V_{OUT} = 0V	8	12	16	A
Oscillator frequency	f_{SW}		360	450	540	kHz
Maximum duty cycle	D_{MAX}	FREQ = 450kHz	91	95	99	%
Minimum off time	T_{OFF_MIN}			110		ns
Minimum on time (7)	T_{ON_MIN}			130		ns
Soft-start time	t_{SS}	Output from 10% to 90%	1	2	3.4	ms
USB Switch						
Under-voltage lockout threshold rising	V_{USB_UVR}		3.7	4	4.3	V
Under-voltage lockout threshold hysteresis	V_{USB_UVHYS}			200		mV
Switch on resistance	R_{DSON_SW}			18	35	mΩ
Output discharge resistance	R_{DIS_USB}	USB disabled, apply 5V voltage on USB output	250	500	750	kΩ

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{EN} = 5V, T_J = -40°C to +125°C (6), typical value is tested at T_J = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
USB OVP clamp	V_{USB_OV}		5.3	5.6	5.9	V
Current limit	I_{Limit1}	V_{OUT} drop 10%, Type-C mode, T_J = +25°C	-6%	3.55	6%	A
	I_{Limit2}	V_{OUT} drop 10%, Type-A mode, T_J = +25°C	2.6	2.75	2.9	
Line drop compensation	V_{DROP_COM}	I_{OUT} = 2.4A, V_{OUT} = 5V	40	90	140	mV
V_{BUS} soft-start time	T_{SS}	V_{OUT} = 5V, from 10% to 90%	1	2	3	ms
Hiccup mode on time	T_{HICP_ON}	V_{OUT} = 5V, OC, V_{OUT} drop 10%, T_J = +25°C	3.5	5	6.5	ms
		V_{OUT} = 5V, OC, V_{OUT} drop 10%, T_J = -40°C to +125°C	3	5	7	
Hiccup mode off time	T_{HICP_OFF}	V_{BUS} connected to GND	1	2	3	s
BC1.2 DCP Mode						
DP and DM short resistance	R_{DP/DM_Short}	V_{DP} = 0.8V, I_{DM} = 1mA, T_J = +25°C		85	155	Ω
		V_{DP} = 0.8V, I_{DM} = 1mA, T_J = -40°C to +125°C		85	160	
Divider Mode						
DP/DM output voltage	$V_{DP/DM\_Divider}$	V_{OUT} = 5V	2.55	2.7	2.85	V
DP/DM output impedance	$R_{DP/DM\_Divider}$	T_J = +25°C	14	22	30	kΩ
		T_J = -40°C to +125°C	12	22	34	
1.2V/1.2V Mode						
DP/DM output voltage	$V_{DP/DM\_1.2V}$	V_{OUT} = 5V, T_J = +25°C	1.12	1.2	1.28	V
		V_{OUT} = 5V, T_J = -40°C to +125°C	1.1	1.2	1.3	
DP/DM output impedance	$R_{DP/DM\_1.2V}$	T_J = +25°C	70	105	140	kΩ
		T_J = -40°C to +125°C	60	105	150	
USB Type-C 5V @ 3A Mode (CC1, CC2)						
CC resistor to disable Type-C mode	R_A	CC1 pin, for Type-C mode application, add a 1nF capacitor on CC1	70		90	kΩ
CC voltage to enable VCONN	V_{Ra}				0.75	V
CC voltage to enable V_{BUS}	V_{Rd}		0.9		2.45	V
CC detach threshold	V_{OPEN}		2.75			V
CC voltage falling debounce timer	$T_{CC\_debounce}$	V_{BUS} enable deglitch	100	144	200	ms
CC voltage rising debounce timer	$T_{PD\_debounce}$	V_{BUS} disable deglitch	10	15	20	ms
VCONN output power	P_{VCONN}	VCONN comes from buck output with some series resistance, T_J = +25°C	1			W
POL output low voltage	V_{POL}	Pull CC1 to ground with 5.1kΩ resistor, POL sink 1mA			150	mV
POL leakage	$I_{Leakage\_POL}$				1	µA

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{EN} = 5V, T_J = -40°C to +125°C (6), typical value is tested at T_J = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
CDP (MODE)						
MODE logic high voltage	V_{MODE_H}	MODE has 1MΩ pull-up resistor to internal VDD	2			V
MODE logic low voltage	V_{MODE_L}				0.7	V
DM CDP output voltage	V_{DM_SRC}	VDP = 0.6V	0.5	0.6	0.7	V
DP rising lower window threshold for V_{DM_SRC} activation	V_{DAT_RE}		0.25	0.3	0.4	V
DP rising lower window threshold hysteresis for V_{DM_SRC} activation	$V_{DAT\_RE\_HYS}$			100		mV
DP rising upper window threshold for V_{DM_SRC} deactivation	V_{LGC_SRC}		0.8	0.9	1	V
DP rising upper window threshold hysteresis for V_{DM_SRC} deactivation	$V_{LGC\_SRC\_HYS}$			150		mV
V_{DM_SRC} on/off deglitch time	$V_{DM\_SRC\_Deglitch}$			5		ms
RDP_Down, RDM_Down	R_{DP/DM_Down}		14.25	19.5	24.8	kΩ
DP/DM switch on resistance	$R_{ON\_DP/DM}$			2		Ω
DP to DP_OUT SW on cap (7)	C_{DP}	Same for DM switch		5.3		pF
3dB bandwidth of analog data SW (7)			500			MHz

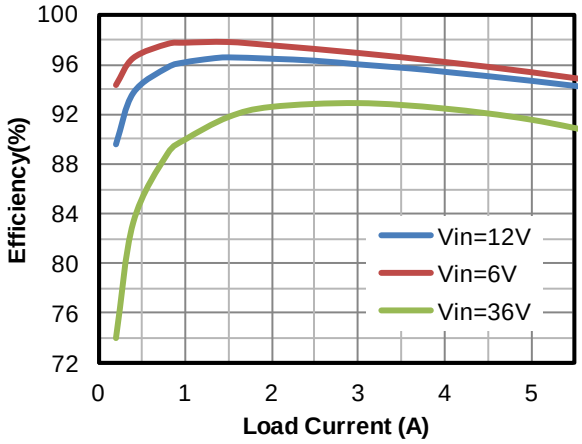
NOTES:

6) All min/max parameters are tested at T_J = 25°C. Limits over temperature are guaranteed by design, characterization and correlation.
7) Guaranteed by design.

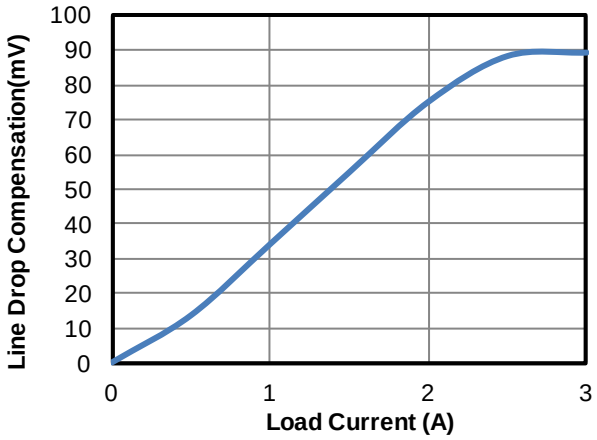
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 5.17V, L = 4.7µH, T_A = 25°C, set USB1 to Type-C 5V @ 3A DFP mode, set USB2 to CDP mode, unless otherwise noted.

Efficiency vs. Load Current

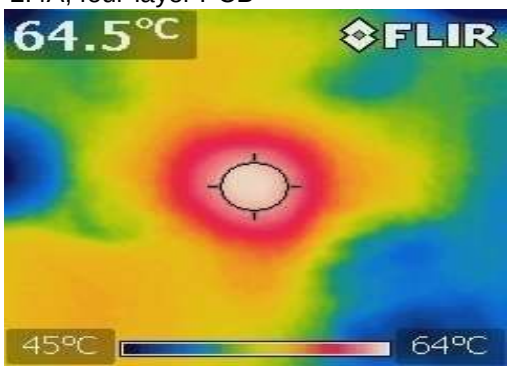


Line Drop Compensation vs. Load Current



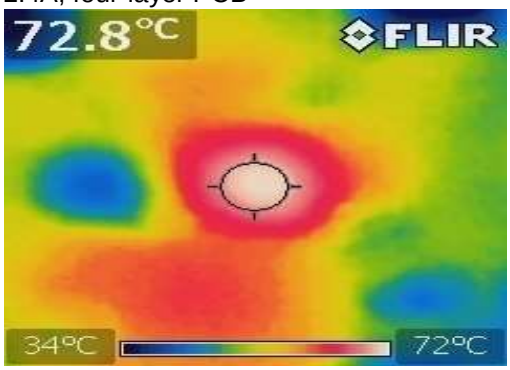
Thermal Image

V_{IN} = 12V, USB1_IOUT = USB2_IOUT = 2.4A, four-layer PCB



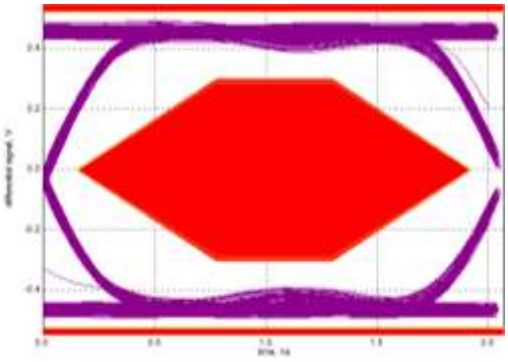
Thermal Image

V_{IN} = 12V, USB1_IOUT = 3A, USB2_IOUT = 2.4A, four-layer PCB



USB2 Eye Pattern Test

Recommended CDP mode set-up

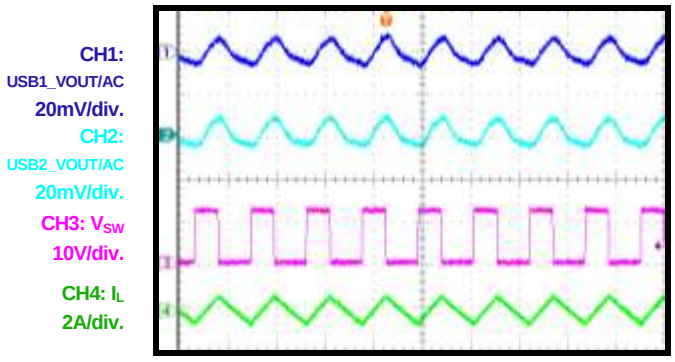


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5.17V, L = 4.7µH, T_A = 25°C, set USB1 to Type-C 5V @ 3A DFP mode, set USB2 to CDP mode, unless otherwise noted.

Output Ripple

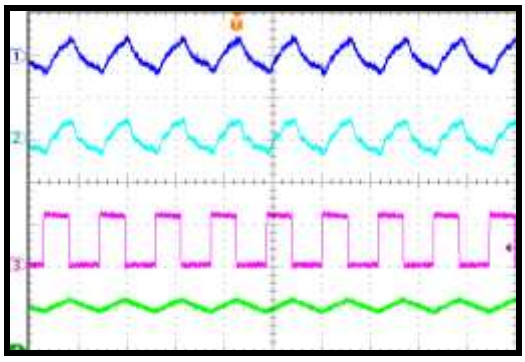
USB1_Io = USB2_Io = 0A



2µs/div.

Output Ripple

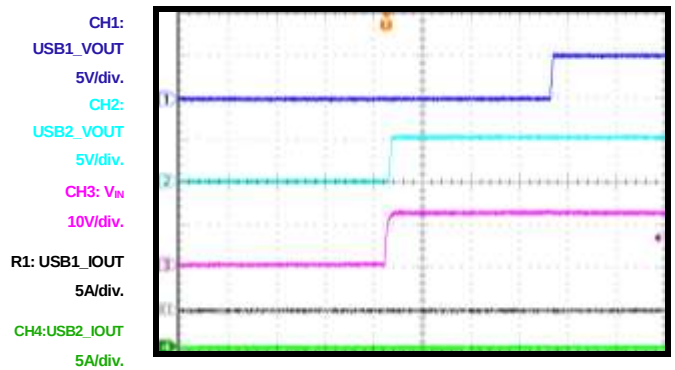
USB1_Io = 3A, USB2_Io = 2.4A



2µs/div.

Power Start-Up

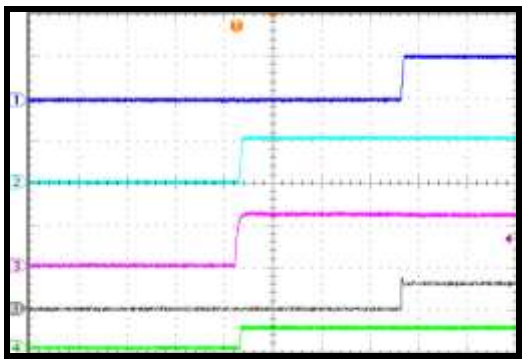
USB1_Io = USB2_Io = 0A



40ms/div.

Power Start-Up

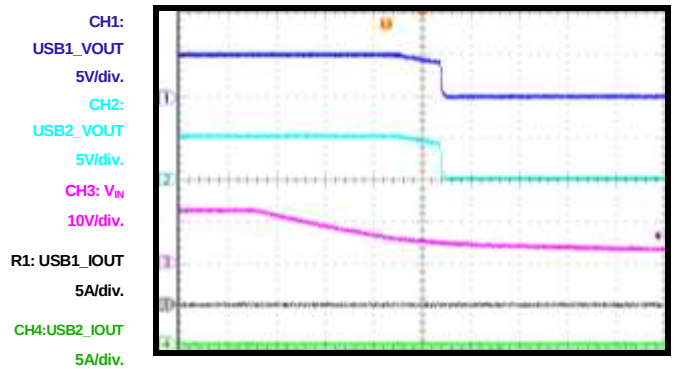
USB1_Io = 3A, USB2_Io = 2.4A



40ms/div.

Power Shutdown

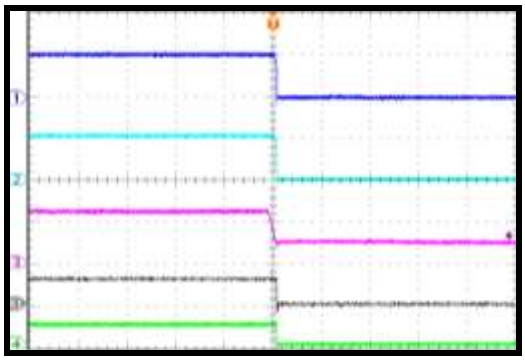
USB1_Io = USB2_Io = 0A



40ms/div.

Power Shutdown

USB1_Io = 3A, USB2_Io = 2.4A



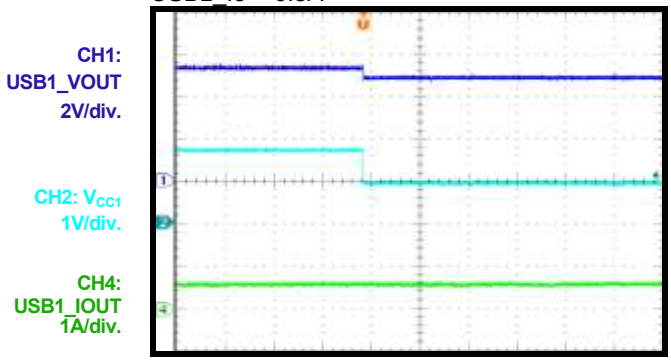
4ms/div.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5.17V, L = 4.7µH, T_A = 25°C, set USB1 to Type-C 5V @ 3A DFP mode, set USB2 to CDP mode, unless otherwise noted.

Load Shedding Entry (For MPQ4485GU-LS-AEC1 Only)

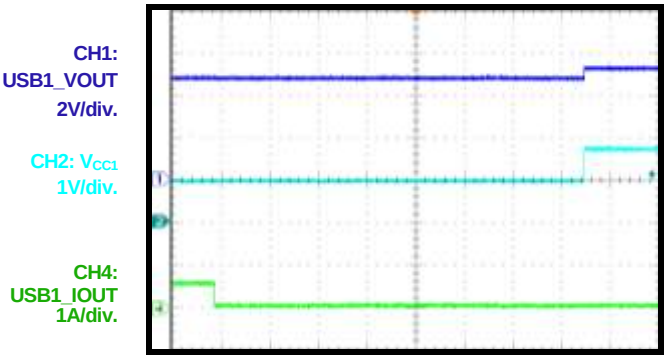
USB1_Io = 0.5A



10ms/div.

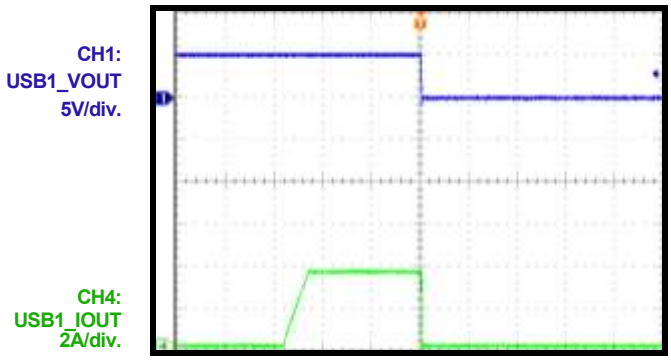
Load Shedding Recovery (For MPQ4485GU-LS-AEC1 Only)

USB1 load current from 0.5A to 0A



2s/div.

USB1 Over-Current Protection



2ms/div.

PIN FUNCTIONS

QFN 5x5 Pin #	Name	Description
1	CC1	**Configuration channel.** CC1 is used to detect connections and configure the interface across the USB1 Type-C cables and connectors. Once a connection is established, CC1 or CC2 is reassigned to provide power over the VCONN pin of the plug.
2	USB1	**USB1 output.**
3, 15, 25	OUT	**Buck output.** OUT is the power input for USB1 and USB2.
4, 14	IN	**Supply voltage.** IN is the drain of the internal power device and provides power to the entire chip. The MPQ4485 operates from a 6V to 36V input voltage. The input capacitor (C_{IN}) can prevent large voltage spikes at the input. Place C_{IN} as close to the IC as possible.
5, 13	PGND	**Power ground.** PGND is the reference ground of the regulated output voltage. PGND requires extra care during the PCB layout. Connect PGND to GND with copper traces and vias.
6	AGND	**Analog ground.** Connect AGND to PGND.
7	VCC	**Internal 4.6V LDO regulator output.** Decouple VCC with a 0.22µF capacitor.
8, 9, 26	SW	**Switch output.** Use a wide PCB trace to make the connection.
10	BST	**Bootstrap.** A 0.1µF capacitor is connected between SW and BST to form a floating supply across the high-side switch driver.
11	POL	**Type-C plug orientation indication.** When POL is low, CC1 is used as the CC pin. When POL is high, CC2 is used as the CC pin.
12	MODE	**USB2 mode control.** Float MODE to set USB2 to DCP mode. Pull MODE low to set USB2 to CDP mode. MODE has a 1MΩ pull-up resistor to the internal VCC.
16	USB2	**USB2 output.**
17	DM2_OUT	**D- data line output.**
18	DP2_OUT	**D+ data line output.**
19	DM2	**D- data line to USB2 connector.** DM2 is the input/output used for handshaking with portable devices.
20	DP2	**D+ data line to USB2 connector.** DP2 is the input/output used for handshaking with portable devices.
21	EN	**On/off control input.** EN has an internal auto pull-up with a 8µA current source.
22	DP1	**D+ data line to USB1 connector.** DP1 is the input/output used for handshaking with portable devices.
23	DM1	**D- data line to USB1 connector.** DM1 is the input/output used for handshaking with portable devices.
24	CC2	**Configuration channel.** CC2 is used to detect connections and configure the interface across the USB1 Type-C cables and connectors. Once a connection is established, CC1 or CC2 is reassigned to provide power over the VCONN pin of the plug.

BLOCK DIAGRAM

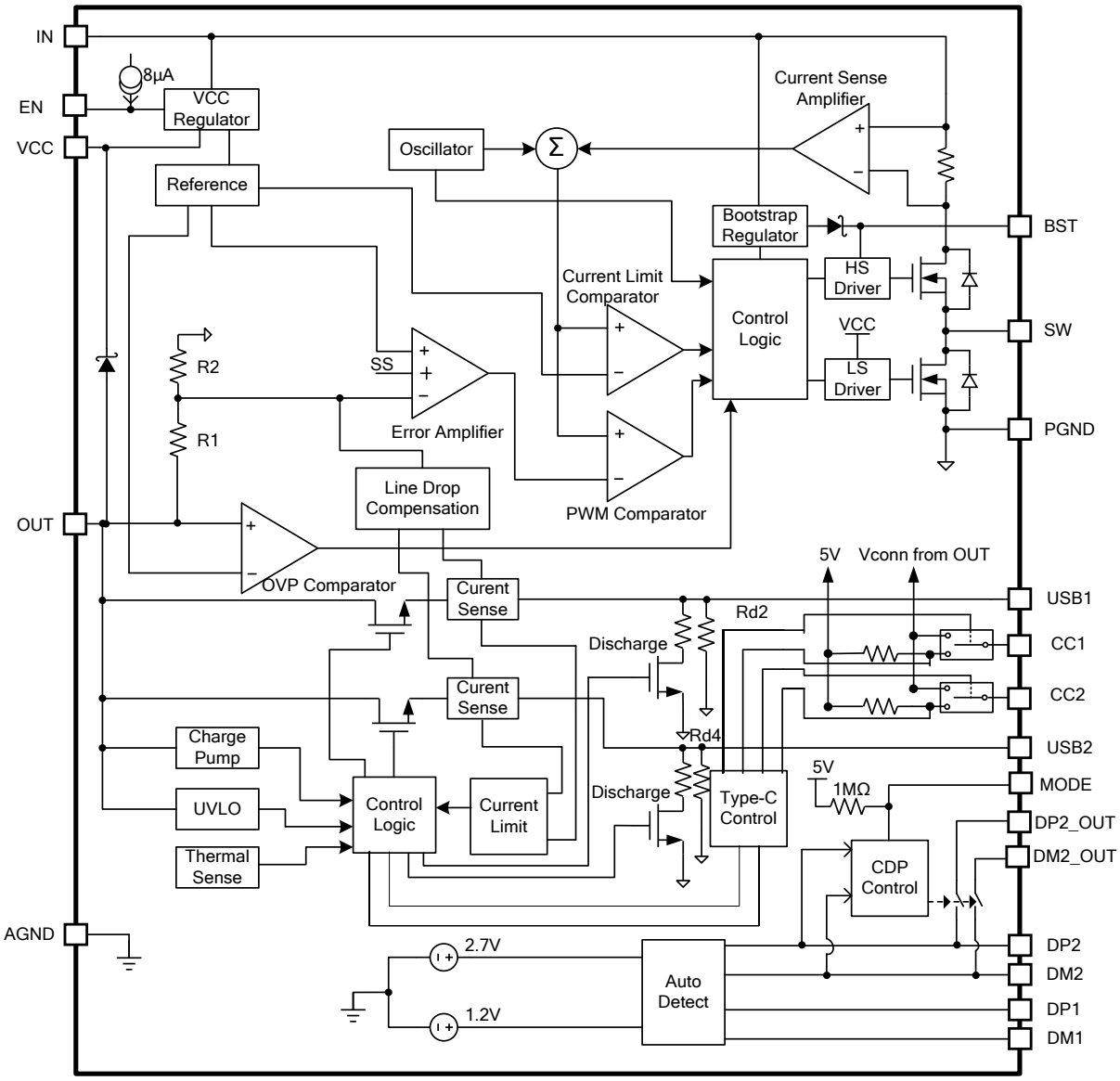


Figure 1: Functional Block Diagram

OPERATION

BUCK CONVERTER SECTION

The MPQ4485 integrates a monolithic, synchronous, rectified, step-down, switch-mode converter with internal power MOSFETs and two USB current-limit switches with charging port auto-detection. The MPQ4485 offers a compact solution that achieves 6A of continuous output current with excellent load and line regulation over a wide input-supply range.

The MPQ4485 operates in a fixed-frequency, peak-current-mode control to regulate the output voltage. The internal clock initiates the pulse-width modulation (PWM) cycle, which turns on the integrated high-side power MOSFET (HS-FET). The HS-FET remains on until its current reaches the value set by the COMP voltage (V_{COMP}). When the power switch is off, it remains off until the next clock cycle begins. If the duty cycle reaches 95% (450kHz switching frequency) in one PWM period, the current in the power MOSFET cannot reach the COMP-set current value, and the power MOSFET turns off.

Error Amplifier (EA)

The error amplifier (EA) compares the internal feedback voltage against the internal reference (REF) and outputs V_{COMP}. V_{COMP} controls the power MOSFET current. The optimized, internal compensation network minimizes the external component count and simplifies the control loop design.

Internal VCC Regulator

The 4.6V internal regulator powers most of the internal circuitries. This regulator takes V_{IN} and operates in the full V_{IN} range. When V_{IN} exceeds 4.6V, the output of the regulator is in full regulation. If V_{IN} is less than 4.6V, the output decreases with V_{IN}. VCC requires an external 1µF ceramic decoupling capacitor.

After the buck output starts up, the internal VCC LDO output is biased by the buck output through a Schottky diode.

Enable Control (EN)

The MPQ4485 has an enable control (EN) pin. An internal 8µA pull-up current allows EN to be floated for automatic start-up. Pull EN high or float EN to enable the IC. Pull EN low to disable the IC.

EN is clamped internally using a 7.6V series Zener diode and a 10V breakdown voltage of the ESD cell (see Figure 2).

Connect EN through a pull-up resistor to V_{IN} to enhance the EN pull-up current ability. This requires limiting the EN voltage below 10V or limiting the EN input current below 500µA if the EN pull-up voltage is larger than 10V.

For example, if connecting EN to V_{IN} = 36V, then R_{PULLUP} ≥ (36V - 10V)/500µA = 52kΩ.

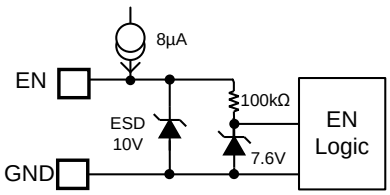


Figure 2: Zener Diode between EN and GND

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The UVLO comparator monitors the input voltage. The UVLO rising threshold is 5V, and its falling threshold is 4.3V.

Internal Soft Start (SS)

Soft start (SS) prevents the converter output voltage from overshooting during start-up. When the chip starts up, the internal circuitry generates an SS voltage that ramps up from 0V to 5V. When SS is lower than REF, the error amplifier uses SS as the reference. When SS is higher than REF, the error amplifier uses REF as the reference. The SS time is set to 2ms internally.

If the output of the MPQ4485 is pre-biased to a certain voltage during start-up, the IC disables the switching of both the high-side and low-side switches until the voltage on the internal SS capacitor exceeds the internal feedback voltage.

Forced CCM Operation

The MPQ4485 works in forced continuous conduction mode (CCM) continuously. The MPQ4485 operates in a fixed switching frequency regardless of whether it is operating in light load or full load. The advantage of CCM is the controllable frequency, smaller output ripple, and sufficient bootstrap charge time, but it also has low efficiency at light-load condition. A proper inductance should be selected to avoid triggering the low-side switch's negative current limit (typically 2A, from SW to GND). If the negative current limit is triggered, the low-side switch turns off, and the high-side switch turns on when the internal clock begins.

Buck Over-Current Protection (OCP)

The MPQ4485 has a cycle-by-cycle over-current limit when the inductor peak current exceeds the current-limit threshold, and the FB voltage drops below the under-voltage (UV) threshold (typically 50% below the reference). Once UV is triggered, the MPQ4485 enters hiccup mode to restart the part periodically. This protection mode is especially useful when the output is dead-shorted to ground. This reduces the average short-circuit current greatly, alleviates thermal issues, and protects the regulator. The MPQ4485 exits hiccup mode once the over-current condition is removed.

Buck Output Over-Voltage Protection (OVP)

The MPQ4485 has output over-voltage protection (OVP). If the output is higher than 5.85V, the high-side switch stops turning on. The low-side switch turns on to discharge the output voltage until the output decreases to 5.7V, and then the chip resumes normal operation.

Floating Driver and Bootstrap Charging

An external bootstrap capacitor powers the floating power MOSFET driver. This floating driver has its own UVLO protection. The UVLO's rising threshold is 2.2V with a hysteresis of 150mV. The bootstrap capacitor voltage is regulated internally by V_{IN} and VCC through D1, D2, M1, C4, L1, and C2 (see Figure 5). The BST capacitor (C4) voltage is charged up quickly by VCC through M1.

The 2.5μA input to the BST current source can also charge the BST capacitor when the low-side switch does not turn on.

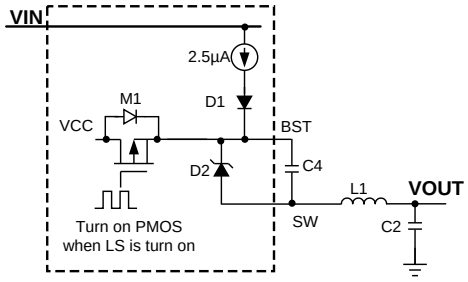


Figure 3: Internal Bootstrap Charging Circuit

Start-Up and Shutdown

If both IN and EN exceed their respective thresholds, the chip is enabled. The reference block starts first, generating a stable reference voltage and current, and then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuitries.

Three events can shut down the chip: EN low, IN low, and thermal shutdown. During shutdown, the signaling path is blocked to avoid any fault triggering. Then V_{COMP} and the internal supply rail are pulled down. The floating driver is not subject to this shutdown command.

Buck Output Impedance

The buck does not involve an output discharge function during EN shutdown. After EN shuts down, there are only two feedback resistors connected to OUT, which have a typical resistance of 160kΩ in total.

USB CURRENT-LIMIT SWITCH SECTION

Over-Current Protection (OCP) and Hiccup

The MPQ4485 integrates two USB current-limit switches. The MPQ4485 provides built-in soft-start circuitry, which controls the rising slew rate of the output voltage to limit inrush current and voltage surges.

When the load current reaches the current-limit threshold, the USB power MOSFET works in a constant current-limit mode (see Figure 6). If the over-current limit condition lasts longer than 5ms (V_{OUT} does not drop too low), the corresponding USB channel enters hiccup mode with 5ms of on time and 2s of off time. Another USB channel works normally.

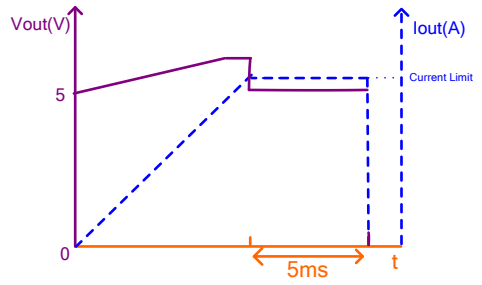


Figure 6: Over-Current Limit

After the soft-start finishes, if the USB output voltage is lower than 3.5V and lasts longer than 50µs, the MPQ4485 enters hiccup mode without having to wait 5ms (see Figure 7). This can prevent an abnormal thermal rise during the constant resistor (CR) load over-current case.

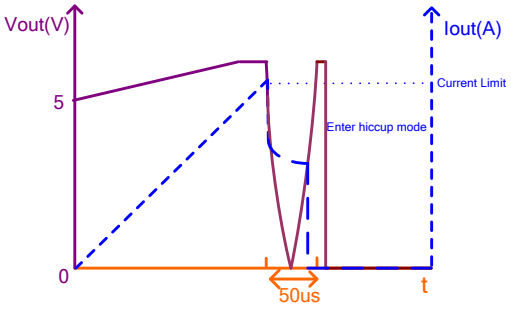


Figure 7: Over-Current Limit for CR Load

Fast Response for Short-Circuit Protection (SCP)

If the load current increases rapidly due to a short-circuit event, the current may exceed the current-limit threshold before the control loop is able to respond. If the current reaches the 7A secondary current-limit level, a fast turn-off circuit activates to turn off the power MOSFET. This can help limit the peak current through the switch, keeping the buck output voltage from dropping too much and affecting another USB channel. The total short-circuit response time is less than 1µs.

When the fast turn-off function is triggered, the MOSFET turns off for 100µs and restarts with a soft start. During the restart process, if the short still remains, the MPQ4485 regulates the gate voltage to hold the current at a normal current-limit level.

Output Line Drop Compensation

The MPQ4485 can compensate for an output voltage drop, such as high impedance caused by a long trace, to maintain a fairly constant output voltage at the load-side voltage.

The internal comparator compares the current-sense output voltage of the two current-limit switches and uses the larger current-sense output voltage to compensate for the line drop voltage.

The line drop compensation amplitude increases linearly as the load current increases and also has an upper limitation. The default line drop amplitude at a >2.4A output current is 90mV.

USB Output Over-Voltage Protection (OVP)

To protect the device at the cable terminal, the USB switch output has a fixed over-voltage protection (OVP) threshold. When the input voltage is higher than the OVP threshold, the output voltage is clamped at the OVP threshold value.

USB Output Discharge and Impedance

Each USB switch has a fast discharge path that can discharge the external output capacitor's energy quickly during a power shutdown. This function is active when the CC pins are released or the part is disabled (input voltage is under UVLO or EN off). The discharge path is turned off when the USB output voltage is discharged below 50mV. After the fast discharge path turns off, there is only a high impedance resistor (typically 500kΩ) from USB1 or USB2 to ground.

Auto Detection

The MPQ4485 USB1 integrates a USB-dedicated charging port auto-detect function. This function recognizes most mainstream portable devices and supports the following charging schemes:

- USB battery charging specification BC1.2/ Chinese Telecommunications Industry Standard YD/T 1591-2009
- Divider mode
- 1.2V/1.2V mode
- USB Type-C 5V @ 3A DFP mode

The auto-detect function is a state machine that supports all of the DCP charging schemes above. Connect DP and DM with a 150Ω resistor for DCP mode.

CDP Mode

USB2 supports dynamically selectable DCP or CDP mode. Float MODE to set USB2 to DCP mode. Pull MODE low to set USB2 to CDP mode.

To achieve better data transmission performance, use USB2 CDP mode for handshaking and bypass DP to DP_OUT only. DM to DM_OUT switches internally (see Figure 8).

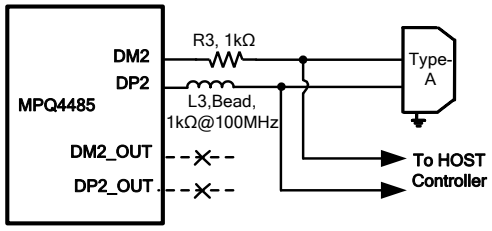


Figure 8: Data Transmission Enhanced Set-Up

Type-C Plug Orientation Indication (POL)

POL is an open-drain output that indicates the Type-C plug's orientation. When POL is low, CC1 is used as the CC pin. When POL is high, CC2 is used as the CC pin.

USB Type-C Mode and VCONN

For USB Type-C solutions, two pins (CC1, CC2) on the connector are used to establish and manage the source-to-sink connection. The general concept for setting up a valid connection between a source and sink is based on being able to detect terminations residing in the product being attached. To aid in defining the functional behavior of CC, a pull-up (Rp) and pull-down (Rd 5.1kΩ) termination model is used based on a pull-up resistor and pull-down resistor (see Figure 9).

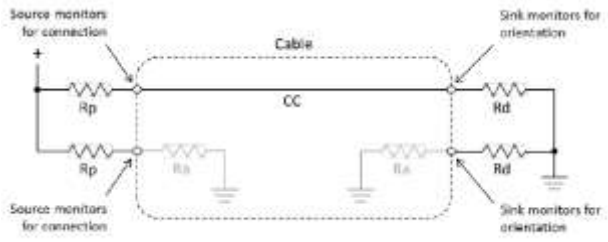


Figure 9: Current Source/Pull-Down CC Model

Initially, a source exposes independent Rp terminations on its CC1 and CC2 pins, and a sink exposes independent Rd terminations on its CC1 and CC2 pins, the source-to-sink combination of this circuit configuration represents a valid connection. To detect this, the source monitors CC1 and CC2 for a voltage lower than its unterminated voltage. The choice of Rp is a function of the pull-up termination voltage and the source's detection circuit. This indicates that either a sink, a powered cable, or a sink connected via a powered cable has been attached.

Prior to the application of VCONN, a powered cable exposes Ra (typically 1kΩ) on its VCONN. Ra represents the load on VCONN plus any resistive elements to ground. In some cable plugs, this might be pure resistance, and in others, it may be simply the load.

The source must be able to differentiate between the presence of Rd and Ra to know whether there is a sink attached and where to apply VCONN. The source is not required to source VCONN unless Ra is detected.

Two special termination combinations on the CC pins as seen by a source are defined for directly attached accessory modes: Ra/Ra for audio adapter accessory mode and Rd/Rd for debug accessory mode (see Figure 10 and Table 1).

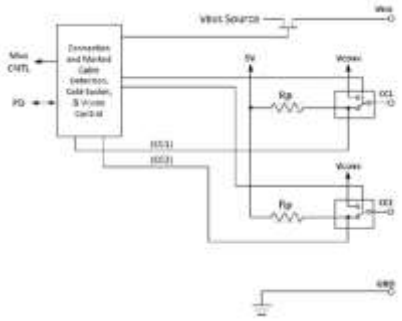


Figure 10: CC Functional Block

A port that behaves as a source has the following functional characteristics.

1. The source uses a MOSFET to enable or disable power delivery across V_{BUS}. Initially, the source is disabled.
2. The source supplies pull-up resistors (Rp) on CC1 and CC2 and monitors both to detect a sink. The presence of an Rd pull-

down resistor on either CC1 or CC2 indicates that a sink is being attached. The value of Rp indicates the initial USB Type-C current level supported by the host. The MPQ4485 default Rp is 10kΩ, which represents a 3A current level.

3. The source uses the CC pull-down characteristic to detect and determine which CC pin is intended to supply VCONN (when Ra is discovered).
4. Once a sink is detected, the source enables V_{BUS} and VCONN.
5. The source can adjust the value of Rp dynamically to indicate a change in available USB Type-C current to a sink. For example, at high temperatures, the MPQ4485GU-LS-AEC1 changes Rp to 22kΩ to indicate a 1.5A current ability.
6. The source monitors the continued presence of Rd to detect a sink detachment. When a detach event is detected, the source is removed, and V_{BUS} and VCONN return to step 2.

Disable Type-C Mode

During the MPQ4485 initial start-up, the IC sources 10μA for 20μs on CC1. If the CC1 voltage falls into the 400mV to 1.2V voltage range, USB1 latches in Type-A mode unless the part is re-enabled. Type-C mode is disabled, so CC is attached, the detach logic is disabled, and V_{BUS} is always enabled. The current limit changes to a Type-A spec.

To trigger Type-A mode, the external pull-down resistor should be 70 - 90kΩ. Do not connect extra capacitors on CC1.

In normal Type-C mode applications, a 1nF capacitor should be added on CC1 to avoid falsely triggering Type-A mode.

The MPQ4485 also supports debug mode and audio adapter accessory mode in Type-C applications. If two Ra resistors pull down CC1 and CC2 or two Rd resistors pull down CC1 and CC2, there is no action inside the IC (V_{BUS} is not enabled).

Load Shedding versus Temperature

The MPQ4485GU-LS-AEC1 monitors the die temperature and changes its output current capability dynamically. This feature is supported by both Type-C and USB2.0 applications.

When the die temperature is higher than 125°C, the USB port's CC pin pull-up resistance Rp changes to 22kΩ to indicate that its source capability has changed to 1.5A. Meanwhile, V_{BUS} changes to 4.77V.

If the die temperature is lower than 100°C for 16 seconds, V_{BUS} reverts to the normal voltage set by OUT_SEL. Meanwhile, the USB Type-C current capability changes back to 3A (Rp = 10kΩ). The current limit threshold remains at 3.55A during this period.

Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the silicon die temperature exceeds 165°C, the entire chip shuts down. When the temperature falls below its lower threshold, (typically 145°C), the chip is enabled.

Table 2: CC Logic Truth Table

EN	CC of USB1	Buck	VCONN (USB1)	USB1	USB2
0	X	Disabled	Disabled	Disabled	Disabled
1	AUDIO	Enabled	Disabled	Disabled	Enabled
	DEBUG	Enabled	Disabled	Disabled	Enabled
	“A” (8)	Enabled	Disabled	Enabled	Enabled
	Rd, Ra	Enabled	Enabled	Enabled	Enabled
	Open	Enabled	Disabled	Disabled	Enabled

NOTE:

8) "A" means Type-A mode. CC1 is requested to be pulled down by a 80.6kΩ resistor to enter this mode.

APPLICATION INFORMATION

Selecting the Inductor

For most applications, use an inductor with a DC current rating at least 25% higher than the maximum load current. Select an inductor with a small DC resistance for optimum efficiency. For most designs, the inductor value can be derived with Equation (1):

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}} \quad (1)$$

Where ΔI_L is the inductor ripple current.

Choose the inductor ripple current at approximately 30% of the maximum load current. The maximum inductor peak current can be calculated with Equation (2):

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2} \quad (2)$$

Selecting Buck Input Capacitor

The input current to the step-down converter is discontinuous and therefore requires a capacitor to supply AC current while maintaining the DC input voltage. Use low ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. 100µF electrolytic and 50µF ceramic capacitors are recommended for automotive applications.

Since the input capacitor (C1) absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated with Equation (3):

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (3)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, shown in Equation (4):

$$I_{C1} = \frac{I_{LOAD}}{2} \quad (4)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using an electrolytic capacitor, place two additional high-quality ceramic capacitors as close to IN as possible. Estimate the input voltage ripple caused by the capacitance with Equation (5):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_S \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (5)$$

Selecting Buck Output Capacitor

The device requires an output capacitor (C2) to maintain the DC output voltage. Estimate the output voltage ripple with Equation (6):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_S \times C2}\right) \quad (6)$$

Where L_1 is the inductor value, and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

For an electrolytic capacitor, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated with Equation (8):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (8)$$

A 100 - 270µF capacitor with an ESR less than 50mΩ (e.g.: polymer or tantalum capacitors) and two 10µF ceramic capacitors are recommended in the application.

ESD Protection for I/O Pins

A higher ESD level should be considered for all USB I/O pins. The MPQ4485 features high ESD protection up to ±8kV human body model on DP, DM, DM_OUT, DP_OUT, USB1, and USB2, and ±5.5kV human body model on CC1 and CC2. The ESD structures can withstand high ESD both in normal operation and when the device is powered off. To further extend DP1 and DM1's ESD level for covering complicated application environments, additional resistors and capacitors can be added (see Figure 11).

Similar R-C networks cannot be added on CC1 or CC2 because the CC line must support 200mA of current and 300kHz of signaling. Additional ESD diodes can be added on the CC pins.

When USB2 is in DCP mode, the R-C network can be added on DM2 and DP2 for ESD enhancement. When USB2 is in CDP mode, similar R-C networks cannot be added on DP2, DM2, DP2_OUT, or DM2-OUT pins due to the data transmission.

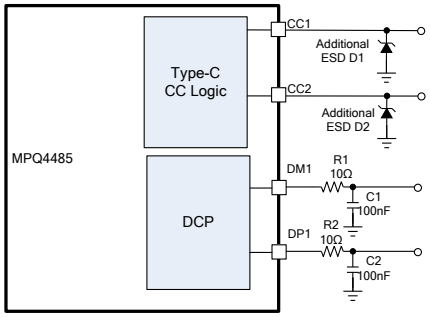


Figure 11: I/O Pins for ESD Enhancing

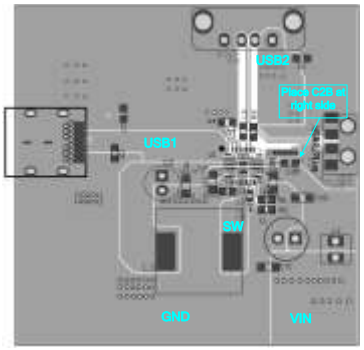
PCB Layout Guidelines [9]

Efficient PCB layout is critical for stable operation and thermal dissipation. For best results, refer to Figure 12 and follow the guidelines below.

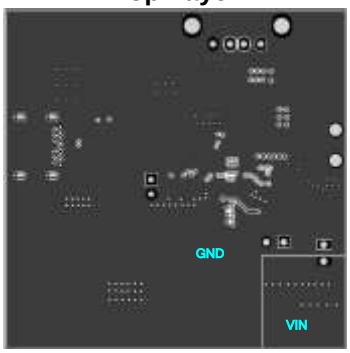
1. Use short, direct, and wide traces to connect OUT.
2. Add vias under the IC.
3. Route the OUT trace on both PCB layers.
4. Place the buck output ceramic capacitor C2A on the left side and C2B on the right side.
5. Add a large copper plane for PGND.
6. Add multiple vias to improve thermal dissipation.
7. Connect AGND to PGND.
8. Place a large copper plane for SW, USB1, and USB2.
9. Route the USB1 and USB2 traces on both PCB layers.
10. Add multiple vias.
11. Place two ceramic input decoupling capacitors as close to IN and PGND as possible to improve EMI performance.
12. Place the symmetrical C_{IN} capacitors on each side of the IC.
13. Place the BST capacitor close to BST and SW.
14. Place the VCC decoupling capacitor as close to VCC as possible.

NOTE:

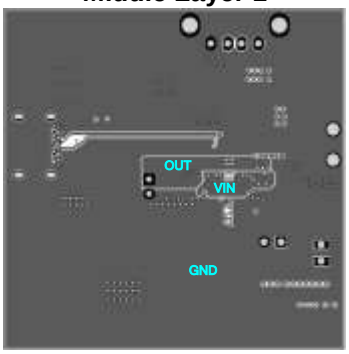
9) The recommended layout is based on setting USB1 to DCP mode and USB2 to CDP mode (see the Typical Application Circuits in Figure 13 to Figure 15).



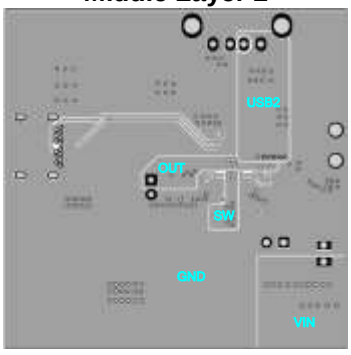
Top Layer



Middle Layer 1



Middle Layer 2



Bottom Layer

Figure 12: Recommended Layout

TYPICAL APPLICATION CIRCUITS

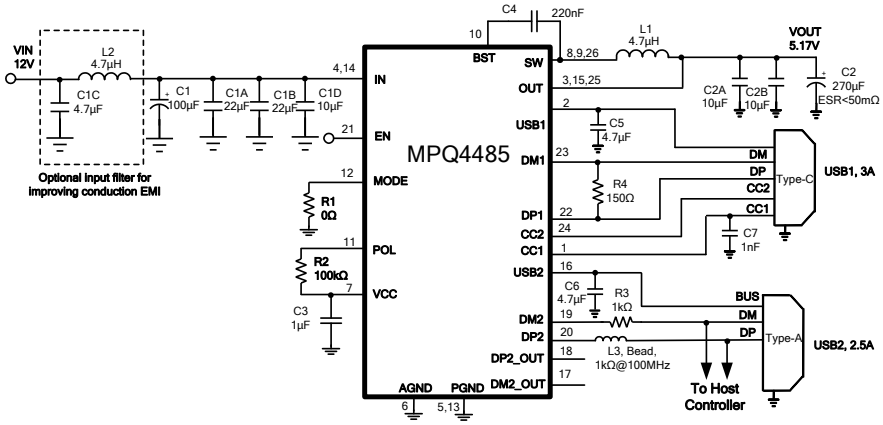


Figure 13: USB1 5V @ 3A Type-C Mode, USB2 Type-A Port with CDP Mode (10) (11)

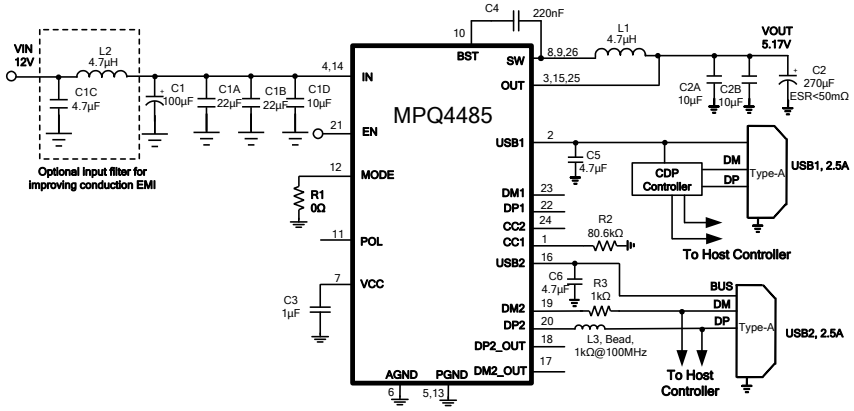


Figure 14: Dual Type-A Port with CDP Mode (10) (11)

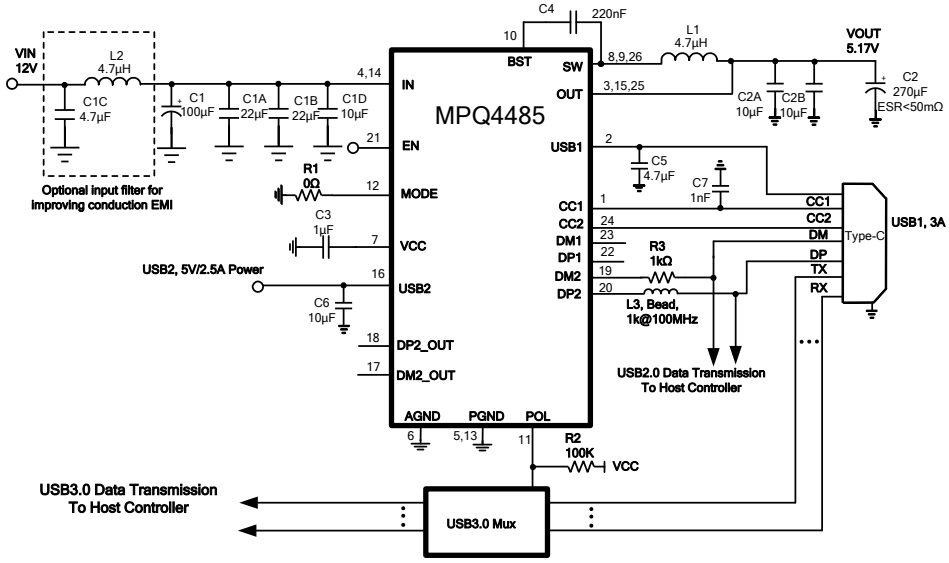


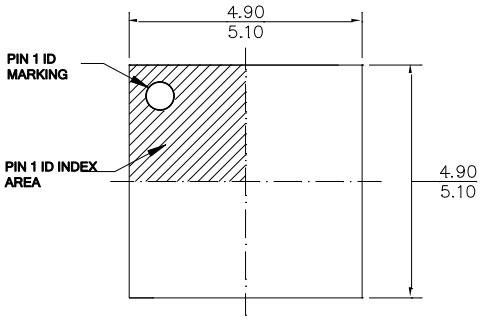
Figure 15: USB1 Type-C 5V @ 3A DFP Mode with USB3.0/USB2.0 Data Transmission, USB2 5V @ 2.5A Power Output (10) (11)

NOTES:

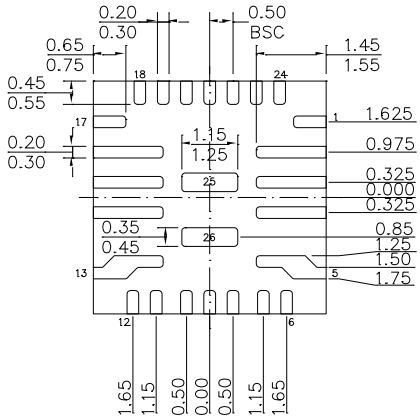
10) See Figure 11 for I/O pins' ESD protection enhancing details.
11) See Figure 8 for enhanced CDP mode data transmission set-up details.

PACKAGE INFORMATION

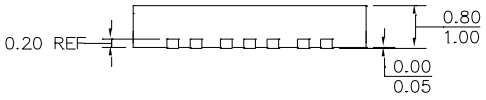
QFN-26 (5mmx5mm)



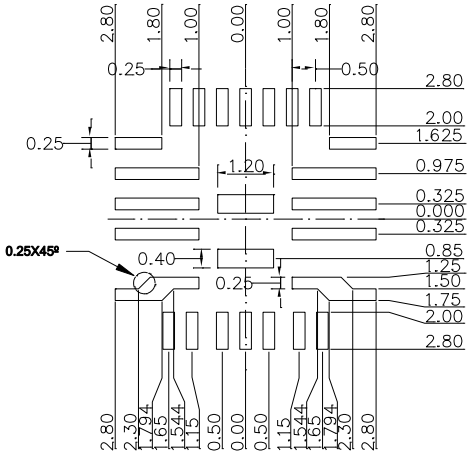
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) LAND PATTERNS OF PIN 2~4 AND 14~16 HAVE THE SAME LENGTH AND WIDTH.
2) LAND PATTERNS OF PIN 5 AND PIN13 HAVE THE SAME LENGTH AND WIDTH.
3) ALL DIMENSIONS ARE IN MILLIMETERS.
4) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
5) REFERENCEIS MO-220.
6) DRAWING IS NOT TO SCALE.