MPQ4372

36V, 6A to 11A, Low-EMI, Scalable, Synchronous Step-Down Converters with ZDP™, AEC-Q100 Qualified

DESCRIPTION

The MPQ4372 is a configurable-frequency (200kHz to 2.5MHz), synchronous, step-down switching regulator with integrated low on-resistance high-side and low-side power MOSFETs (HS-FET and LS-FET, respectively). It offers a 6A to 11A output current (I_{OUT}) range and employs Zero-Delay PWM (ZDP™) control, an MPS-exclusive technology that delivers extremely fast transient response while reducing the need for costly external capacitors.

The wide 3.3V to 36V input voltage (V_{IN}) range accommodates a variety of step-down applications in automotive input environments. A 1.8µA shutdown mode quiescent current (I_{SHDN}) allows use in battery-powered applications. High power conversion efficiency across a wide load range is achieved by scaling down the switching frequency (f_{SW}) under light loads to reduce switching and gate driver losses.

An open-drain power good (PG) signal indicates whether the output voltage (V_{OUT}) is within 94% to 106% of its nominal voltage. Frequency foldback helps prevent inductor current (I_L) runaway during start-up. Thermal shutdown provides reliable, fault-tolerant operation. High duty cycle and low-dropout (LDO) mode support automotive cold-crank conditions.

The MPQ4372 is available in a QFN-23 (4mmx5mm) or TQFN-23 (4mmx5mm) package with wettable flanks. It is available in AEC-Q100 Grade 1.

FEATURES

- Designed for Automotive Transients
  - 3.3V to 36V Input Voltage (V_{IN}) Range
  - Load Dump Up to 42V
  - Low-Dropout (LDO) Mode
  - Available in AEC-Q100 Grade 1
- Highly Scalable Family
  - 6A to 11A Output Current (I_{OUT}) Versions in Pin-Compatible Family
  - Multi-Phase Capable up to 8 Phases

FEATURES *(continued)*

- Designed for High Performance and Reduced Component Overhead
  - ZDP™ Control for Fast Transient Response and Fewer Capacitors
  - ±1% Output Accuracy
  - Fixed- or Adjustable-Output Voltage (V_{OUT}) Options
  - Fixed Output [1]: 1V, 1.2V, 1.8V, 2.5V, 3.3V, 3.8V, or 5V
  - Adjustable V_{OUT} Up to 12V
  - Internal Soft Start (SS)
  - 30ns Minimum On Time
- High Efficiency for Increased Battery Life and Improved Thermals
  - 1.8µA Shutdown Current (I_{SHDN}), 3.5µA Standby Current
  - Advanced Asynchronous Modulation (AAM) Mode Increases Efficiency under Light Loads
  - Integrated Low-Resistance High-Side MOSFET (HS-FET, 22mΩ) and Low-Side MOSFET (LS-FET, 11mΩ)
- Optimized for Low EMC/EMI
  - 200kHz to 2.5MHz Configurable Switching Frequency (f_{SW})
  - Symmetric VIN Pinout Placement
  - Low Noise at High Frequency Bands via Quiet-FET™ Switching Technology
  - Frequency Spread Spectrum (FSS) Modulation
  - Synchronizable to an External Clock
  - CISPR 25 Class 5 Compliant
  - Available in a Mesh-Connect™ QFN-23 (4mmx5mm) or TQFN-23 (4mmx5mm) Package with Wettable Flanks
- Functional Safety System Design Capability
  - MPSafe™-Compatible: Functional Safety Supporting Document Available

MPSafe™ FuSa Compatible

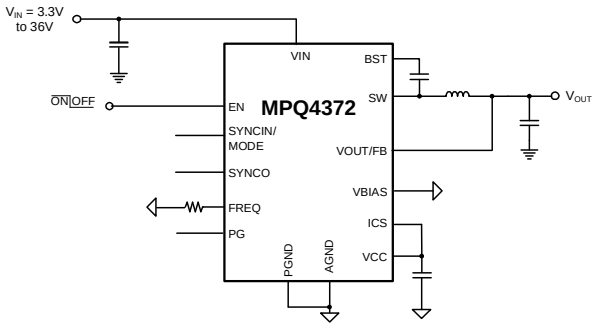
APPLICATIONS

- Automotive Infotainment
- Telematics
- Advanced Driver-Assistance Systems (ADAS)
- Industrial Power Systems

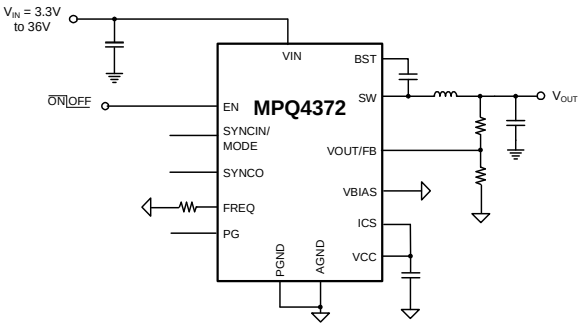
Note:

1) See the Ordering Information section on page 4 for fixed-output version information. Additional output voltages may be available. Contact MPS for details.

TYPICAL APPLICATION



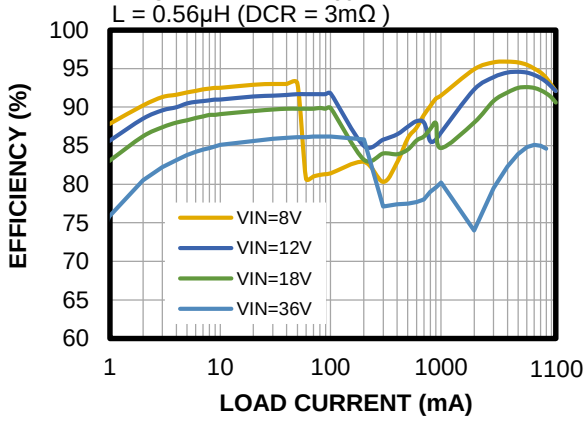
Fixed-Output Version



Adjustable-Output Version

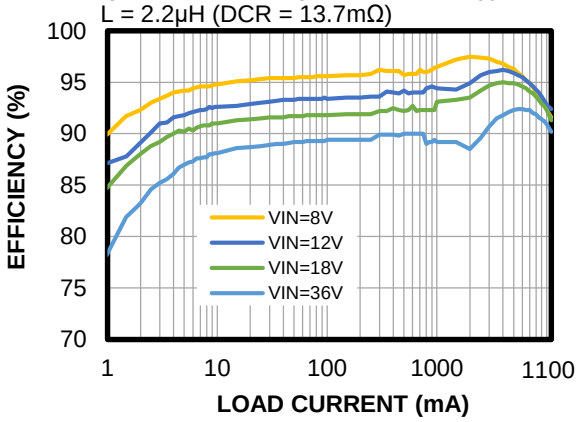
Efficiency vs. Load Current

AAM mode, V_{OUT} = 5V, f_{SW} = 2.2MHz, V_{BIAS} connected to V_{OUT}, L = 0.56µH (DCR = 3mΩ)



Efficiency vs. Load Current

AAM mode, V_{OUT} = 5V, f_{SW} = 410kHz, V_{BIAS} connected to V_{OUT}, L = 2.2µH (DCR = 13.7mΩ)



ORDERING INFORMATION

Part Number (2) (3) *	Package	Top Marking	MSL Rating**
MPQ4372GVE-xxxx-AEC1***	QFN-23 (4mmx5mm)	*See Below*	1
MPQ4372GVTE-xxxx-AEC1***	TQFN-23 (4mmx5mm)	*See Below*	1

* For Tape & Reel, add suffix -Z (e.g. MPQ4372GVE-xxxx-AEC1-Z).

**Moisture Sensitivity Level Rating

***Wettable Flank

Notes:

2) Contact MPS for details regarding fixed-output versions.
3) The detailed part number information can be indicated as MPQ4372-WXYZ. Table 1 shows the meaning of the four-digit code.

Table 1: Part Number Digit Code Naming Rules

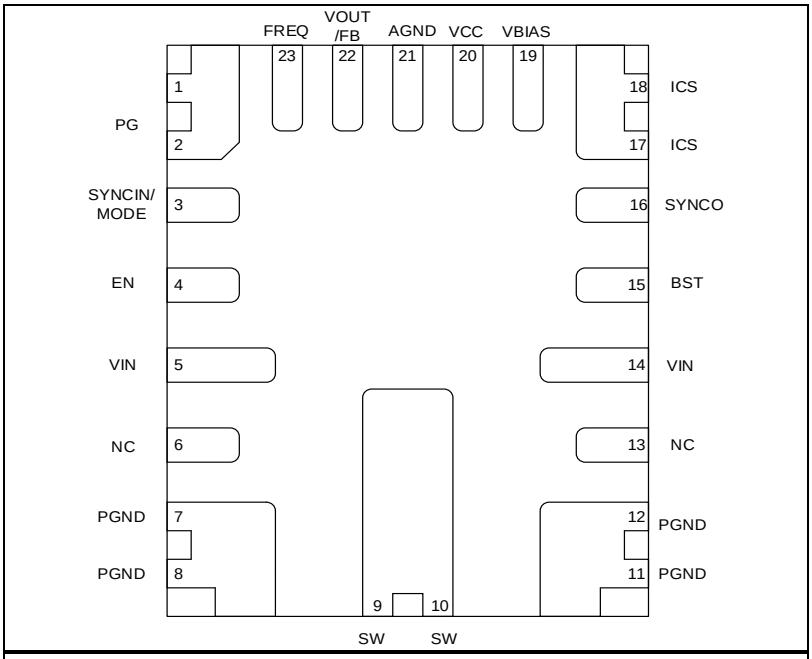
Digit Code	Naming Rule
W: Defines the nominal load current	1: 11A
	0: 10A
	8: 8A
	6: 6A
X: Defines the output voltage	0: Adjustable output
	1: Fixed 1V output
	A: Fixed 1.2V output
	B: Fixed 1.8V output
	2: Fixed 2.5V output
	3: Fixed 3.3V output
	4: Fixed 3.8V output
	5: Fixed 5V output
Y: Defines the frequency spread spectrum (FSS) configuration	0: With FSS
	A: Without FSS
Z: Defines the multi-phase capability	0: Single phase
	1: Multi-phase

TOP MARKING

MPSYWW
MP4372
LLLLLL
E

MPS: MPS prefix
Y: Year code
WW: Week code
MP4372: Part number
LLLLLL: Lot number
E: Wettable flank

PACKAGE REFERENCE



QFN-23 (4mmx5mm) and TQFN-23 (4mmx5mm)

PIN FUNCTIONS

Pin #	Name	Description
1, 2	PG	**Power good (PG) output and secondary phase selection.** For single-phase applications, PG is an open drain output. A pull-up resistor to a power source is needed if the PG function is used. PG goes high if the output voltage (V_{OUT}) is within 94% to 106% of the nominal voltage; PG goes low if V_{OUT} exceeds 107% or falls below 93% of the nominal voltage for as long as VCC is present of the nominal voltage. In single-phase applications, float PG when it is not used. When VCC is not present due to EN low, PG follows the state of its pull-up power source. PG will pull high if the pull-up power source is high (e.g. external source) or PG will pull low if the pull-up source is low (e.g. VCC). For multi-phase applications, if the device is in primary mode, the PG pin's function is the same as for single-phase applications. If the device is in secondary mode, connect a resistor to ground to set the phase shift. Then PG indication is disabled and does not pull high. The PG pin cannot be left floating for secondary devices. See the Power Good (PG) Indication or Phase Shift Setting (PG, Pins 1–2) section on page 70 for more information about multi-phase operation and how to configure the primary and secondary.
3	SYNCIN/ MODE	**External sync input and primary mode selection.** Apply a clock signal to this pin to synchronize the internal oscillator frequency to the external clock. If the device is set as the primary device, use an external clock or pull this pin high to enter forced continuous conduction mode (FCCM). Pull this pin low to enable discontinuous conduction mode (DCM) and pulse-skipping during light loads. SYNCIN/MODE has a weak internal pull-down resistor, so it can be floated to select advanced asynchronous modulation (AAM) mode. When the part is set as a secondary device, connect this pin to the primary device's SYNCO pin.
4	EN	**Enable.** Pulling this pin below the specified threshold (0.85V) shuts the chip down. Pulling EN above the specified threshold (1V) enables the chip. EN can be directly connected to VIN. Do not float this pin.
5, 14	VIN	**Input supply.** VIN supplies power to all the internal control circuitry and the power switch connected to SW. A proper decoupling capacitor must be connected between VIN and PGND at each side of the IC to minimize switching spikes.
6, 13	NC	**No connection.** The NC pin does not have an internal connection to the die. It can be left floating.
7, 8, 11, 12	PGND	**Power ground.** Connect the PGND pin to a large ground plane to ensure good heat dissipation.
9, 10	SW	**Switch node.** The SW pin is connected to the high-side MOSFET's (HS-FET's) source and the low-side MOSFET's (LS-FET's) drain. Connect the power inductor to this pin with a wide trace and limit its area to avoid EMI radiation.
15	BST	**Bootstrap.** The BST pin is the positive power supply for the HS-FET driver connected to SW. Connect a bypass capacitor between BST and SW.
16	SYNCO	**Sync output and secondary mode selection.** When SYNCO is in a high-impedance (Hi-Z) state, the device operates in primary operation mode, this pin outputs a clock signal in phase with the internal oscillator signal or external clock at the SYNCIN/MODE pin. In single-phase applications, this pin must be floating. In multi-phase applications, if this pin is tied to a low-impedance ground, voltage source, or clock, the MPQ4372 operates as a secondary device. When working as a secondary device, SYNCO selects the light-load operating mode (high for FCCM; low for AAM mode). In multi-phase applications, connect the SYNCO pin of all secondary devices together with the primary device's SYNC/MODE pin.
17, 18	ICS	**Current-sharing pin.** In single-phase applications, connect ICS to the VCC pin. In multi-phase applications, connect the ICS pins from all the parts together in order to improve current sharing between the different phases.

PIN FUNCTIONS *(continued)*

Pin #	Name	Description
19	VBIAS	**Internal LDO supply.** VBIAS is the power supply for the VCC regulator. The VCC regulator uses VBIAS as a power supply if the BIAS pin's voltage (V_{BIAS}) is between 4.5V and 5.5V. This pin can be connected directly to V_{OUT} when V_{OUT} is between 4.6V and 5.5V to improve the converter's efficiency, especially at high frequencies. Alternatively, connect this pin to another 5V rail if it is available in the system, and the current draw is <30mA. Add one decoupling capacitor between the VBIAS pin and AGND if this function is used. If there is no suitable power source for VBIAS, or the function is not used, connect this pin to V_{OUT} or AGND. If V_{OUT} > 5.5V, avoid connecting the VBIAS pin to the output. Avoid providing an external VBIAS voltage before V_{IN} is sufficiently high. Do not float this pin.
20	VCC	**Internal LDO output.** VCC supplies 5V of power to the internal control circuitry and gate drivers. A decoupling capacitor must be connected from VCC to AGND, placed close to this pin.
21	AGND	**Analog ground.** Connect the AGND pin to the DC/DC ground, close to the VCC capacitor.
22	VOUT/FB	**VOUT Regulation Input / Feedback Divider.** For the fixed-output version, connect to the output voltage directly to regulate it. For the adjustable-output version, set V_{OUT} by connecting FB to the center point between the external resistor divider from the output and AGND. The feedback voltage is 0.6V. Place the resistor divider as close to FB as possible. Avoid placing many vias on the FB traces.
23	FREQ	**Switching frequency configuration.** Connect a resistor from the FREQ pin to ground to set the switching frequency (f_{SW}).

ABSOLUTE MAXIMUM RATINGS (4)

VIN, EN .....-0.3V to +42V
SW ..... -0.3V to $V_{IN(MAX)}$ + 0.3V
BST ..... V_{SW} + 5.5V
VBIAS.....-0.3V to +6V
All other pins .....-0.3V to +6V
Continuous power dissipation (T_A = 25°C) (5) (9)
QFN-23 (4mmx5mm) 5.48W
TQFN-23 (4mmx5mm)..... 5.48W
Junction temperature (T_J) .....150°C
Lead temperature .....260°C
Storage temperature ..... -65°C to +150°C

ESD Ratings

Human body model (HBM) .....Class 2 (6)
Charged-device model (CDM) ..... Class C2b (7)

Recommended Operating Conditions

Input voltage (V_{IN}) .....3.3V to 36V
V_{BIAS}.....4.5V to 5.5V
Output voltage (V_{OUT}).....0.6V to 12V
Operating junction temp (T_J).... -40°C to +150°C

Thermal Resistance θ_{JA} θ_{JC}

QFN-23 (4mmx5mm)
JESD51-7.....41.2.....3.9....°C/W (8)
EVQ4372-V-00A.....22.8.....°C/W (9)

Ψ_{JT}
JESD51-7..... 0.5.....°C/W (8)
EVQ4372-V-00A.....1.14.... °C/W (9)

TQFN-23 (4mmx5mm)
JESD51-7.....41.2.....3.9....°C/W (8)

Ψ_{JT}
JESD51-7..... 0.4.....°C/W (8)

Notes:

4) Exceeding these ratings may damage the device.
5) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
6) Per AECQ100-002
7) Per AECQ100-011
8) Measured on a JESD51-7, 4-layer PCB. The values given in this table are only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application, the value of θ_{Jc} shows the thermal resistance from junction-to-case bottom. and the value of Ψ_{JT} shows the characterization parameter from junction-to-case top
9) Measured on an MPS standard EVB: 8.3cmx8.3cm, 2oz. copper thickness, 4-layer PCB. The value of Ψ_{JT} shows the characterization parameter from junction-to-case top.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, V_{EN} = 2V, T_J = -40°C to +150°C, typical values are at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Supply						
Input voltage (V_{IN}) under-voltage lockout (UVLO) rising threshold	$V_{IN\_UV\_RISING}$		3.6	3.8	4.1	V
V_{IN} UVLO falling threshold	$V_{IN\_UV\_FALLING}$		2.7	2.9	3.1	V
V_{IN} UVLO hysteresis	$V_{IN\_UV\_HYS}$			0.9		V
VIN quiescent current (10)	I_Q	FB = 0.63V, no load, SYNCIN/MODE = AGND (AAM mode), non-switching, T_J = -40 to +85°C		3.5	8.6	µA
		FB = 0.63V, no load, SYNCIN/MODE = AGND (AAM mode), non-switching, T_J = -40 to +125°C			15	µA
VIN quiescent current (switching) (10)	I_{Q_SLEEP}	SYNCIN/MODE = AGND (AAM mode), switching, V_{BIAS} = 5V, no load, T_J = -40 to +85°C		4.5	9	µA
		SYNCIN/MODE = AGND (AAM mode), switching, V_{BIAS} = 5V, no load, T_J = -40 to +125°C			16.5	µA
VIN active current (non-switching)	I_{Q_ACTIVE}	FB = 0.63V, no load, SYNCIN/MODE = VCC (FCCM), non-switching		1300	2300	µA
VIN shutdown current	I_{SHDN}	EN = 0V, T_J = -40°C to +85°C		1.8	4	µA
		EN = 0V			22.5	µA
V_{IN} over-voltage protection (OVP) threshold	$V_{IN\_OVP\_RISING}$		36	38	40	V
V_{IN} OVP hysteresis	$V_{IN\_OVP\_HYS}$			1		V
VCC and VBIAS						
VCC voltage	V_{CC}	I_{VCC} = 0, VCC from VIN	4.8	5	5.2	V
		I_{VCC} = 30mA, V_{BIAS} = 5V		4.95		V
VCC regulation		I_{VCC} = 30mA		1		%
VCC current limit	I_{LIMIT_VCC}	V_{CC} = 4V	89	120	167	mA
		V_{CC} = 0V	40	70	120	mA
VBIAS takeover rising threshold	$V_{BIAS-RISING}$			4.5		V
VBIAS takeover hysteresis				200		mV
Soft Start (SS)						
Soft-start time	t_{SS}	EN high to PG high	4	5	6	ms
Enable (EN) Function						
EN rising threshold	V_{EN_RISING}		0.8	1	1.2	V
EN falling threshold	$V_{EN\_FALLING}$		0.65	0.85	1.05	V
EN hysteresis voltage	V_{EN_HYS}			150		mV

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{EN} = 2V, T_J = -40°C to +150°C, typical values are at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Output and Regulation						
FB voltage (adjustable-output version)	V_{FB}		594	600	606	mV
V_{OUT} regulation voltage (fixed-output version)	V_{OUT_REG}	V_{IN} = 3.3V to 36V	-1		+1	%
FB leakage in fixed-output version	I_{VOUT}	V_{OUT} = V_{OUT_REG}		2.3		µA
FB leakage in adjustable-output version		V_{FB} = 0.63V		1	100	nA
Switches and Frequency						
Minimum on time (10)	t_{ON_MIN}		12	30	35	ns
Minimum off time (10)	t_{OFF_MIN}			100	125	ns
Minimum off time in low-dropout (LDO) mode (10)	$t_{OFF\_MIN\_DROPOUT}$			50	60	ns
Switch Leakage Current	I_{SW_LKG}			0.01	9	µA
High-side MOSFET (HS-FET) on resistance	$R_{DS(ON)\_HS}$	V_{BST} - V_{SW} = 5V		22	42	mΩ
Low-side MOSFET (LS-FET) on resistance	$R_{DS(ON)\_LS}$	V_{CC} = 5V		11	22	mΩ
Switching frequency	f_{SW}	R_{FREQ} = 88.7kΩ	370	410	450	kHz
		R_{FREQ} = 33kΩ	900	1000	1100	kHz
		R_{FREQ} = 15kΩ	1980	2200	2420	kHz
SYNCIN and SYNCO						
SYNCIN voltage rising threshold	V_{SYNC_RISING}				1.4	V
SYNCIN voltage falling threshold	$V_{SYNC\_FALLING}$		0.4			V
SYNCIN timeout	t_{MODE}	SYNCIN/MODE low to DCM	30		65	µs
SYNCIN clock range	f_{SYNC}	% of freerunning frequency (f_{SW})	90		110	%
SYNCO high voltage	V_{SYNCO_HIGH}	I_{SYNCO} = -1mA	3.3	4.5		V
SYNCO low voltage	V_{SYNCO_LOW}	I_{SYNCO} = 1mA			0.4	V
Frequency Spread Spectrum (FSS) (10)						
FSS modulation frequency low	FSS_LF_MOD			15		kHz
FSS span for FSS_LF_MOD	FSS_LF_SPAN			6.2		%
FSS modulation frequency high	FSS_HF_MOD			120		kHz
FSS span for FSS_HF_MOD	FSS_HF_SPAN			2.5		%

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{EN} = 2V, T_J = -40°C to +150°C, typical values are at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
BST						
BST-SW refresh rising threshold	$V_{UVBST-SW-RISING}$			2.5		V
BST-SW refresh falling threshold	$V_{UVBST-SW-FALLING}$			2.3		V
BST-SW refresh hysteresis	$V_{UVBST-SW\_HYS}$		0.19			V
ICS						
Current-sharing gain	G_{CS}			30		mV/A
Power Good (PG) Function						
PG rising threshold	V_{PGVTH_RISING}	V_{OUT} rising	91	94	97	% of V_{OUT}
		V_{OUT} falling	103	106	109	
PG falling threshold	$V_{PGVTH\_FALLING}$	V_{OUT} falling	90	93	96	
		V_{OUT} rising	104	107	110	
PG trip threshold hysteresis	V_{PGVTH_HYS}			1		
PG output voltage low	V_{PG_LOW}	I_{SINK} = 1mA		10	100	mV
PG rising deglitch time	$t_{PG\_R\_DELAY}$			120		µs
PG falling deglitch time	$t_{PG\_F\_DELAY}$			100		µs
Protections						
High-side (HS) current limit (11)	I_{LIMIT_HS}	For MPQ4372-1XYZ	16.6	19	22	A
		For MPQ4372-0XYZ	15.2	17.2	19	
		For MPQ4372-8XYZ	12.6	13.8	15	
		For MPQ4372-6XYZ	8.6	10.3	12	
Low-side (LS) valley current limit (11)	I_{LIMIT_LS}	For MPQ4372-1XYZ	11.2	13.2		A
		For MPQ4372-0XYZ	10.2	13	15.2	
		For MPQ4372-8XYZ	8.2	9.6		
		For MPQ4372-6XYZ	6.2	7.2		
Zero-current detection (ZCD) threshold	I_{ZCD}	AAM mode	0	100	300	mA
LS reverse current limit	$I_{LIMIT\_REVERSE}$	FCCM	-5.2	-4	-2.8	A
Thermal shutdown (10)	T_{SD}		150	170		°C
Thermal shutdown hysteresis (10)	T_{SD_HYS}			20		°C

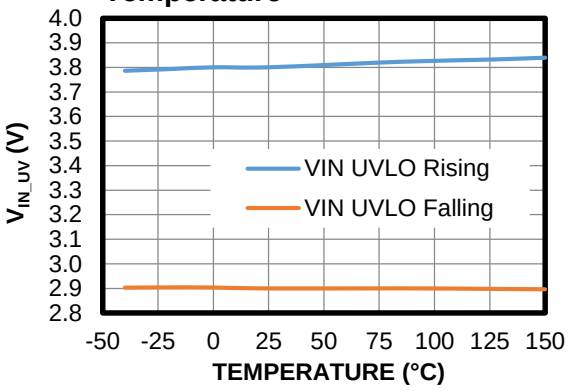
Notes:

10) Derived from bench characterization; not tested in production.
11) Cannot test in production for MPQ4372-1XYZ/8XYZ/6XYZ. Guaranteed by design and bench test characterization.

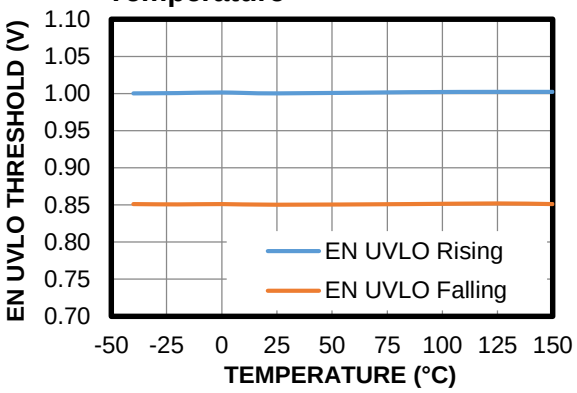
TYPICAL CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 5V, T_J = -40°C to +150°C, unless otherwise noted.

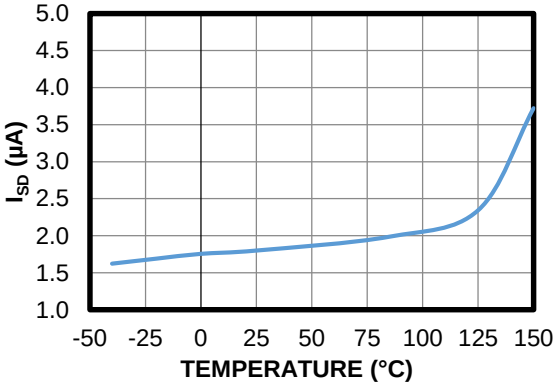
V_{IN} UVLO Threshold vs. Temperature



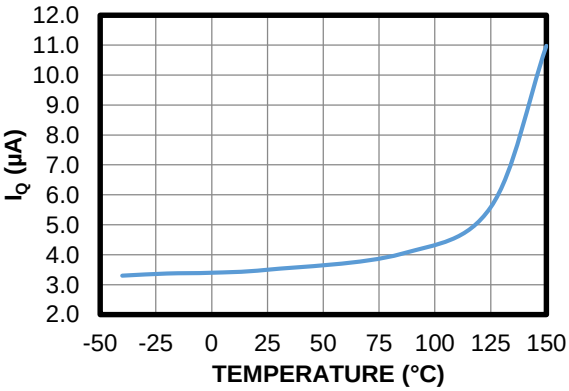
EN UVLO Threshold vs. Temperature



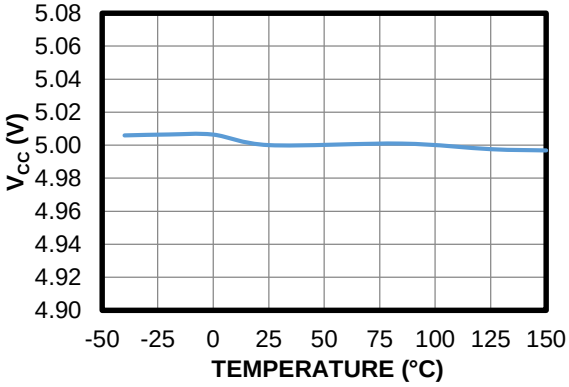
V_{IN} Shutdown Current vs. Temperature



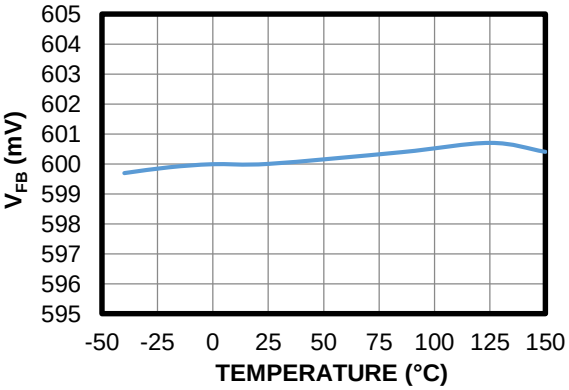
Quiescent Current vs. Temperature



V_{CC} vs. Temperature



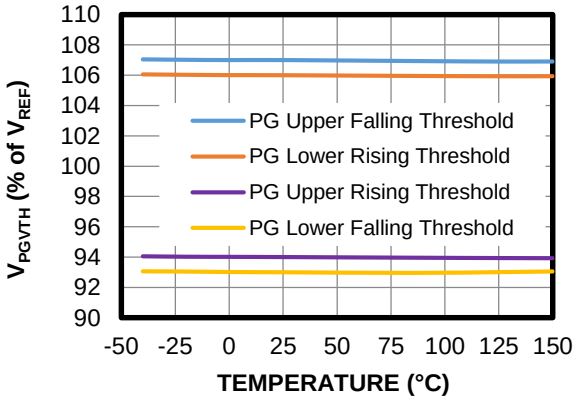
FB Voltage vs. Temperature



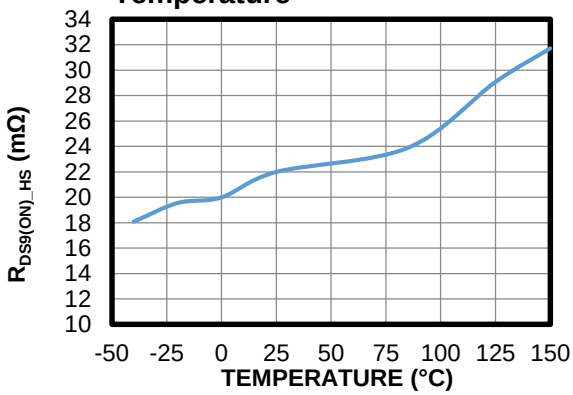
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, T_J = -40°C to +150°C, unless otherwise noted.

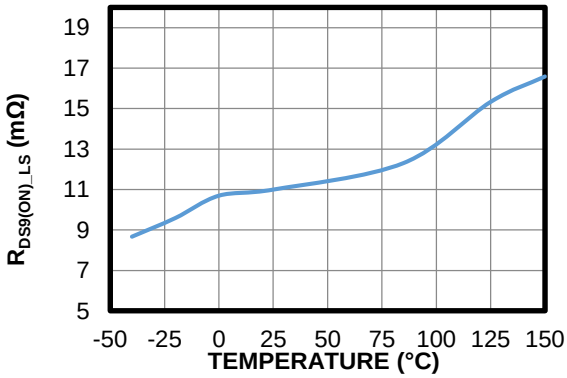
PG Rising/Falling Threshold vs. Temperature



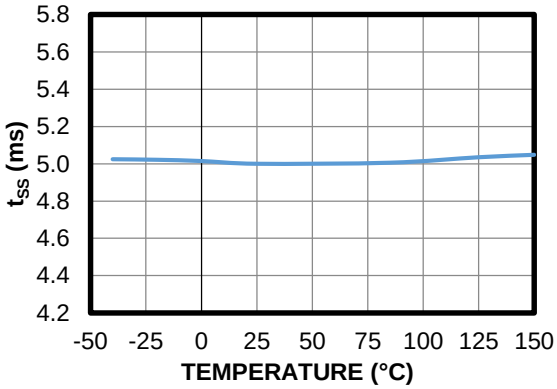
HS-FET On Resistance vs. Temperature



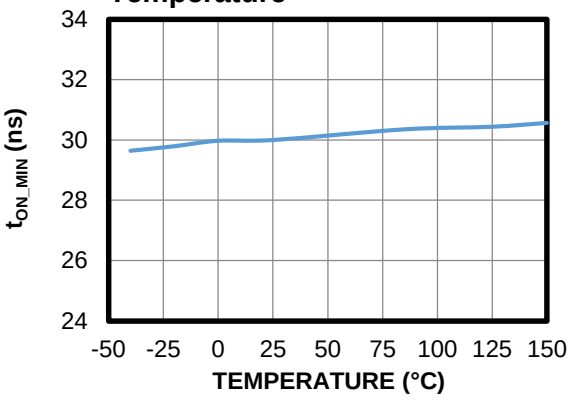
LS-FET On Resistance vs. Temperature



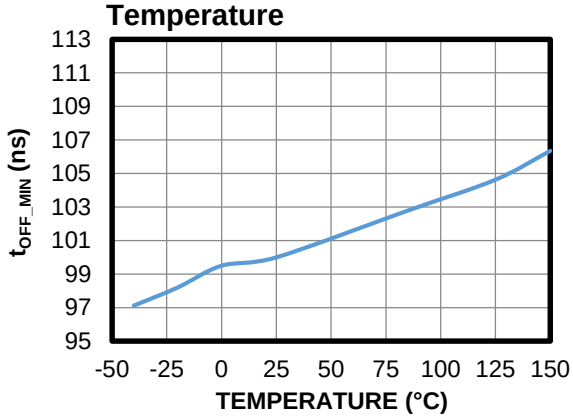
Soft-Start Time vs. Temperature



HS-FET Minimum On Time vs. Temperature



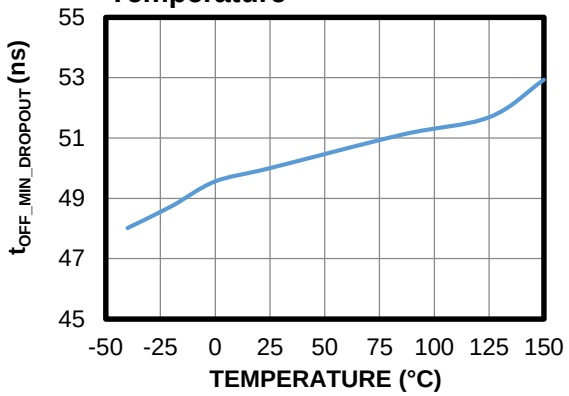
HS-FET Minimum Off Time vs. Temperature



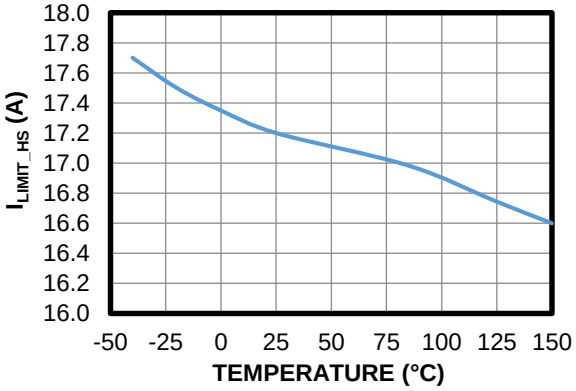
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, T_J = -40°C to +150°C, unless otherwise noted.

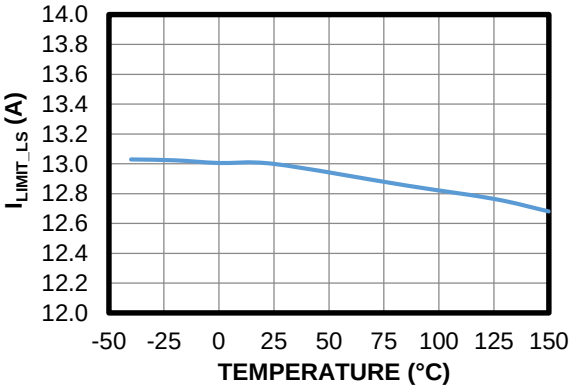
HS-FET Minimum Off Time in Low-Dropout Mode vs. Temperature



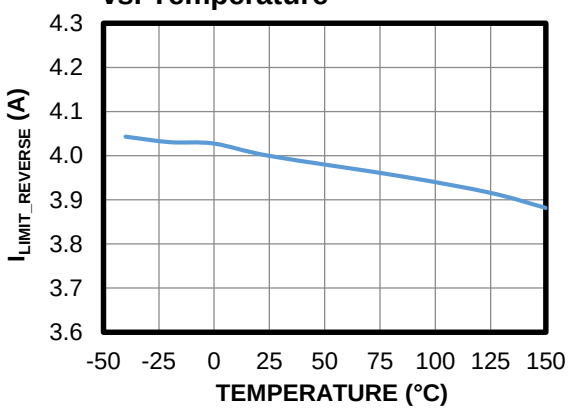
High-Side Current LImit vs. Temperature for the MPQ4372-0000



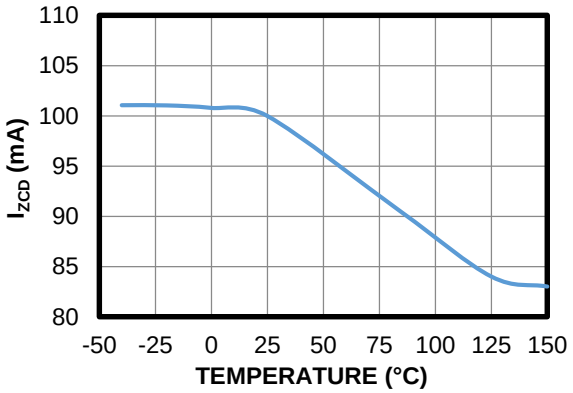
Low-Side Current LImit vs. Temperature for the MPQ4372-0000



Low-Side Reverse Current LImit vs. Temperature

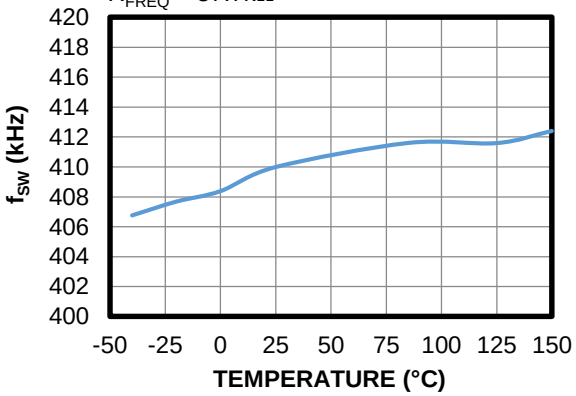


Zero-Current Detection Threshold vs. Temperature



Switching Frequency vs. Temperature

R_{FREQ} = 87.7kΩ

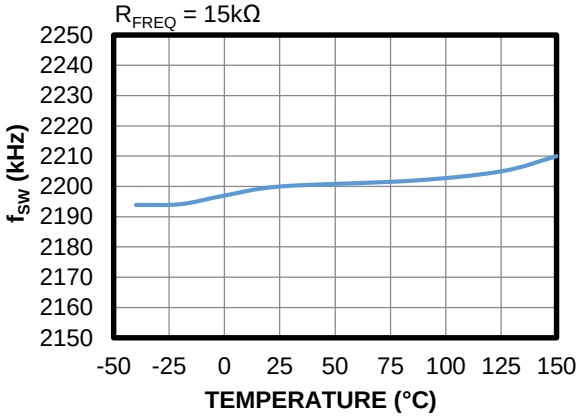


TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, T_J = -40°C to +150°C, unless otherwise noted.

Switching Frequency vs. Temperature

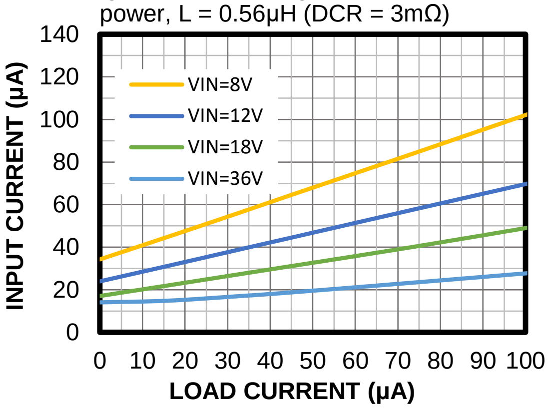
R_{FREQ} = 15kΩ



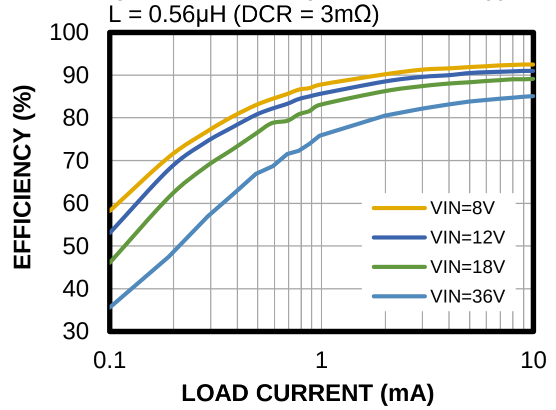
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 0.56μH (DCR = 3mΩ), T_A = 25°C, unless otherwise noted.

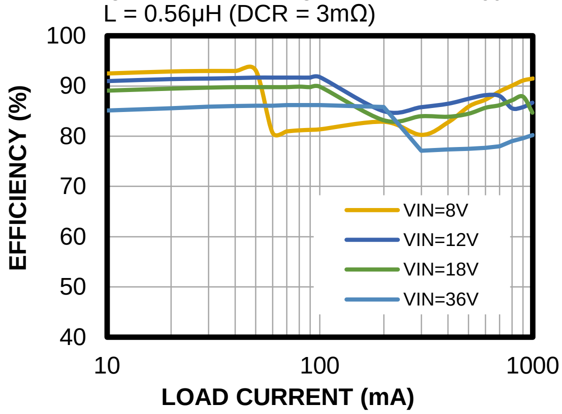
Input Current vs. Load Current
AAM mode, V_{OUT} = 5V,
f_{SW} = 2.2MHz, V_{BIAS} connected to 5V
power, L = 0.56μH (DCR = 3mΩ)



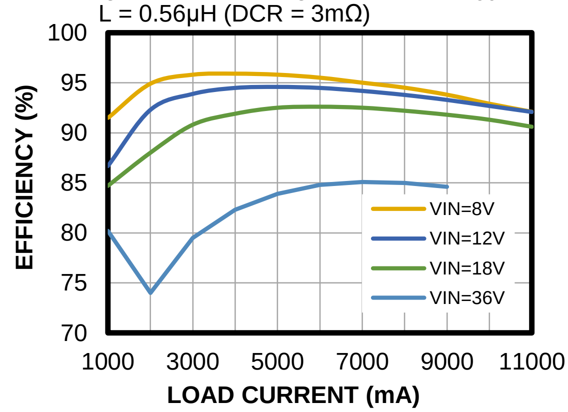
Efficiency vs. Load Current
AAM mode, V_{OUT} = 5V,
f_{SW} = 2.2MHz, V_{BIAS} connected to V_{OUT},
L = 0.56μH (DCR = 3mΩ)



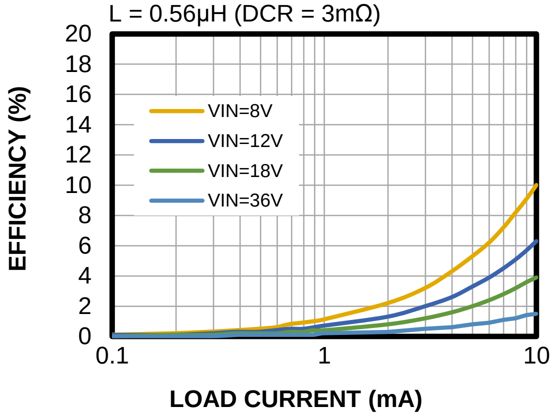
Efficiency vs. Load Current
AAM mode, V_{OUT} = 5V,
f_{SW} = 2.2MHz, V_{BIAS} connected to V_{OUT},
L = 0.56μH (DCR = 3mΩ)



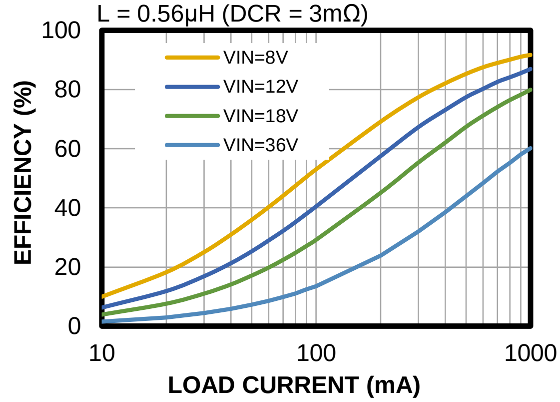
Efficiency vs. Load Current
AAM mode, V_{OUT} = 5V,
f_{SW} = 2.2MHz, V_{BIAS} connected to V_{OUT},
L = 0.56μH (DCR = 3mΩ)



Efficiency vs. Load Current
FCCM, V_{OUT} = 5V, f_{SW} = 2.2MHz,
V_{BIAS} connected to V_{OUT},
L = 0.56μH (DCR = 3mΩ)



Efficiency vs. Load Current
FCCM, V_{OUT} = 5V, f_{SW} = 2.2MHz,
V_{BIAS} connected to V_{OUT},
L = 0.56μH (DCR = 3mΩ)

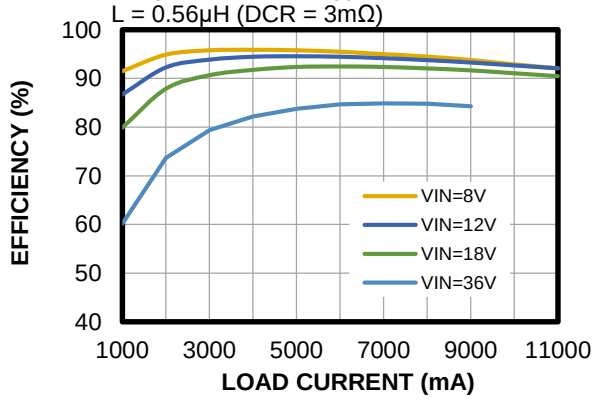


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 0.56µH (DCR = 3mΩ), T_A = 25°C, unless otherwise noted.

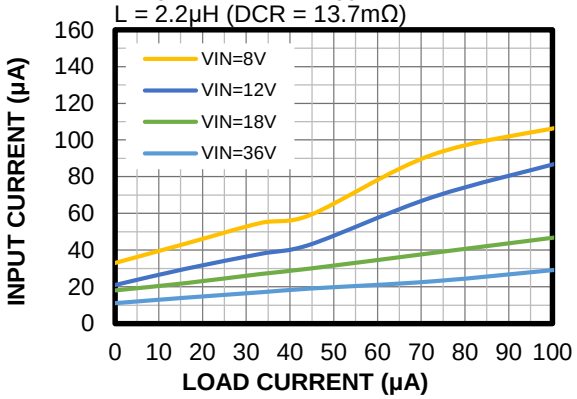
Efficiency vs. Load Current

FCCM, V_{OUT} = 5V, f_{SW} = 2.2MHz,
V_{BIAS} connected to V_{OUT},
L = 0.56µH (DCR = 3mΩ)



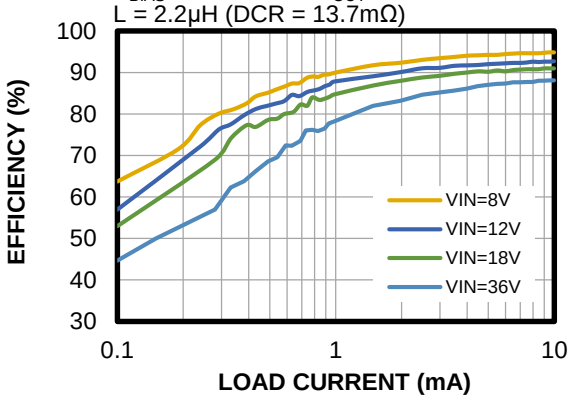
Input Current vs. Load Current

AAM mode, V_{OUT} = 5V, f_{SW} = 410kHz,
V_{BIAS} connected to V_{OUT},
L = 2.2µH (DCR = 13.7mΩ)



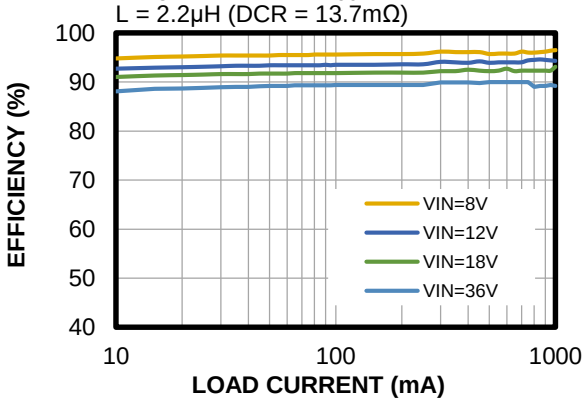
Efficiency vs. Load Current

AAM mode, V_{OUT} = 5V, f_{SW} = 410kHz,
V_{BIAS} connected to V_{OUT},
L = 2.2µH (DCR = 13.7mΩ)



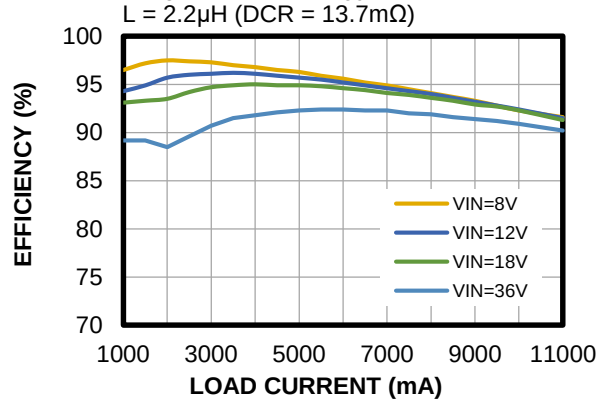
Efficiency vs. Load Current

AAM mode, V_{OUT} = 5V, f_{SW} = 410kHz,
V_{BIAS} connected to V_{OUT},
L = 2.2µH (DCR = 13.7mΩ)



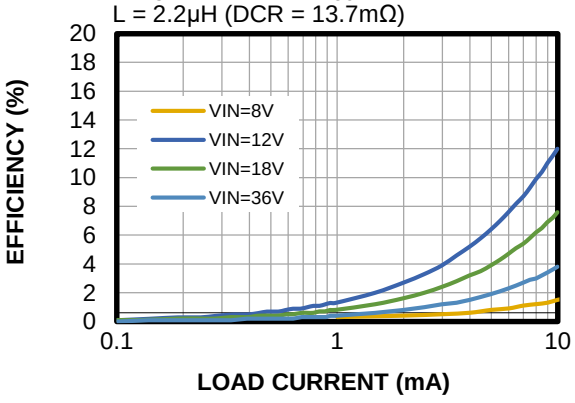
Efficiency vs. Load Current

AAM mode, V_{OUT} = 5V, f_{SW} = 410kHz,
V_{BIAS} connected to V_{OUT},
L = 2.2µH (DCR = 13.7mΩ)



Efficiency vs. Load Current

FCCM, V_{OUT} = 5V, f_{SW} = 410kHz,
V_{BIAS} connected to V_{OUT},
L = 2.2µH (DCR = 13.7mΩ)

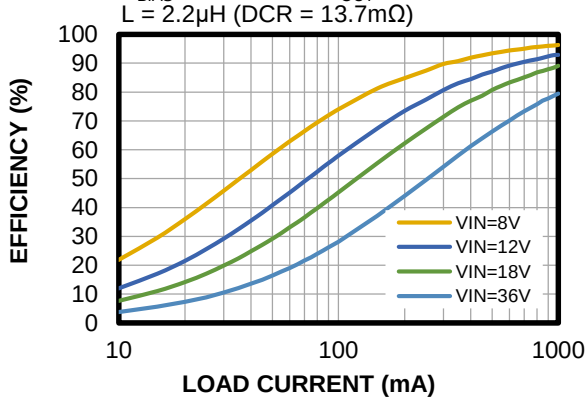


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 0.56µH (DCR = 3mΩ), T_A = 25°C, unless otherwise noted.

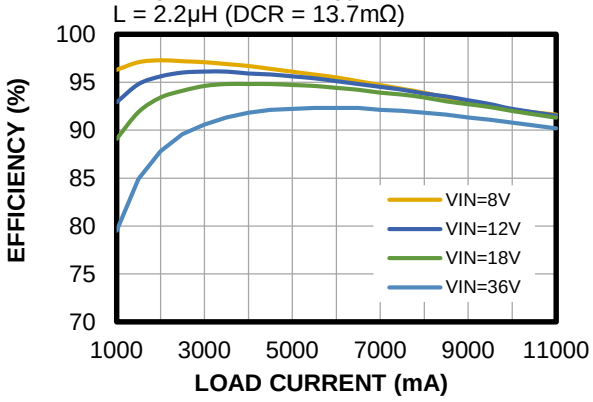
Efficiency vs. Load Current

FCCM, V_{OUT} = 5V, f_{SW} = 410kHz, V_{BIAS} connected to V_{OUT}, L = 2.2µH (DCR = 13.7mΩ)



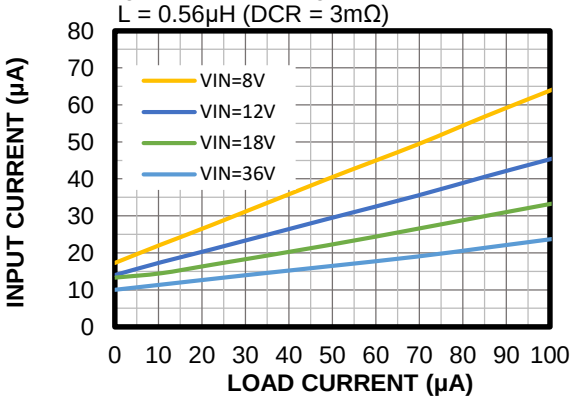
Efficiency vs. Load Current

FCCM, V_{OUT} = 5V, f_{SW} = 410kHz, V_{BIAS} connected to V_{OUT}, L = 2.2µH (DCR = 13.7mΩ)



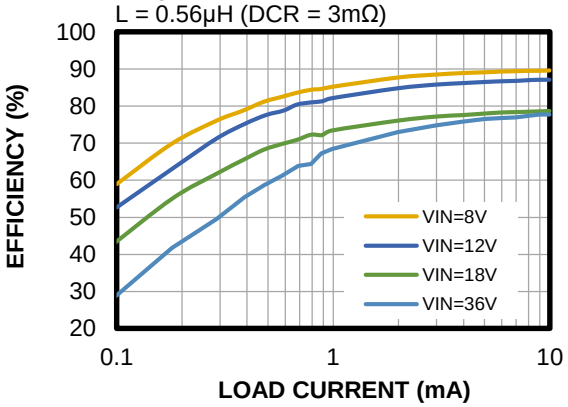
Input Current vs. Load Current

AAM mode, V_{OUT} = 3.3V, f_{SW} = 2.2MHz, V_{BIAS} connected to GND, L = 0.56µH (DCR = 3mΩ)



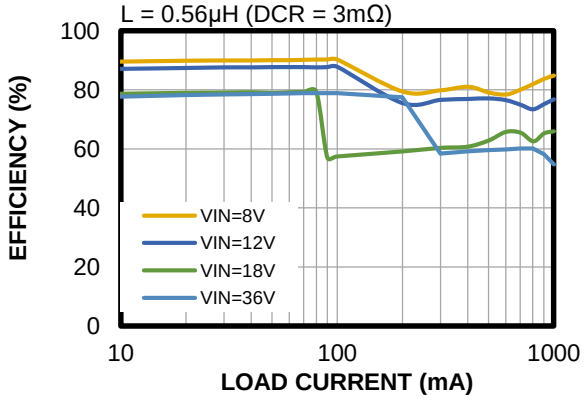
Efficiency vs. Load Current

AAM mode, V_{OUT} = 3.3V, f_{SW} = 2.2MHz, V_{BIAS} connected to GND, L = 0.56µH (DCR = 3mΩ)



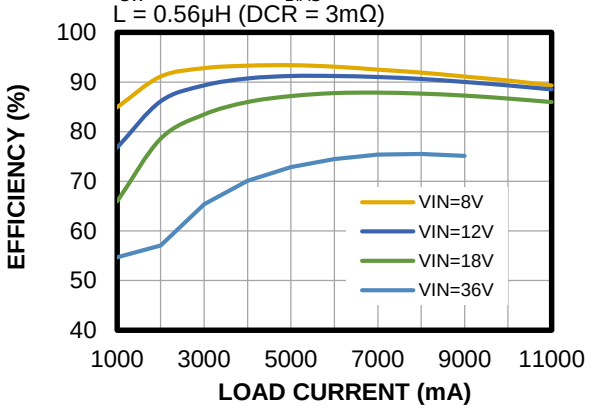
Efficiency vs. Load Current

AAM mode, V_{OUT} = 3.3V, f_{SW} = 2.2MHz, V_{BIAS} connected to GND, L = 0.56µH (DCR = 3mΩ)



Efficiency vs. Load Current

AAM mode, V_{OUT} = 3.3V, f_{SW} = 2.2MHz, V_{BIAS} connected to GND, L = 0.56µH (DCR = 3mΩ)

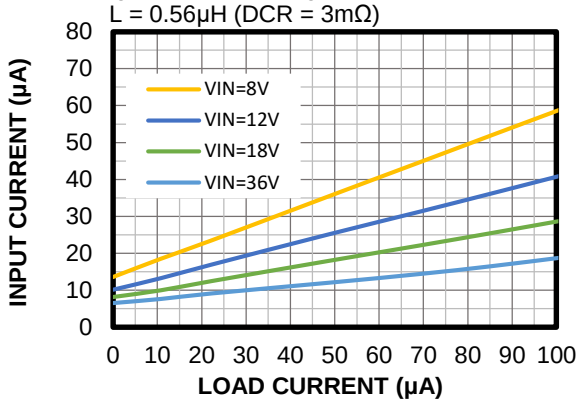


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 0.56µH (DCR = 3mΩ), T_A = 25°C, unless otherwise noted.

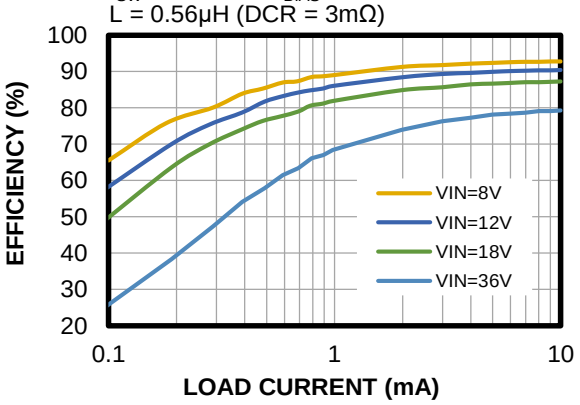
Input Current vs. Load Current

AAM mode, V_{OUT} = 3.3V,
f_{SW} = 2.2MHz, V_{BIAS} connected to 5V power,
L = 0.56µH (DCR = 3mΩ)



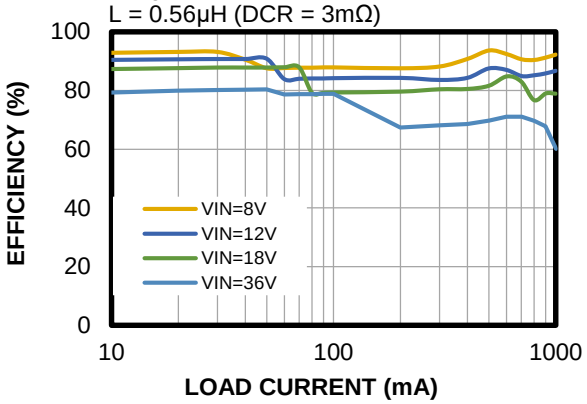
Efficiency vs. Load Current

AAM mode, V_{OUT} = 3.3V,
f_{SW} = 2.2MHz, V_{BIAS} connected to 5V power,
L = 0.56µH (DCR = 3mΩ)



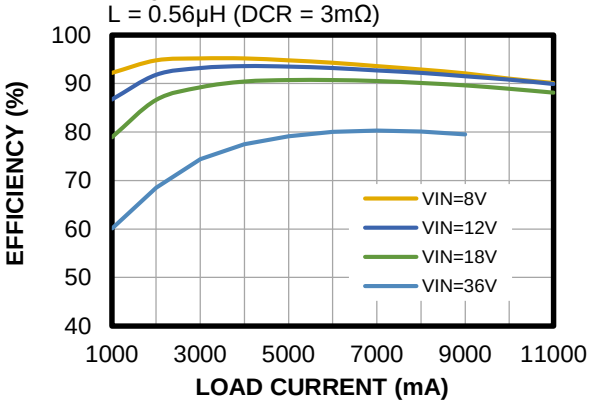
Efficiency vs. Load Current

AAM mode, V_{OUT} = 3.3V, f_{SW} = 2.2MHz,
V_{BIAS} connected to 5V power,
L = 0.56µH (DCR = 3mΩ)



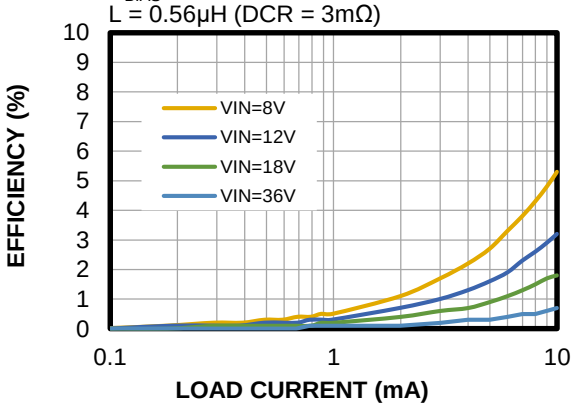
Efficiency vs. Load Current

AAM mode, V_{OUT} = 3.3V, f_{SW} = 2.2MHz,
V_{BIAS} connected to 5V power,
L = 0.56µH (DCR = 3mΩ)



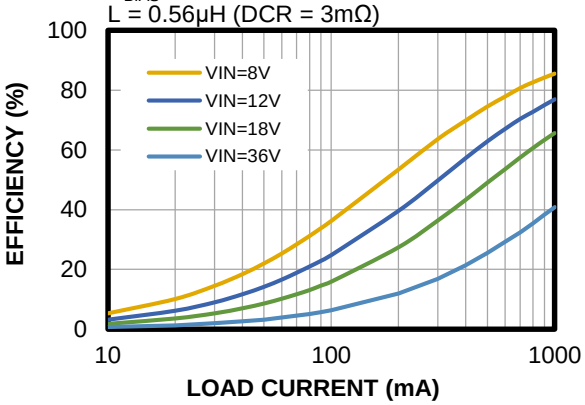
Efficiency vs. Load Current

FCCM, V_{OUT} = 3.3V, f_{SW} = 2.2MHz,
V_{BIAS} connected to GND,
L = 0.56µH (DCR = 3mΩ)



Efficiency vs. Load Current

FCCM, V_{OUT} = 3.3V, f_{SW} = 2.2MHz,
V_{BIAS} connected to GND,
L = 0.56µH (DCR = 3mΩ)

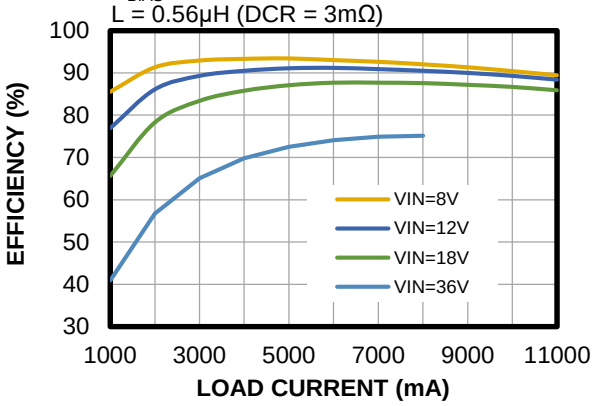


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 0.56µH (DCR = 3mΩ), T_A = 25°C, unless otherwise noted.

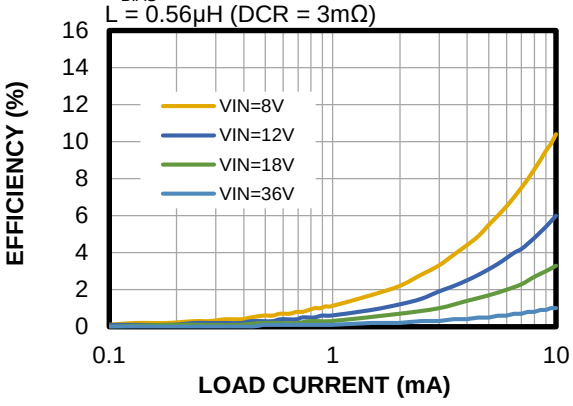
Efficiency vs. Load Current

FCCM, V_{OUT} = 3.3V, f_{SW} = 2.2MHz,
V_{BIAS} connected to GND,
L = 0.56µH (DCR = 3mΩ)



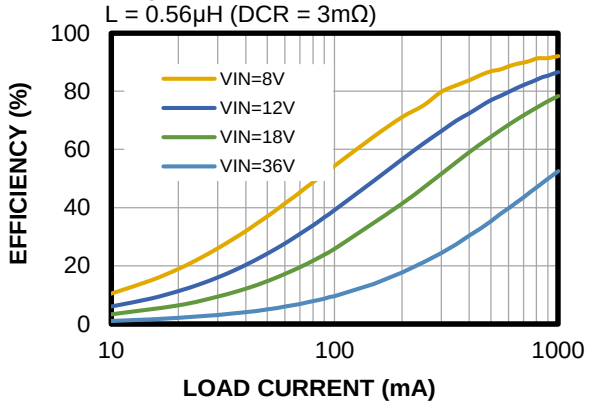
Efficiency vs. Load Current

FCCM, V_{OUT} = 3.3V, f_{SW} = 2.2MHz,
V_{BIAS} connected to 5V power,
L = 0.56µH (DCR = 3mΩ)



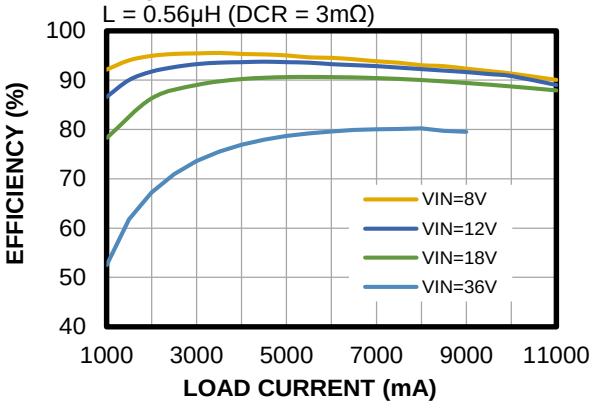
Efficiency vs. Load Current

FCCM, V_{OUT} = 3.3V, f_{SW} = 2.2MHz,
V_{BIAS} connected to 5V power,
L = 0.56µH (DCR = 3mΩ)



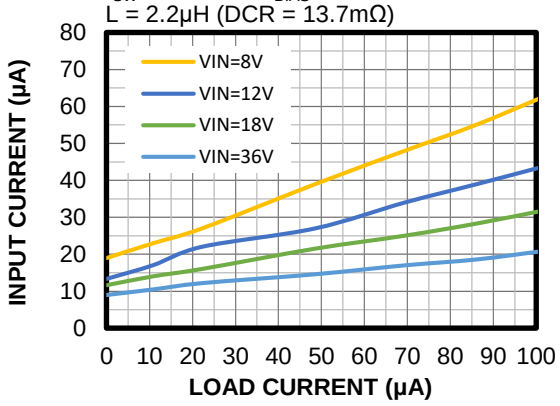
Efficiency vs. Load Current

FCCM, V_{OUT} = 3.3V, f_{SW} = 2.2MHz,
V_{BIAS} connected to 5V power,
L = 0.56µH (DCR = 3mΩ)



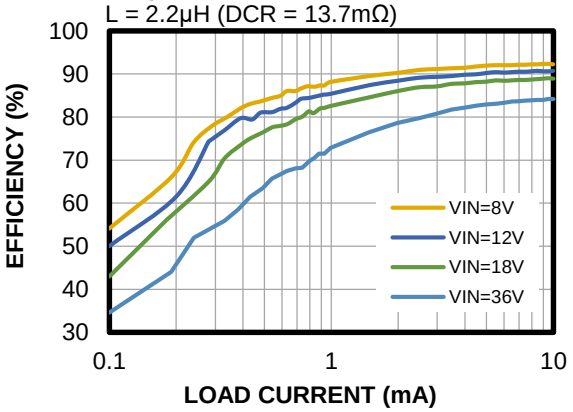
Input Current vs. Load Current

AAM mode, V_{OUT} = 3.3V,
f_{SW} = 410kHz, V_{BIAS} connected to GND,
L = 2.2µH (DCR = 13.7mΩ)



Efficiency vs. Load Current

AAM mode, V_{OUT} = 3.3V, f_{SW} = 410kHz,
V_{BIAS} connected to GND,
L = 2.2µH (DCR = 13.7mΩ)

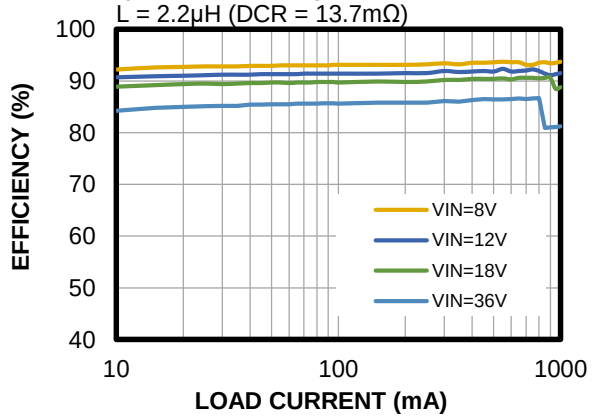


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 0.56µH (DCR = 3mΩ), T_A = 25°C, unless otherwise noted.

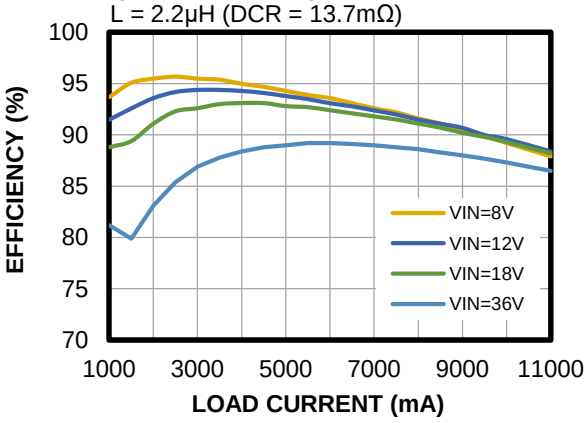
Efficiency vs. Load Current

AAM mode, V_{OUT} = 3.3V,
f_{SW} = 410kHz, V_{BIAS} connected to GND,
L = 2.2µH (DCR = 13.7mΩ)



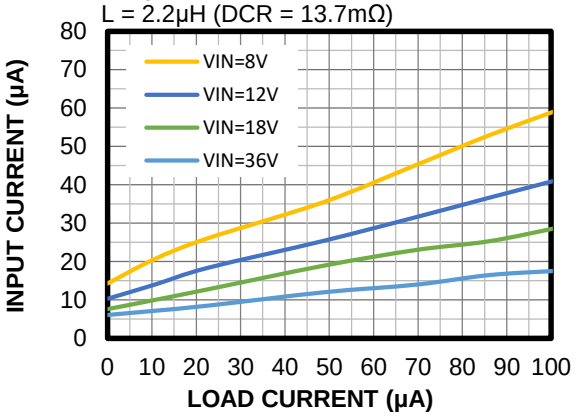
Efficiency vs. Load Current

AAM mode, V_{OUT} = 3.3V,
f_{SW} = 410kHz, V_{BIAS} connected to GND,
L = 2.2µH (DCR = 13.7mΩ)



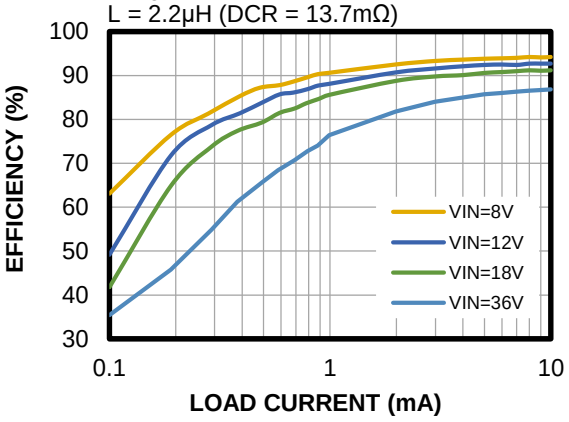
Input Current vs. Load Current

AAM mode, V_{OUT} = 3.3V, f_{SW} = 410kHz,
V_{BIAS} connected to 5V power,
L = 2.2µH (DCR = 13.7mΩ)



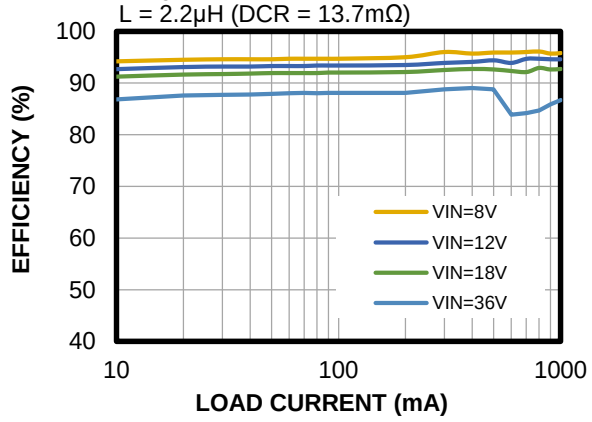
Efficiency vs. Load Current

AAM mode, V_{OUT} = 3.3V, f_{SW} = 410kHz,
V_{BIAS} connected to 5V power,
L = 2.2µH (DCR = 13.7mΩ)



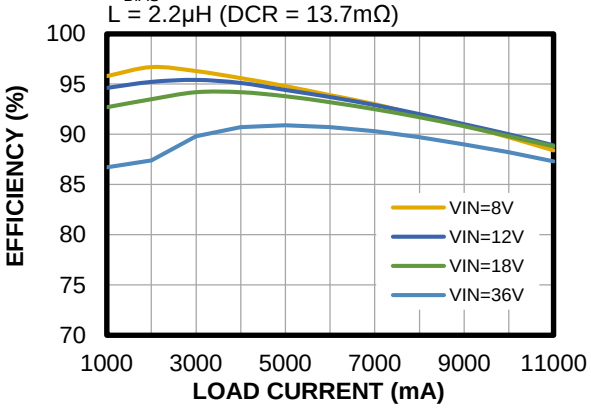
Efficiency vs. Load Current

AAM mode, V_{OUT} = 3.3V, f_{SW} = 410kHz,
V_{BIAS} connected to 5V power,
L = 2.2µH (DCR = 13.7mΩ)



Efficiency vs. Load Current

AAM mode, V_{OUT} = 3.3V, f_{SW} = 410kHz,
V_{BIAS} connected to 5V power,
L = 2.2µH (DCR = 13.7mΩ)

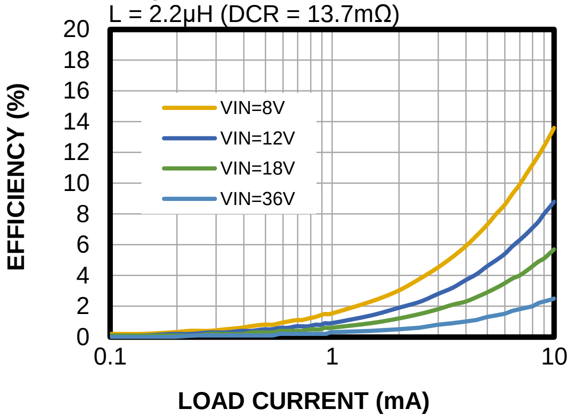


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 0.56µH (DCR = 3mΩ), T_A = 25°C, unless otherwise noted.

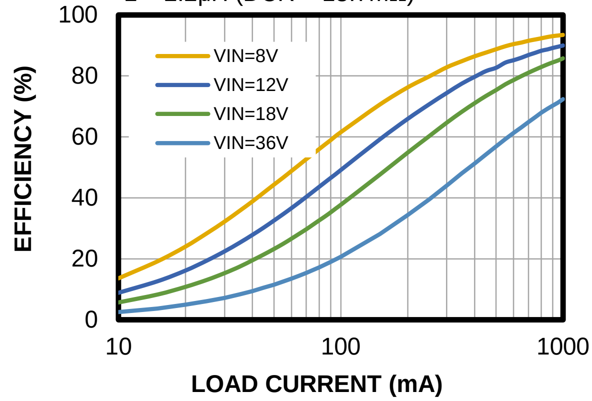
Efficiency vs. Load Current

FCCM, V_{OUT} = 3.3V, f_{SW} = 410kHz, V_{BIAS} connected to GND, L = 2.2µH (DCR = 13.7mΩ)



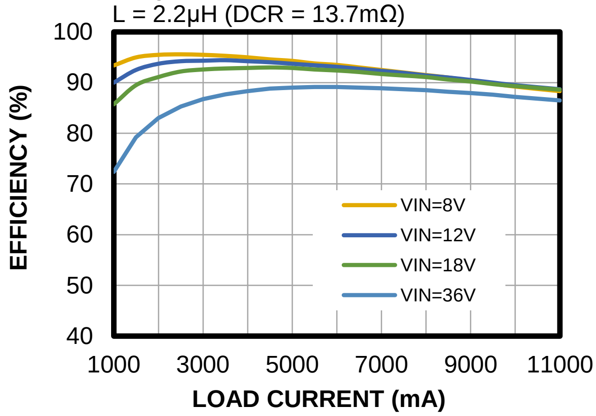
Efficiency vs. Load Current

FCCM, V_{OUT} = 3.3V, f_{SW} = 410kHz, V_{BIAS} connected to GND, L = 2.2µH (DCR = 13.7mΩ)



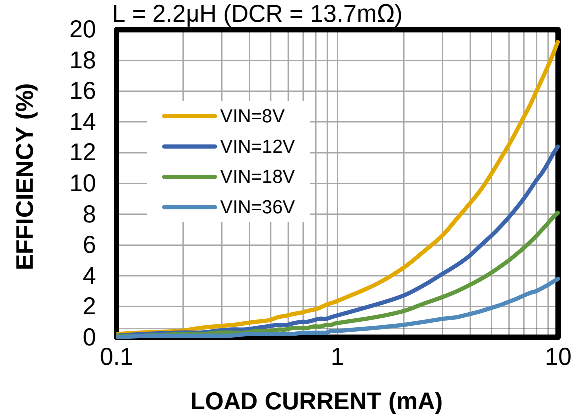
Efficiency vs. Load Current

FCCM, V_{OUT} = 3.3V, f_{SW} = 410kHz, V_{BIAS} connected to GND, L = 2.2µH (DCR = 13.7mΩ)



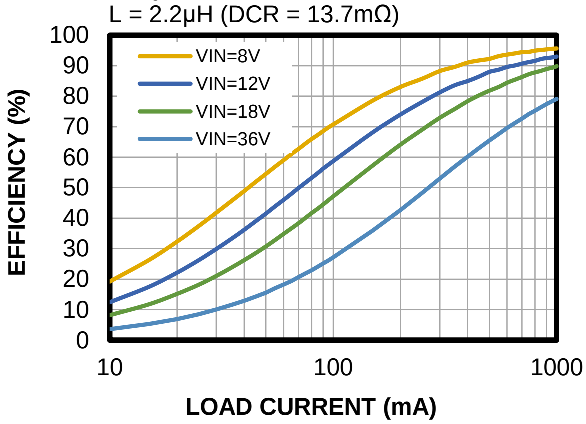
Efficiency vs. Load Current

FCCM, V_{OUT} = 3.3V, f_{SW} = 410kHz, V_{BIAS} connected to 5V power, L = 2.2µH (DCR = 13.7mΩ)



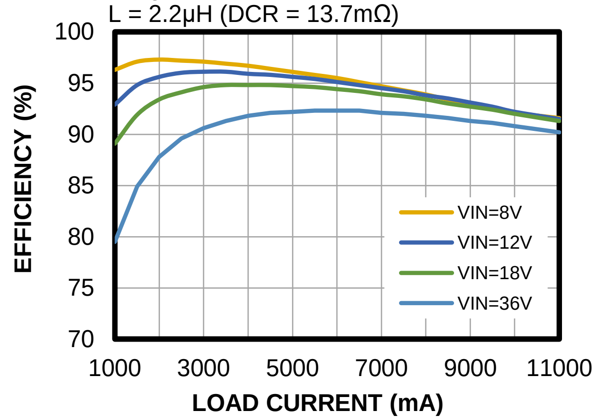
Efficiency vs. Load Current

AAM mode, V_{OUT} = 3.3V, f_{SW} = 410kHz, V_{BIAS} connected to 5V power, L = 2.2µH (DCR = 13.7mΩ)



Efficiency vs. Load Current

AAM mode, V_{OUT} = 3.3V, f_{SW} = 410kHz, V_{BIAS} connected to 5V power, L = 2.2µH (DCR = 13.7mΩ)

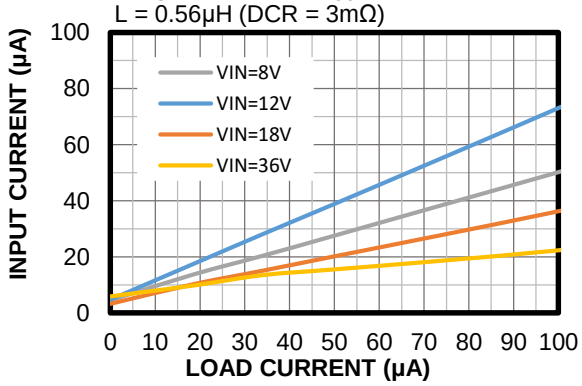


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 0.56µH (DCR = 3mΩ), T_A = 25°C, unless otherwise noted.

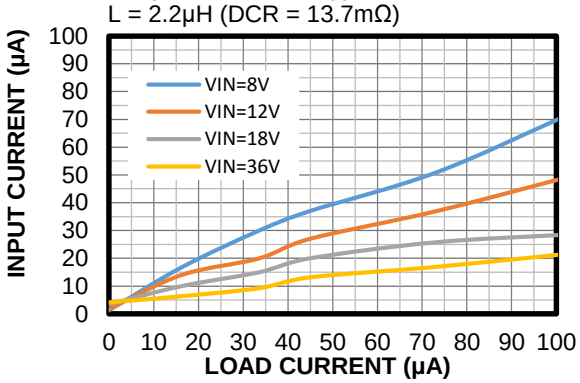
Input Current vs. Load Current the for MPQ4372-x5xx

AAM mode, V_{OUT} = 5V, f_{SW} = 2.2MHz, V_{BIAS} connected to V_{OUT}, L = 0.56µH (DCR = 3mΩ)



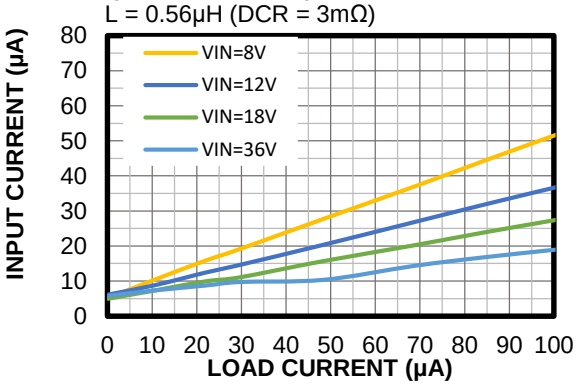
Input Current vs. Load Current for the MPQ4372-x5xx

AAM mode, V_{OUT} = 5V, f_{SW} = 410kHz, V_{BIAS} connected to V_{OUT}, L = 2.2µH (DCR = 13.7mΩ)



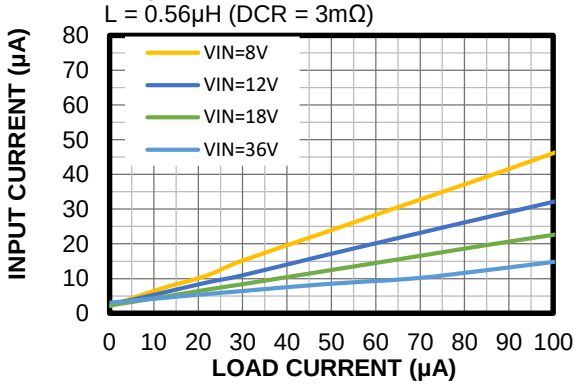
Input Current vs. Load Current for the MPQ4372-x3xx

AAM mode, V_{OUT} = 3.3V, f_{SW} = 2.2MHz, V_{BIAS} connected to GND, L = 0.56µH (DCR = 3mΩ)



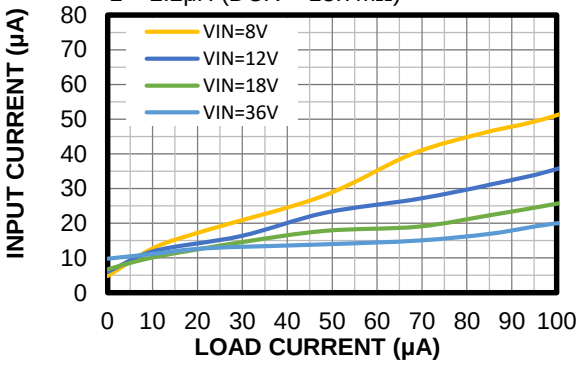
Input Current vs. Load Current for the MPQ4372-x3xx

AAM mode, V_{OUT} = 3.3V, f_{SW} = 2.2MHz, V_{BIAS} connected to 5V power, L = 0.56µH (DCR = 3mΩ)



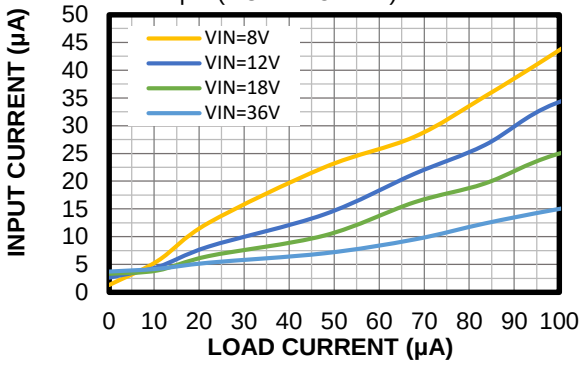
Input Current vs. Load Current for the MPQ4372-x3xx

AAM mode, V_{OUT} = 3.3V, f_{SW} = 410kHz, V_{BIAS} connected to GND, L = 2.2µH (DCR = 13.7mΩ)



Inutu Current vs. Load Current for the MPQ4372-x3xx

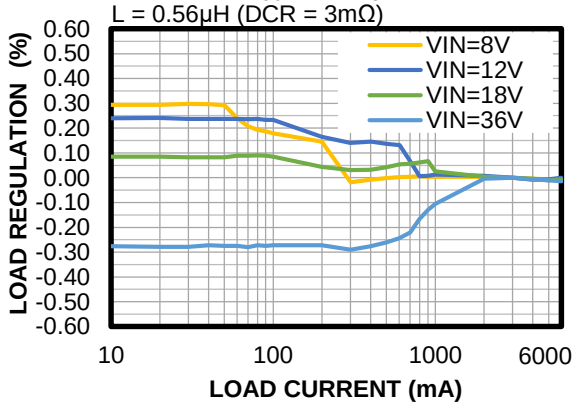
AAM mode, V_{OUT} = 3.3V, f_{SW} = 410kHz, V_{BIAS} connected to 5V power, L = 2.2µH (DCR = 13.7mΩ)



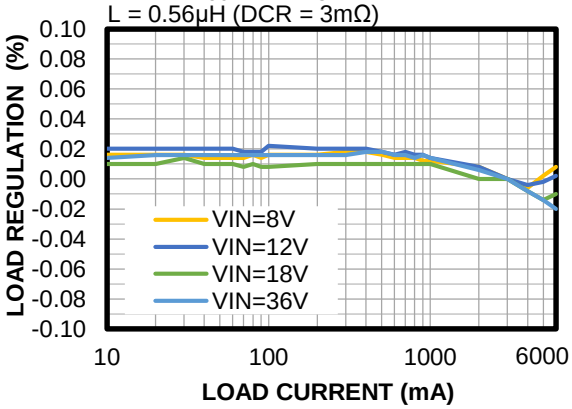
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 0.56µH (DCR = 3mΩ), T_A = 25°C, unless otherwise noted.

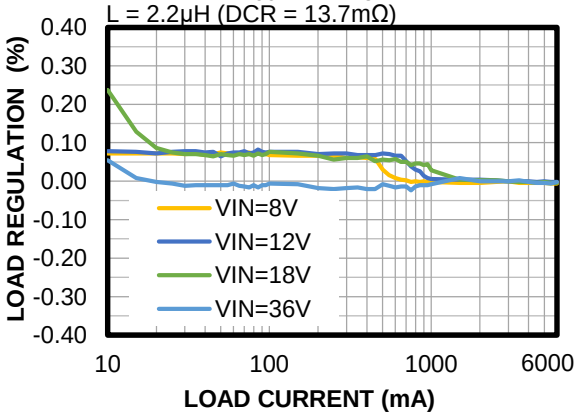
Load Regulation for the MPQ4372-6000
AAM mode, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 0.56µH (DCR = 3mΩ)



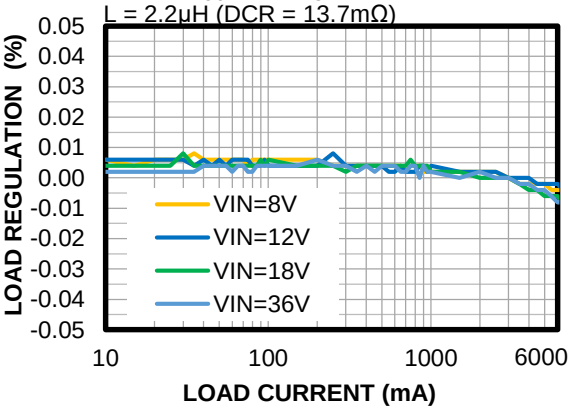
Load Regulation for the MPQ4372-6000
FCCM, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 0.56µH (DCR = 3mΩ)



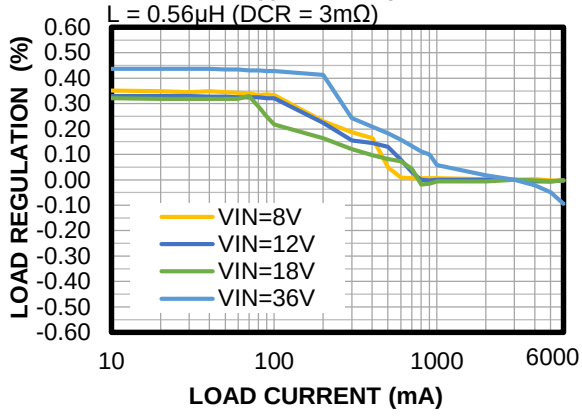
Load Regulation for the MPQ4372-6000
AAM mode, V_{OUT} = 5V, f_{SW} = 410kHz, L = 2.2µH (DCR = 13.7mΩ)



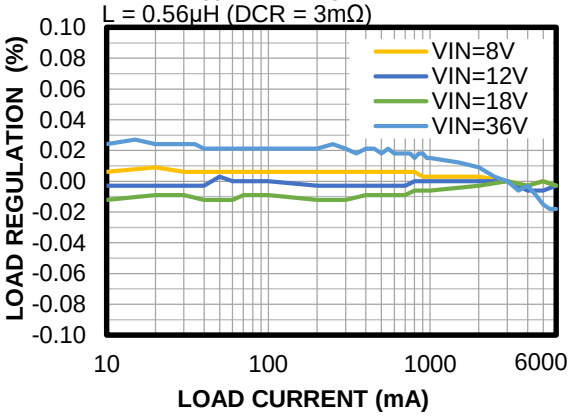
Load Regulation for the MPQ4372-6000
FCCM, V_{OUT} = 5V, f_{SW} = 410kHz, L = 2.2µH (DCR = 13.7mΩ)



Load Regulation for the MPQ4372-6000
AAM mode, V_{OUT} = 3.3V, f_{SW} = 2.2MHz, L = 0.56µH (DCR = 3mΩ)



Load Regulation for the MPQ4372-6000
FCCM, V_{OUT} = 3.3V, f_{SW} = 2.2MHz, L = 0.56µH (DCR = 3mΩ)

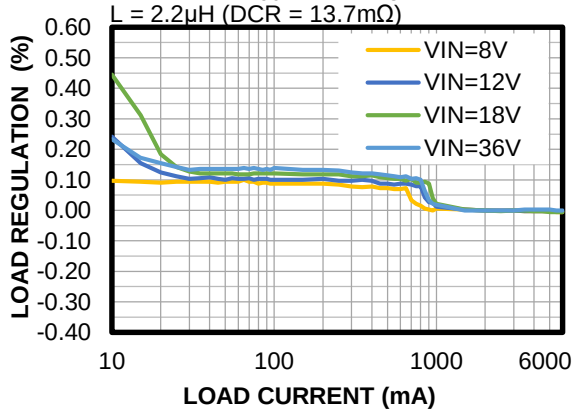


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 0.56µH (DCR = 3mΩ), T_A = 25°C, unless otherwise noted.

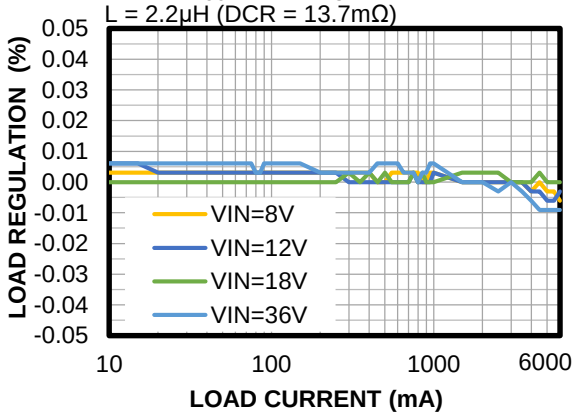
Load Regulation for the MPQ4372-6000

AAM mode, V_{OUT} = 3.3V, f_{SW} = 410kHz, L = 2.2µH (DCR = 13.7mΩ)



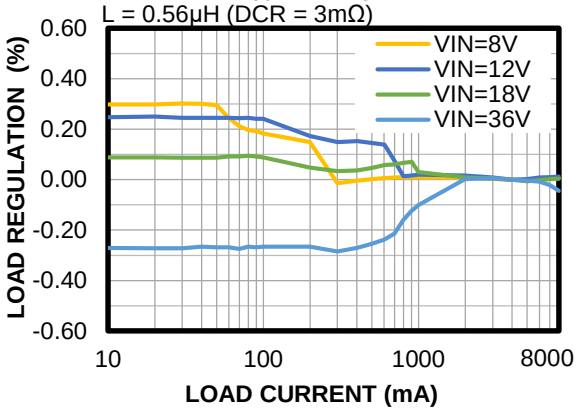
Load Regulation for the MPQ4372-6000

FCCM, V_{OUT} = 3.3V, f_{SW} = 410kHz, L = 2.2µH (DCR = 13.7mΩ)



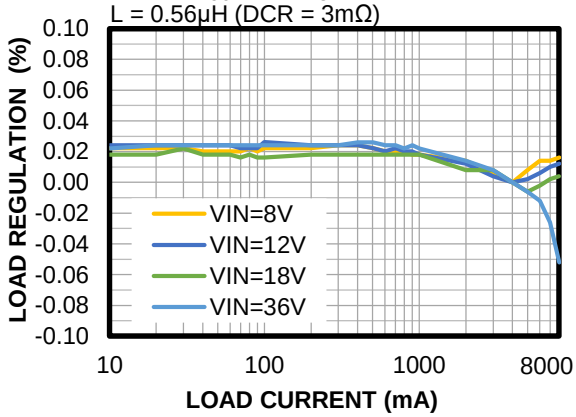
Load Regulation for the MPQ4372-8000

AAM mode, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 0.56µH (DCR = 3mΩ)



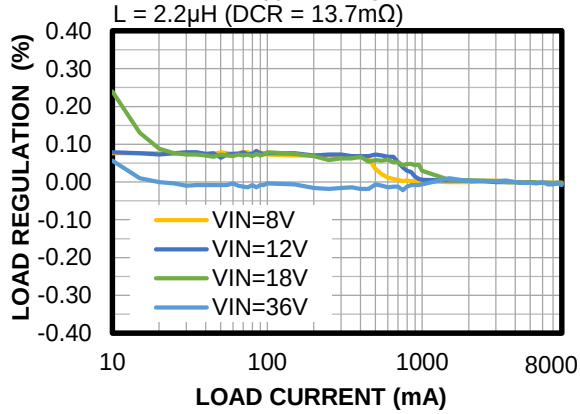
Load Regulation for the MPQ4372-8000

FCCM, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 0.56µH (DCR = 3mΩ)



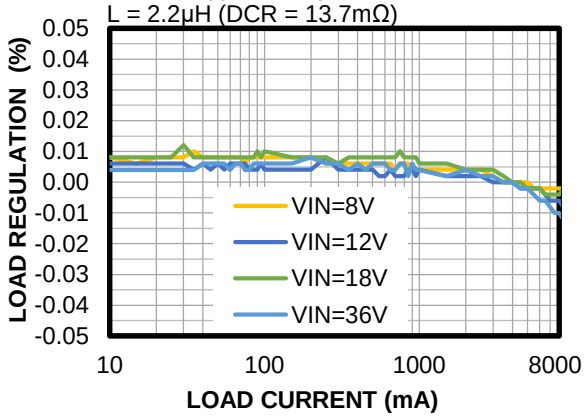
Load Regulation for the MPQ4372-8000

AAM mode, V_{OUT} = 5V, f_{SW} = 410kHz, L = 2.2µH (DCR = 13.7mΩ)



Load Regulation for the MPQ4372-8000

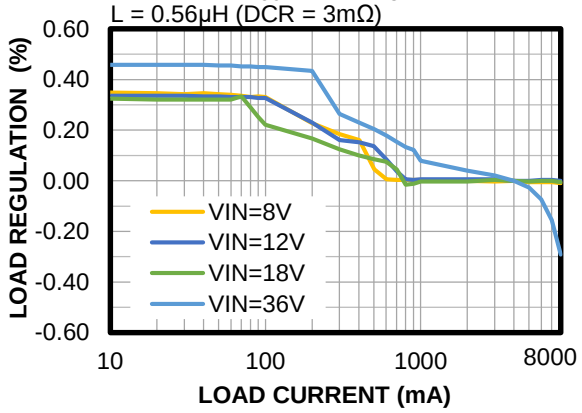
FCCM, V_{OUT} = 5V, f_{SW} = 410kHz, L = 2.2µH (DCR = 13.7mΩ)



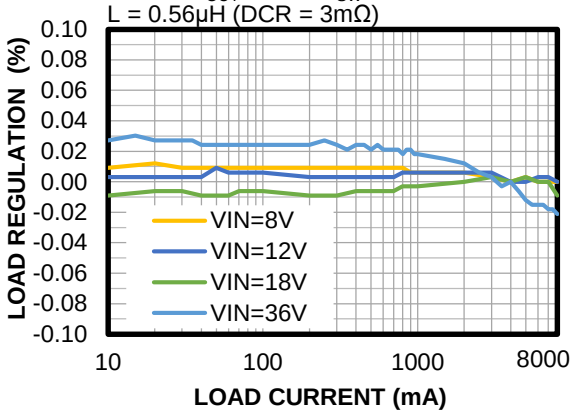
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 0.56µH (DCR = 3mΩ), T_A = 25°C, unless otherwise noted.

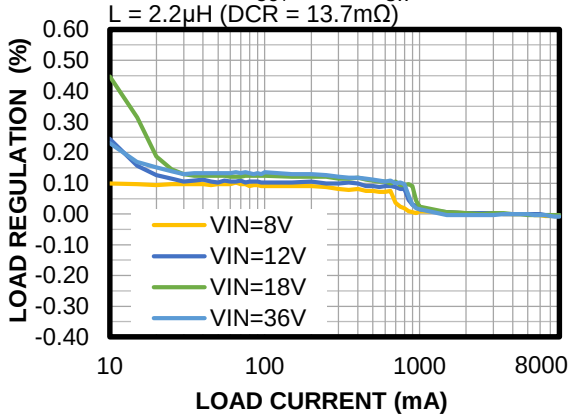
Load Regulation for the MPQ4372-8000
AAM mode, V_{OUT} = 3.3V, f_{SW} = 2.2MHz, L = 0.56µH (DCR = 3mΩ)



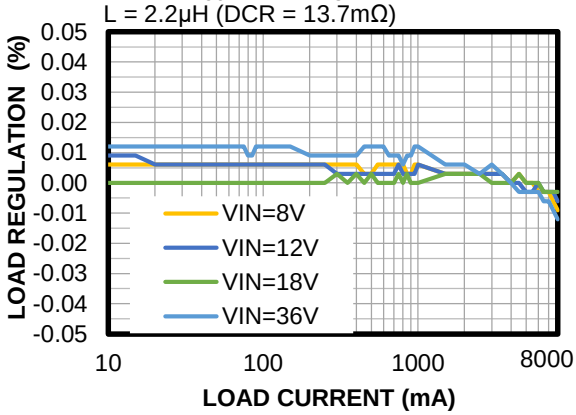
Load Regulation for the MPQ4372-8000
FCCM, V_{OUT} = 3.3V, f_{SW} = 2.2MHz, L = 0.56µH (DCR = 3mΩ)



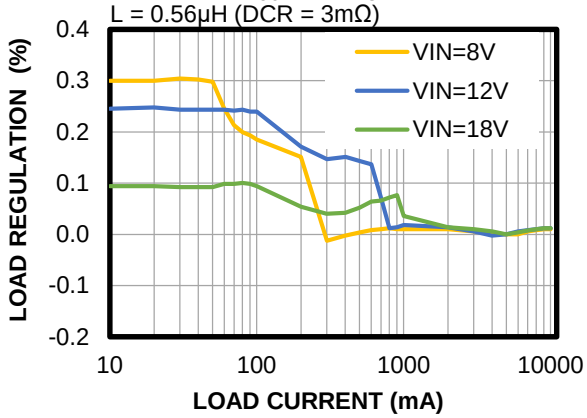
Load Regulation for the MPQ4372-8000
AAM mode, V_{OUT} = 3.3V, f_{SW} = 410kHz, L = 2.2µH (DCR = 13.7mΩ)



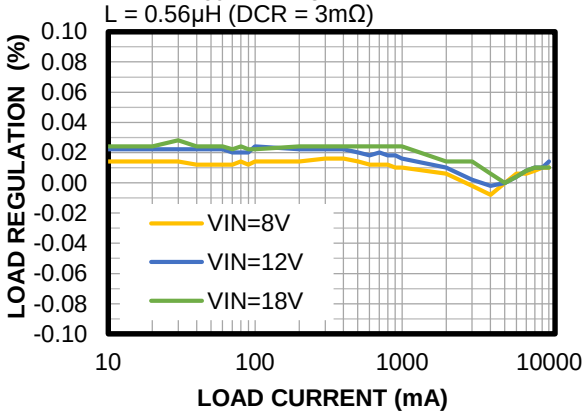
Load Regulation for the MPQ4372-8000
FCCM, V_{OUT} = 3.3V, f_{SW} = 410kHz, L = 2.2µH (DCR = 13.7mΩ)



Load Regulation for the MPQ4372-0000
AAM mode, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 0.56µH (DCR = 3mΩ)



Load Regulation for the MPQ4372-0000
FCCM, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 0.56µH (DCR = 3mΩ)

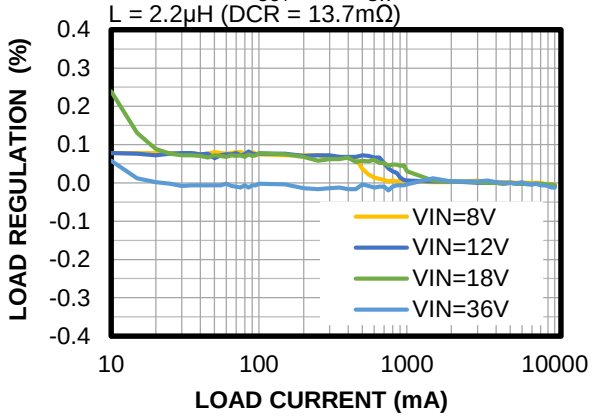


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 0.56µH (DCR = 3mΩ), T_A = 25°C, unless otherwise noted.

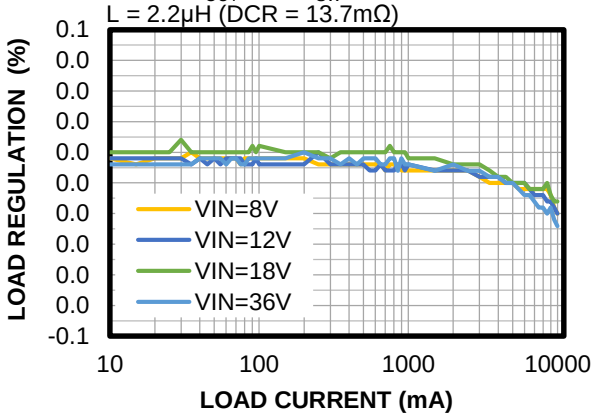
Load Regulation for the MPQ4372-0000

AAM mode, V_{OUT} = 5V, f_{SW} = 410kHz, L = 2.2µH (DCR = 13.7mΩ)



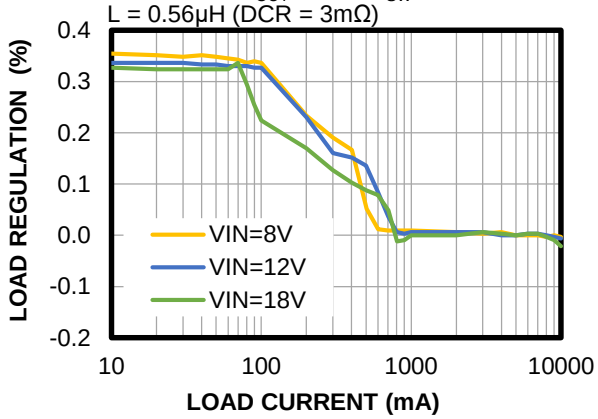
Load Regulation for the MPQ4372-0000

FCCM, V_{OUT} = 5V, f_{SW} = 410kHz, L = 2.2µH (DCR = 13.7mΩ)



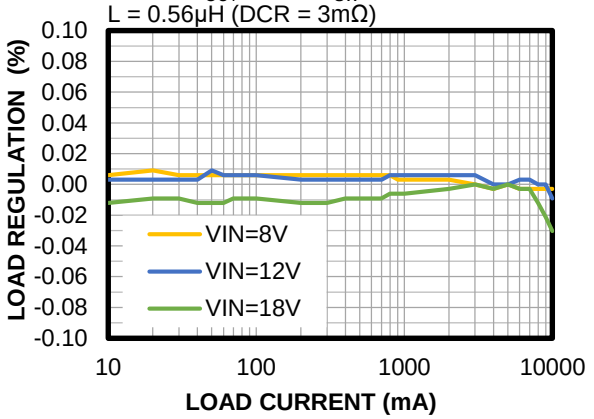
Load Regulation for the MPQ4372-0000

AAM mode, V_{OUT} = 3.3V, f_{SW} = 2.2MHz, L = 0.56µH (DCR = 3mΩ)



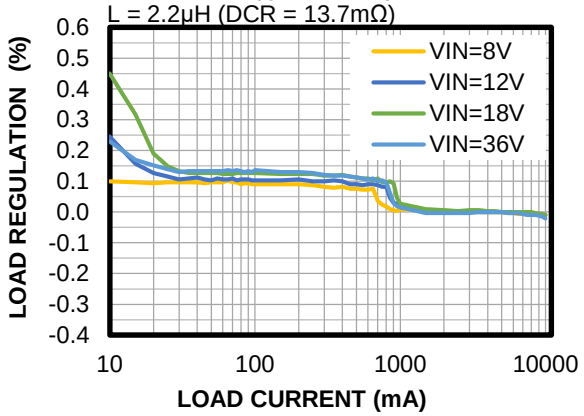
Load Regulation for the MPQ4372-0000

FCCM, V_{OUT} = 3.3V, f_{SW} = 2.2MHz, L = 0.56µH (DCR = 3mΩ)



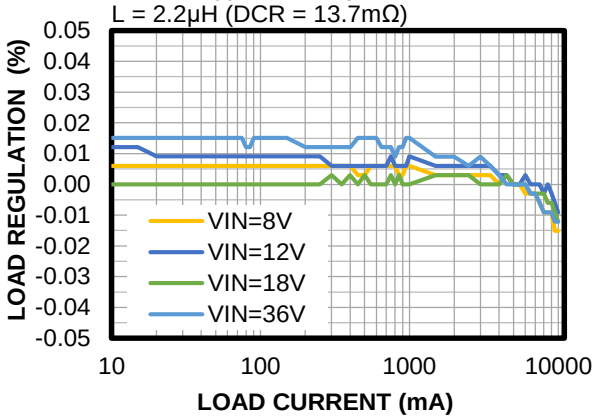
Load Regulation for the MPQ4372-0000

AAM mode, V_{OUT} = 3.3V, f_{SW} = 410kHz, L = 2.2µH (DCR = 13.7mΩ)



Load Regulation for the MPQ4372-0000

FCCM, V_{OUT} = 3.3V, f_{SW} = 410kHz, L = 2.2µH (DCR = 13.7mΩ)

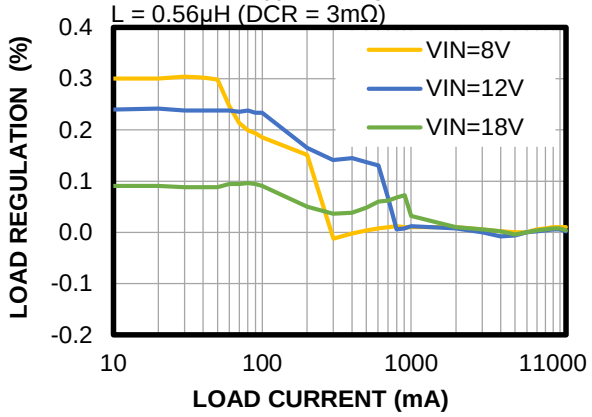


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 0.56µH (DCR = 3mΩ), T_A = 25°C, unless otherwise noted.

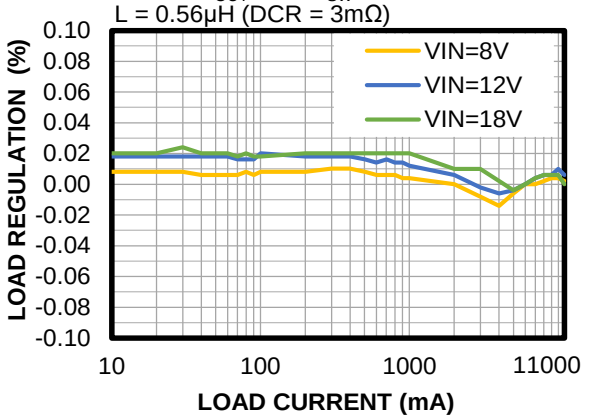
Load Regulation for the MPQ4372-1000

AAM mode, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 0.56µH (DCR = 3mΩ)



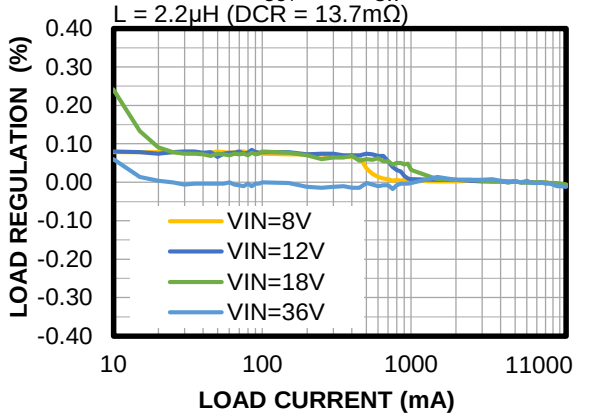
Load Regulation for the MPQ4372-1000

FCCM, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 0.56µH (DCR = 3mΩ)



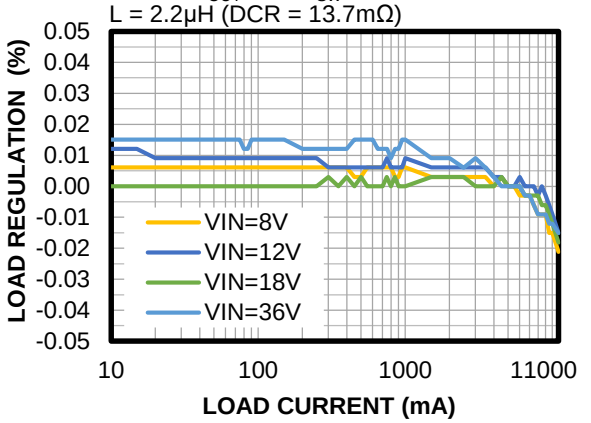
Load Regulation for the MPQ4372-1000

AAM mode, V_{OUT} = 5V, f_{SW} = 410kHz, L = 2.2µH (DCR = 13.7mΩ)



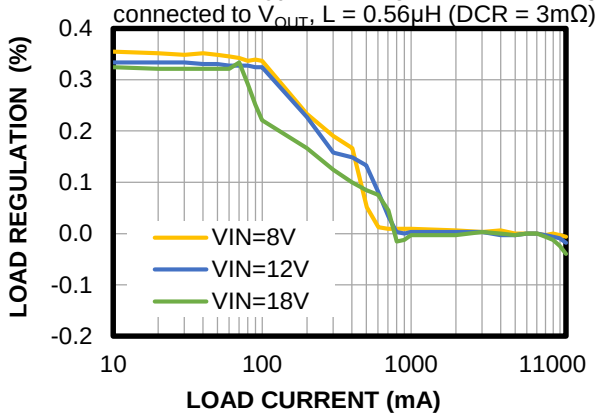
Load Regulation for the MPQ4372-1000

FCCM, V_{OUT} = 5V, f_{SW} = 410kHz, L = 2.2µH (DCR = 13.7mΩ)



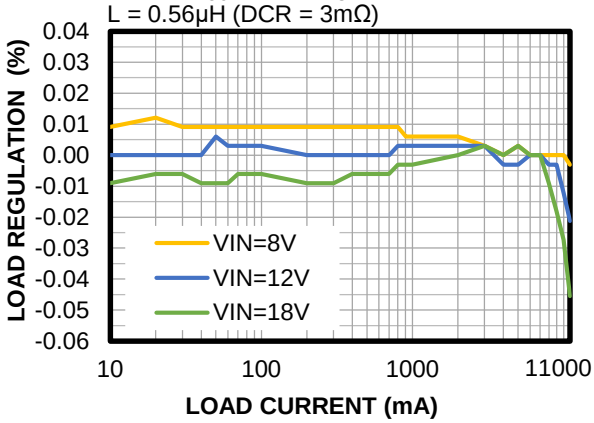
Load Regulation for the MPQ4372-1000

AAM mode, V_{OUT} = 3.3V, f_{SW} = 2.2MHz, V_{BIAS} connected to V_{OUT}, L = 0.56µH (DCR = 3mΩ)



Load Regulation for the MPQ4372-1000

FCCM, V_{OUT} = 3.3V, f_{SW} = 2.2MHz, L = 0.56µH (DCR = 3mΩ)

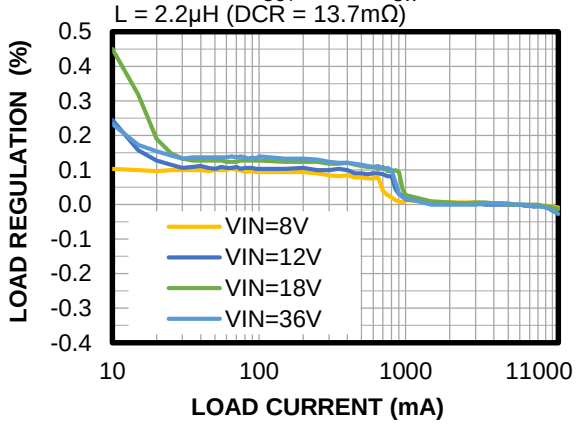


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 0.56µH (DCR = 3mΩ), T_A = 25°C, unless otherwise noted.

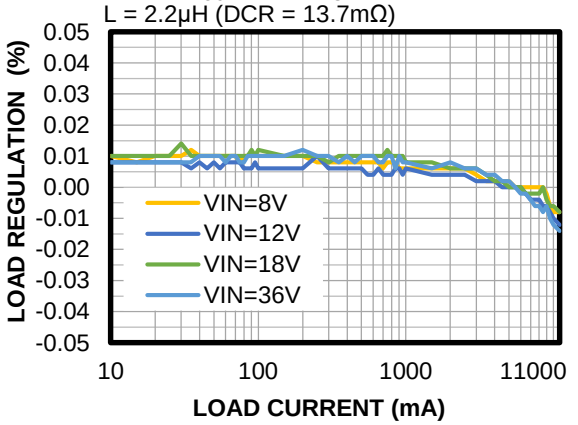
Load Regulation for the MPQ4372-1000

AAM mode, V_{OUT} = 3.3V, f_{SW} = 410kHz, L = 2.2µH (DCR = 13.7mΩ)



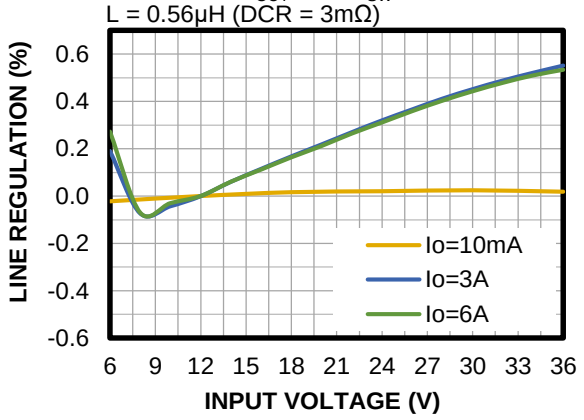
Load Regulation for the MPQ4372-1000

FCCM, V_{OUT} = 3.3V, f_{SW} = 410kHz, L = 2.2µH (DCR = 13.7mΩ)



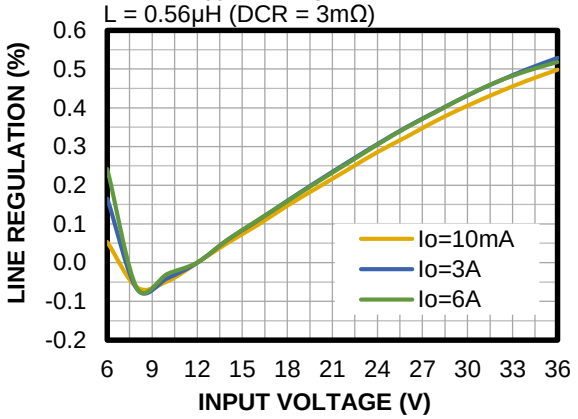
Line Regulation for the MPQ4372-6000

AAM mode, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 0.56µH (DCR = 3mΩ)



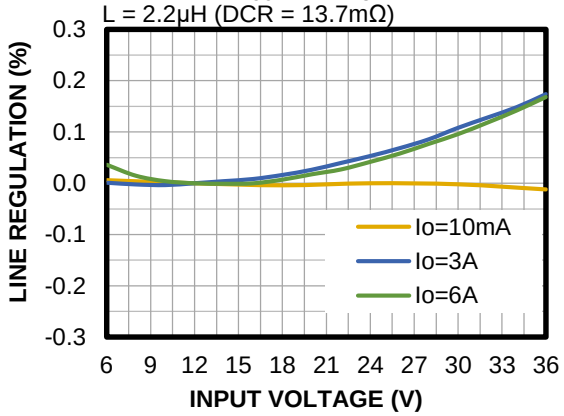
Line Regulation for the MPQ4372-6000

FCCM, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 0.56µH (DCR = 3mΩ)



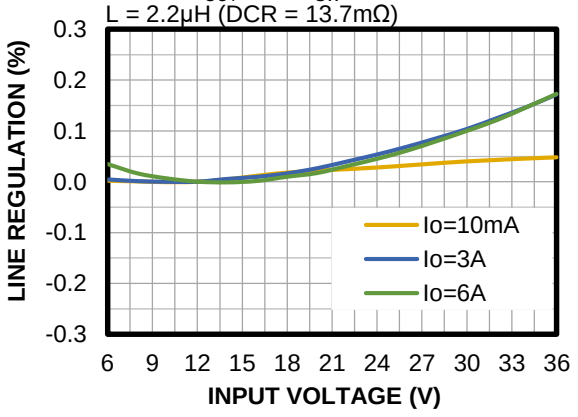
Line Regulation for the MPQ4372-6000

AAM mode, V_{OUT} = 5V, f_{SW} = 410kHz, L = 2.2µH (DCR = 13.7mΩ)



Line Regulation for the MPQ4372-6000

FCCM, V_{OUT} = 5V, f_{SW} = 410kHz, L = 2.2µH (DCR = 13.7mΩ)

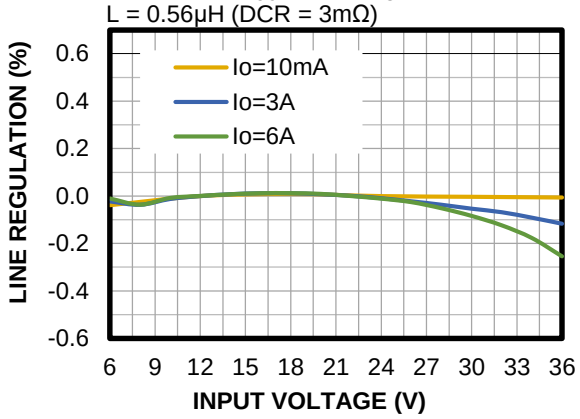


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 0.56µH (DCR = 3mΩ), T_A = 25°C, unless otherwise noted.

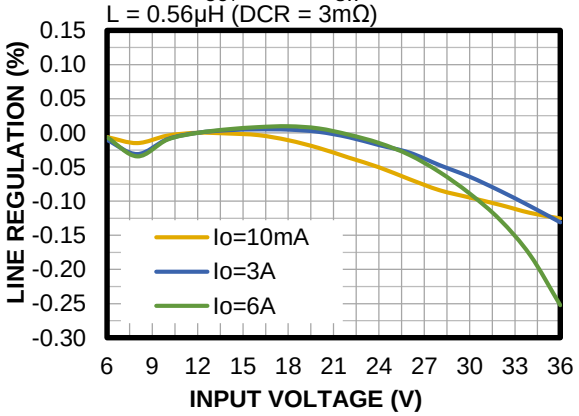
Line Regulation for the MPQ4372-6000

AAM mode, V_{OUT} = 3.3V, f_{SW} = 2.2MHz, L = 0.56µH (DCR = 3mΩ)



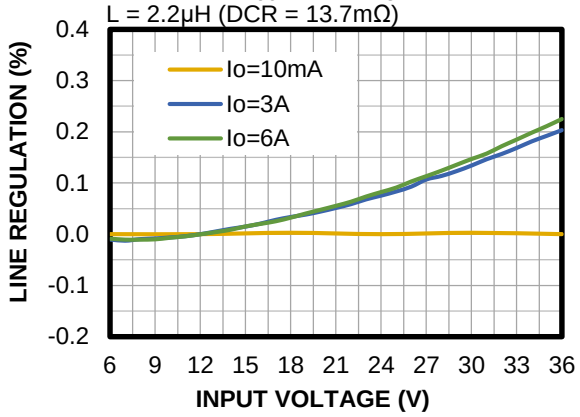
Line Regulation for the MPQ4372-6000

FCCM, V_{OUT} = 3.3V, f_{SW} = 2.2MHz, L = 0.56µH (DCR = 3mΩ)



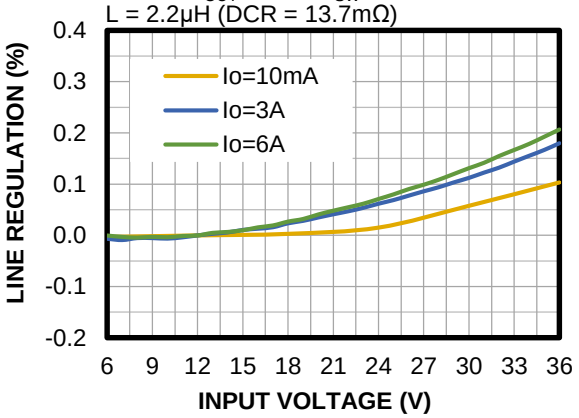
Line Regulation for the MPQ4372-6000

AAM mode, V_{OUT} = 3.3V, f_{SW} = 410kHz, L = 2.2µH (DCR = 13.7mΩ)



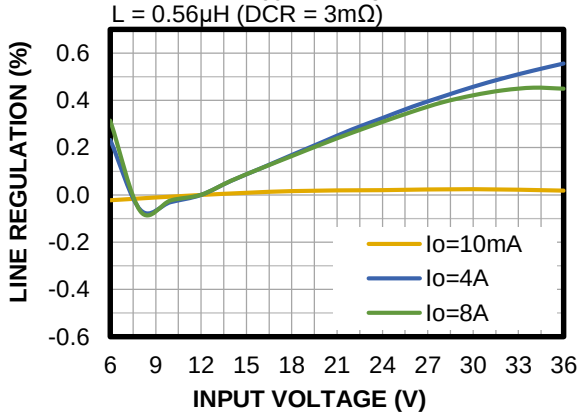
Line Regulation for the MPQ4372-6000

FCCM, V_{OUT} = 3.3V, f_{SW} = 410kHz, L = 2.2µH (DCR = 13.7mΩ)



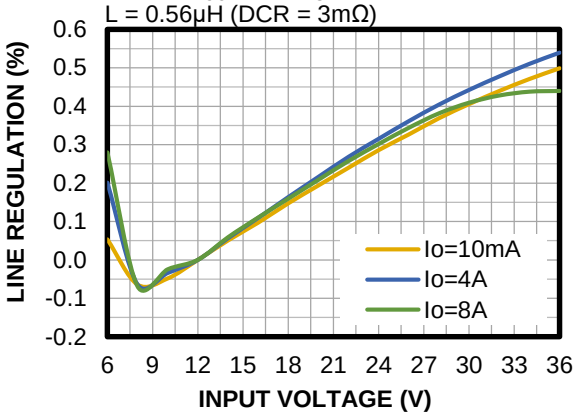
Line Regulation for the MPQ4372-8000

AAM mode, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 0.56µH (DCR = 3mΩ)



Line Regulation for the MPQ4372-8000

FCCM, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 0.56µH (DCR = 3mΩ)

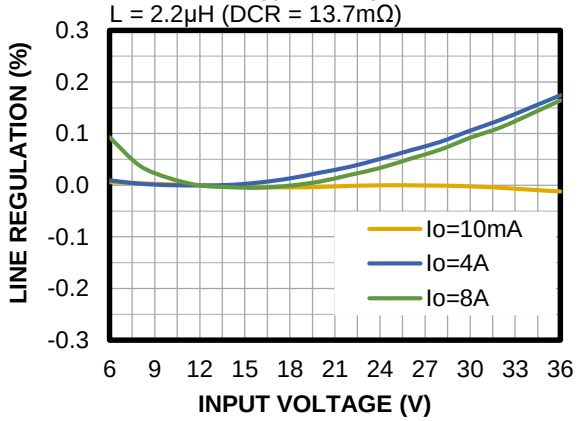


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 0.56µH (DCR = 3mΩ), T_A = 25°C, unless otherwise noted.

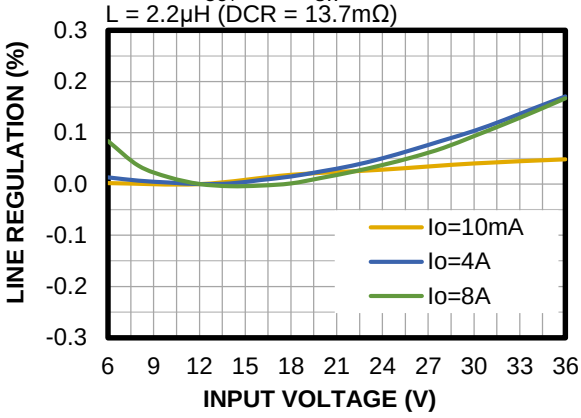
Line Regulation for the MPQ4372-8000

AAM mode, V_{OUT} = 5V, f_{SW} = 410kHz, L = 2.2µH (DCR = 13.7mΩ)



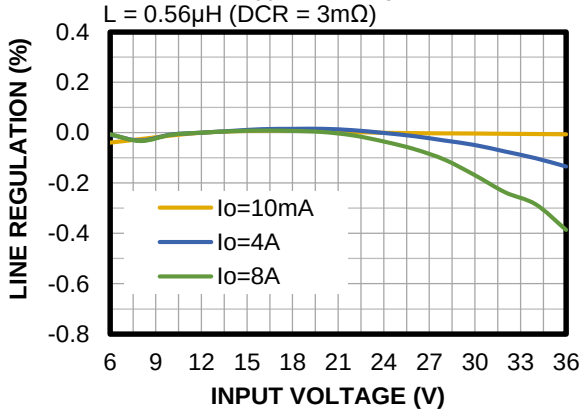
Line Regulation for the MPQ4372-8000

FCCM, V_{OUT} = 5V, f_{SW} = 410kHz, L = 2.2µH (DCR = 13.7mΩ)



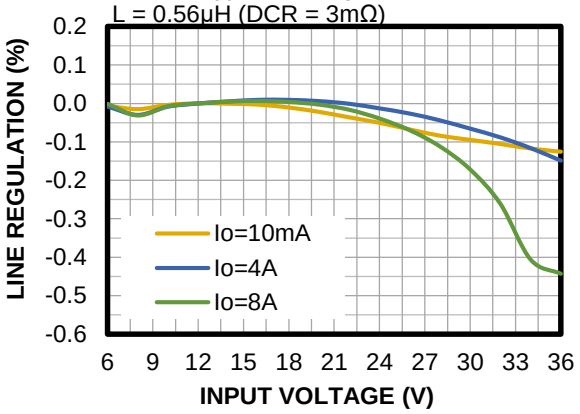
Line Regulation for the MPQ4372-8000

AAM mode, V_{OUT} = 3.3V, f_{SW} = 2.2MHz, L = 0.56µH (DCR = 3mΩ)



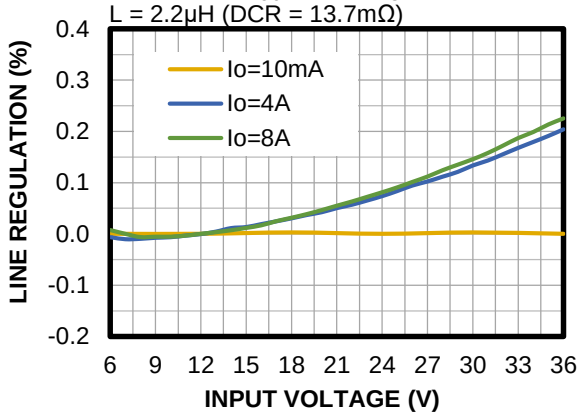
Line Regulation for the MPQ4372-8000

FCCM, V_{OUT} = 3.3V, f_{SW} = 2.2MHz, L = 0.56µH (DCR = 3mΩ)



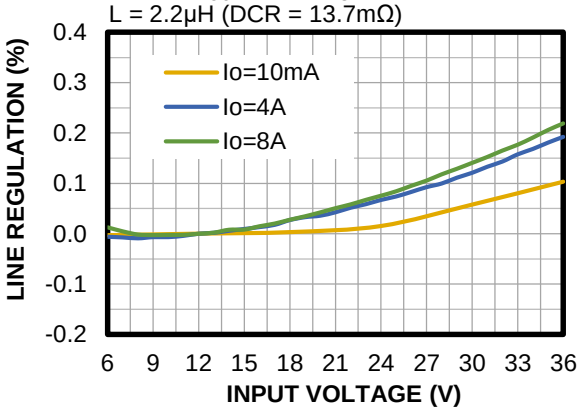
Line Regulation for the MPQ4372-8000

AAM mode, V_{OUT} = 3.3V, f_{SW} = 410kHz, L = 2.2µH (DCR = 13.7mΩ)



Line Regulation for the MPQ4372-8000

FCCM, V_{OUT} = 3.3V, f_{SW} = 410kHz, L = 2.2µH (DCR = 13.7mΩ)

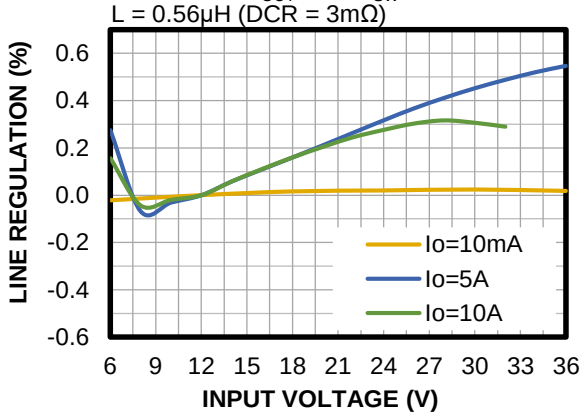


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 0.56µH (DCR = 3mΩ), T_A = 25°C, unless otherwise noted.

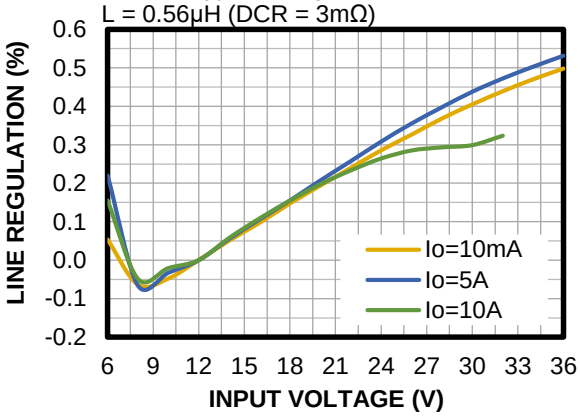
Line Regulation for the MPQ4372-0000

AAM mode, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 0.56µH (DCR = 3mΩ)



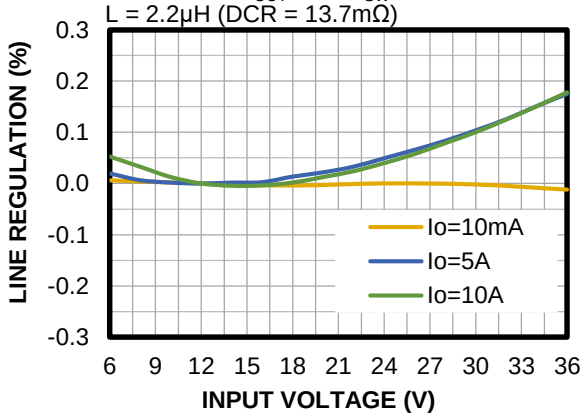
Line Regulation for the MPQ4372-0000

FCCM, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 0.56µH (DCR = 3mΩ)



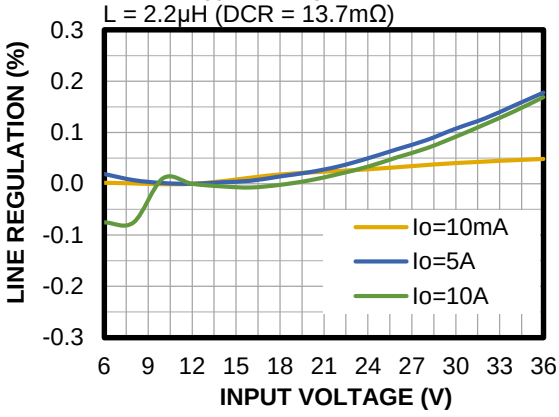
Line Regulation for the MPQ4372-0000

AAM mode, V_{OUT} = 5V, f_{SW} = 410kHz, L = 2.2µH (DCR = 13.7mΩ)



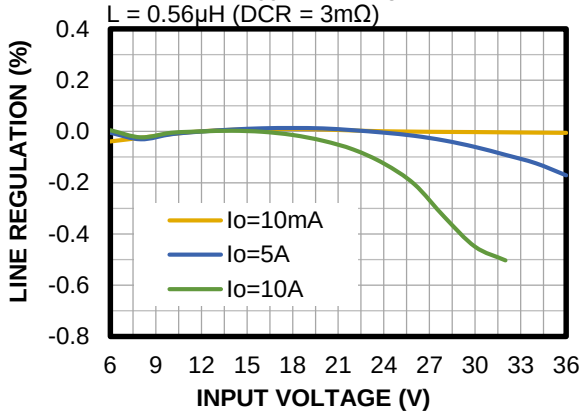
Line Regulation for the MPQ4372-0000

FCCM, V_{OUT} = 5V, f_{SW} = 410kHz, L = 2.2µH (DCR = 13.7mΩ)



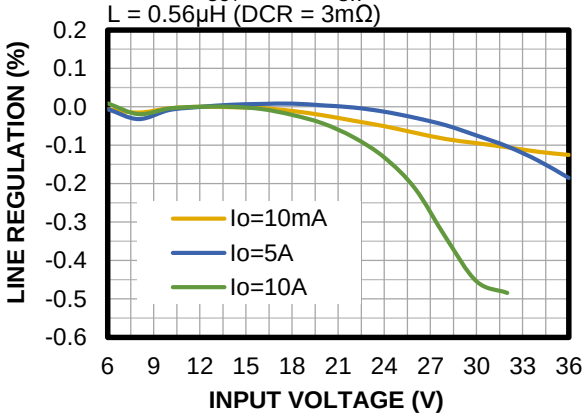
Line Regulation for the MPQ4372-0000

AAM mode, V_{OUT} = 3.3V, f_{SW} = 2.2MHz, L = 0.56µH (DCR = 3mΩ)



Line Regulation for the MPQ4372-0000

FCCM, V_{OUT} = 3.3V, f_{SW} = 2.2MHz, L = 0.56µH (DCR = 3mΩ)

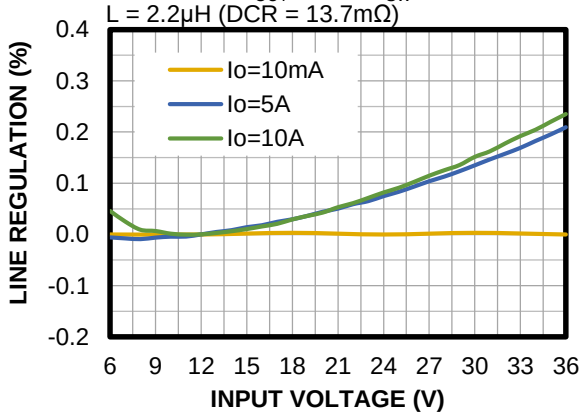


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 0.56µH (DCR = 3mΩ), T_A = 25°C, unless otherwise noted.

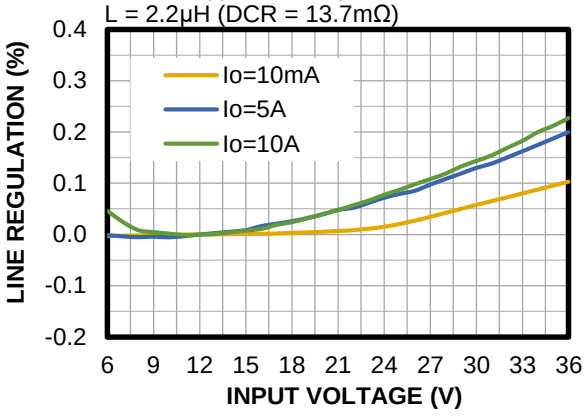
Line Regulation for the MPQ4372-0000

AAM mode, V_{OUT} = 3.3V, f_{SW} = 410kHz, L = 2.2µH (DCR = 13.7mΩ)



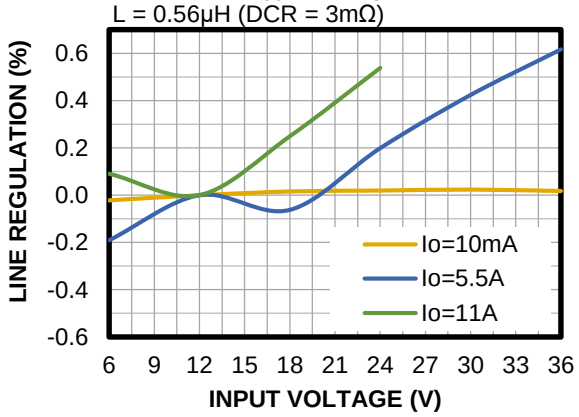
Line Regulation for the MPQ4372-0000

FCCM, V_{OUT} = 3.3V, f_{SW} = 410kHz, L = 2.2µH (DCR = 13.7mΩ)



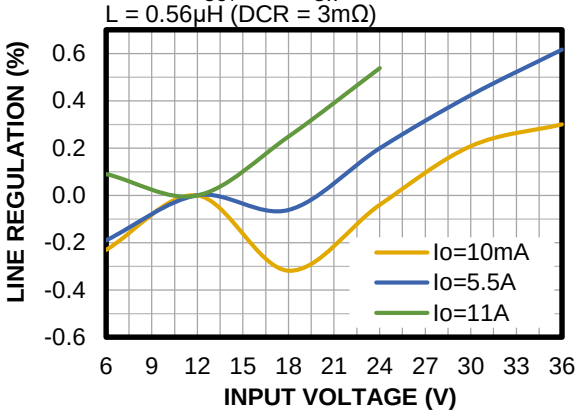
Line Regulation for the MPQ4372-1000

AAM mode, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 0.56µH (DCR = 3mΩ)



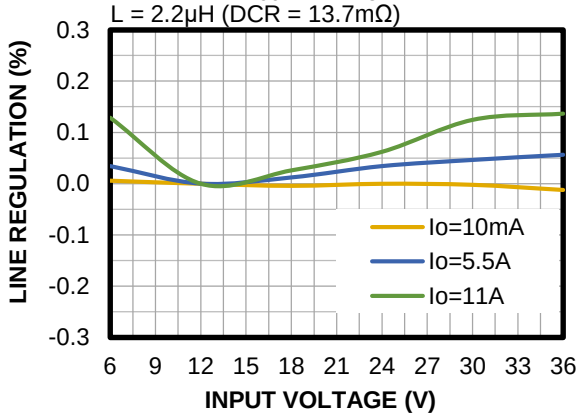
Line Regulation for the MPQ4372-1000

FCCM, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 0.56µH (DCR = 3mΩ)



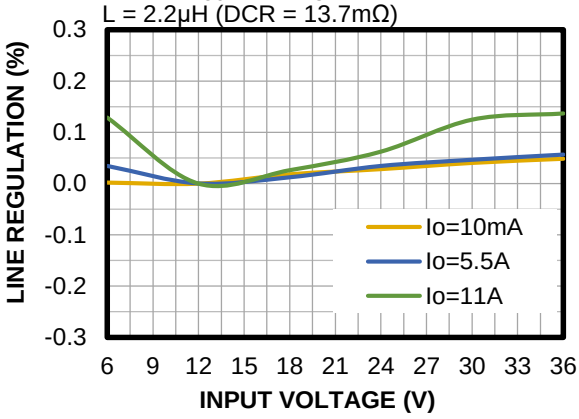
Line Regulation for the MPQ4372-1000

AAM mode, V_{OUT} = 5V, f_{SW} = 410kHz, L = 2.2µH (DCR = 13.7mΩ)



Line Regulation for the MPQ4372-1000

FCCM, V_{OUT} = 5V, f_{SW} = 410kHz, L = 2.2µH (DCR = 13.7mΩ)

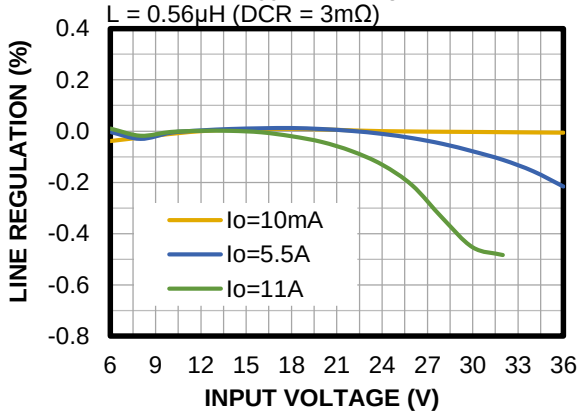


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 0.56µH (DCR = 3mΩ), T_A = 25°C, unless otherwise noted.

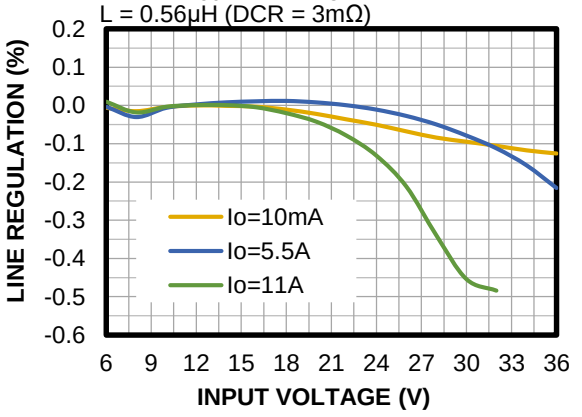
Line Regulation for the MPQ4372-1000

AAM mode, V_{OUT} = 3.3V, f_{SW} = 2.2MHz, L = 0.56µH (DCR = 3mΩ)



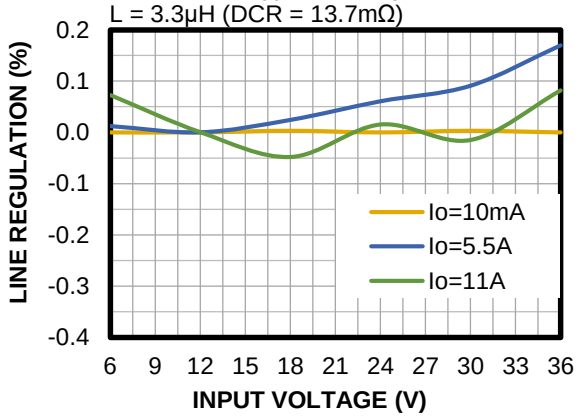
Line Regulation for the MPQ4372-1000

FCCM, V_{OUT} = 3.3V, f_{SW} = 2.2MHz, L = 0.56µH (DCR = 3mΩ)



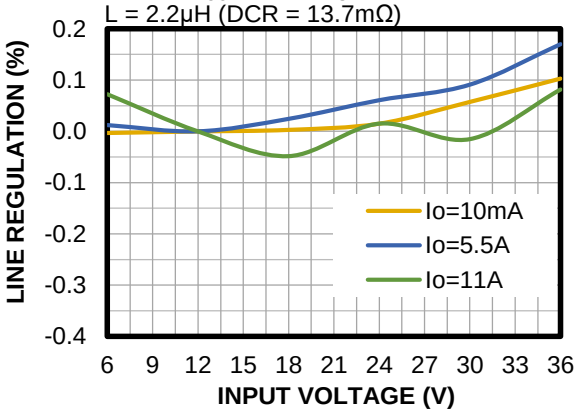
Line Regulation for the MPQ4372-1000

AAM mode, V_{OUT} = 3.3V, f_{SW} = 410kHz, L = 3.3µH (DCR = 13.7mΩ)



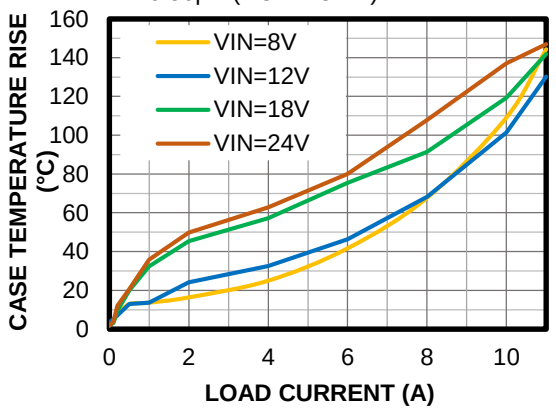
Line Regulation for the MPQ4372-1000

FCCM, V_{OUT} = 3.3V, f_{SW} = 410kHz, L = 2.2µH (DCR = 13.7mΩ)



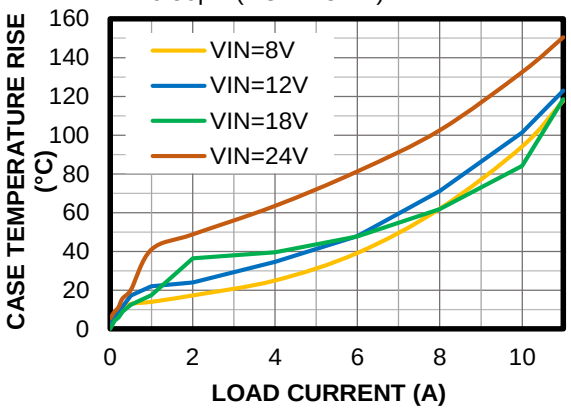
Case Temperature Rise

AAM mode, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 0.56µH (DCR = 3mΩ)



Case Temperature Rise

AAM mode, V_{OUT} = 3.3V, f_{SW} = 2.2MHz, L = 0.56µH (DCR = 3mΩ)

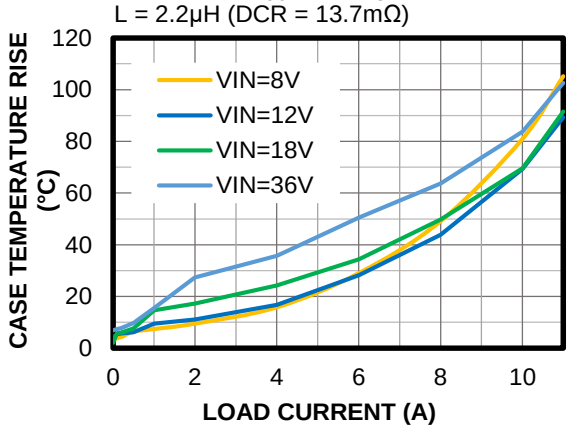


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 0.56µH (DCR = 3mΩ), T_A = 25°C, unless otherwise noted.

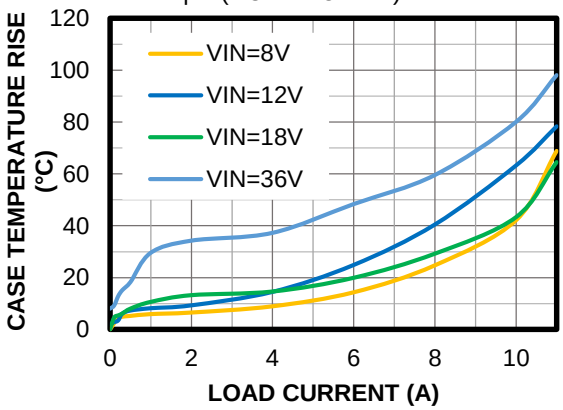
Case Temperature Rise

AAM mode, V_{OUT} = 5V, f_{SW} = 410kHz, L = 2.2µH (DCR = 13.7mΩ)



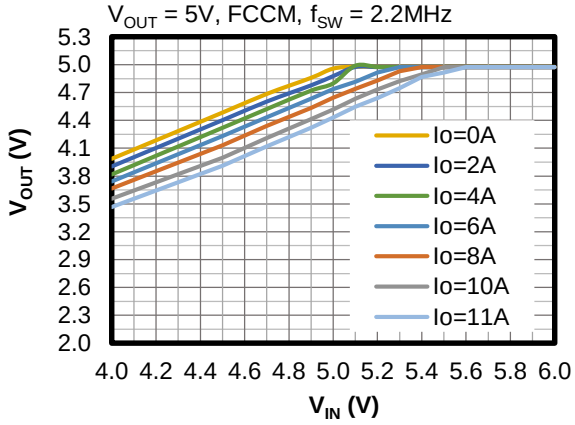
Case Temperature Rise

AAM mode, V_{OUT} = 3.3V, f_{SW} = 410kHz, L = 2.2µH (DCR = 13.7mΩ)



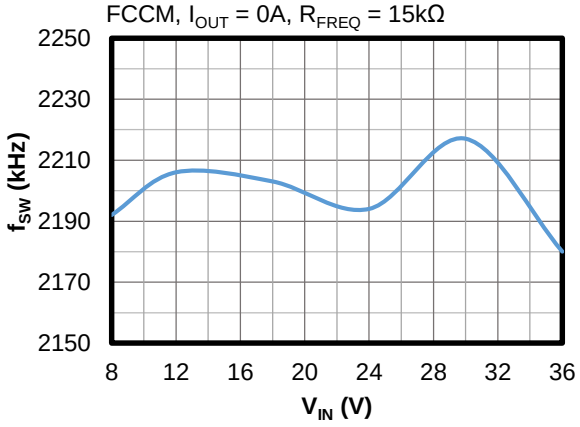
Low-Dropout Mode

V_{OUT} = 5V, FCCM, f_{SW} = 2.2MHz



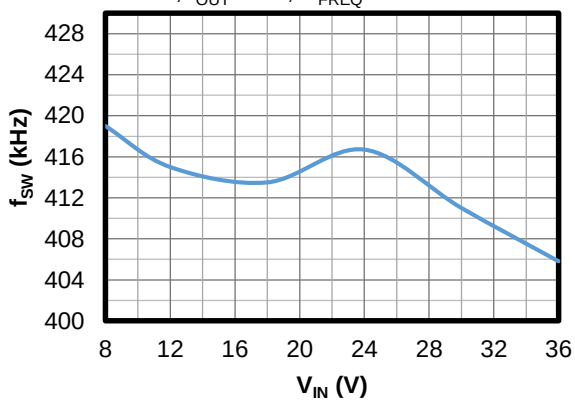
Switching Frequency vs. Input Voltage

FCCM, I_{OUT} = 0A, R_{FREQ} = 15kΩ



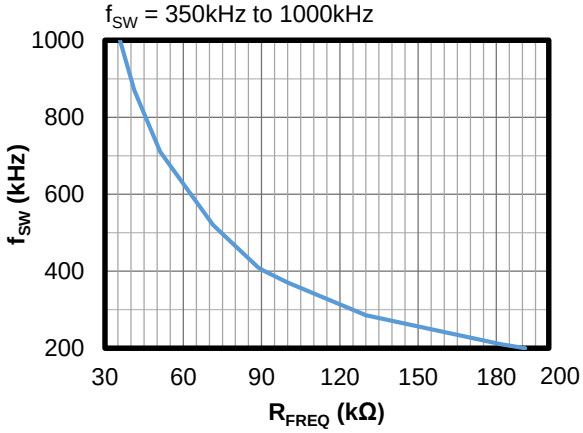
Switching Frequency vs. Input Voltage

FCCM, I_{OUT} = 0A, R_{FREQ} = 88.6kΩ



Switching Frequency vs. Frequency Resistance

f_{SW} = 350kHz to 1000kHz

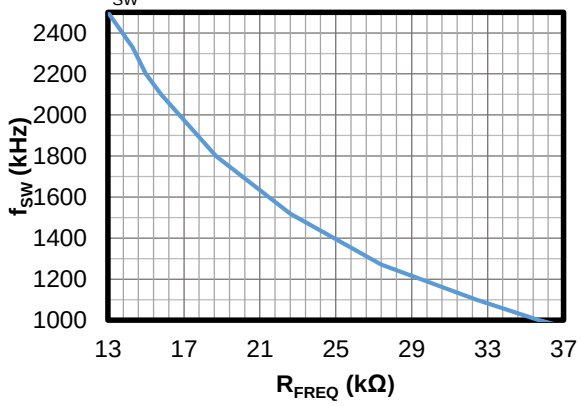


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 0.56µH (DCR = 3mΩ), T_A = 25°C, unless otherwise noted.

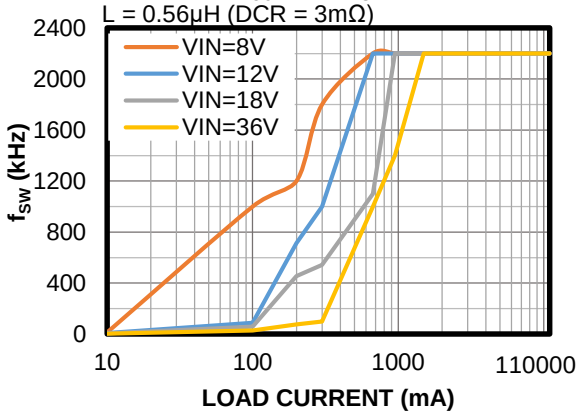
Switching Frequency vs. Frequency Resistance

f_{SW} = 1000kHz to 2500kHz



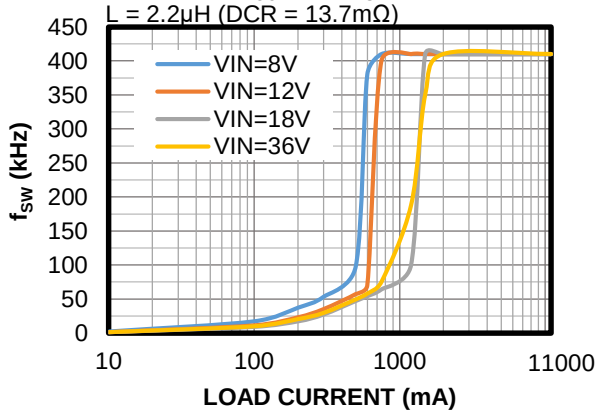
Switching Frequency vs. Load Current

AAM mode, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 0.56µH (DCR = 3mΩ)



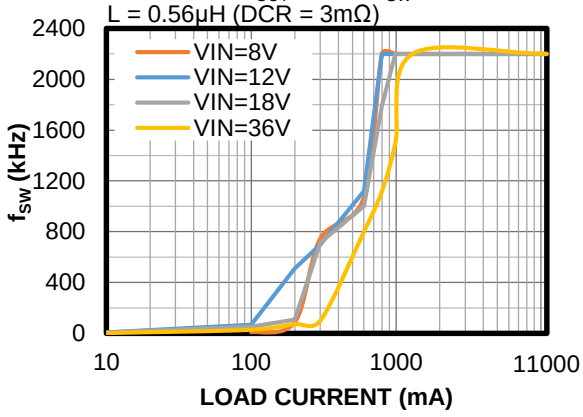
Switching Frequency vs. Load Current

AAM mode, V_{OUT} = 5V, f_{SW} = 410kHz, L = 2.2µH (DCR = 13.7mΩ)



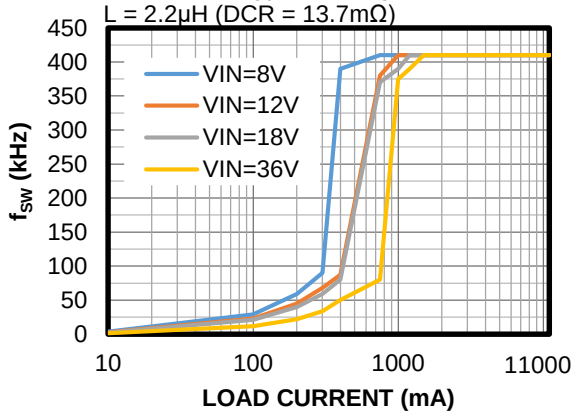
Switching Frequency vs. Load Current

AAM mode, V_{OUT} = 3.3V, f_{SW} = 2.2MHz, L = 0.56µH (DCR = 3mΩ)



Switching Frequency vs. Load Current

AAM mode, V_{OUT} = 3.3V, f_{SW} = 410kHz, L = 2.2µH (DCR = 13.7mΩ)

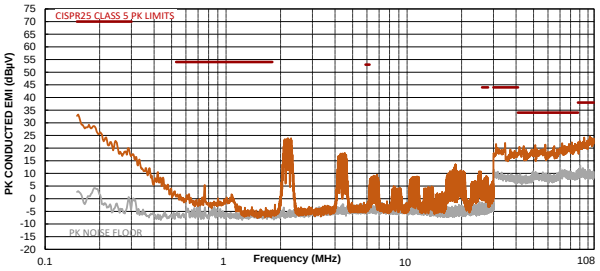


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, single-phase, I_{OUT} = 11A, L = 0.56µH (12), f_{SW} = 2.2MHz, AAM mode, T_A = 25°C, unless otherwise noted. (13)

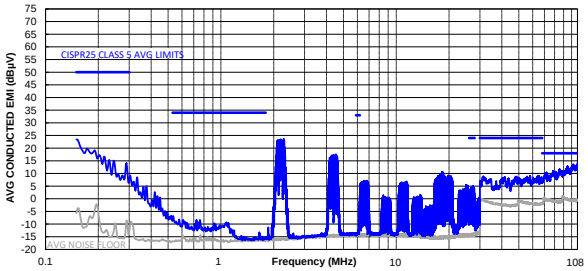
CISPR 25 Class 5 Peak Conducted Emissions

150kHz to 108MHz



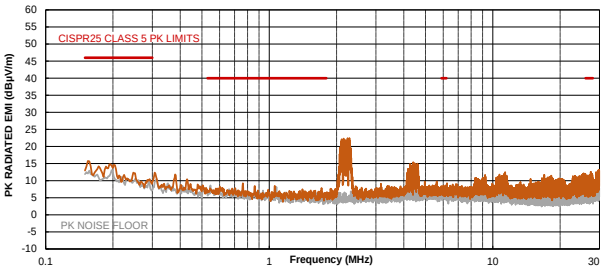
CISPR 25 Class 5 Average Conducted Emissions

150kHz to 108MHz



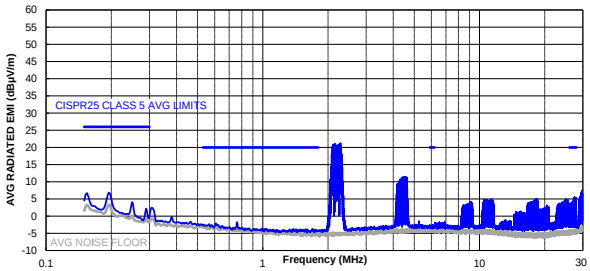
CISPR 25 Class 5 Peak Radiated Emissions

150kHz to 30MHz



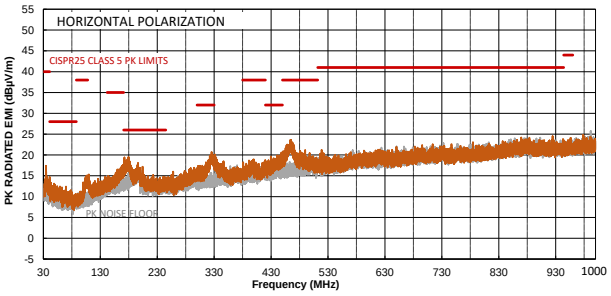
CISPR 25 Class 5 Average Radiated Emissions

150kHz to 30MHz



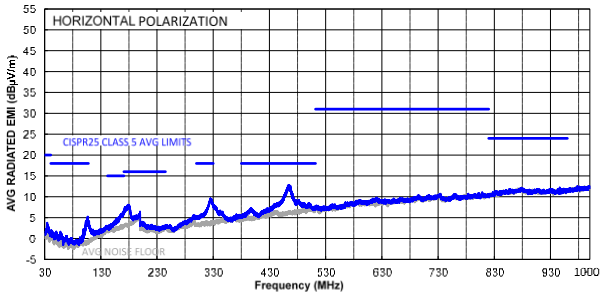
CISPR 25 Class 5 Peak Radiated Emissions

Horizontal, 30MHz to 1GHz



CISPR 25 Class 5 Average Radiated Emissions

Horizontal, 30MHz to 1GHz

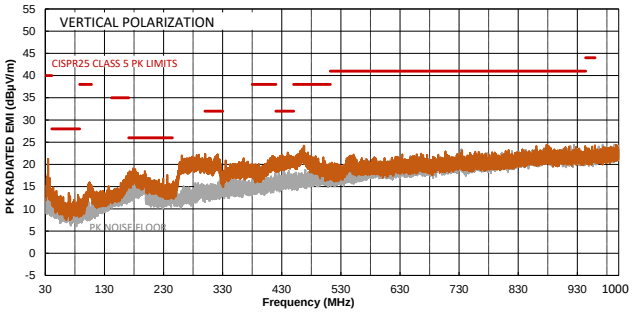


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, single-phase, I_{OUT} = 11A, L = 0.56µH (12), f_{SW} = 2.2MHz, AAM mode, T_A = 25°C, unless otherwise noted. (13)

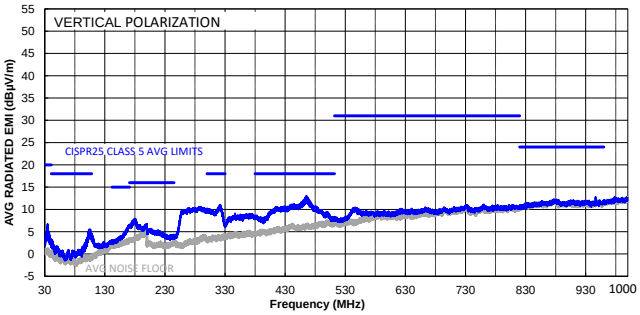
CISPR 25 Class 5 Peak Radiated Emissions

Vertical, 30MHz to 1GHz



CISPR 25 Class 5 Average Radiated Emissions

Vertical, 30MHz to 1GHz

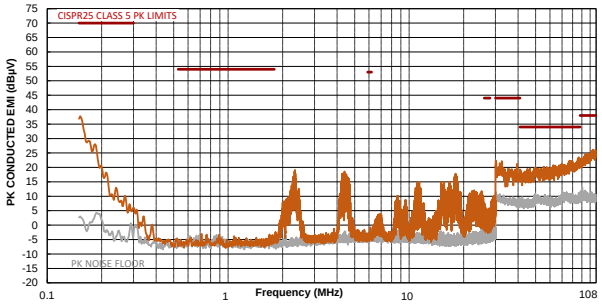


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, dual-phase, I_{OUT} = 22A, L = 0.56µH (12), f_{SW} = 2.2MHz, AAM mode, T_A = 25°C, unless otherwise noted. (14)

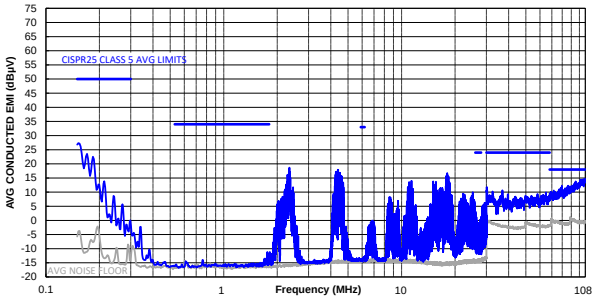
CISPR 25 Class 5 Peak Conducted Emissions

150kHz to 108MHz



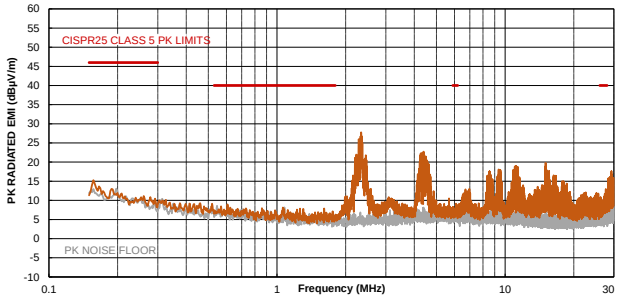
CISPR 25 Class 5 Average Conducted Emissions

150kHz to 108MHz



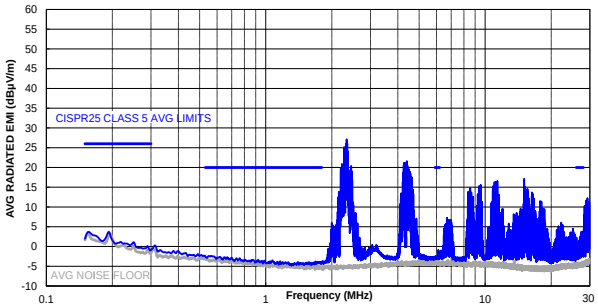
CISPR 25 Class 5 Peak Radiated Emissions

150kHz to 30MHz



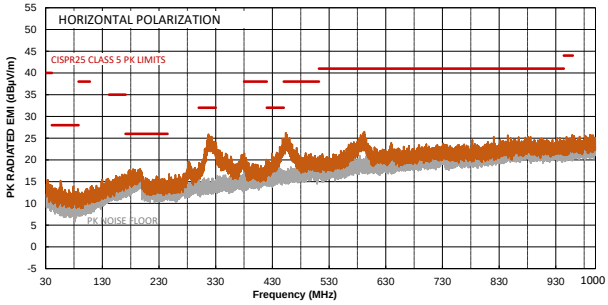
CISPR 25 Class 5 Average Radiated Emissions

150kHz to 30MHz



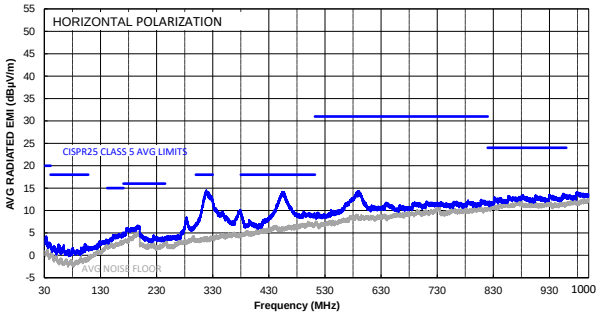
CISPR 25 Class 5 Peak Radiated Emissions

Horizontal, 30MHz to 1GHz



CISPR 25 Class 5 Average Radiated Emissions

Horizontal, 30MHz to 1GHz

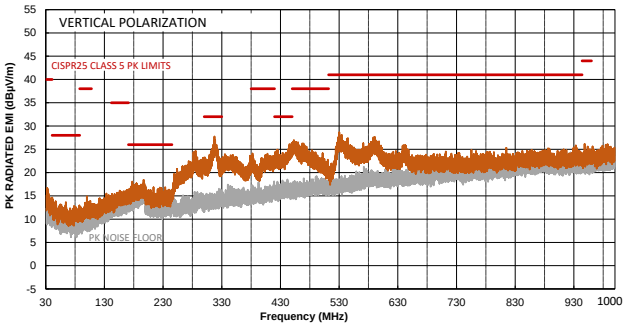


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, dual-phase, I_{OUT} = 22A, L = 0.56µH (12), f_{SW} = 2.2MHz, AAM mode, T_A = 25°C, unless otherwise noted. (14)

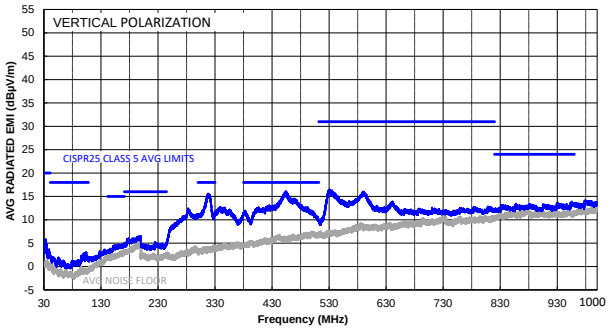
CISPR 25 Class 5 Peak Radiated Emissions

Vertical, 30MHz to 1GHz



CISPR 25 Class 5 Average Radiated Emissions

Vertical, 30MHz to 1GHz



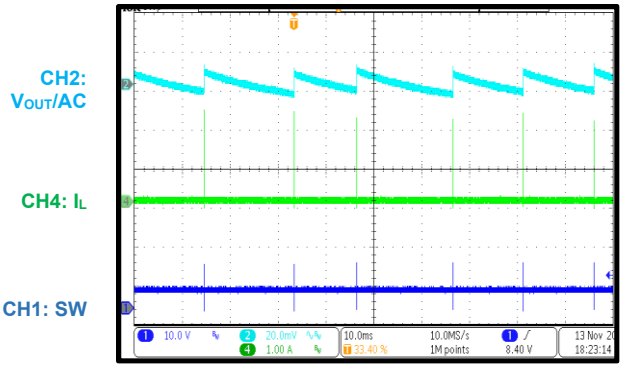
Notes:

12) Inductor part number: XEL6030-561MEB/C. DCR = 3mΩ.
13) The EMC test results are based on the application circuit with EMI filters (see Figure 18 on page 77).
14) The EMC test results are based on the application circuit with EMI filters (see Figure 22 on page 79).

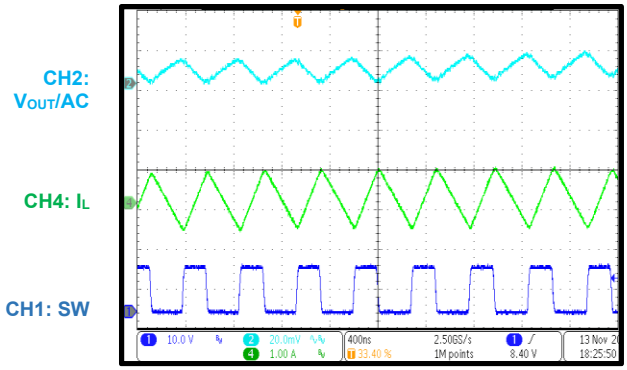
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, single-phase, L = 0.56µH, f_{SW} = 2.2MHz, AAM mode, T_A = 25°C, unless otherwise noted.

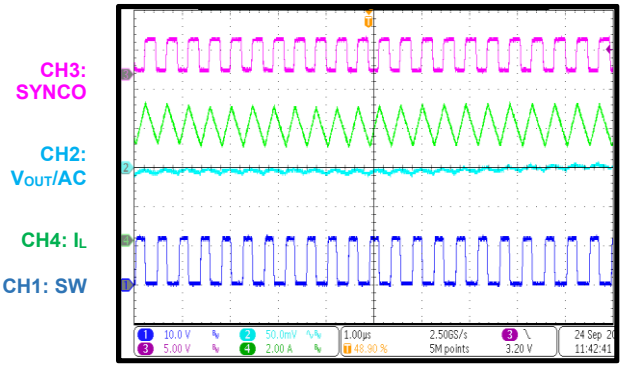
Steady State
I_{OUT} = 0A, AAM mode



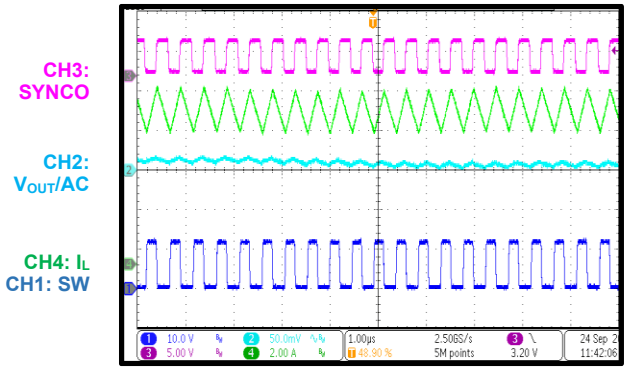
Steady State
I_{OUT} = 0A, FCCM



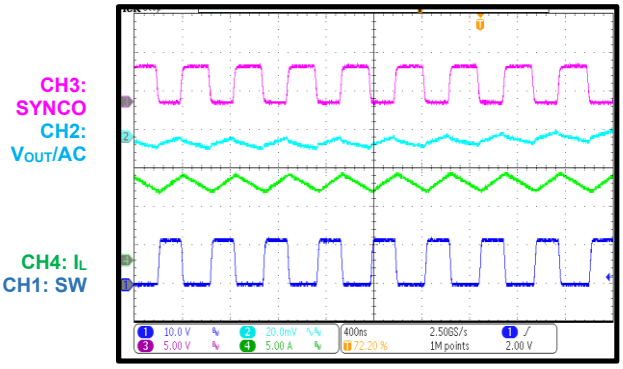
Steady State
I_{OUT} = 6A



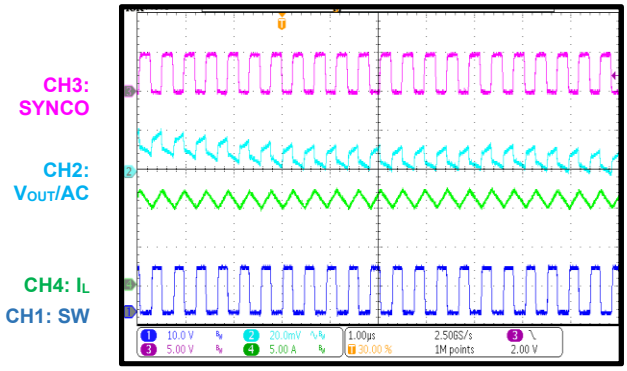
Steady State
I_{OUT} = 8A



Steady State
I_{OUT} = 10A



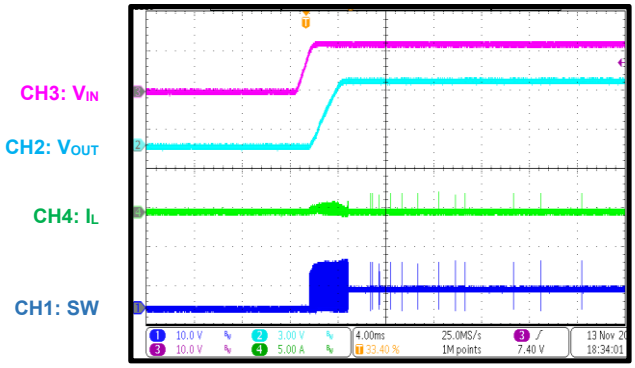
Steady State
I_{OUT} = 11A



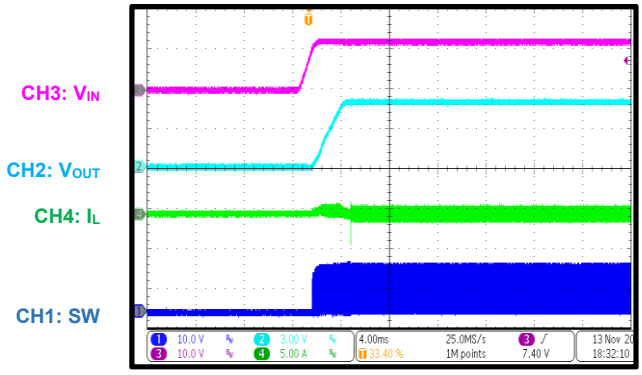
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, single-phase, L = 0.56µH, f_{SW} = 2.2MHz, AAM mode, T_A = 25°C, unless otherwise noted.

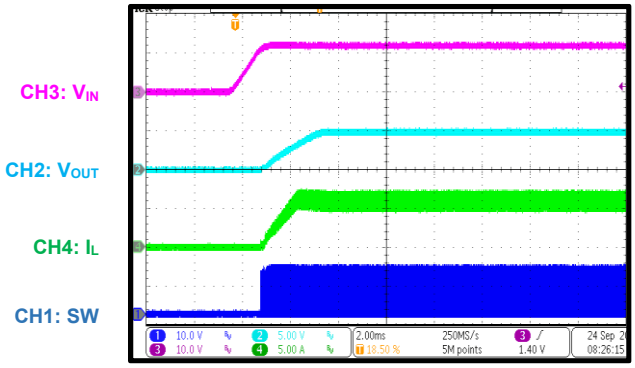
Start-Up through VIN
I_{OUT} = 0A, AAM mode



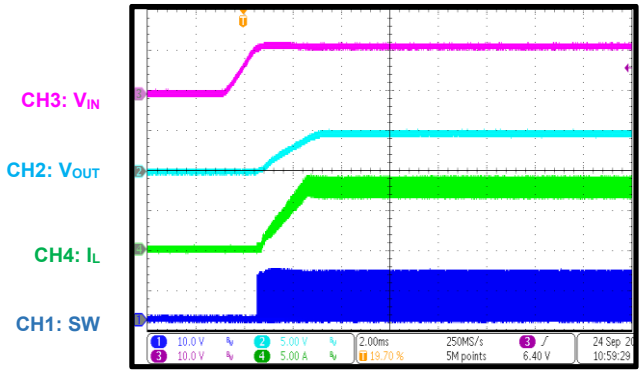
Start-Up through VIN
I_{OUT} = 0A, FCCM



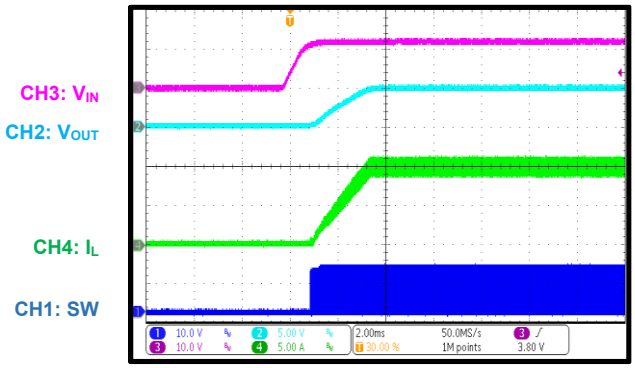
Start-Up through VIN
I_{OUT} = 6A



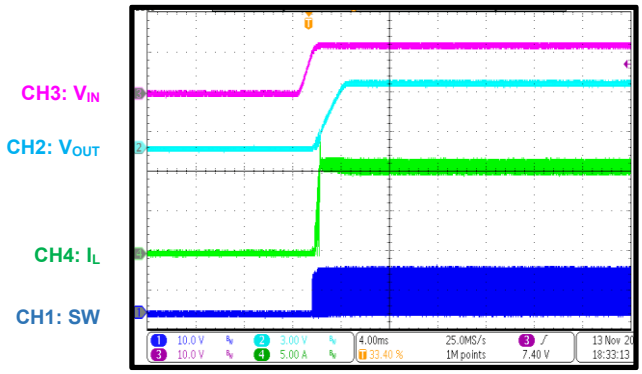
Start-Up through VIN
I_{OUT} = 8A



Start-Up through VIN
I_{OUT} = 10A



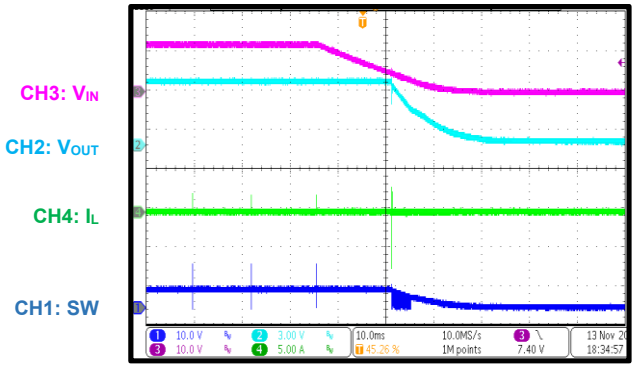
Start-Up through VIN
I_{OUT} = 11A



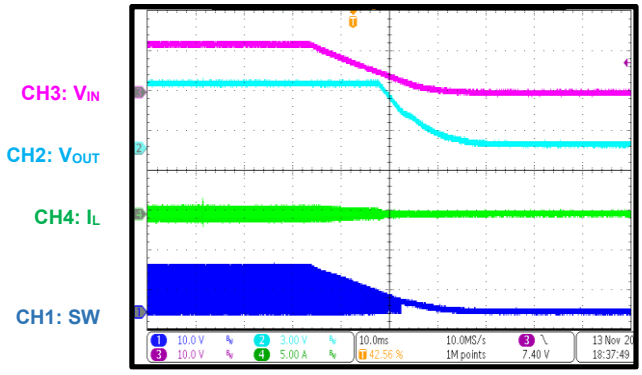
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, single-phase, L = 0.56µH, f_{SW} = 2.2MHz, AAM mode, T_A = 25°C, unless otherwise noted.

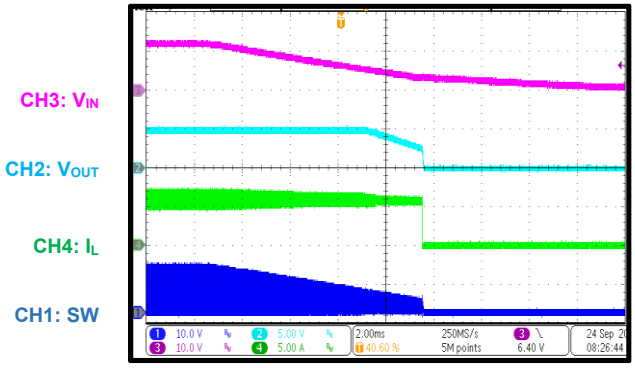
Shutdown through VIN
I_{OUT} = 0A, AAM mode



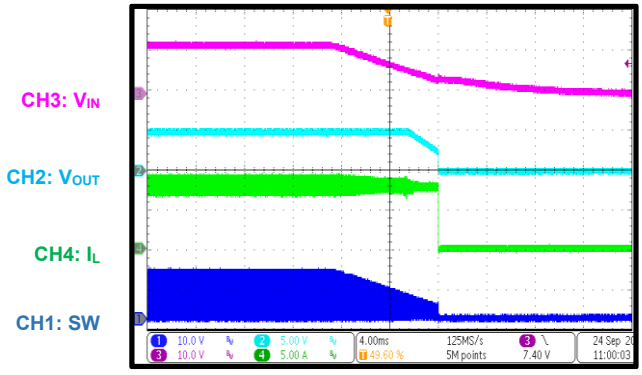
Shutdown through VIN
I_{OUT} = 0A, FCCM



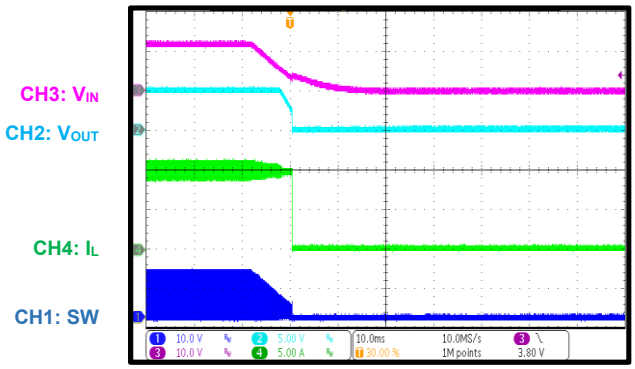
Shutdown through VIN
I_{OUT} = 6A



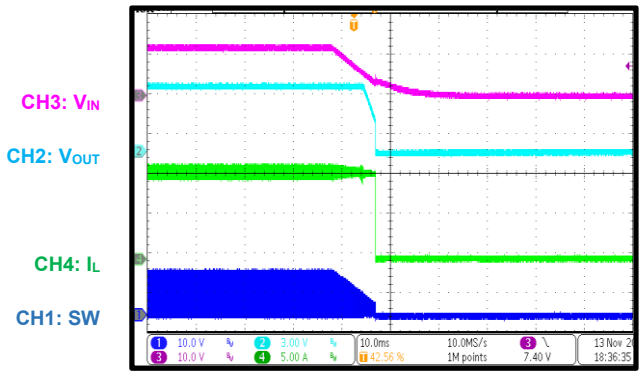
Shutdown through VIN
I_{OUT} = 8A



Shutdown through VIN
I_{OUT} = 10A



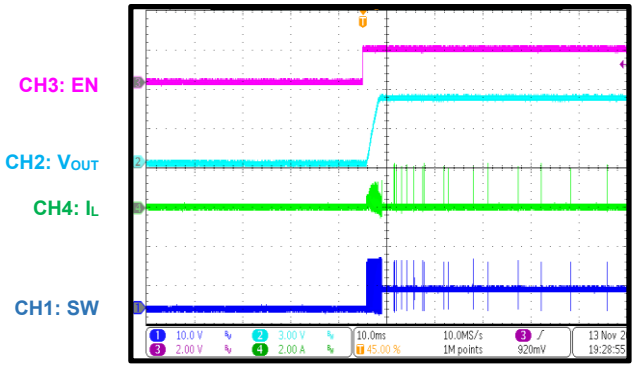
Shutdown through VIN
I_{OUT} = 11A



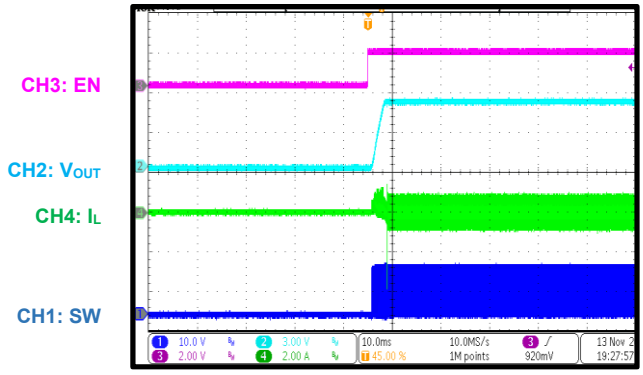
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, single-phase, L = 0.56µH, f_{SW} = 2.2MHz, AAM mode, T_A = 25°C, unless otherwise noted.

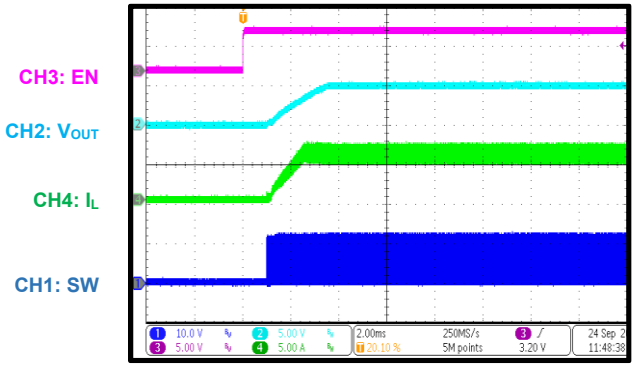
Start-Up through EN
I_{OUT} = 0A, AAM mode



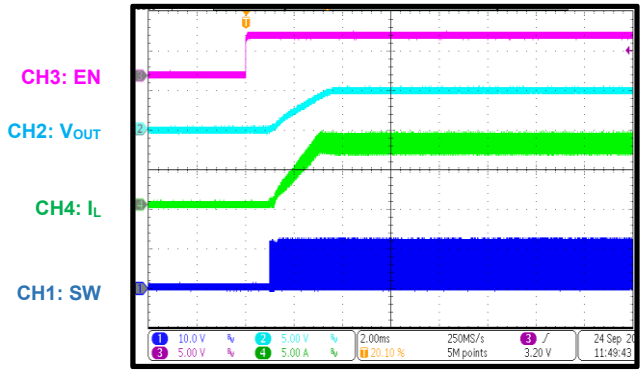
Start-Up through EN
I_{OUT} = 0A, FCCM



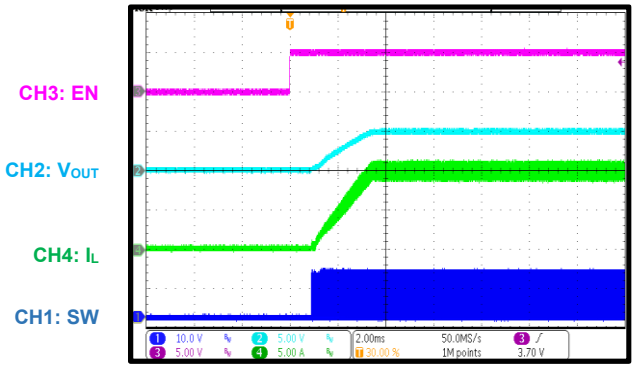
Start-Up through EN
I_{OUT} = 6A



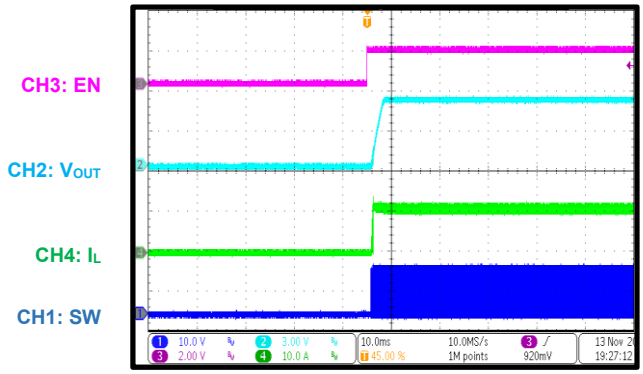
Start-Up through EN
I_{OUT} = 8A



Start-Up through EN
I_{OUT} = 10A



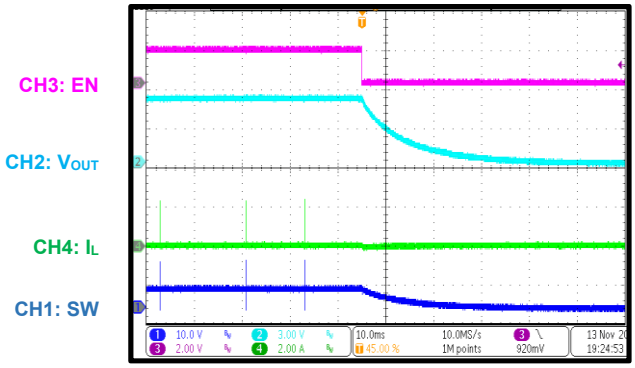
Start-Up through EN
I_{OUT} = 11A



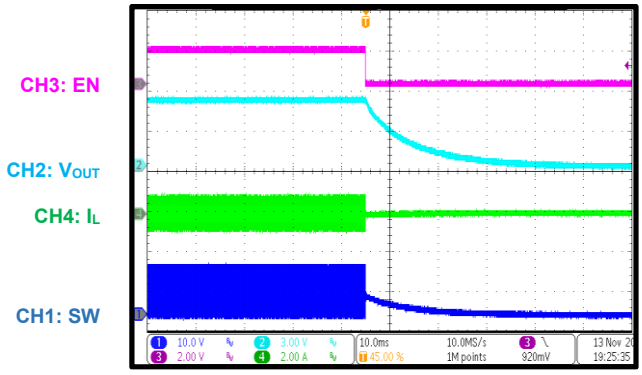
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, single-phase, L = 0.56µH, f_{SW} = 2.2MHz, AAM mode, T_A = 25°C, unless otherwise noted.

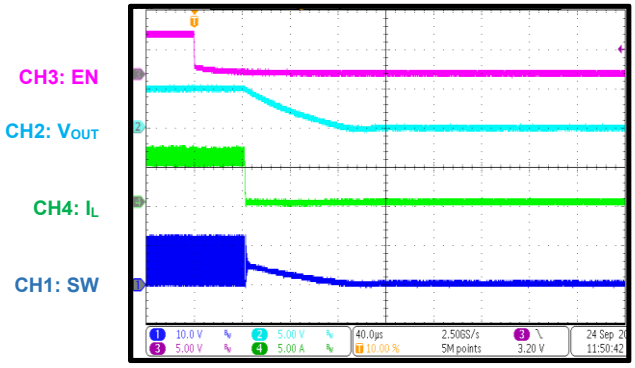
Shutdown through EN
I_{OUT} = 0A, AAM mode



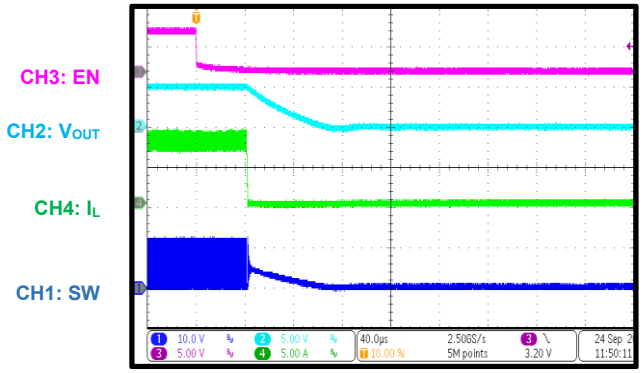
Shutdown through EN
I_{OUT} = 0A, FCCM



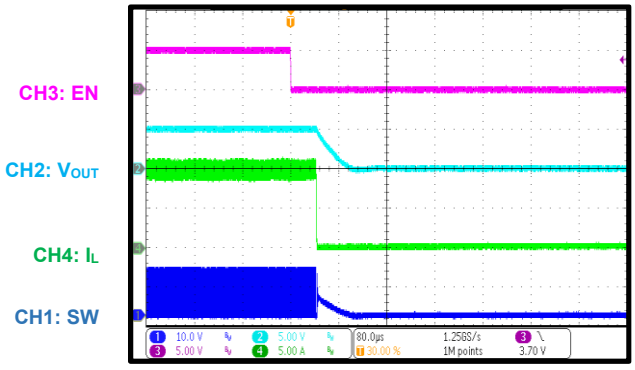
Shutdown through EN
I_{OUT} = 6A



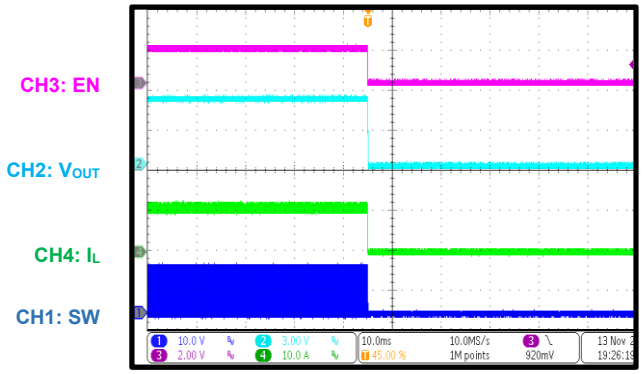
Shutdown through EN
I_{OUT} = 8A



Shutdown through EN
I_{OUT} = 10A



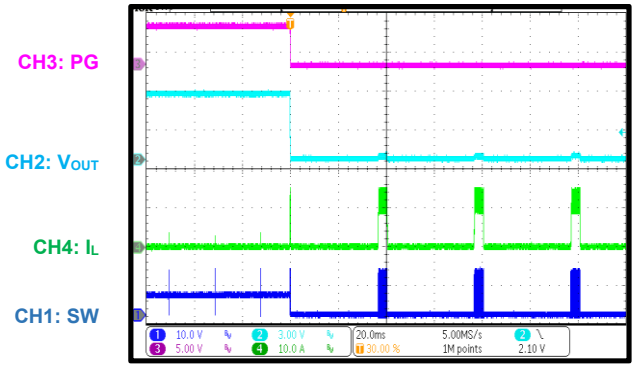
Shutdown through EN
I_{OUT} = 11A



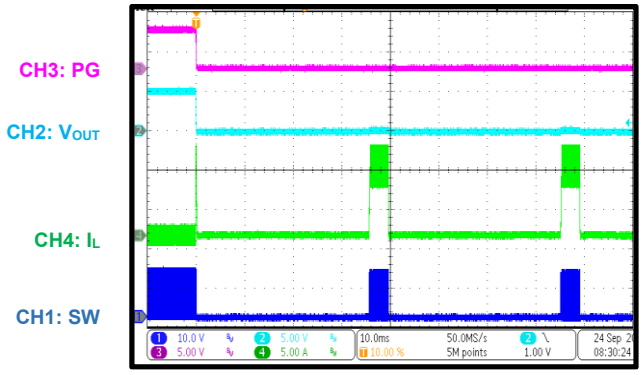
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, single-phase, L = 0.56µH, f_{SW} = 2.2MHz, AAM mode, T_A = 25°C, unless otherwise noted.

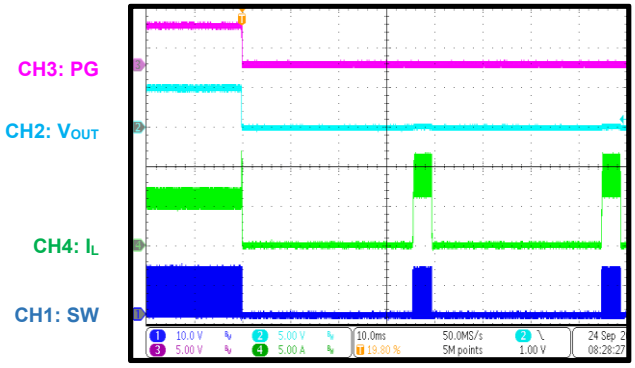
SCP Entry for the MPQ4372-6xxx
I_{OUT} = 0A, AAM mode



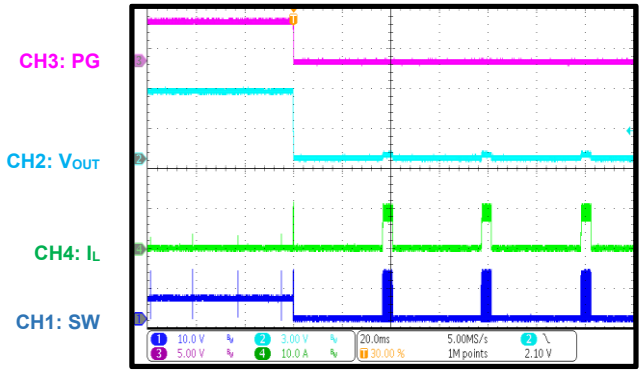
SCP Entry for the MPQ4372-6xxx
I_{OUT} = 0A, FCCM



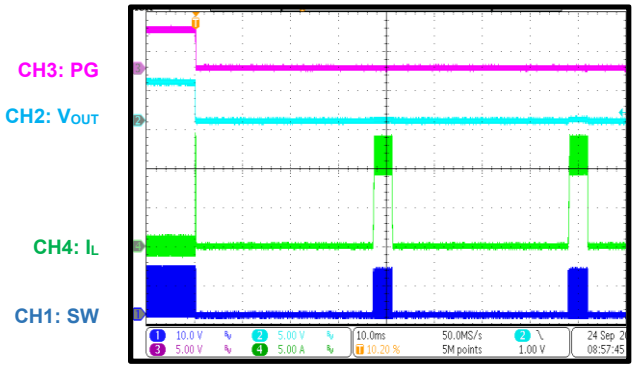
SCP Entry for the MPQ4372-6xxx
v = 6A



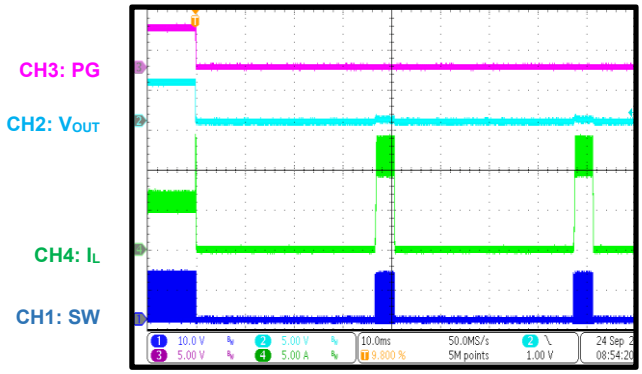
SCP Entry for the MPQ4372-8xxx
I_{OUT} = 0A, AAM mode



SCP Entry for the MPQ4372-8xxx
I_{OUT} = 0A, FCCM



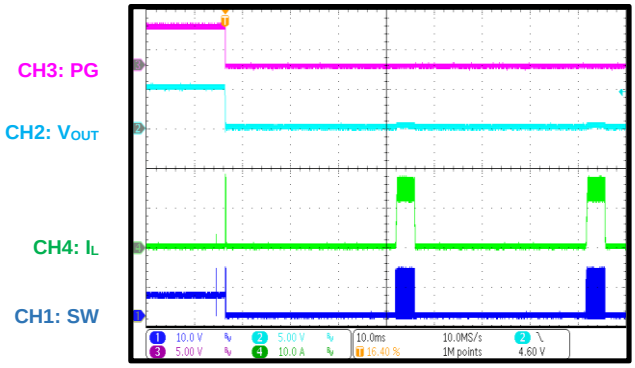
SCP Entry for the MPQ4372-8xxx
I_{OUT} = 8A



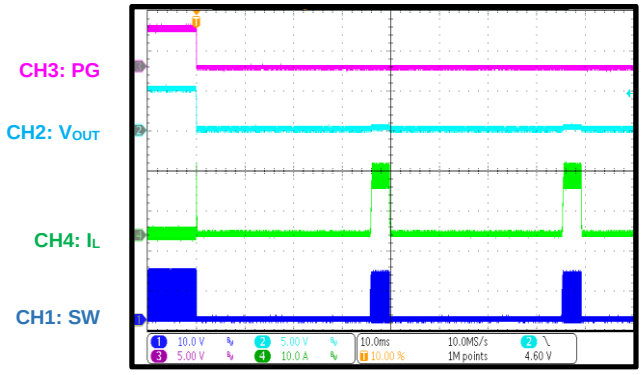
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, single-phase, L = 0.56µH, f_{SW} = 2.2MHz, AAM mode, T_A = 25°C, unless otherwise noted.

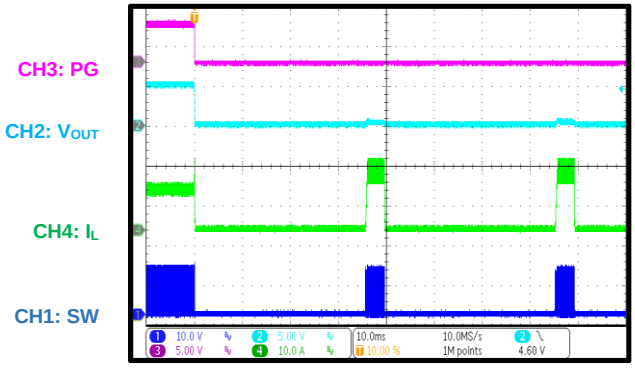
SCP Entry for the MPQ4372-0xxx
I_{OUT} = 0A, AAM mode



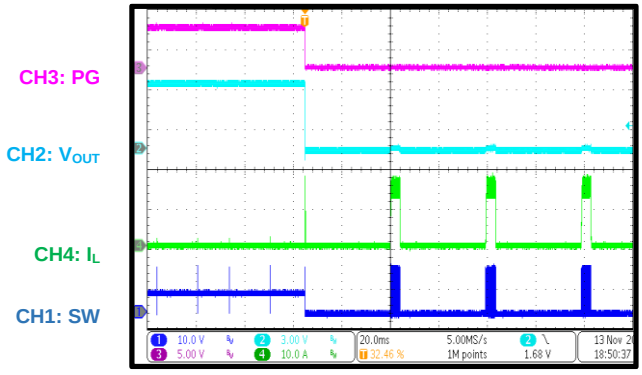
SCP Entry for the MPQ4372-0xxx
I_{OUT} = 0A, FCCM



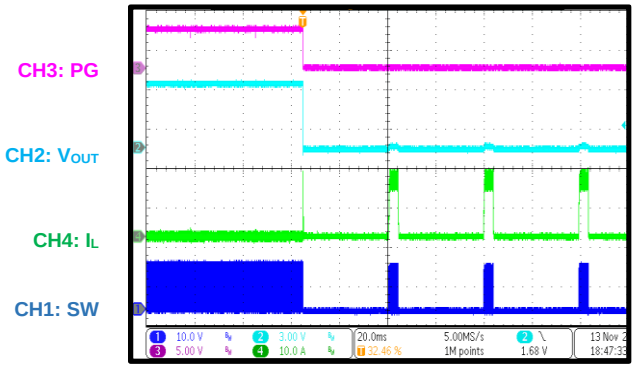
SCP Entry for the MPQ4372-0xxx
I_{OUT} = 10A, FCCM



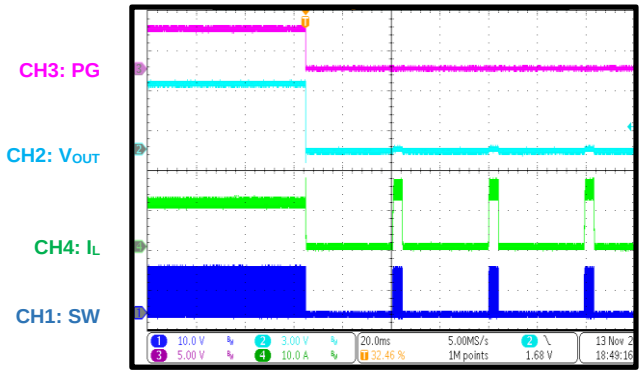
SCP Entry for the MPQ4372-1xxx
I_{OUT} = 0A, AAM mode



SCP Entry for the MPQ4372-1xxx
I_{OUT} = 0A, FCCM



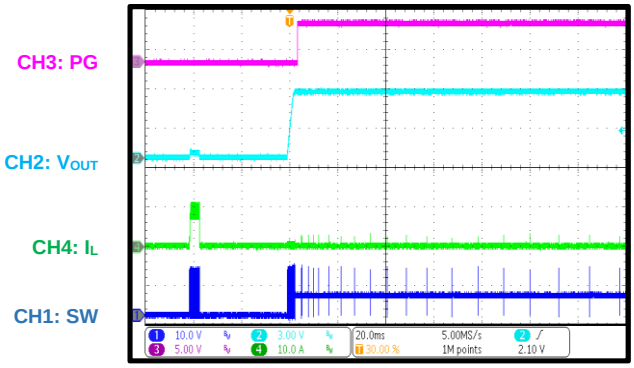
SCP Entry for the MPQ4372-1xxx
I_{OUT} = 11A



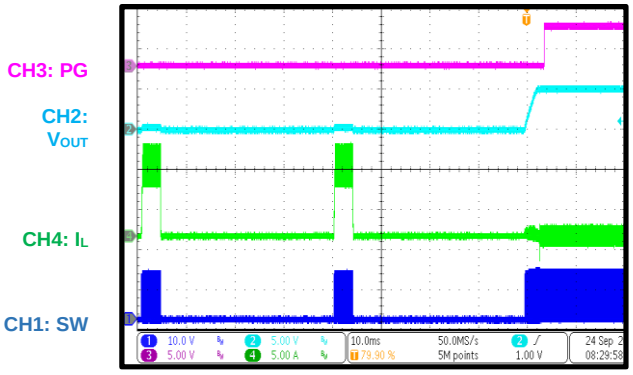
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, single-phase, L = 0.56µH, f_{SW} = 2.2MHz, AAM mode, T_A = 25°C, unless otherwise noted.

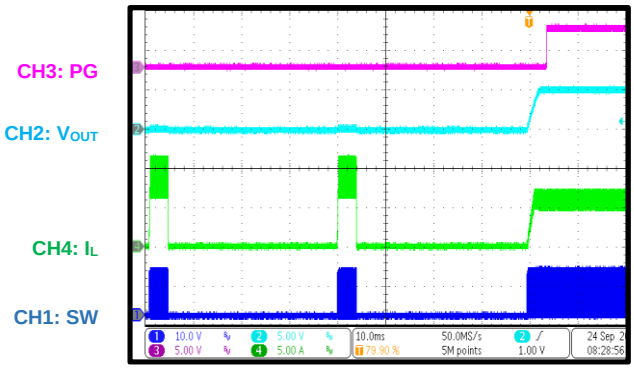
SCP Recovery for the MPQ4372-6xxx
I_{OUT} = 0A, AAM mode



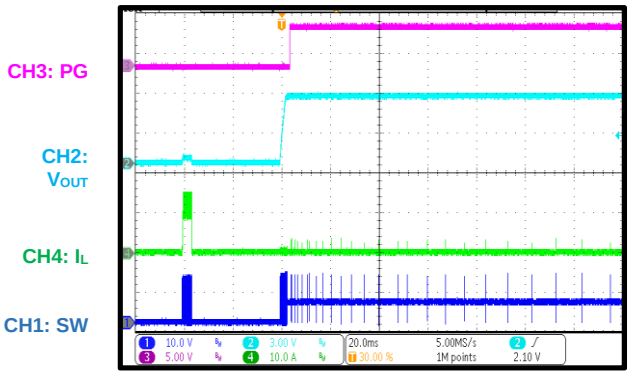
SCP Recovery for the MPQ4372-6xxx
I_{OUT} = 0A, FCCM



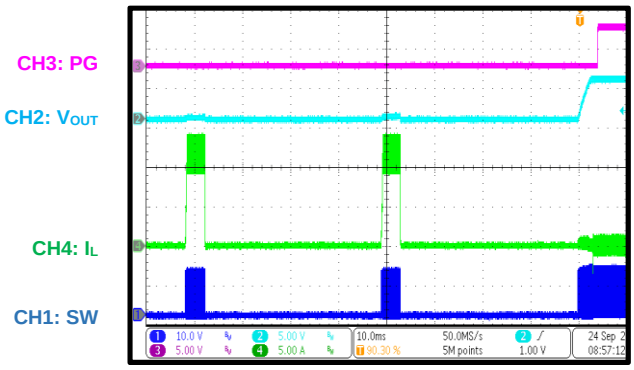
SCP Recovery for the MPQ4372-6xxx
I_{OUT} = 6A



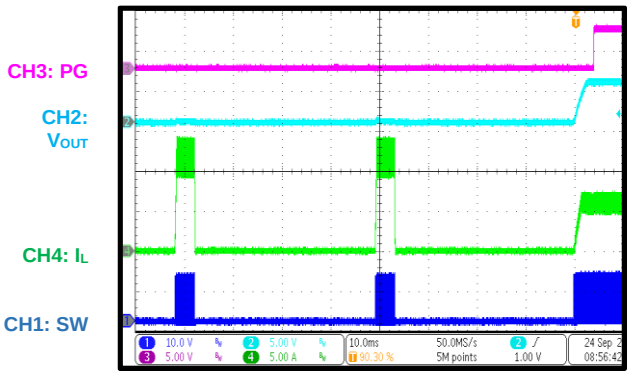
SCP Recovery for the MPQ4372-8xxx
I_{OUT} = 0A, AAM mode



SCP Recovery for the MPQ4372-8xxx
I_{OUT} = 8A, FCCM



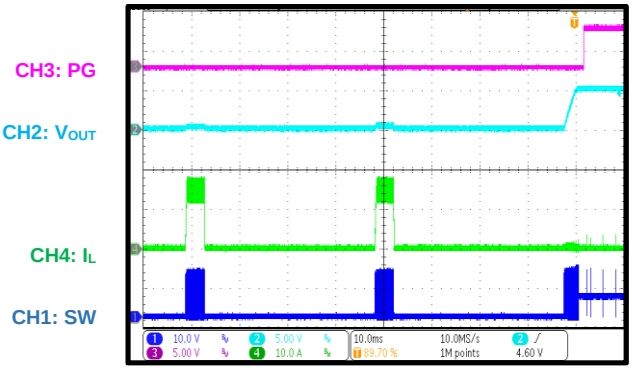
SCP Recovery for the MPQ4372-8xxx
I_{OUT} = 8A



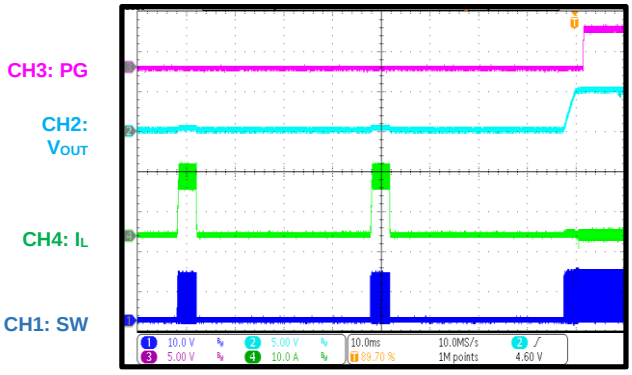
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, single-phase, L = 0.56µH, f_{SW} = 2.2MHz, AAM mode, T_A = 25°C, unless otherwise noted.

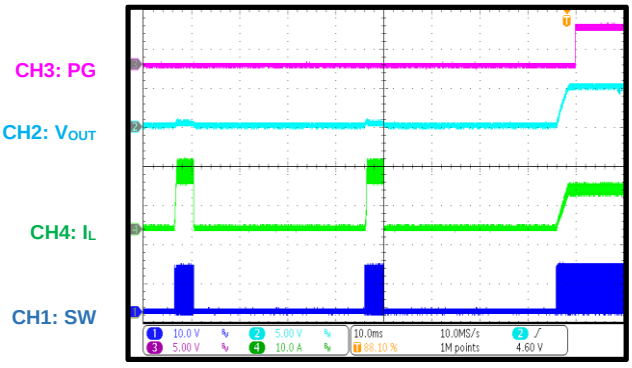
SCP Recovery for the MPQ4372-0xxx
I_{OUT} = 0A, AAM mode



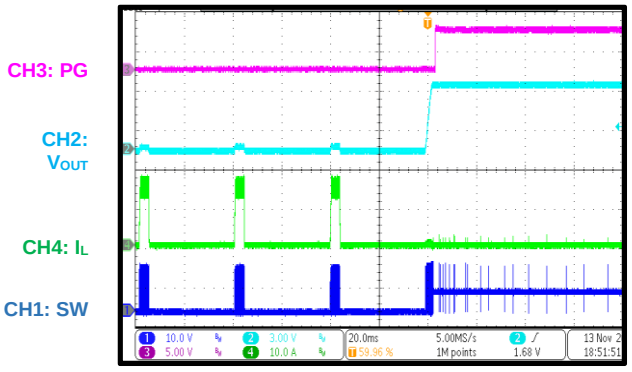
SCP Recovery for the MPQ4372-0xxx
I_{OUT} = 0A, FCCM



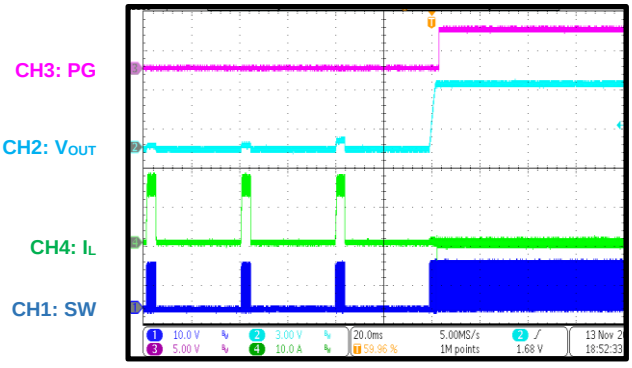
SCP Recovery for the MPQ4372-0xxx
I_{OUT} = 10A



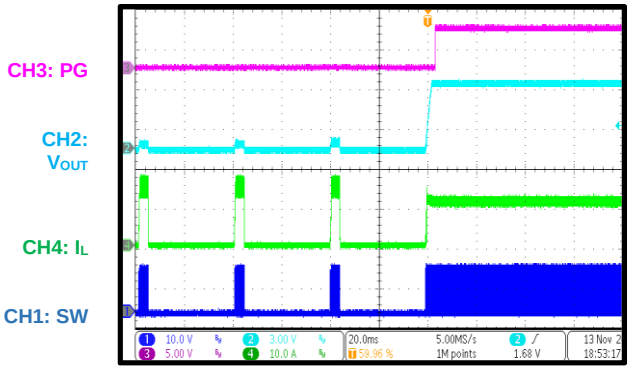
SCP Recovery for the MPQ4372-1xxx
I_{OUT} = 0A, AAM mode



SCP Recovery for the MPQ4372-1xxx
I_{OUT} = 0A, FCCM



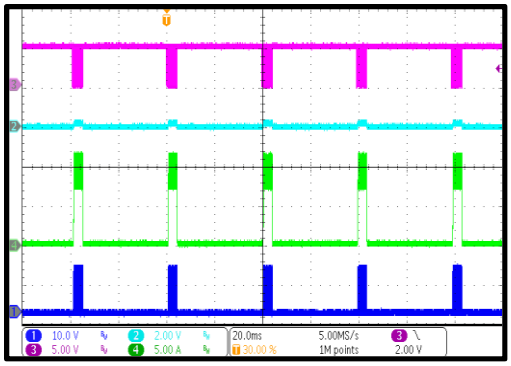
SCP Recovery for the MPQ4372-1xxx
I_{OUT} = 11A



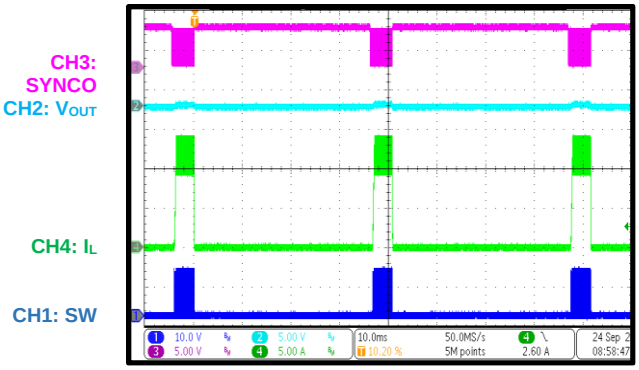
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, single-phase, L = 0.56µH, f_{SW} = 2.2MHz, AAM mode, T_A = 25°C, unless otherwise noted.

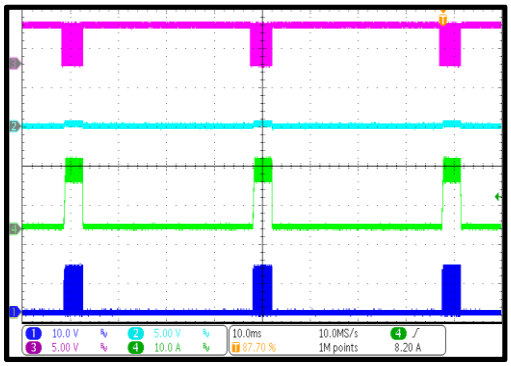
SCP Steady State for the MPQ4372-6xxx



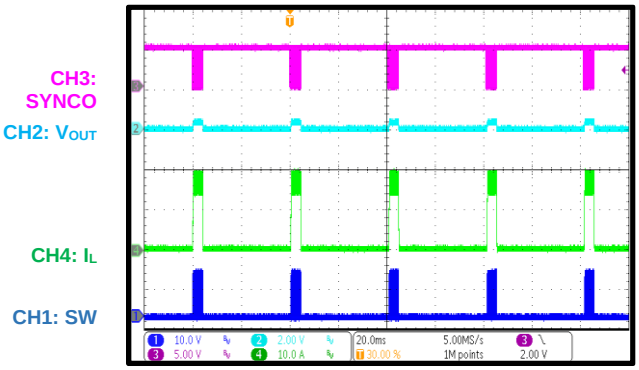
SCP Steady State for the MPQ4372-8xxx



SCP Steady State for the MPQ4372-0xxx

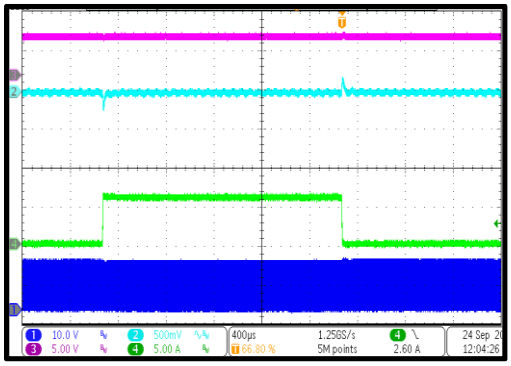


SCP Steady State for the MPQ4372-1xxx



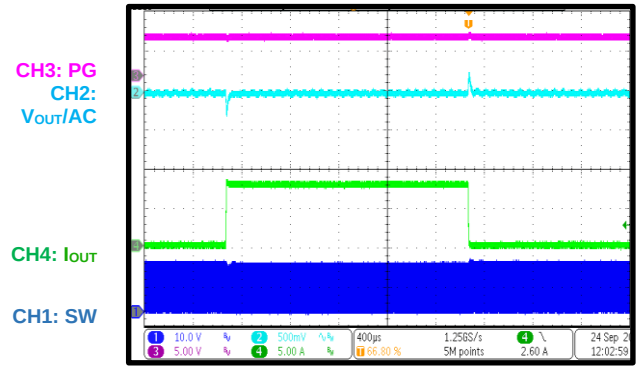
Load Transient

I_{OUT} = 0A to 6A, 1.6A/µs, FCCM



Load Transient

I_{OUT} = 0A to 8A, 1.6A/µs, FCCM

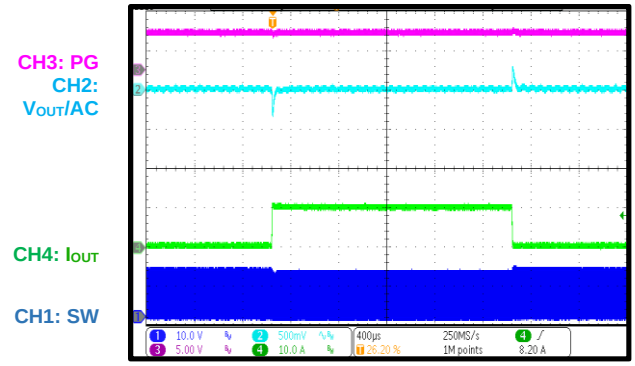


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, single-phase, L = 0.56µH, f_{SW} = 2.2MHz, AAM mode, T_A = 25°C, unless otherwise noted.

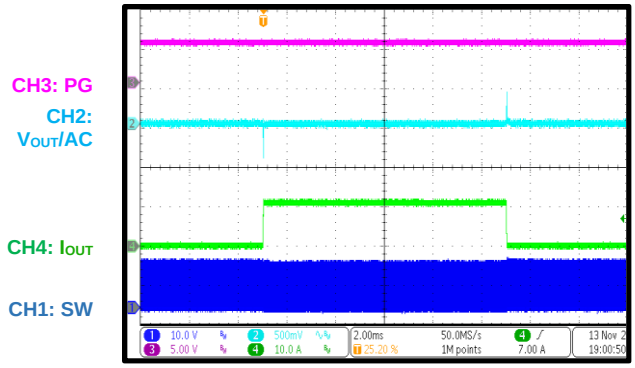
Load Transient

I_{OUT} = 0A to 10A, 1.6A/µs, FCCM



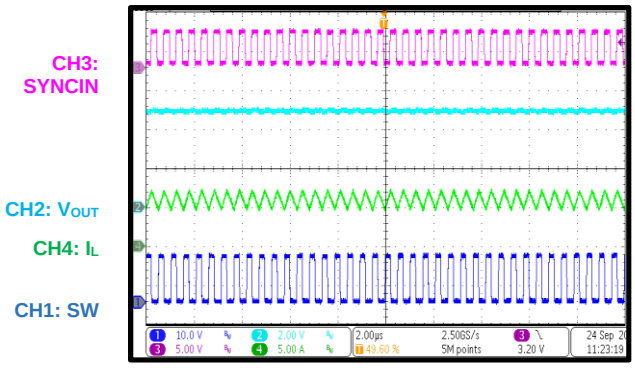
Load Transient

I_{OUT} = 0A to 11A, 1.6A/µs, FCCM



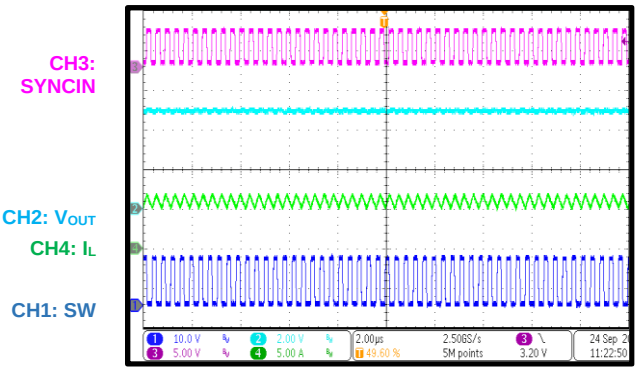
SYNCIN Operation

I_{OUT} = 6A, f_{SW} = 2.2MHz, f_{SYNC} = 1.9MHz



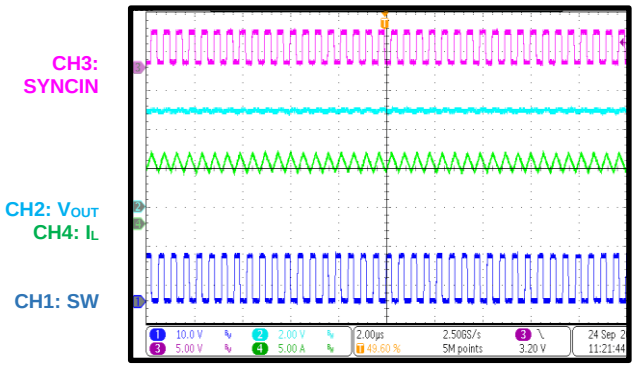
SYNCIN Operation

I_{OUT} = 6A, f_{SW} = 2.2MHz, f_{SYNC} = 2.6MHz



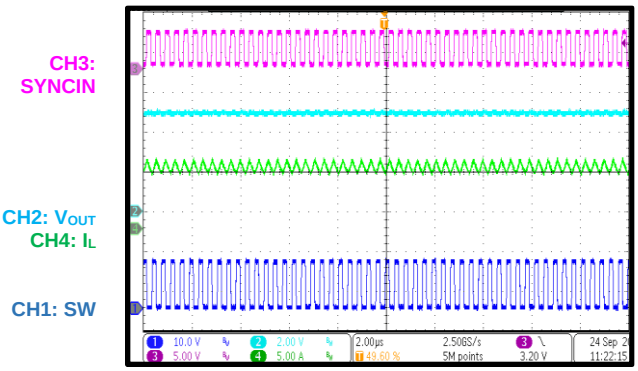
SYNCIN Operation

I_{OUT} = 8A, f_{SW} = 2.2MHz, f_{SYNC} = 1.9MHz



SYNCIN Operation

I_{OUT} = 8A, f_{SW} = 2.2MHz, f_{SYNC} = 2.6MHz

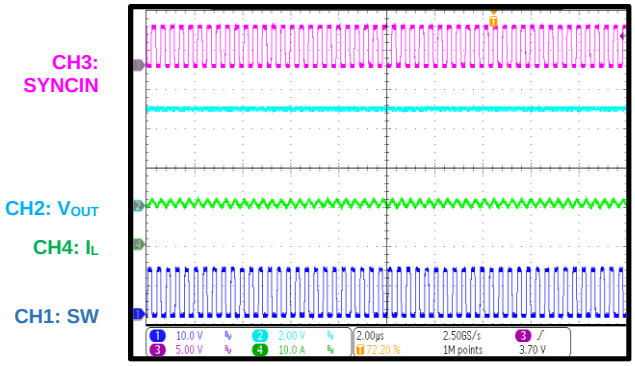


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, single-phase, L = 0.56µH, f_{SW} = 2.2MHz, AAM mode, T_A = 25°C, unless otherwise noted.

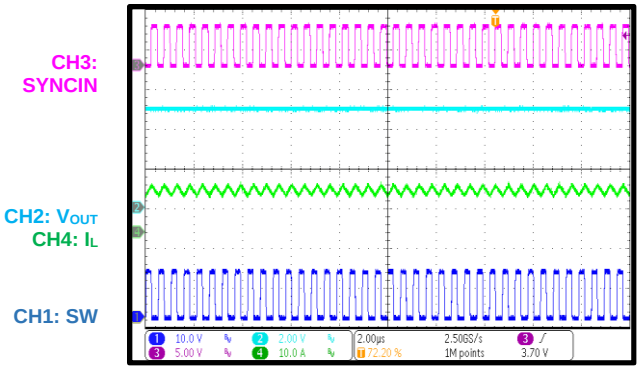
SYNCIN Operation

I_{OUT} = 10A, f_{SW} = 2.2MHz, f_{SYNC} = 1.9MHz



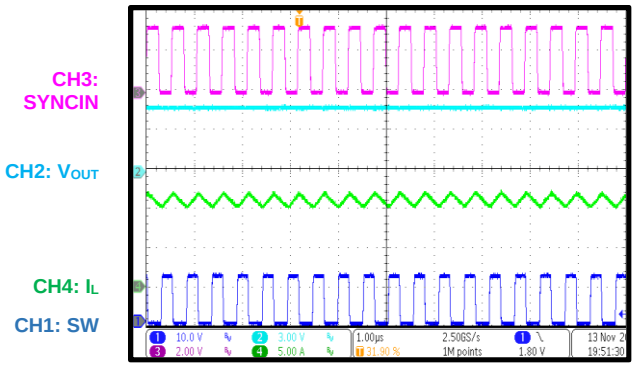
SYNCIN Operation

I_{OUT} = 10A, f_{SW} = 2.2MHz, f_{SYNC} = 2.6MHz



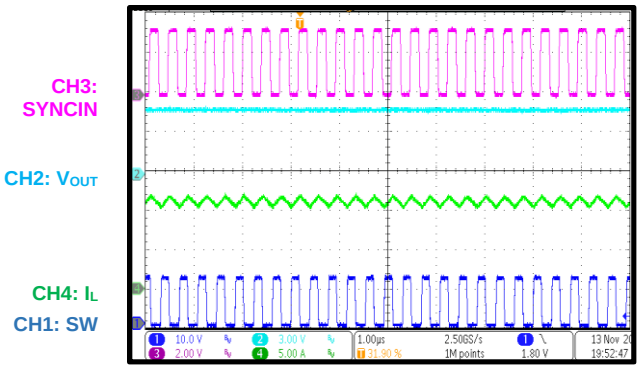
SYNCIN Operation

I_{OUT} = 11A, f_{SW} = 2.2MHz, f_{SYNC} = 1.9MHz



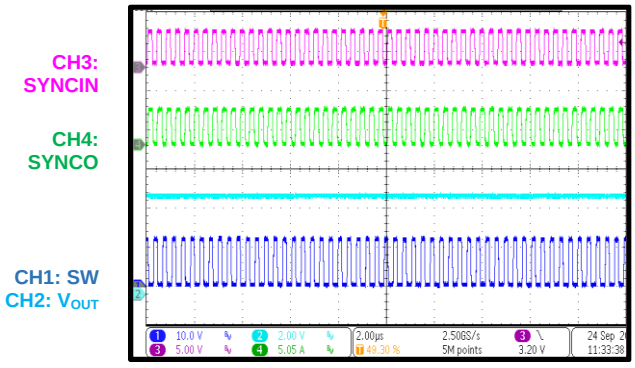
SYNCIN Operation

I_{OUT} = 11A, f_{SW} = 2.2MHz, f_{SYNC} = 2.6MHz



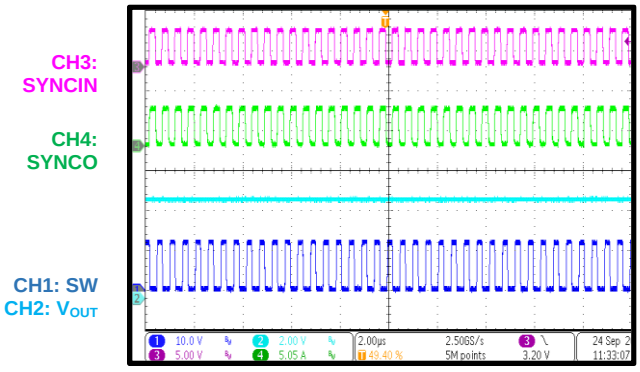
SYNCO Operation

I_{OUT} = 11A, f_{SW} = 2.2MHz, f_{SYNC} = 1.9MHz



SYNCO Operation

I_{OUT} = 11A, f_{SW} = 2.2MHz, f_{SYNC} = 2.6MHz

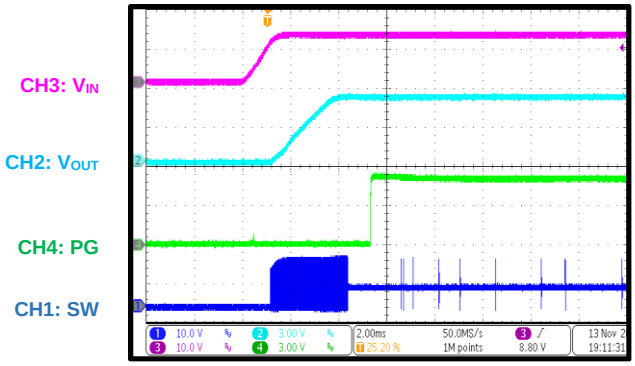


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, single-phase, L = 0.56µH, f_{SW} = 2.2MHz, AAM mode, T_A = 25°C, unless otherwise noted.

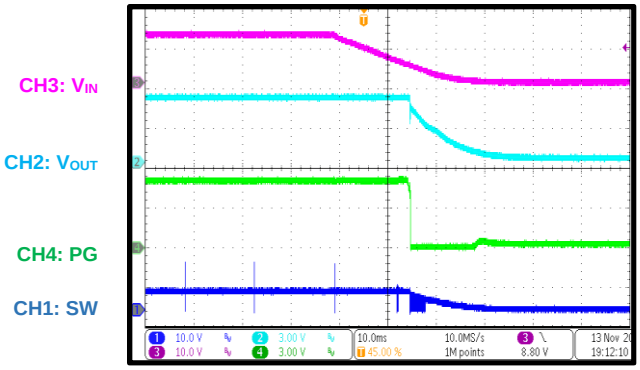
PG in Start-Up through VIN

I_{OUT} = 0A, AAM mode



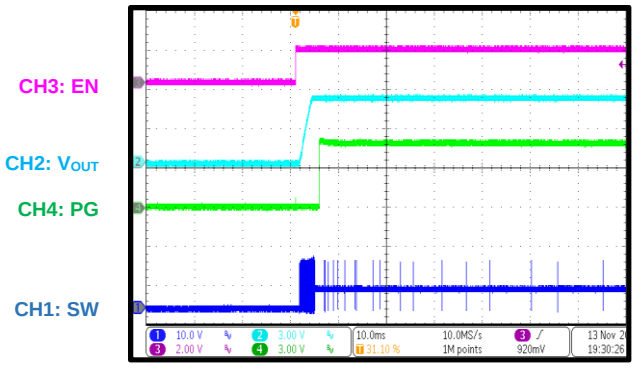
PG in Shutdown through VIN

I_{OUT} = 0A, AAM mode



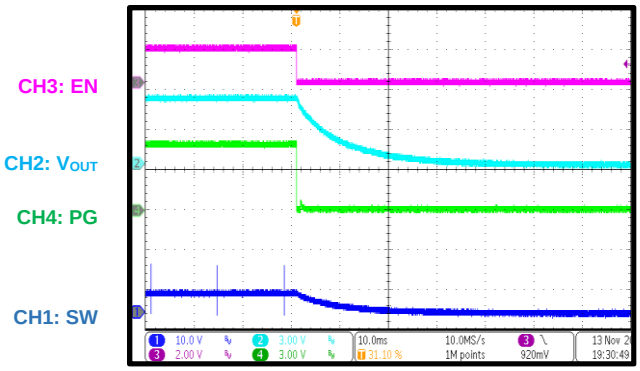
PG in Start-Up through EN

I_{OUT} = 0A, AAM mode



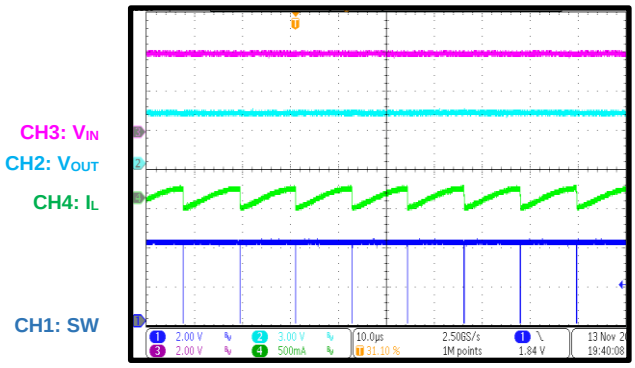
PG in Shutdown through EN

I_{OUT} = 0A, AAM mode



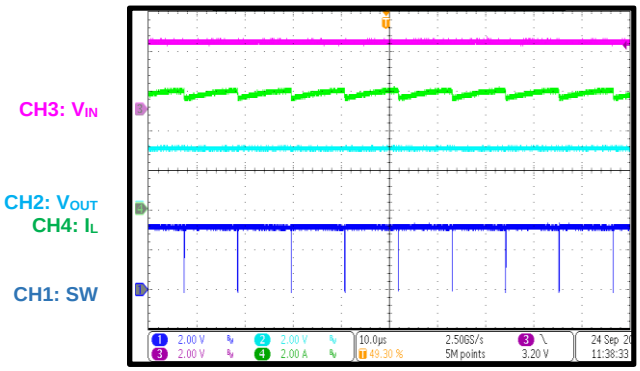
Low-Dropout Mode

V_{IN} = 4V, V_{OUT} set to 5V, I_{OUT} = 0A



Low-Dropout Mode

V_{IN} = 4V, V_{OUT} set to 5V, I_{OUT} = 6A

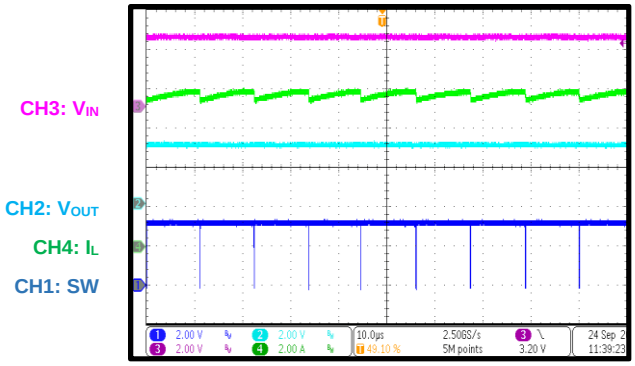


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, single-phase, L = 0.56µH, f_{SW} = 2.2MHz, AAM mode, T_A = 25°C, unless otherwise noted.

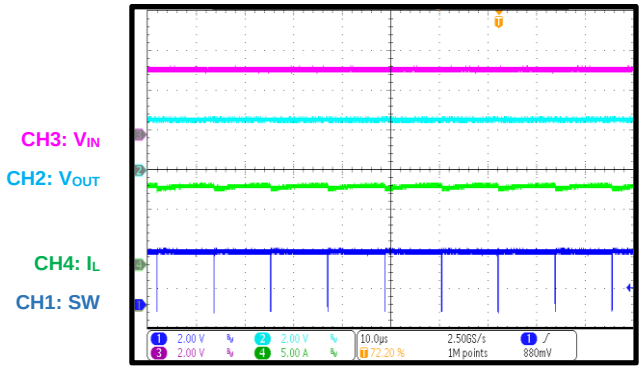
Low-Dropout Mode

V_{IN} = 4V, V_{OUT} set to 5V, I_{OUT} = 8A



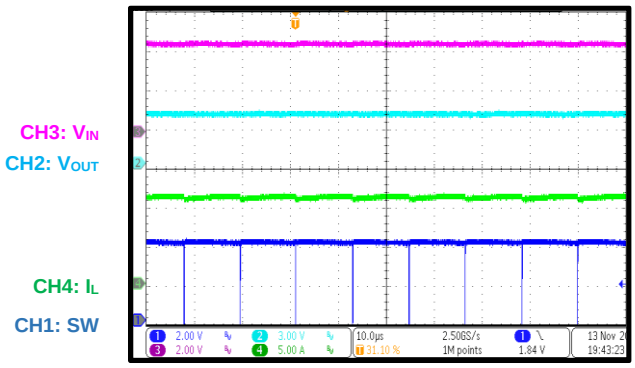
Low-Dropout Mode

V_{IN} = 4V, V_{OUT} set to 5V, I_{OUT} = 10A



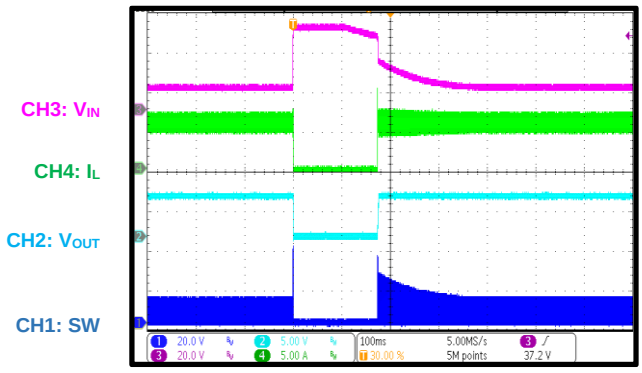
Low-Dropout Mode

V_{IN} = 3.3V, V_{OUT} set to 5V, I_{OUT} = 11A



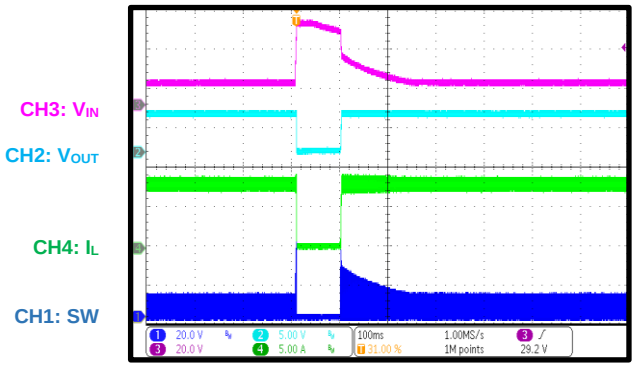
Load Dump

V_{IN} = 12V to 42V, I_{OUT} = 6A



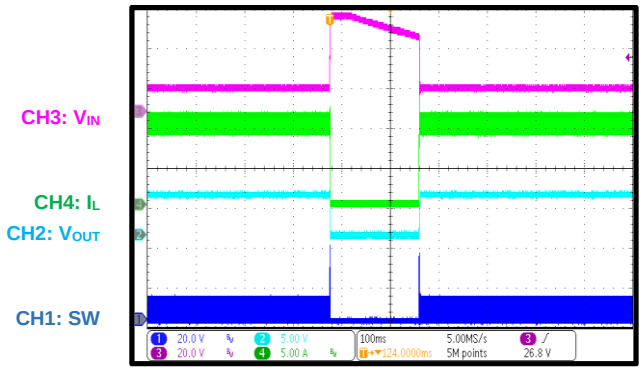
Load Dump

V_{IN} = 12V to 42V, I_{OUT} = 8A



Load Dump

V_{IN} = 12V to 42V, I_{OUT} = 10A

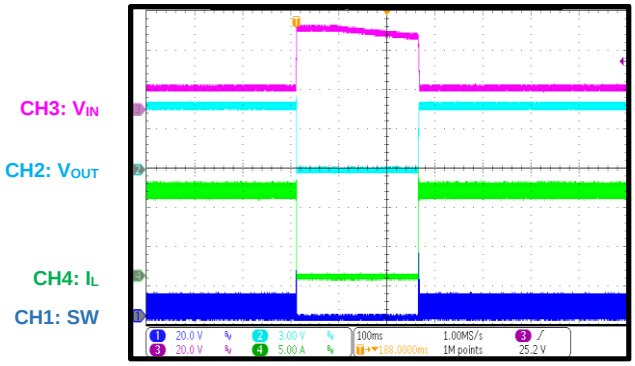


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, single-phase, L = 0.56µH, f_{SW} = 2.2MHz, AAM mode, T_A = 25°C, unless otherwise noted.

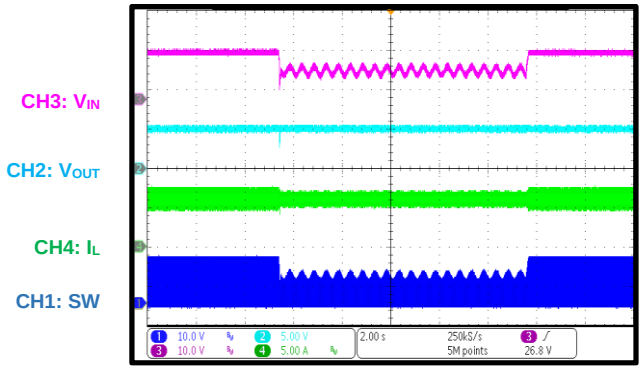
Load Dump

V_{IN} = 12V to 42V, I_{OUT} = 11A



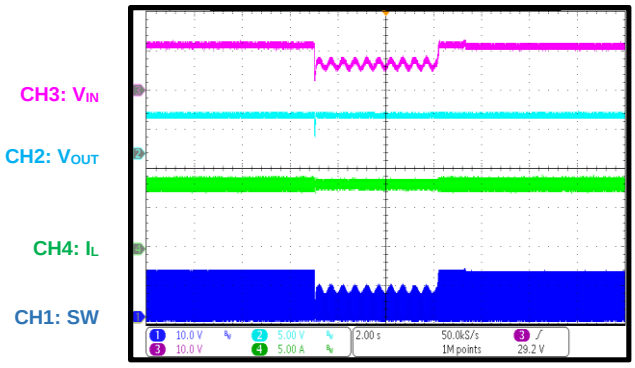
Cold Crank

I_{OUT} = 6A



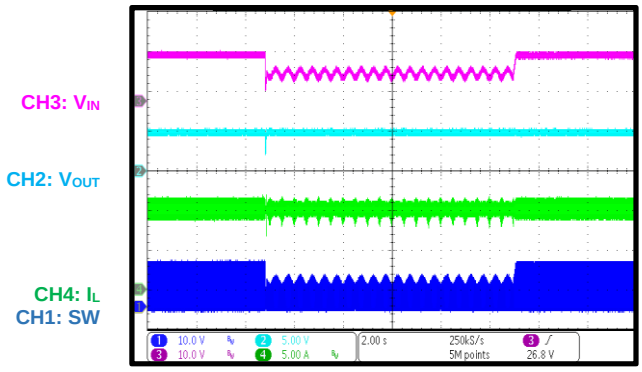
Cold Crank

I_{OUT} = 8A



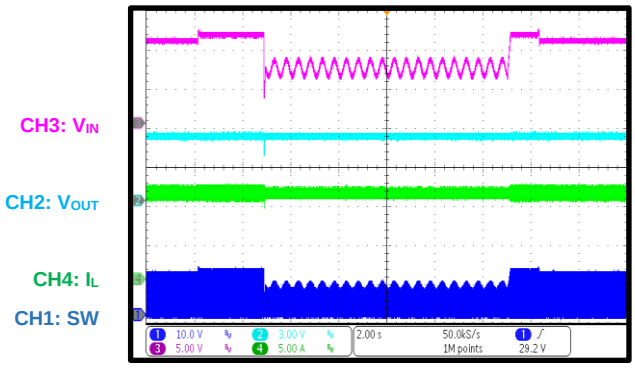
Cold Crank

I_{OUT} = 10A



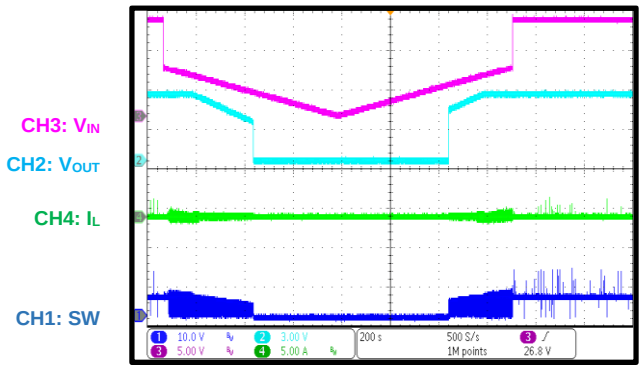
Cold Crank

I_{OUT} = 11A



V_{IN} Ramping Down and Up

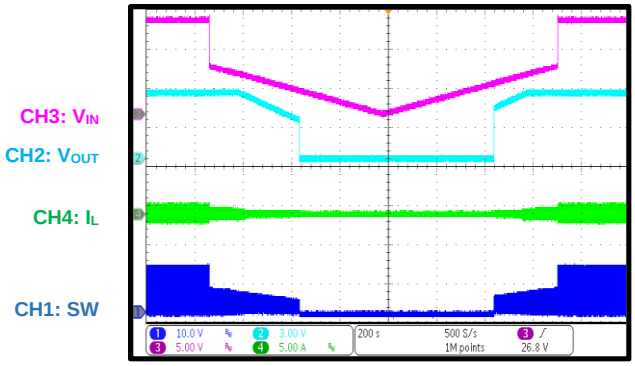
I_{OUT} = 0A, AAM mode



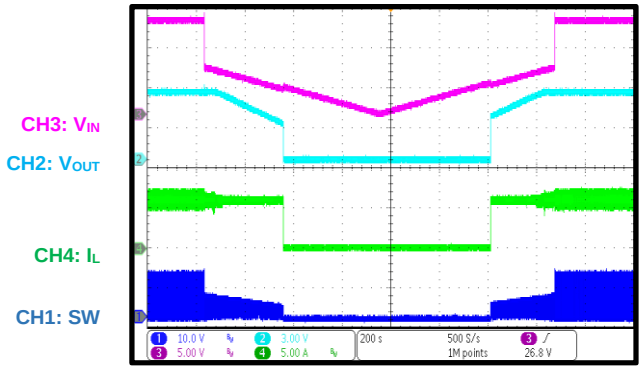
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, single-phase, L = 0.56µH, f_{SW} = 2.2MHz, AAM mode, T_A = 25°C, unless otherwise noted.

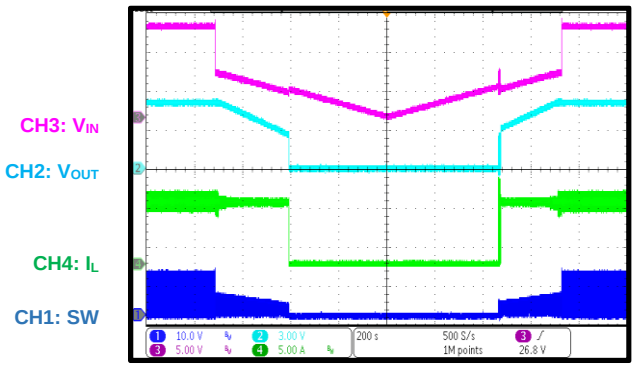
V_{IN} Ramping Down and Up
I_{OUT} = 0A, FCCM



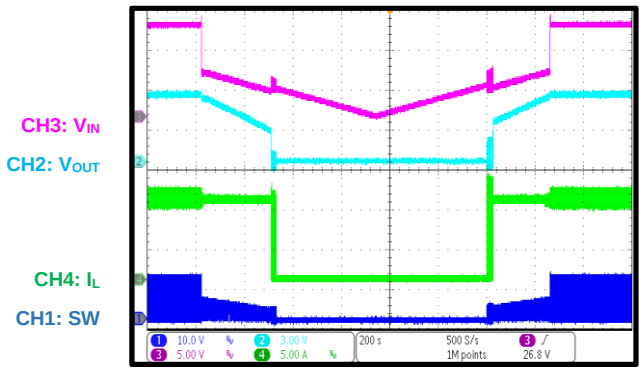
V_{IN} Ramping Down and Up
I_{OUT} = 6A



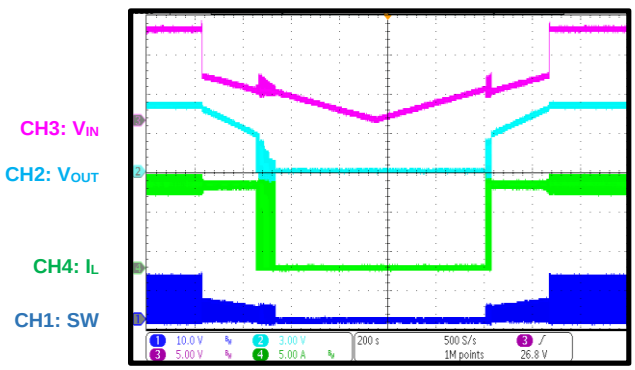
V_{IN} Ramping Down and Up
I_{OUT} = 8A



V_{IN} Ramping Down and Up
I_{OUT} = 10A



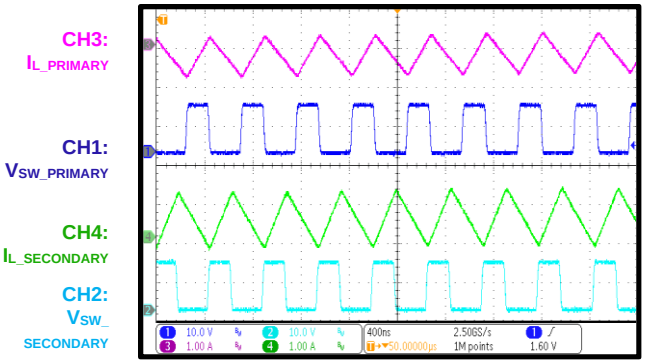
V_{IN} Ramping Down and Up
I_{OUT} = 11A



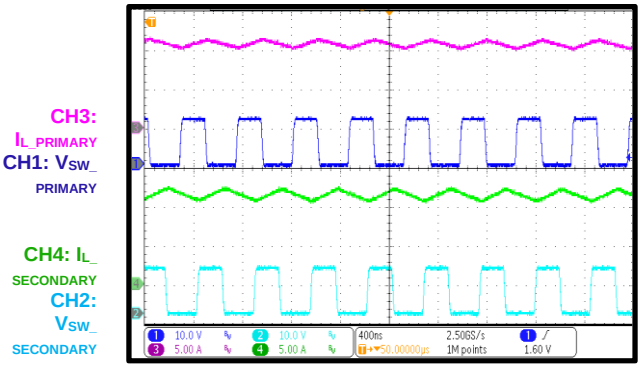
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, dual-phase, L = 0.56µH, f_{SW} = 2.2MHz, AAM mode, T_A = 25°C, unless otherwise noted.

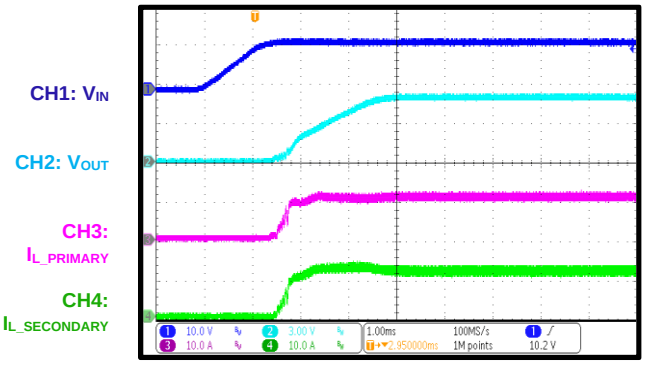
Steady State
I_{OUT} = 0A



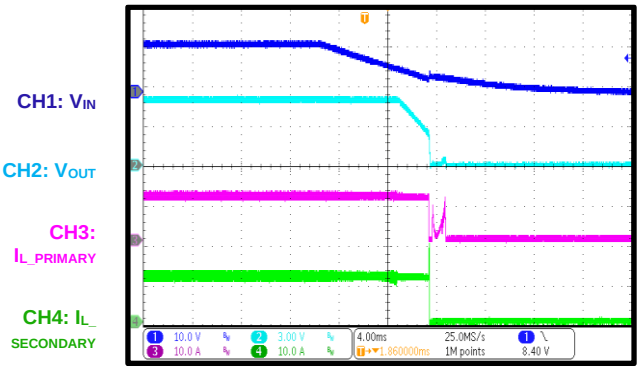
Steady State
I_{OUT} = 22A



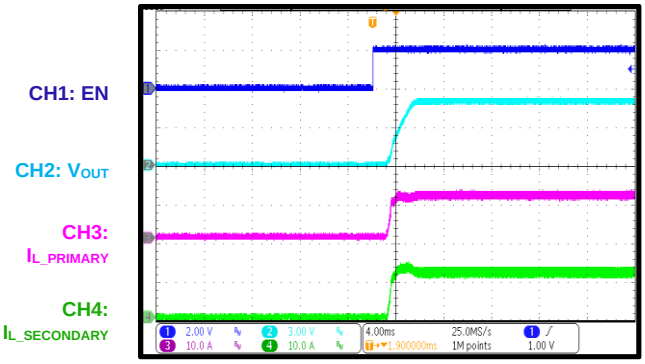
Start-Up through VIN
I_{OUT} = 22A



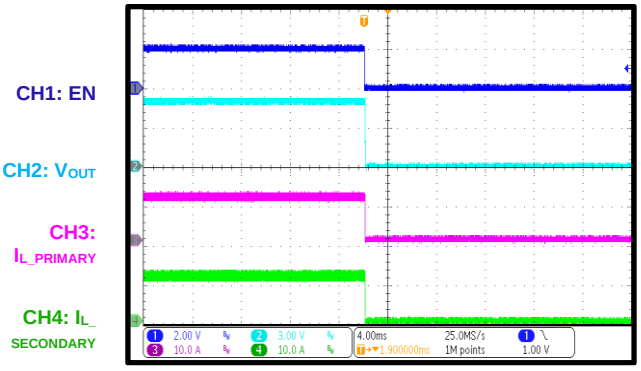
Shutdown through VIN
I_{OUT} = 22A



Start-Up through EN
I_{OUT} = 22A



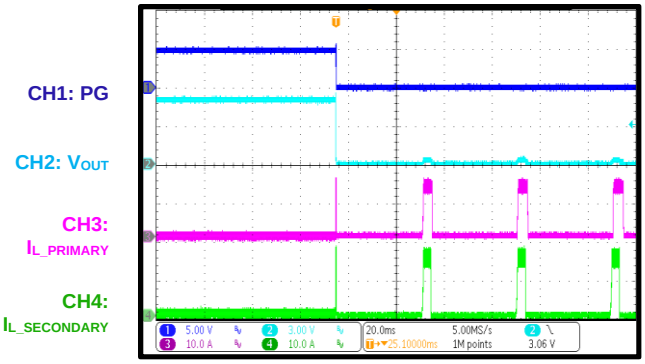
Shutdown through EN
I_{OUT} = 22A



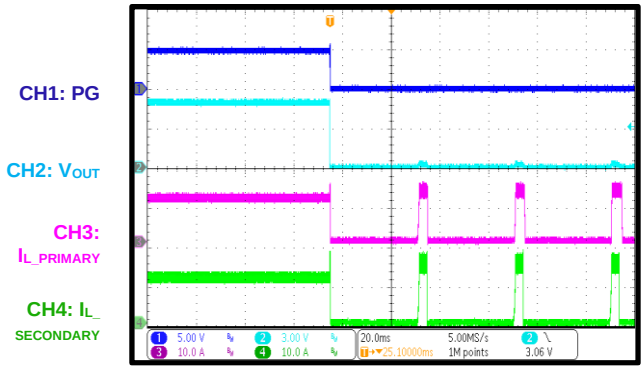
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, dual-phase, L = 0.56µH, f_{SW} = 2.2MHz, AAM mode, T_A = 25°C, unless otherwise noted.

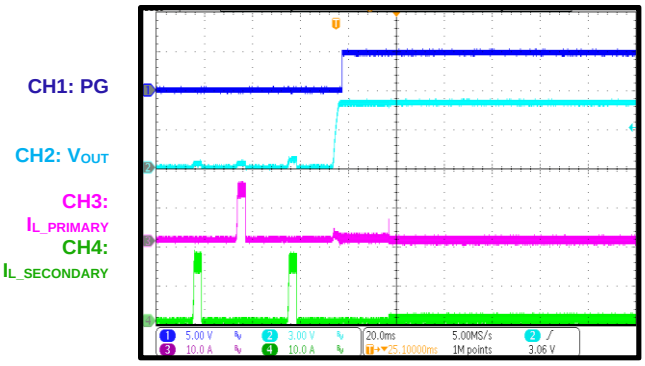
SCP Entry
I_{OUT} = 0A



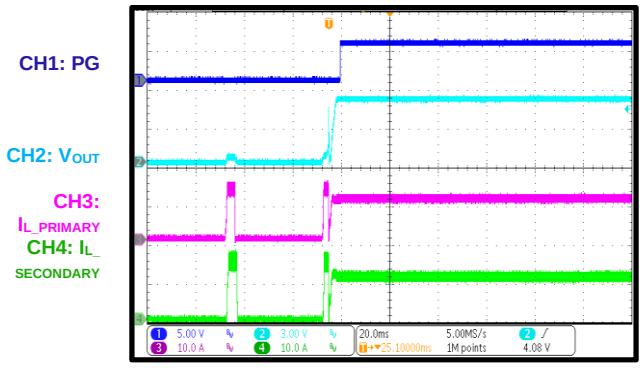
SCP Entry
I_{OUT} = 22A



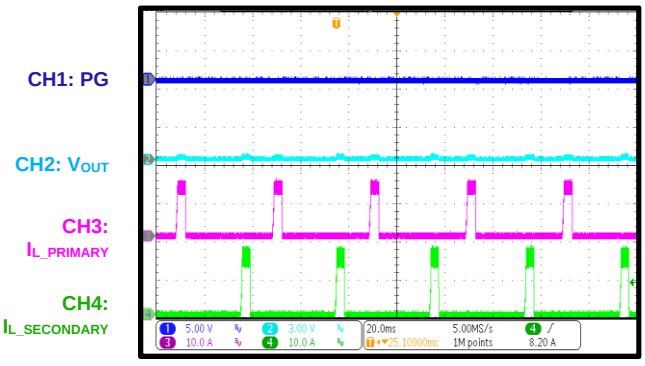
SCP Recovery
I_{OUT} = 0A



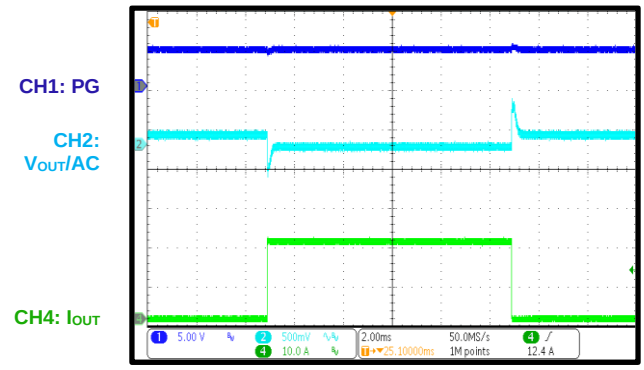
SCP Recovery
I_{OUT} = 22A



SCP Steady State



Load Transient
I_{OUT} = 0A to 22A, 1.6A/µs

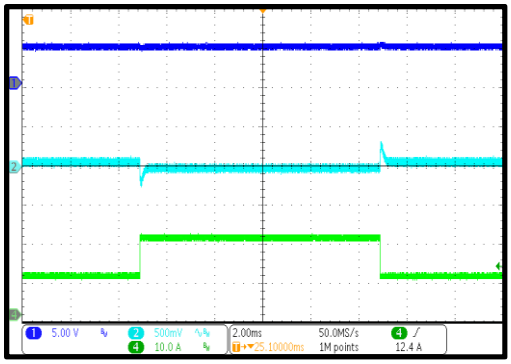


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, dual-phase, L = 0.56µH, f_{SW} = 2.2MHz, AAM mode, T_A = 25°C, unless otherwise noted.

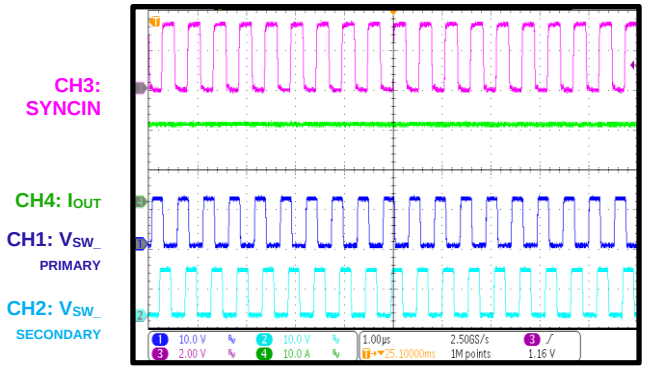
Load Transient

I_{OUT} = 10A to 22A, 1.6A/µs



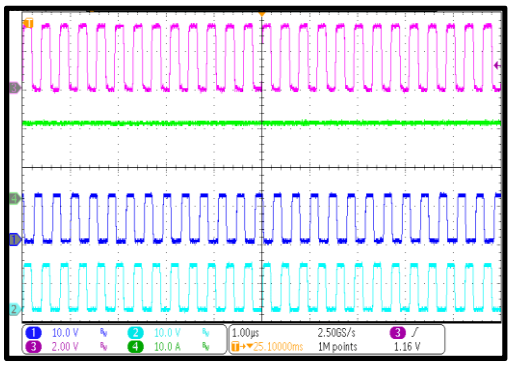
SYNCIN Operation

I_{OUT} = 22A, f_{SYNC} = 1.9MHz



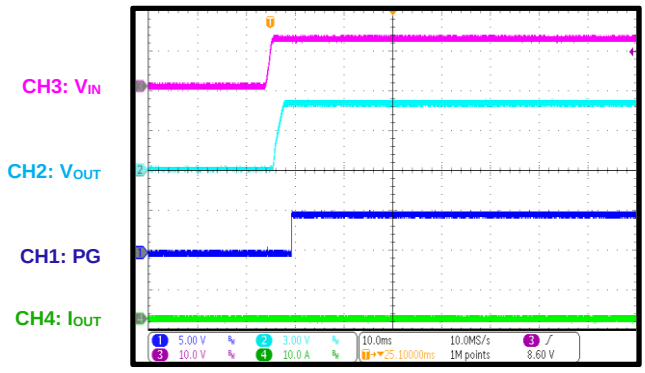
SYNCIN Operation

I_{OUT} = 22A, f_{SYNC} = 2.6MHz



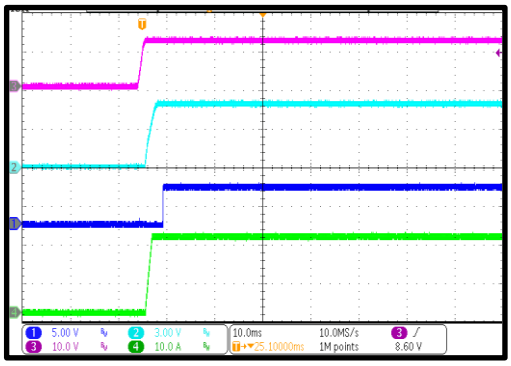
PG in Start-Up through VIN

I_{OUT} = 0A



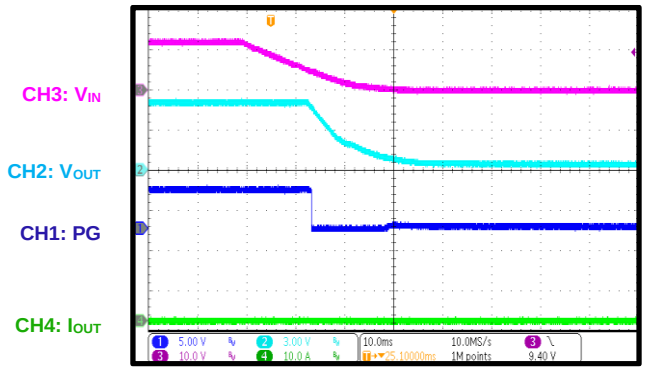
PG in Start-Up through VIN

I_{OUT} = 22A



PG in Shutdown through VIN

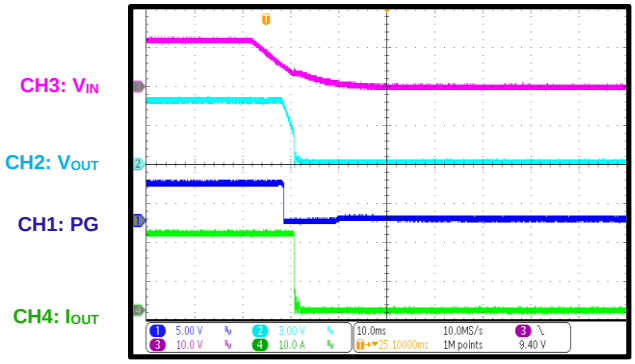
I_{OUT} = 0A



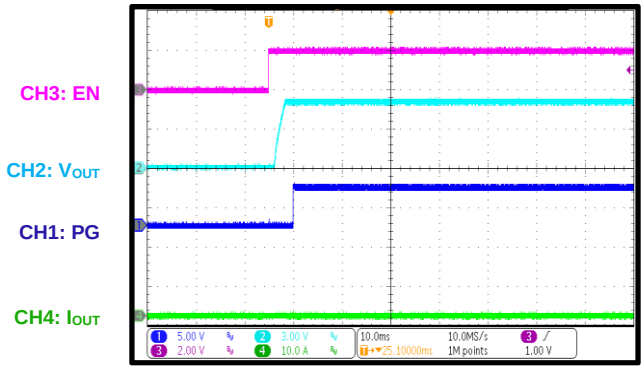
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, dual-phase, L = 0.56µH, f_{SW} = 2.2MHz, AAM mode, T_A = 25°C, unless otherwise noted.

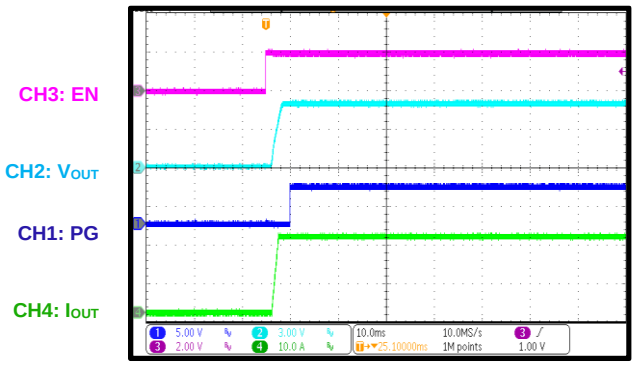
PG in Shutdown through VIN
I_{OUT} = 22A



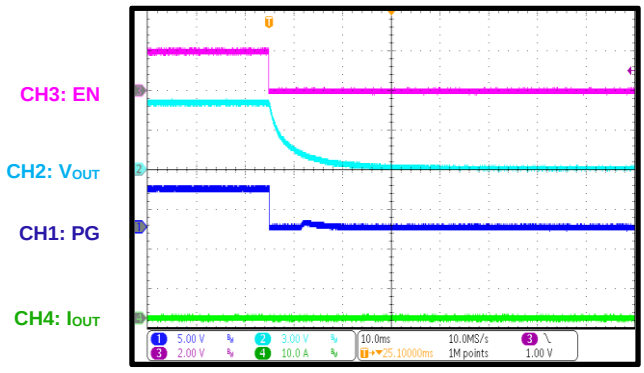
PG in Start-Up through EN
I_{OUT} = 0A



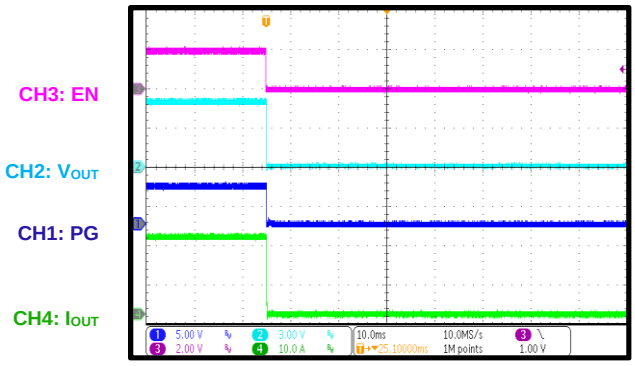
PG in Start-Up through EN
I_{OUT} = 22A



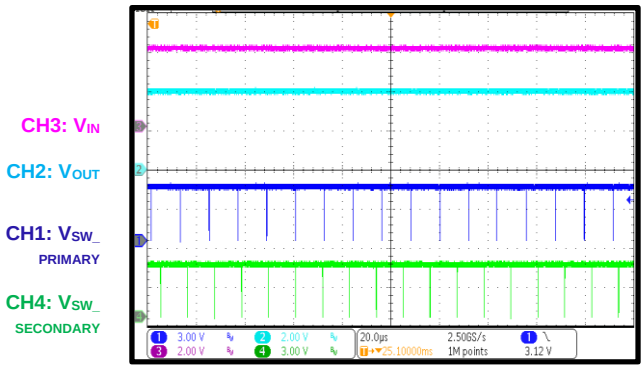
PG in Shutdown through EN
I_{OUT} = 0A



PG in Shutdown through EN
I_{OUT} = 22A



Low-Dropout Mode
V_{IN} = 4V, V_{OUT} set to 5V, I_{OUT} = 0A

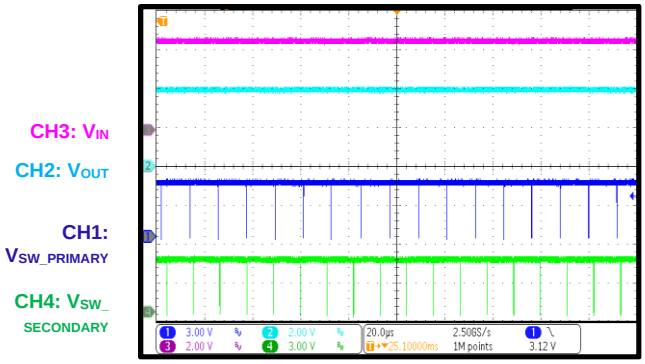


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

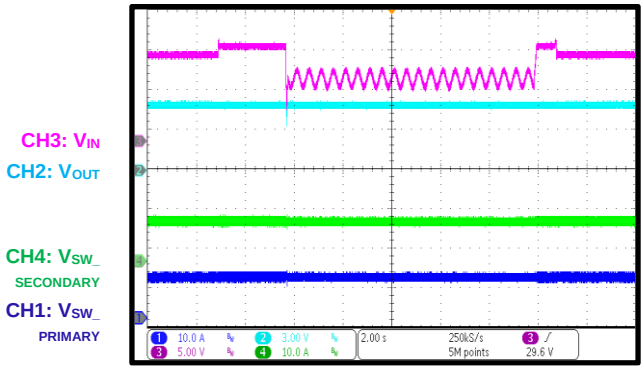
V_{IN} = 12V, V_{OUT} = 5V, dual-phase, L = 0.56µH, f_{SW} = 2.2MHz, AAM mode, T_A = 25°C, unless otherwise noted.

Low-Dropout Mode

V_{IN} = 4V, V_{OUT} set to 5V, I_{OUT} = 22A

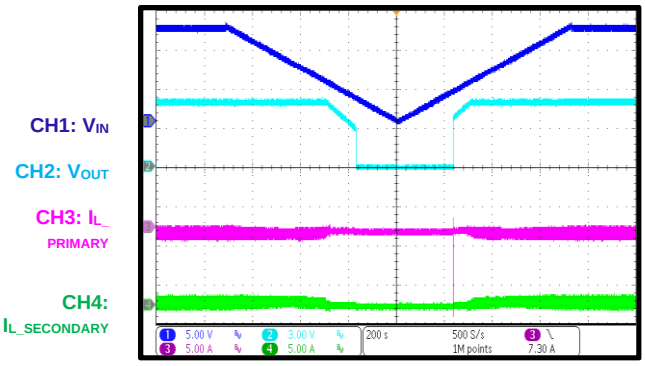


Cold Crank



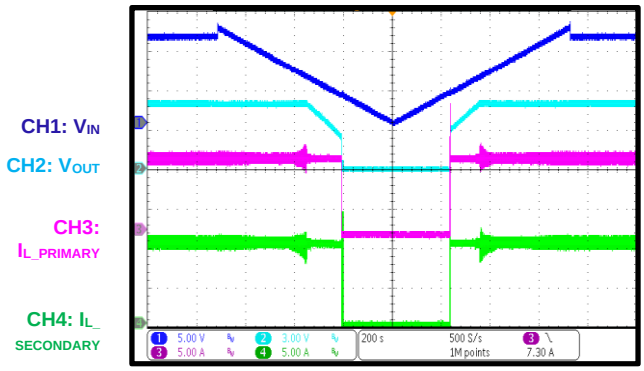
V_{IN} Ramping Down and Up

I_{OUT} = 0A



V_{IN} Ramping Down and Up

I_{OUT} = 22A



FUNCTIONAL BLOCK DIAGRAM

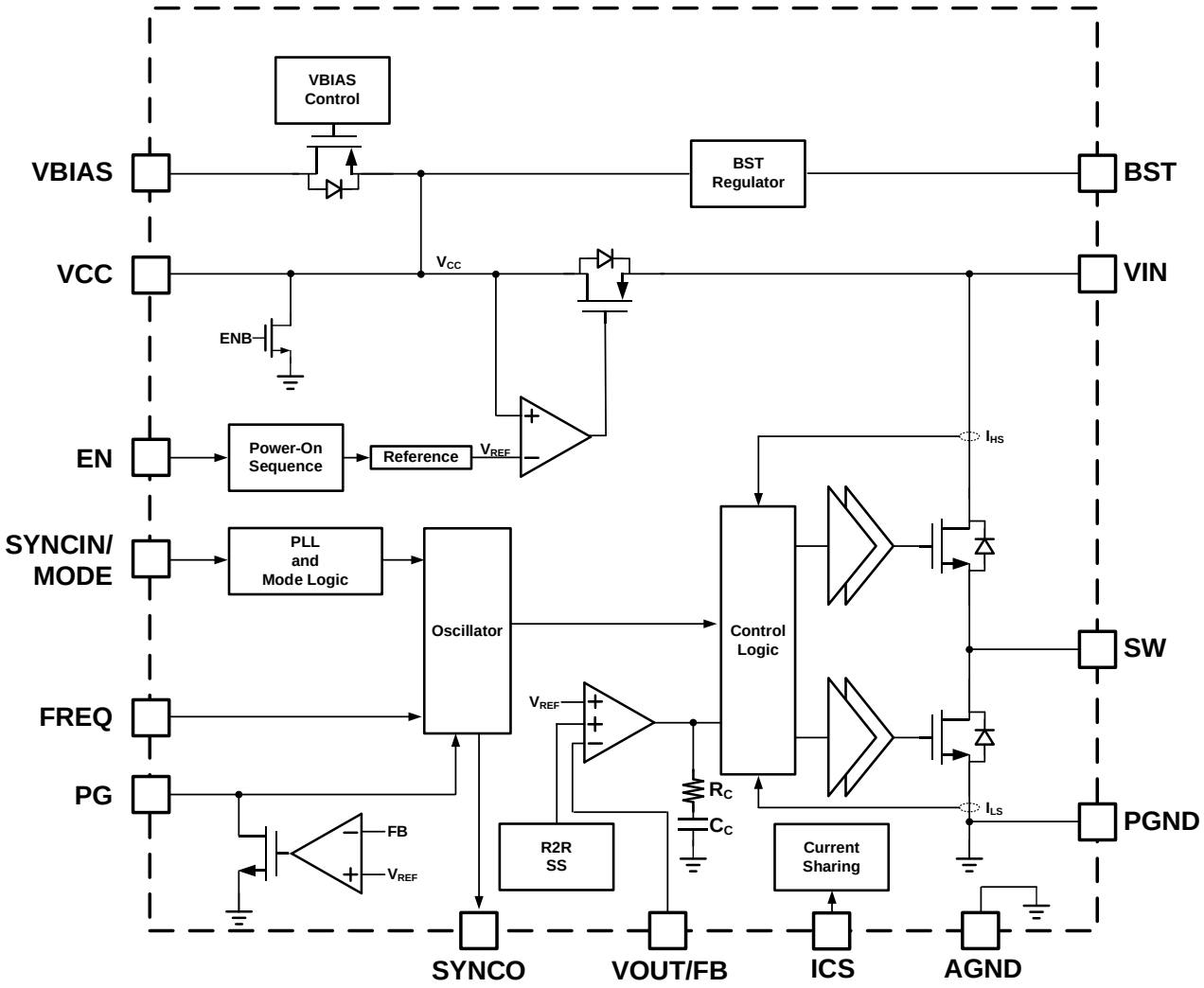


Figure 1: Functional Block Diagram for the Adjustable-Output Version

FUNCTIONAL BLOCK DIAGRAM *(continued)*

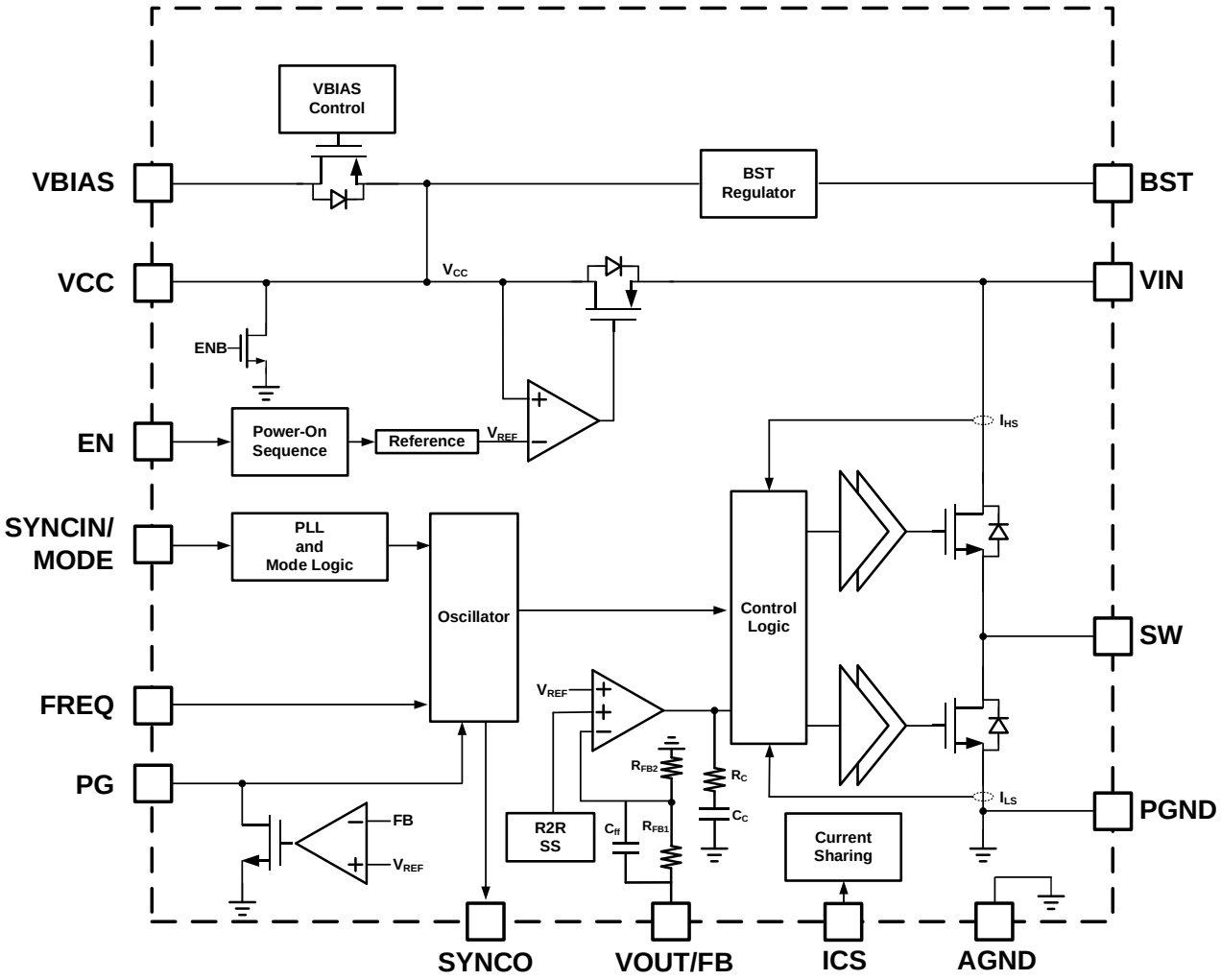


Figure 2: Functional Block Diagram for the Fixed-Output Version

TIMING SEQUENCE DIAGRAM

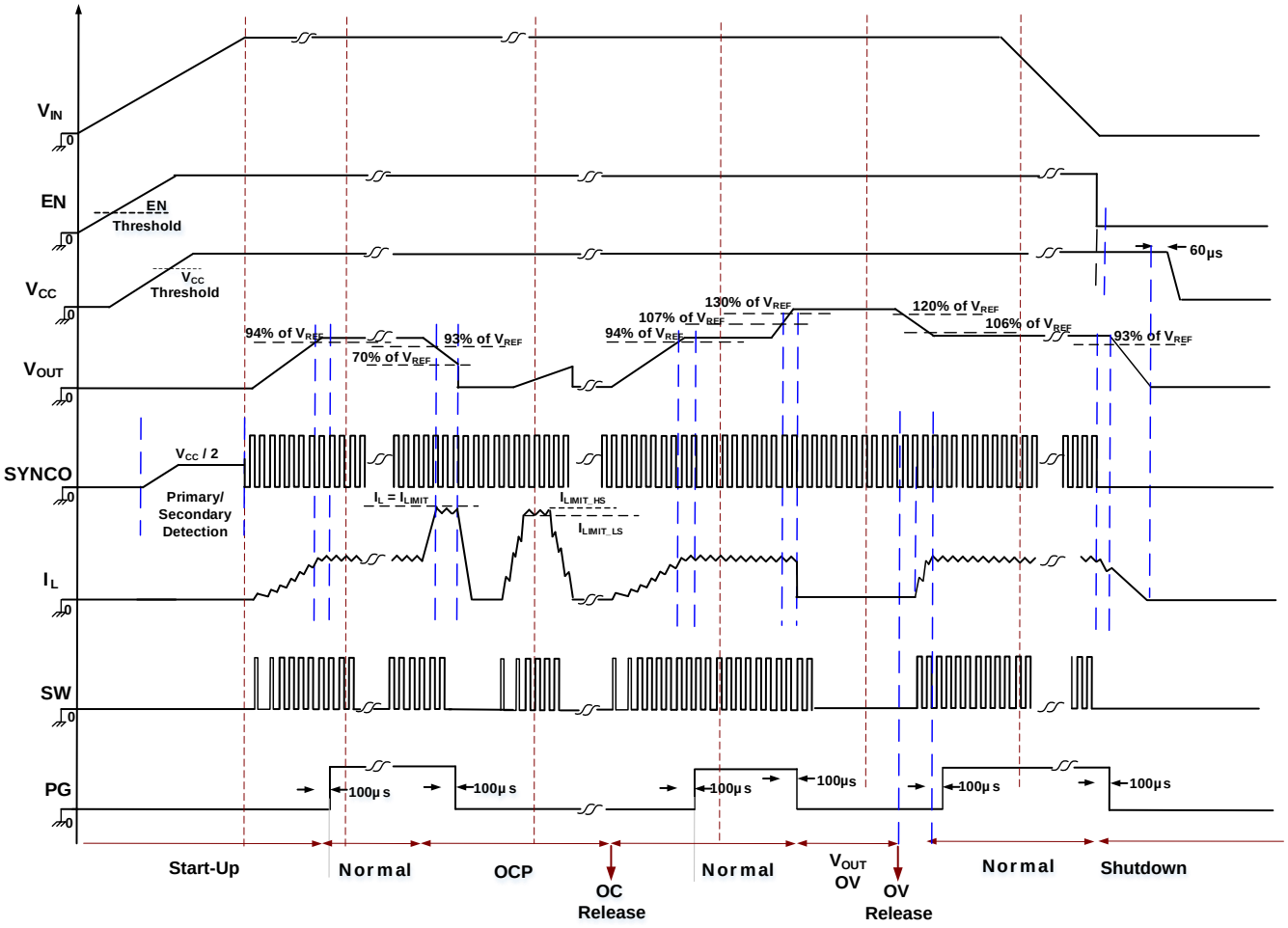


Figure 3: Timing Sequence Diagram

OPERATION

The MPQ4372 family of buck converters are configurable-frequency (200kHz to 2.5MHz), synchronous, step-down switching regulators with integrated low on-resistance HS-FETs and LS-FETs. The family covers a 6A to 11A output current (I_{OUT}) range and employs zero-delay pulse-width modulation (PWM) (ZDP™) control, an MPS-exclusive technology that delivers fast transient response while reducing external capacitor count. In addition, it maintains the fixed switching frequency (f_{SW}), and its low operational quiescent current (I_Q) makes this device well-suited for battery-powered applications.

Zero-Delay PWM (ZDP™) Control

Automotive applications generally require fixed-frequency operation to reduce EMI concerns, but traditional topologies with fixed-frequency control have major limitations. For example, voltage mode is difficult to compensate in automotive environments, while peak current mode control struggles to keep up with stringent modern system-on-chip (SoC) transient requirements without excessive output capacitance. With these requirements in mind, the MPQ4372 features fixed-frequency ZDP™ control.

ZDP™ control combines current information with the hysteretic-style output voltage (V_{OUT}) control in a clocked system. This provides optimal transient response while maintaining a high phase margin across a wide variety of operating conditions and external component values. This control maintains superior EMI performance. The improved transient response reduces output capacitor requirements and lowers system cost. Trailing edge modulation facilitates a narrow minimum on time for high conversion ratio applications.

At the beginning of the PWM cycle, the high-side MOSFET (HS-FET) turns off, and the low-side MOSFET (LS-FET) turns on immediately until the control signal reaches the COMP voltage (V_{COMP}). The HS-FET remains off for at least 80ns at the beginning of the cycle.

Light-Load Operation

Under light-load conditions, the MPQ4372 can operate in two different operation modes by setting the state of the SYNCIN/MODE pin.

The MPQ4372 works in forced continuous conduction mode (FCCM) when the SYNCIN/MODE pin is pulled above 1.4V or an external clock is used. In FCCM, the MPQ4372 works with a fixed frequency from the no-load to full-load range. The MPQ4372 has a reverse current limit to prevent the negative current from dropping too low and damaging the components. Once the negative inductor current (I_L) reaches the reverse current limit, the HS-FET immediately turns on, and the LS-FET turns off. The advantages of FCCM are its constant frequency and lower V_{OUT} ripple at light loads. FCCM also has a better response to sudden load changes.

The MPQ4372 works in advanced asynchronous modulation (AAM) mode when the SYNCIN/MODE pin is pulled below 0.4V. AAM mode cannot be entered until soft start (SS) has completed. AAM mode optimizes efficiency under light-load and no-load conditions.

In AAM mode, the LS-FET emulates a diode and the HS-FET has a fixed one-shot on-time to charge the inductor and regulate the output. As the load decreases, the interval between each one-shot increases. When this interval is longer than 8µs, the MPQ4372 enters sleep mode, which turns off some internal circuits and extends the on time to achieve an ultra-low I_Q. When the load increases and the interval becomes shorter than 6µs, the device exits sleep mode and re-enters AAM mode. The part can exit AAM mode immediately if the SYNCIN/MODE pin goes high. If a fault occurs (e.g. over-current [OC], over-temperature [OT]), then the MPQ4372 does not disable the internal circuits in sleep mode.

Start-Up and Shutdown

If both the input voltage (V_{IN}) and EN exceed their appropriate thresholds, the chip starts up. The reference block starts first, generating a stable reference voltage (V_{REF}) and currents, and then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuitries.

While the internal supply rail is up, an internal timer holds the HS-FET and LS-FET off for about 100µs to blank any start-up glitches. When the

SS block is enabled, it first holds its SS output low to ensure that the remaining circuits are ready, then slowly ramps up.

Four events can shut down the chip: EN going low, V_{IN} going low, thermal shutdown, and V_{IN} over-voltage (OV) shutdown. During the shutdown procedure, the signaling path is blocked first to avoid any fault triggering, then V_{COMP} and the internal supply rail are pulled down. The floating driver is not subject to this shutdown command, but its charging path is disabled.

Error Amplifier (EA)

The error amplifier (EA) compares the FB pin's voltage (V_{FB}) with the internal V_{REF} (0.6V). The EA's output is then compared to V_{FB} again. The output of this comparator is compared to the current information to control the power MOSFET's duty cycle.

Low-Dropout (LDO) Mode

When V_{IN} drops close to V_{OUT} and the device detects the minimum off time (100ns) that the HS-FET is using, the MPQ4372 is in low-dropout mode. The MPQ4372 reduces f_{SW} to achieve a high duty cycle. When f_{SW} drops to about 100kHz, the minimum off time is about 50ns to achieve a higher duty cycle. During SS, the MPQ4372 only enters low-dropout mode after 60% of the SS time (t_{SS}) has elapsed.

The effective duty cycle during the regulator's dropout period is mainly influenced by the voltage drop across the power MOSFET, the inductor's resistance, and the PCB resistance.

Frequency Spread Spectrum (FSS)

The MPQ4372 uses dual spread spectrum modulation. First, the MPQ4372 has a 15kHz modulating frequency (f_{MOD1}) with ≤128 steps and a triangular profile to spread the internal oscillator frequency across a ±6.2% window. The number of steps varies with the configured oscillator frequency so that the exact same f_{SW} steps cycle by cycle.

A second modulating frequency (f_{MOD2}) of 120kHz varies the oscillator frequency across a ±2.5% window with a maximum of 16 steps. This higher modulating frequency improves the effect of FSS across the high-frequency EMI measurements, where the resolution bandwidth (RBW) is 120kHz (see Figure 4).

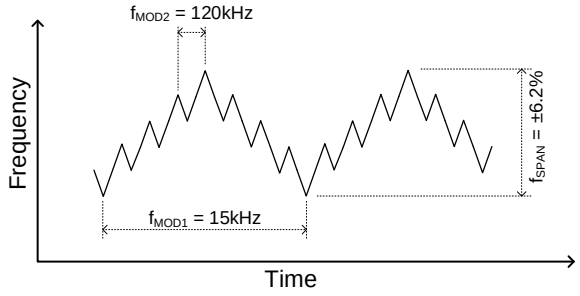


Figure 4: FSS

The emission power of the fundamental f_{SW} and its harmonics is distributed into smaller pieces by creating side-bands when modulating f_{SW} with the triangle modulation waveform. This significantly reduces the amplitude of individual EMI spikes (also called spurs).

Soft Start (SS)

The MPQ4372 has an internal SS implemented to prevent the converter's V_{OUT} from overshooting during start-up. The default t_{SS} is 4ms.

Pre-Biased Start-Up

When the MPQ4372 starts up and V_{FB} is <100% of its target, the part enters SS.

If V_{FB} is between 100% and 130% of its target at start-up while in FCCM, this means that the output has a pre-biased voltage. Neither the HS-FET nor LS-FET turn on until the internal SS process is 80% complete. Then the MPQ4372 starts switching and regulates the output before SS finishes.

If V_{FB} exceeds 130% of its target at start-up, the MPQ4372 starts to slowly discharge the output through the discharging FET on SW. Once V_{FB} reaches 120% of its target, the MPQ4372 starts the internal SS and operates following the pre-biased start-up process, as explained in the previous paragraph.

SYNCIN and SYNCO

f_{SW} can be synchronized to the rising edge of a clock signal applied at the SYNCIN/MODE pin. The recommended SYNCIN frequency range is between 200kHz and 2.5MHz. The SYNCIN frequency should be set to match the internal f_{SW} with a ±10% tolerance.

The SYNCO pin provides a clock signal in phase with the internal oscillator when there is no SYNCIN signal, or a clock signal in phase with SYNCIN. Figure 7 shows when an external clock signal is applied at SYNCIN. This makes it simple to enable a dual-phase interleaving configuration.

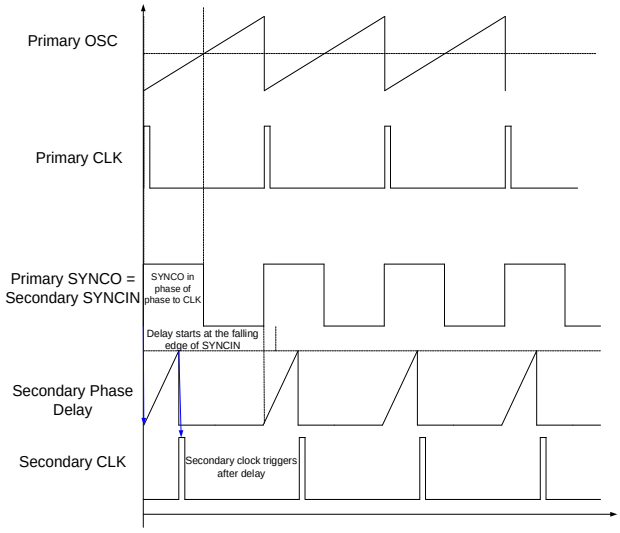


Figure 5: SYNCIN & SYNCO Scheme

Primary/Secondary Selection and Multi-Phase Function

"Primary" and "secondary" are terms are used to describe the role of the different ICs in a multi-phase power converter. The primary device generates a clock signal to which the secondary device is synchronized, and it also asserts PG based on the output regulation.

The device detects the SYNCO pin's status during start-up to configure the primary and secondary selection. The impedance measurement is done by internally biasing the SYNCO pin and comparing the voltage at the pin to a reference. If the SYNCO voltage (V_{SYNCO}) is between (5 / 12 x V_{CC}) and (7 / 12 x V_{CC}), then the part is configured as the primary device. If V_{SYNCO} is <(5 / 12 x V_{CC}) or >(7 / 12 x V_{CC}), then the part is detected as a secondary device. In applications where the mode is changed during operation, use a pull-up or pull-down resistor of ≤4.7kΩ for the secondary devices to ensure proper detection.

To work in a multi-phase topology, The VOUT/FB pins of the devices must be connected together directly or through feedback resistors.

The ICS pins must be connected together, and a local, lower-value capacitor much be placed between each ICS pin and GND.

The primary device's SYNCO pin is connected to the SYNCIN/MODE pins of the secondary devices, which are interleaved. If the primary device's SYNCIN/MODE pin is used for mode selection, the secondary devices' SYNCO pins can be tied to the primary device's SYNCIN/MODE pin; pull SYNCIN/MODE low to select AAM mode, or pull it high for FCCM. If the primary device's SYNCIN/MODE pin is applied with the external clock signal to synchronize the internal oscillator frequency, the SYNCO pins of the secondary devices can only be pulled high or low, and they cannot be connected to the primary device's SYNCN/MODE pin. For multi-phase applications, avoid floating the primary device's SYNCIN/MODE pin, or connect it to GND/VCC through a larger resistor (>20kΩ).

Pull the PG pin to a power source through a resistor or leave it floating if it is not used for the primary device. For secondary devices, connect a resistor to ground on the PG pin to set the phase delay and allow for simple multi-phase operation; Connect PG directly to GND to select no delay on the SYNCIN signal for secondary phase.

Figure 6 shows dual-phase configuration.

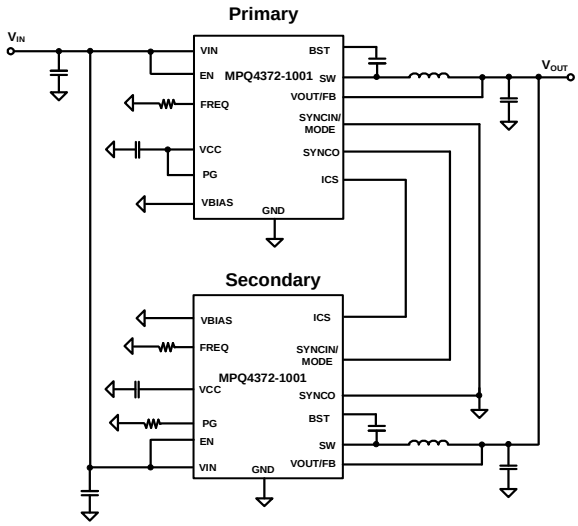


Figure 6: Dual-Phase Configuration

Figure 7 shows 4-phase configuration.

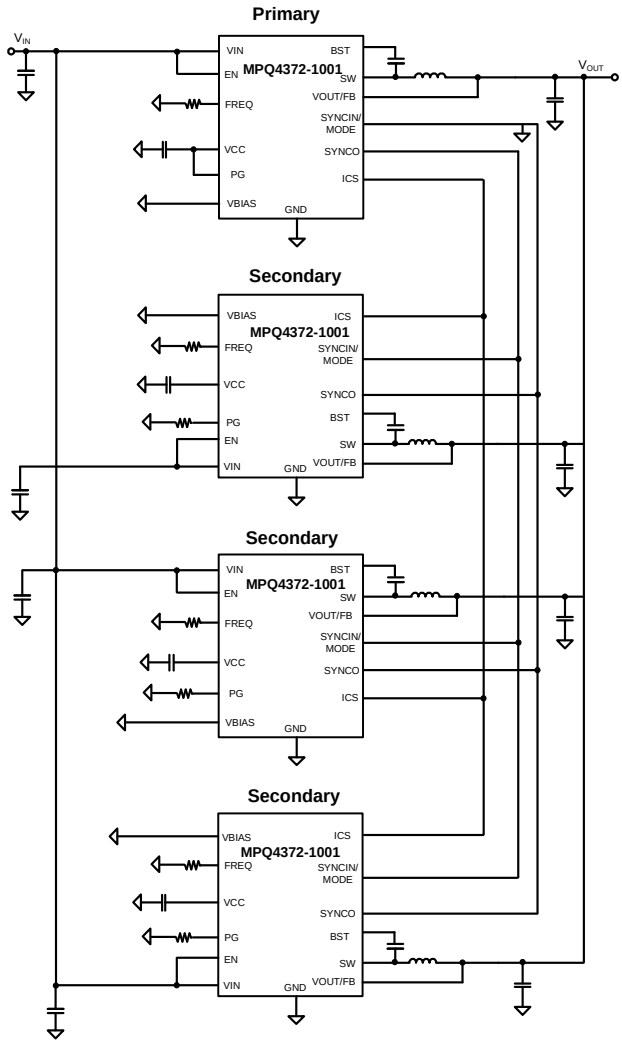


Figure 7: Four-Phase Configuration

Thermal Shutdown

Thermal shutdown is implemented to protect the chip from thermal runaway. If the silicon die temperature exceeds its upper threshold (170°C), the MPQ4372 shuts down the power MOSFETs. Once the temperature falls below the lower threshold (150°C), the chip is enabled again and resumes normal operation.

V_{IN} Over-Voltage Protection (OVP)

If V_{IN} exceeds its OV rising threshold (typically 38V), the MPQ4372 stops switching. Once V_{IN} drops to the OV falling threshold (typically 37V), the device resumes normal regulation and switching. If the MPQ4372 is operating in sleep mode, this OVP function is turned off between the no-switching periods. The V_{IN} OVP function only works during the one-shot HS on time and detects if V_{IN} reaches the OVP threshold.

Peak and Valley Current Limit

Both the HS-FET and LS-FET have cycle-by-cycle current-limit protection. When I_L reaches the high-side (HS) peak current limit (typically 17.2A for a device with a 10A load (MPQ4372-0xxx)) while the HS-FET is on, the HS-FET is forced off immediately to prevent I_L from rising further. If there is an internal clock signal before the peak current limit is reached, the HS-FET also turns off.

When the LS-FET is on, the next clock's rising edge is held until I_L drops below the low-side (LS) valley current limit (typically 12A for a device with a 10A load (MPQ4372-0xxx)). Then I_L can drop to a sufficiently low value when the HS-FET turns on again. This current limit scheme prevents current runaway if an overload or short-circuit event occurs.

Short-Circuit Protection (SCP)

If V_{OUT} drops below 93% of its nominal output and the EA's output is clamped, the MPQ4372 counts the valley current limit counter (LSOC) about 128 times and enters hiccup mode.

If V_{OUT} drops below 70% of its nominal output, the MPQ4372 counts the LSOC about 8 times then enters hiccup mode. The device restarts with a full SS after about 32ms. This hiccup process repeats until the fault is removed.

During the hiccup period, when V_{FB} reaches 80% of the internal reference (V_{REF}), the part enters SCP recovery. In this scenario, the device re-initiates SS, which can prevents large V_{OUT} spikes if the MPQ4372 recovers during the SCP period.

Output Over-Voltage Protection (OVP) and Discharge

If V_{OUT} exceeds 130% of its nominal regulation value, the MPQ4372 stops switching. Then an internal discharge path from SW to GND is activated to discharge V_{OUT}. Once V_{OUT} drops back to 120% of its nominal value, the discharge is disabled. Once V_{OUT} drops below its nominal value, the device resumes switching.

APPLICATION INFORMATION

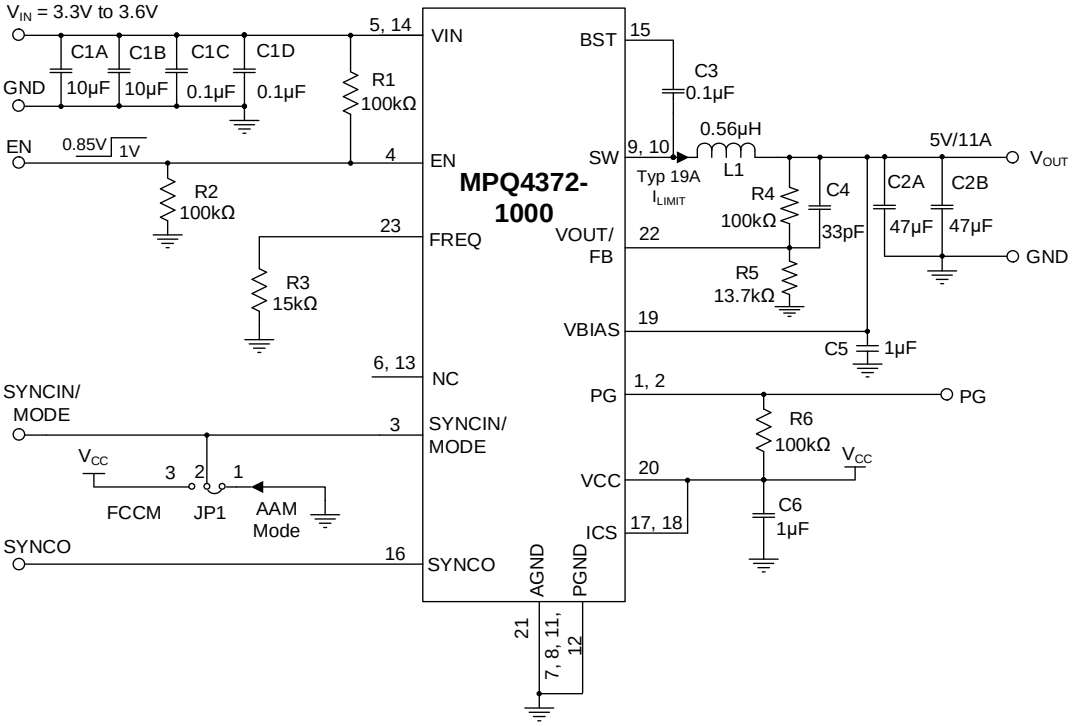


Figure 8: Typical Application Circuit for the MPQ4372-1000 (V_{OUT} = 5V, f_{SW} = 2.2MHz)

Table 1: Design Guide Index and Recommended Values

Pin #	Pin Name	Component	Design Guide Index	Value
1, 2	PG	R6	Power Good (PG) Indication or Phase Shift Setting (PG, Pins 1–2)	100kΩ
3	SYNCIN/ MODE	-	Sync Input and MODE Selection (SYNCIN/MODE, Pin 3)	-
4	EN	R1, R2	Enable and VIN Under-Voltage Lockout (UVLO) (EN, Pin 4)	100kΩ, 100kΩ
5, 14	VIN	C1A, C1B, C1C, C1D	Selecting the Input Capacitors (VIN, Pins 5 and 14)	10µF, 10µF, 0.1µF, 0.1µF
6, 13	NC	N/A	N/A	-
7, 8, 11, 12	PGND	-	GND Connection (PGND, Pins 7–8 and Pins 11–12; AGND, Pin 21)	-
9, 10	SW	L1, C2A, C2B	Selecting the Inductor and Output Capacitors (SW, Pins 9–10)	0.56µH, 47µF, 47µF
15	BST	C3	Floating Driver and Bootstrap Charging (BST, Pin 15)	0.1µF
16	SYNCO	-	Sync Output (SYNCO, Pin 16)	-
17, 18	ICS	-	Current Sharing (ICS, Pins 17–18)	-
19	VBIAS	C5	Internal LDO Supply (VBIAS, Pin 19)	1µF
20	VCC	C6	Internal LDO Supply (VCC, Pin 20)	1µF
21	AGND	-	GND Connection (PGND, Pins 7–8 and Pins 11–12; AGND, Pin 21)	-
22	VOUT/FB	R4, R5, C4	Setting the Feedback (VOUT/FB, Pin 22)	100kΩ, 13.7kΩ, 33pF
23	FREQ	R3	Setting the Switching Frequency (f_{SW}) (FREQ, Pin 23)	15kΩ

Power Good (PG) Indication or Phase Shift Setting (PG, Pins 1–2)

For single-phase applications and for the primary device in multi-phase applications, the PG resistance (R_{PG}, also R6) is recommended to be about 100kΩ. The MPQ4372 has an open-drain PG output that indicates whether the regulator output is within its specific nominal output window. If using PG, connect it to a logic high level power source via a pull-up resistor. PG goes high if V_{OUT} is within 94% to 106% of the nominal voltage; PG goes low if V_{OUT} exceeds 107% or falls below 93% of the nominal voltage. Float PG if it is not used.

When V_{IN} is present and V_{CC} is not present due to EN going low, the PG pin's open-drain N-channel MOSFET becomes unbiased, which causes PG to follow its pull-up source. If the pull-up source is VCC, then VCC asserts low to PG due to VCC being pulled low through its discharge path to GND. If the pull-up source is an external source, then PG follows the external source as soon as V_{CC} discharges below the open-drain N-channel MOSFET's bias value. Once EN pulls high and V_{CC} rises to its regulated 5V, then PG's state is based on the state of V_{OUT}, regardless of the pull-up source. If V_{IN} is not present, then PG always follows its pull-up source.

Table 2 shows the PG state based on different device input values if V_{IN} is present.

Table 2: PG State with V_{IN} Present

Circuit Configuration	EN	VCC	V_{OUT}	PG
PG pull-up to VCC	Low	Off	-	Low
	High	On	Out of Range	Low
	High	On	In Range	High
PG pull-up to ext. source	Low	Off	-	High
	High	On	Out of Range	Low
	High	On	In Range	High

To ensure that PG pulls low after EN shutdown when PG is pulled up to external source, an external circuit is recommended (see Figure 9).

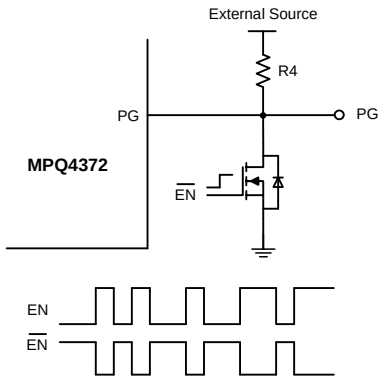


Figure 9: Recommended Circuit for PG Pull-Up to External Source

For secondary devices in multi-phase applications, this pin can set the phase shift by connecting a resistor (R_{PHASE}) to ground. Table 3 shows the relationship between the phase shift and R_{PHASE} under high- and low-frequency conditions.

Table 3: Phase Shift vs. R_{PHASE}

Phase Shift	R_{PHASE} at $f_{SW\_PRIMARY}$ = 410kHz	R_{PHASE} at $f_{SW\_PRIMARY}$ = 2.2MHz
90°	33kΩ	4.87kΩ
120°	46.4kΩ	7.32kΩ
180°	73.2kΩ	12.1kΩ
240°	97.6kΩ	16.9kΩ
270°	115kΩ	19.1kΩ
359°	150kΩ	26.1kΩ

Sync Input and MODE Selection (SYNCIN/MODE, Pin 3)

For single-phase applications and primary devices in multi-phase applications, when this pin is used as the sync input pin, f_{SW} can be synchronized to the rising edge of a clock signal applied at the SYNCIN/MODE pin. The recommended SYNCIN frequency range is between 90% and 110% of the set f_{SW}. When this pin is used for mode selection, pull this pin high so that the MPQ4372 operates in FCCM; pull this pin low or float this pin for AAM mode. Table 4 shows the detailed mode selection.

Table 4: Mode Selection

SYNCIN/MODE Input	Operation
Floating	AAM mode
<0.4V	AAM mode
>1.4V	FCCM
External clock in	FCCM

For secondary devices in multi-phase applications, it is recommended to connect the SYNCIN/MODE pin of the secondary devices to the primary device's SYNCO pin. In this scenario, keep the primary device's SYNCO pin at a high impedance.

Enable and V_{IN} Under-Voltage Lockout (EN, Pin 4)

EN is a digital control pin that turns the regulator on and off.

Enabled by External Logic High/Low (H/L) Signal

When the EN voltage reaches about 0.7V, the VCC supply turns on. When V_{IN} exceeds about 2.7V, then V_{IN} provides an accurate reference voltage for the EN threshold. Forcing EN to exceed its rising voltage threshold of 1V turns on the device. The device is turned off by driving EN below 0.85V.

Configurable V_{IN} UVLO

When V_{IN} is sufficiently high, the chip can be enabled and disabled by the EN pin. The EN pin can generate a configurable V_{IN} UVLO threshold and hysteresis.

The MPQ4372 has an internal, fixed UVLO threshold. The rising threshold is 3.8V, while the falling threshold is about 2.9V. For applications that need a higher UVLO point, an external resistor divider can be placed between VIN and EN to achieve a higher equivalent UVLO threshold (see Figure 10).

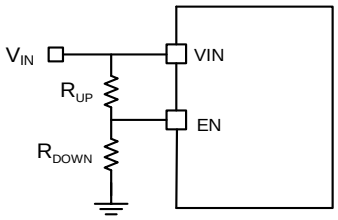


Figure 10: Adjustable UVLO Using EN Divider

The UVLO rising and falling thresholds ($V_{IN\_UV\_RISING}$ and $V_{IN\_UV\_FALLING}$, respectively) can be calculated with Equation (1) and Equation (2), respectively:

$$VIN_{UV\_RISING} = (1+\frac{R_{UP}}{R_{DOWN}}) \times V_{EN\_RISING} \quad (1)$$

$$VIN_{UV\_FALLING} = (1+\frac{R_{UP}}{R_{DOWN}}) \times V_{EN\_FALLING} \quad (2)$$

Where V_{EN_RISING} is 1V, and $V_{EN\_FALLING}$ is 0.85V.

Selecting the Input Capacitors (VIN, Pins 5 and 14)

The step-down converters have a discontinuous input current, and require a capacitor to supply AC current to the converters while maintaining the DC input voltage. For the best performance, use low-ESR capacitors. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients.

For most applications, use a 4.7µF to 10µF capacitor. It is strongly recommended to use another, lower-value capacitor (e.g. 0.1µF) with a small package size (0603) to absorb high-frequency switching noise. Place this capacitor as close to VIN and GND as possible.

Since C_{IN} absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor (I_{CIN}) can be estimated with Equation (3):

$$I_{CIN} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1-\frac{V_{OUT}}{V_{IN}})} \quad (3)$$

The worst-case condition occurs at V_{IN} = 2 x V_{OUT}, calculated with Equation (4):

$$I_{CIN} = \frac{I_{LOAD}}{2} \quad (4)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, add a small, high-quality ceramic capacitor (e.g. 0.1µF) as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide a sufficient charge to prevent excessive voltage ripple at the input. The input voltage ripple (ΔV_{IN}) caused by the capacitance can be estimated with Equation (5):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1-\frac{V_{OUT}}{V_{IN}}) \quad (5)$$

Selecting the Inductor and Output Capacitors (SW, Pins 9–10)

Selecting the Inductor

A 0.1µH to 10µH inductor with a DC current rating at least 25% higher than the maximum load current is recommended for most applications. For higher efficiency, choose an inductor with a lower DC resistance. A larger-value inductor results in less ripple current and a lower output voltage ripple, but also has a larger physical size, higher series resistance, and lower saturation current. A good rule to determine the inductance is to allow the inductor ripple current to be approximately 30% of the maximum load current. The inductance (L) can be calculated with Equation (6):

$$L = \frac{V_{OUT}}{f_{sw} x \Delta I_L} x (1 - \frac{V_{OUT}}{V_{IN}}) \quad (6)$$

Where ΔI_L is the peak-to-peak inductor ripple current.

Choose the inductor ripple current to be approximately 30% of the maximum load current. The maximum inductor peak current (I_{LP}) can be calculated with Equation (7):

$$I_{LP} = I_{LOAD} + \frac{V_{OUT}}{2 x f_{sw} x L} x (1 - \frac{V_{OUT}}{V_{IN}}) \quad (7)$$

Selecting the Output Capacitor

The output capacitor maintains the DC V_{OUT}. Use ceramic, tantalum, or low-ESR electrolytic capacitors. For the best results, use low-ESR capacitors to keep the V_{OUT} ripple low. The V_{OUT} ripple (ΔV_{OUT}) can be estimated with Equation (8):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 f_{SW} \times C_{OUT}}) \quad (8)$$

Where L is the inductance, and R_{ESR} is the output capacitor's equivalent series resistance (ESR).

For ceramic capacitors, the capacitance dominates the impedance at the switching frequency and causes the majority of the output voltage ripple. For simplification, ΔV_{OUT} can be calculated with Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^2 \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (9)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, ΔV_{OUT} can be estimated with Equation (10):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (10)$$

The characteristics of the output capacitor also affect the stability of the regulation system. The part can be optimized for a wide range of capacitance and ESR values.

Floating Driver and Bootstrap Charging (BST, Pin 15)

The BST capacitor (C_{BST}, also called C3) is recommended to be between 0.1µF to 0.47µF.

It is not recommended to place a resistor (R_{BST}) in series with the BST capacitor, as this results in minimal EMI improvement and increases power dissipation. The MPQ4372 employs a sophisticated FET turn-on technique that greatly reduces the high-frequency EMI and eliminates the need for this resistor. If R_{BST} is necessary, it should be below 20Ω.

The voltage between BST and SW (V_{BST-SW}) is regulated to about 5V by the dedicated internal bootstrap regulator. When $V_{BOOT-SW}$ is below its regulation value, an N-channel MOSFET (NMOS) pass transistor connected from VCC to BST is turned on to charge C_{BST}. When the HS-FET is on, the BST voltage exceeds V_{CC}, which means that the bootstrap capacitor cannot be charged.

Under conditions with higher duty cycles, the time available for bootstrap charging is shorter, so the bootstrap capacitor may not be charged sufficiently. External circuitry can be used to ensure that the bootstrap voltage remains in the normal operation region.

If the bootstrap voltage reaches its under-voltage lockout (UVLO) threshold, the HS-FET turns off, and the LS-FET turns on with a minimum off time to refresh the bootstrap voltage with the set f_{SW}.

The BST refresh function can only be triggered during the start-up period, sleep mode, or if the feedback over-voltage (OV) condition is triggered.

Sync Output (SYNCO, Pin 16)

For single-phase applications and for the primary device in multi-phase applications, the SYNCO pin outputs a clock signal in phase with the internal oscillator signal or external SYNCIN clock.

For secondary devices in multi-phase applications, this pin can be connected to the SYNCIN/MODE pin of the primary device, or it can be pulled low or high to select AAM mode or FCCM, respectively. The mode setting threshold is same as the selections for the SYNCIN/MODE pin (see Table 4).

Current Sharing (ICS, Pins 17–18)

The ICS pin's function is disabled if the voltage of this pin exceeds 2.4V. Connect ICS to VCC to disable this function in single-phase applications.

In multi-phase applications, connect the ICS pins together for each MPQ4372 phase. Connect a small capacitor between the ICS pin and GND to filter the noise disturbance. For high-frequency conditions (e.g. 2.2MHz), it is recommended for the capacitance to be between 22pF and 180pF. For low-frequency conditions (e.g. 410kHz), it is recommended for the capacitance to be between 100pF and 1.2nF.

Internal LDO Supply (VBIAS, Pin 19)

The VBIAS capacitor (C5) is recommended to be 1µF.

The VBIAS pin is the internal LDO's supply pin. When the VBIAS pin is connected to a 5V voltage, VBIAS is the power supply for the VCC regulator. The input supply current can be lower to obtain a higher efficiency. When V_{BIAS} exceeds 4.5V, this pin takes over VCC; when V_{BIAS} is below 4.3V, this function is disabled.

VBIAS can be connected directly to the output voltage when V_{OUT} is between 4.6V to 5.5V to improve the converter's efficiency, especially at high frequencies. Alternatively, connect VBIAS to another 5V rail if one is available in the system, and the current draw is <30mA. Add one decoupling capacitor between the VBIAS pin and GND if this function is used.

When there is no suitable power source for VBIAS, or its function is not used, connect this pin to VOUT or GND. For applications where V_{OUT} > 5.5V, avoid connecting the VBIAS pin to the output. Do not provide an external VBIAS voltage before VIN. Do not float this pin.

Internal LDO Supply (VCC, Pin 20)

The VCC capacitor (C6) is recommended to be 1µF.

The VCC capacitor should be 10 times larger than the BST capacitor. A VCC capacitor exceeding 68µF is not recommended.

The internal circuitry is powered by the internal 5V VCC regulator. This regulator uses VIN as its input and operates across the full V_{IN} range. When V_{IN} exceeds 5V, V_{CC} is in full regulation and maintains a 5V voltage. When V_{IN} is below 5V, the VCC output degrades.

When VCC is powered by VBIAS, V_{CC} follows V_{BIAS}.

Setting the Feedback (VOUT/FB, Pin 22)

For the adjustable-output version, V_{FB} is typically 0.6V. The external resistor divider connected to FB sets the output voltage (see Figure 11).

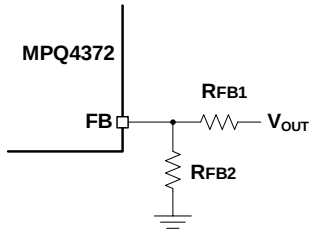


Figure 11: Feedback Divider Network of Adjustable-Output Version

Calculate R_{FB2} with Equation (11):

$$R_{FB2} = \frac{R_{FB1}}{\frac{V_{OUT}}{0.6V} - 1} \quad (11)$$

Table 5 lists the recommended feedback resistor values for common output voltages.

Table 5: Feedback Resistor Selection for Adjustable-Output Version

V_{OUT} (V)	R_{FB1} (kΩ)	R_{FB2} (kΩ)
1.0	66.5 (1%)	100 (1%)
3.3	100 (1%)	22.1 (1%)
5.0	100 (1%)	13.7 (1%)

For the fixed-output version, the FB resistor divider is integrated internally, so connect FB to V_{OUT} directly to set the output voltage (see Figure

12). The following fixed outputs are available: 1V, 1.2V, 1.8V, 2.5V, 3.3V, 3.8V, and 5V.

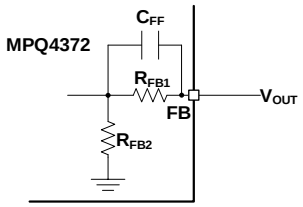


Figure 12: Feedback Divider Network of Fixed-Output Version

Table 6 shows the relationship between the internal R_{FB} and V_{OUT}.

Table 6: R_{FB} vs. V_{OUT} for Fixed Output Version

V_{OUT} (V)	R_{FB2} (MΩ)	R_{FB1} (MΩ)	C_{FF} (pF)
1.0	0.25	0.166	2.0
1.2	0.25	0.25	2.0
1.8	0.25	0.5	2.0
2.5	0.25	0.791	2.0
3.3	0.25	1.125	2.0
3.8	0.25	1.333	2.0
5.0	0.25	1.833	2.0

Setting the Switching Frequency Setting (f_{SW}) (FREQ, Pin 23)

A resistor (R3, also called R_{FREQ}) can be used to f_{SW}. Table 7 shows the R_{FREQ} values to set the adjustable f_{SW}.

Table 7: R_{FREQ} vs. f_{SW}

R_{FREQ} (kΩ)	f_{SW} (kHz)
13	2500
14.3	2330
15	2200
15.8	2100
18.7	1800
22.6	1520
27.4	1270
32.4	1100
41.2	870
51.1	710
71.5	520
88.7	410
100	370
130	285
191	200

GND Connection (PGND, Pins 7–8 and Pins 11–12; AGND, Pin 21)

See the PCB Layout Guidelines section on page 75 for more details.

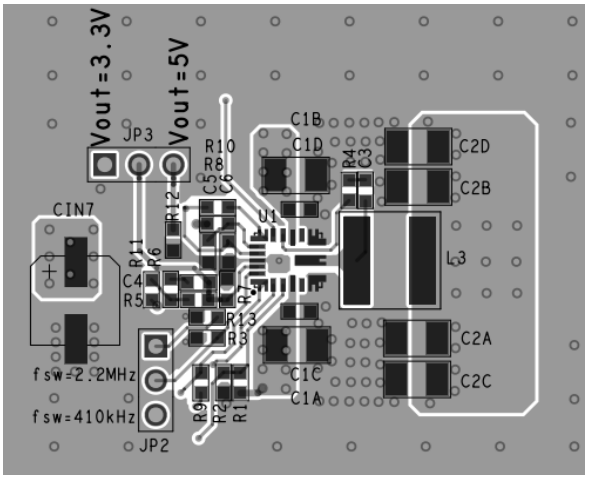
PCB Layout Guidelines [15]

Efficient PCB layout, especially for input capacitor placement, is critical for stable operation. A 4-layer layout is strongly recommended to achieve better thermal performance. For best results, refer to Figure 13 and follow the guidelines below:

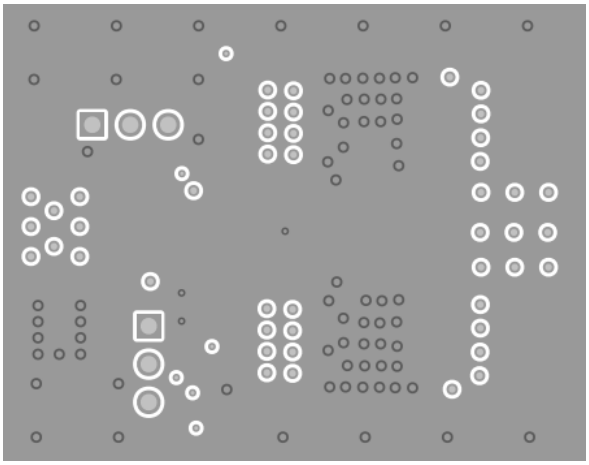
1. Place the symmetric input capacitors as close to VIN and GND as possible.
2. Use a large ground plane to connect directly to PGND.
3. Add vias near PGND if the bottom layer is a ground plane.
4. Ensure that the high-current paths at GND and VIN have short, direct, and wide traces. Place the ceramic input capacitor, especially the small package size (0603) input bypass capacitor, as close to VIN and PGND as possible to minimize high-frequency noise.
5. Keep the connection of the input capacitor and VIN as short and wide as possible.
6. Place the VCC capacitor as close to VCC and GND as possible.
7. Route SW and BST away from sensitive analog areas, such as FB.
8. Use multiple vias to connect the power planes to the internal layers.

Note:

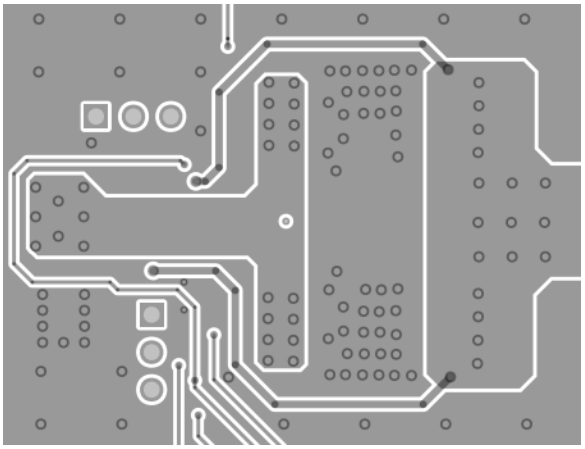
15) The recommended PCB layout is based on Figure 14 on page 76.



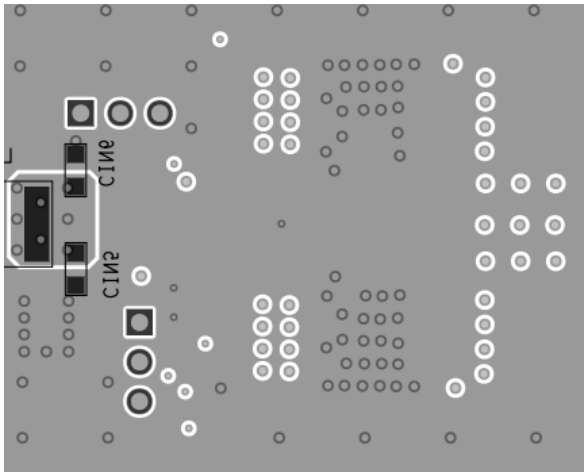
Top Layer



Mid-Layer 1



Mid-Layer 2



Bottom Layer

Figure 13: Recommended PCB Layout

TYPICAL APPLICATION CIRCUITS

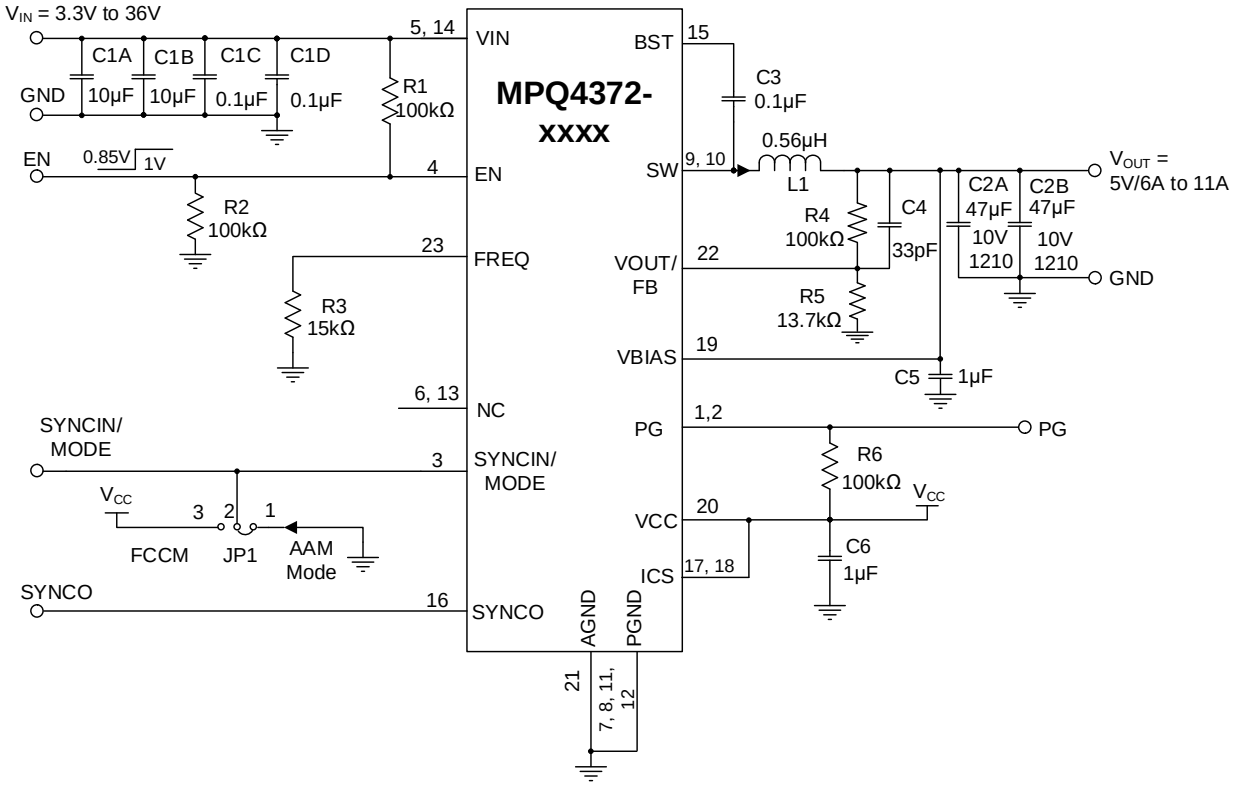


Figure 14: Typical Application Circuit (Single-Phase, V_{OUT} Adjustable for the MPQ4372-xxxx, V_{OUT} = 5V, f_{SW} = 2.2MHz)

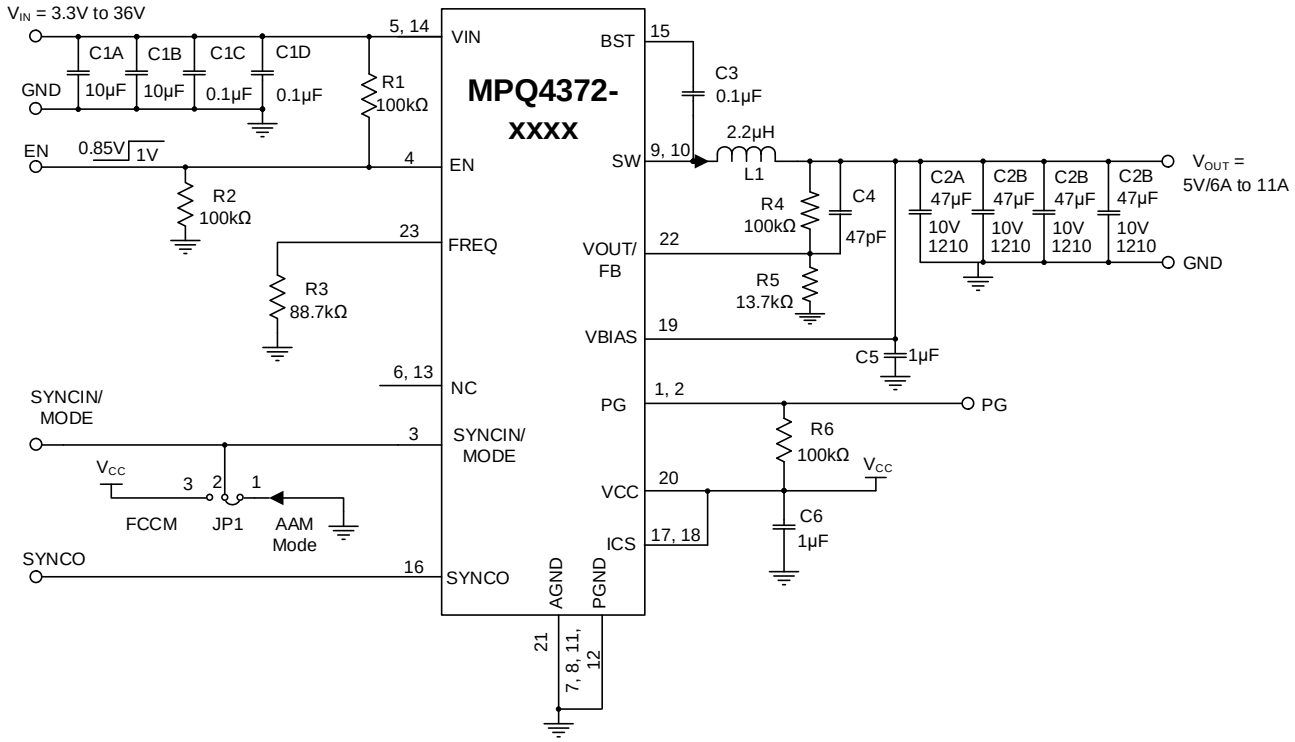


Figure 15: Typical Application Circuit (Single-Phase, V_{OUT} Adjustable for the MPQ4372-xxxx, V_{OUT} = 5V, f_{SW} = 410kHz)

TYPICAL APPLICATION CIRCUITS *(continued)*

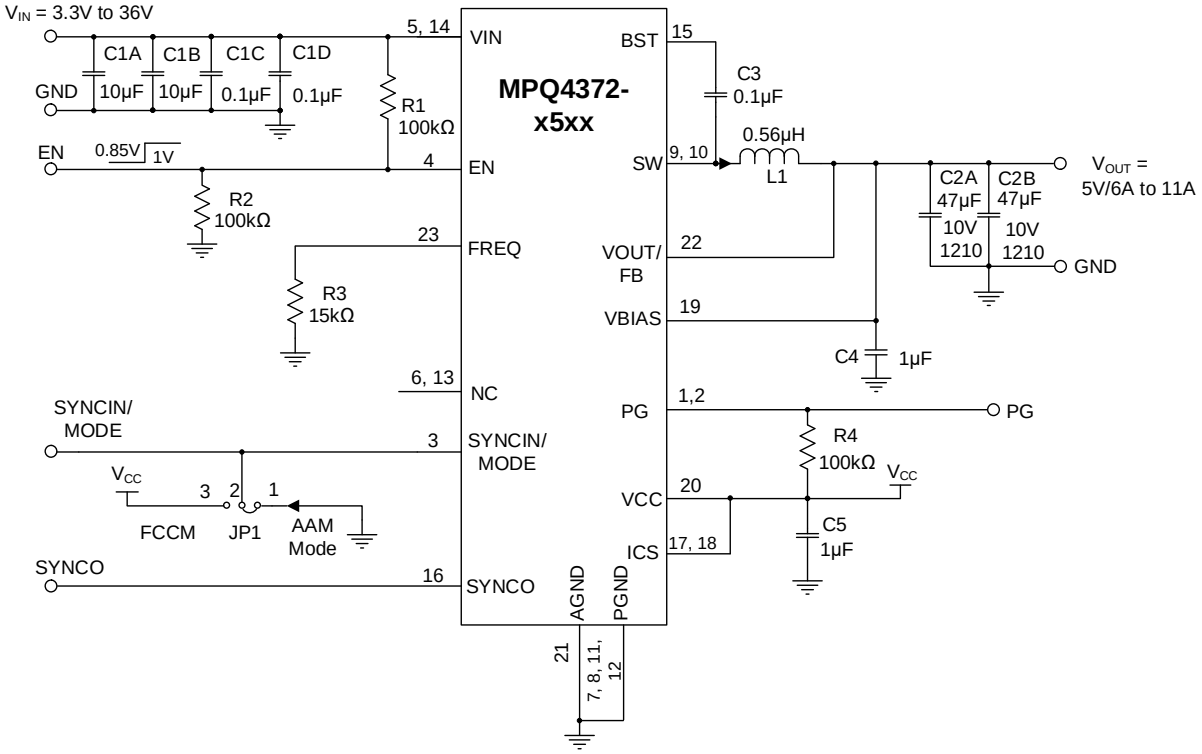


Figure 16: Typical Application Circuit (Single-Phase, 5V Fixed V_{OUT} for the MPQ4372-x5xx, f_{SW} = 2.2MHz)

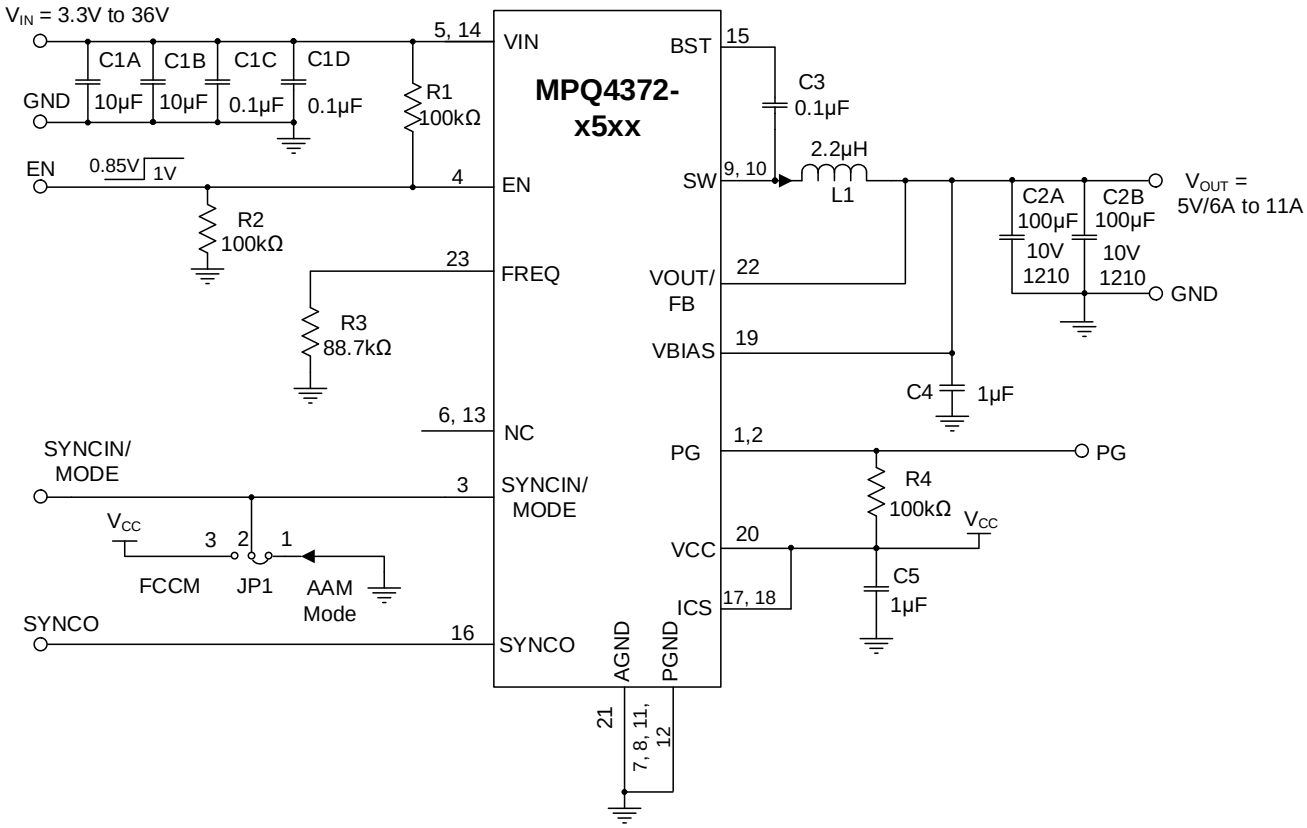


Figure 17: Typical Application Circuit (Single-Phase, 5V Fixed V_{OUT} for the MPQ4372-x5xx, f_{SW} = 410kHz)

TYPICAL APPLICATION CIRCUITS *(continued)*

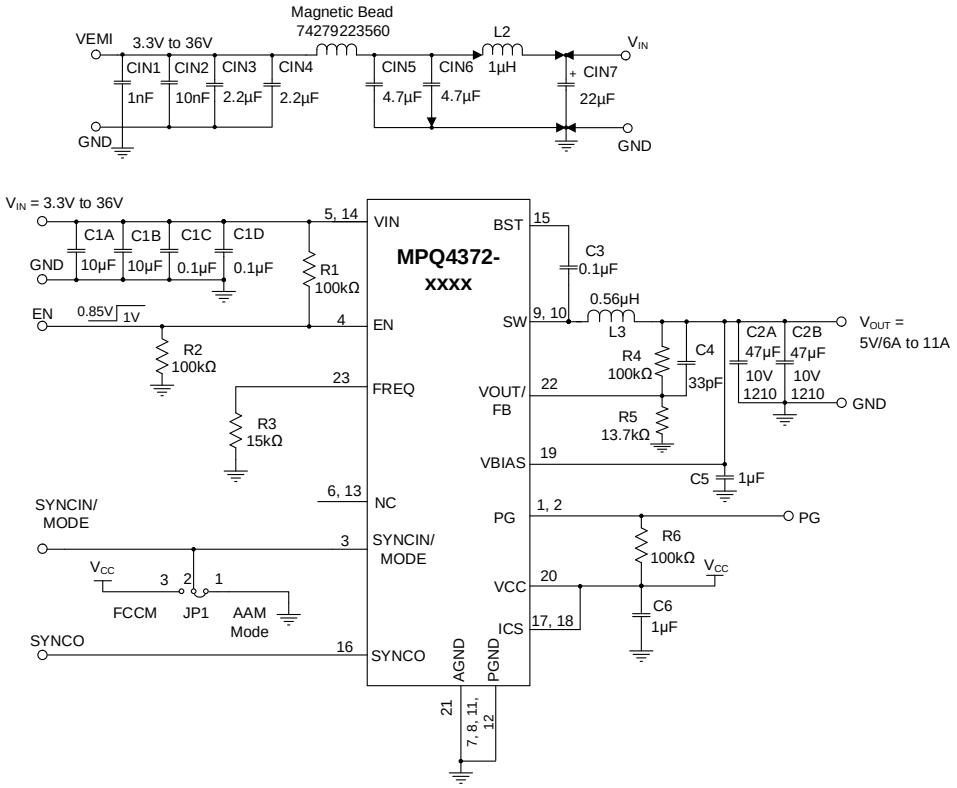


Figure 18: Typical Application Circuit (Single-Phase, V_{OUT} Adjustable for the MPQ4372-xxxx, V_{OUT} = 5V, f_{SW} = 2.2MHz with EMI Filter)

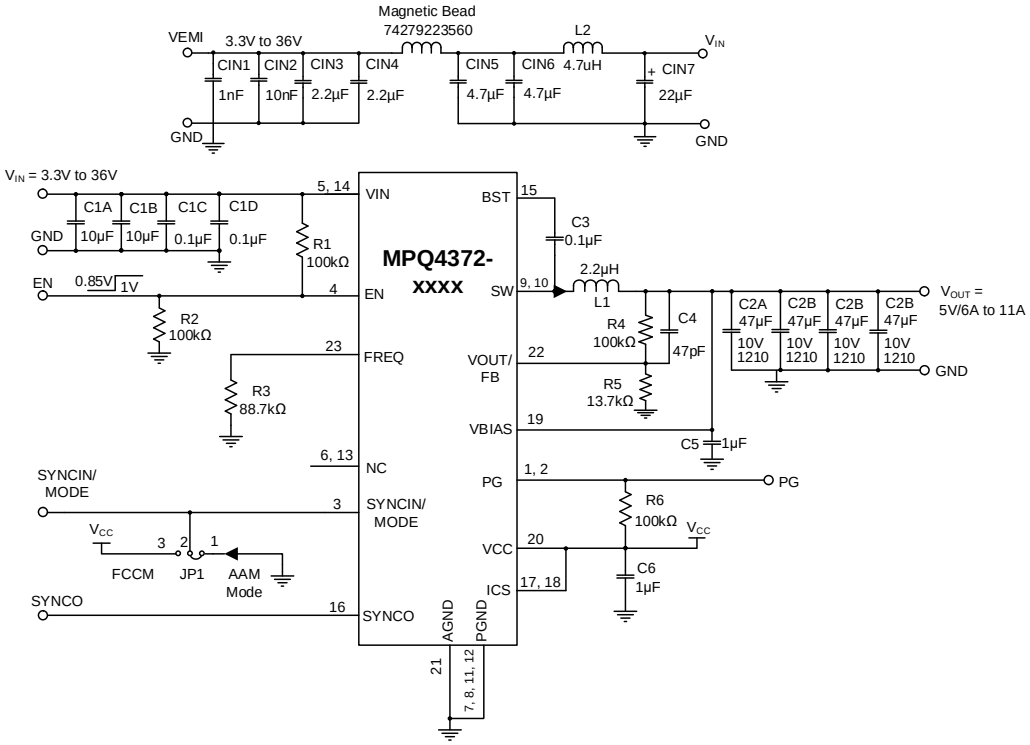


Figure 19: Typical Application Circuit (Single-Phase, V_{OUT} Adjustable for the MPQ4372-xxxx, V_{OUT} = 5V, f_{SW} = 410kHz with EMI Filter)

TYPICAL APPLICATION CIRCUITS (*continued*)

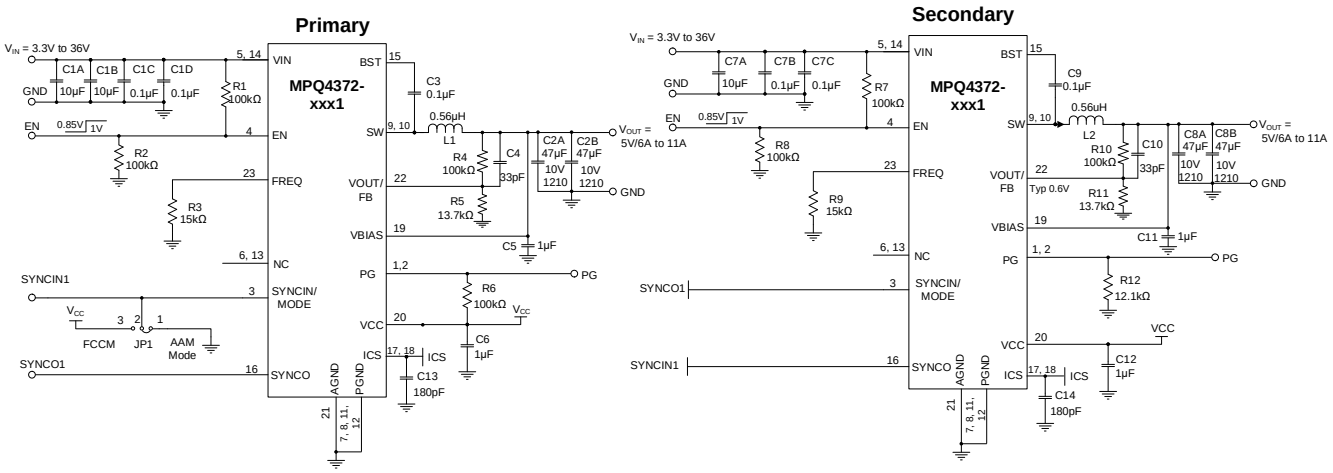


Figure 20: Typical Application Circuit (Dual-Phase, V_{OUT} Adjustable for the MPQ4372-xxx1, V_{OUT} = 5V, f_{SW} = 2.2MHz)

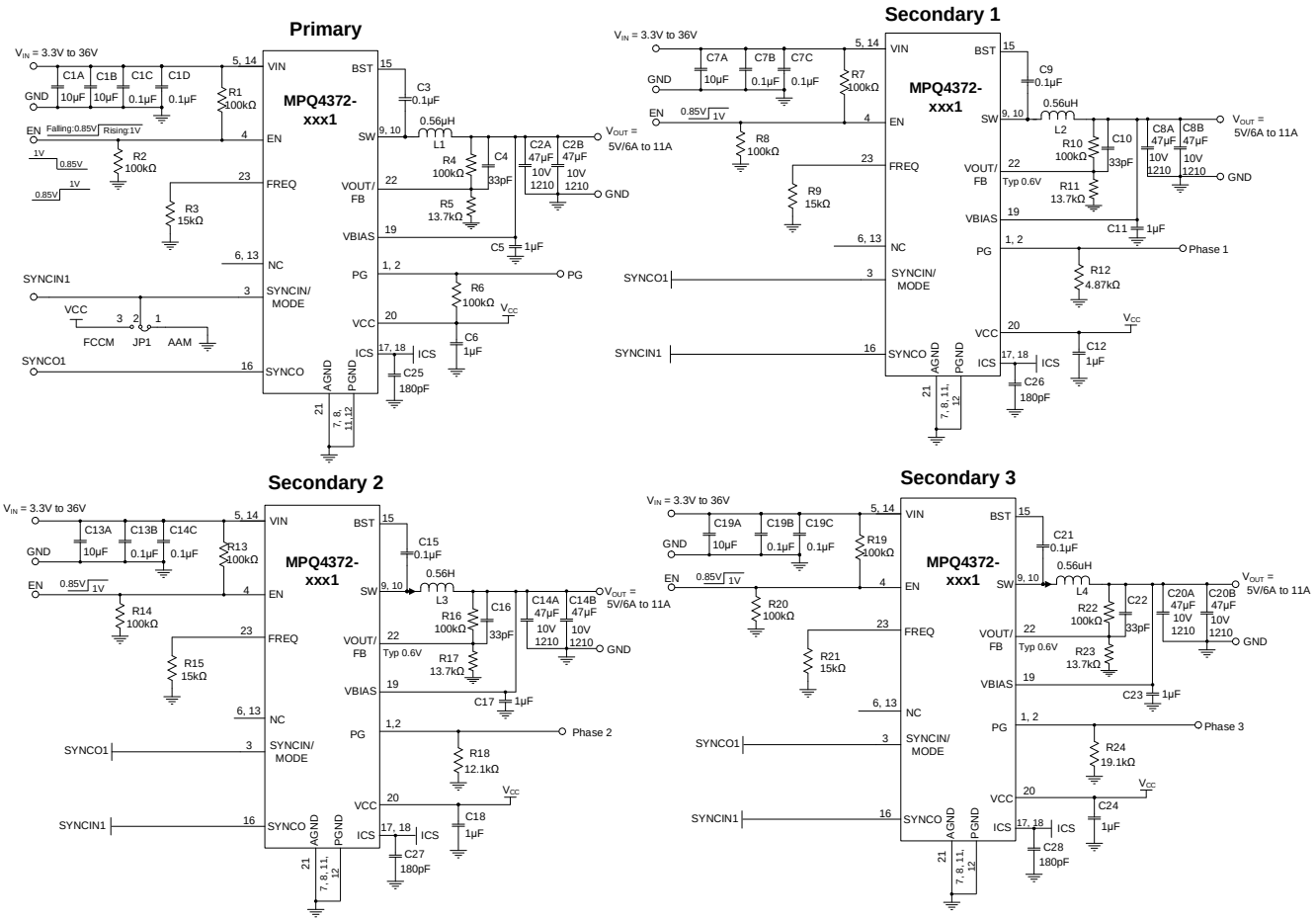


Figure 21: Typical Application Circuit (Four-Phase, V_{OUT} = 5V for the MPQ4372-xxx1, f_{SW} = 2.2MHz)

TYPICAL APPLICATION CIRCUITS *(continued)*

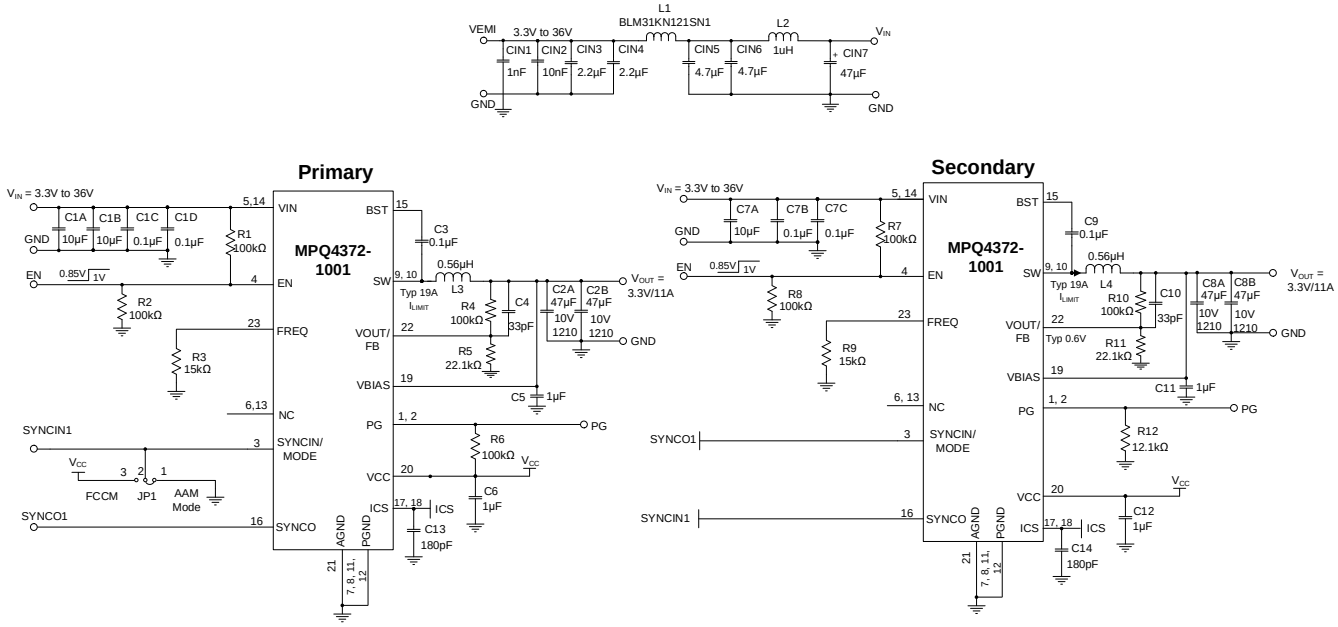
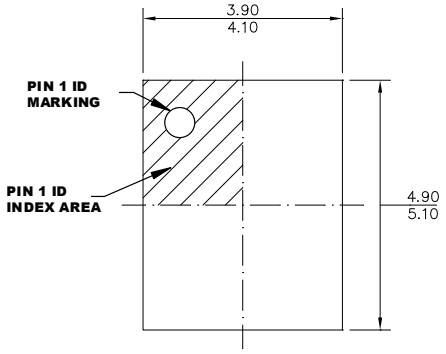


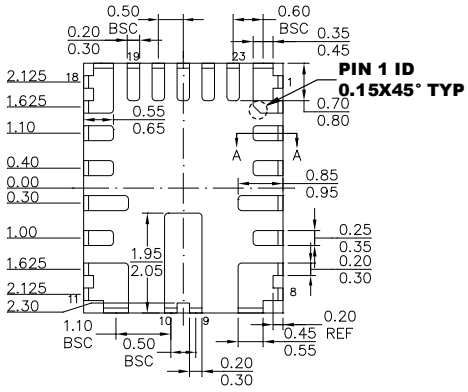
Figure 22: Typical Application Circuit (Dual-Phase, V_{OUT} Adjustable for the MPQ4372-1001, V_{OUT} = 3.3V, f_{SW} = 2.2MHz，I_{OUT} = 22A with EMI Filter)

PACKAGE INFORMATION

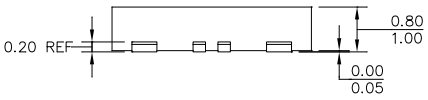
QFN-23 (4mmx5mm)



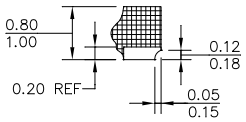
TOP VIEW



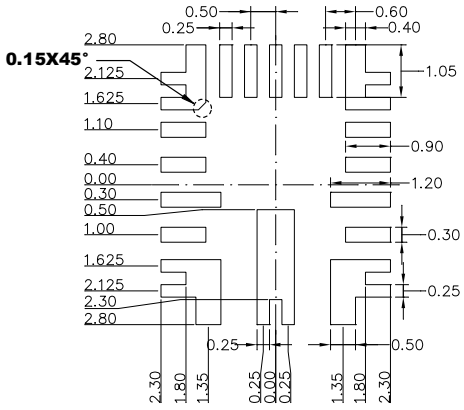
BOTTOM VIEW



SIDE VIEW



SECTION A-A



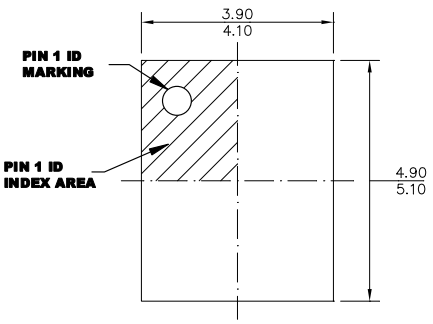
RECOMMENDED LAND PATTERN

NOTE:

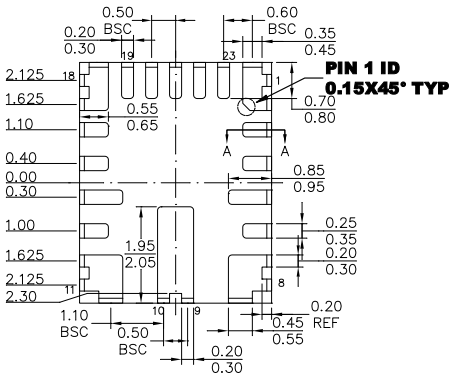
1) THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

PACKAGE INFORMATION *(continued)*

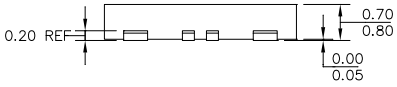
TQFN-23 (4mmx5mm)



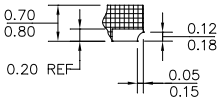
TOP VIEW



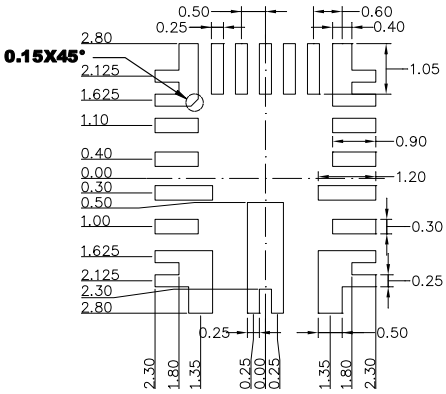
BOTTOM VIEW



SIDE VIEW



SECTION A-A



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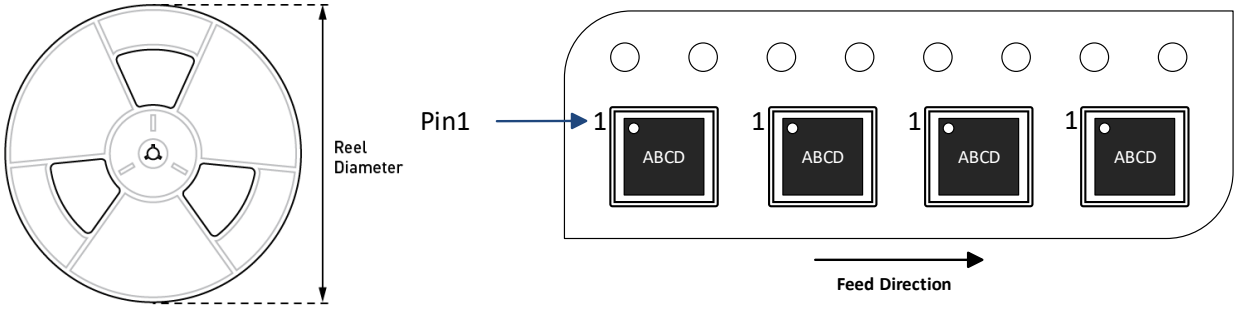
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube (16)	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ4372GVE-xxxx-AEC1-Z	QFN-23 (4mmx5mm)	5000	N/A	13in	12mm	8mm
MPQ4372GVTE-xxxx-AEC1-Z	TQFN-23 (4mmx5mm)	5000	N/A	13in	12mm	8mm

Note:

16) N/A indicates “not available” in tubes. For 500-piece tape & reel prototype quantities, contact the factory. (The order code for a 500-piece partial reel is “-P”; the tape & reel dimensions are the same as for the full reel.)

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	9/27/2024	Initial Release	-