



# MPQ4345/4345J

## 36V, 2A, Ultra-Low Quiescent Current, Synchronous Step-Down Converter, AEC-Q100 Qualified

### DESCRIPTION

The MPQ4345/4345J is a synchronous, step-down switching regulator with a 350kHz to 2.5MHz configurable frequency and an integrated internal high-side MOSFET (HS-FET) and low side MOSFET (LS-FET). The device provides up to 2A of highly efficient output current ( $I_{OUT}$ ) with fixed-frequency, zero-delay pulse-width modulation (PWM) control to optimize transient response.

The wide 3.3V to 36V input voltage ( $V_{IN}$ ) range and 42V load dump tolerance accommodate a variety of step-down applications in automotive input environments. A 1 $\mu$ A quiescent current ( $I_Q$ ) in shutdown mode allows the device to be used in battery-powered applications.

High power conversion efficiency across a wide load range is achieved by scaling down the switching frequency ( $f_{SW}$ ) under light-load conditions to reduce switching and gate driving losses.

An open-drain power good (PG) signal indicates that the output is within 94% to 106% of its nominal voltage.

Thermal shutdown provides reliable, fault-tolerant operation. A high duty cycle and low-dropout (LDO) mode are provided for automotive cold-crank conditions.

The MPQ4345 is available in a QFN-17 (3mmx4mm) package. The MPQ4345J is available in a QFN-19 (3mmx4mm) package.

### FEATURES

- Designed for Automotive Applications:
  - Survives 42V Load Dump
  - Supports 3.1V Cold Crank
  - Low-Dropout (LDO) Mode
  - 2A Continuous Output Current ( $I_{OUT}$ )
  - Continuous Operation Up to 36V
  - Zero-Delay Pulse-Width Modulation (PWM) Control
  - 20ns Minimum On Time ( $t_{ON\_MIN}$ )
  - 40°C to +150°C Operating Junction Temperature ( $T_J$ )

- Available in AEC-Q100 Grade 1
- Increases Battery Life:
  - 1 $\mu$ A Low Shutdown Supply Current
  - 3 $\mu$ A Sleep Mode Quiescent Current ( $I_Q$ )
  - Advanced Asynchronous Modulation (AAM) Mode Increases Efficiency under Light Loads
- High Performance for Improved Thermals:
  - Internal 60m $\Omega$  HS-FET and 35m $\Omega$  LS-FET
- Optimized for EMC and EMI:
  - 350kHz to 2.5MHz Configurable Switching Frequency ( $f_{SW}$ )
  - Symmetric VIN Pinout
  - Frequency Spread Spectrum (FSS) Modulation
  - MeshConnect™ Flip-Chip Package
- Additional Features:
  - Fixed Output Options <sup>(1)</sup>: 1V, 1.1V, 1.8V, 2.5V, 3V, 3.3V, 3.8V, 5V
  - Power Good (PG) Output
  - Synchronizable to External Clock
  - Synchronized Clock Output
  - External Soft Start (SS)
  - Over-Current Protection (OCP) in Hiccup Mode
  - Available in a QFN-17 (3mmx4mm) Package for MPQ4345 and a QFN-19 (3mmx4mm) Package for MPQ4345J with Wettable Flanks

### APPLICATIONS

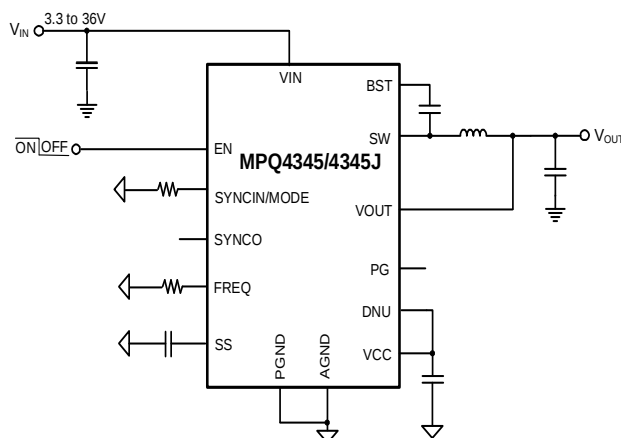
- Automotive Clusters
- Automotive Infotainment
- Advanced Driver Assistance Systems (ADAS)
- Industrial Power Systems

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#### Note:

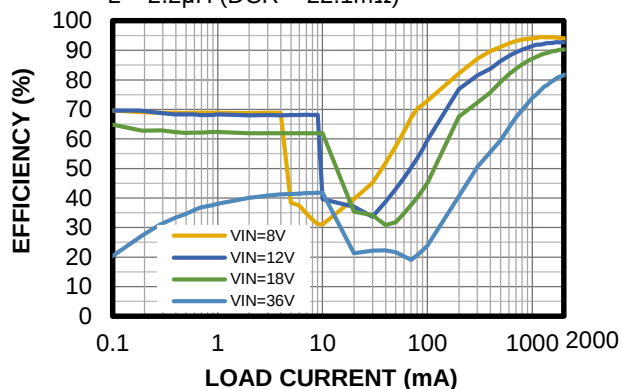
- See the Ordering Information section on page 3 for the exact availability of each fixed output version. Additional output voltages may be available. Contact MPS for more details.

## TYPICAL APPLICATION



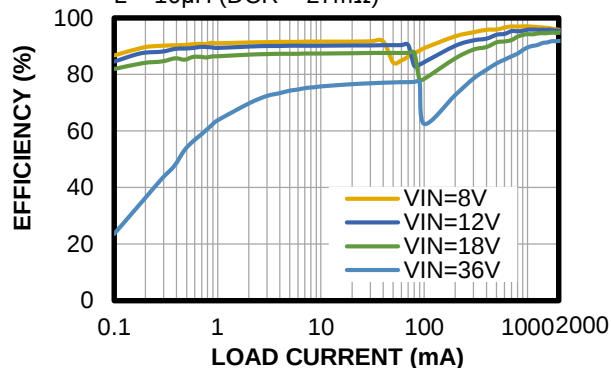
### Efficiency vs. Load Current

AAM mode,  $V_{OUT} = 5V$ ,  $f_{SW} = 2.2MHz$ ,  
 $R_{FB1} = 14.67M\Omega$ ,  $R_{FB2} = 2M\Omega$ ,  
 $L = 2.2\mu H$  (DCR = 22.1m $\Omega$ )



### Efficiency vs. Load Current

AAM mode,  $V_{OUT} = 5V$ ,  $f_{SW} = 410kHz$ ,  
 $R_{FB1} = 14.67M\Omega$ ,  $R_{FB2} = 2M\Omega$ ,  
 $L = 10\mu H$  (DCR = 27m $\Omega$ )



## ORDERING INFORMATION

| Part Number <sup>(2)</sup> * | Output Voltage | Package          | Top Marking | MSL Rating** |
|------------------------------|----------------|------------------|-------------|--------------|
| MPQ4345GLE-33-AEC1***        | Fixed 3.3V     | QFN-17 (3mmx4mm) | See Below   | 1            |
| MPQ4345GLE-5-AEC1***         | Fixed 5V       | QFN-17 (3mmx4mm) | See Below   | 1            |
| MPQ4345JGLE-33-AEC1***       | Fixed 3.3V     | QFN-19 (3mmx4mm) | See Below   | 1            |
| MPQ4345JGLE-5-AEC1***        | Fixed 5V       | QFN-19 (3mmx4mm) | See Below   | 1            |

\* For Tape & Reel, add suffix -Z (e.g. MPQ4345GLE-33-AEC1-Z).

\*\* Moisture Sensitivity Level Rating

\*\*\* Wettable flank

### Note:

2) Contact MPS for details on additional fixed output versions.

## TOP MARKING

(MPQ4345GLE-33-AEC1 and MPQ4345GLE-5-AEC1)

**MPYW**

**4345**

**LLL**

**E**

MP: MPS prefix  
Y: Year code  
W: Week code  
4345: Part number  
LLL: Lot number  
E: Wettable flank

## TOP MARKING

(MPQ4345JGLE-33-AEC1 and MPQ4345JGLE-5-AEC1)

**MPYW**

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MP: MPS prefix  
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## PACKAGE REFERENCE

| TOP VIEW                |   |    |    | TOP VIEW                |    |       |  |
|-------------------------|---|----|----|-------------------------|----|-------|--|
| VOUT AGND VCC           |   |    |    | VOUT AGND VCC           |    |       |  |
| SS                      | 1 | 17 | 16 | 15                      | 14 | DNU   |  |
| FREQ                    | 2 |    |    |                         | 13 | PG    |  |
| SYNCIN /MODE            | 3 |    |    |                         | 12 | SYNCO |  |
| VIN                     | 4 |    |    |                         | 11 | VIN   |  |
| PGND                    | 5 |    |    |                         | 10 | PGND  |  |
| BST                     | 6 |    |    |                         | 9  | EN    |  |
|                         |   | 7  | 8  |                         |    |       |  |
|                         |   | SW | SW |                         |    |       |  |
| <b>QFN-17 (3mmx4mm)</b> |   |    |    | <b>QFN-19 (3mmx4mm)</b> |    |       |  |

## PIN FUNCTIONS

| Pin #<br>QFN-19 | Pin #<br>QFN-17 | Name            | Description                                                                                                                                                                                                                                                                                                                                                                                  |
|-----------------|-----------------|-----------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1               | 1               | SS              | <b>Soft-start input.</b> Place a capacitor from the SS pin to ground to set the soft-start period. The MPQ4345/4345J sources 10 $\mu$ A from SS to the soft-start capacitor ( $C_{SS}$ ) at start-up. As the SS voltage ( $V_{SS}$ ) rises, the feedback reference voltage ( $V_{REF}$ ) increases to limit inrush current during start-up. Do not float this pin.                           |
| 2               | 2               | FREQ            | <b>Switching frequency configuration.</b> Connect a resistor from the FREQ pin to ground to set the switching frequency ( $f_{sw}$ ).                                                                                                                                                                                                                                                        |
| 3               | 3               | SYNCIN/<br>MODE | <b>SYNC input and MODE selection.</b> Apply a clock signal to the SYNCIN/MODE pin to synchronize the internal oscillator frequency to the external clock. Use an external clock or pull this pin high to enter forced continuous conduction mode (FCCM). Pull this pin low to allow advanced asynchronous modulation (AAM) mode and pulse skipping under light loads. Do not float this pin. |
| 4, 13           | 4, 11           | VIN             | <b>Input supply.</b> The VIN pin supplies power to all the internal control circuitry, as well as the power switch connected to SW. Place a decoupling capacitor from VIN to ground to minimize switching spikes. The capacitor should be placed close to VIN.                                                                                                                               |
| 5, 12           | -               | NC              | <b>No connection.</b> Float the NC pin.                                                                                                                                                                                                                                                                                                                                                      |
| 6, 11           | 5, 10           | PGND            | <b>Power ground.</b>                                                                                                                                                                                                                                                                                                                                                                         |
| 7               | 6               | BST             | <b>Bootstrap.</b> The BST pin is the positive power supply for the high-side MOSFET (HS-FET) connected to SW. Connect a bypass capacitor between the BST and SW pins. See the Bootstrap Charging (BST, Pin 6) section on page 37 to calculate the size of this capacitor.                                                                                                                    |
| 8, 9            | 7, 8            | SW              | <b>Switch node.</b> The SW pin is the internal power switch's output.                                                                                                                                                                                                                                                                                                                        |
| 10              | 9               | EN              | <b>Enable.</b> Pull the EN pin below the specified threshold (0.85V) to shut down the chip. Pull EN above the specified threshold (1V) to enable the chip. Do not float this pin.                                                                                                                                                                                                            |
| 14              | 12              | SYNCO           | <b>SYNC output.</b> The SYNCO pin outputs a clock signal in phase with the internal oscillator signal, or the clock signal applied at the SYNCIN/MODE pin. This pin can be floated.                                                                                                                                                                                                          |
| 15              | 13              | PG              | <b>Power good output.</b> The PG pin's output is an open drain. If PG is used, it should be connected to a power source via a pull-up resistor. PG goes high if the output voltage ( $V_{OUT}$ ) is within 94% to 106% of the nominal voltage. PG goes low if $V_{OUT}$ is above 107% or below 93% of the nominal voltage. Float this pin if not used.                                       |
| 16              | 14              | DNU             | <b>Do not use.</b> Connect the DNU pin directly to VCC.                                                                                                                                                                                                                                                                                                                                      |
| 17              | 15              | VCC             | <b>Bias supply.</b> The VCC pin supplies 5V power to the internal control circuit and gate drivers. Place a decoupling capacitor from VCC to ground, and close to this pin. See the Setting the VCC Capacitor (VCC, Pin 15) section on page 39 to calculate the size of this capacitor.                                                                                                      |
| 18              | 16              | AGND            | <b>Analog ground.</b>                                                                                                                                                                                                                                                                                                                                                                        |
| 19              | 17              | VOUT            | <b><math>V_{OUT}</math> regulation point.</b> Connect the VOUT pin directly to $V_{OUT}$ .                                                                                                                                                                                                                                                                                                   |

## ABSOLUTE MAXIMUM RATINGS <sup>(3)</sup>

|                                                      |                                      |
|------------------------------------------------------|--------------------------------------|
| VIN, EN.....                                         | -0.3V to +42V                        |
| SW.....                                              | -0.3V to V <sub>IN(MAX)</sub> + 0.3V |
| BST.....                                             | V <sub>SW</sub> +5.5V                |
| All other pins.....                                  | -0.3V to +6V                         |
| Continuous power dissipation (T <sub>A</sub> = 25°C) |                                      |
| QFN-17 (3mmx4mm) <sup>(4) (8)</sup> .....            | 4.28W                                |
| QFN-19 (3mmx4mm) <sup>(4) (8)</sup> .....            | 4.13W                                |
| Operating junction temperature .....                 | 150°C                                |
| Lead temperature.....                                | 260°C                                |
| Storage temperature.....                             | -65°C to +150°C                      |

## ESD Ratings

|                                 |                          |
|---------------------------------|--------------------------|
| Human body model (HBM).....     | Class 2 <sup>(5)</sup>   |
| Charged device model (CDM)..... | Class C2b <sup>(6)</sup> |

## Recommended Operating Conditions

|                                                |                 |
|------------------------------------------------|-----------------|
| Supply voltage (V <sub>IN</sub> ).....         | 3.3V to 36V     |
| Operating junction temp (T <sub>J</sub> )..... | -40°C to +150°C |

| Thermal Resistance  | $\theta_{JA}$ | $\theta_{JC}$              |
|---------------------|---------------|----------------------------|
| QFN-17 (3mmx4mm)    |               |                            |
| JESD51-7.....       | 44.7.....     | 5.2....°C/W <sup>(7)</sup> |
| EVQ4345-L-00A.....  | 29.2.....     | °C/W <sup>(8)</sup>        |
|                     |               | $\Psi_{JT}$                |
| JESD51-7.....       |               | 1.2....°C/W <sup>(7)</sup> |
| EVQ4345-L-00A.....  |               | 6.1....°C/W <sup>(8)</sup> |
| QFN-19 (3mmx4mm)    | $\theta_{JA}$ | $\theta_{JC}$              |
| JESD51-7.....       | 43.6.....     | 5.4....°C/W <sup>(7)</sup> |
| EVQ4345J-L-00A..... | 30.3.....     | °C/W <sup>(8)</sup>        |
|                     |               | $\Psi_{JT}$                |
| JESD51-7.....       |               | 0.9....°C/W <sup>(7)</sup> |
| EVQ4345J-L-00A..... |               | 5.17...°C/W <sup>(8)</sup> |

### Notes:

- 3) Exceeding these ratings may damage the device.
- 4) The maximum allowable power dissipation is a function of the maximum junction temperature, T<sub>J</sub> (MAX), the junction-to-ambient thermal resistance,  $\theta_{JA}$ , and the ambient temperature, T<sub>A</sub>. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P<sub>D</sub> (MAX) = (T<sub>J</sub> (MAX) - T<sub>A</sub>) /  $\theta_{JA}$ . Exceeding the maximum allowable power dissipation can produce an excessive die temperature, which may cause the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- 5) Per AEC-Q100-002.
- 6) Per AEC-Q100-011.
- 7) Measured on JESD51-7, a 4-layer PCB. The values given in this table are only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application. The  $\theta_{JC}$  value shows the thermal resistance from junction-to-case bottom. The  $\Psi_{JT}$  value shows the characterization parameter from the junction-to-case top.
- 8) Measured on an MPS standard EVB, a 2oz copper thickness, 4-layer PCB (8.3cmx8.3cm). The  $\Psi_{JT}$  value shows the characterization parameter from the junction-to-case top.

## ELECTRICAL CHARACTERISTICS

$V_{IN} = 12V$ ,  $V_{EN} = 2V$ ,  $T_J = -40^{\circ}C$  to  $+150^{\circ}C$ , typical values are at  $T_J = 25^{\circ}C$ , unless otherwise noted.

| Parameter                                              | Symbol                  | Condition                                                                                       | Min  | Typ  | Max  | Units      |
|--------------------------------------------------------|-------------------------|-------------------------------------------------------------------------------------------------|------|------|------|------------|
| <b>Input Supply</b>                                    |                         |                                                                                                 |      |      |      |            |
| Minimum operating input voltage ( $V_{IN}$ )           | $V_{IN\_MIN}$           |                                                                                                 |      |      | 3.3  | V          |
| $V_{IN}$ under-voltage lockout (UVLO) rising threshold | $V_{IN\_UVLO\_RISING}$  |                                                                                                 | 2.8  | 3    | 3.2  | V          |
| $V_{IN}$ UVLO falling threshold                        | $V_{IN\_UVLO\_FALLING}$ |                                                                                                 | 2.6  | 2.8  | 3    | V          |
| $V_{IN}$ UVLO hysteresis                               | $V_{IN\_UVLO\_HYS}$     |                                                                                                 |      | 200  |      | mV         |
| $V_{IN}$ quiescent current <sup>(9)</sup>              | $I_Q$                   | $V_{OUT} = 1.05 \times V_{SET}$ , no load (sleep mode), $T_J = -40^{\circ}C$ to $+85^{\circ}C$  | 1.9  | 3    | 3.6  | $\mu A$    |
|                                                        |                         | $V_{OUT} = 1.05 \times V_{SET}$ , no load (sleep mode), $T_J = -40^{\circ}C$ to $+125^{\circ}C$ | 1.5  |      | 15   | $\mu A$    |
| $V_{IN}$ switching quiescent current <sup>(9)</sup>    | $I_{Q\_SLEEP}$          | SYNCIN/MODE = GND (AAM mode), switching, no load, $T_J = -40^{\circ}C$ to $+85^{\circ}C$        | 2.4  | 3.5  | 4.5  | $\mu A$    |
|                                                        |                         | SYNCIN/MODE = GND (AAM mode), switching, no load, $T_J = -40^{\circ}C$ to $+125^{\circ}C$       | 2    |      | 16   | $\mu A$    |
| $V_{IN}$ active current (no switching)                 | $I_{Q\_ACTIVE}$         | SYNCIN/MODE = VCC (FCCM), no switching                                                          |      | 1200 |      | $\mu A$    |
| $V_{IN}$ shutdown current                              | $I_{SHDN}$              | EN = 0V, $T_J = 25^{\circ}C$                                                                    |      | 1    | 3    | $\mu A$    |
|                                                        |                         | EN = 0V                                                                                         |      |      | 11   | $\mu A$    |
| $V_{IN}$ over-voltage protection (OVP) threshold       | $V_{IN\_OVP\_RISING}$   |                                                                                                 | 36   | 38   | 40   | V          |
| $V_{IN}$ OVP hysteresis                                | $V_{IN\_OVP\_HYS}$      |                                                                                                 |      | 10   |      | V          |
| <b>Enable (EN)</b>                                     |                         |                                                                                                 |      |      |      |            |
| EN rising threshold                                    | $V_{EN\_RISING}$        |                                                                                                 | 0.8  | 1    | 1.2  | V          |
| EN falling threshold                                   | $V_{EN\_FALLING}$       |                                                                                                 | 0.65 | 0.85 | 1.05 | V          |
| EN hysteresis voltage                                  | $V_{EN\_HYS}$           |                                                                                                 |      | 150  |      | mV         |
| <b>Switches and Frequency</b>                          |                         |                                                                                                 |      |      |      |            |
| Switching frequency                                    | $f_{SW}$                | $R_{FREQ} = 86.6k\Omega$                                                                        | 370  | 410  | 450  | kHz        |
|                                                        |                         | $R_{FREQ} = 33k\Omega$                                                                          | 950  | 1050 | 1150 | kHz        |
|                                                        |                         | $R_{FREQ} = 15k\Omega$                                                                          | 1980 | 2200 | 2420 | kHz        |
| Minimum on time                                        | $t_{ON\_MIN}$           |                                                                                                 |      | 20   | 35   | ns         |
| Minimum off time                                       | $t_{OFF\_MIN}$          |                                                                                                 |      | 120  | 140  | ns         |
| Switch leakage current                                 | $I_{SW\_LKG}$           |                                                                                                 |      | 0.01 | 5    | $\mu A$    |
| High-side MOSFET (HS-FET) on resistance                | $R_{DS(ON)\_HS}$        | $V_{BST} - V_{SW} = 5V$                                                                         |      | 60   | 110  | m $\Omega$ |
| Low-side MOSFET (LS-FET) on resistance                 | $R_{DS(ON)\_LS}$        | $V_{CC} = 5V$                                                                                   |      | 35   | 60   | m $\Omega$ |

## ELECTRICAL CHARACTERISTICS (continued)

V<sub>IN</sub> = 12V, V<sub>EN</sub> = 2V, T<sub>J</sub> = -40°C to +150°C, typical values are at T<sub>J</sub> = 25°C, unless otherwise noted.

| Parameter                                                              | Symbol                      | Condition                                                       | Min  | Typ  | Max  | Units |
|------------------------------------------------------------------------|-----------------------------|-----------------------------------------------------------------|------|------|------|-------|
| <b>Bootstrap (BST)</b>                                                 |                             |                                                                 |      |      |      |       |
| BST to SW refresh rising threshold                                     | V <sub>BST-SW_RISING</sub>  |                                                                 |      | 2.5  | 2.9  | V     |
| BST to SW refresh falling threshold                                    | V <sub>BST-SW_FALLING</sub> |                                                                 |      | 2.3  | 2.7  | V     |
| BST to SW refresh hysteresis                                           | V <sub>BST-SW_HYS</sub>     |                                                                 |      | 0.2  |      | V     |
| <b>Soft Start (SS) and VCC</b>                                         |                             |                                                                 |      |      |      |       |
| VCC voltage                                                            | V <sub>CC</sub>             | I <sub>VCC</sub> = 0                                            | 4.7  | 5    | 5.3  | V     |
| VCC regulation                                                         |                             | I <sub>VCC</sub> = 0mA and 30mA                                 |      |      | 1    | %     |
| VCC current limit                                                      | I <sub>LIMIT_VCC</sub>      | V <sub>CC</sub> = 4V                                            | 50   | 100  |      | mA    |
|                                                                        |                             | V <sub>CC</sub> = 0V                                            |      | 70   |      | mA    |
| Soft-start current                                                     | I <sub>SS</sub>             | V <sub>SS</sub> = 0V                                            |      | 10   |      | μA    |
| <b>Output and Regulation</b>                                           |                             |                                                                 |      |      |      |       |
| Output voltage (V <sub>OUT</sub> ) accuracy, 3.3V fixed output version | V <sub>OUT_ACC_3.3</sub>    | T <sub>J</sub> = 25°C                                           | 3260 | 3300 | 3340 | mV    |
|                                                                        |                             | T <sub>J</sub> = -40°C to +150°C                                | 3230 | 3300 | 3370 | mV    |
| V <sub>OUT</sub> accuracy, 5V fixed output version                     | V <sub>OUT_ACC_5</sub>      | T <sub>J</sub> = 25°C                                           | 4940 | 5000 | 5060 | mV    |
|                                                                        |                             | T <sub>J</sub> = -40°C to +150°C                                | 4900 | 5000 | 5100 | mV    |
| V <sub>OUT</sub> current                                               | I <sub>VOUT</sub>           | V <sub>OUT</sub> = V <sub>OUT_REG</sub>                         |      | 300  |      | nA    |
| V <sub>OUT</sub> discharge                                             | I <sub>DISCHARGE</sub>      | EN = 0V, V <sub>OUT</sub> = 0.3V, V <sub>IN</sub> = 3.3V to 36V | 1.8  |      |      | mA    |
| <b>Power Good (PG)</b>                                                 |                             |                                                                 |      |      |      |       |
| PG rising threshold                                                    | PG <sub>VTH_RISING</sub>    | V <sub>OUT</sub> rising                                         | 91   | 94   | 97   | %     |
|                                                                        |                             | V <sub>OUT</sub> falling                                        | 103  | 106  | 109  |       |
| PG falling threshold                                                   | PG <sub>VTH_FALLING</sub>   | V <sub>OUT</sub> falling                                        | 90   | 93   | 96   | %     |
|                                                                        |                             | V <sub>OUT</sub> rising                                         | 104  | 107  | 110  |       |
| PG trip threshold hysteresis                                           | PG <sub>Vth_HYS</sub>       |                                                                 |      | 1    |      | %     |
| PG low V <sub>OUT</sub>                                                | V <sub>PG_LOW</sub>         | I <sub>SINK</sub> = 1mA                                         |      | 0.1  | 0.3  | V     |
| PG rising delay time                                                   | t <sub>PG_R_DELAY</sub>     |                                                                 |      | 50   |      | μs    |
| PG falling delay time                                                  | t <sub>PG_F_DELAY</sub>     |                                                                 |      | 50   |      | μs    |
| <b>SYNCIN and SYNCO</b>                                                |                             |                                                                 |      |      |      |       |
| SYNCIN/MODE voltage rising threshold                                   | V <sub>SYNC_RISING</sub>    |                                                                 | 1.8  |      |      | V     |
| SYNCIN/MODE voltage falling threshold                                  | V <sub>SYNC_FALLING</sub>   |                                                                 |      |      | 0.4  | V     |
| SYNCIN/MODE timeout                                                    | t <sub>MODE</sub>           | SYNCIN/MODE low to AAM mode                                     |      | 41   |      | μs    |
| SYNCIN clock range                                                     | f <sub>SYNC</sub>           | % of free-running frequency                                     | 90   |      | 115  | %     |
| SYNCO high voltage                                                     | V <sub>SYNCO_HIGH</sub>     | I <sub>SYNCO</sub> = -1mA                                       | 3.3  | 5    |      | V     |
| SYNCO low voltage                                                      | V <sub>SYNCO_LOW</sub>      | I <sub>SYNCO</sub> = 1mA                                        |      |      | 0.4  | V     |

## ELECTRICAL CHARACTERISTICS (continued)

$V_{IN} = 12V$ ,  $V_{EN} = 2V$ ,  $T_J = -40^{\circ}C$  to  $+150^{\circ}C$ , typical values are at  $T_J = 25^{\circ}C$ , unless otherwise noted.

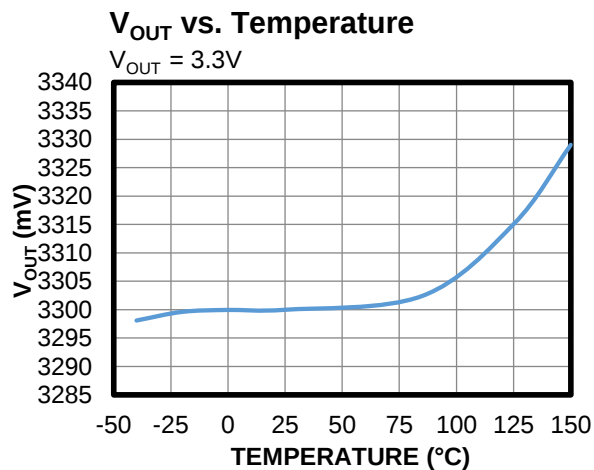
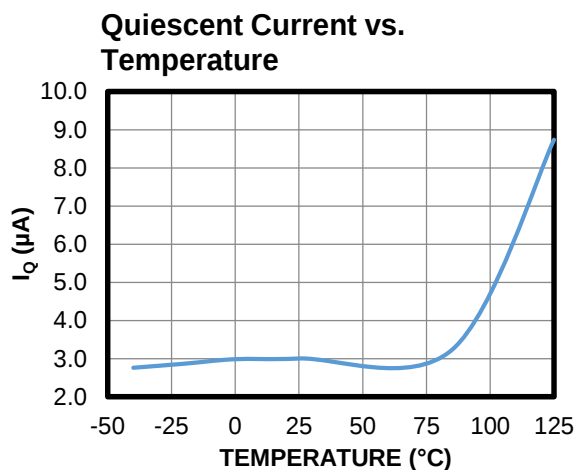
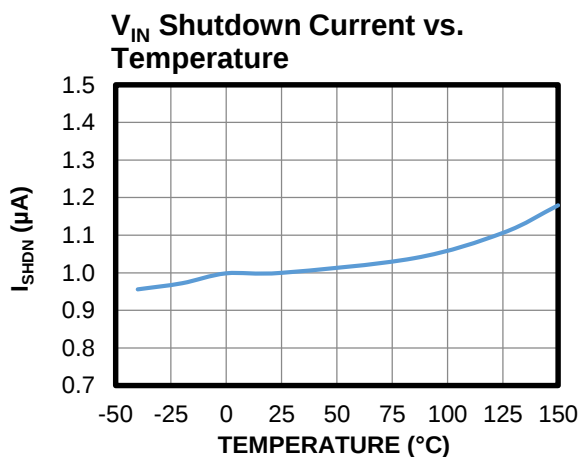
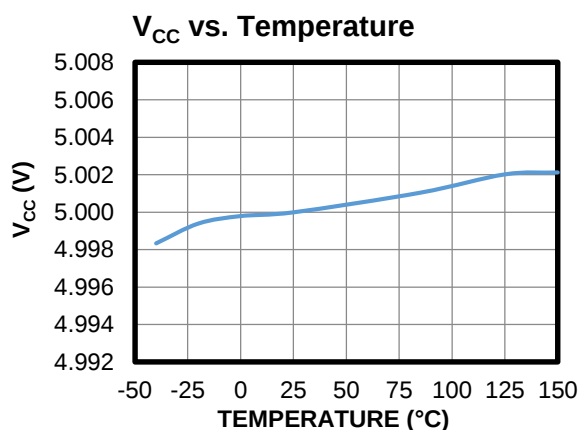
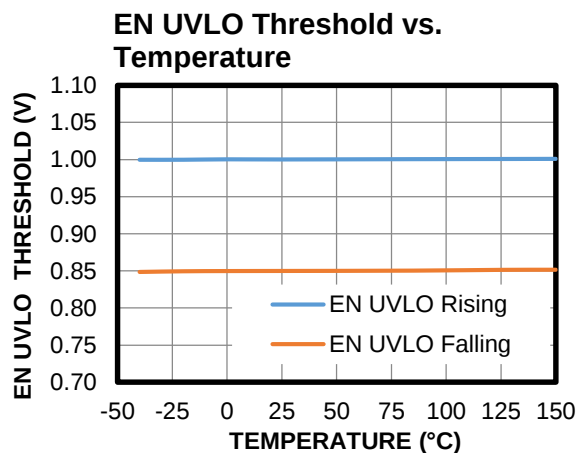
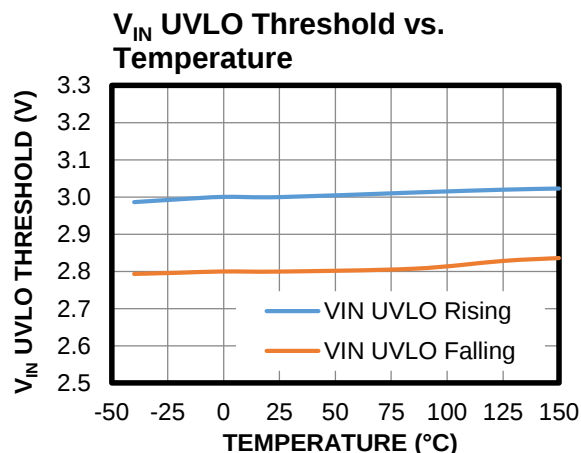
| Parameter                                         | Symbol               | Condition        | Min   | Typ  | Max   | Units       |
|---------------------------------------------------|----------------------|------------------|-------|------|-------|-------------|
| <b>Protections</b>                                |                      |                  |       |      |       |             |
| High-side (HS) current limit                      | $I_{LIMIT\_HS}$      | Duty cycle = 30% | 4.7   | 5.8  | 7.3   | A           |
| Low-side (LS) valley current limit <sup>(9)</sup> | $I_{LIMIT\_LS}$      |                  | 3     | 4.4  | 5.7   | A           |
| Zero-current detection (ZCD) current              | $I_{ZCD}$            | AAM mode         | -0.05 | +0.1 | +0.25 | A           |
| LS reverse current limit                          | $I_{LIMIT\_REVERSE}$ | FCCM             |       | 4    |       | A           |
| Thermal shutdown <sup>(9)</sup>                   | $T_{SD}$             |                  | 150   | 170  |       | $^{\circ}C$ |
| Thermal shutdown hysteresis <sup>(9)</sup>        | $T_{SD\_HYS}$        |                  |       | 20   |       | $^{\circ}C$ |

**Note:**

9) Guaranteed by design and characterization. Not tested in production.

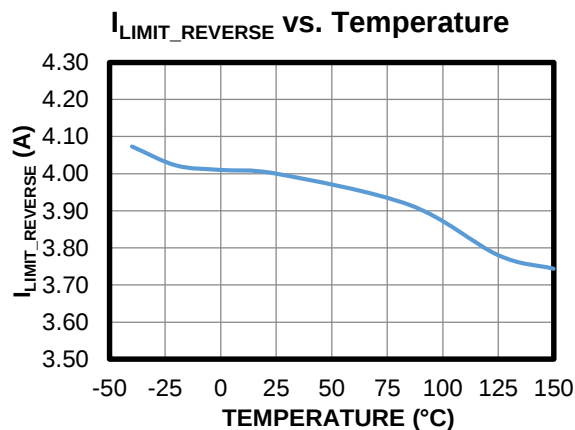
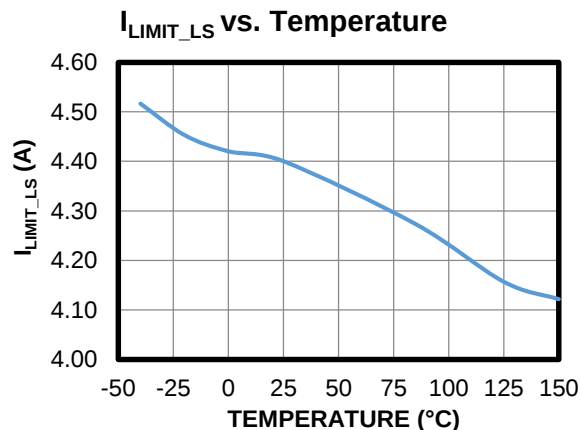
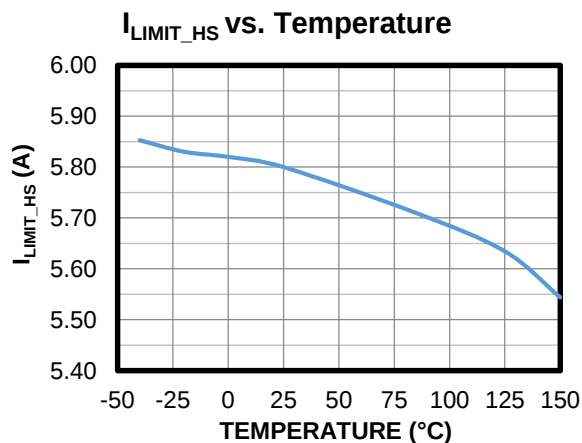
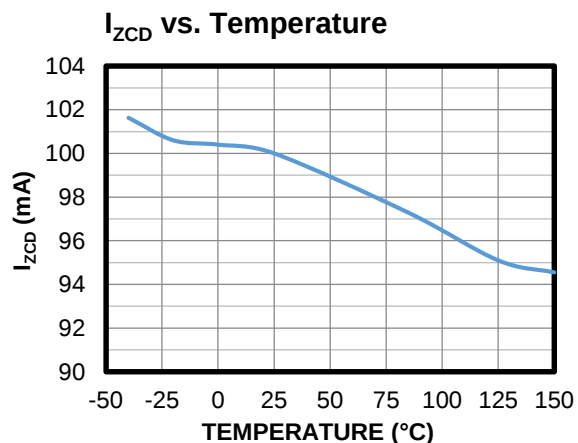
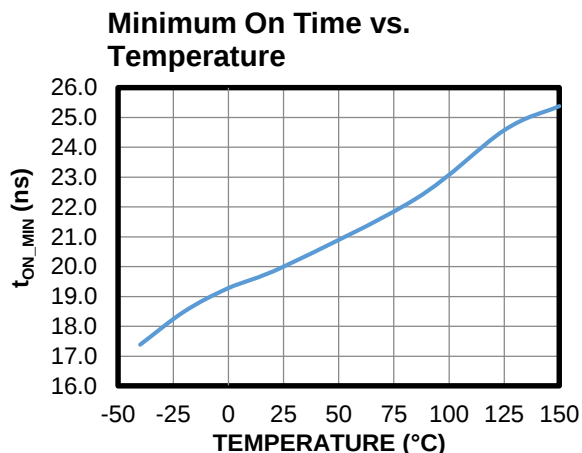
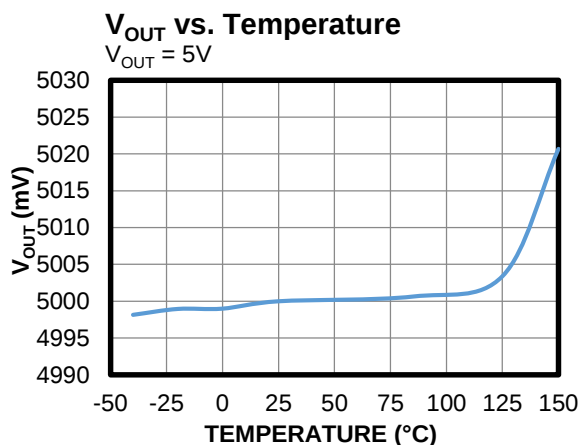
# TYPICAL CHARACTERISTICS

$V_{IN} = 12V$ ,  $T_J = -40^{\circ}C$  to  $+150^{\circ}C$ , unless otherwise noted.



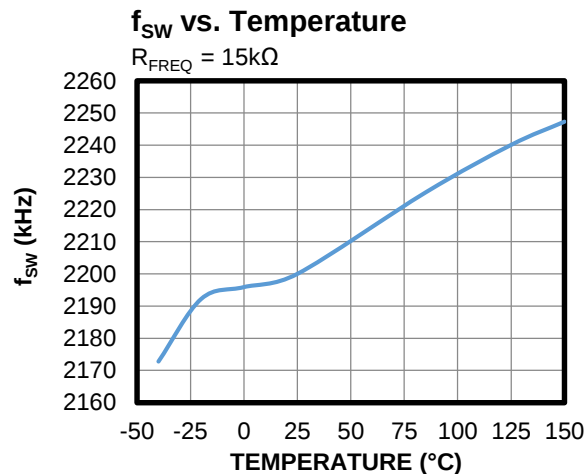
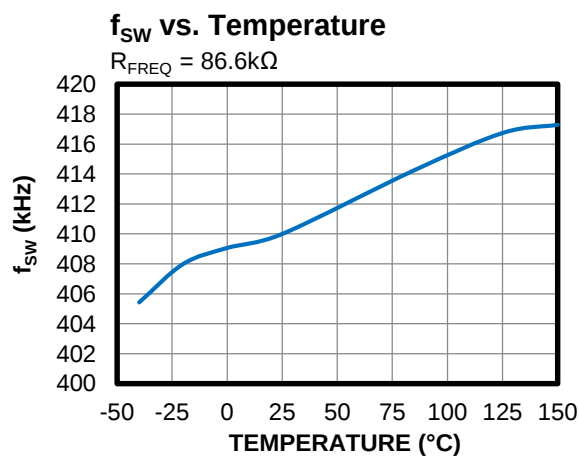
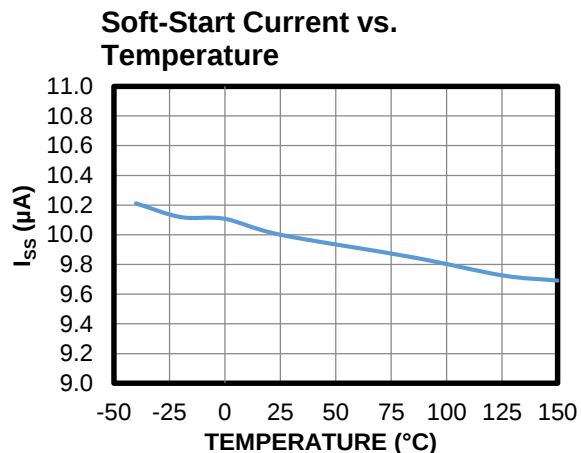
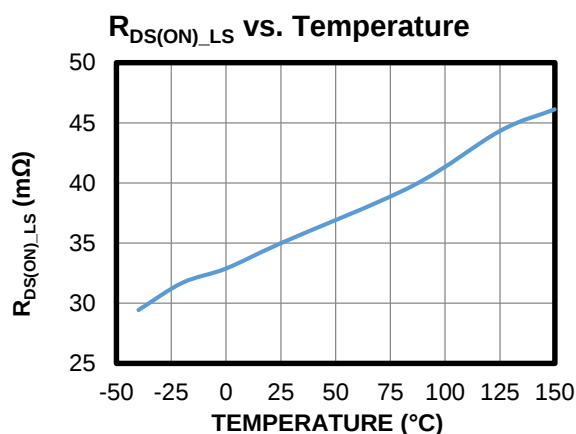
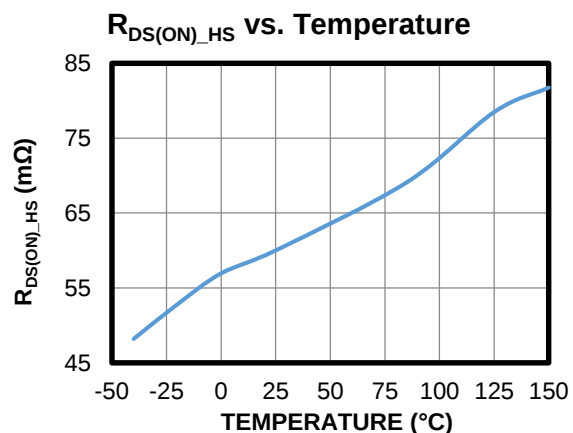
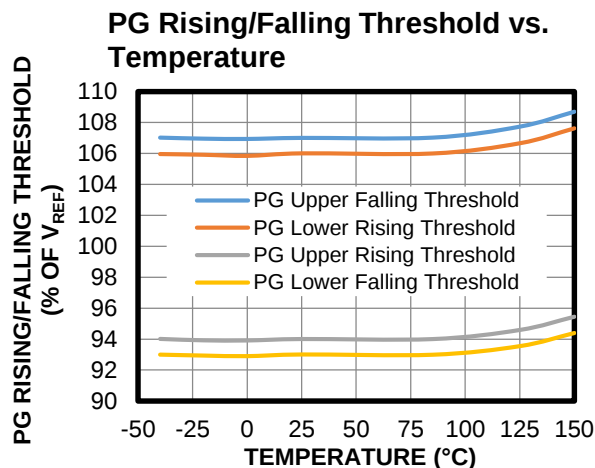
# TYPICAL CHARACTERISTICS (continued)

$V_{IN} = 12V$ ,  $T_J = -40^{\circ}C$  to  $+150^{\circ}C$ , unless otherwise noted.



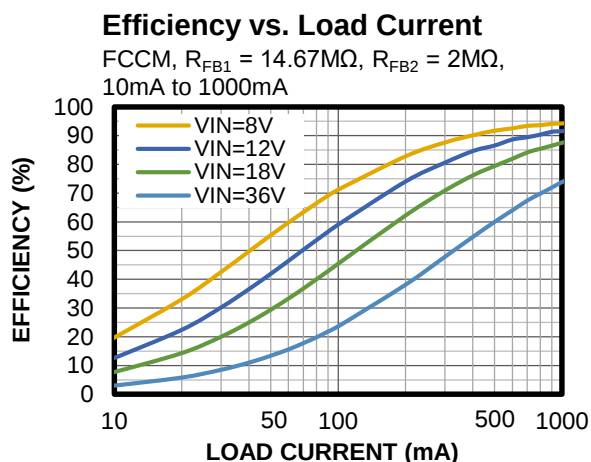
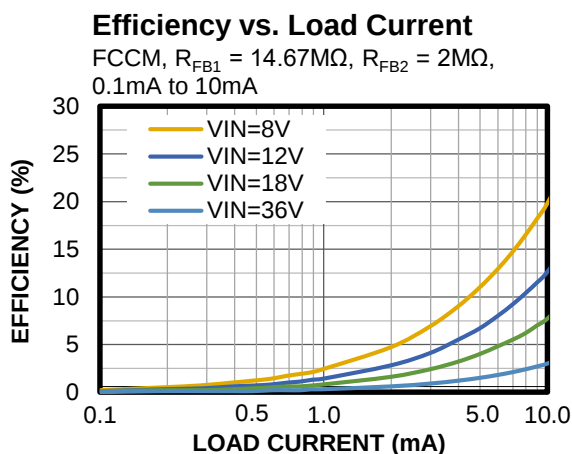
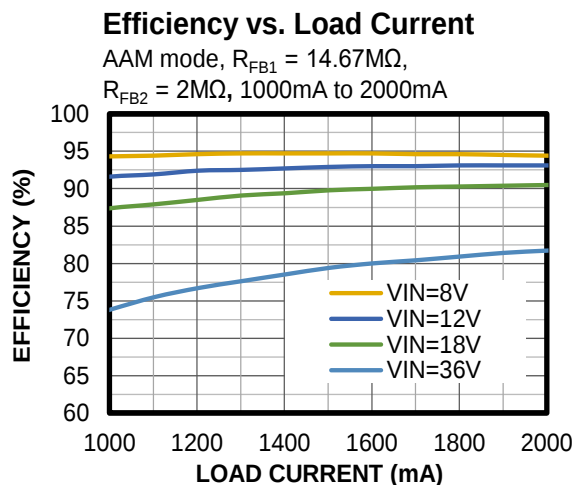
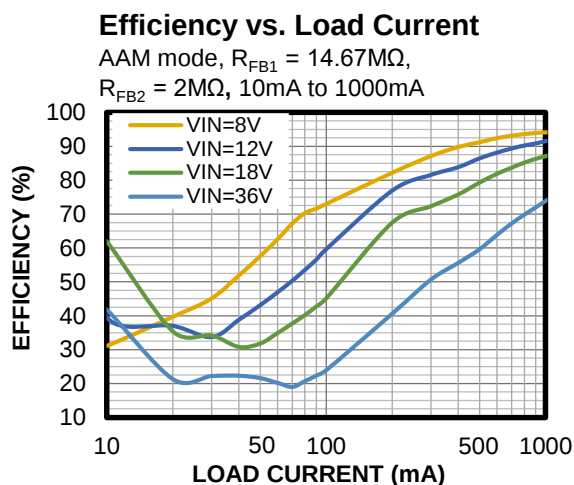
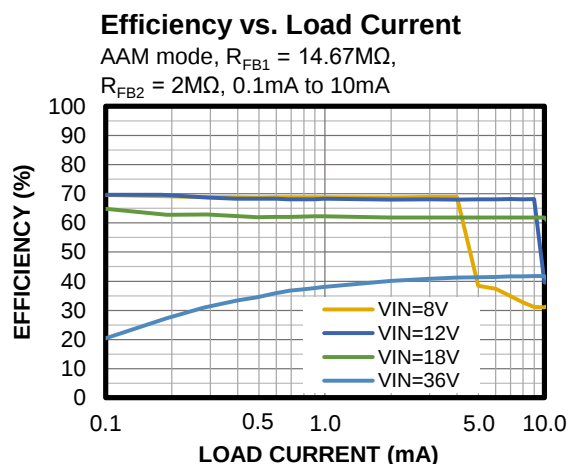
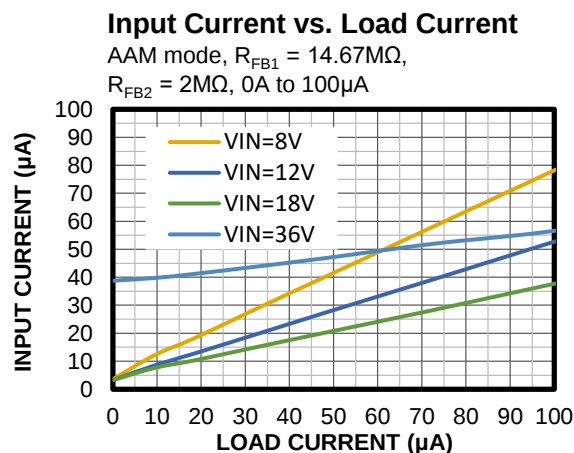
# TYPICAL CHARACTERISTICS (continued)

$V_{IN} = 12V$ ,  $T_J = -40^{\circ}C$  to  $+150^{\circ}C$ , unless otherwise noted.



## TYPICAL PERFORMANCE CHARACTERISTICS

$V_{IN} = 12V$ ,  $V_{OUT} = 5V$ ,  $L = 2.2\mu H$  (DCR = 22.1m $\Omega$ ),  $f_{SW} = 2.2MHz$ , AAM mode,  $T_A = 25^\circ C$ , unless otherwise noted.

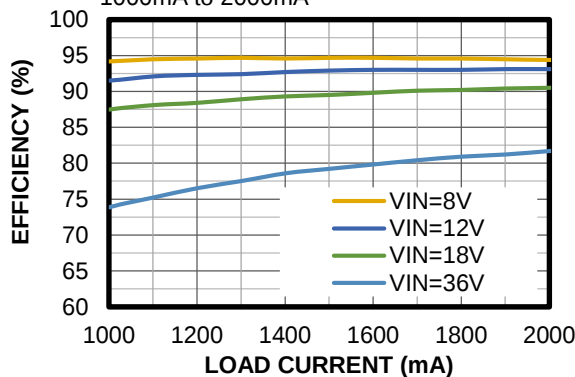


# TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN} = 12V$ ,  $V_{OUT} = 5V$ ,  $L = 2.2\mu H$  (DCR = 22.1m $\Omega$ ),  $f_{SW} = 2.2MHz$ , AAM mode,  $T_A = 25^\circ C$ , unless otherwise noted.

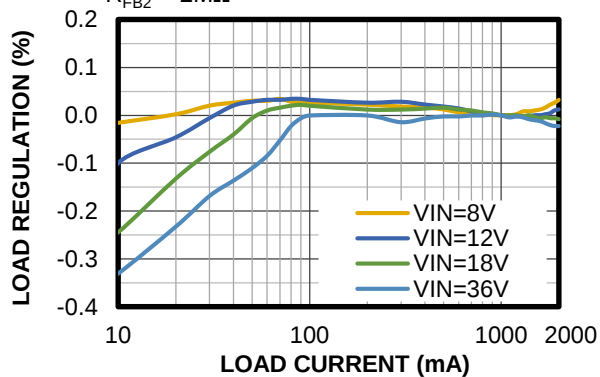
## Efficiency vs. Load Current

FCCM,  $R_{FB1} = 14.67M\Omega$ ,  $R_{FB2} = 2M\Omega$ ,  
1000mA to 2000mA



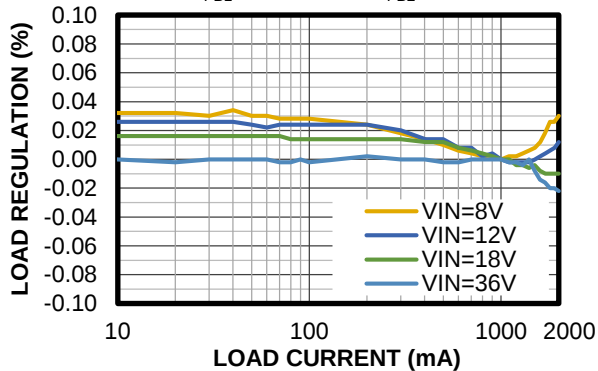
## Load Regulation

AAM mode,  $R_{FB1} = 14.67M\Omega$ ,  
 $R_{FB2} = 2M\Omega$



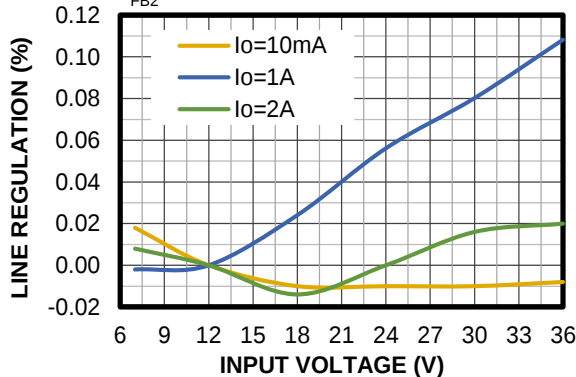
## Load Regulation

FCCM,  $R_{FB1} = 14.67M\Omega$ ,  $R_{FB2} = 2M\Omega$



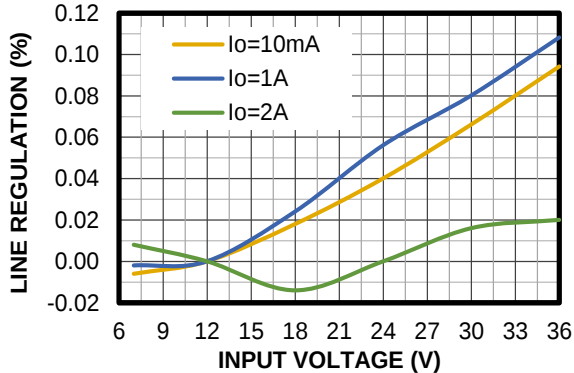
## Line Regulation

AAM mode,  $R_{FB1} = 14.67M\Omega$ ,  
 $R_{FB2} = 2M\Omega$



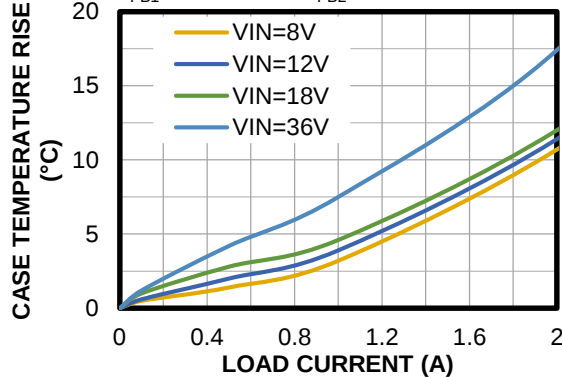
## Line Regulation

FCCM,  $R_{FB1} = 14.67M\Omega$ ,  $R_{FB2} = 2M\Omega$



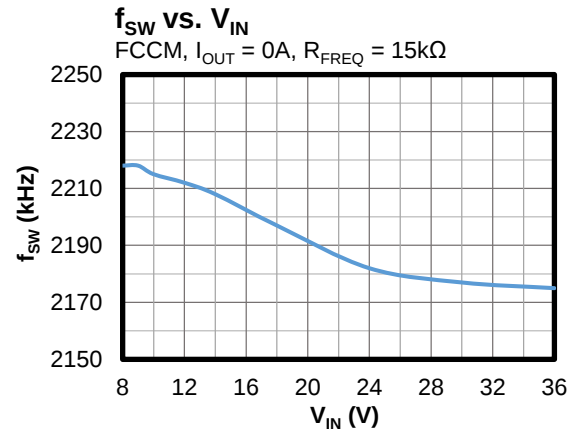
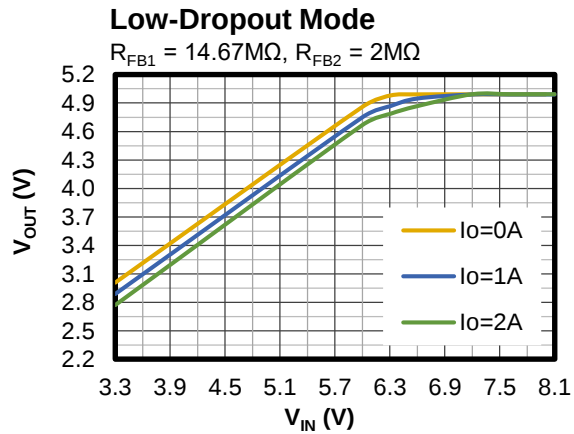
## Case Temperature Rise

$R_{FB1} = 14.67M\Omega$ ,  $R_{FB2} = 2M\Omega$



## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

$V_{IN} = 12V$ ,  $V_{OUT} = 5V$ ,  $L = 2.2\mu H$  (DCR = 22.1m $\Omega$ ),  $f_{SW} = 2.2MHz$ , AAM mode,  $T_A = 25^\circ C$ , unless otherwise noted.

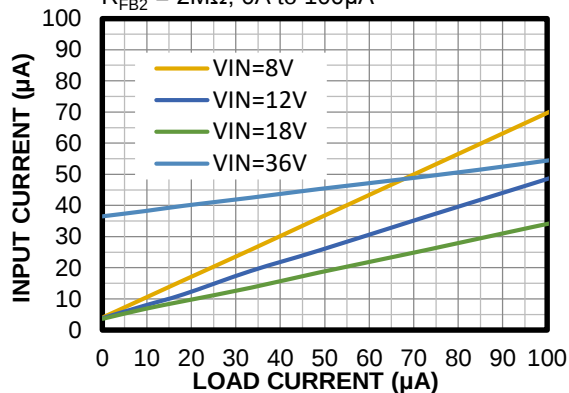


# TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN} = 12V$ ,  $V_{OUT} = 5V$ ,  $L = 10\mu H$  (DCR = 27m $\Omega$ ),  $f_{SW} = 410kHz$ , AAM mode,  $T_A = 25^\circ C$ , unless otherwise noted.

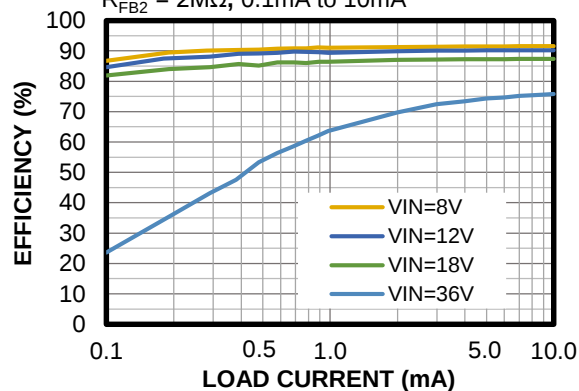
## Input Current vs. Load Current

AAM mode,  $R_{FB1} = 14.67M\Omega$ ,  
 $R_{FB2} = 2M\Omega$ , 0A to 100 $\mu A$



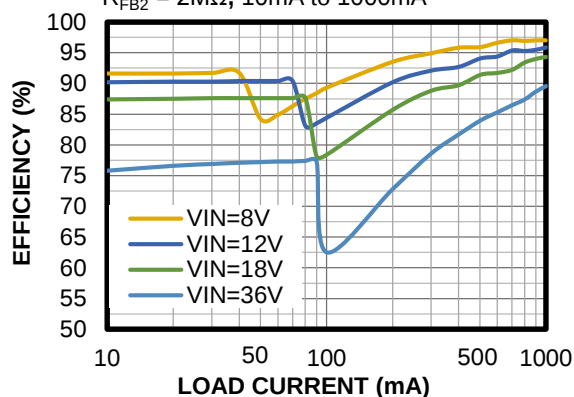
## Efficiency vs. Load Current

AAM mode,  $R_{FB1} = 14.67M\Omega$ ,  
 $R_{FB2} = 2M\Omega$ , 0.1mA to 10mA



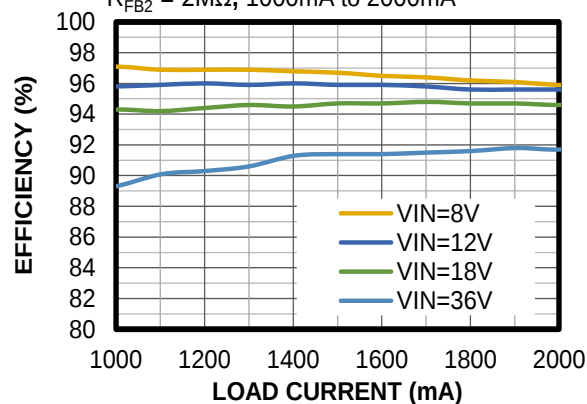
## Efficiency vs. Load Current

AAM mode,  $R_{FB1} = 14.67M\Omega$ ,  
 $R_{FB2} = 2M\Omega$ , 10mA to 1000mA



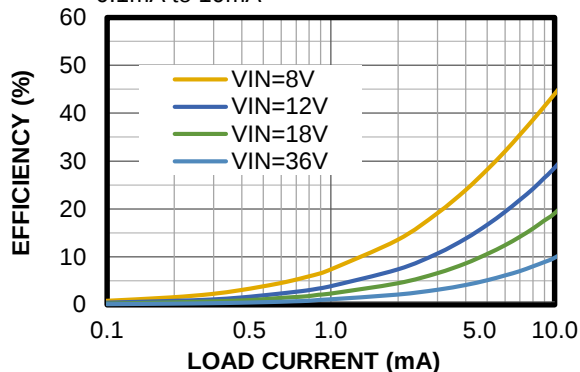
## Efficiency vs. Load Current

AAM mode,  $R_{FB1} = 14.67M\Omega$ ,  
 $R_{FB2} = 2M\Omega$ , 1000mA to 2000mA



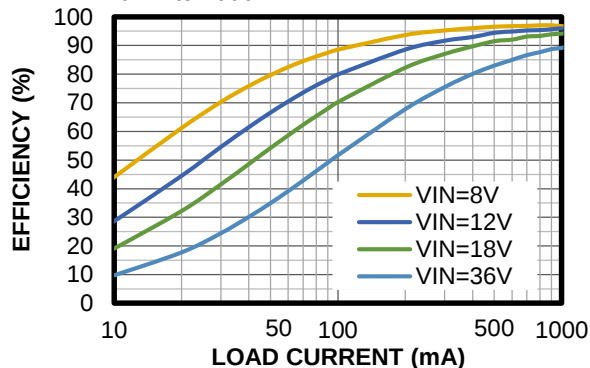
## Efficiency vs. Load Current

FCCM,  $R_{FB1} = 14.67M\Omega$ ,  $R_{FB2} = 2M\Omega$ ,  
0.1mA to 10mA



## Efficiency vs. Load Current

FCCM,  $R_{FB1} = 14.67M\Omega$ ,  $R_{FB2} = 2M\Omega$ ,  
10mA to 1000mA

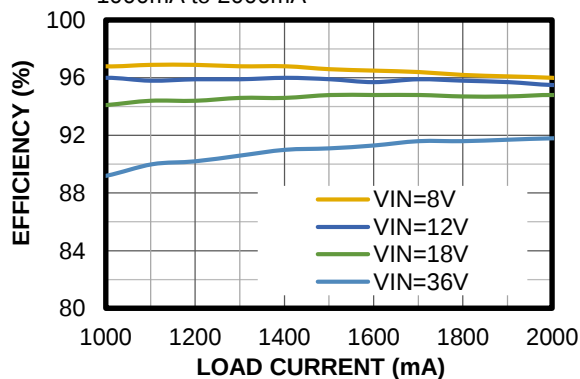


# TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN} = 12V$ ,  $V_{OUT} = 5V$ ,  $L = 10\mu H$  (DCR = 27m $\Omega$ ),  $f_{SW} = 410kHz$ , AAM mode,  $T_A = 25^\circ C$ , unless otherwise noted.

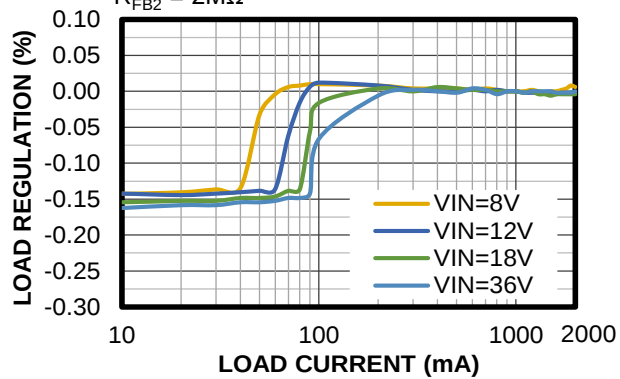
## Efficiency vs. Load Current

FCCM,  $R_{FB1} = 14.67M\Omega$ ,  $R_{FB2} = 2M\Omega$ ,  
1000mA to 2000mA



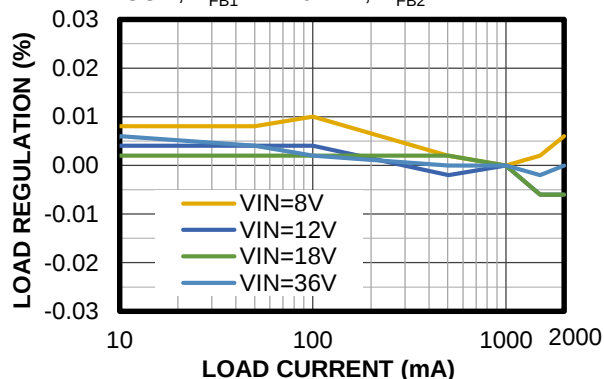
## Load Regulation

AAM mode,  $R_{FB1} = 14.67M\Omega$ ,  
 $R_{FB2} = 2M\Omega$



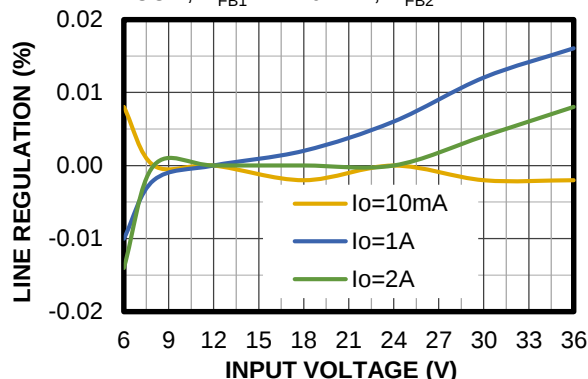
## Load Regulation

FCCM,  $R_{FB1} = 14.67M\Omega$ ,  $R_{FB2} = 2M\Omega$



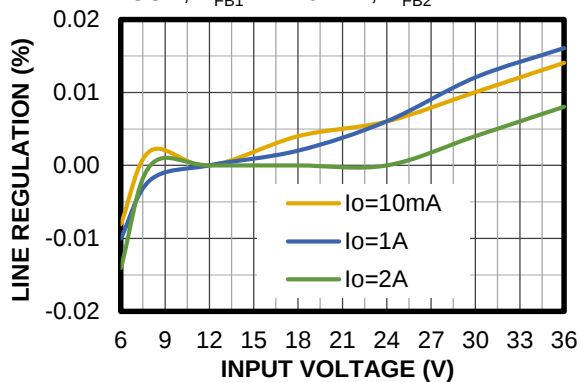
## Line Regulation

FCCM,  $R_{FB1} = 14.67M\Omega$ ,  $R_{FB2} = 2M\Omega$



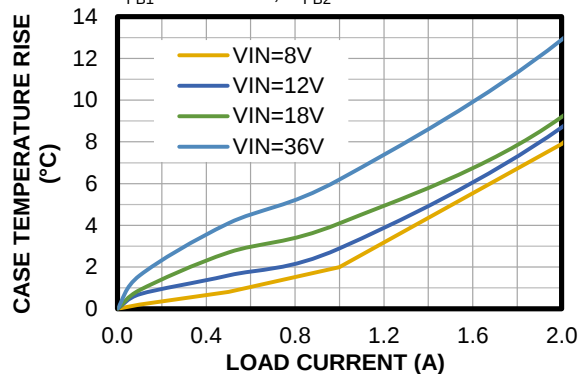
## Line Regulation

FCCM,  $R_{FB1} = 14.67M\Omega$ ,  $R_{FB2} = 2M\Omega$



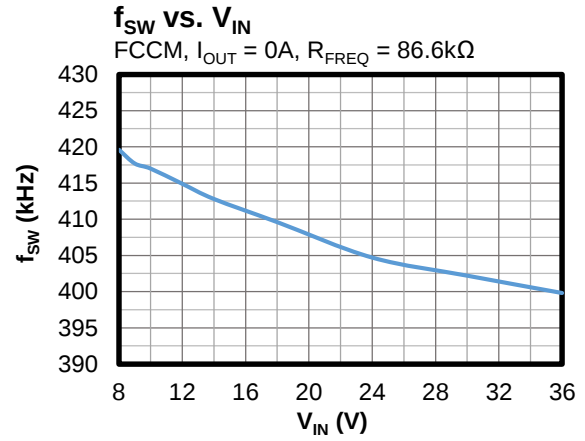
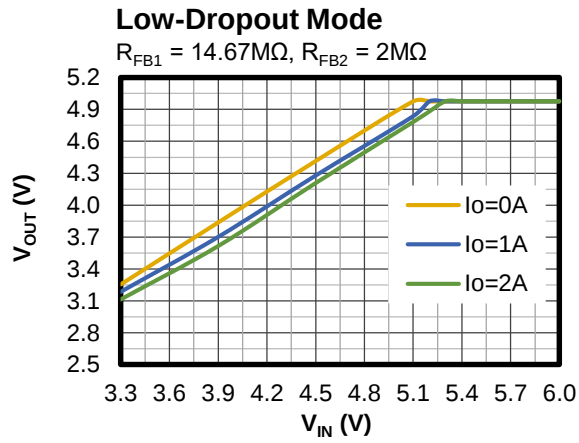
## Case Temperature Rise

$R_{FB1} = 14.67M\Omega$ ,  $R_{FB2} = 2M\Omega$



## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN} = 12V$ ,  $V_{OUT} = 5V$ ,  $L = 10\mu H$  (DCR = 27m $\Omega$ ),  $f_{SW} = 410kHz$ , AAM mode,  $T_A = 25^\circ C$ , unless otherwise noted.

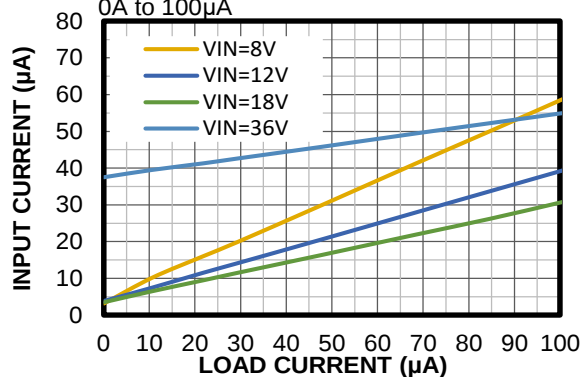


# TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN} = 12V$ ,  $V_{OUT} = 3.3V$ ,  $L = 2.2\mu H$  (DCR = 22.1m $\Omega$ ),  $f_{SW} = 2.2MHz$ , AAM mode,  $T_A = 25^\circ C$ , unless otherwise noted.

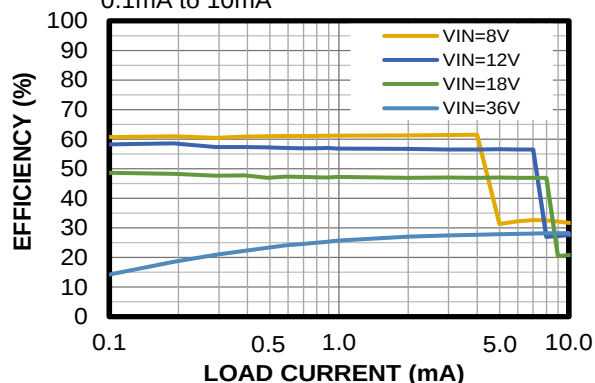
## Input Current vs. Load Current

AAM mode,  $R_{FB1} = 9M\Omega$ ,  $R_{FB2} = 2M\Omega$ ,  
0A to 100 $\mu A$



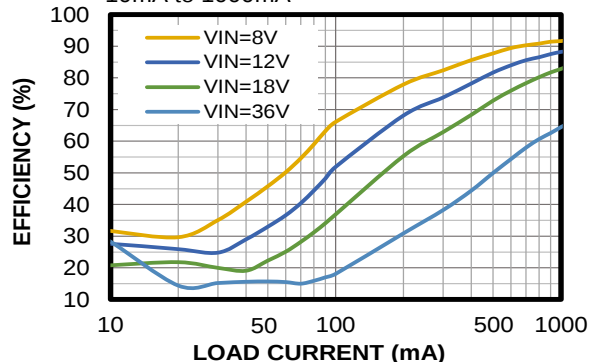
## Efficiency vs. Load Current

AAM mode,  $R_{FB1} = 9M\Omega$ ,  $R_{FB2} = 2M\Omega$ ,  
0.1mA to 10mA



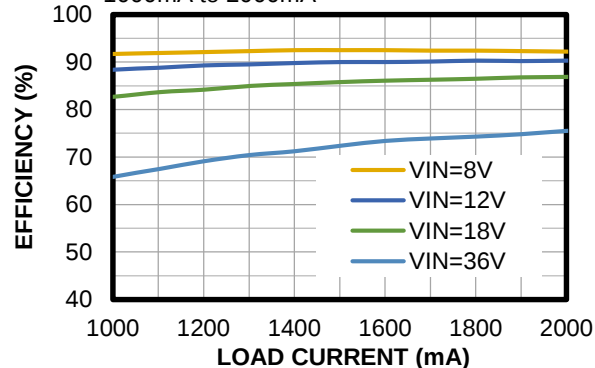
## Efficiency vs. Load Current

AAM mode,  $R_{FB1} = 9M\Omega$ ,  $R_{FB2} = 2M\Omega$ ,  
10mA to 1000mA



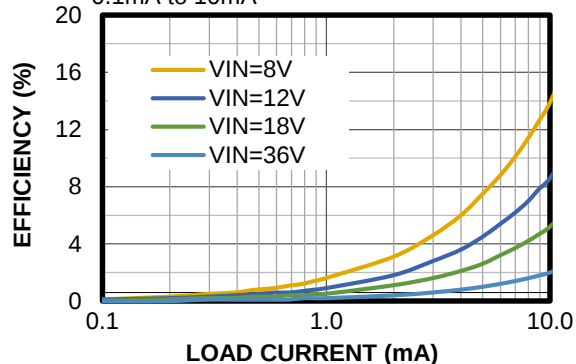
## Efficiency vs. Load Current

AAM mode,  $R_{FB1} = 9M\Omega$ ,  $R_{FB2} = 2M\Omega$ ,  
1000mA to 2000mA



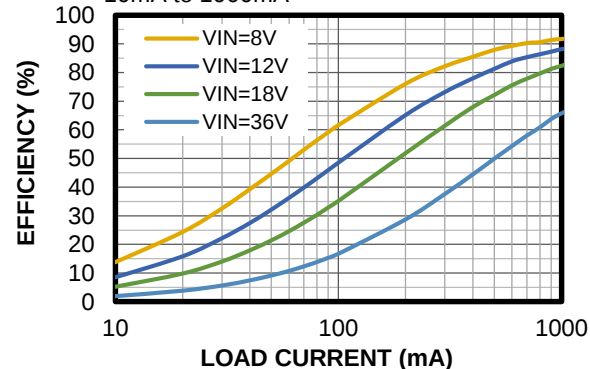
## Efficiency vs. Load Current

FCCM,  $R_{FB1} = 9M\Omega$ ,  $R_{FB2} = 2M\Omega$ ,  
0.1mA to 10mA



## Efficiency vs. Load Current

FCCM,  $R_{FB1} = 9M\Omega$ ,  $R_{FB2} = 2M\Omega$ ,  
10mA to 1000mA

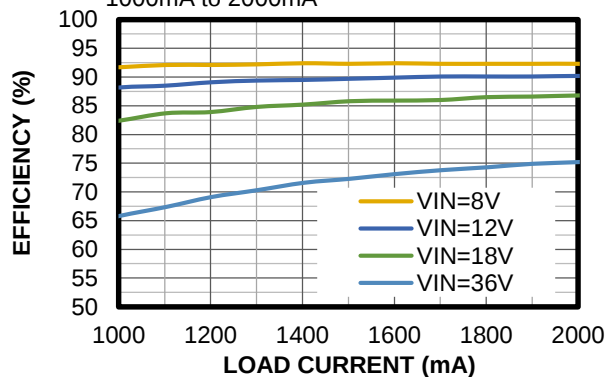


# TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN} = 12V$ ,  $V_{OUT} = 3.3V$ ,  $L = 2.2\mu H$  (DCR = 22.1m $\Omega$ ),  $f_{SW} = 2.2MHz$ , AAM mode,  $T_A = 25^\circ C$ , unless otherwise noted.

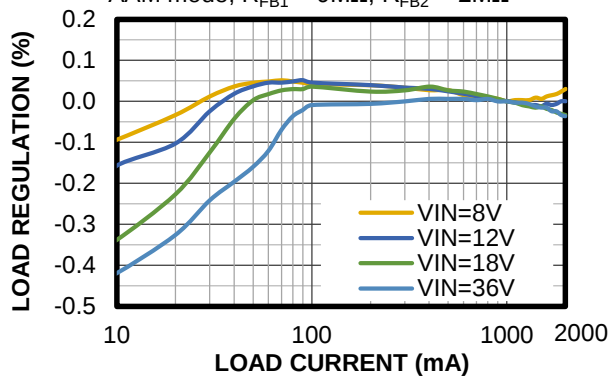
## Efficiency vs. Load Current

FCCM,  $R_{FB1} = 9M\Omega$ ,  $R_{FB2} = 2M\Omega$ ,  
1000mA to 2000mA



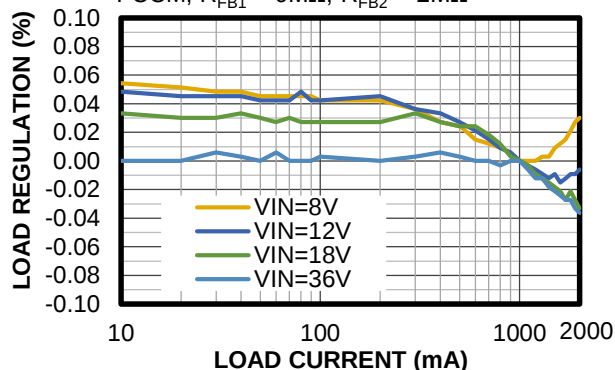
## Load Regulation

AAM mode,  $R_{FB1} = 9M\Omega$ ,  $R_{FB2} = 2M\Omega$



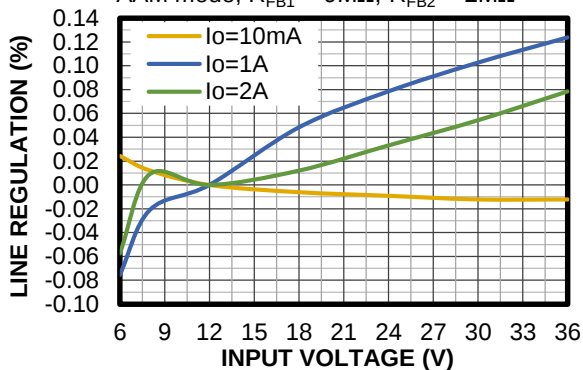
## Load Regulation

FCCM,  $R_{FB1} = 9M\Omega$ ,  $R_{FB2} = 2M\Omega$



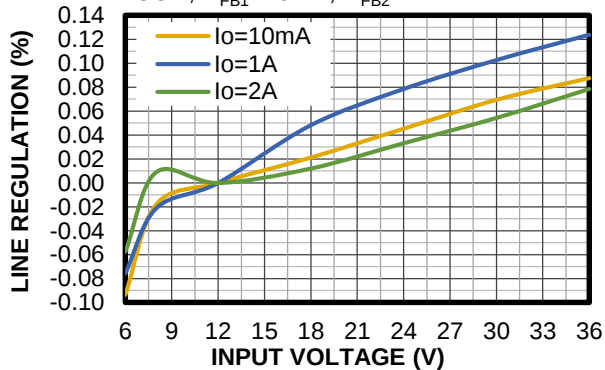
## Line Regulation

AAM mode,  $R_{FB1} = 9M\Omega$ ,  $R_{FB2} = 2M\Omega$



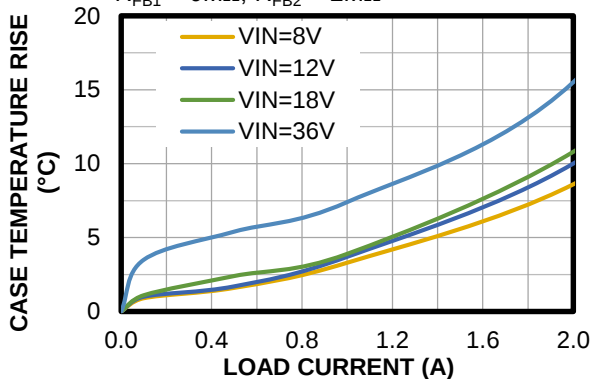
## Line Regulation

FCCM,  $R_{FB1} = 9M\Omega$ ,  $R_{FB2} = 2M\Omega$



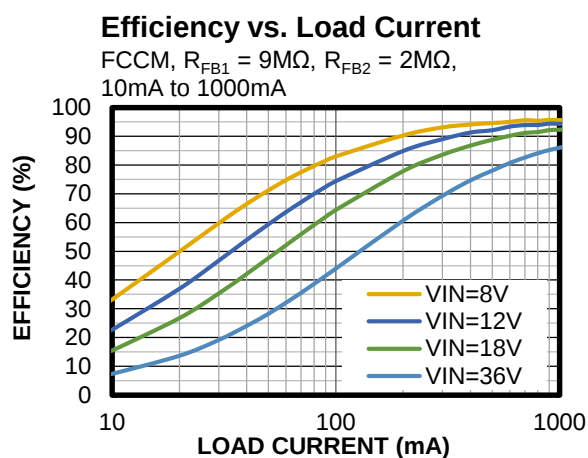
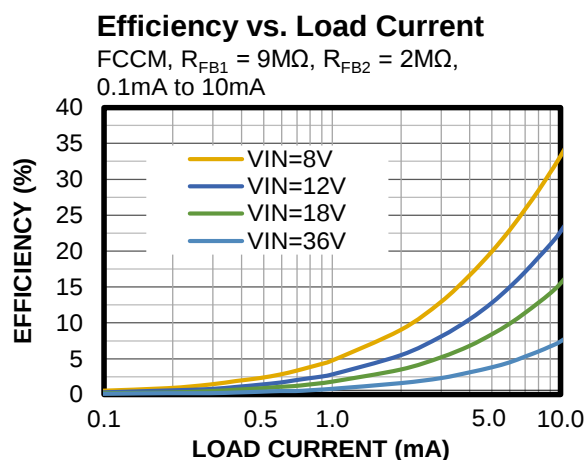
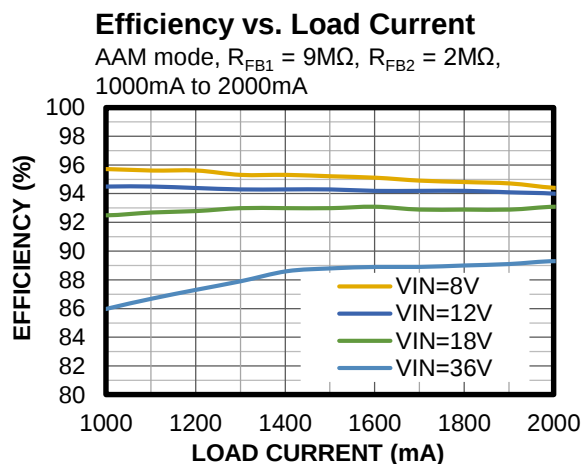
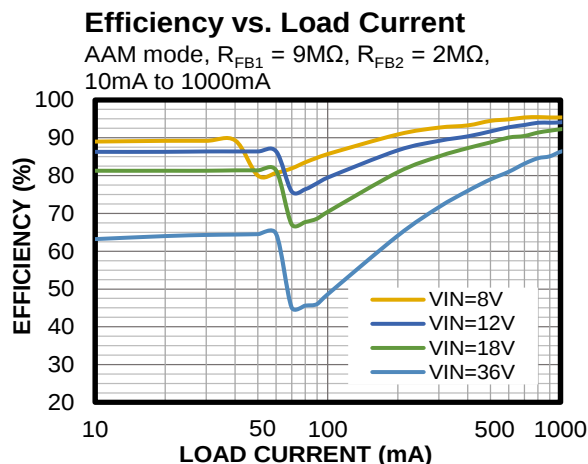
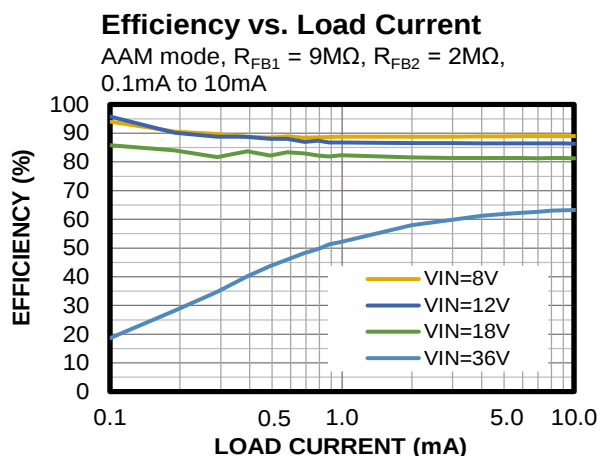
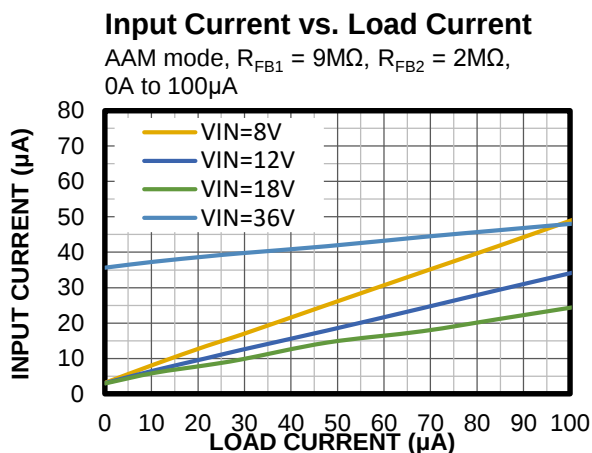
## Case Temperature Rise

$R_{FB1} = 9M\Omega$ ,  $R_{FB2} = 2M\Omega$



# TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN} = 12V$ ,  $V_{OUT} = 3.3V$ ,  $L = 10\mu H$  (DCR = 27m $\Omega$ ),  $f_{SW} = 410kHz$ , AAM mode,  $T_A = 25^\circ C$ , unless otherwise noted.

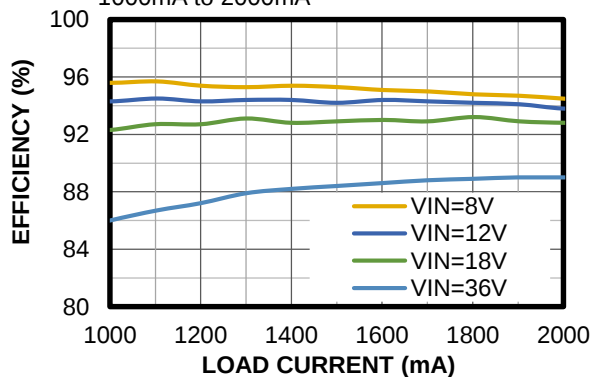


# TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN} = 12V$ ,  $V_{OUT} = 3.3V$ ,  $L = 10\mu H$  (DCR = 27m $\Omega$ ),  $f_{SW} = 410kHz$ , AAM mode,  $T_A = 25^\circ C$ , unless otherwise noted.

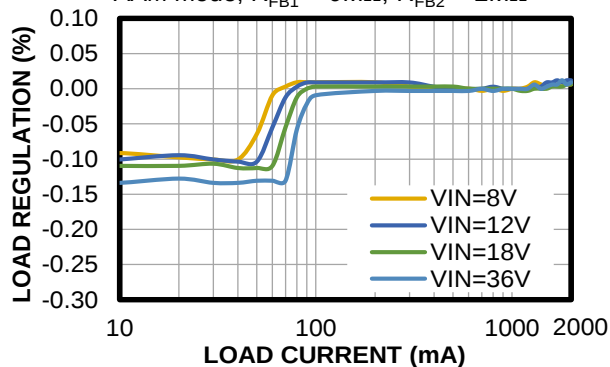
## Efficiency vs. Load Current

FCCM,  $R_{FB1} = 9M\Omega$ ,  $R_{FB2} = 2M\Omega$ ,  
1000mA to 2000mA



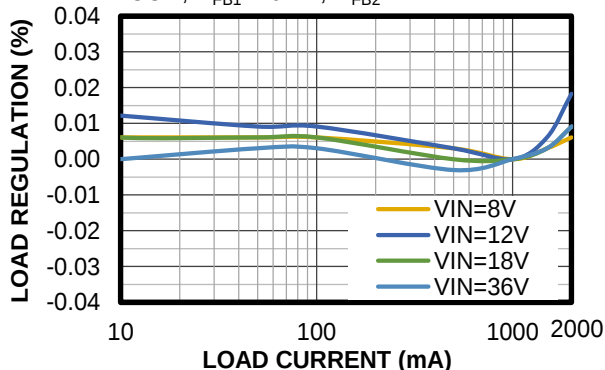
## Load Regulation

AAM mode,  $R_{FB1} = 9M\Omega$ ,  $R_{FB2} = 2M\Omega$



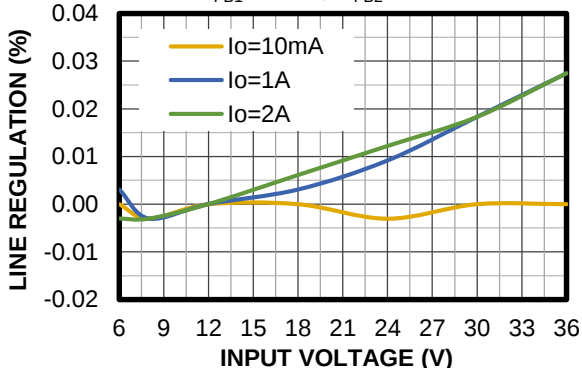
## Load Regulation

FCCM,  $R_{FB1} = 9M\Omega$ ,  $R_{FB2} = 2M\Omega$



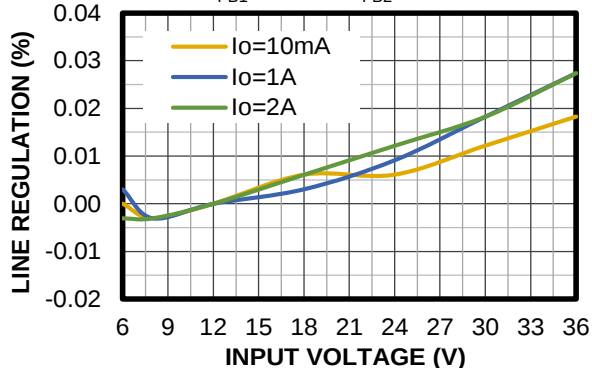
## Line Regulation

FCCM,  $R_{FB1} = 9M\Omega$ ,  $R_{FB2} = 2M\Omega$



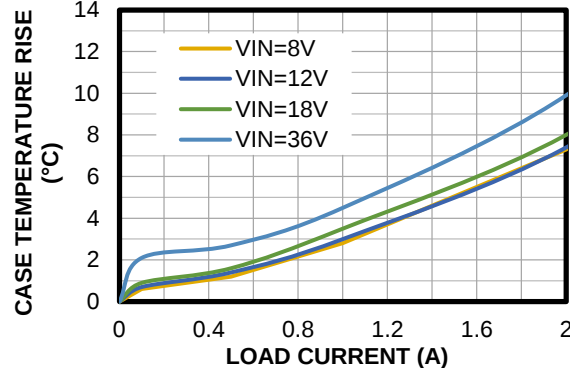
## Line Regulation

FCCM,  $R_{FB1} = 9M\Omega$ ,  $R_{FB2} = 2M\Omega$



## Case Temperature Rise

$R_{FB1} = 9M\Omega$ ,  $R_{FB2} = 2M\Omega$

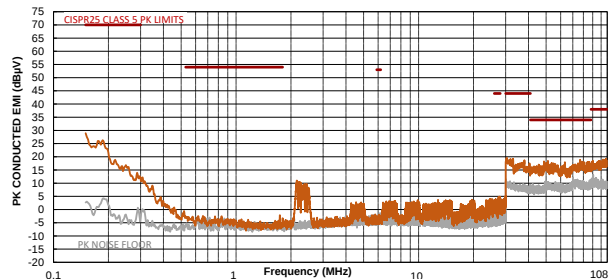


# TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN} = 12V$ ,  $V_{OUT} = 5V$ ,  $L = 2.2\mu H$  <sup>(10)</sup>,  $f_{SW} = 2.2MHz$ , AAM mode,  $T_A = 25^\circ C$ , unless otherwise noted. <sup>(11)</sup>

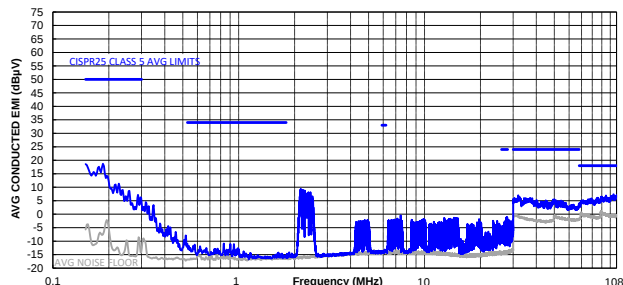
## CISPR25 Class 5 Peak Conducted Emissions

150kHz to 108MHz



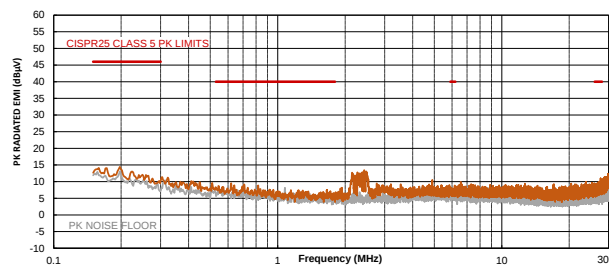
## CISPR25 Class 5 Average Conducted Emissions

150kHz to 108MHz



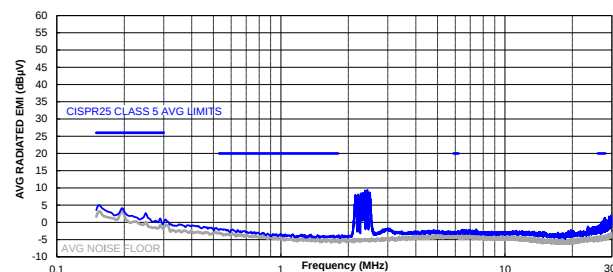
## CISPR25 Class 5 Peak Radiated Emissions

150kHz to 30MHz



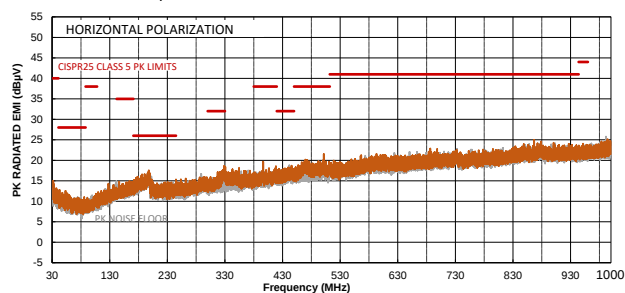
## CISPR25 Class 5 Average Radiated Emissions

150kHz to 30MHz



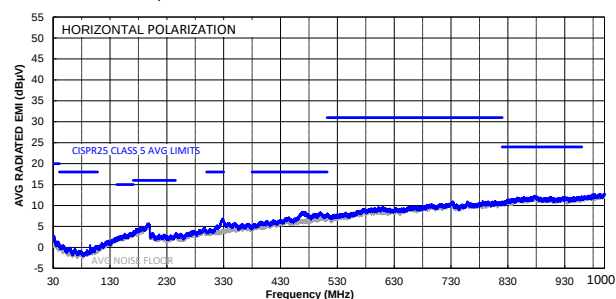
## CISPR25 Class 5 Peak Radiated Emissions

Horizontal, 30MHz to 1GHz



## CISPR25 Class 5 Average Radiated Emissions

Horizontal, 30MHz to 1GHz

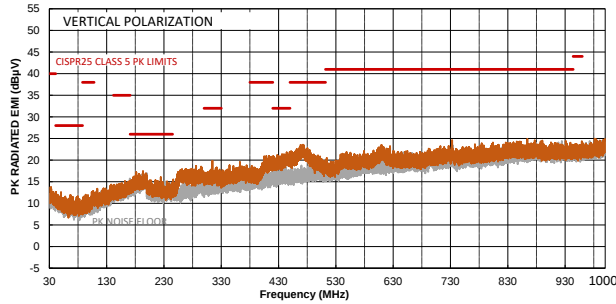


## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN} = 12V$ ,  $V_{OUT} = 5V$ ,  $L = 2.2\mu H$  <sup>(10)</sup>,  $f_{SW} = 2.2MHz$ , AAM mode,  $T_A = 25^\circ C$ , unless otherwise noted. <sup>(11)</sup>

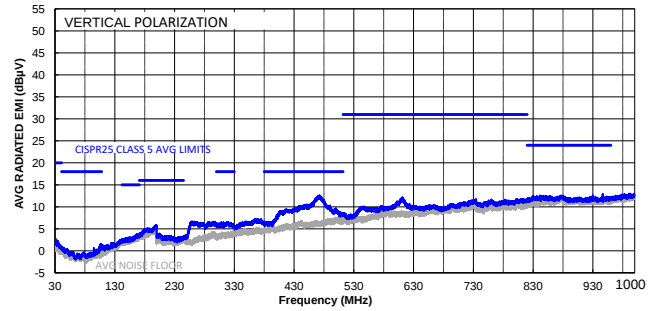
### CISPR25 Class 5 Peak Radiated Emissions

Vertical, 30MHz to 1GHz



### CISPR25 Class 5 Average Radiated Emissions

Vertical, 30MHz to 1GHz



#### Notes:

10) Inductor part number: XEL4030-222MEB/C. DCR = 22.1mΩ.

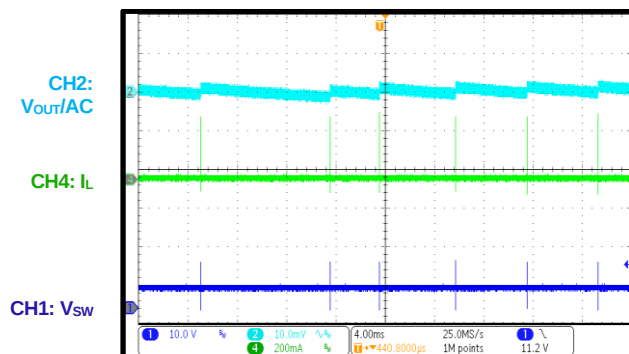
11) The EMC test results are based on the application circuit with EMI filters (see Figure 13 on page 43).

# TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN} = 12V$ ,  $V_{OUT} = 5V$ ,  $L = 2.2\mu H$ ,  $f_{SW} = 2.2MHz$ , AAM mode,  $T_A = 25^\circ C$ , unless otherwise noted.

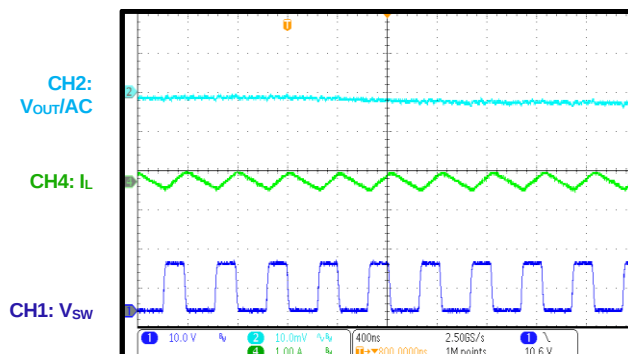
## Steady State

$I_{OUT} = 0A$ , AAM mode



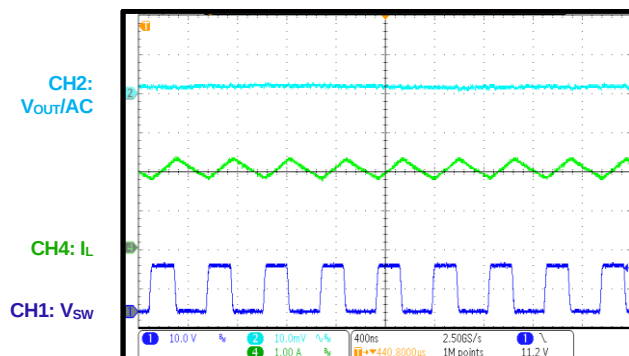
## Steady State

$I_{OUT} = 0A$ , FCCM



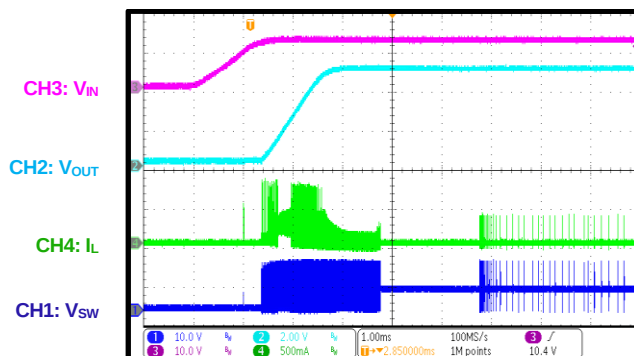
## Steady State

$I_{OUT} = 2A$



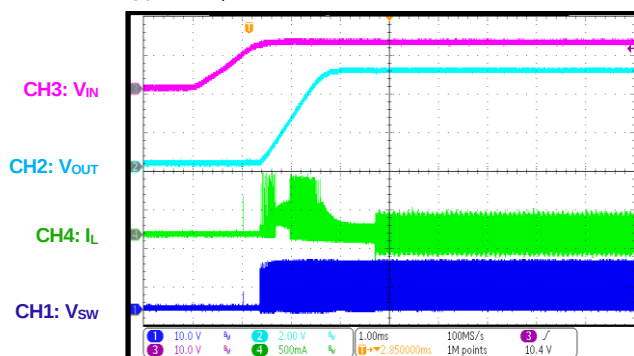
## Start-Up through VIN

$I_{OUT} = 0A$ , AAM mode



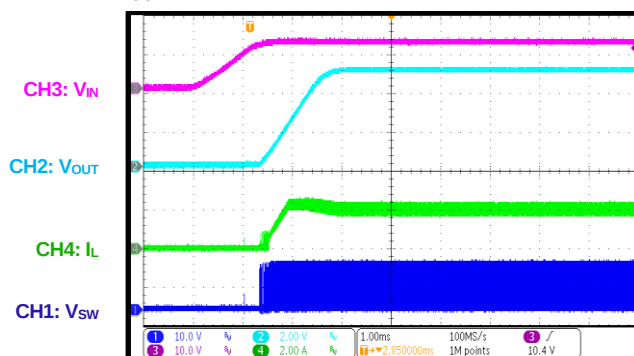
## Start-Up through VIN

$I_{OUT} = 0A$ , FCCM



## Start-Up through VIN

$I_{OUT} = 2A$

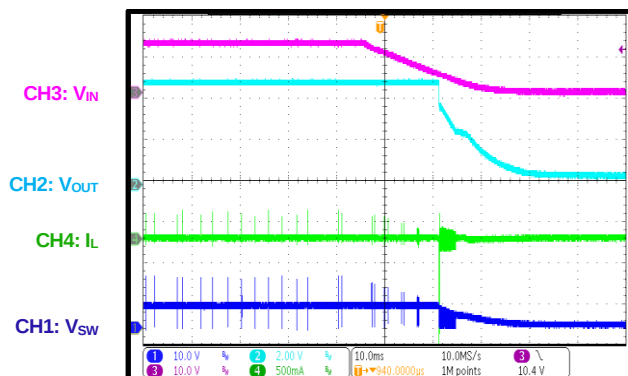


# TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN} = 12V$ ,  $V_{OUT} = 5V$ ,  $L = 2.2\mu H$ ,  $f_{SW} = 2.2MHz$ , AAM mode,  $T_A = 25^\circ C$ , unless otherwise noted.

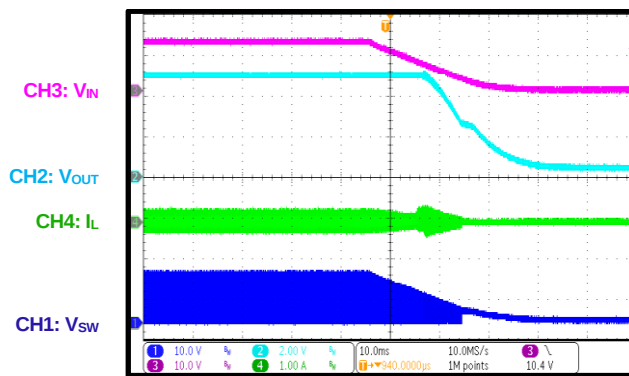
## Shutdown through VIN

$I_{OUT} = 0A$ , AAM mode



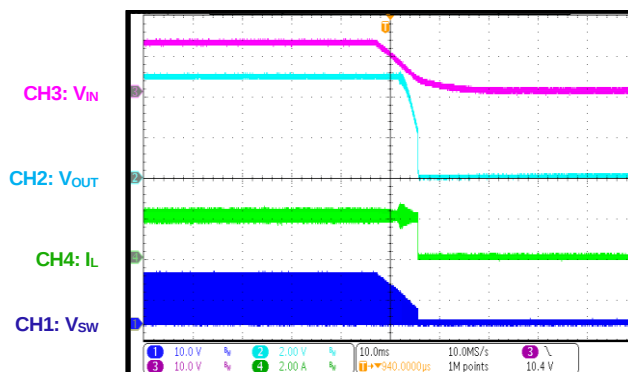
## Shutdown through VIN

$I_{OUT} = 0A$ , FCCM



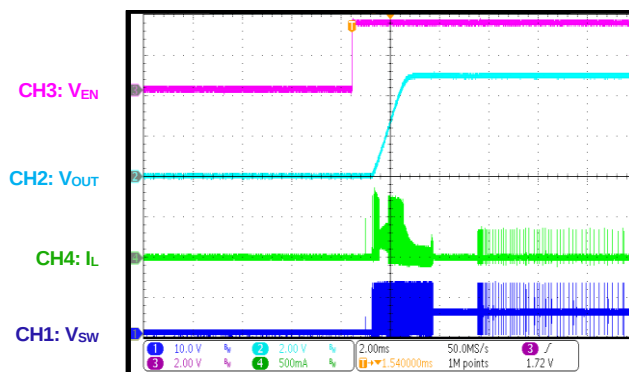
## Shutdown through VIN

$I_{OUT} = 2A$



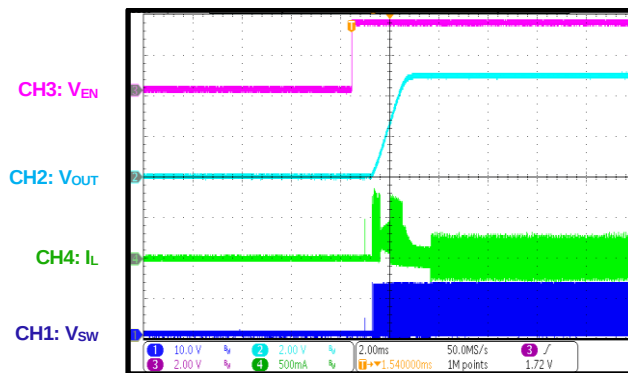
## Start-Up through EN

$I_{OUT} = 0A$ , AAM mode



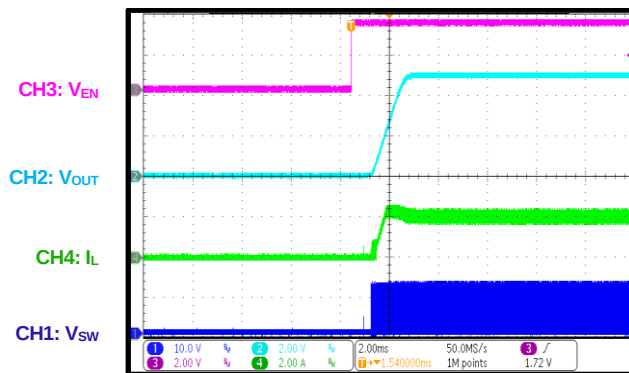
## Start-Up through EN

$I_{OUT} = 0A$ , FCCM



## Start-Up through EN

$I_{OUT} = 2A$

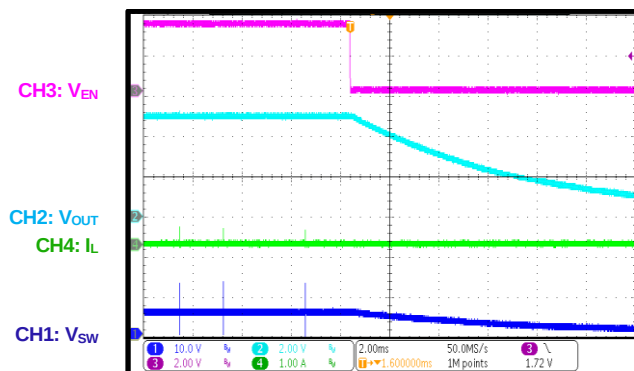


# TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN} = 12V$ ,  $V_{OUT} = 5V$ ,  $L = 2.2\mu H$ ,  $f_{SW} = 2.2MHz$ , AAM mode,  $T_A = 25^\circ C$ , unless otherwise noted.

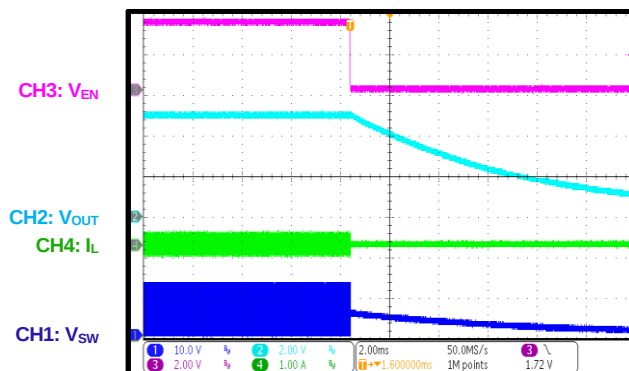
## Shutdown through EN

$I_{OUT} = 0A$ , AAM mode



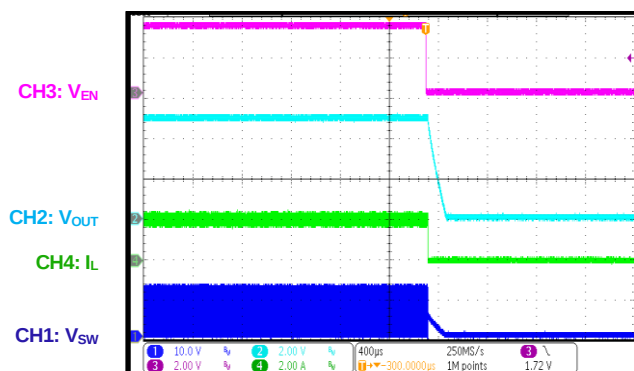
## Shutdown through EN

$I_{OUT} = 0A$ , FCCM



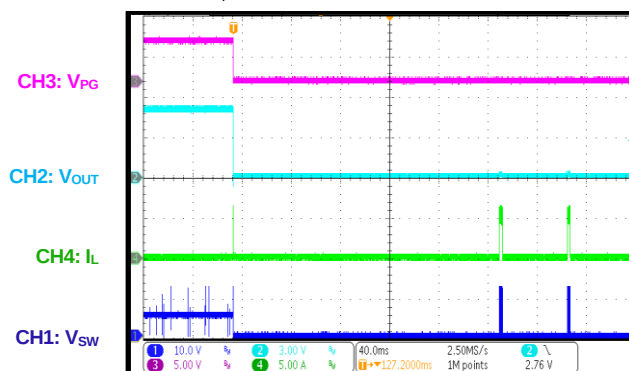
## Shutdown through EN

$I_{OUT} = 2A$



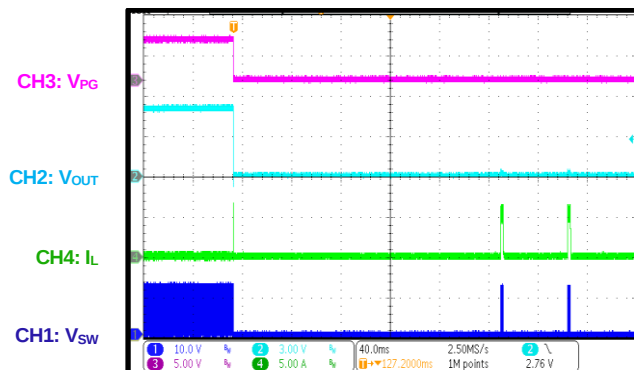
## SCP Entry

$I_{OUT} = 0A$ , AAM mode



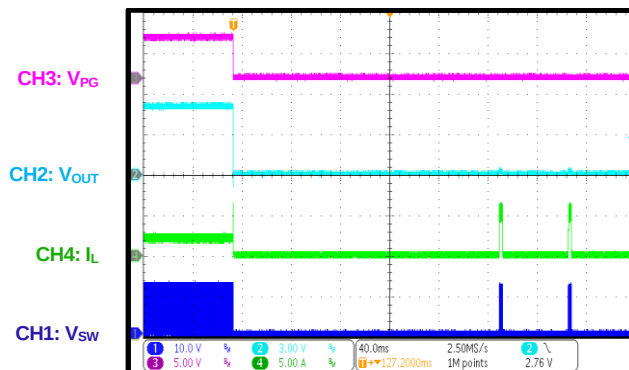
## SCP Entry

$I_{OUT} = 0A$ , FCCM



## SCP Entry

$I_{OUT} = 2A$

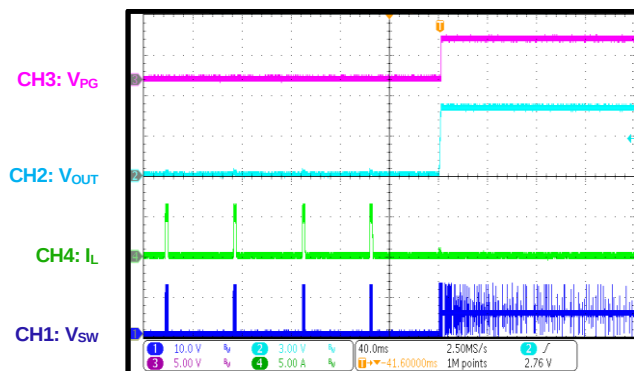


# TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN} = 12V$ ,  $V_{OUT} = 5V$ ,  $L = 2.2\mu H$ ,  $f_{SW} = 2.2MHz$ , AAM mode,  $T_A = 25^\circ C$ , unless otherwise noted.

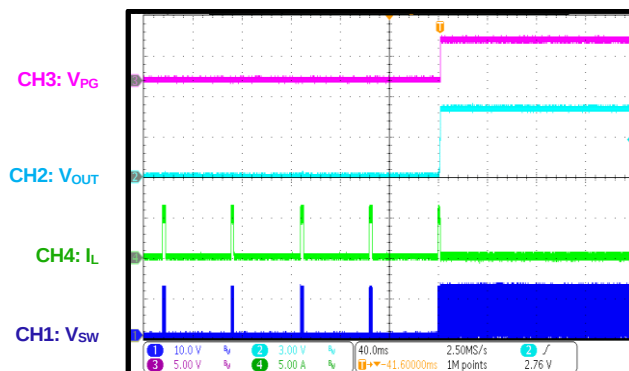
## SCP Recovery

$I_{OUT} = 0A$ , AAM mode



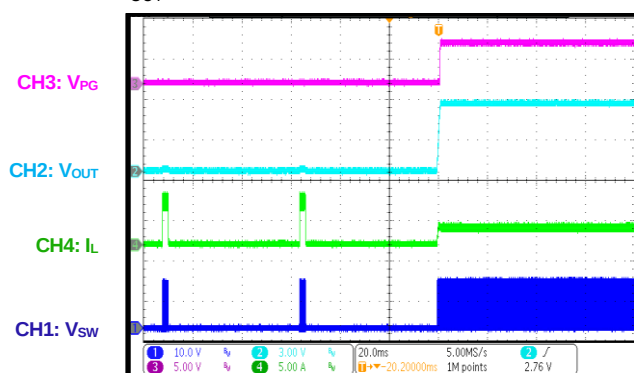
## SCP Recovery

$I_{OUT} = 0A$ , FCCM

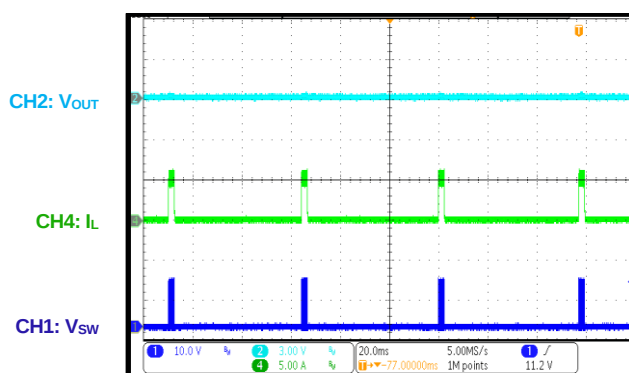


## SCP Recovery

$I_{OUT} = 2A$

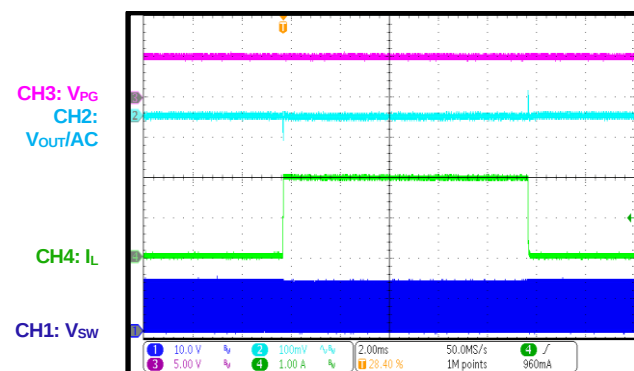


## SCP Steady State



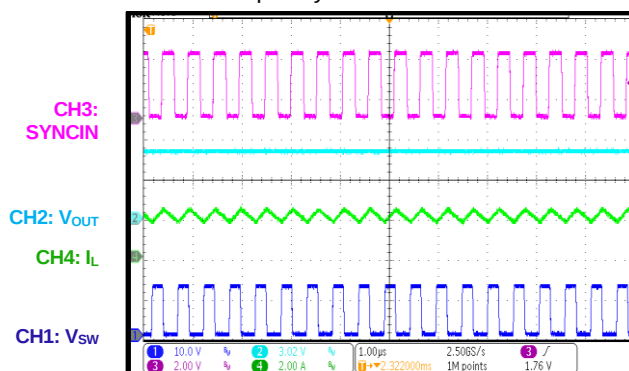
## Load Transient

$I_{OUT} = 0A$  to  $2A$ ,  $1.6A/\mu s$



## SYNCIN Operation

$I_{OUT} = 2A$ ,  $f_{SW} = 2.2MHz$ ,  
SYNCIN frequency =  $1.9MHz$

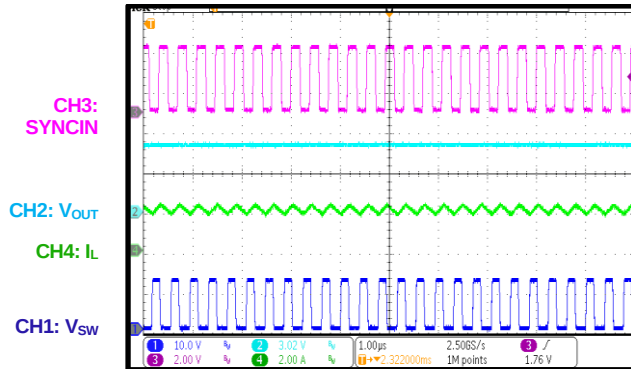


## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN} = 12V$ ,  $V_{OUT} = 5V$ ,  $L = 2.2\mu H$ ,  $f_{SW} = 2.2MHz$ , AAM mode,  $T_A = 25^\circ C$ , unless otherwise noted.

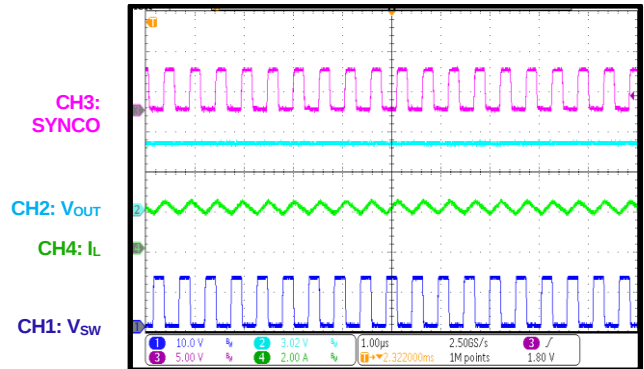
### SYNCIN Operation

$I_{OUT} = 2A$ ,  $f_{SW} = 2.2MHz$ ,  
SYNCIN frequency = 2.6MHz



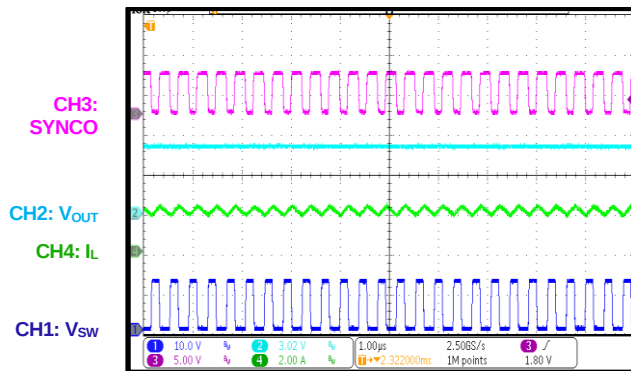
### SYNCO Operation

$I_{OUT} = 2A$ ,  $f_{SW} = 2.2MHz$ ,  
SYNCIN frequency = 1.9MHz



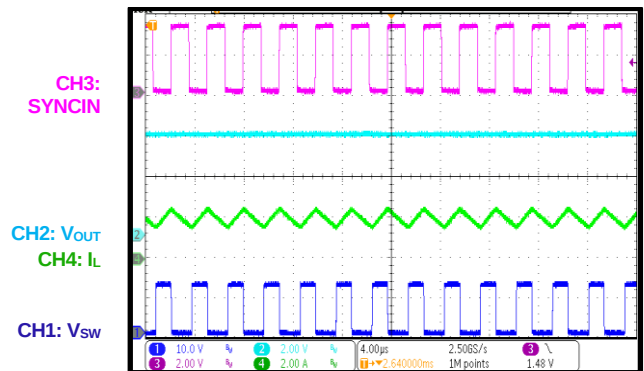
### SYNCO Operation

$I_{OUT} = 2A$ ,  $f_{SW} = 2.2MHz$ ,  
SYNCIN frequency = 2.6MHz



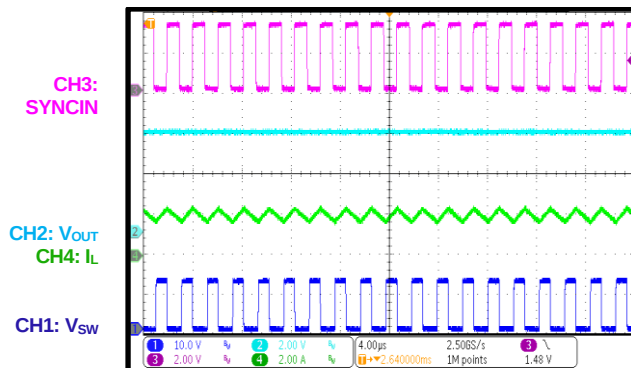
### SYNCIN Operation

$I_{OUT} = 2A$ ,  $f_{SW} = 410kHz$ ,  $L = 10\mu H$ ,  
SYNCIN frequency = 350kHz



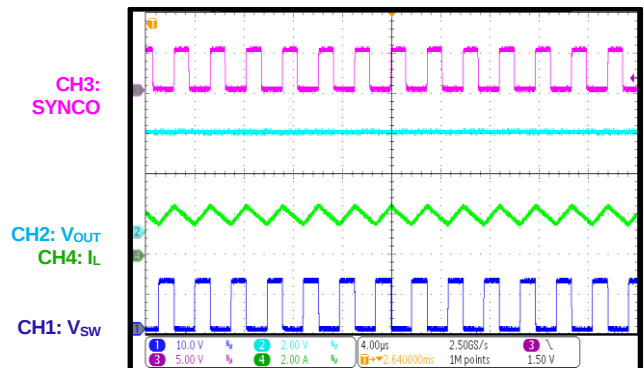
### SYNCIN Operation

$I_{OUT} = 2A$ ,  $f_{SW} = 410kHz$ ,  $L = 10\mu H$ ,  
SYNCIN frequency = 480kHz



### SYNCO Operation

$I_{OUT} = 2A$ ,  $f_{SW} = 410kHz$ ,  $L = 10\mu H$ ,  
SYNCIN frequency = 350kHz

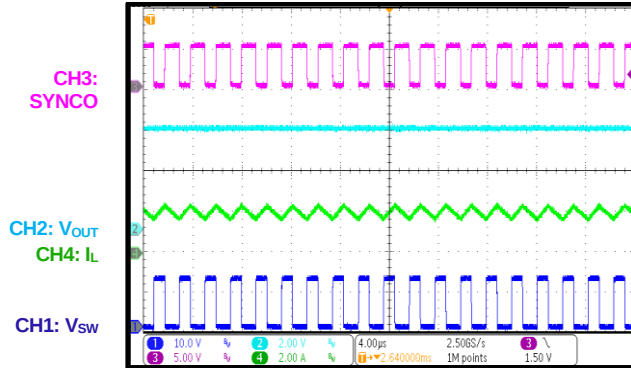


# TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN} = 12V$ ,  $V_{OUT} = 5V$ ,  $L = 2.2\mu H$ ,  $f_{SW} = 2.2MHz$ , AAM mode,  $T_A = 25^\circ C$ , unless otherwise noted.

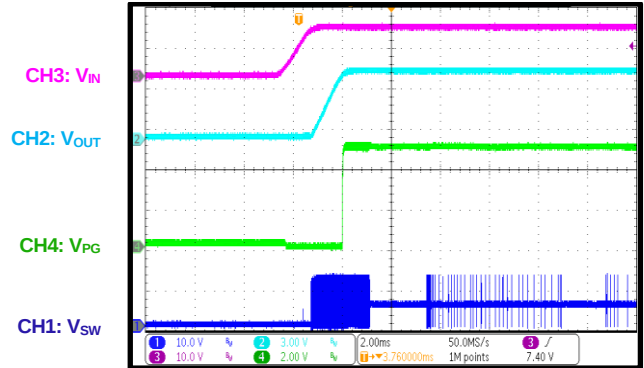
## SYNCO Operation

$I_{OUT} = 2A$ ,  $f_{SW} = 410kHz$ ,  $L = 10\mu H$ ,  
SYNCIN frequency = 480kHz



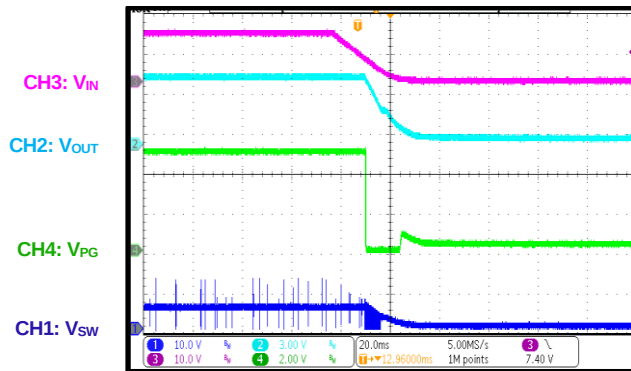
## PG Start-Up through VIN

$I_{OUT} = 0A$ , AAM mode



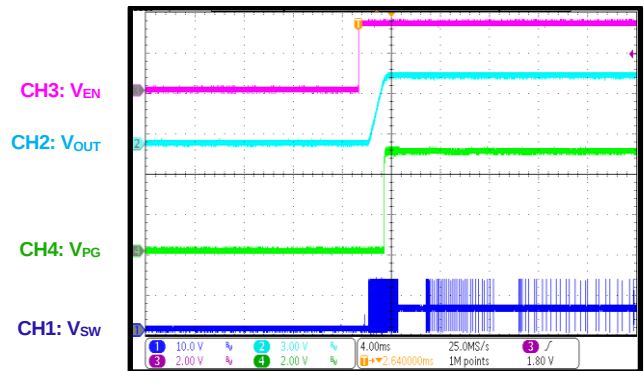
## PG Shutdown through VIN

$I_{OUT} = 0A$ , AAM mode



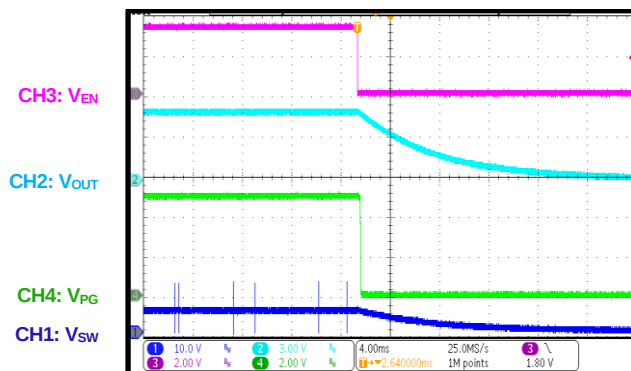
## PG Start-Up through EN

$I_{OUT} = 0A$ , AAM mode



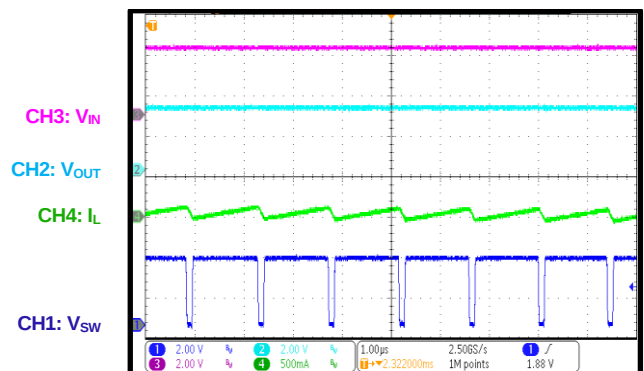
## PG Shutdown through EN

$I_{OUT} = 0A$ , AAM mode



## Low-Dropout Mode

$V_{IN} = 3.3V$ ,  $V_{OUT} = 5V$ ,  $I_{OUT} = 0A$

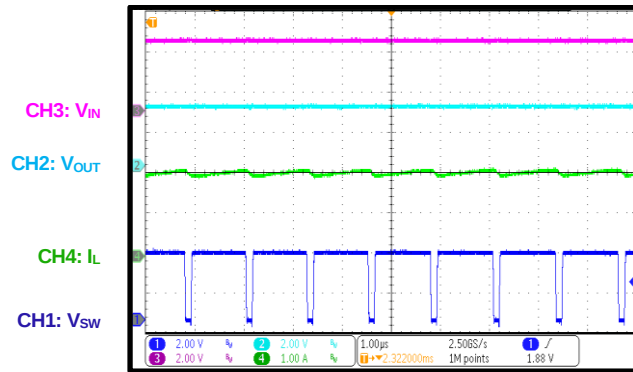


## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN} = 12V$ ,  $V_{OUT} = 5V$ ,  $L = 2.2\mu H$ ,  $f_{SW} = 2.2MHz$ , AAM mode,  $T_A = 25^\circ C$ , unless otherwise noted.

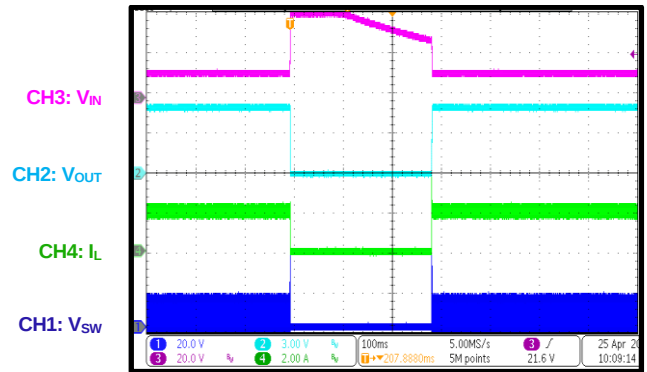
### Low-Dropout Mode

$V_{IN} = 3.3V$ ,  $V_{OUT} = 5V$ ,  $I_{OUT} = 2A$



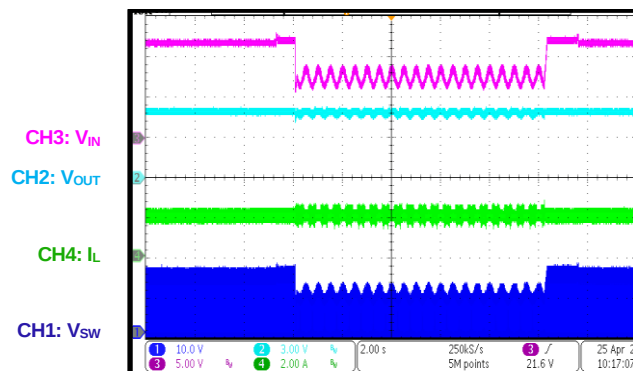
### Load Dump

$V_{IN} = 12V$  to  $42V$ ,  $I_{OUT} = 2A$



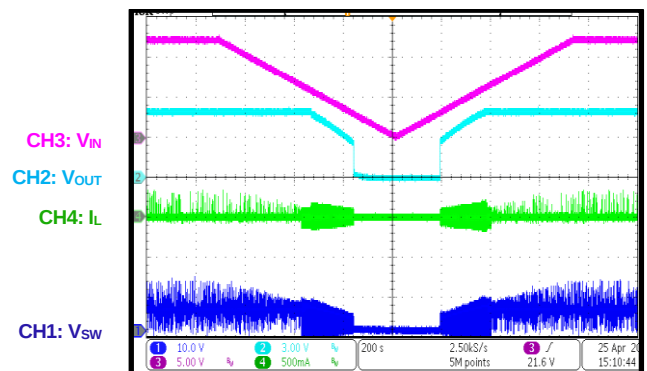
### Cold Crank

$I_{OUT} = 2A$



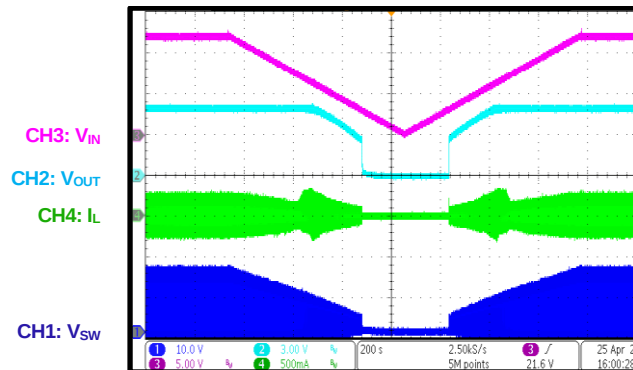
### $V_{IN}$ Ramping Up and Down

$I_{OUT} = 0A$ , AAM mode



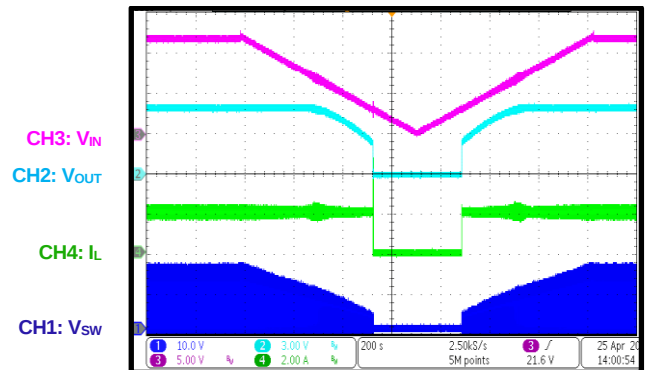
### $V_{IN}$ Ramping Up and Down

$I_{OUT} = 0A$ , FCCM



### $V_{IN}$ Ramping Up and Down

$I_{OUT} = 2A$



## FUNCTIONAL BLOCK DIAGRAM

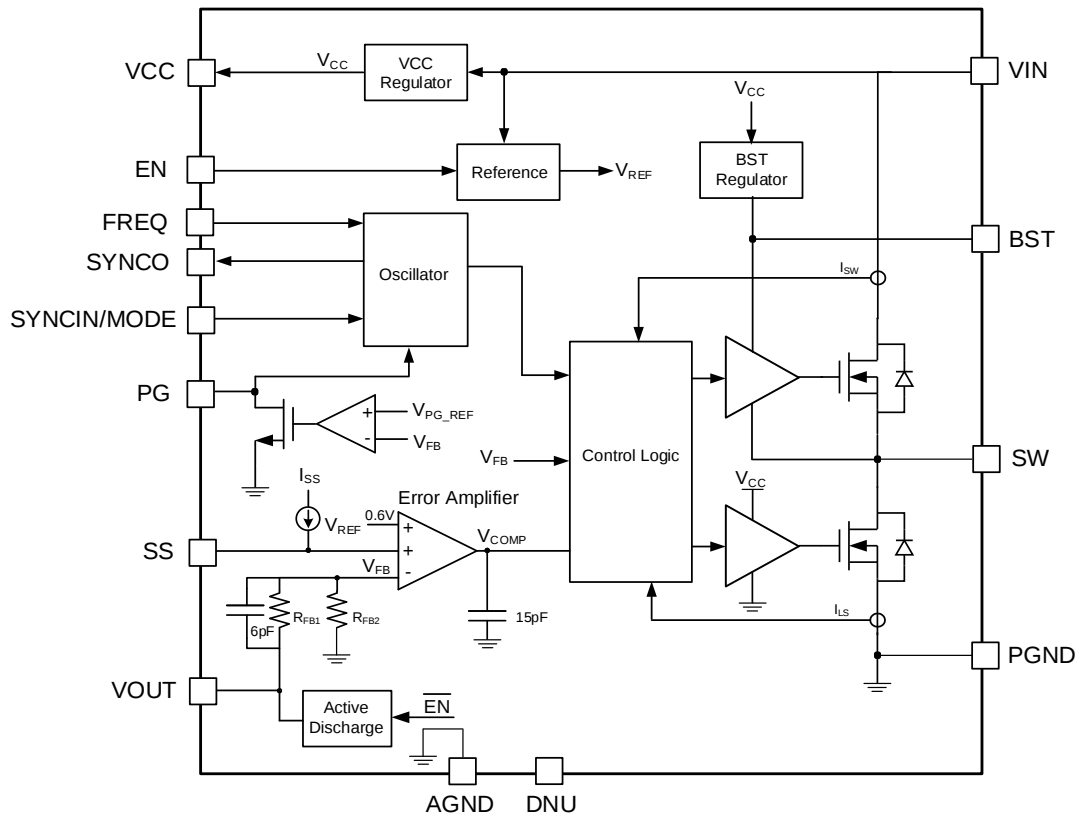


Figure 1: Functional Block Diagram

## OPERATION

The MPQ4345/4345J is a synchronous, step-down switching regulator with an integrated internal high-side MOSFET (HS-FET) and low-side MOSFET (LS-FET). It provides up to 2A of highly efficient output current ( $I_{OUT}$ ) with fixed-frequency, zero-delay pulse-width modulation (PWM) control.

The MPQ4345/4345J features a wide input voltage ( $V_{IN}$ ) range, configurable 350kHz to 2.5MHz switching frequency ( $f_{SW}$ ), external soft start (SS), and precision current limit. Its very low operational quiescent current ( $I_Q$ ) makes the MPQ4345/4345J well-suited for battery-powered applications.

### Zero-Delay Pulse-Width Modulation (PWM) Control

Automotive applications typically require fixed-frequency operation to reduce EMI, but traditional fixed-frequency control topologies have major limitations. Voltage mode is difficult to compensate for in automotive environments, while peak current mode control cannot always keep up with stringent, modern system-on-chip (SoC) transient requirements without excessive output capacitance. With these requirements in mind, the MPQ4345/4345J introduces fixed-frequency, zero-delay PWM control.

Zero-delay PWM control combines current information with hysteretic-style output voltage ( $V_{OUT}$ ) control in a clocked system. This provides a near optimal transient response while maintaining a high phase margin across a wide variety of operating conditions and external component values. In addition, zero-delay PWM control maintains superior EMI performance. The improved transient response reduces output capacitor requirements and lowers the system cost. Trailing-edge modulation facilitates a narrow minimum on time ( $t_{ON\_MIN}$ ) for high conversion ratio applications.

At the beginning of the PWM cycle, the HS-FET turns off and the LS-FET turns on immediately, then remains on until the control signal reaches the COMP voltage ( $V_{COMP}$ ). HS-FET remains off for at least 120ns at the beginning of the cycle.

### Light-Load Operation

At moderate-to-high output currents, the MPQ4345/4345J operates at a fixed frequency. Under light-load conditions, the MPQ4345/4345J can work in two different operation modes by setting the state of the SYNCIN/MODE pin.

If the SYNCIN/MODE pin is pulled above 1.8V or an external clock is used, then the MPQ4345/4345J works in forced continuous conduction mode (FCCM). In FCCM, the device works with a fixed frequency from no-load to full-load conditions. The part has a -4A reverse current limit to prevent the negative current from dropping too low and potentially damaging the components. Once the negative inductor current ( $I_L$ ) reaches the reverse current limit, the LS-FET immediately turns off and the HS-FET turns on. The advantage of FCCM is the constant frequency and lower output ripple under light loads.

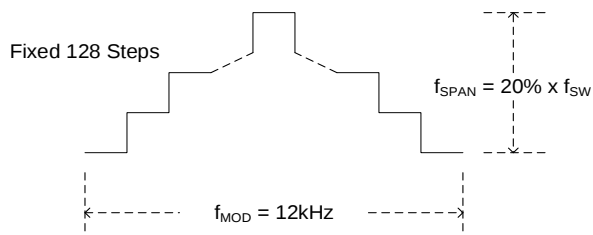
If the SYNCIN/MODE pin is pulled below 0.4V, then the MPQ4345/4345J works in advanced asynchronous modulation (AAM) mode. The device cannot enter AAM mode until SS completes. AAM mode optimizes efficiency under light-load and no-load conditions.

During AAM mode, the LS-FET emulates a diode, and the HS-FET has a fixed one-shot on time to charge the inductor and regulate the output. As the load decreases, the interval between one-shots increases. When this interval exceeds 8 $\mu$ s, the part enters sleep mode, which turns off some internal circuits and extends the on time to achieve an ultra-low  $I_Q$ .

When the load increases, and the interval decreases to be shorter than 6 $\mu$ s, the part exits sleep mode and enters AAM mode again. In AAM mode, the device employs a zero-current detection (ZCD) circuit to turn off the LS-FET and prevent negative  $I_L$  flow under light loads. The device exits AAM mode if the MODE pin goes high. If a fault occurs in sleep mode, such as an over-voltage (OV) or over-temperature (OT) fault, the internal circuits are not disabled.

## Frequency Spread Spectrum (FSS)

The MPQ4345/4345J uses a 12kHz modulation frequency with a fixed, 128-step triangular profile to spread the internal  $f_{SW}$  across a 20% ( $\pm 10\%$ ) window. The absolute frequency step size varies proportionally with  $f_{SW}$  to maintain the  $\pm 10\%$  frequency spread (see Figure 2).



**Figure 2: Frequency Spread Spectrum**

Sidebands are created by modulating  $f_{SW}$  with the triangle modulation waveform. The emission power of the fundamental  $f_{SW}$  and its harmonics is distributed into smaller pieces. This significantly reduces peak EMI noise.

## Low-Dropout (LDO) Mode

When  $V_{IN}$  drops to about 7V, the MPQ4345/4345J folds back the frequency. Once  $V_{IN}$  is almost equal to  $V_{OUT}$ , the device enters low-dropout (LDO) mode. This allows for a shorter off time to achieve higher duty cycle.

The effective duty cycle during the regulator's dropout period is mainly influenced by the voltage drops across the power MOSFET, the inductor resistance, the LS-FET diode, and the PCB resistance.

## Start-Up and Shutdown

If both  $V_{IN}$  and EN exceed their respective thresholds, the device starts up. The reference block starts first, generating a stable reference voltage and currents, and then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuitries.

While the internal supply rail is up, an internal timer holds the power MOSFET off for about 50 $\mu$ s to blank any start-up glitches. When the SS block is enabled, it first holds its SS output low to ensure the remaining circuits are ready. Then the SS block slowly ramps up.

Three events shut down the chip: EN going low,  $V_{IN}$  going low, and thermal shutdown. During shutdown, the signaling path is blocked first to avoid any fault triggering. Then  $V_{COMP}$  and the internal supply rail are pulled down. The floating driver is not subject to this shutdown command, but its charging path is disabled.

## SYNCIN and SYNCO

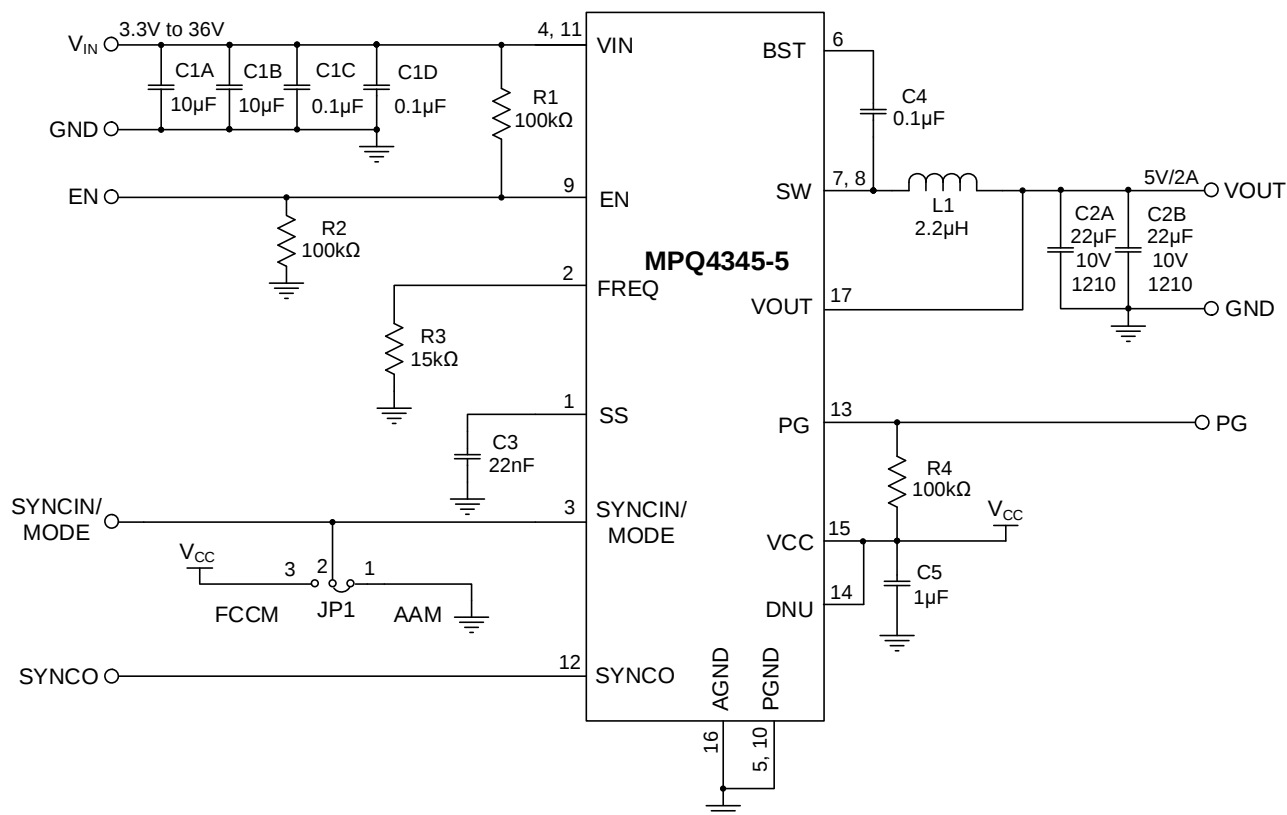
$f_{SW}$  can be synchronized to the rising edge of a clock signal applied to the SYNCIN/MODE pin. The recommended SYNCIN frequency range is 90% to 115% of  $f_{SW}$ .

The SYNCO pin can output a clock signal in phase with the internal oscillator signal (inverter to switching clock) or the external SYNCIN frequency.

## Thermal Shutdown

Thermal shutdown is implemented to prevent the chip from thermal runaway. If the silicon die temperature exceeds its upper 170°C threshold, the power MOSFETs shut down. Once the temperature drops below its lower threshold (150°C), the thermal shutdown condition is removed and the chip starts up again.

## APPLICATION INFORMATION



**Figure 3: Typical Application Circuit for the MPQ4345GLE-5 ( $V_{OUT} = 5V$ ,  $f_{sw} = 2.2MHz$ )**

**Table 1: Design Guide Index**

| Pin # | Pin Name    | Component          | Design Guide Index                                                         |
|-------|-------------|--------------------|----------------------------------------------------------------------------|
| 1     | SS          | C3                 | Selecting the Soft-Start Capacitor (SS, Pin 1)                             |
| 2     | FREQ        | R3                 | Setting the Switching Frequency ( $f_{sw}$ ) (FREQ, Pin 2)                 |
| 3     | SYNCIN/MODE | -                  | SYNC Input and MODE Selection (SYNCIN/MODE, Pin 3)                         |
| 4, 11 | VIN         | C1A, C1B, C1C, C1D | Selecting the Input Capacitors (VIN, Pins 4 and 11)                        |
| 5, 10 | PGND        | -                  | Connection to GND (GND, Pins 5, 10, and 16)                                |
| 6     | BST         | C4                 | Bootstrap Charging (BST, Pin 6)                                            |
| 7,8   | SW          | L1, C2A, C2B       | Selecting the Inductor; Selecting the Output Capacitors (SW, Pins 7 and 8) |
| 9     | EN          | R1, R2             | Enable (EN, Pin 9) and $V_{IN}$ Under-Voltage Lockout (UVLO)               |
| 12    | SYNCO       | -                  | SYNCO (Pin 12)                                                             |
| 13    | PG          | R4                 | Power Good (PG) Indicator (PG, Pin 13)                                     |
| 14    | DNU         | -                  | DNU (Pin 14)                                                               |
| 15    | VCC         | C5                 | Input Bias Supply (VCC, Pin 15)                                            |
| 16    | AGND        | -                  | Connection to GND (GND, Pins 5,10, and 16)                                 |
| 17    | VOUT        | -                  | VOUT (Pin 17)                                                              |

### Selecting the Soft-Start Capacitor (SS, Pin 1)

Soft start (SS) is implemented to prevent the converter's V<sub>OUT</sub> from overshooting during start-up.

When SS begins, an internal current source begins charging the external SS capacitor (C<sub>SS</sub>). When the SS voltage (V<sub>SS</sub>) is below the internal reference voltage (V<sub>REF</sub>), V<sub>SS</sub> overrides V<sub>REF</sub>, so the error amplifier (EA) uses V<sub>SS</sub> as the reference. When V<sub>SS</sub> exceeds V<sub>REF</sub>, V<sub>REF</sub> regains control.

C<sub>SS</sub> can be calculated with Equation (1):

$$C_{SS}(\text{nF}) = \frac{t_{SS}(\text{ms}) \times I_{SS}(\mu\text{A})}{V_{REF}(\text{V})} = 16.6 \times t_{SS}(\text{ms}) \quad (1)$$

The SS pin can be used for tracking and sequencing.

### Setting the Switching Frequency (f<sub>sw</sub>) (FREQ, Pin 2)

f<sub>sw</sub> can be configured by an external resistor connected from the FREQ pin to ground, placed as close to the device as possible.

The resistance that sets f<sub>sw</sub> (R<sub>3</sub>) can be selected using the f<sub>sw</sub> vs R<sub>FREQ</sub> curves. Figure 4 shows the f<sub>sw</sub> vs. R<sub>FREQ</sub> curve when f<sub>sw</sub> is between 1000kHz and 2500kHz.

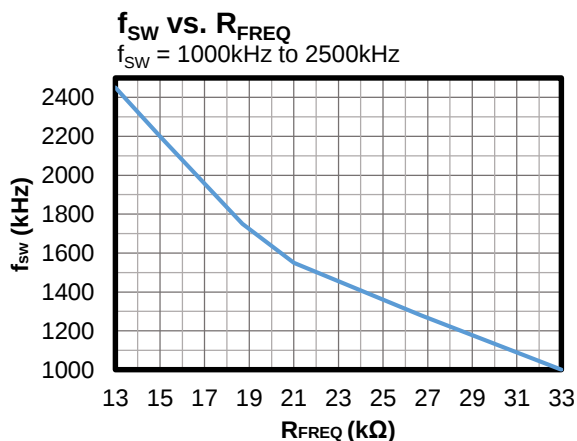


Figure 4: f<sub>sw</sub> vs. R<sub>FREQ</sub>

Figure 5 shows the f<sub>sw</sub> vs. R<sub>FREQ</sub> curve when f<sub>sw</sub> is between 350kHz and 1000kHz.

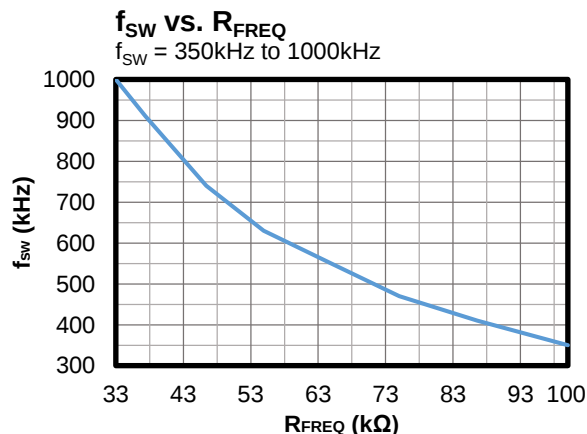


Figure 5: f<sub>sw</sub> vs. R<sub>FREQ</sub>

Table 2 shows some common f<sub>sw</sub> and R<sub>FREQ</sub> values when selecting f<sub>sw</sub>.

Table 2: f<sub>sw</sub> vs. R<sub>FREQ</sub>

| R <sub>FREQ</sub> (kΩ) | f <sub>sw</sub> (kHz) |
|------------------------|-----------------------|
| 100                    | 350                   |
| 86.6                   | 410                   |
| 75                     | 470                   |
| 64.9                   | 550                   |
| 54.9                   | 630                   |
| 46.4                   | 740                   |
| 37.4                   | 910                   |
| 33                     | 1050                  |
| 26.7                   | 1280                  |
| 21                     | 1550                  |
| 18.7                   | 1750                  |
| 15                     | 2200                  |
| 13                     | 2450                  |

### SYNC Input and MODE Selection (SYNCIN/MODE, Pin 3)

When the SYNCIN/MODE pin is used as the SYNC input pin (SYNCIN), f<sub>sw</sub> can be synchronized to the rising edge of a clock signal applied to SYNCIN/MODE. The recommended SYNCIN frequency range is 90% to 115% of f<sub>sw</sub>.

When SYNCIN/MODE is used for mode selection (MODE), pulling this pin high allows the device to operate in FCCM, while pulling it low allows the device to operate in AAM mode (see Table 3 on page 37).

**Table 3: Mode Selection**

| SYNCIN/MODE Input | Operation Mode |
|-------------------|----------------|
| <0.4V             | AAM mode       |
| >1.8V             | FCCM           |
| External clock in | FCCM           |

### Selecting the Input Capacitor (V<sub>IN</sub>, Pins 4 and 11)

The step-down converter has a discontinuous input current, and requires a capacitor to supply AC current to the converter while maintaining the DC V<sub>IN</sub>. For the best performance, use low-ESR capacitors. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients.

For most applications, it is recommended to use a 4.7μF to 10μF capacitor. It is strongly recommended to use another, lower-value capacitor (e.g. 0.1μF) with a small package size (0603) to absorb high-frequency switching noise. Place the smaller capacitor as close to V<sub>IN</sub> and GND as possible.

Since the input capacitor (C<sub>IN</sub>) absorbs the input switching current, it requires an adequate ripple current rating. The RMS current for C<sub>IN</sub> (I<sub>CIN</sub>) can be estimated with Equation (2):

$$I_{CIN} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (2)$$

The worst-case condition occurs at V<sub>IN</sub> = 2 × V<sub>OUT</sub>, which can be calculated with Equation (3):

$$I_{CIN} = \frac{I_{LOAD}}{2} \quad (3)$$

For simplification, choose C<sub>IN</sub> with an RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, add a small, high-quality ceramic capacitor (e.g. 0.1μF) as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide a sufficient charge to prevent excessive voltage ripple at the input.

The input voltage ripple (ΔV<sub>IN</sub>) caused by the capacitance can be estimated with Equation (4):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (4)$$

### V<sub>IN</sub> Over-Voltage Protection (OVP)

The MPQ4345/4345J has a built-in V<sub>IN</sub> over-voltage protection (OVP) circuit. V<sub>IN</sub> OVP becomes active at 25V. When V<sub>IN</sub> exceeds the OVP threshold (typically 38V), the LS-FET turns on until I<sub>L</sub> is fully discharged, and then switching stops. When V<sub>IN</sub> drops to the OV falling threshold (typically 28V), and the hiccup restart delay time expires, the device completes a soft-start cycle and resumes normal regulation.

### Bootstrap Charging (BST, Pin 6)

The BST capacitor (C<sub>4</sub>) is recommended to be between 0.1μF and 0.22μF.

It is not recommended to place a resistor (R<sub>BST</sub>) in series with the BST capacitor (C<sub>BST</sub>) unless there is a strict EMI requirement. R<sub>BST</sub> helps enhance EMI performance and reduce voltage stress at high input voltages, but it also increases power consumption and reduces efficiency. When R<sub>BST</sub> is necessary, it should be below 10Ω.

C<sub>BST</sub> is charged and regulated to about 5V by the dedicated internal bootstrap regulator. When the voltage between the BST and SW nodes is below its regulation, an N-channel MOSFET pass transistor connected from V<sub>CC</sub> to BST turns on to charge C<sub>BST</sub>. The external circuit should provide sufficient voltage headroom to facilitate charging.

When the HS-FET is on, the BST voltage (V<sub>BST</sub>) exceeds V<sub>CC</sub>, so C<sub>BST</sub> cannot be charged.

At higher duty cycles, the time available for bootstrap charging is shorter, so C<sub>BST</sub> may not be sufficiently charged. If the external circuit has both insufficient voltage and time to charge C<sub>BST</sub>, use additional external circuitry to ensure V<sub>BST</sub> remains within the normal operation range.

### Selecting the Output Capacitor (SW, Pins 7 and 8)

The output capacitor (C<sub>OUT</sub>) maintains the DC V<sub>OUT</sub>. Use ceramic, tantalum, or low-ESR electrolytic capacitors. For the best results, use low-ESR capacitors to keep the output voltage ripple (ΔV<sub>OUT</sub>) low. ΔV<sub>OUT</sub> can be estimated with Equation (5):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}}\right) \quad (5)$$

Where L is the inductance, and R<sub>ESR</sub> is the equivalent series resistance (ESR) value of C<sub>OUT</sub>.

For ceramic capacitors, the capacitance dominates the impedance at f<sub>SW</sub> and causes the majority of ΔV<sub>OUT</sub>. For simplification, ΔV<sub>OUT</sub> can be estimated with Equation (6):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^2 \times L \times C_{OUT}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (6)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at f<sub>SW</sub>. For simplification, ΔV<sub>OUT</sub> can be estimated with Equation (7):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (7)$$

The C<sub>OUT</sub> characteristics also affect the stability of the regulation system. The part can be optimized for a wide range of capacitances and ESR values.

### Selecting the Inductor

A 1μH to 10μH inductor with a DC current rating at least 25% greater than the maximum load current is recommended for most applications. For higher efficiency, choose an inductor with a lower DC resistance. A larger-value inductor results in less ripple current and a lower ΔV<sub>OUT</sub>; however, it also has a larger physical size, higher series resistance, and lower saturation current. A good rule for determining the inductance is to allow the inductor ripple current to be approximately 30% of the maximum load current. The inductance (L) can be calculated with Equation (8):

$$L = \frac{V_{OUT}}{f_{SW} \times \Delta I_L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (8)$$

Where ΔI<sub>L</sub> is the peak-to-peak inductor ripple current.

Choose the inductor ripple current to be approximately 30% of the maximum load current. The maximum peak inductor current (I<sub>LP</sub>) can be calculated with Equation (9):

$$I_{LP} = I_{LOAD} + \frac{V_{OUT}}{2f_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (9)$$

### Peak and Valley Current Limit

Both the HS-FET and LS-FET have cycle-by-cycle current-limit protection. When I<sub>L</sub> reaches the high-side peak current limit (typically 5.8A) or the rising edge of the internal clock is reached while the current is rising and the HS-FET is on, the HS-FET is forced off immediately to prevent the current from rising further. When the LS-FET is on, the valley current limit circuit blocks the PWM from turning on the HS-FET until I<sub>L</sub> is below the low-side valley current limit (typically 4.4A). This current limit scheme prevents current runaway if an overload or short-circuit event occurs.

### Short-Circuit Protection (SCP)

If the output is shorted to ground, V<sub>OUT</sub> drops below 70% of its nominal output, and the LS-FET current exceeds the 4.4A valley current limit, then the device turns on the LS-FET until I<sub>L</sub> is fully discharged. The device also begins slowly discharging C<sub>SS</sub>. The device restarts with a full SS when C<sub>SS</sub> is fully discharged. This hiccup process repeats until the fault is removed.

### Output Over-Voltage Protection (OVP) and Discharge

There is an internal V<sub>OUT</sub> OVP circuit. When the device is operating in discontinuous conduction mode (DCM) and V<sub>OUT</sub> exceeds 106% of the target voltage, an output discharge path from V<sub>OUT</sub> to GND is activated to discharge V<sub>OUT</sub>. The output discharge path remains activated until the device returns to regulation and switching resumes.

When the device is operating in FCCM and V<sub>OUT</sub> exceeds 106% of the target voltage, the output discharge path turns on. If the negative current limit is triggered 265 times, the part enters hiccup mode and switching stops. Once V<sub>OUT</sub> drops to or below 105% of the target value, a new SS cycle resumes. The V<sub>OUT</sub> discharge path remains

on until V<sub>OUT</sub> reaches its regulated value, and the device begins switching.

### Enable (EN, Pin 9) and V<sub>IN</sub> Under-Voltage Lockout (UVLO)

EN is a digital control pin that turns the regulator on and off.

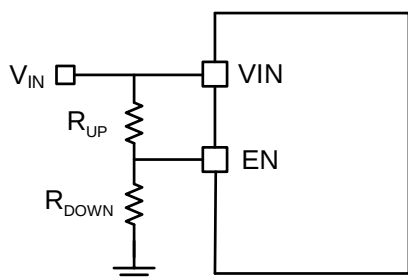
#### Enabled by External Logic High/Low Signal

When the EN voltage (V<sub>EN</sub>) reaches about 0.7V, the VCC supply turns on. When V<sub>IN</sub> exceeds 2.7V, it provides an accurate reference voltage for the EN threshold. Forcing EN above its 1V rising threshold turns on the device. Driving EN below 0.85V turns off the device.

### Configurable V<sub>IN</sub> Under-Voltage Lockout (UVLO)

When V<sub>IN</sub> is sufficiently high, the chip can be enabled and disabled via the EN pin. An internal pull-down resistor in this circuit can generate a configurable V<sub>IN</sub> under-voltage lockout (UVLO) and hysteresis.

The device requires a higher voltage (≥3.3V) for V<sub>IN</sub> to directly start up. The part has an internal, fixed UVLO threshold. The rising threshold is 3V, while the falling threshold is about 2.8V. For applications that require a higher UVLO point, an external resistor divider placed between V<sub>IN</sub> and EN can raise the equivalent UVLO threshold (see Figure 6).



**Figure 6: Adjustable UVLO Using EN Divider**

The UVLO rising threshold (V<sub>IN\_UVLO\_RISING</sub>) can be calculated with Equation (10):

$$V_{IN\_UVLO\_RISING} = \left(1 + \frac{R_{UP}}{R_{DOWN}}\right) \times V_{EN\_RISING} \quad (10)$$

The UVLO falling threshold (V<sub>IN\_UVLO\_FALLING</sub>) can be calculated with Equation (11):

$$V_{IN\_UVLO\_FALLING} = \left(1 + \frac{R_{UP}}{R_{DOWN}}\right) \times V_{EN\_FALLING} \quad (11)$$

Where V<sub>EN\_RISING</sub> is 1V, and V<sub>EN\_FALLING</sub> is 0.85V.

### SYNCO (Pin 12)

The SYNCO pin outputs a clock signal in phase with the internal oscillator signal or the external SYNCIN clock.

### Power Good (PG, Pin 13)

The device includes an open-drain power good (PG) output that indicates whether the regulator's output is within its nominal output range. PG goes high if the V<sub>OUT</sub> is within 94% to 106% of its nominal voltage; PG goes low if V<sub>OUT</sub> exceeds 107% or is below 93% of its nominal voltage. Float PG if it is not used. The PG resistance (R<sub>PG</sub>/R<sub>4</sub>) is recommended to be about 100kΩ.

### DNU (Pin14)

Connect the DNU pin directly to the VCC pin.

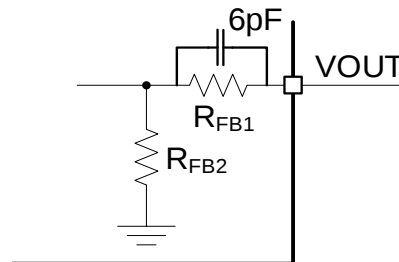
### Setting the VCC Capacitor (VCC, Pin 15)

Most of the internal circuitry is powered by the internal, 5V VCC regulator. This regulator uses V<sub>IN</sub> as its input and operates across the full V<sub>IN</sub> range. When V<sub>IN</sub> exceeds 5V, V<sub>CC</sub> is in full regulation. When V<sub>IN</sub> is below 5V, the output V<sub>CC</sub> degrades.

The VCC capacitor (C<sub>VCC</sub>) should have a capacitance at least 10 times greater than the boost capacitor, and at least 1μF nominally. A C<sub>VCC</sub> greater than 68μF nominal is not recommended.

### VOUT (Pin 17)

Because the feedback resistor divider is integrated internally, connect the VOUT pin directly to the output (see Figure 7).



**Figure 7: Feedback Divider Network of Fixed-Output Version**

The selectable fixed-output options are as follows: 1V, 1.1V, 1.8V, 2.5V, 3V, 3.3V, 3.8V, and 5V.

Table 4 shows the relationship between the internal feedback resistor (R<sub>FB</sub>) and V<sub>OUT</sub>.

**Table 4: R<sub>FB</sub> vs. V<sub>OUT</sub>**

| V <sub>OUT</sub> (V) | R <sub>FB1</sub> (MΩ) | R <sub>FB2</sub> (MΩ) |
|----------------------|-----------------------|-----------------------|
| 1                    | 1.33                  | 2                     |
| 1.1                  | 1.67                  | 2                     |
| 1.8                  | 4                     | 2                     |
| 2.5                  | 6.33                  | 2                     |
| 3                    | 8                     | 2                     |
| 3.3                  | 9                     | 2                     |
| 3.8                  | 10.67                 | 2                     |
| 5                    | 14.67                 | 2                     |

### Connection to GND (GND, Pins 5, 10, and 16)

See the PCB Layout Guidelines section below for more details.

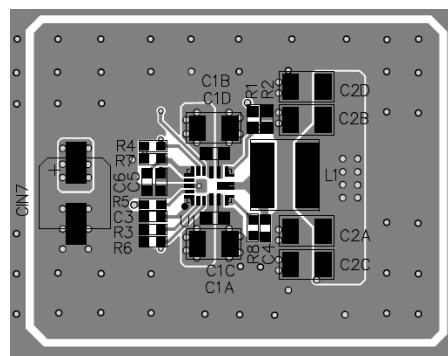
### PCB Layout Guidelines <sup>(12)</sup>

Efficient PCB layout is critical for stable operation. A 4-layer layout is strongly recommended to achieve improved thermal performance. For the best results, refer to Figure 8 and follow the steps below:

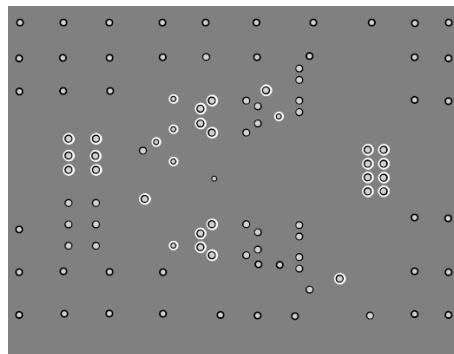
1. Place the symmetric C<sub>IN</sub> as close to VIN and GND as possible.
2. Use a large ground plane to connect directly to PGND.
3. Add vias near PGND if the bottom layer is a ground plane.
4. Ensure that the high-current paths at GND and VIN have short, direct, and wide traces.
5. Place the ceramic C<sub>IN</sub>, especially the small package size (0603) input bypass capacitor, as close to VIN and PGND as possible to minimize high-frequency noise.
6. Keep the connection between C<sub>IN</sub> and VIN as short and wide as possible.
7. Place C<sub>VCC</sub> as close to VCC and GND as possible.
8. Route SW and BST away from sensitive analog areas, such as FB.
9. Use multiple vias to connect the power planes to the internal layers.

#### Note:

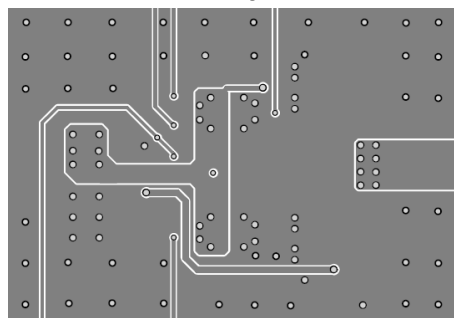
- 12) The recommended PCB layout is based on Figure 9 on page 41.



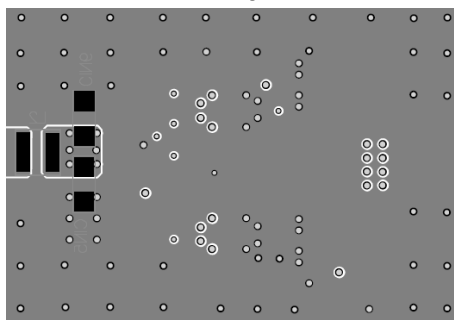
**Top Layer**



**Mid-Layer 1**



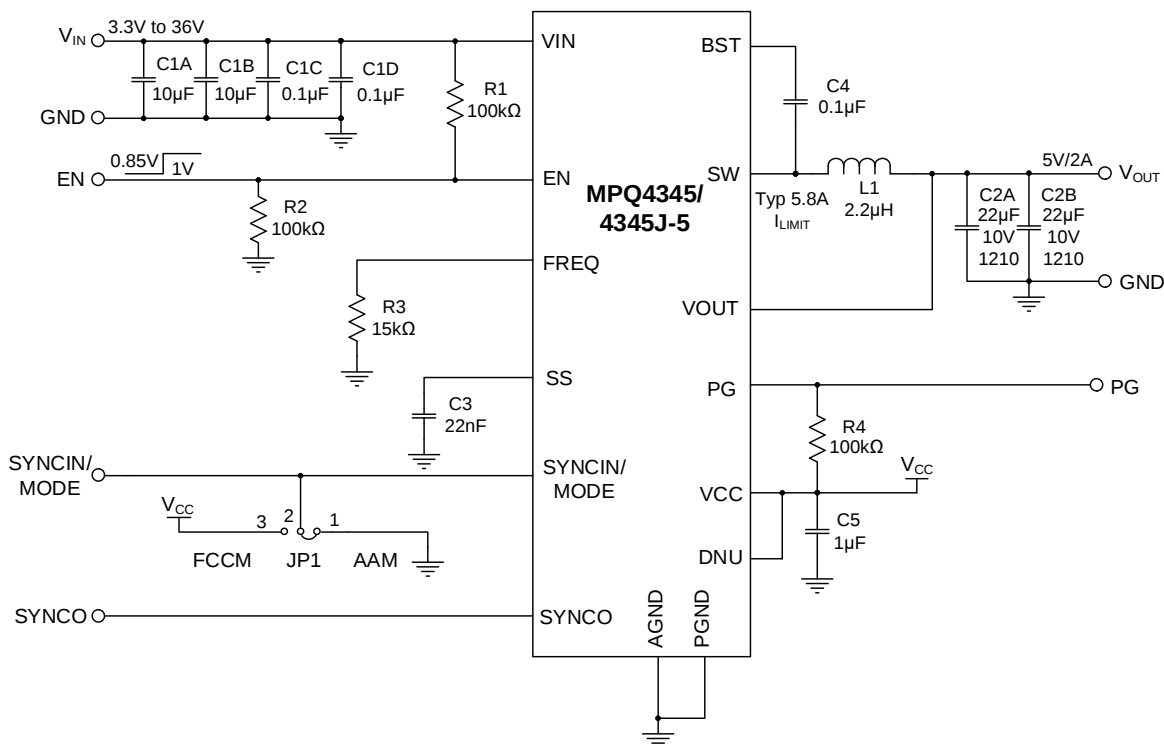
**Mid-Layer 2**



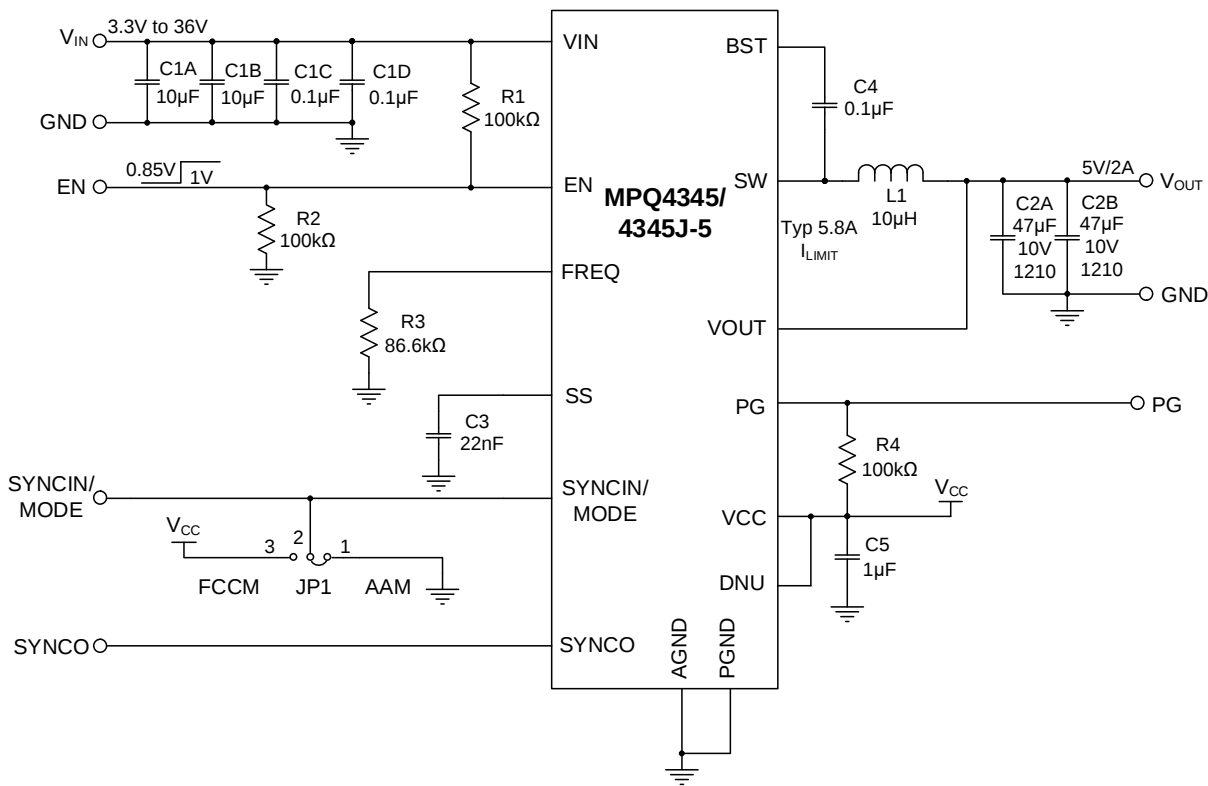
**Bottom Layer**

**Figure 8: Recommended PCB Layout**

## TYPICAL APPLICATION CIRCUITS

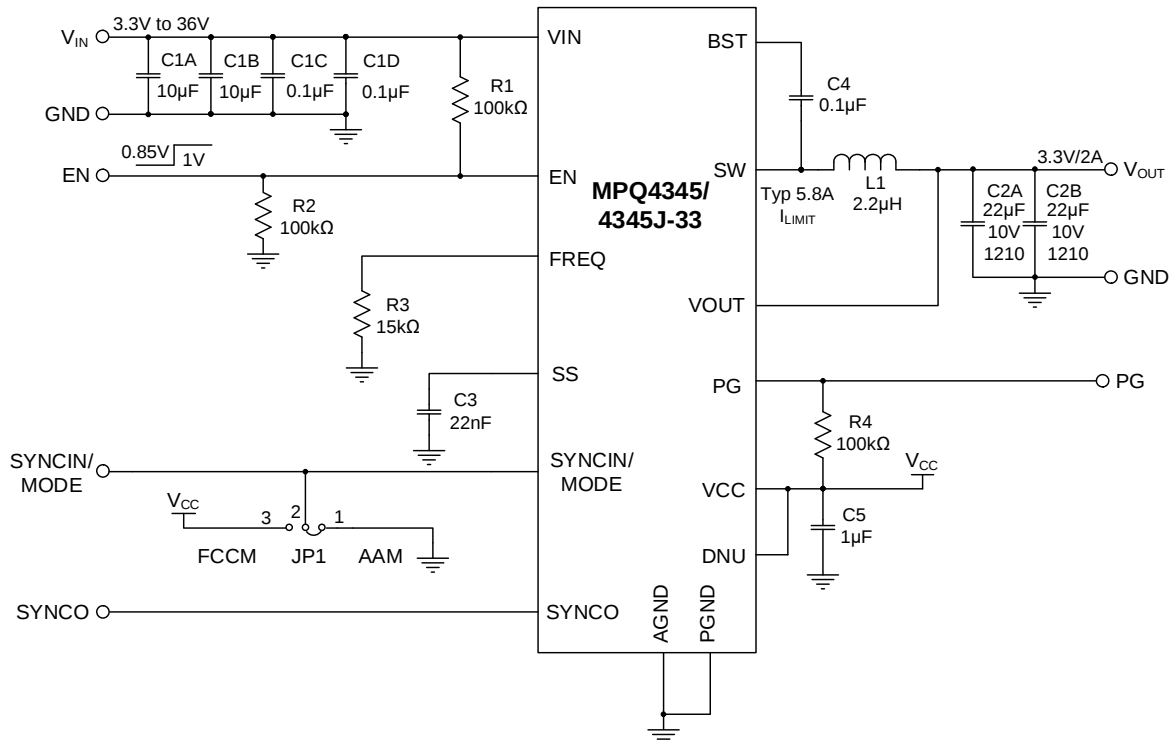


**Figure 9: Typical Application Circuit ( $V_{OUT} = 5V$ ,  $f_{SW} = 2.2MHz$ )**

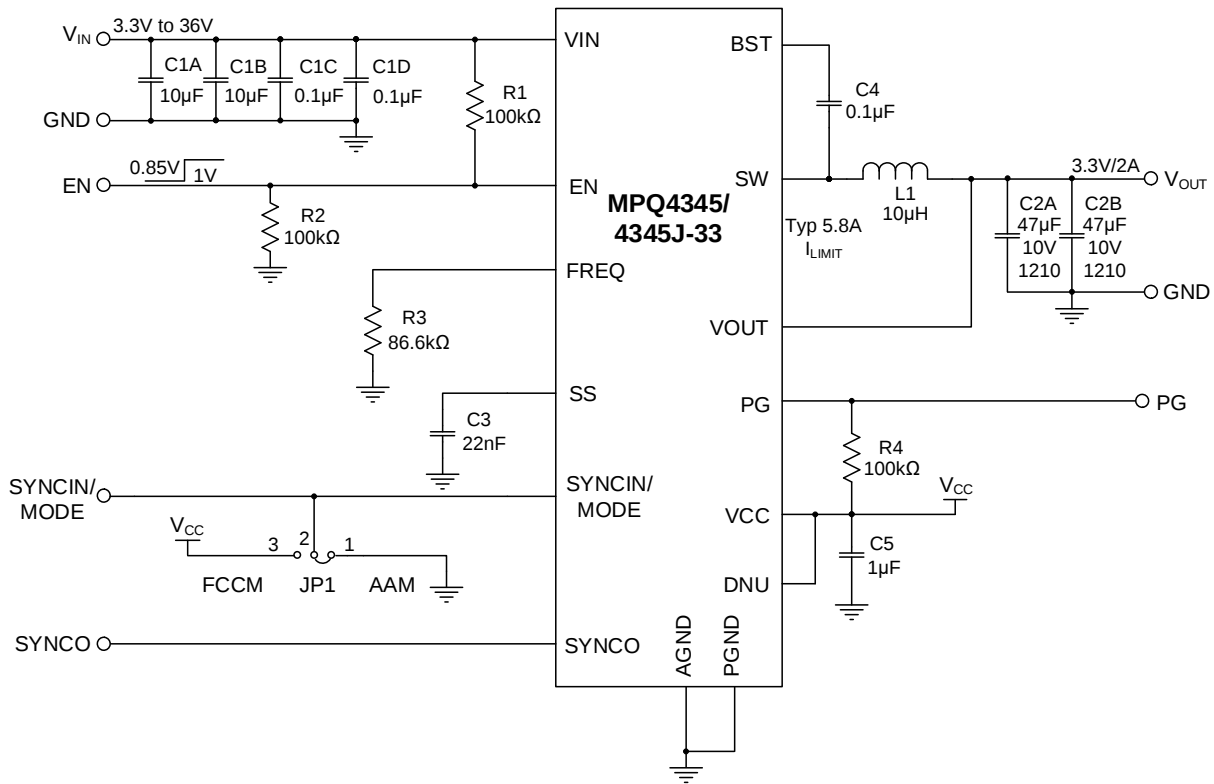


**Figure 10: Typical Application Circuit ( $V_{OUT} = 5V$ ,  $f_{SW} = 410kHz$ )**

## TYPICAL APPLICATION CIRCUITS (continued)

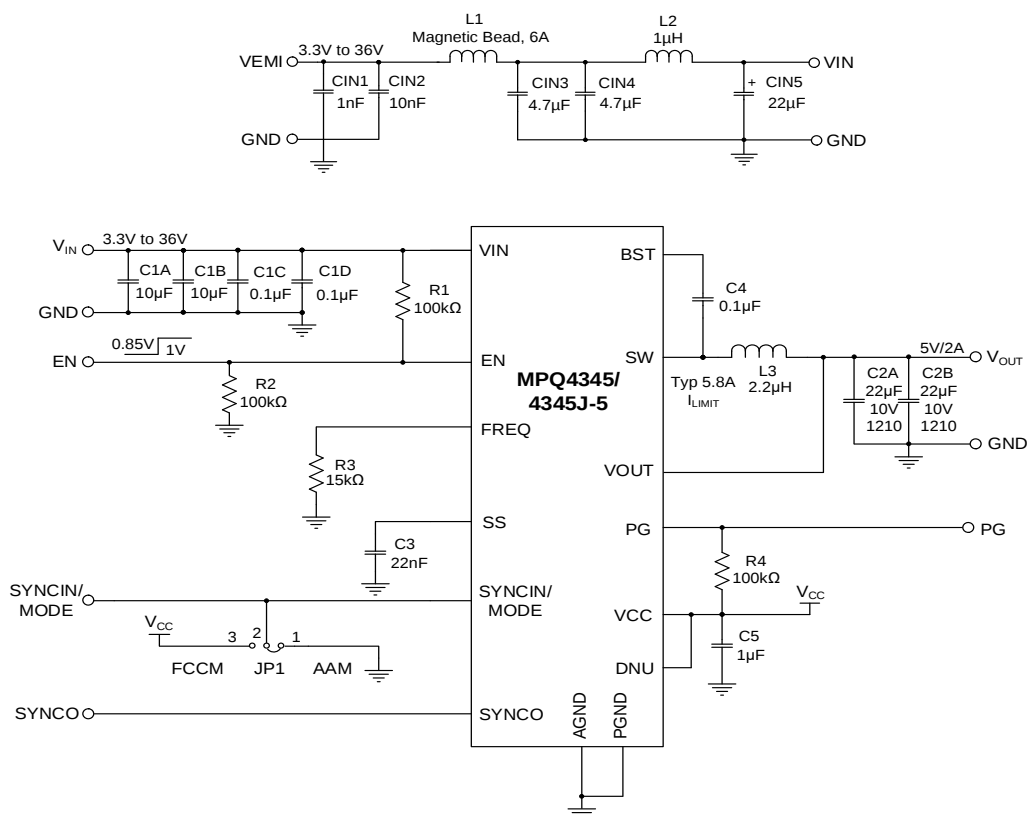


**Figure 11: Typical Application Circuit ( $V_{OUT} = 3.3\text{V}$ ,  $f_{sw} = 2.2\text{MHz}$ )**

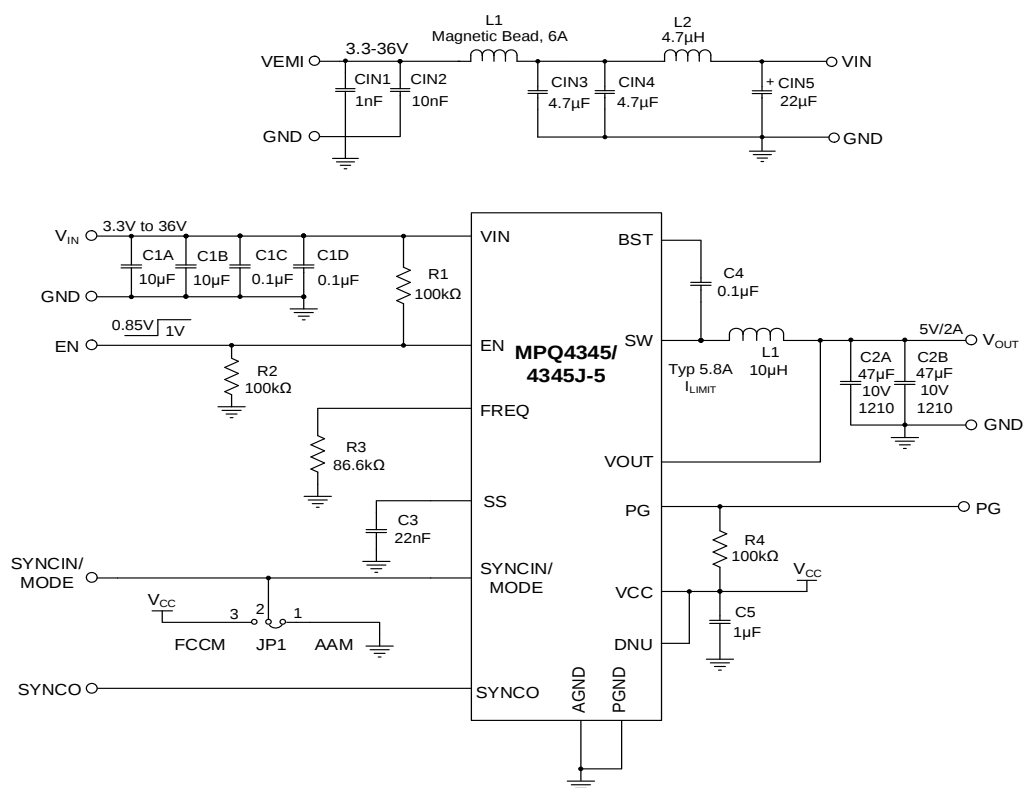


**Figure 12: Typical Application Circuit ( $V_{OUT} = 3.3\text{V}$ ,  $f_{sw} = 410\text{kHz}$ )**

## TYPICAL APPLICATION CIRCUITS *(continued)*



**Figure 13: Typical Application Circuit ( $V_{OUT} = 5V$ ,  $f_{SW} = 2.2MHz$  with EMI Filter)**

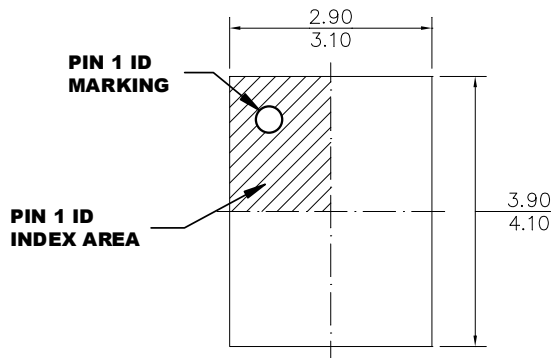


**Figure 14: Typical Application Circuit ( $V_{OUT} = 5V$ ,  $f_{SW} = 410kHz$  with EMI Filter)**

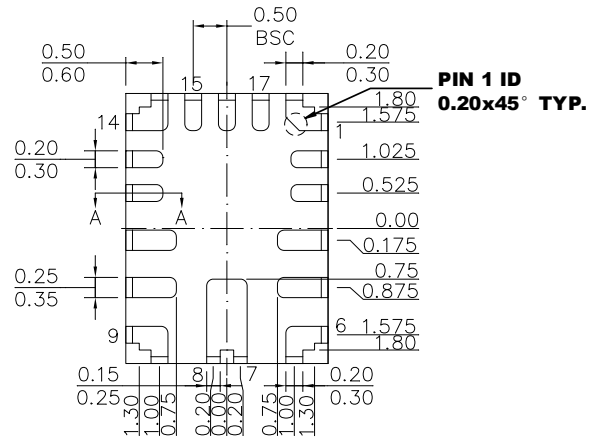
# PACKAGE INFORMATION

## QFN-17 (3mmx4mm)

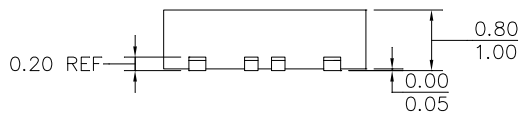
### Wettable Flank



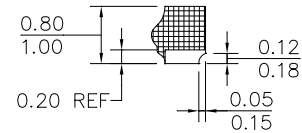
**TOP VIEW**



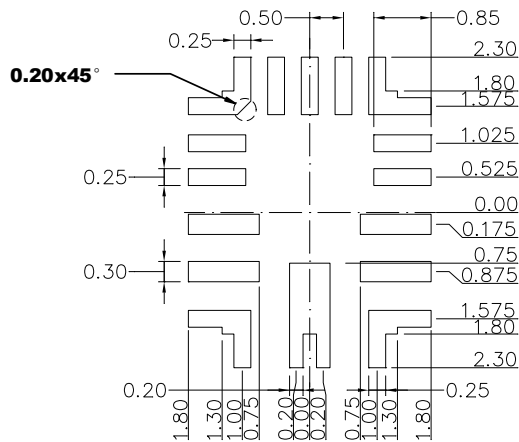
**BOTTOM VIEW**



**SIDE VIEW**



**SECTION A-A**



**RECOMMENDED LAND PATTERN**

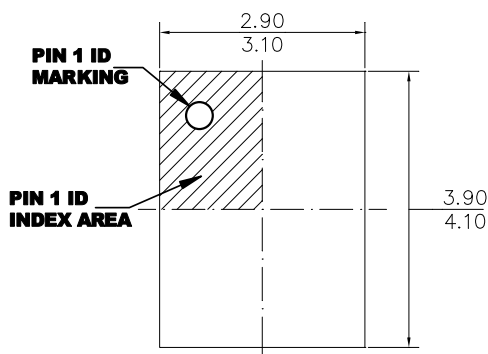
### NOTE:

- 1) THE LEAD SIDE IS WETTABLE.
- 2) ALL DIMENSIONS ARE IN MILLIMETERS.
- 3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
- 4) JEDEC REFERENCE IS MO-220.
- 5) DRAWING IS NOT TO SCALE.

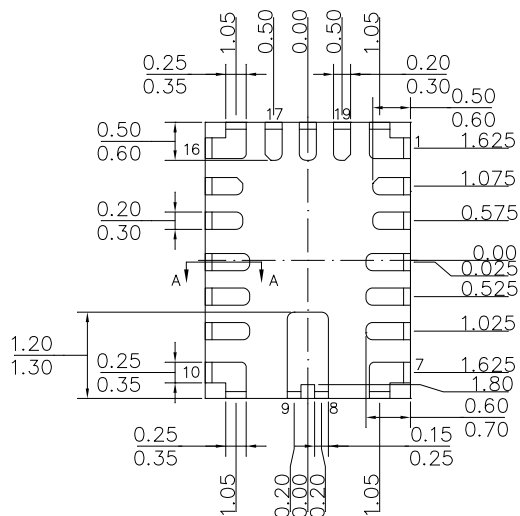
### PACKAGE INFORMATION (continued)

### QFN-19 (3mmx4mm)

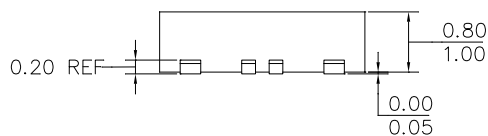
## Wettable Flank



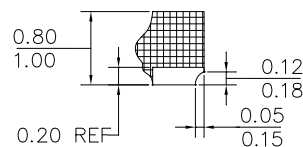
### TOP VIEW



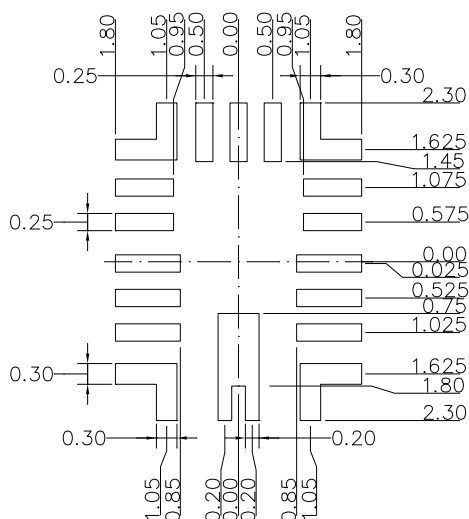
### BOTTOM VIEW



### SIDE VIEW



## SECTION A-A

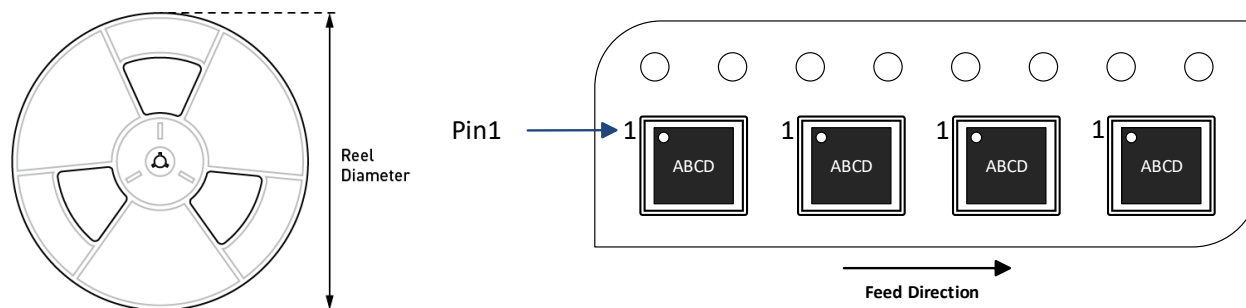


## RECOMMENDED LAND PATTERN

**NOTE:**

- 1) THE LEAD SIDE IS WETTABLE.
- 2) ALL DIMENSIONS ARE IN MILLIMETERS.
- 3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
- 4) JEDEC REFERENCE IS MO-220.
- 5) DRAWING IS NOT TO SCALE.

## CARRIER INFORMATION



| Part Number           | Package Description | Quantity /Reel | Quantity /Tube <sup>(13)</sup> | Quantity /Tray <sup>(13)</sup> | Reel Diameter | Carrier Tape Width | Carrier Tape Pitch |
|-----------------------|---------------------|----------------|--------------------------------|--------------------------------|---------------|--------------------|--------------------|
| MPQ4345GLE-33-AEC1-Z  | QFN-17 (3mmx4mm)    | 5000           | N/A                            | N/A                            | 13in          | 12mm               | 8mm                |
| MPQ4345GLE-5-AEC1-Z   | QFN-17 (3mmx4mm)    | 5000           | N/A                            | N/A                            | 13in          | 12mm               | 8mm                |
| MPQ4345JGLE-33-AEC1-Z | QFN-19 (3mmx4mm)    | 5000           | N/A                            | N/A                            | 13in          | 12mm               | 8mm                |
| MPQ4345JGLE-5-AEC1-Z  | QFN-19 (3mmx4mm)    | 5000           | N/A                            | N/A                            | 13in          | 12mm               | 8mm                |

**Note:**

13) N/A indicates "not available" in tubes. For 500-piece tape & reel prototype quantities, see factory. (Order code for 500-piece partial reel is "-P", tape & reel dimensions same as full reel.)



## REVISION HISTORY

| Revision # | Revision Date | Description     | Pages Updated |
|------------|---------------|-----------------|---------------|
| 1.0        | 12/20/2022    | Initial Release | -             |

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