MPQ4326B

36V, 3A to 7A, Low Quiescent Current, Synchronous Step-Down Converter, AEC-Q100 Qualified

DESCRIPTION

The MPQ4326B is a configurable-frequency (200kHz to 2.5MHz), synchronous step-down switching regulator with integrated internal high-side and low side power MOSFET (HS-FET and LS-FET, respectively). This family provides 3A to 7A of highly efficient output current (I_{OUT}) with peak current mode control.

The wide 3.3V to 36V input voltage (V_{IN}) range accommodates a variety of step-down applications in automotive input environments. A 1µA shutdown mode quiescent current allows for use in battery-powered applications.

High power conversion efficiency across a wide load range is achieved by scaling down the switching frequency (f_{SW}) under light-load conditions to reduce the switching and gate driving losses.

An open-drain power good (PG) signal indicates whether the output is within 94.5% to 105.5% of its nominal voltage.

Frequency foldback helps prevent inductor current (I_L) runaway during start-up. Thermal shutdown provides reliable, fault-tolerant operation.

A high duty cycle and low-dropout mode are provided for automotive cold-crank conditions.

The MPQ4326B is available in a QFN-14 (4mmx4mm) package. It is available in AEC-Q100 Grade 1.

FEATURES

- Designed for Automotive Applications
  - Survives 42V Load Dump
  - 3A to 7A Continuous Output Current (I_{OUT}) Versions in Pin-Compatible Family
  - Continuous Operation Up to 36V
  - Low-Dropout Mode
  - 50ns Minimum On Time
  - Junction Temperature (T_J) Operation from -40°C to +150°C
  - Available in AEC-Q100 Grade 1

FEATURES *(continued)*

- Increases Battery Life
  - 1µA Low Shutdown Supply Current
  - 27µA Sleep Mode Quiescent Current
  - 30µA Quiescent Current with Switching
  - Advanced Asynchronous Modulation (AAM) Mode Increases Efficiency under Light Loads
- High Performance for Improved Thermals
  - Internal 45mΩ High-Side and 25mΩ Low-Side MOSFET
- Optimized for EMC/EMI
  - 200kHz to 2.5MHz Configurable Switching Frequency (f_{SW})
  - Frequency Spread Spectrum Modulation
  - Symmetric VIN Pinout
  - CISPR 25 Class 5 Compliant
  - MeshConnect™ Flip-Chip Package
- Additional Features
  - Fixed Output Options(1): 3.3V, 3.8V, 5V
  - Power Good (PG) Output
  - Can be Synchronized to External Clock
  - Over-Current Protection (OCP) with Hiccup Mode
  - Available in a QFN-14 (4mmx4mm) Package with Wettable Flanks
- Functional Safety System Design Capable
  - Documents Available for MPSafe™ System Design

MPSafe™ FuSa Compatible

APPLICATIONS

- Automotive Infotainment
- Automotive Clusters
- Advanced Driver-Assistance Systems
- Industrial Power Systems

Note:

1) See the Ordering Information section on page 3 for the exact availability of each fixed output version. Additional output voltages may be available. Contact MPS for details.

TYPICAL APPLICATION

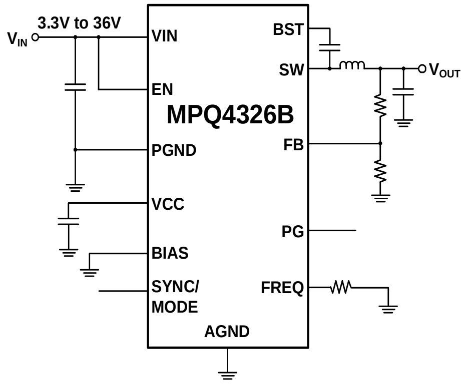


Figure 1: Adjustable Output Version

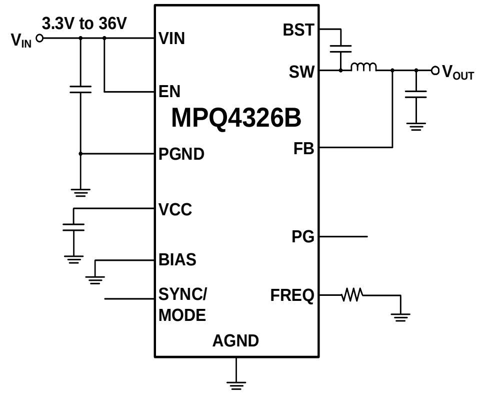
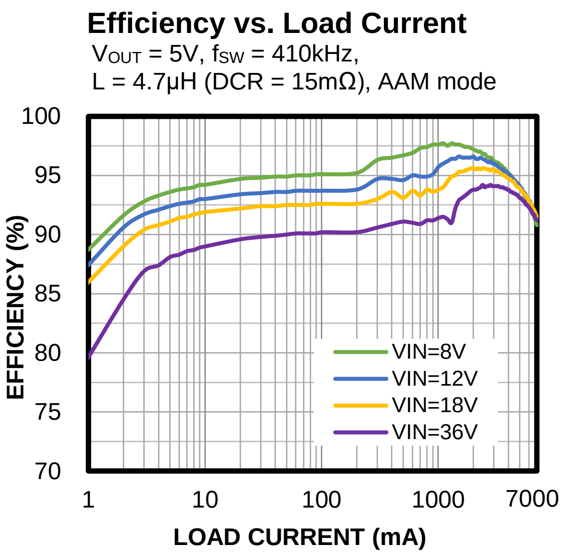
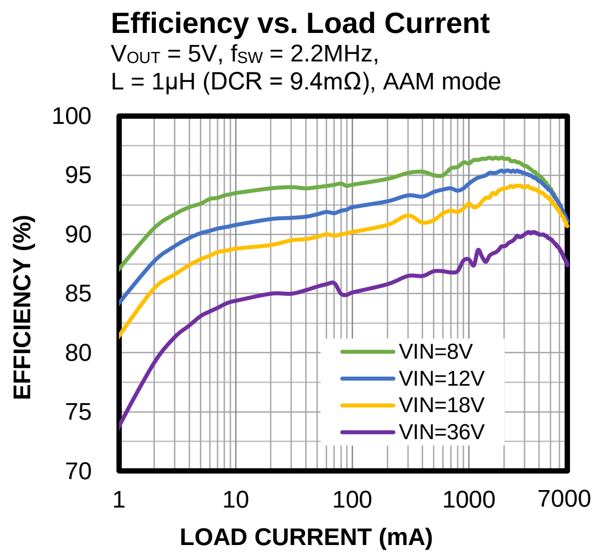


Figure 2: Fixed Output Version





ORDERING INFORMATION

Part Number* (2)(3)	Package	Top Marking	MSL Rating**
MPQ4326BGRE-xxxx-AEC1 ***	QFN-14 (4mmx4mm)	*See Below*	*1*

* For Tape & Reel, add suffix -Z (e.g. MPQ4326BGRE-xxxx-AEC1-Z).

** Moisture Sensitivity Level Rating

*** Wettable flank

Notes:

2) Contact MPS for the details regarding fixed output versions.
3) The detailed information of part number can be marked as MPQ4326B-WXYZ. Table 1 shows the meaning of the 4-digit code.

Table 1: Part Number Digit Code Naming Rule

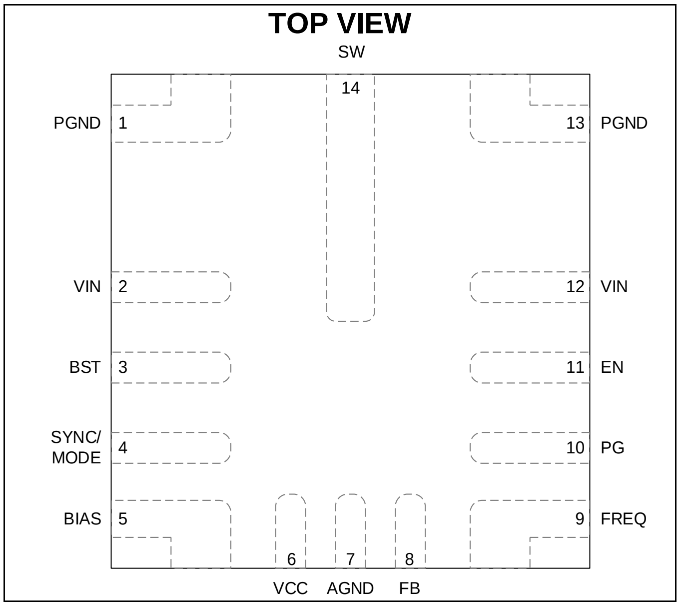
Digit Code	Naming Rule
W: Defines the nominal output current	3: 3A
	4: 4A
	5: 5A
	6: 6A
	7: 7A
X: Defines the output voltage	0: Adjustable output
	3: Fixed 3.3V output
	4: Fixed 3.8V output
	5: Fixed 5V output
Y: Defines the frequency spread spectrum configuration	0: With FSS
	A: Without FSS
Z: Defines V_{IN} OVP function	0: V_{IN} OVP enabled
	1: V_{IN} OVP disabled

TOP MARKING

<u>MPSYWW</u>
M4326B
LLLLLL
E

MPS: MPS prefix
Y: Year code
WW: Week code
M4326B: Part number
LLLLLL: Lot number
E: Wettable flank

PACKAGE REFERENCE



QFN-14 (4mmx4mm)

PIN FUNCTIONS

Pin #	Name	Description
1, 13	PGND	**Power ground.**
2, 12	VIN	**Input supply.** VIN supplies power to all the internal control circuitry, as well as the power switch connected to SW. The two VIN pins are connected internally. Place decoupling capacitors from each pin to ground, and as close as possible to each VIN pin, to minimize the input voltage ripple and switching spikes.
3	BST	**Bootstrap.** BST is the positive power supply for the high-side MOSFET (HS-FET) driver connected to SW. Connect a bypass capacitor between BST and SW. See the Application Information section starting on page 57 to calculate the size of this capacitor.
4	SYNC/ MODE	**SYNC input and mode selection pin.** Pull the SYNC/MODE pin below the specified threshold (0.4V) for advanced asynchronous modulation (AAM) mode; pull it above the specified threshold (1.4V) for forced continuous conduction mode (FCCM). There is an external 200kHz to 2.5MHz clock source tied to this pin. The converter synchronizes with the external clock and operates in FCCM. This pin has one 100kΩ internal pull-down resistor. When this pin is floating, the part operates in AAM mode.
5	BIAS	**External bias.** Connect the BIAS pin to the 5V output voltage (V_{OUT}) supply for a lower quiescent current (I_Q). For the 5V output version, tie this pin to the output voltage directly. For other output versions, connect this pin to an external 5V source or GND. It is recommended to avoid providing an external bias voltage before V_{IN}. Do not float this pin.
6	VCC	**Internal bias supply.** The VCC pin is the output of the internal regulator that supplies power to the internal control circuit and gate drivers. VCC is typically 5V. Place a decoupling capacitor exceeding 1µF between VCC and ground. The capacitor should be placed as close to VCC as possible.
7	AGND	**Analog ground.**
8	FB	**Feedback input.** For the fixed-output versions, connect the FB pin directly to V_{OUT}. For the adjustable-output version, connect FB to the middle point of the external feedback divider between the output and AGND to set V_{OUT}. The feedback threshold voltage is 0.8V. Place the resistor divider as close to FB as possible. Avoid placing vias on the FB traces.
9	FREQ	**Switching frequency configuration.** Connect a resistor from the FREQ pin to ground to set the switching frequency (f_{SW}).
10	PG	**Power good output.** The PG pin is an open-drain output. If PG is used, connect a pull-up resistor to the power source. PG goes high if V_{OUT} is within 94.5% to 105.5% of the nominal voltage. PG goes low if V_{OUT} exceeds 107% or is below 93% of the nominal voltage. Float this pin if it is not used.
11	EN	**Enable.** Pull the EN pin below the specified threshold (0.85V) to shut down the chip. Pull EN above the specified threshold (1.02V) to enable the chip. Do not float this pin.
14	SW	**Switch node.** The SW pin is the source of the HS-FET and the drain of the low-side MOSFET (LS-FET).

ABSOLUTE MAXIMUM RATINGS (4)

VIN, EN…………………..............-0.3V to +40V
VIN, EN…..…....42V for automotive load dump (5)
SW………………………. -0.3V to $V_{IN(MAX)}$ + 0.3V
BST……………………………………..V_{SW} + 5.5V
FREQ…………...…………………-0.3V to +5.5V
All other pins…………………………-0.3V to +6V
Continuous power dissipation (T_A = 25°C) (6) (10)
QFN-14 (4mmx4mm) …………………….... 4.86W
Junction temperature (T_J)…...………....... 150°C
Lead temperature………….………....…. 260°C
Storage temperature…………...-65°C to +150°C

ESD Ratings

Human body model (HBM)..................Class 2 (7)
Charged-device model (CDM).........Class C2b (8)

Recommended Operating Conditions

Supply voltage (V_{IN})………………….3.3V to 36V
Output voltage (V_{OUT})………...0.8V to 0.95 x V_{IN}
Operating junction temp (T_J) .... -40°C to +150°C

Thermal Resistance θJA θJC

QFN-14 (4mmx4mm)
JESD51-7….....….……….46.7.....7.9.....°C/W (9)
EVQ4326B-R-00A.......….25.7..............°C/W (10)

ΨJT

QFN-14 (4mmx4mm)
JESD51-7 …....…..........................2.6......°C/W (9)
EVQ4326B-R-00A.…...…............2.2.... °C/W (10)

Notes:

4) Absolute maximum ratings are rated under room temperature unless otherwise noted. Exceeding these ratings may damage the device.
5) Refer to ISO16750.
6) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
7) Per AEC-Q100-002.
8) Per AEC-Q100-011.
9) Measured on a JESD51-7, 4-layer PCB. The values given in this table are only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application. The value of θ_{JC} shows the thermal resistance from junction-to-case bottom, and the value of Ψ_{JT} shows the characterization parameter from junction-to-case top.
10) Measured on an MPS standard EVB: 8.3cmx8.3cm, 2oz copper thickness, 4-layer PCB. The value of Ψ_{JT} shows the characterization parameter from junction-to-case top.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, V_{EN} = 2V, T_J = -40°C to +150°C, typical values are at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Supply						
Input voltage (V_{IN}) minimum operating voltage	V_{IN_MIN}				3.3	V
V_{IN} under-voltage lockout (UVLO) rising threshold	V_{INUVLO_RISING}		3.5	3.7	3.9	V
V_{IN} UVLO falling threshold	$V_{INUVLO\_FALLING}$		2.75	2.9	3.15	V
V_{IN} UVLO hysteresis	V_{INUVLO_HYS}			800		mV
VIN quiescent current	I_Q	FB = 0.85V, no load, (sleep mode), connect BIAS pin to GND, T_J = 25°C		27	35	µA
		FB = 0.85V, no load, (sleep mode), connect BIAS pin to GND, T_J = -40°C to +150°C		27	80	µA
		FB = 0.85V, no load, (sleep mode), connect BIAS pin to 5V		3		µA
VIN quiescent current (switching)	I_{Q_SLEEP}	SYNC/MODE = GND (AAM mode), switching, no load		30		µA
VIN active current (non-switching) (11)	I_{Q_ACTIVE}	SYNC/MODE = V_{CC} (CCM), non-switching, R_{FREQ} = 8.66kΩ		950		µA
VIN shutdown current	I_{SHDN}	EN = 0V		1	10	µA
V_{IN} over-voltage protection (OVP) threshold	V_{INOVP_RISING}		36	38	40	V
VIN OVP hysteresis	V_{INOVP_HYS}			1		V
Switches and Frequency						
Switching frequency	f_{SW}	R_{FREQ} = 49.9kΩ	350	410	460	kHz
		R_{FREQ} = 19.6kΩ	900	1000	1100	kHz
		R_{FREQ} = 8.66kΩ	1980	2200	2420	kHz
Minimum on time (11)	t_{ON_MIN}			50	65	ns
Minimum off time (11)	t_{OFF_MIN}			40	55	ns
Switch leakage current	I_{SW_LKG}	T_J = 25°C		0.01	1	µA
		T_J = -40°C to +150°C		0.01	5	µA
High-side (HS) switch on resistance	R_{ON_HS}	V_{BST} - V_{SW} = 5V		45		mΩ
Low-side (LS) switch on resistance	R_{ON_LS}	V_{CC} = 5V		25		mΩ
BIAS						
BIAS voltage (V_{BIAS}) takeover threshold	V_{BIAS_RISING}			4.6		V
V_{BIAS} takeover hysteresis	V_{BIAS_HYS}			240		mV

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{EN} = 2V, T_J = -40°C to +150°C, typical values are at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Output and Regulation						
FB voltage (adjustable output version)	V_{FB}	T_J = 25°C	794	800	806	mV
		T_J = -40°C to +150°C	790	800	810	mV
Output regulation voltage (3.3V fixed-output version)	$V_{OUT\_3.3V}$	T_J = 25°C	3250	3300	3350	mV
		T_J = -40°C to +150°C	3234	3300	3366	mV
Output regulation voltage (5V fixed-output version)	V_{OUT_5V}	T_J = 25°C	4950	5000	5050	mV
		T_J = -40°C to +150°C	4900	5000	5100	mV
FB input current	I_{FB}	Adjustable-output version		0	100	nA
		Fixed-output version, V_{OUT} = V_{OUT_REG}		3.3		µA
VOUT discharge current	$I_{DISCHARGE}$	EN = 0V, V_{OUT} = 0.3V	2			mA
Bootstrap (BST)						
BST-SW refresh rising threshold	$V_{UVBST-SW\_RISING}$		2.2	2.7	3.2	V
BST-SW refresh falling threshold	$V_{UVBST-SW\_FALLING}$		2.0	2.5	3.0	V
BST-SW refresh hysteresis	$V_{UVBST-SW\_HYS}$			0.2		V
Enable (EN)						
EN rising threshold	V_{EN_RISING}		0.97	1.02	1.07	V
EN falling threshold	$V_{EN\_FALLING}$		0.80	0.85	0.90	V
EN hysteresis voltage	V_{EN_HYS}			170		mV
Soft Start (SS) and VCC						
Soft-start time	t_{SS}	EN high to PG high	4.5	6.0	7.5	ms
VCC voltage	V_{CC}	I_{VCC} = 0mA	4.7	5.0	5.3	V
VCC regulation		I_{VCC} = 30mA, AAM mode		1		%
VCC current limit	I_{LIMIT_VCC}	V_{CC} = 4V	50	65		mA
SYNC/MODE						
SYNC/MODE voltage rising threshold	V_{SYNC_RISING}		1.4			V
SYNC/MODE voltage falling threshold	$V_{SYNC\_FALLING}$				0.4	V
SYNC/MODE timeout	t_{MODE}	SYNC/MODE low to DCM		55	80	µs
SYNCIN clock range	f_{SYNC}	% of free-running frequency	90%		110%	f_{SW}
SYNCIN clock locking time	t_{SYNC_LOCK}	SYNC clock locking time			128	cycle
SYNCIN clock duty	D_{SYNC_DUTY}	SYNC clock duty for min input clock edge >40ns	20		80	%
f_{SW} After SYNC		f_{SW} accuracy compares to f_{SYNC}	-5		+5	%

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{EN} = 2V, T_J = -40°C to +150°C, typical values are at T_J = 25°C, unless otherwise noted.

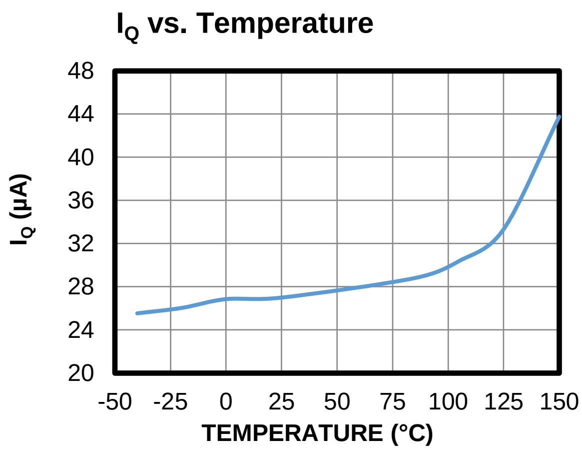
Parameter	Symbol	Condition	Min	Typ	Max	Units
Frequency Spread Spectrum (FSS)						
FSS modulation frequency	f_{SSFREQ}			7.5		kHz
FSS span	f_{SSSPAN}	% of free-running frequency		20%		f_{SW}
Power Good (PG)						
PG rising threshold	V_{PGVTH_RISING}	V_{OUT} rising	93%	94.5%	96%	V_{OUT}
		V_{OUT} falling	104%	105.5%	107%	V_{OUT}
PG falling threshold	$V_{PGVTH\_FALLING}$	V_{OUT} falling	91.5%	93%	94.5%	V_{OUT}
		V_{OUT} rising	105.5%	107%	108.5%	V_{OUT}
PG trip threshold hysteresis	V_{PGVTH_HYS}			1.5%		V_{OUT}
PG output voltage low	V_{PG_LOW}	I_{SINK} = 1mA		0.1	0.3	V
PG power on rising delay	$t_{PG\_R\_DELAY}$			1.2		ms
PG rising deglitch	$t_{PG\_R\_DEGLITCH}$			160		µs
PG falling deglitch	$t_{PG\_F\_DEGLITCH}$			160		µs
Protections						
HS current limit	I_{LIMIT_HS}	Duty cycle = 30%, For MPQ4326B-3xxx	4.3	5.8	7.3	A
		Duty cycle = 30%, For MPQ4326B-4xxx	5.5	7.5	9.5	
		Duty cycle = 30%, For MPQ4326B-5xxx	7.5	9.5	11.5	
		Duty cycle = 30%, For MPQ4326B-6xxx	8.5	11	13	
		Duty cycle = 30%, For MPQ4326B-7xxx	9.5	12	14	
LS valley current limit	I_{LIMIT_LS}	Duty cycle = 30%, For MPQ4326B-3xxx	3	4.4	5.7	A
		Duty cycle = 30%, For MPQ4326B-4xxx	4	5	6.8	
		Duty cycle = 30%, For MPQ4326B-5xxx	4.7	6	7.3	
		Duty cycle = 30%, For MPQ4326B-6xxx	6	7.5	9	
		Duty cycle = 30%, For MPQ4326B-7xxx	6.5	8	9	
Zero-current detection (ZCD) current	I_{ZCD}	AAM mode	0	200		mA
LS reverse current limit	$I_{LIMIT\_REVERSE}$	FCCM		3		A
Thermal shutdown (11)	T_{SD}		155	170	185	°C
Thermal shutdown hysteresis (11)	T_{SD_HYS}			20		°C

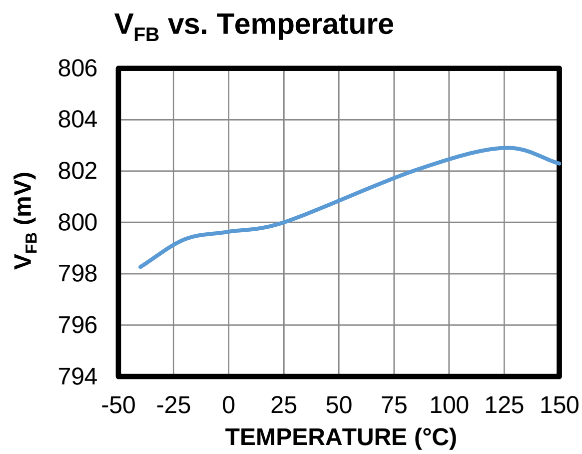
Note:

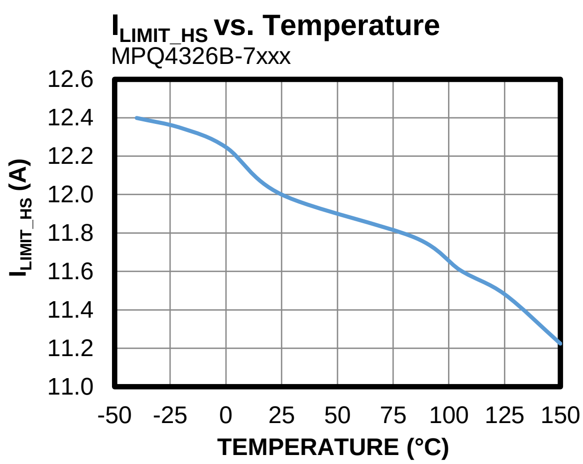
11) Not tested in production and guaranteed by design and characterization.

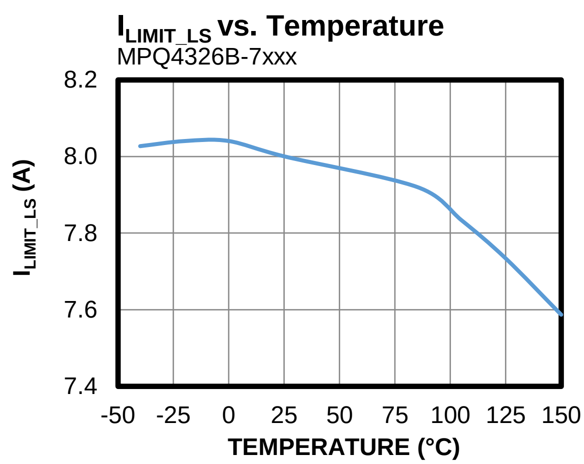
TYPICAL CHARACTERISTICS

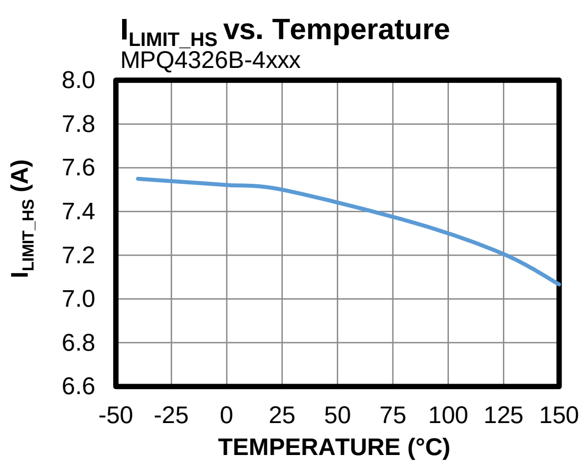
V_{IN} = 12V, T_J = -40°C to +150°C, unless otherwise noted.

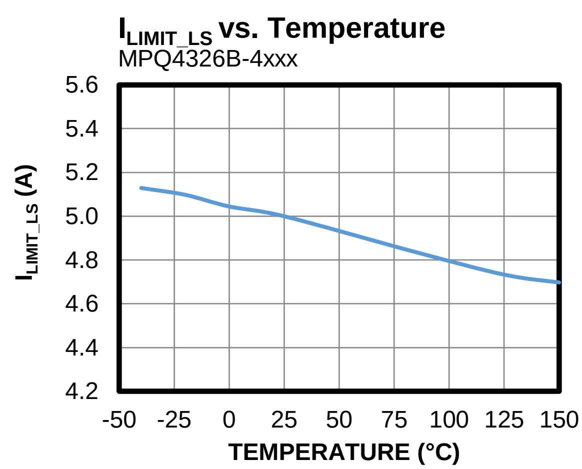








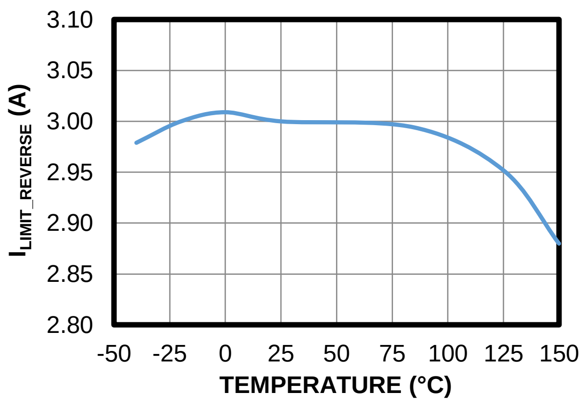




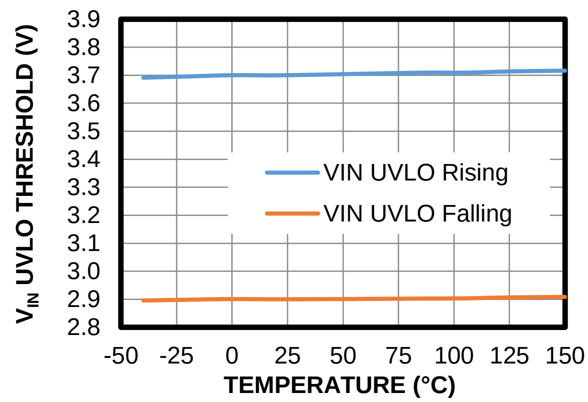
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_J = -40°C to +150°C, unless otherwise noted.

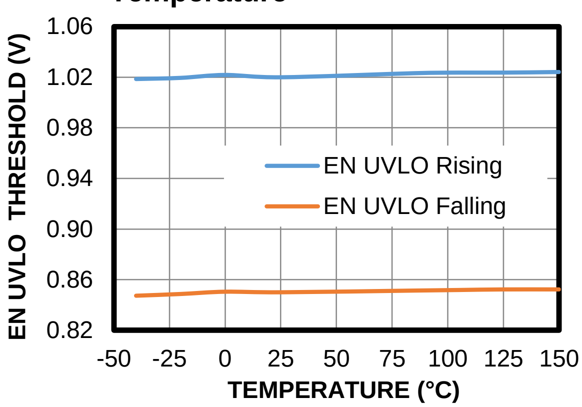
$I_{LIMIT\_REVERSE}$ vs. Temperature



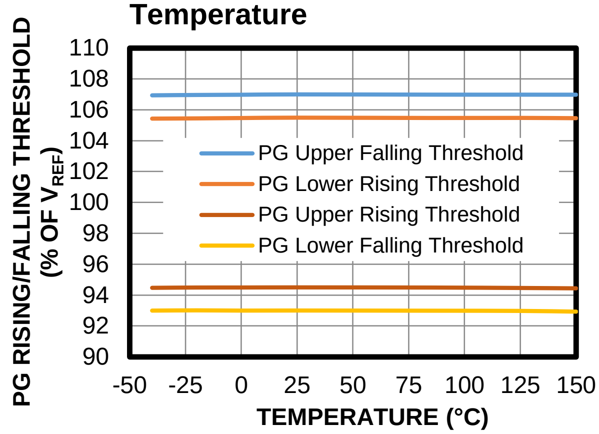
V_{IN} UVLO Threshold vs. Temperature



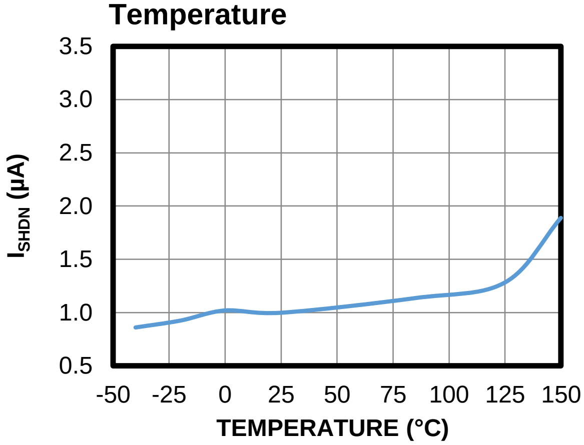
EN UVLO Threshold vs. Temperature



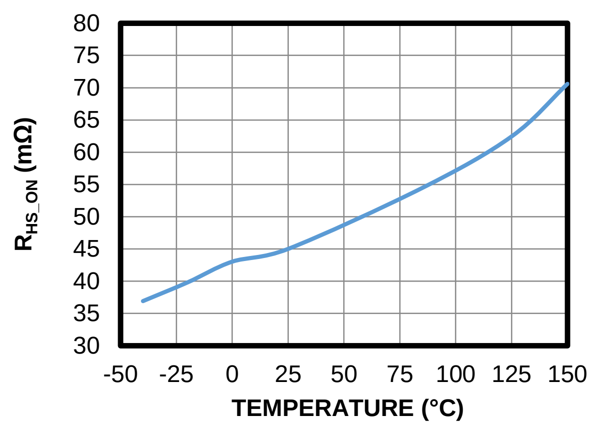
PG Rising/Falling Threshold vs. Temperature



VIN Shutdown Current vs. Temperature



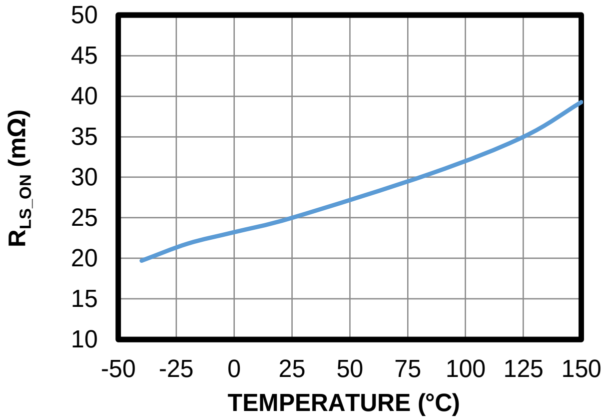
R_{HS_ON} vs. Temperature



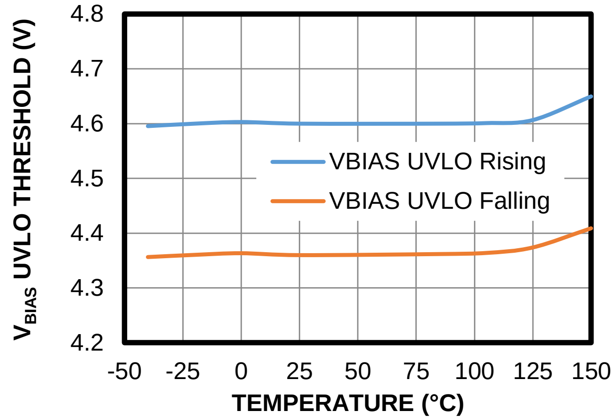
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_J = -40°C to +150°C, unless otherwise noted.

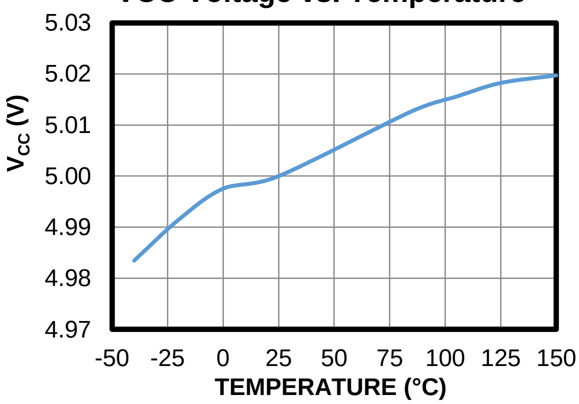
R_{LS_ON} vs. Temperature



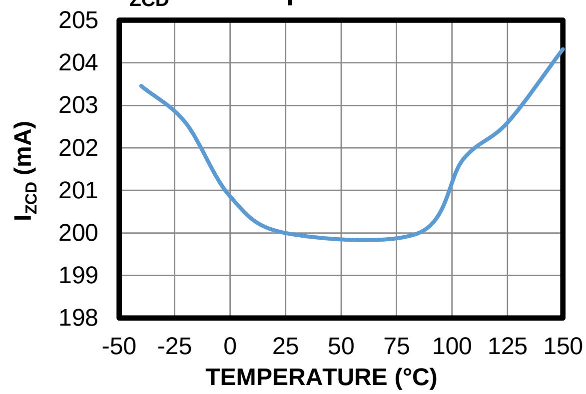
V_{BIAS} UVLO Threshold vs. Temperature



VCC Voltage vs. Temperature

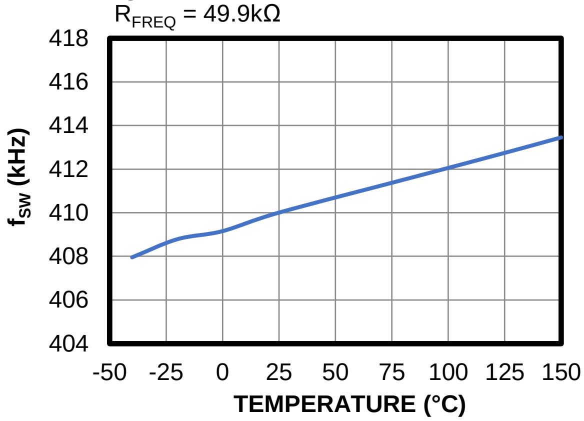


I_{ZCD} vs. Temperature



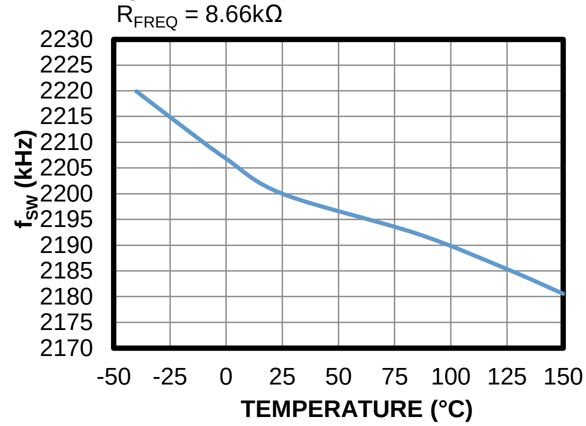
f_{SW} vs. Temperature

R_{FREQ} = 49.9kΩ



f_{SW} vs. Temperature

R_{FREQ} = 8.66kΩ

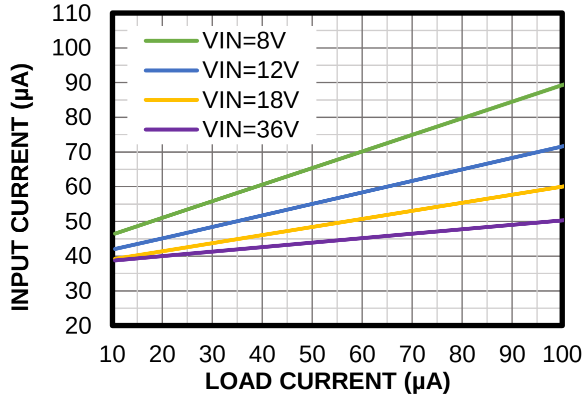


TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 5V, L = 1µH, f_{SW} = 2.2MHz, AAM mode, BIAS connected to V_{OUT}, T_A = 25°C, unless otherwise noted.

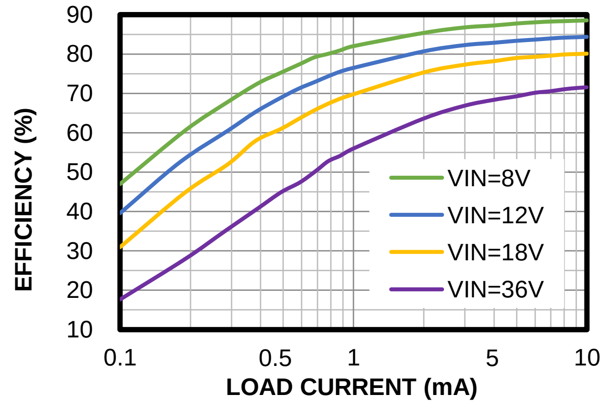
Input Current vs. Load Current

AAM mode, V_{OUT} = 3.3V, f_{SW} = 2.2MHz, L = 1µH (DCR = 9.4mΩ)



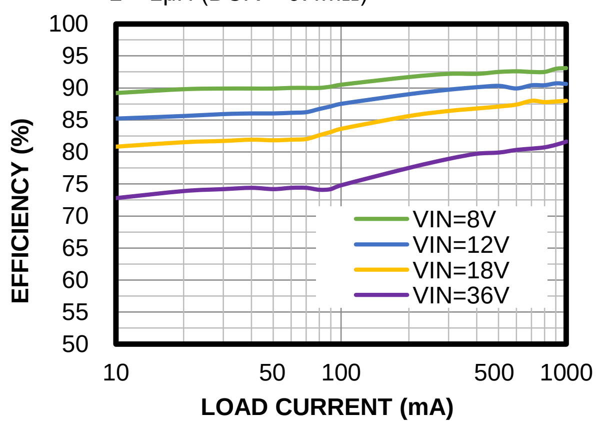
Efficiency vs. Load Current

AAM mode, V_{OUT} = 3.3V , f_{SW} = 2.2MHz, L = 1µH (DCR = 9.4mΩ)



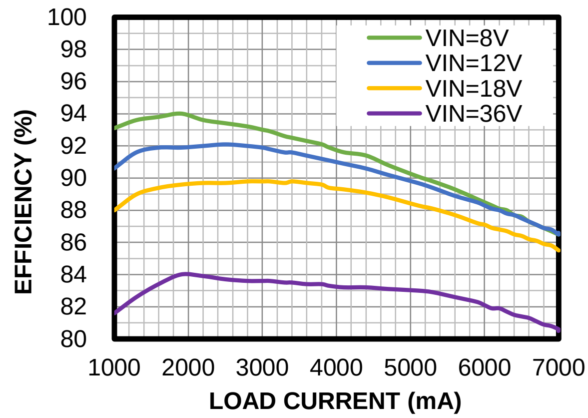
Efficiency vs. Load Current

AAM mode, V_{OUT} = 3.3V, f_{SW} = 2.2MHz, L = 1µH (DCR = 9.4mΩ)



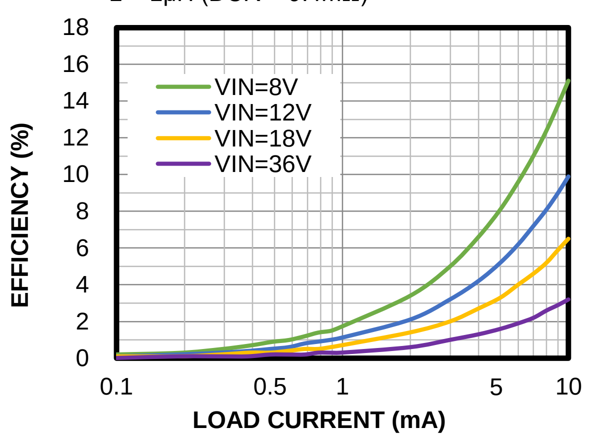
Efficiency vs. Load Current

AAM mode, V_{OUT} = 3.3V, f_{SW} = 2.2MHz, L = 1µH (DCR = 9.4mΩ)



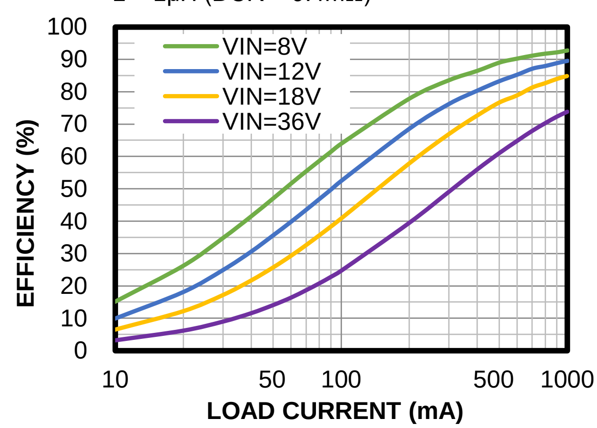
Efficiency vs. Load Current

FCCM, V_{OUT} = 3.3V, f_{SW} = 2.2MHz, L = 1µH (DCR = 9.4mΩ)



Efficiency vs. Load Current

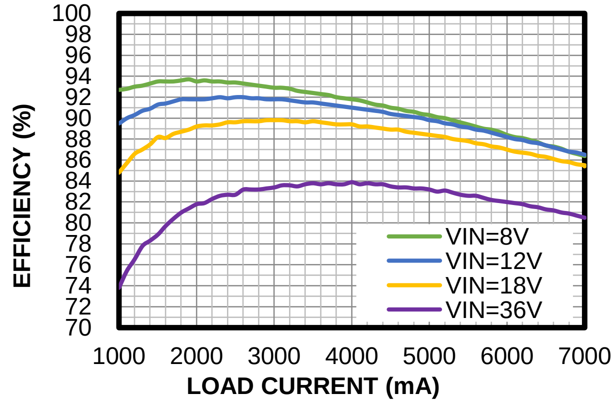
FCCM, V_{OUT} = 3.3V, f_{SW} = 2.2MHz, L = 1µH (DCR = 9.4mΩ)



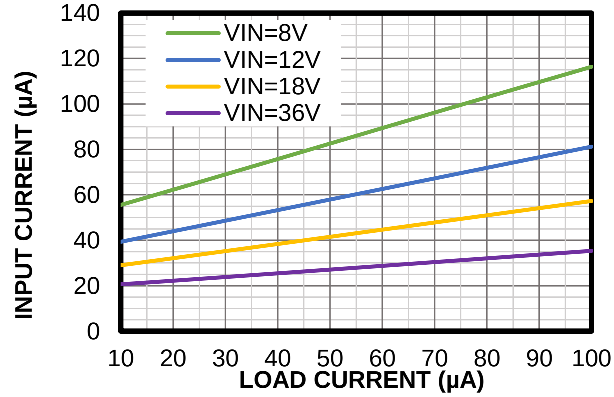
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 1µH, f_{SW} = 2.2MHz, AAM mode, BIAS connected to V_{OUT}, T_A = 25°C, unless otherwise noted.

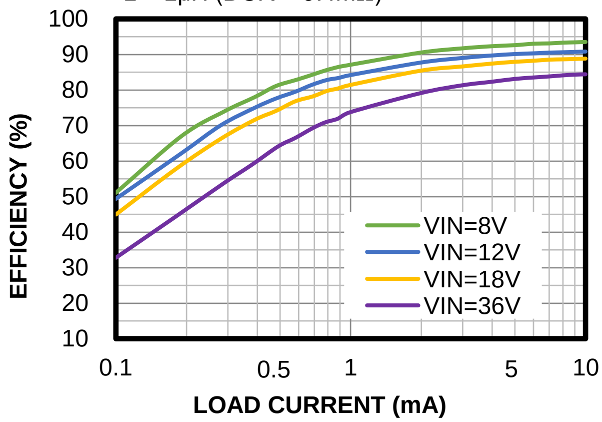
Efficiency vs. Load Current
FCCM, V_{OUT} = 3.3V, f_{SW} = 2.2MHz,
L = 1µH (DCR = 9.4mΩ)



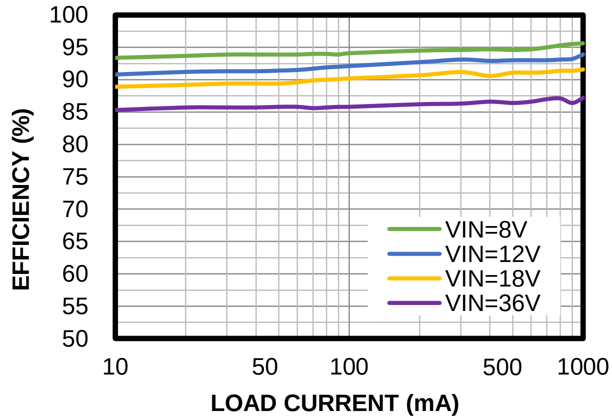
Input Current vs. Load Current
AAM mode, V_{OUT} = 5V, f_{SW} = 2.2MHz,
L = 1µH (DCR = 9.4mΩ)



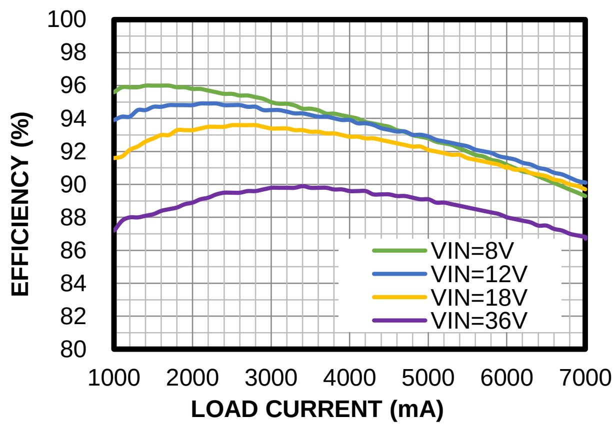
Efficiency vs. Load Current
AAM mode, V_{OUT} = 5V, f_{SW} = 2.2MHz,
L = 1µH (DCR = 9.4mΩ)



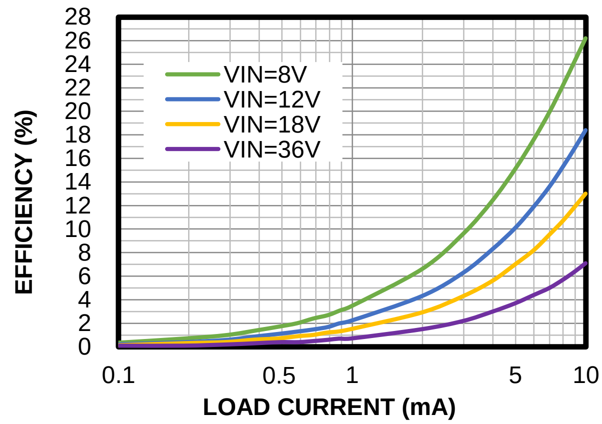
Efficiency vs. Load Current
AAM mode, V_{OUT} = 5V, f_{SW} = 2.2MHz,
L = 1µH (DCR = 9.4mΩ)



Efficiency vs. Load Current
AAM mode, V_{OUT} = 5V, f_{SW} = 2.2MHz,
L = 1µH (DCR = 9.4mΩ)



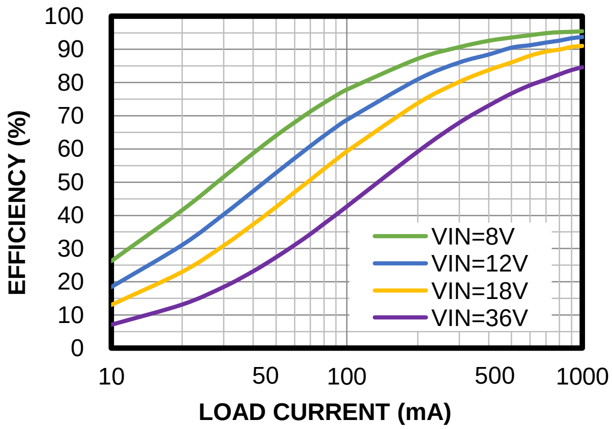
Efficiency vs. Load Current
FCCM, V_{OUT} = 5V, f_{SW} = 2.2MHz,
L = 1µH (DCR = 9.4mΩ)



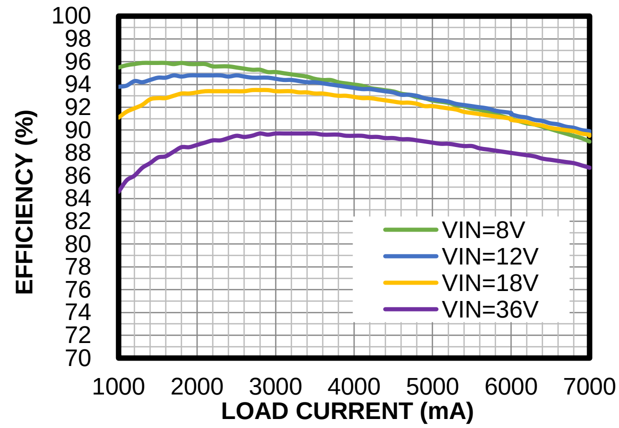
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 1µH, f_{SW} = 2.2MHz, AAM mode, T_A = 25°C, BIAS connected to V_{OUT}, unless otherwise noted.

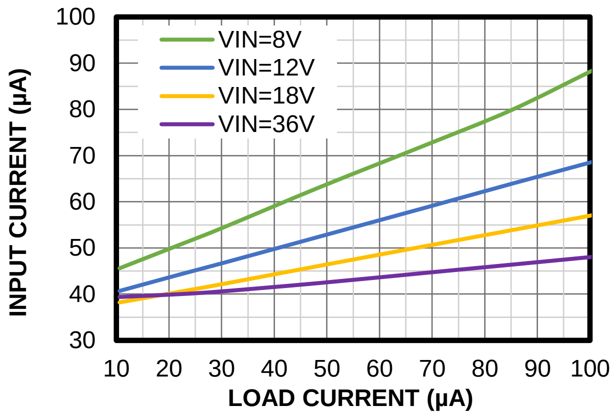
Efficiency vs. Load Current
FCCM, V_{OUT} = 5V, f_{SW} = 2.2MHz,
L = 1µH (DCR = 9.4mΩ)



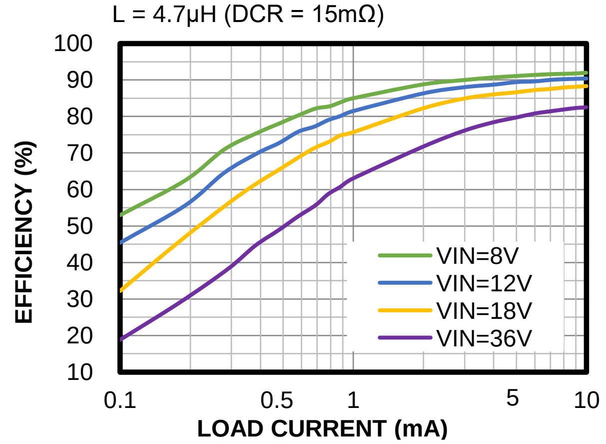
Efficiency vs. Load Current
FCCM, V_{OUT} = 5V, f_{SW} = 2.2MHz,
L = 1µH (DCR = 9.4mΩ)



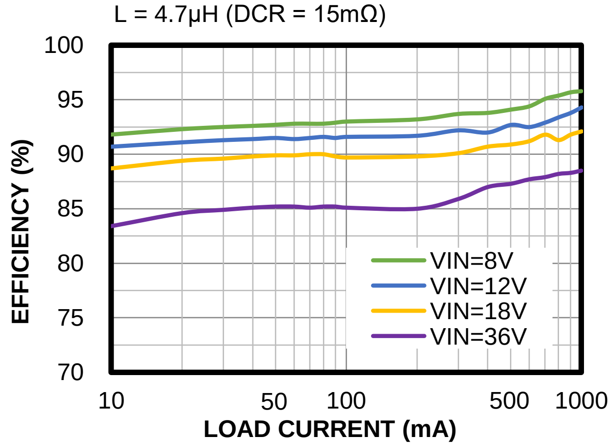
Input Current vs. Load Current
AAM mode, V_{OUT} = 3.3V, f_{SW} = 410kHz,
L = 4.7µH (DCR = 15mΩ)



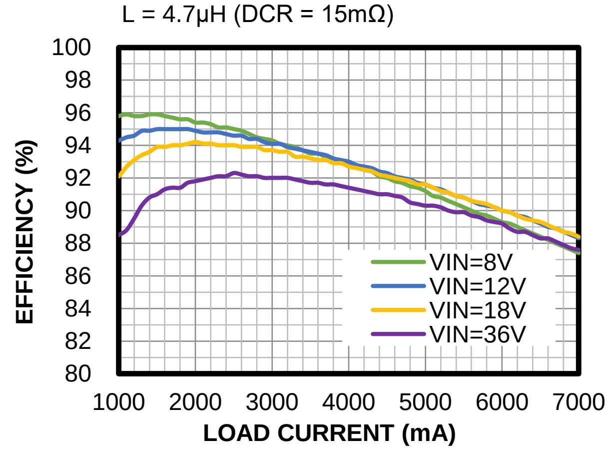
Efficiency vs. Load Current
AAM mode, V_{OUT} = 3.3V, f_{SW} = 410kHz,
L = 4.7µH (DCR = 15mΩ)



Efficiency vs. Load Current
AAM mode, V_{OUT} = 3.3V, f_{SW} = 410kHz,
L = 4.7µH (DCR = 15mΩ)



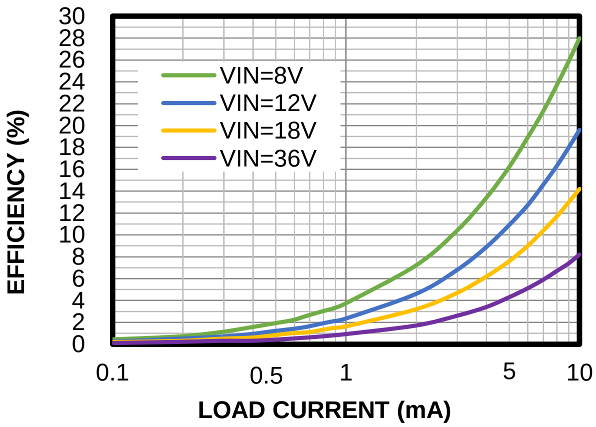
Efficiency vs. Load Current
AAM mode, V_{OUT} = 3.3V, f_{SW} = 410kHz,
L = 4.7µH (DCR = 15mΩ)



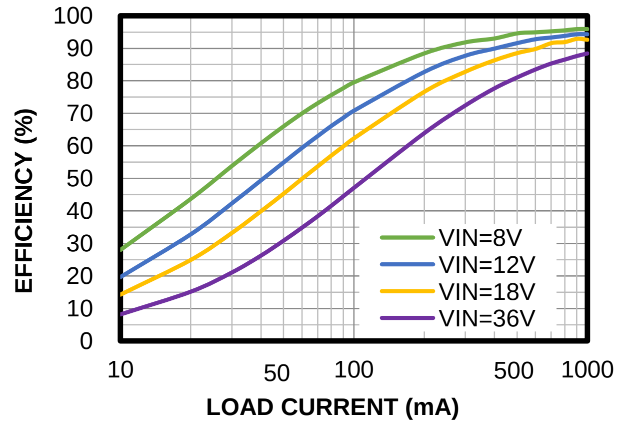
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 1µH, f_{SW} = 2.2MHz, AAM mode, BIAS connected to V_{OUT}, T_A = 25°C, unless otherwise noted.

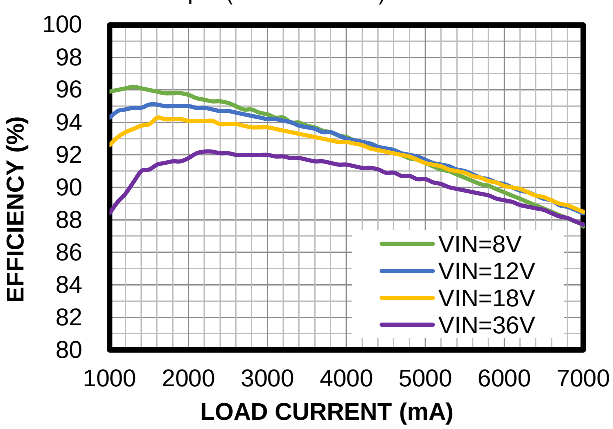
Efficiency vs. Load Current
FCCM, V_{OUT} = 3.3V, f_{SW} = 410kHz,
L = 4.7µH (DCR = 15mΩ)



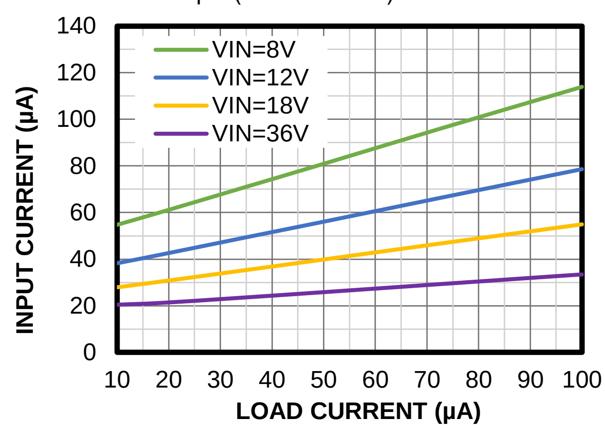
Efficiency vs. Load Current
FCCM, V_{OUT} = 3.3V, f_{SW} = 410kHz,
L = 4.7µH (DCR = 15mΩ)



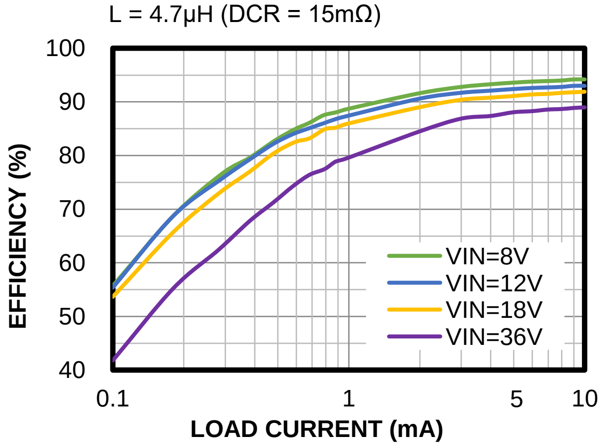
Efficiency vs. Load Current
FCCM, V_{OUT} = 3.3V, f_{SW} = 410kHz,
L = 4.7µH (DCR = 15mΩ)



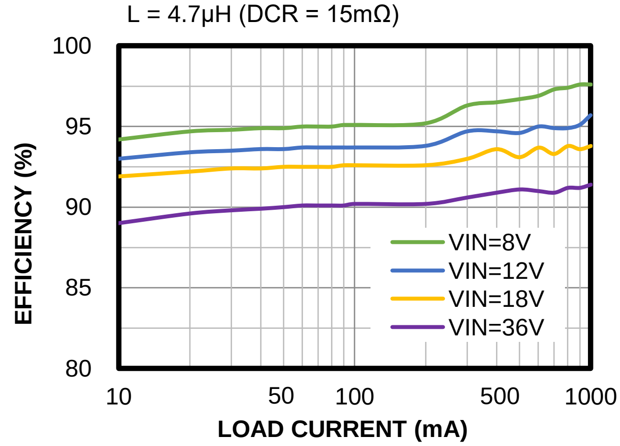
Input Current vs. Load Current
AAM mode, V_{OUT} = 5V, f_{SW} = 410kHz,
L = 4.7µH (DCR = 15mΩ)



Efficiency vs. Load Current
AAM mode, V_{OUT} = 5V, f_{SW} = 410kHz,
L = 4.7µH (DCR = 15mΩ)



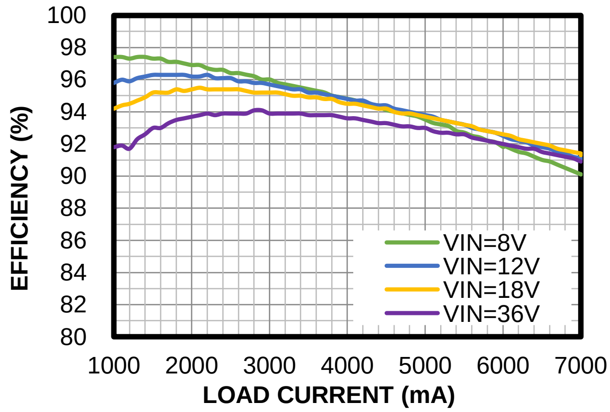
Efficiency vs. Load Current
AAM mode, V_{OUT} = 5V, f_{SW} = 410kHz,
L = 4.7µH (DCR = 15mΩ)



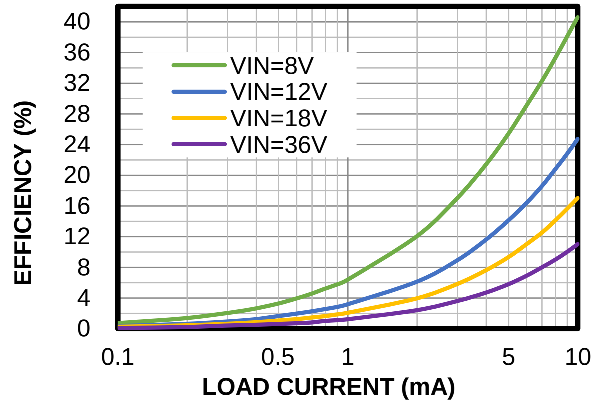
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 1µH, f_{SW} = 2.2MHz, AAM mode, BIAS connected to V_{OUT}, T_A = 25°C, unless otherwise noted.

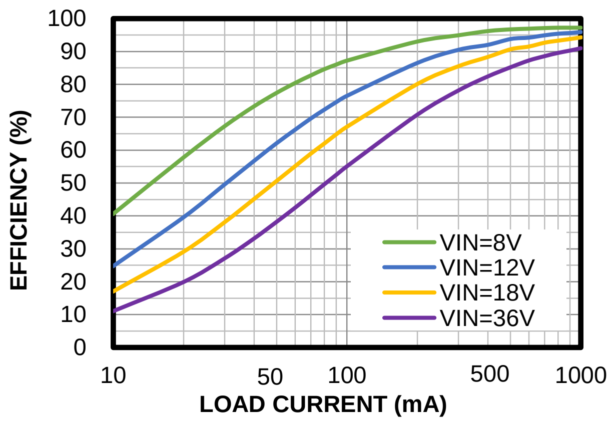
Efficiency vs. Load Current
AAM mode, V_{OUT} = 5V, f_{SW} = 410kHz,
L = 4.7µH (DCR = 15mΩ)



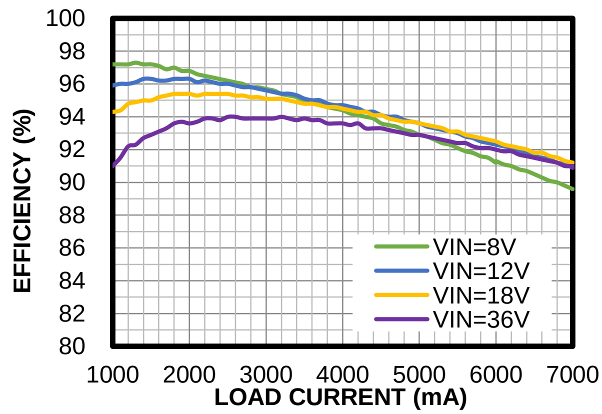
Efficiency vs. Load Current
FCCM, V_{OUT} = 5V, f_{SW} = 410kHz,
L = 4.7µH (DCR = 15mΩ)



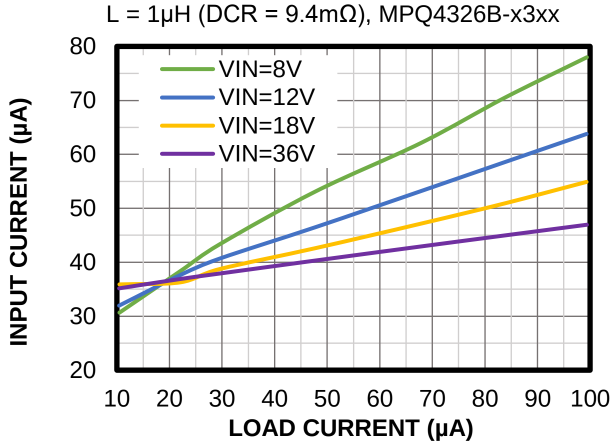
Efficiency vs. Load Current
FCCM, V_{OUT} = 5V, f_{SW} = 410kHz,
L = 4.7µH (DCR = 15mΩ)



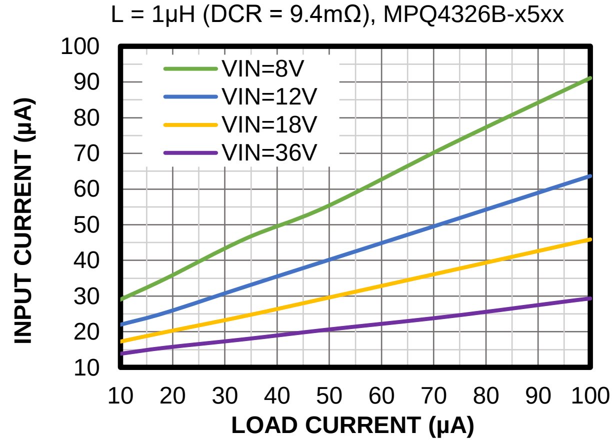
Efficiency vs. Load Current
FCCM, V_{OUT} = 5V, f_{SW} = 410kHz,
L = 4.7µH (DCR = 15mΩ)



Input Current vs. Load Current
AAM mode, V_{OUT} = 3.3V, f_{SW} = 2.2MHz,
L = 1µH (DCR = 9.4mΩ), MPQ4326B-x3xx



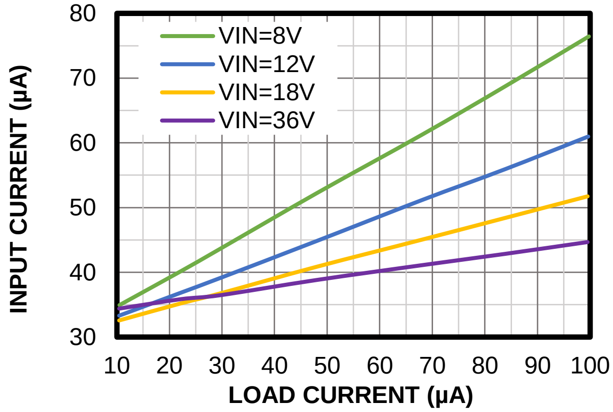
Input Current vs. Load Current
AAM mode, V_{OUT} = 5V, f_{SW} = 2.2MHz,
L = 1µH (DCR = 9.4mΩ), MPQ4326B-x5xx



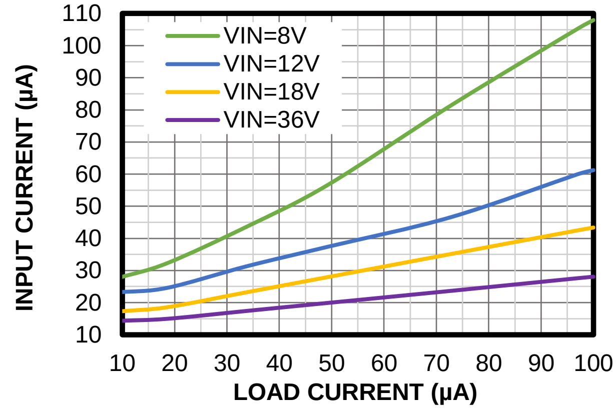
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 1µH, f_{SW} = 2.2MHz, AAM mode, BIAS connected to V_{OUT}, T_A = 25°C, unless otherwise noted.

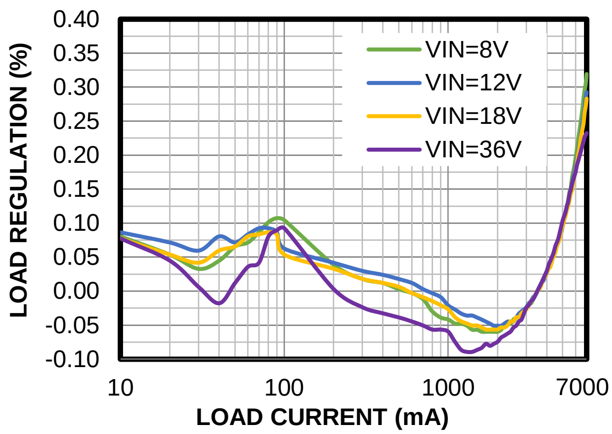
Input Current vs. Load Current
AAM mode, V_{OUT} = 3.3V, f_{SW} = 410kHz,
L = 4.7µH (DCR = 15mΩ), MPQ4326B-x3xx



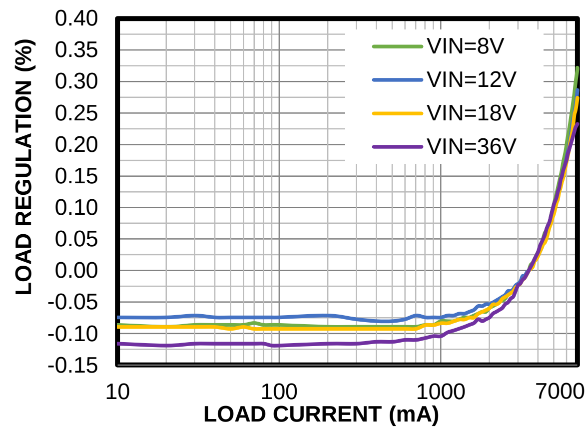
Input Current vs. Load Current
AAM mode, V_{OUT} = 5V, f_{SW} = 410kHz,
L = 4.7µH (DCR = 15mΩ), MPQ4326B-x5xx



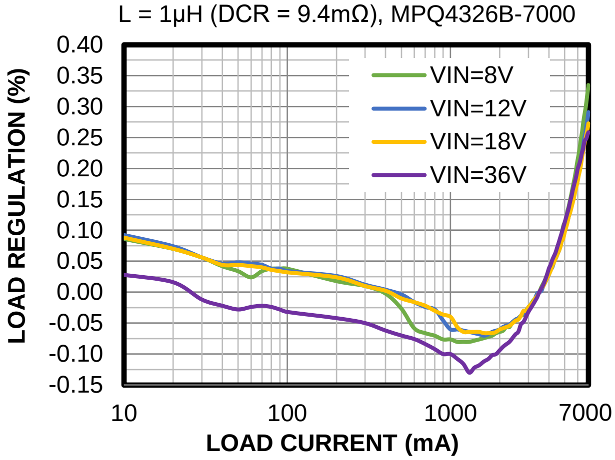
Load Regulation
AAM mode, V_{OUT} = 3.3V,f_{SW} = 2.2MHz,
L = 1µH (DCR = 9.4mΩ), MPQ4326B-7000



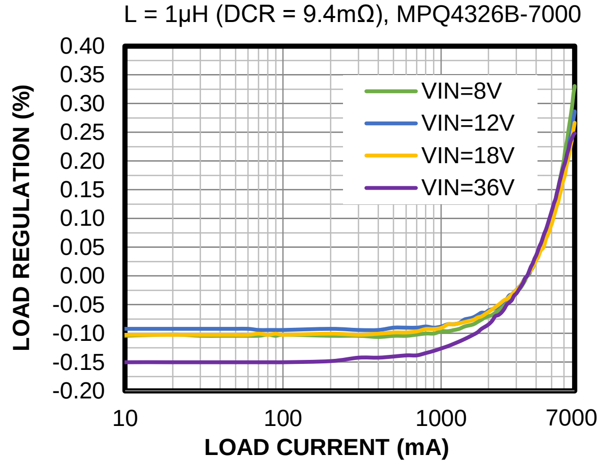
Load Regulation
FCCM, V_{OUT} = 3.3V,f_{SW} = 2.2MHz,
L = 1µH (DCR = 9.4mΩ), MPQ4326B-7000



Load Regulation
AAM mode, V_{OUT} = 5V, f_{SW} = 2.2MHz,
L = 1µH (DCR = 9.4mΩ), MPQ4326B-7000



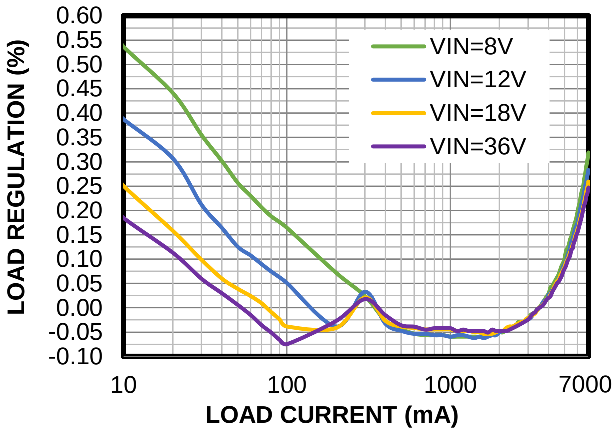
Load Regulation
FCCM, V_{OUT} = 5V, f_{SW} = 2.2MHz,
L = 1µH (DCR = 9.4mΩ), MPQ4326B-7000



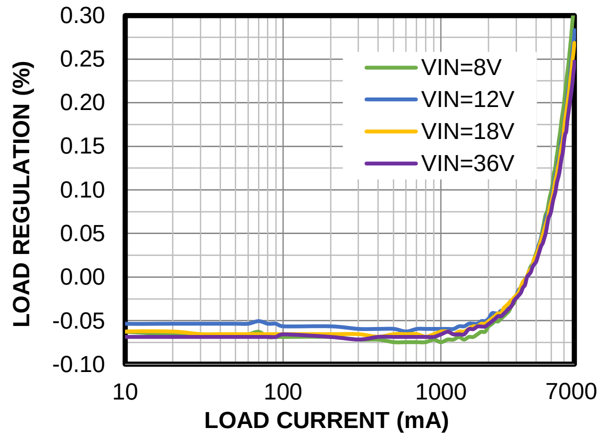
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 1µH, f_{SW} = 2.2MHz, AAM mode, BIAS connected to V_{OUT}, T_A = 25°C, unless otherwise noted.

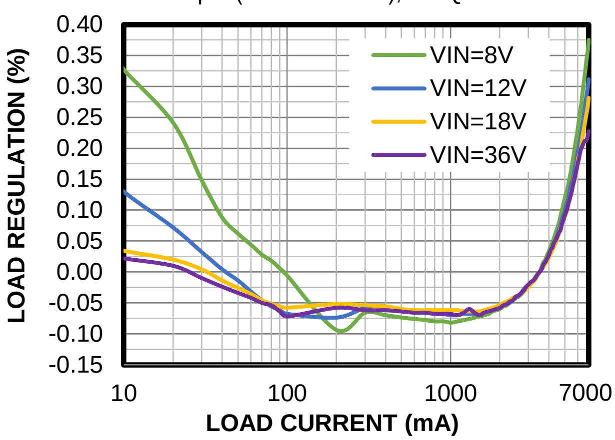
Load Regulation
AAM mode, V_{OUT} = 3.3V, f_{SW} = 410kHz,
L = 4.7µH (DCR = 15mΩ), MPQ4326B-7000



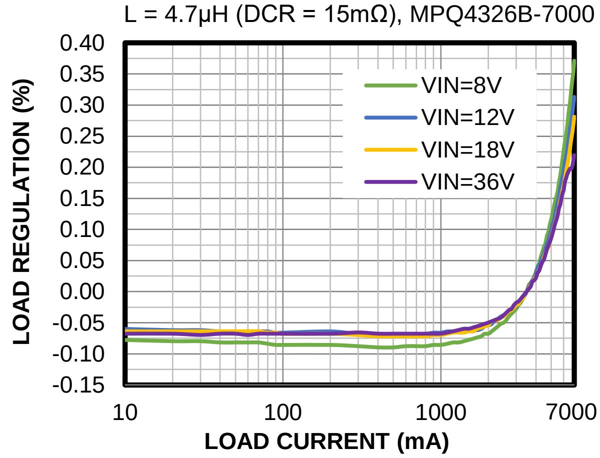
Load Regulation
FCCM, V_{OUT} = 3.3V, f_{SW} = 410kHz,
L = 4.7µH (DCR = 15mΩ), MPQ4326B-7000



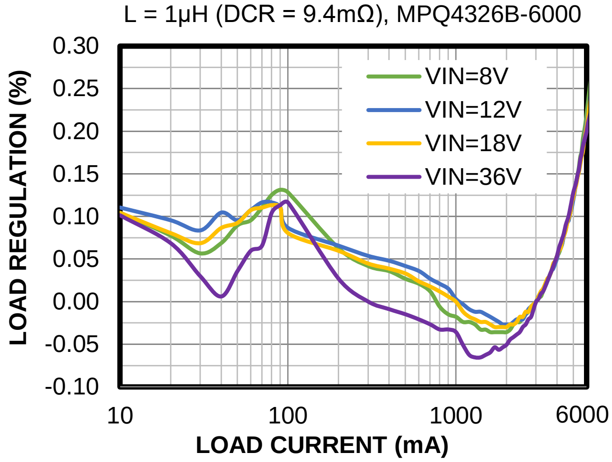
Load Regulation
AAM mode, V_{OUT} = 5V, f_{SW} = 410kHz,
L = 4.7µH (DCR = 15mΩ), MPQ4326B-7000



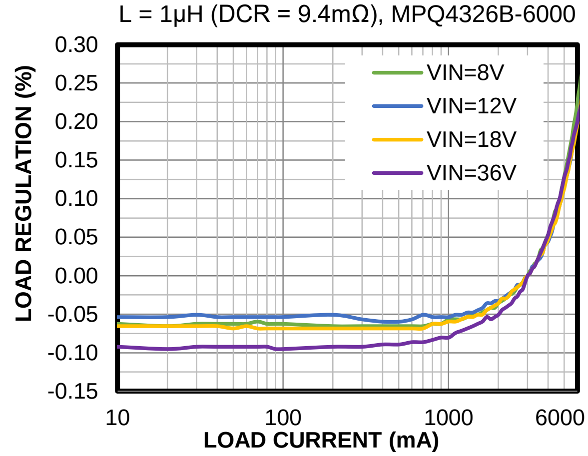
Load Regulation
FCCM, V_{OUT} = 5V, f_{SW} = 410kHz,
L = 4.7µH (DCR = 15mΩ), MPQ4326B-7000



Load Regulation
AAM mode, V_{OUT} = 3.3V, f_{SW} = 2.2MHz,
L = 1µH (DCR = 9.4mΩ), MPQ4326B-6000



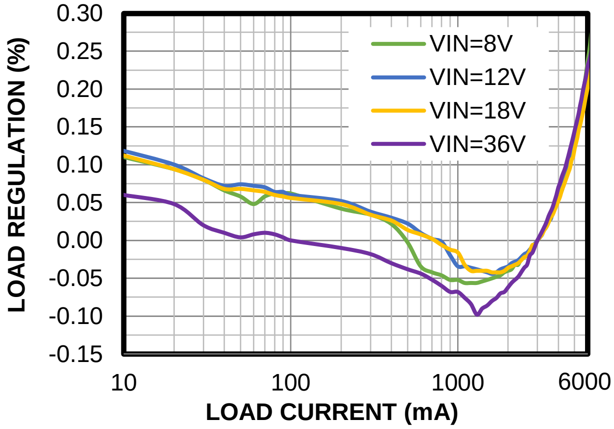
Load Regulation
FCCM, V_{OUT} = 3.3V, f_{SW} = 2.2MHz,
L = 1µH (DCR = 9.4mΩ), MPQ4326B-6000



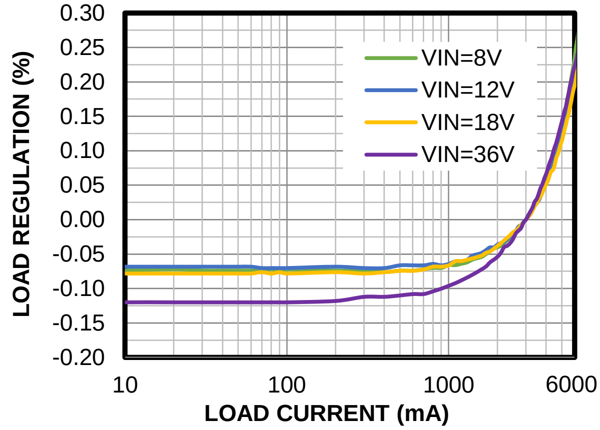
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 1µH, f_{SW} = 2.2MHz, AAM mode, BIAS connected to V_{OUT}, T_A = 25°C, unless otherwise noted.

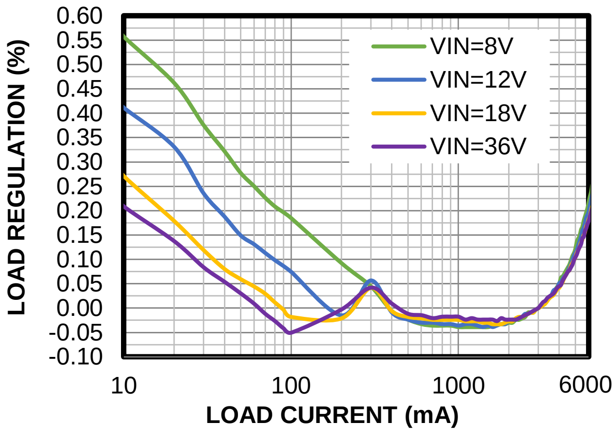
Load Regulation
AAM mode, V_{OUT} = 5V, f_{SW} = 2.2MHz,
L = 1µH (DCR = 9.4mΩ), MPQ4326B-6000



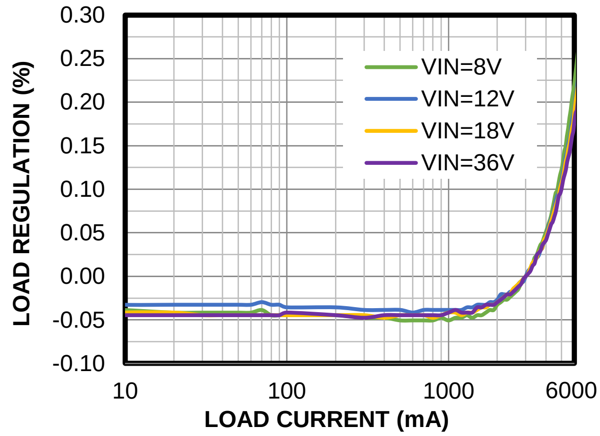
Load Regulation
FCCM, V_{OUT} = 5V, f_{SW} = 2.2MHz,
L = 1µH (DCR = 9.4mΩ), MPQ4326B-6000



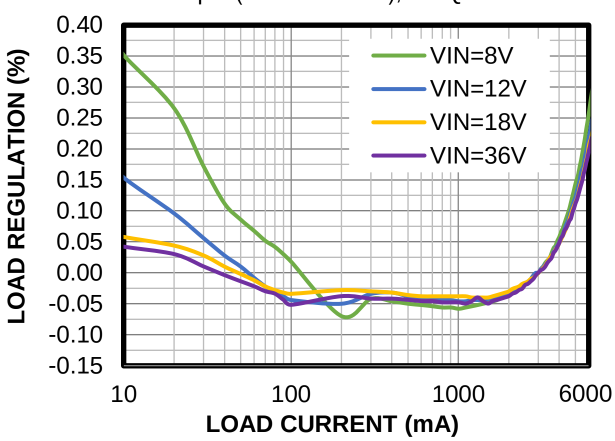
Load Regulation
AAM mode, V_{OUT} = 3.3V, f_{SW} = 410kHz,
L = 4.7µH (DCR = 15mΩ), MPQ4326B-6000



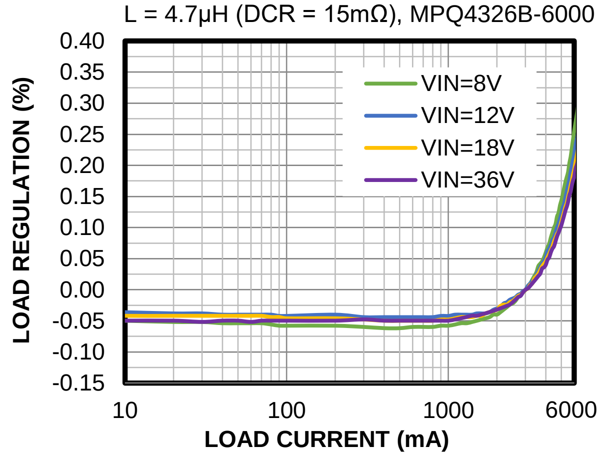
Load Regulation
FCCM, V_{OUT} = 3.3V, f_{SW} = 410kHz,
L = 4.7µH (DCR = 15mΩ), MPQ4326B-6000



Load Regulation
AAM mode, V_{OUT} = 5V, f_{SW} = 410kHz,
L = 4.7µH (DCR = 15mΩ), MPQ4326B-6000



Load Regulation
FCCM, V_{OUT} = 5V, f_{SW} = 410kHz,
L = 4.7µH (DCR = 15mΩ), MPQ4326B-6000

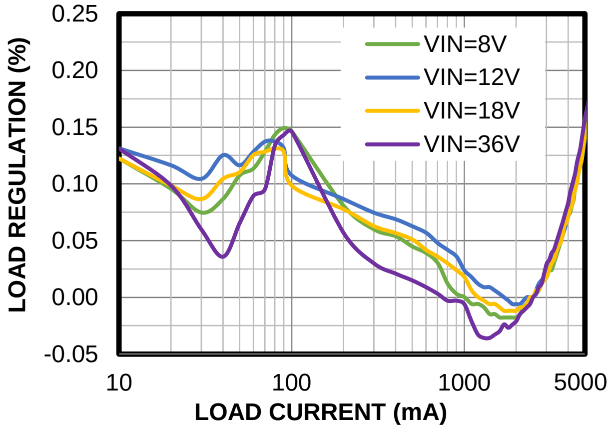


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 1µH, f_{SW} = 2.2MHz, AAM mode, BIAS connected to V_{OUT}, T_A = 25°C, unless otherwise noted.

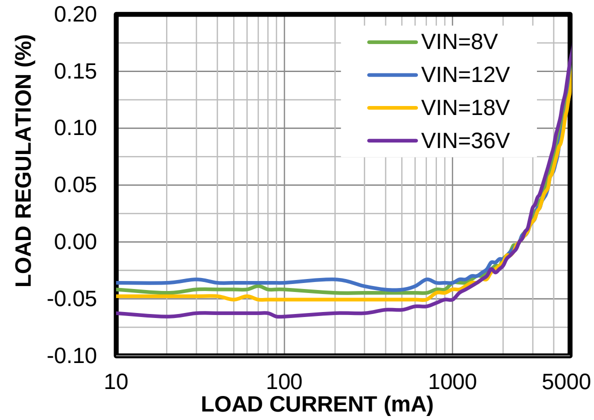
Load Regulation

AAM mode, V_{OUT} = 3.3V,f_{SW} = 2.2MHz,
L = 1µH (DCR = 9.4mΩ), MPQ4326B-5000



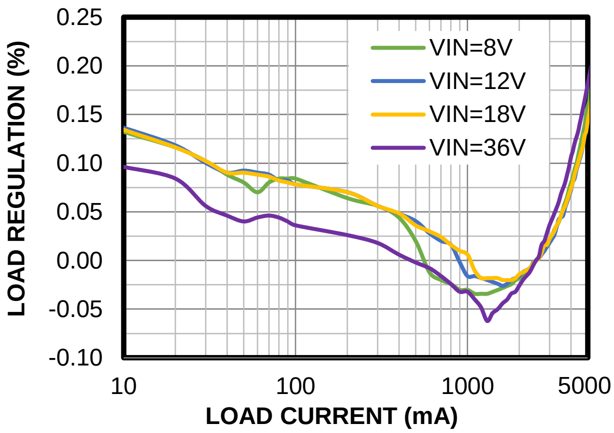
Load Regulation

FCCM, V_{OUT} = 3.3V,f_{SW} = 2.2MHz,
L = 1µH (DCR = 9.4mΩ), MPQ4326B-5000



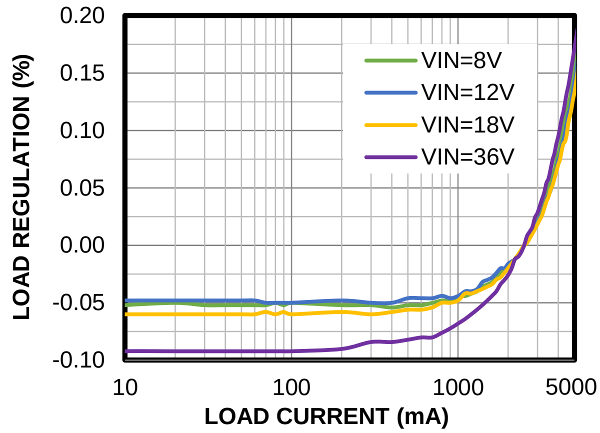
Load Regulation

AAM mode, V_{OUT} = 5V,f_{SW} = 2.2MHz,
L = 1µH (DCR = 9.4mΩ), MPQ4326B-5000



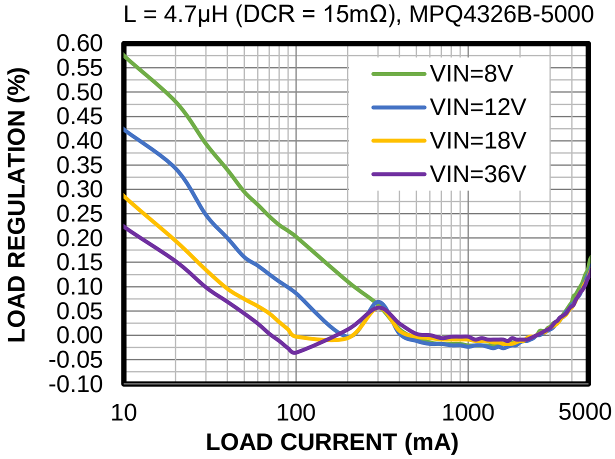
Load Regulation

FCCM, V_{OUT} = 5V,f_{SW} = 2.2MHz,
L = 1µH (DCR = 9.4mΩ), MPQ4326B-5000



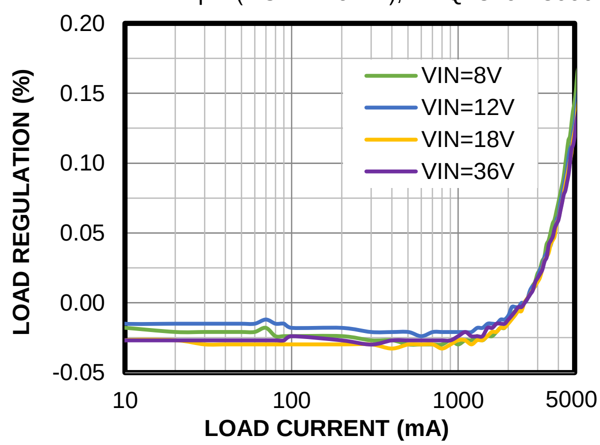
Load Regulation

AAM mode, V_{OUT} = 3.3V, f_{SW} = 410kHz,
L = 4.7µH (DCR = 15mΩ), MPQ4326B-5000



Load Regulation

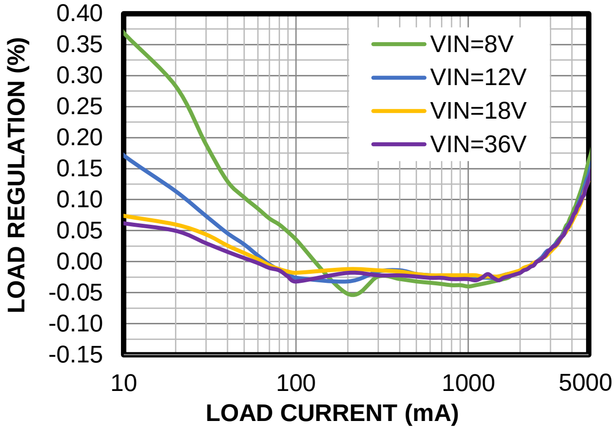
FCCM, V_{OUT} = 3.3V, f_{SW} = 410kHz,
L = 4.7µH (DCR = 15mΩ), MPQ4326B-5000



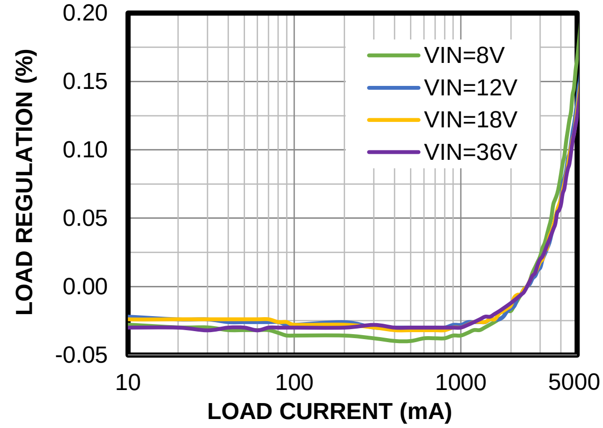
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 1µH, f_{SW} = 2.2MHz, AAM mode, BIAS connected to V_{OUT}, T_A = 25°C, unless otherwise noted.

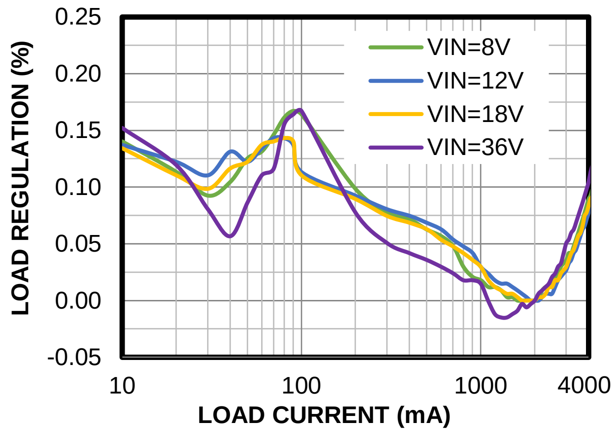
Load Regulation
AAM mode, V_{OUT} = 5V, f_{SW} = 410kHz,
L = 4.7µH (DCR = 15mΩ), MPQ4326B-5000



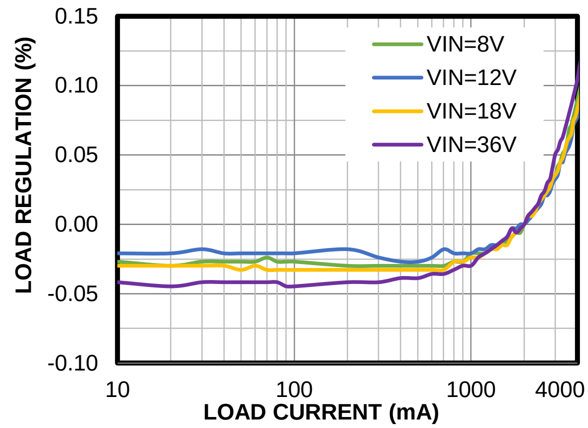
Load Regulation
FCCM, V_{OUT} = 5V, f_{SW} = 410kHz,
L = 4.7µH (DCR = 15mΩ), MPQ4326B-5000



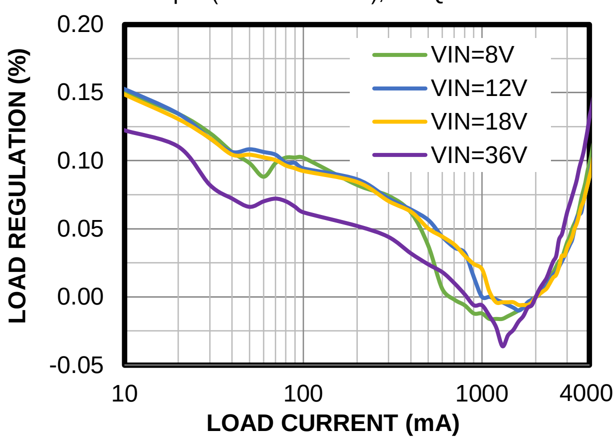
Load Regulation
AAM mode, V_{OUT} = 3.3V,f_{SW} = 2.2MHz,
L = 1µH (DCR = 9.4mΩ), MPQ4326B-4000



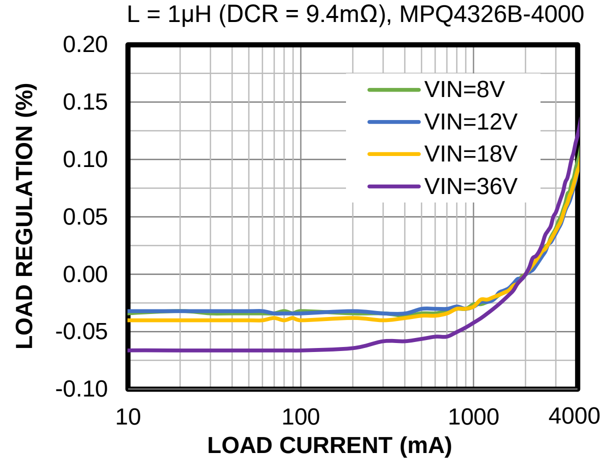
Load Regulation
FCCM, V_{OUT} = 3.3V,f_{SW} = 2.2MHz,
L = 1µH (DCR = 9.4mΩ), MPQ4326B-4000



Load Regulation
AAM mode, V_{OUT} = 5V,f_{SW} = 2.2MHz,
L = 1µH (DCR = 9.4mΩ), MPQ4326B-4000



Load Regulation
FCCM, V_{OUT} = 5V,f_{SW} = 2.2MHz,
L = 1µH (DCR = 9.4mΩ), MPQ4326B-4000

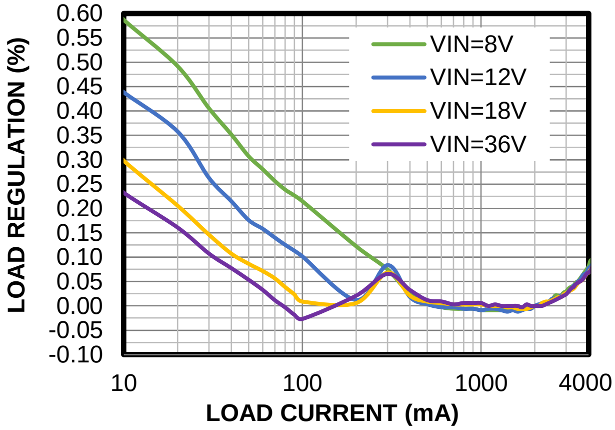


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 1µH, f_{SW} = 2.2MHz, AAM mode, BIAS connected to V_{OUT}, T_A = 25°C, unless otherwise noted.

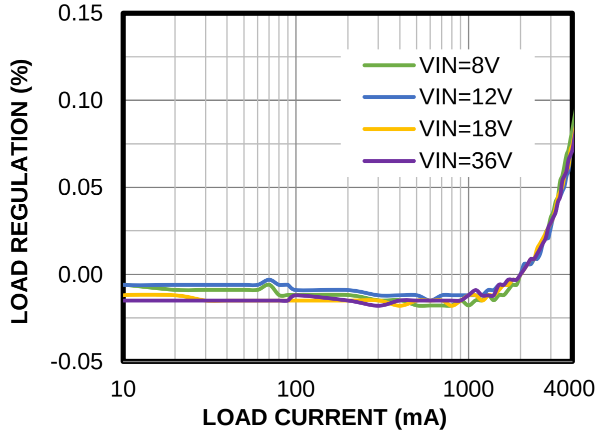
Load Regulation

AAM mode, V_{OUT} = 3.3V, f_{SW} = 410kHz,
L = 4.7µH (DCR = 15mΩ), MPQ4326B-4000



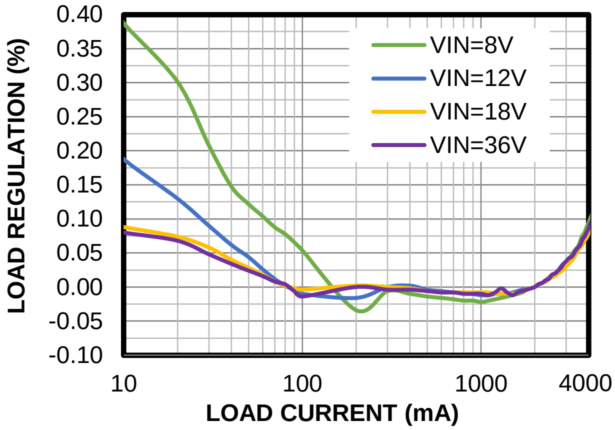
Load Regulation

FCCM, V_{OUT} = 3.3V, f_{SW} = 410kHz,
L = 4.7µH (DCR = 15mΩ), MPQ4326B-4000



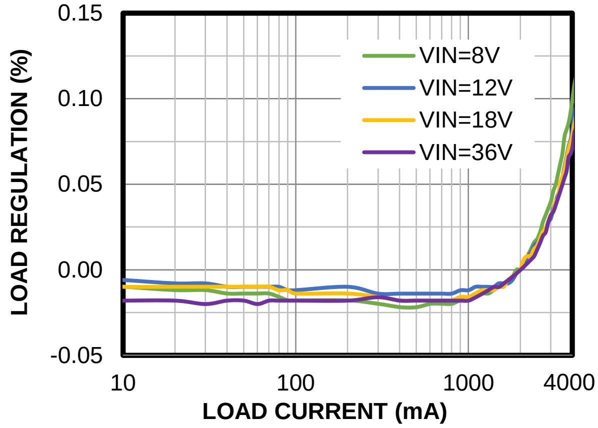
Load Regulation

AAM mode, V_{OUT} = 5V, f_{SW} = 410kHz,
L = 4.7µH (DCR = 15mΩ), MPQ4326B-4000



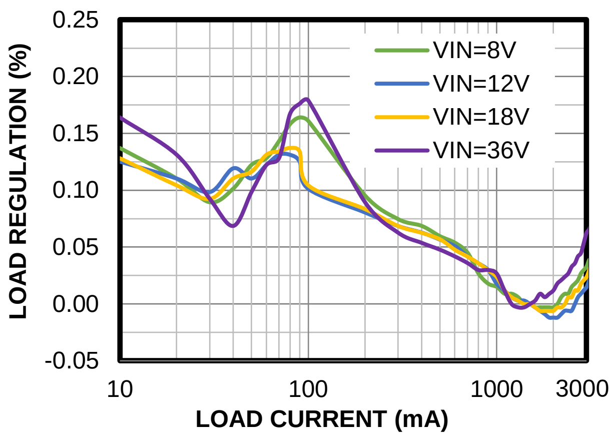
Load Regulation

FCCM, V_{OUT} = 5V, f_{SW} = 410kHz,
L = 4.7µH (DCR = 15mΩ), MPQ4326B-4000



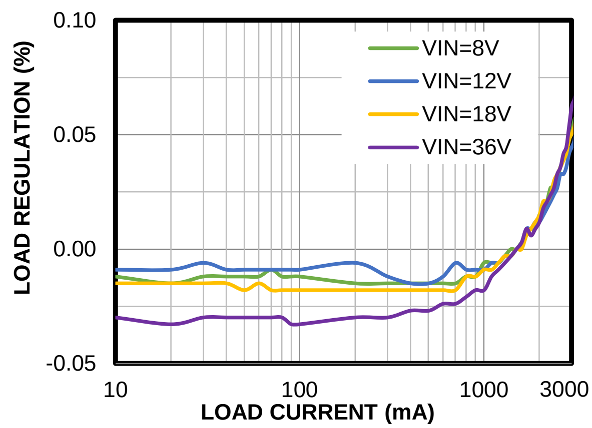
Load Regulation

AAM mode, V_{OUT} = 3.3V,f_{SW} = 2.2MHz,
L = 1µH (DCR = 9.4mΩ), MPQ4326B-3000



Load Regulation

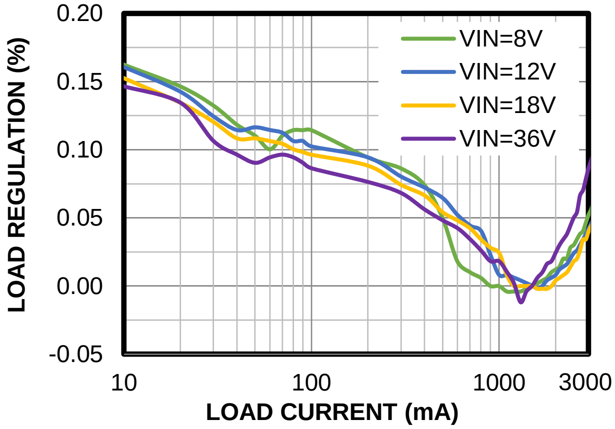
FCCM, V_{OUT} = 3.3V,f_{SW} = 2.2MHz,
L = 1µH (DCR = 9.4mΩ), MPQ4326B-3000



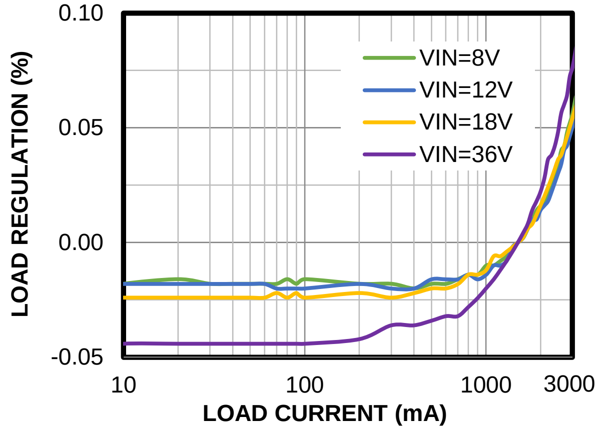
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 1µH, f_{SW} = 2.2MHz, AAM mode, BIAS connected to V_{OUT}, T_A = 25°C, unless otherwise noted.

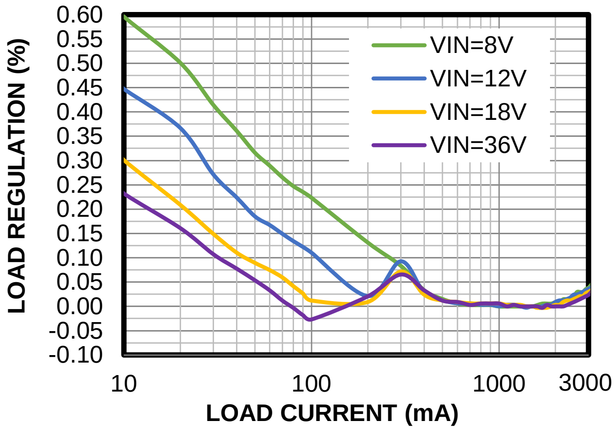
Load Regulation
AAM mode, V_{OUT} = 5V,f_{SW} = 2.2MHz,
L = 1µH (DCR = 9.4mΩ), MPQ4326B-3000



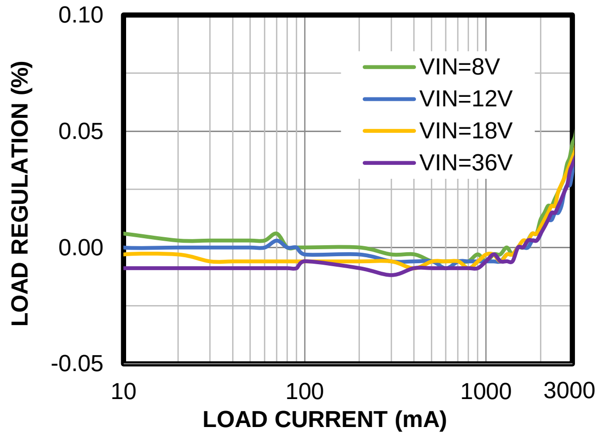
Load Regulation
FCCM, V_{OUT} = 5V,f_{SW} = 2.2MHz,
L = 1µH (DCR = 9.4mΩ), MPQ4326B-3000



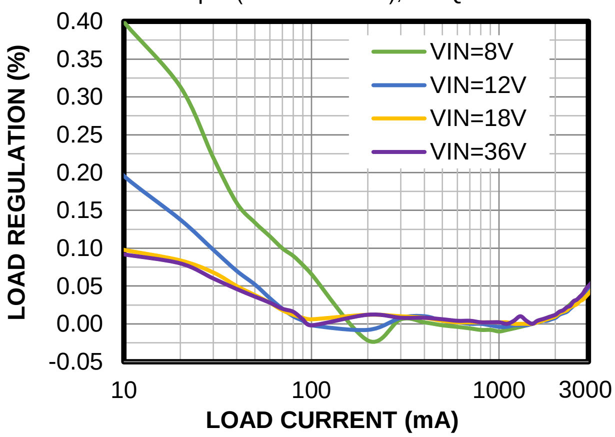
Load Regulation
AAM mode, V_{OUT} = 3.3V, f_{SW} = 410kHz,
L = 4.7µH (DCR = 15mΩ), MPQ4326B-3000



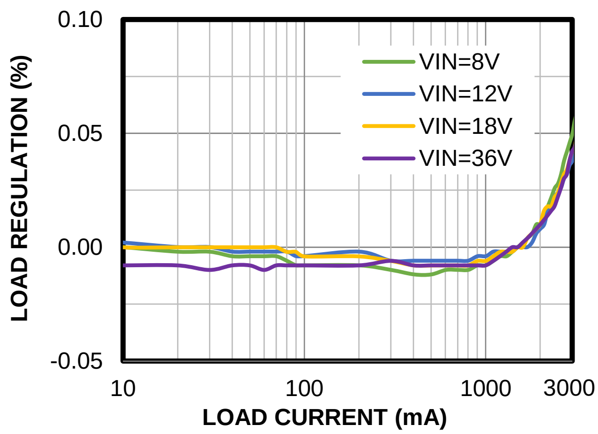
Load Regulation
FCCM, V_{OUT} = 3.3V, f_{SW} = 410kHz,
L = 4.7µH (DCR = 15mΩ), MPQ4326B-3000



Load Regulation
AAM mode, V_{OUT} = 5V, f_{SW} = 410kHz,
L = 4.7µH (DCR = 15mΩ), MPQ4326B-3000



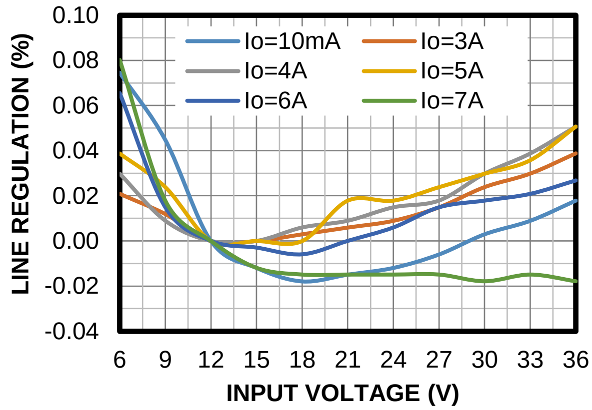
Load Regulation
FCCM, V_{OUT} = 5V, f_{SW} = 410kHz,
L = 4.7µH (DCR = 15mΩ), MPQ4326B-3000



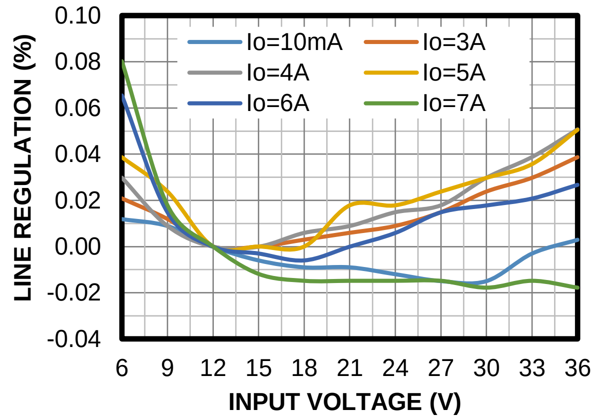
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 1µH, f_{SW} = 2.2MHz, AAM mode, BIAS connected to V_{OUT}, T_A = 25°C, unless otherwise noted.

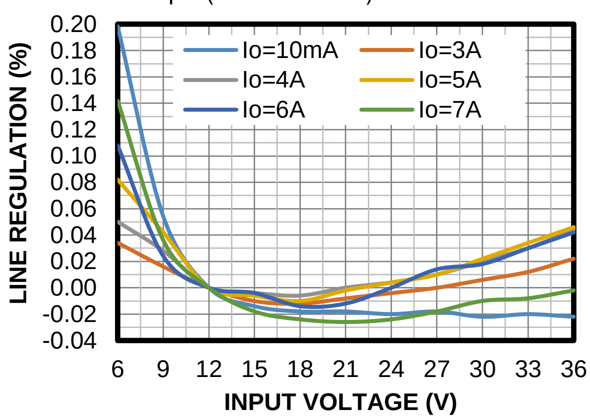
Line Regulation
AAM mode, V_{OUT} = 3.3V, f_{SW} = 2.2MHz,
L = 1µH (DCR = 9.4mΩ)



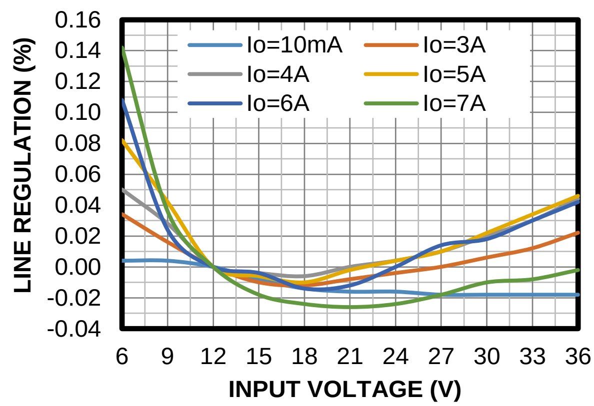
Line Regulation
FCCM, V_{OUT} = 3.3V, f_{SW} = 2.2MHz,
L = 1µH (DCR = 9.4mΩ)



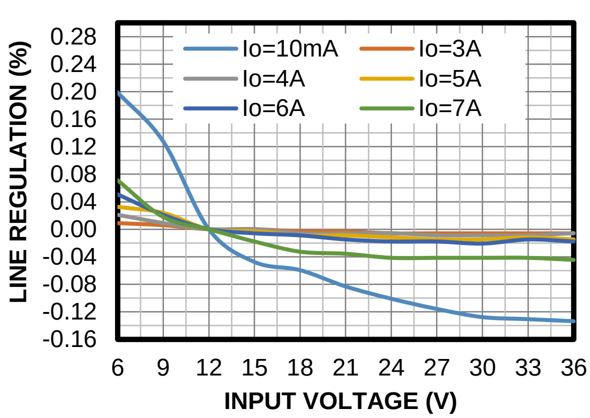
Line Regulation
AAM mode, V_{OUT} = 5V, f_{SW} = 2.2MHz,
L = 1µH (DCR = 9.4mΩ)



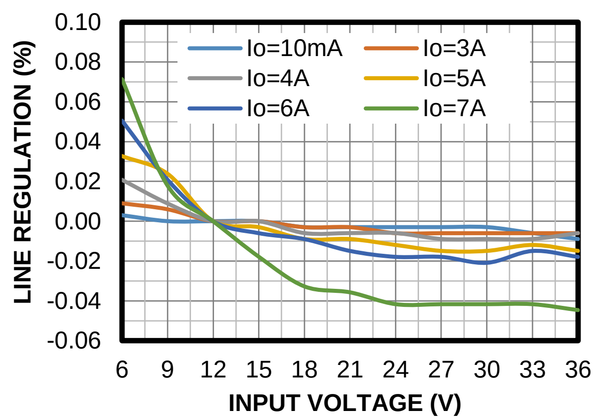
Line Regulation
FCCM, V_{OUT} = 5V, f_{SW} = 2.2MHz,
L = 1µH (DCR = 9.4mΩ)



Line Regulation
AAM mode, V_{OUT} = 3.3V, f_{SW} = 410kHz,
L = 4.7µH (DCR = 15mΩ)



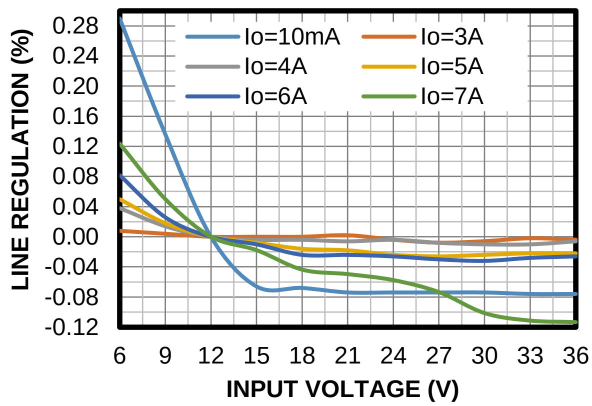
Line Regulation
FCCM, V_{OUT} = 3.3V, f_{SW} = 410kHz,
L = 4.7µH (DCR = 15mΩ)



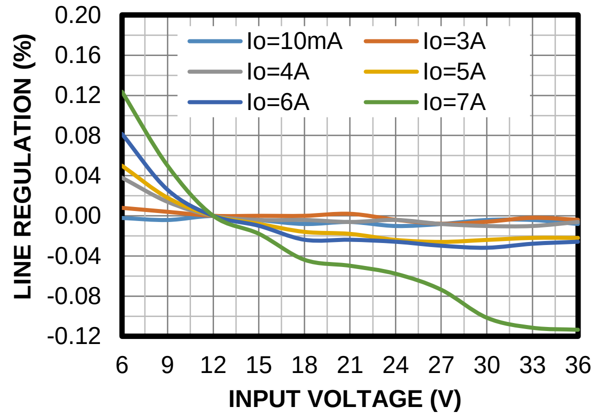
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 1µH, f_{SW} = 2.2MHz, AAM mode, BIAS connected to V_{OUT}, T_A = 25°C, unless otherwise noted.

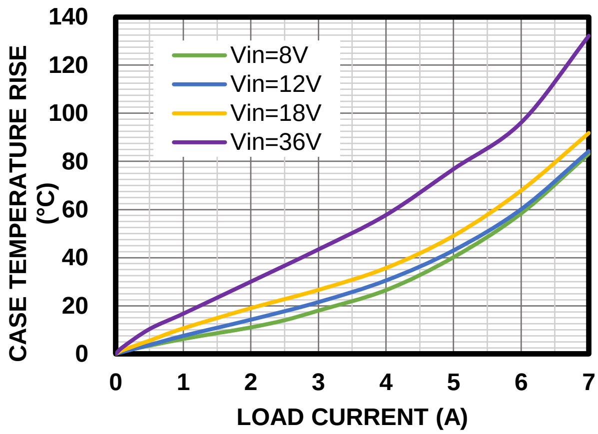
Line Regulation
AAM mode, V_{OUT} = 5V, f_{SW} = 410kHz,
L = 4.7µH (DCR = 15mΩ)



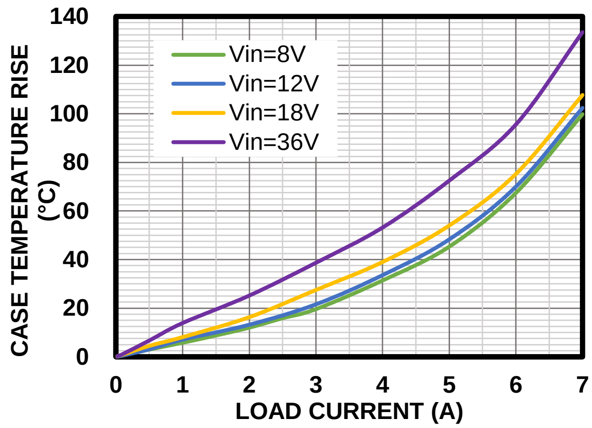
Line Regulation
FCCM, V_{OUT} = 5V, f_{SW} = 410kHz,
L = 4.7µH (DCR = 15mΩ)



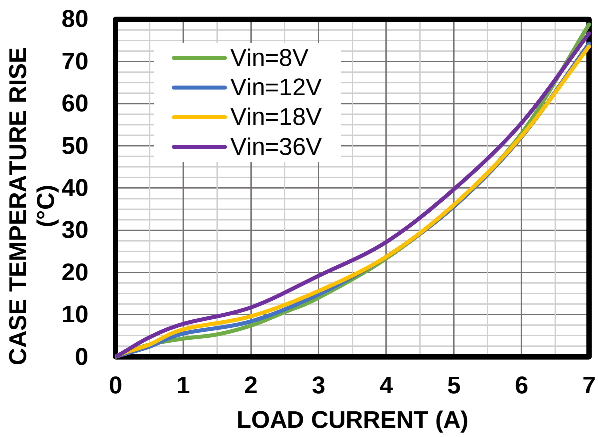
Case Temperature Rise
V_{OUT} = 3.3V, f_{SW} = 2.2MHz,
L = 1µH (DCR = 9.4mΩ)



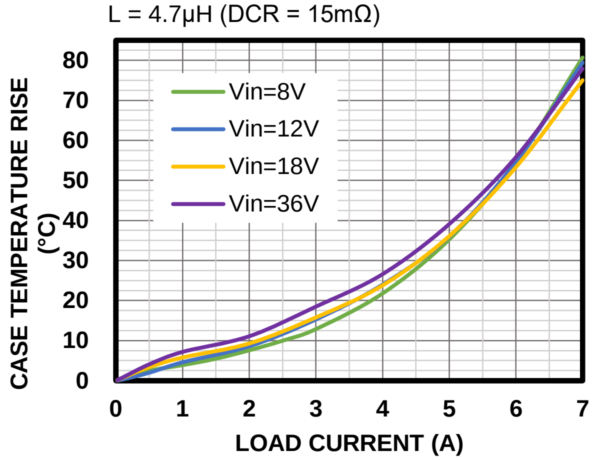
Case Temperature Rise
V_{OUT} = 5V, f_{SW} =2.2MHz,
L = 1µH (DCR = 9.4mΩ)



Case Temperature Rise
V_{OUT} = 3.3V, f_{SW} = 410kHz,
L = 4.7µH (DCR = 15mΩ)



Case Temperature Rise
V_{OUT} = 5V, f_{SW} = 410kHz,
L = 4.7µH (DCR = 15mΩ)

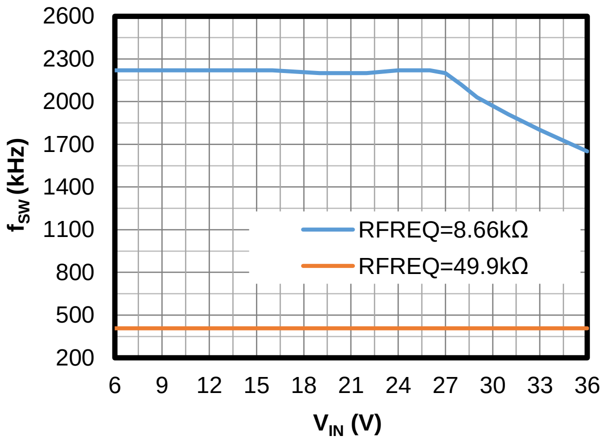


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 1µH, f_{SW} = 2.2MHz, AAM mode, BIAS connected to V_{OUT}, T_A = 25°C, unless otherwise noted.

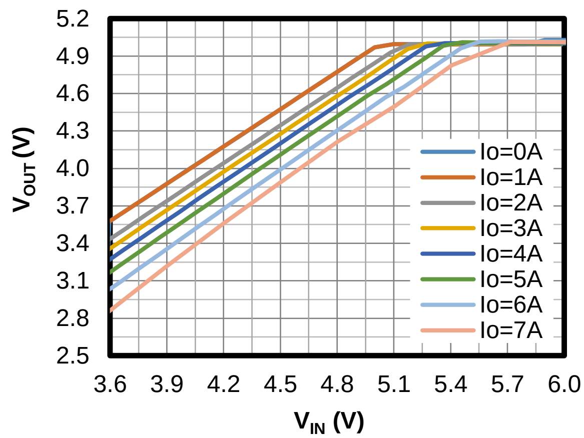
f_{SW} vs. V_{IN}

V_{OUT} = 3.3V



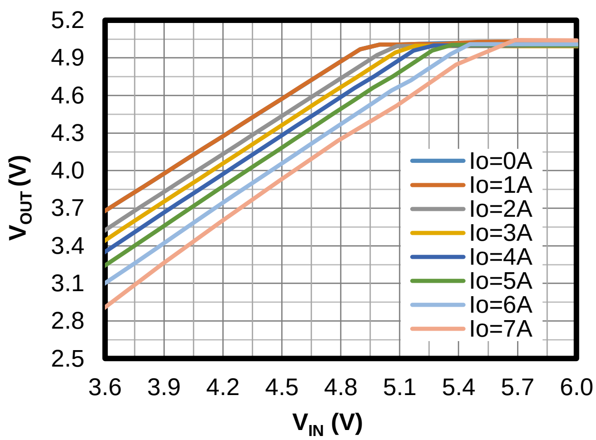
Low-Dropout Mode

V_{OUT} = 5V, f_{SW} = 2.2MHz,
L = 1µH (DCR = 9.4mΩ)



Low-Dropout Mode

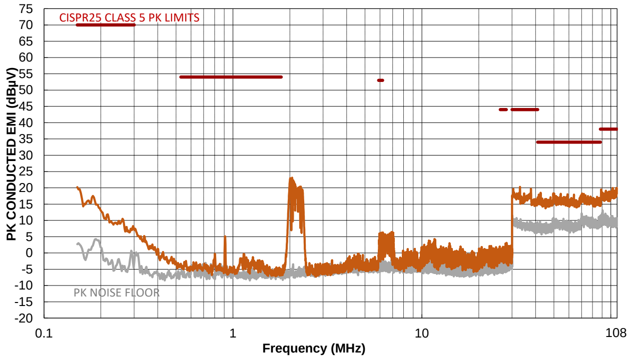
V_{OUT} = 5V, f_{SW} = 410kHz,
L = 4.7µH (DCR = 15mΩ)



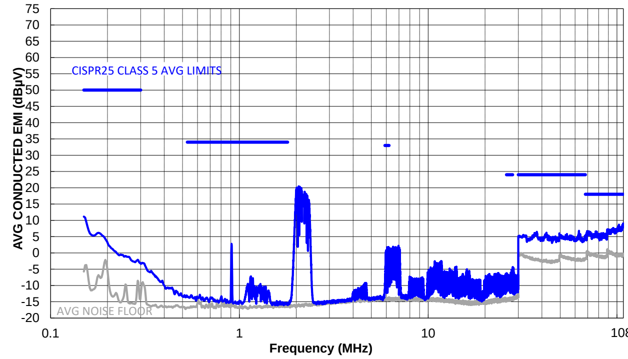
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 1µH (12), f_{SW} = 2.2MHz, T_A = 25°C, unless otherwise noted. (13)

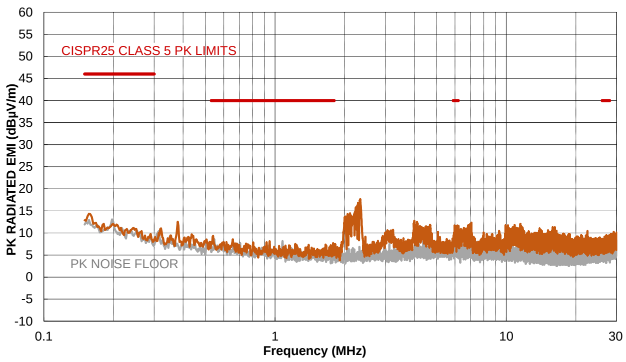
CISPR 25 Class 5 Peak Conducted Emissions
150kHz to 108MHz



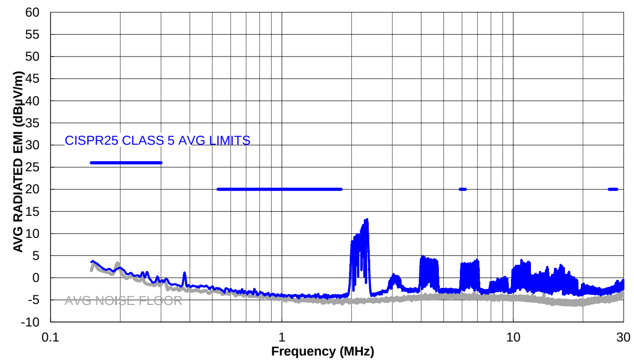
CISPR 25 Class 5 Average Conducted Emissions
150kHz to 108MHz



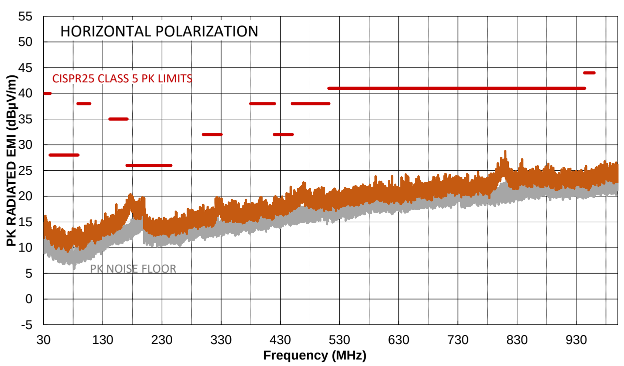
CISPR 25 Class 5 Peak Radiated Emissions
150kHz to 30MHz



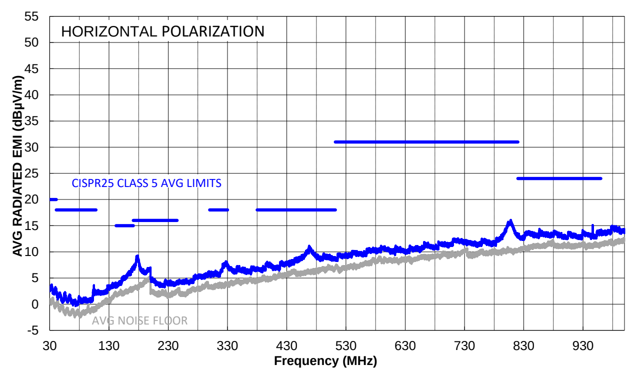
CISPR 25 Class 5 Average Radiated Emissions
150kHz to 30MHz



CISPR 25 Class 5 Peak Radiated Emissions
Horizontal, 30MHz to 1GHz



CISPR 25 Class 5 Average Radiated Emissions
Horizontal, 30MHz to 1GHz

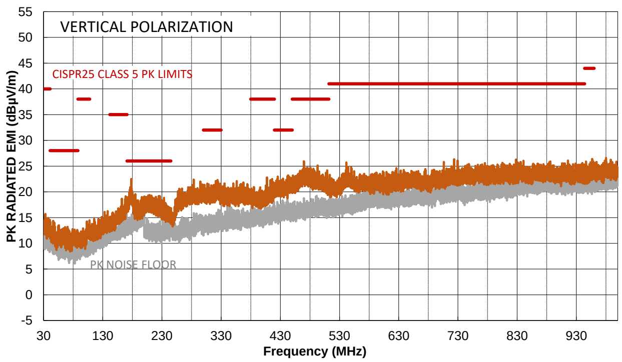


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 1µH (12), f_{SW} = 2.2MHz, T_A = 25°C, unless otherwise noted. (13)

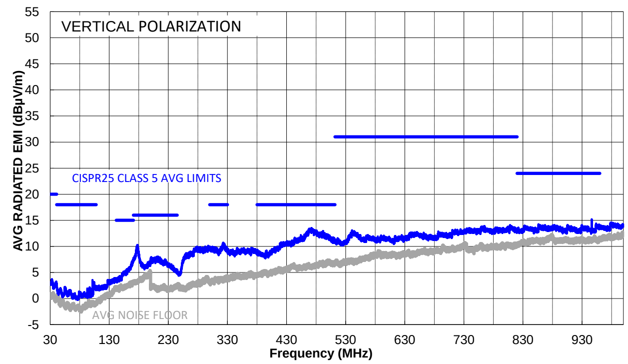
CISPR 25 Class 5 Peak Radiated Emissions

Vertical, 30MHz to 1GHz



CISPR 25 Class 5 Average Radiated Emissions

Vertical, 30MHz to 1GHz



Notes:

12) Inductor part number: XEL4020-102MEB; DCR = 14.6mΩ.

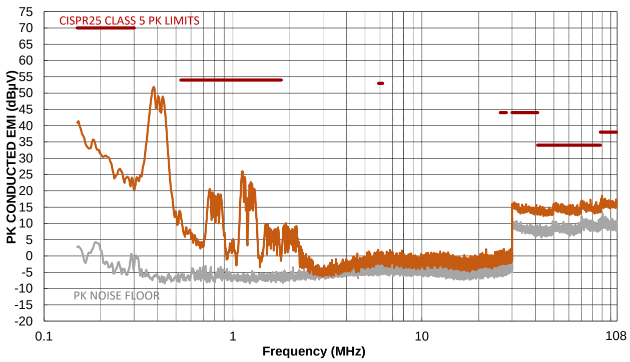
13) The EMC test results are based on the application circuit with EMI filters (see Figure 22 on page 67).

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH [14], f_{SW} = 410kHz, T_A = 25°C, unless otherwise noted. [15]

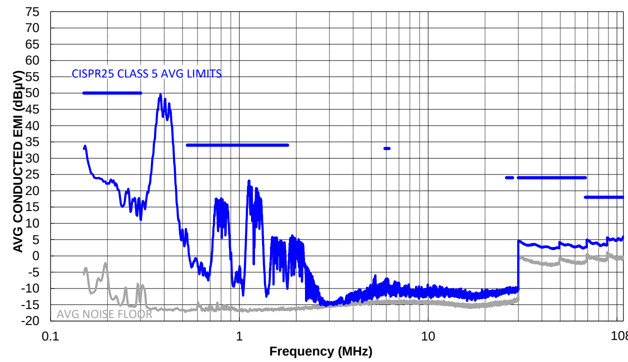
CISPR 25 Class 5 Peak Conducted Emissions

150kHz to 108MHz



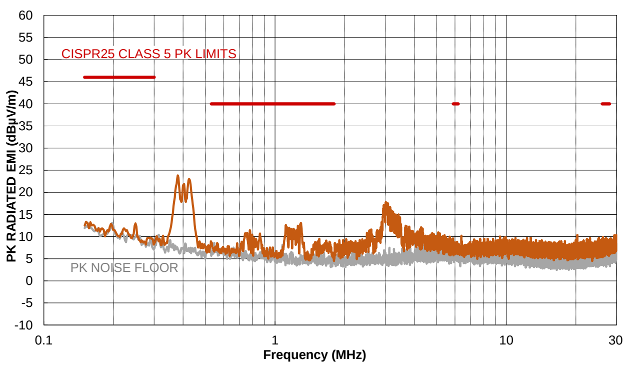
CISPR 25 Class 5 Average Conducted Emissions

150kHz to 108MHz



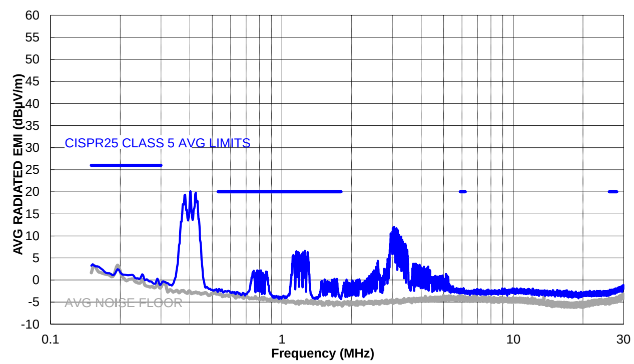
CISPR 25 Class 5 Peak Radiated Emissions

150kHz to 30MHz



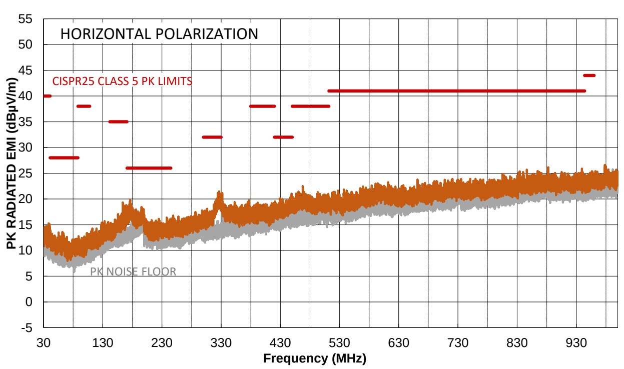
CISPR 25 Class 5 Average Radiated Emissions

150kHz to 30MHz



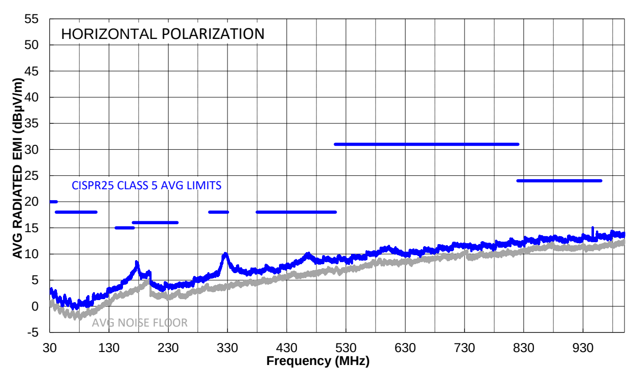
CISPR 25 Class 5 Peak Radiated Emissions

Horizontal, 30MHz to 1GHz



CISPR 25 Class 5 Average Radiated Emissions

Horizontal, 30MHz to 1GHz

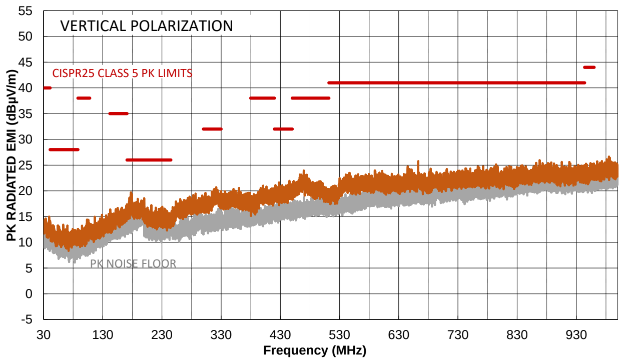


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH (14), f_{SW} = 410kHz, T_A = 25°C, unless otherwise noted. (15)

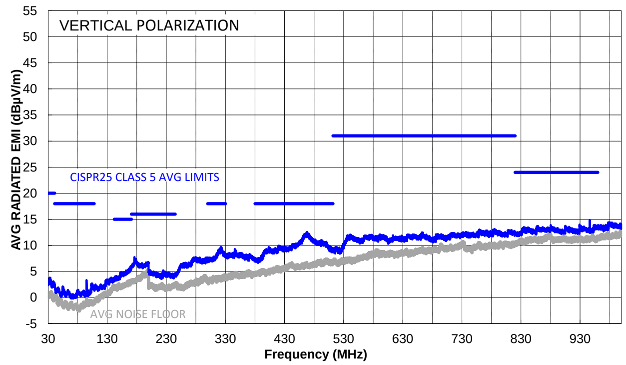
CISPR 25 Class 5 Peak Radiated Emissions

Vertical, 30MHz to 1GHz



CISPR 25 Class 5 Average Radiated Emissions

Vertical, 30MHz to 1GHz



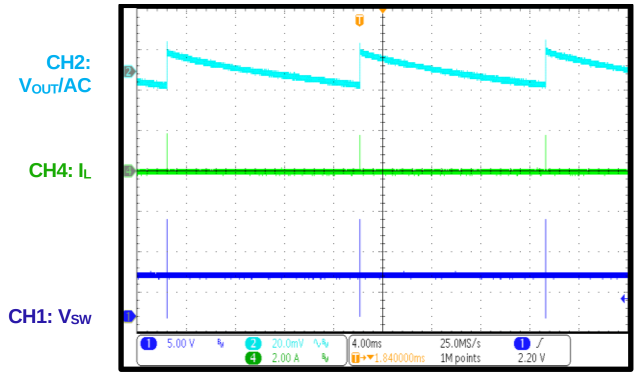
Notes:

14) Inductor part number: XEL6060-472MEB/C; DCR = 15.02mΩ.
15) The EMC test results are based on the application circuit with EMI filters (see Figure 23 on page 68).

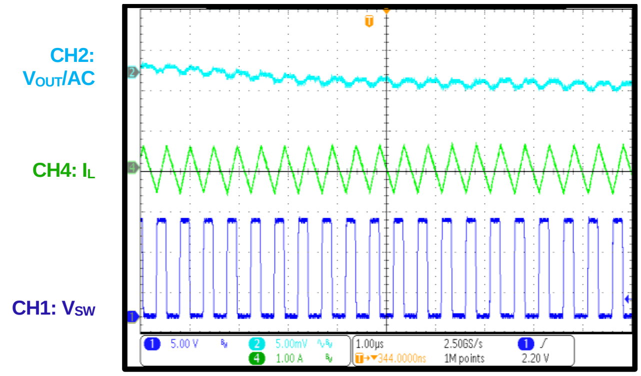
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 1µH, f_{SW} = 2.2MHz, AAM mode, T_A = 25°C, unless otherwise noted.

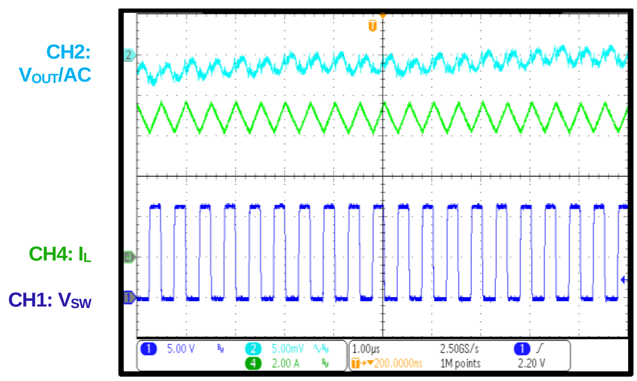
Steady State
I_{OUT} = 0A, AAM mode



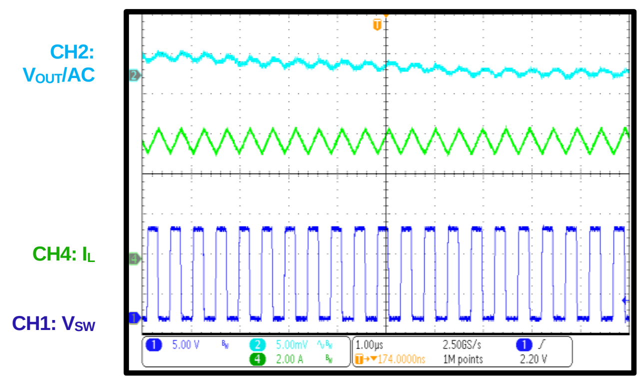
Steady State
I_{OUT} = 0A, FCCM



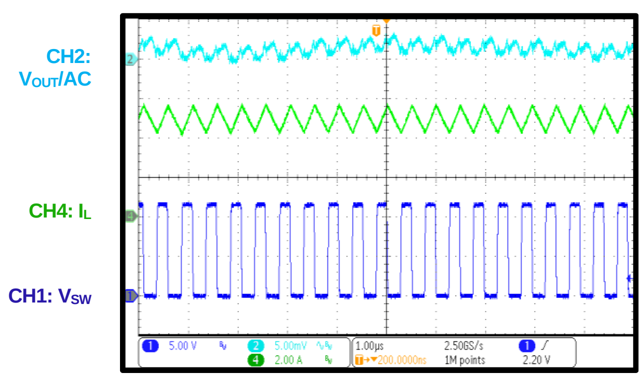
Steady State
I_{OUT} = 7A, MPQ4326B-7000



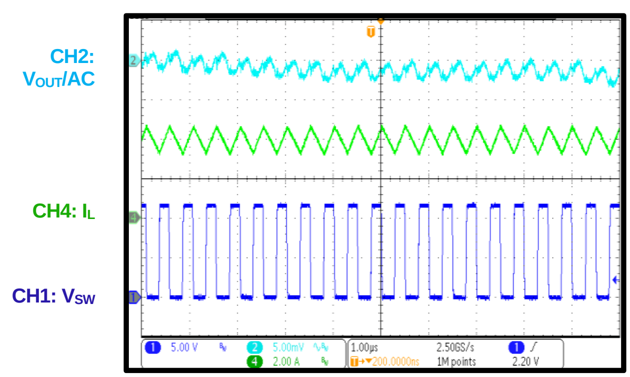
Steady State
I_{OUT} = 6A, MPQ4326B-6000



Steady State
I_{OUT} = 5A, MPQ4326B-5000



Steady State
I_{OUT} = 4A, MPQ4326B-4000

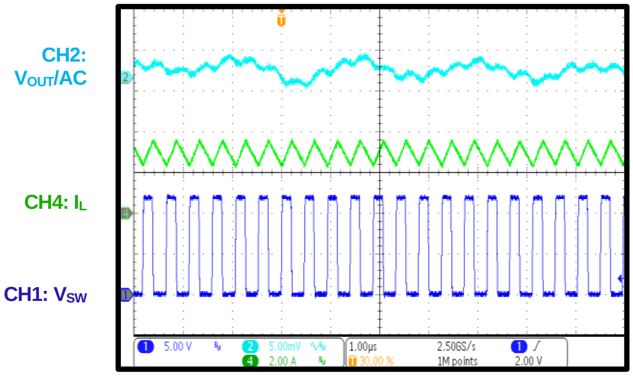


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 1µH, f_{SW} = 2.2MHz, AAM mode, T_A = 25°C, unless otherwise noted.

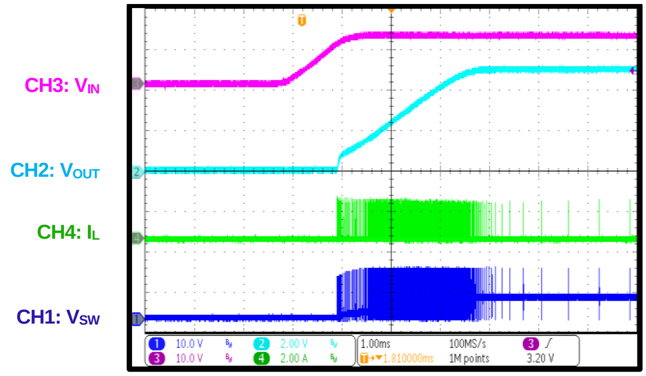
Steady State

I_{OUT} = 3A, MPQ4326B-3000



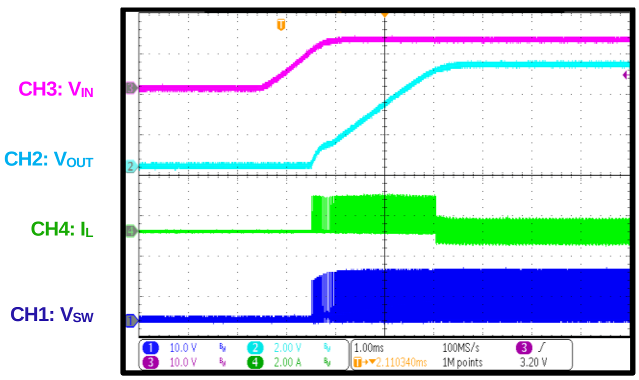
Start-Up through VIN

I_{OUT} = 0A, AAM mode



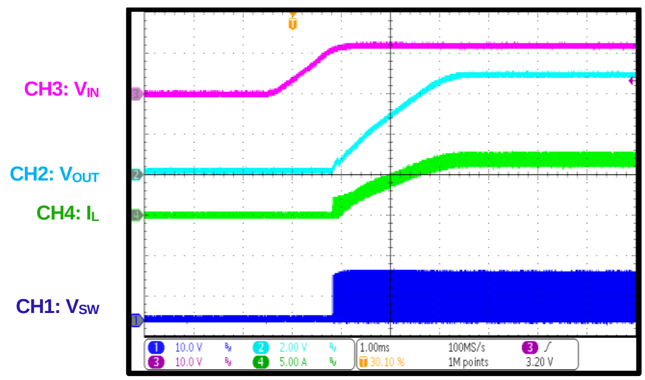
Start-Up through VIN

I_{OUT} = 0A, FCCM



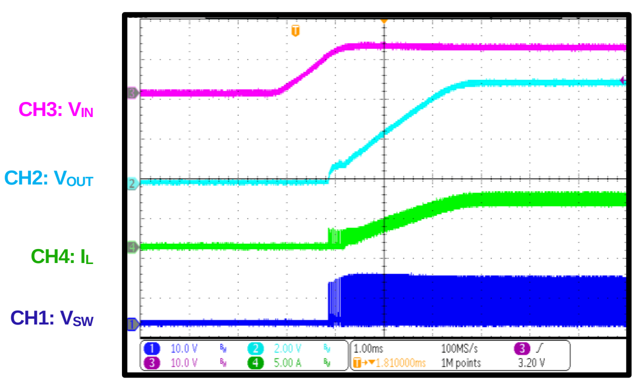
Start-Up through VIN

I_{OUT} = 7A, MPQ4326B-7000



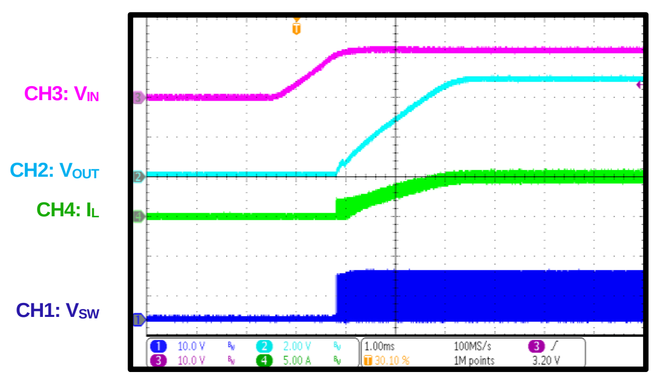
Start-Up through VIN

I_{OUT} = 6A, MPQ4326B-6000



Start-Up through VIN

I_{OUT} = 5A, MPQ4326B-5000

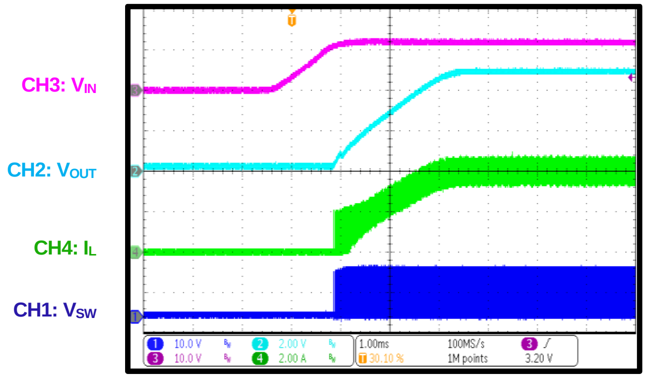


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 1µH, f_{SW} = 2.2MHz, AAM mode, T_A = 25°C, unless otherwise noted.

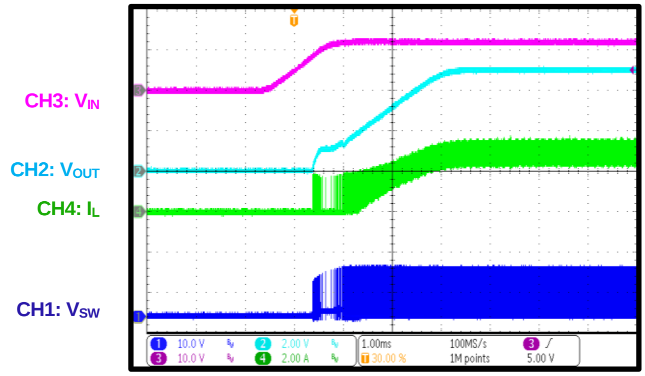
Start-Up through VIN

I_{OUT} = 4A, MPQ4326B-4000



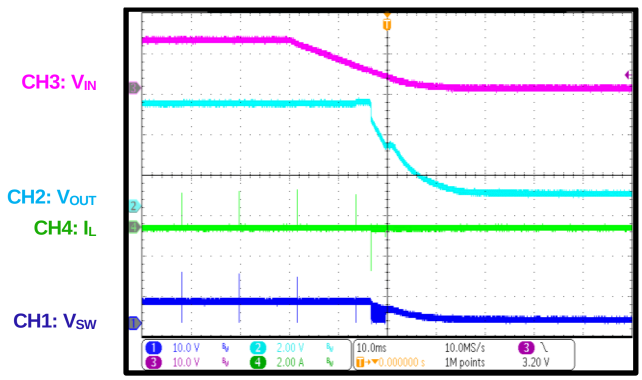
Start-Up through VIN

I_{OUT} = 3A, MPQ4326B-3000



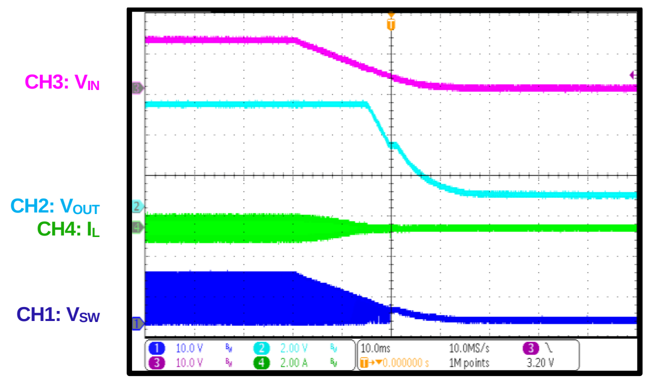
Shutdown through VIN

I_{OUT} = 0A, AAM mode



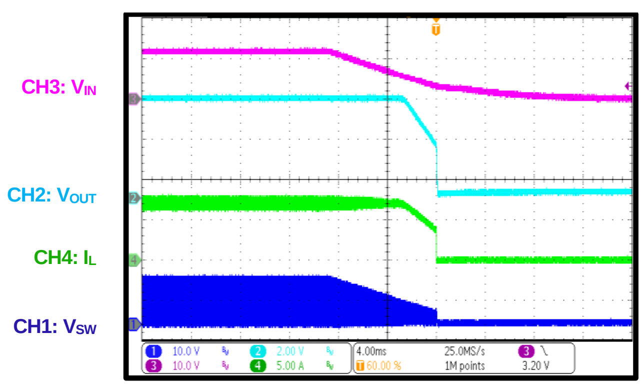
Shutdown through VIN

I_{OUT} = 0A, FCCM



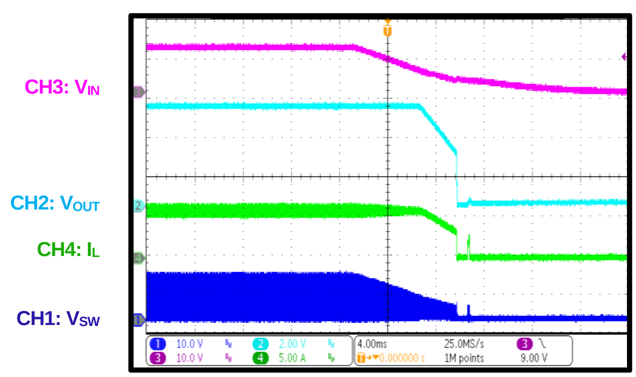
Shutdown through VIN

I_{OUT} = 7A, MPQ4326B-7000



Shutdown through VIN

I_{OUT} = 6A, MPQ4326B-6000

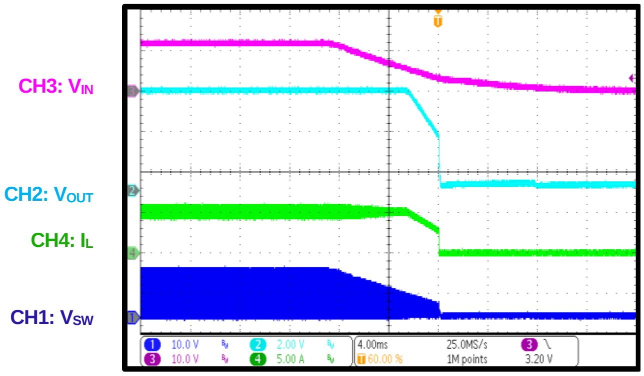


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 1µH, f_{SW} = 2.2MHz, AAM mode, T_A = 25°C, unless otherwise noted.

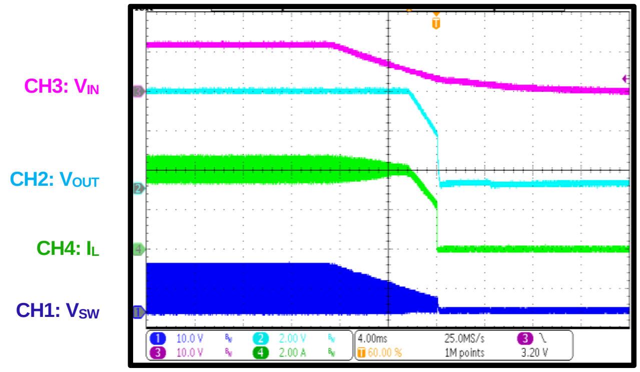
Shutdown through VIN

I_{OUT} = 5A, MPQ4326B-5000



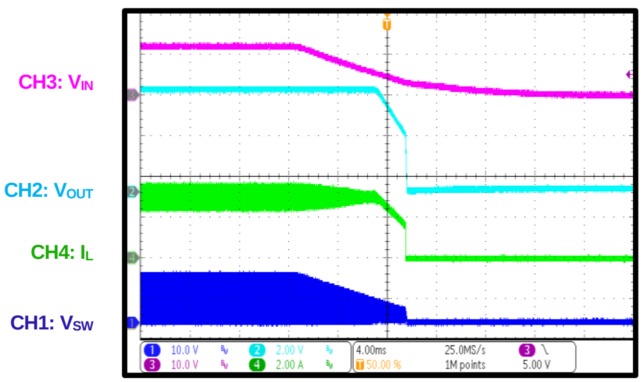
Shutdown through VIN

I_{OUT} = 4A, MPQ4326B-4000



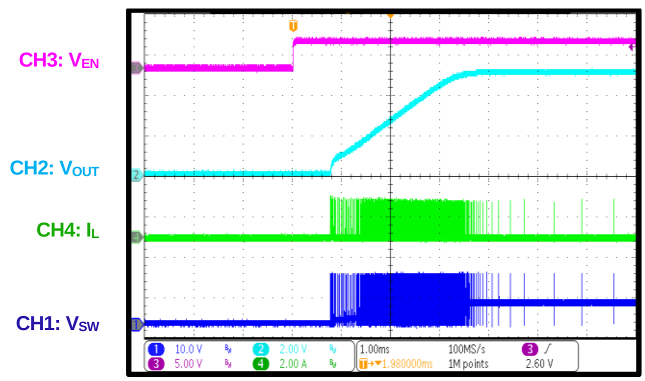
Shutdown through VIN

I_{OUT} = 3A, MPQ4326B-3000



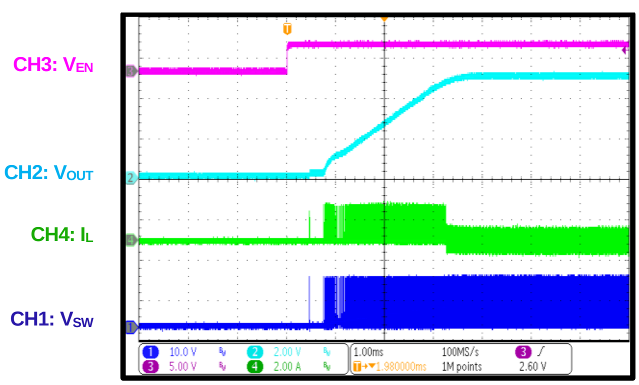
Start-Up through EN

I_{OUT} = 0A, AAM mode



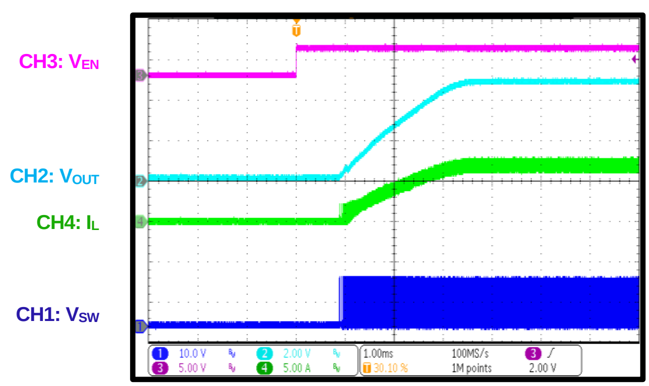
Start-Up through EN

I_{OUT} = 0A, FCCM



Start-Up through EN

I_{OUT} = 7A, MPQ4326B-7000

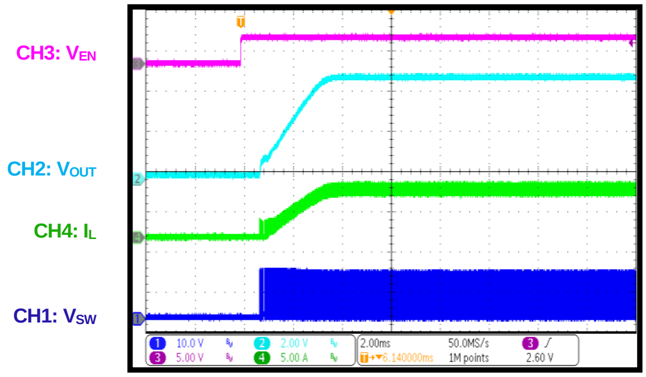


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 1µH, f_{SW} = 2.2MHz, AAM mode, T_A = 25°C, unless otherwise noted.

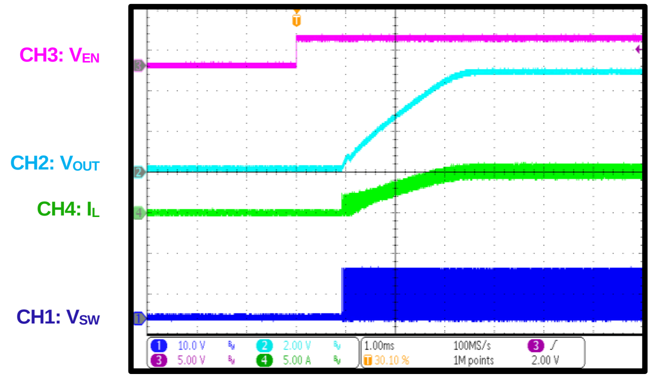
Start-Up through EN

I_{OUT} = 6A, MPQ4326B-6000



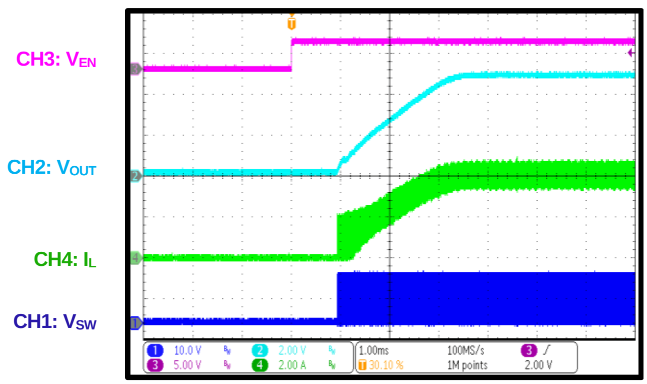
Start-Up through EN

I_{OUT} = 5A, MPQ4326B-5000



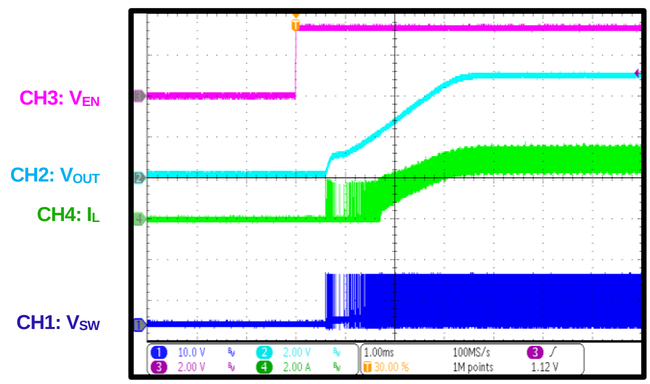
Start-Up through EN

I_{OUT} = 4A, MPQ4326B-4000



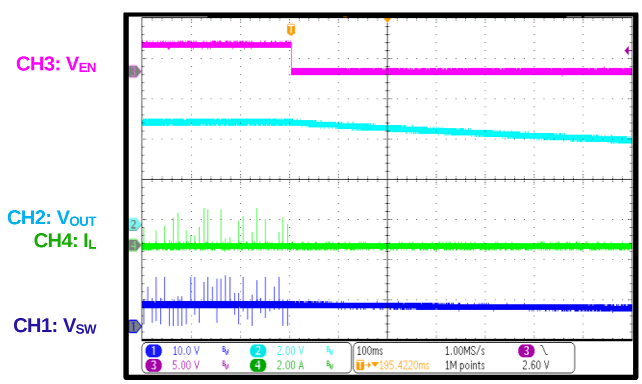
Start-Up through EN

I_{OUT} = 3A, MPQ4326B-3000



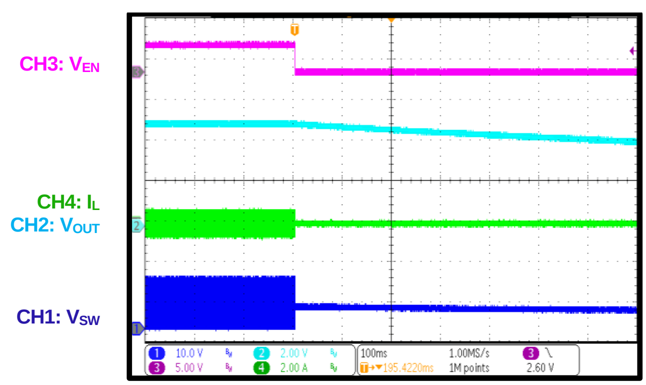
Shutdown through EN

I_{OUT} = 0A, AAM mode



Shutdown through EN

I_{OUT} = 0A, FCCM

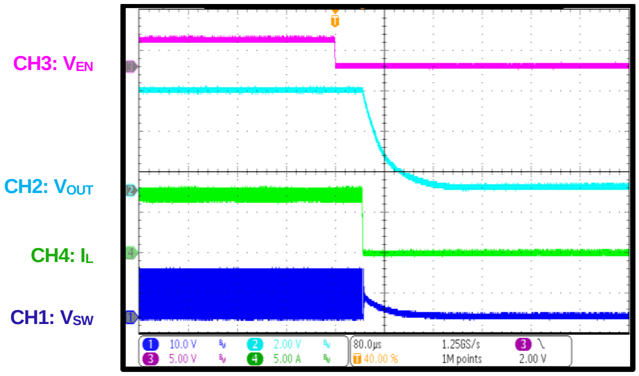


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 1µH, f_{SW} = 2.2MHz, AAM mode, T_A = 25°C, unless otherwise noted.

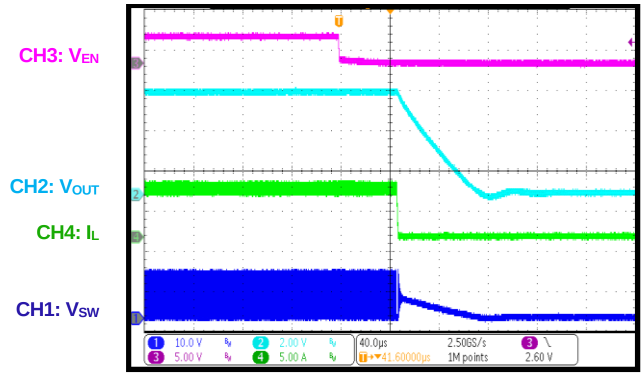
Shutdown through EN

I_{OUT} = 7A, MPQ4326B-7000



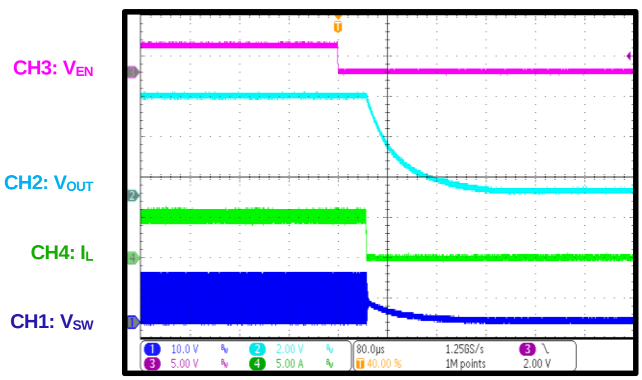
Shutdown through EN

I_{OUT} = 6A, MPQ4326B-6000



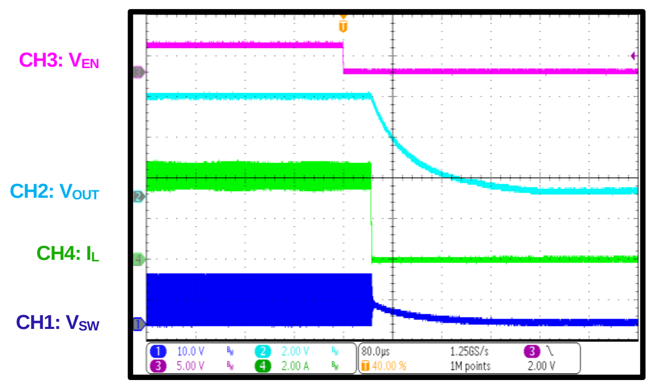
Shutdown through EN

I_{OUT} = 5A, MPQ4326B-5000



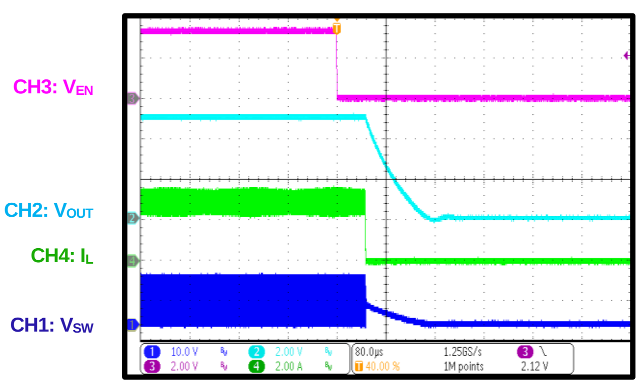
Shutdown through EN

I_{OUT} = 4A, MPQ4326B-4000



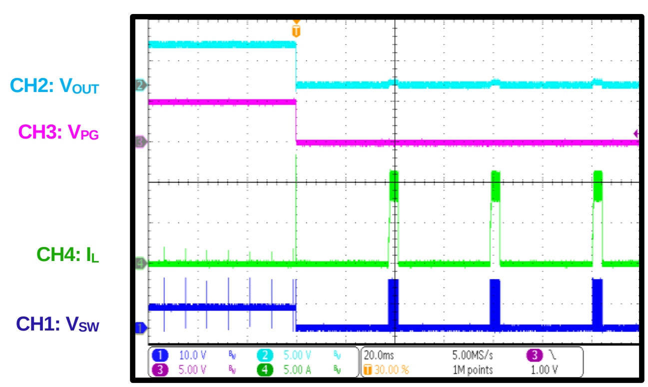
Shutdown through EN

I_{OUT} = 3A, MPQ4326B-3000



SCP Entry

I_{OUT} = 0A, AAM mode, MPQ4326B-7000

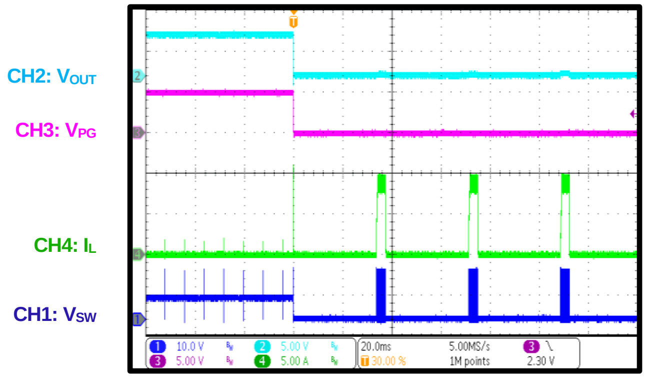


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 1µH, f_{SW} = 2.2MHz, AAM mode, T_A = 25°C, unless otherwise noted.

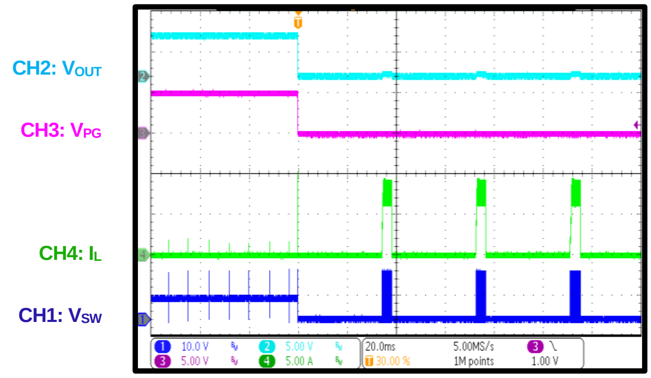
SCP Entry

I_{OUT} = 0A, AAM mode, MPQ4326B-6000



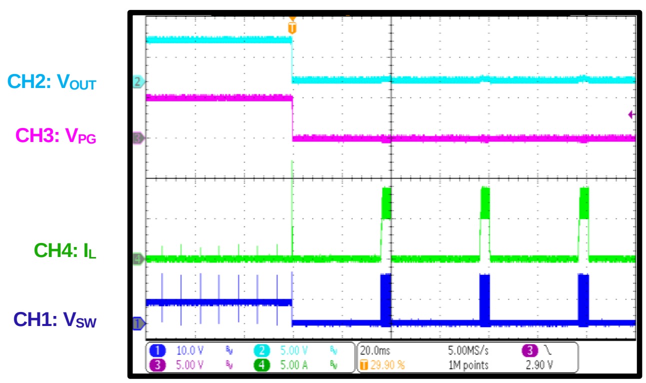
SCP Entry

I_{OUT} = 0A, AAM mode, MPQ4326B-5000



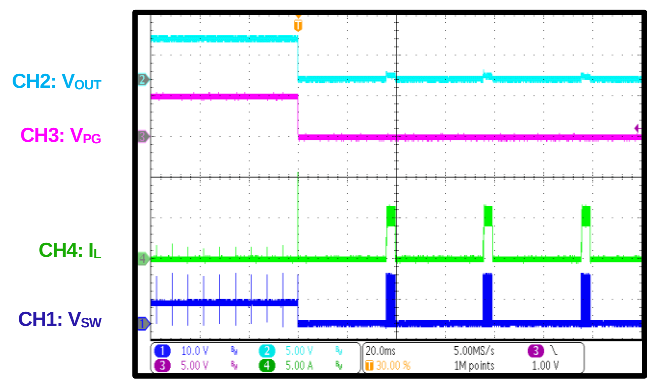
SCP Entry

I_{OUT} = 0A, AAM mode, MPQ4326B-4000



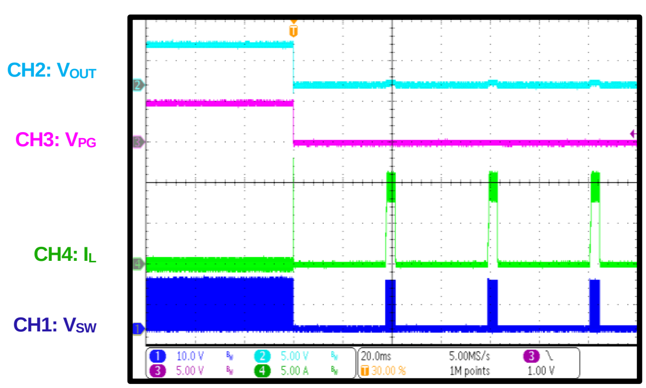
SCP Entry

I_{OUT} = 0A, AAM mode, MPQ4326B-3000



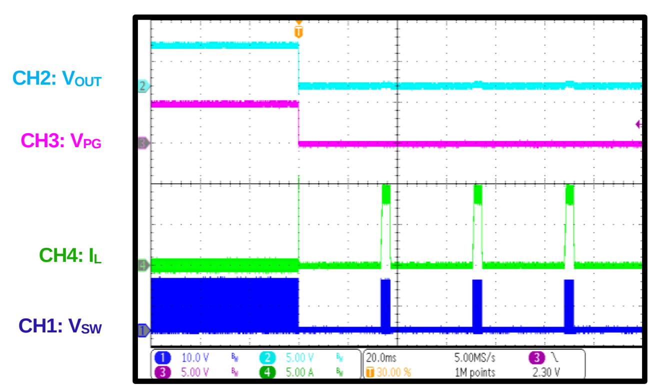
SCP Entry

I_{OUT} = 0A, FCCM, MPQ4326B-7000



SCP Entry

I_{OUT} = 0A, FCCM, MPQ4326B-6000

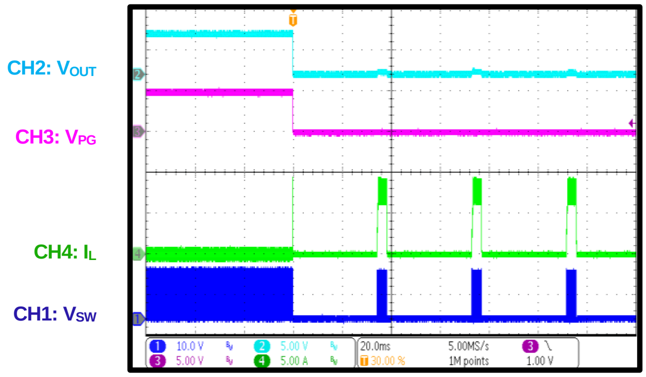


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 1µH, f_{SW} = 2.2MHz, AAM mode, T_A = 25°C, unless otherwise noted.

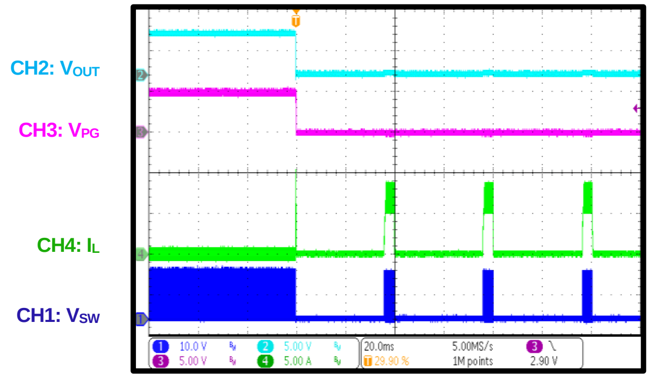
SCP Entry

I_{OUT} = 0A, FCCM, MPQ4326B-5000



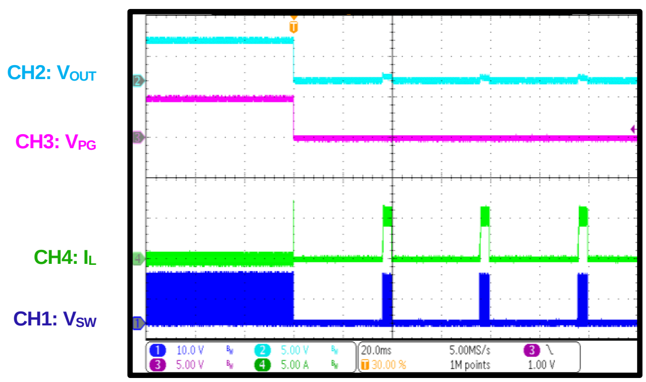
SCP Entry

I_{OUT} = 0A, FCCM, MPQ4326B-4000



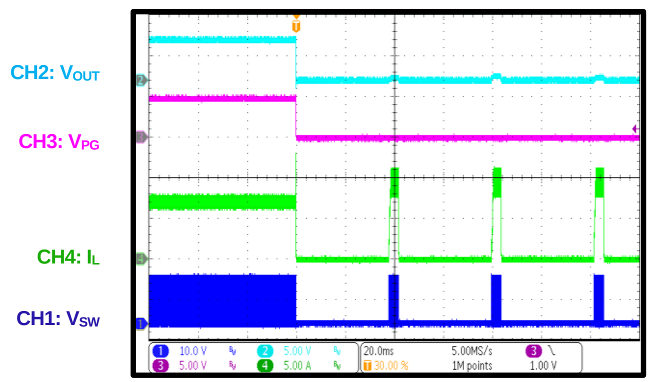
SCP Entry

I_{OUT} = 0A, FCCM, MPQ4326B-3000



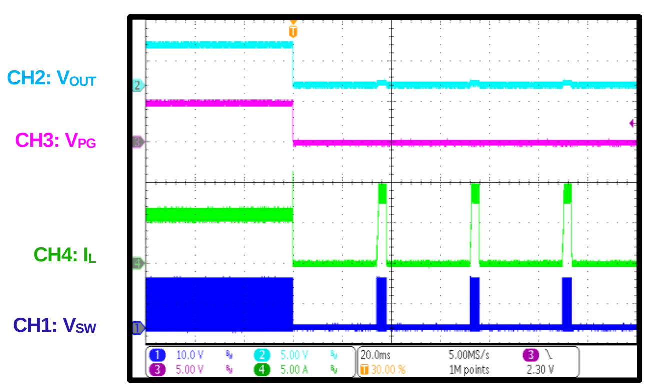
SCP Entry

I_{OUT} = 7A, MPQ4326B-7000



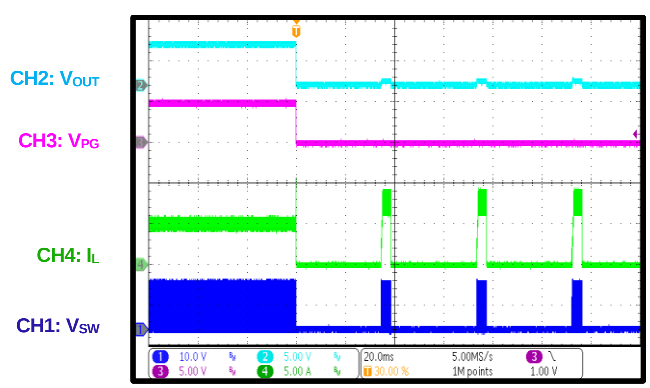
SCP Entry

I_{OUT} = 6A, MPQ4326B-6000



SCP Entry

I_{OUT} = 5A, MPQ4326B-5000

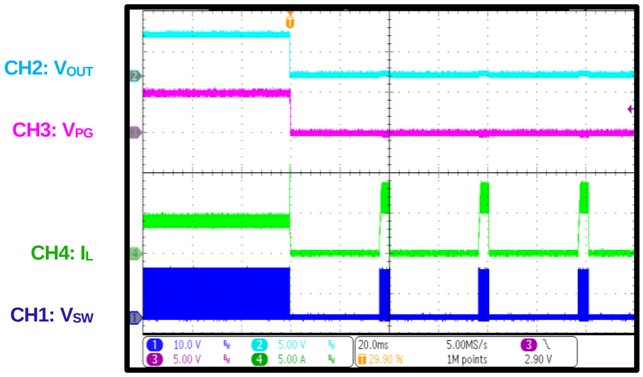


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 1µH, f_{SW} = 2.2MHz, AAM mode, T_A = 25°C, unless otherwise noted.

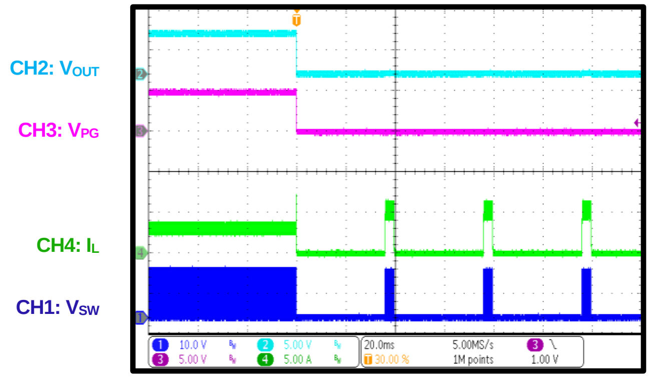
SCP Entry

I_{OUT} = 4A, MPQ4326B-4000



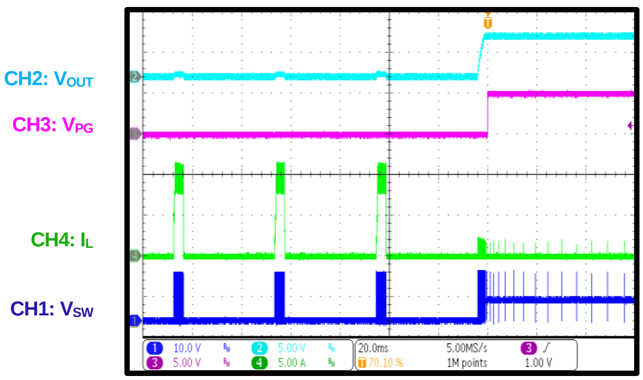
SCP Entry

I_{OUT} = 3A, MPQ4326B-3000



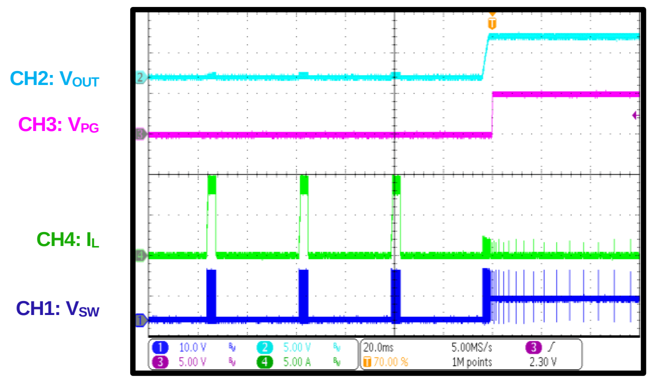
SCP Recovery

I_{OUT} = 0A, AAM mode, MPQ4326B-7000



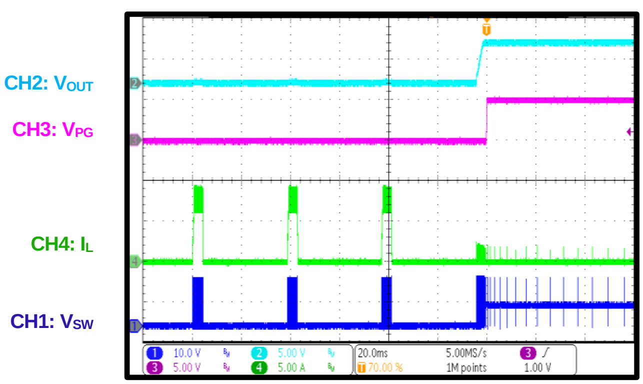
SCP Recovery

I_{OUT} = 0A, AAM mode, MPQ4326B-6000



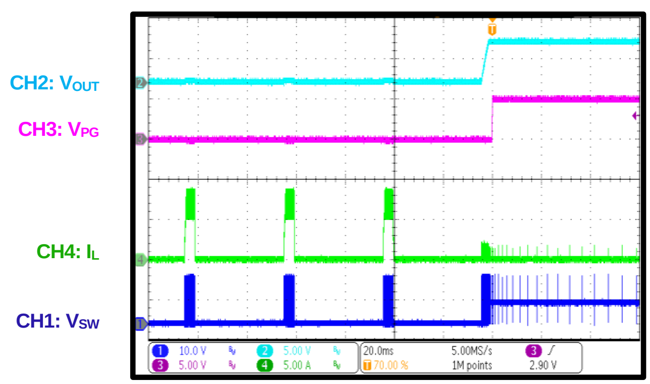
SCP Recovery

I_{OUT} = 0A, AAM mode, MPQ4326B-5000



SCP Recovery

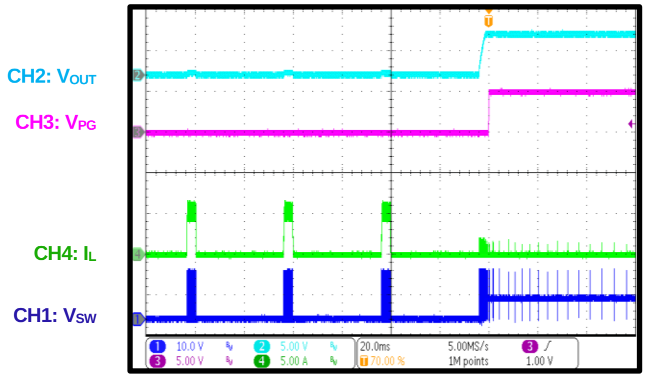
I_{OUT} = 0A, AAM mode, MPQ4326B-4000



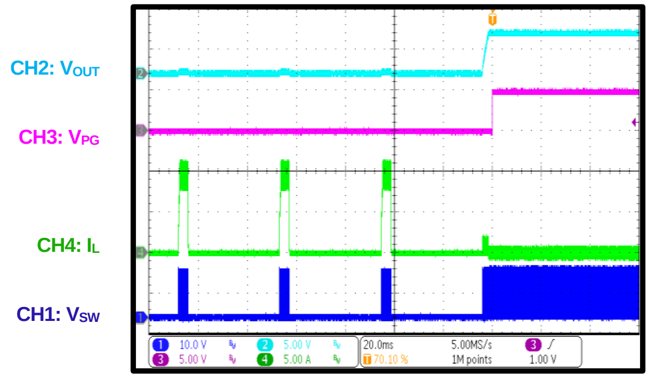
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 1µH, f_{SW} = 2.2MHz, AAM mode, T_A = 25°C, unless otherwise noted.

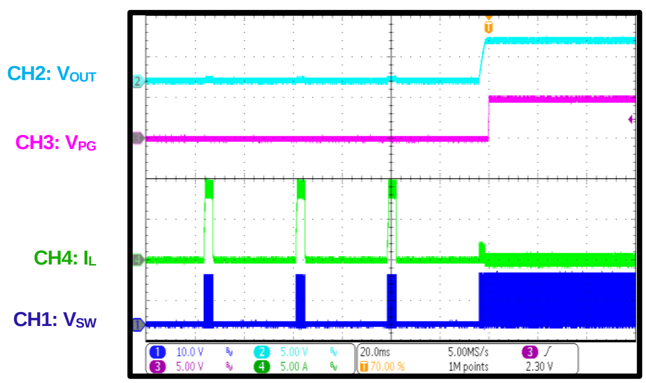
SCP Recovery
I_{OUT} = 0A, AAM mode, MPQ4326B-3000



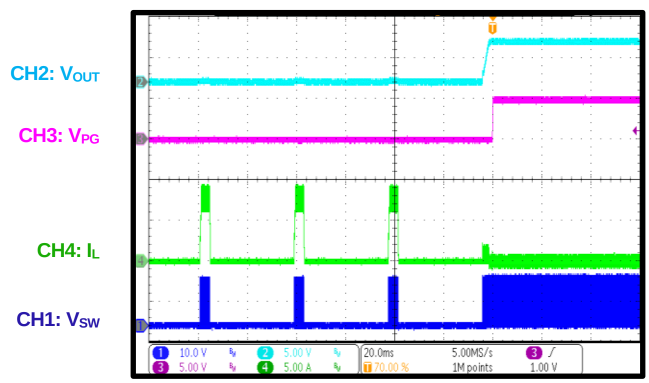
SCP Recovery
I_{OUT} = 0A, FCCM, MPQ4326B-7000



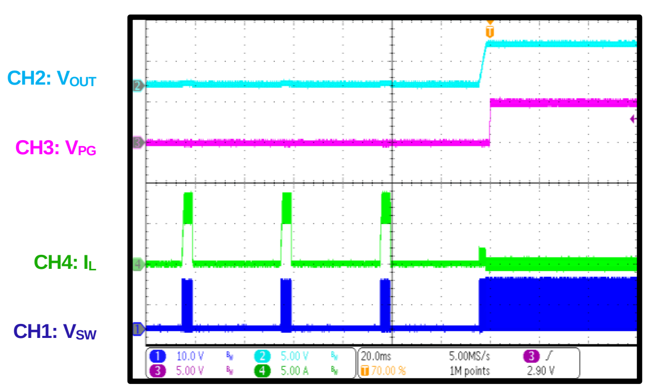
SCP Recovery
I_{OUT} = 0A, FCCM, MPQ4326B-6000



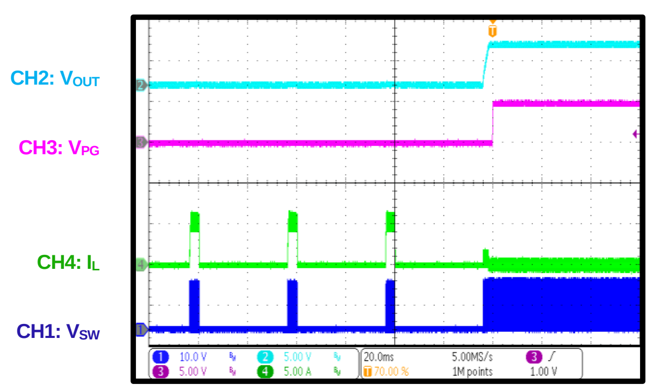
SCP Recovery
I_{OUT} = 0A, FCCM, MPQ4326B-5000



SCP Recovery
I_{OUT} = 0A, FCCM, MPQ4326B-4000



SCP Recovery
I_{OUT} = 0A, FCCM, MPQ4326B-3000

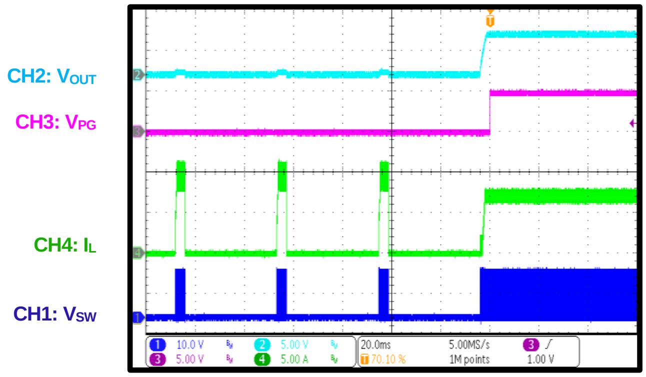


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 1µH, f_{SW} = 2.2MHz, AAM mode, T_A = 25°C, unless otherwise noted.

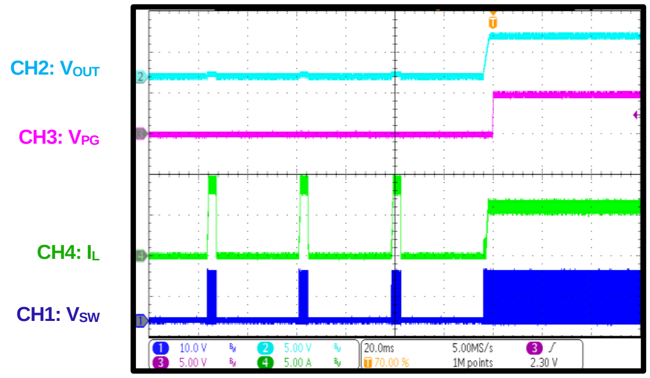
SCP Recovery

I_{OUT} = 7A, MPQ4326B-7000



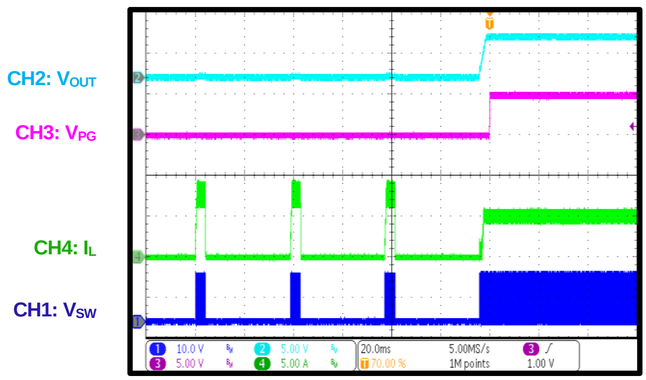
SCP Recovery

I_{OUT} = 6A, MPQ4326B-6000



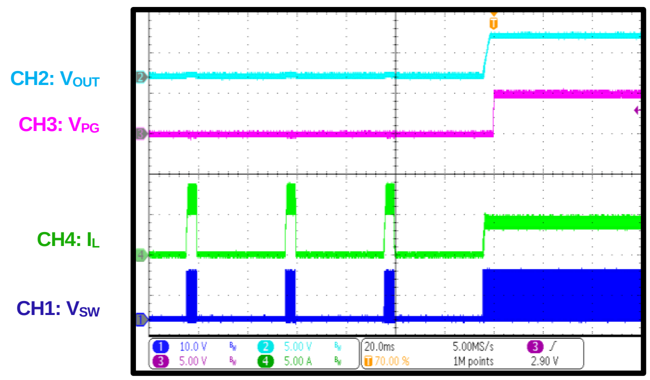
SCP Recovery

I_{OUT} = 5A, MPQ4326B-5000



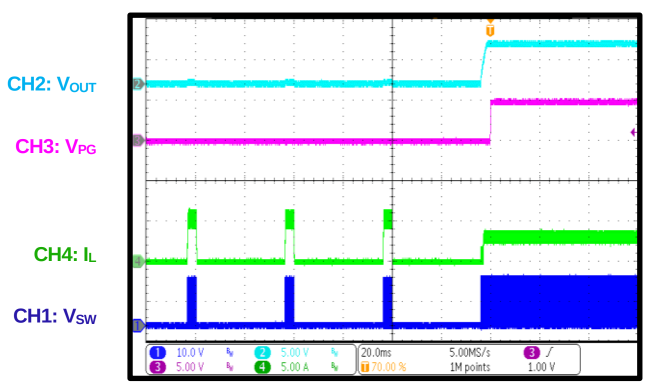
SCP Recovery

I_{OUT} = 4A, MPQ4326B-4000



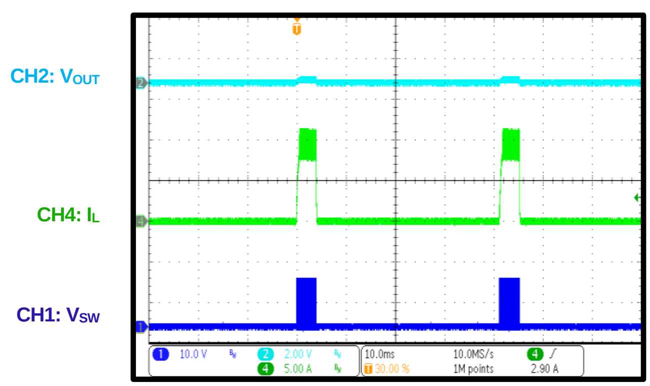
SCP Recovery

I_{OUT} = 3A, MPQ4326B-3000



SCP Steady State

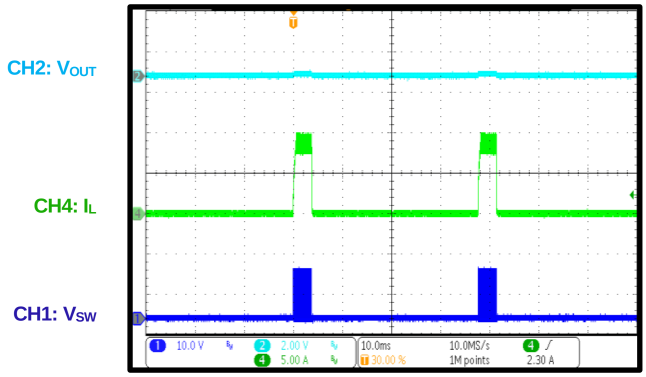
MPQ4326B-7000



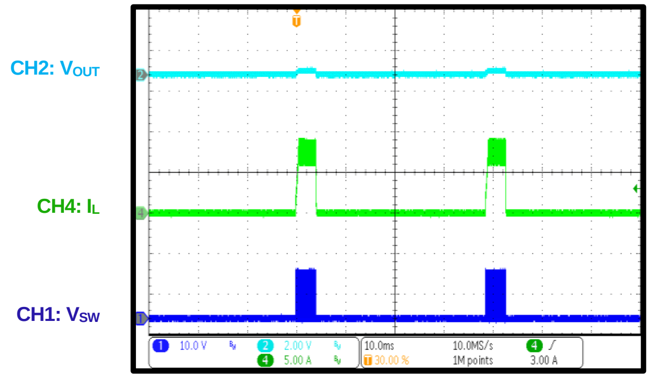
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 1µH, f_{SW} = 2.2MHz, AAM mode, T_A = 25°C, unless otherwise noted.

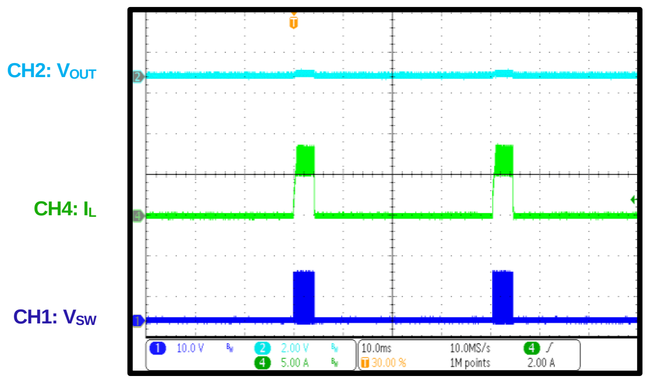
SCP Steady State
MPQ4326B-6000



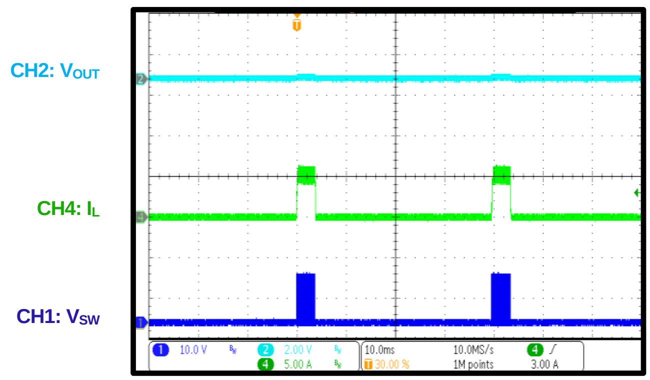
SCP Steady State
MPQ4326B-5000



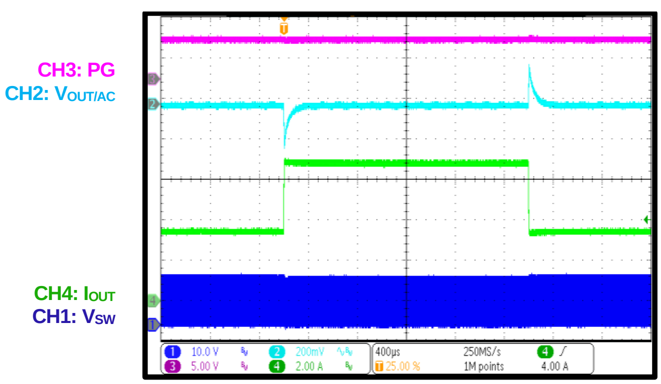
SCP Steady State for
MPQ4326B-4000



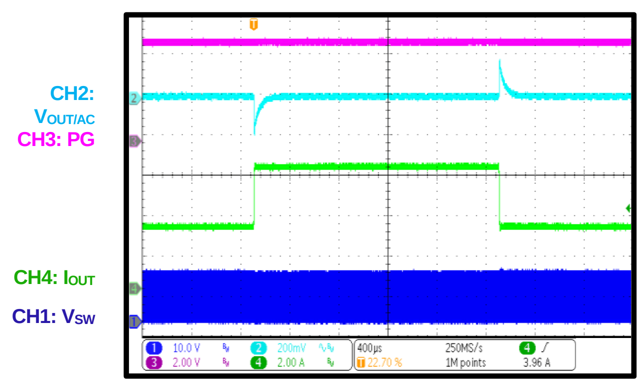
SCP Steady State for
MPQ4326B-3000



Load Transient Response
I_{OUT} = 3.5A to 7A, 2A/µs, MPQ4326B-7000



Load Transient Response
I_{OUT} = 3A to 6A, 2A/µs, MPQ4326B-6000

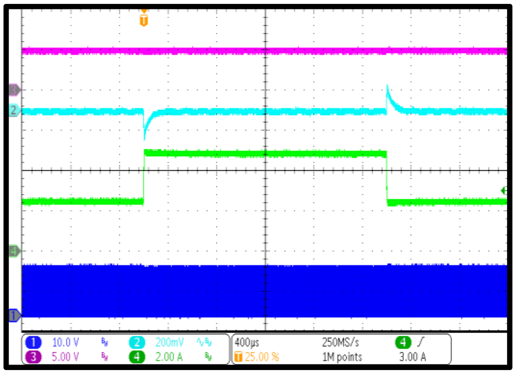


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 1µH, f_{SW} = 2.2MHz, AAM mode, T_A = 25°C, unless otherwise noted.

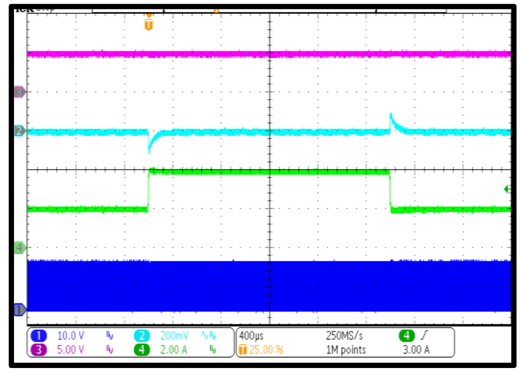
Load Transient Response

I_{OUT} = 2.5A to 5A, 2A/µs, MPQ4326B-5000



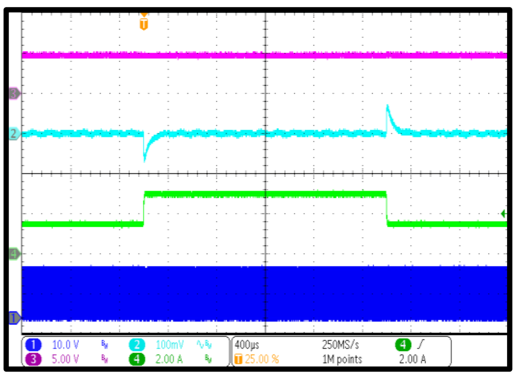
Load Transient Response

I_{OUT} = 2A to 4A, 2A/µs, MPQ4326B-4000



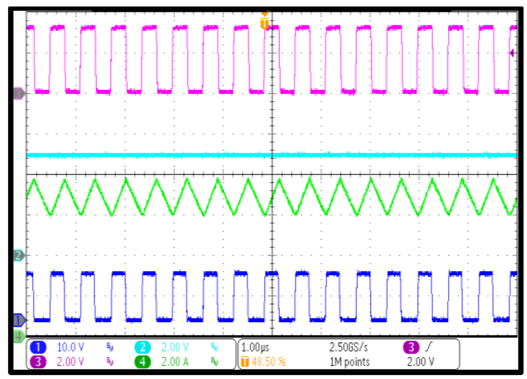
Load Transient Response

I_{OUT} = 1.5A to 3A, 2A/µs, MPQ4326B-3000



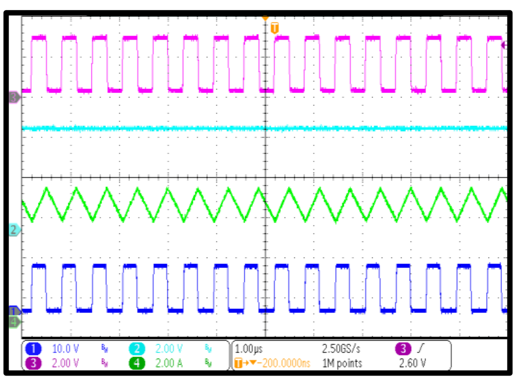
SYNCIN Operation

I_{OUT} = 7A, SYNC frequency = 1800kHz



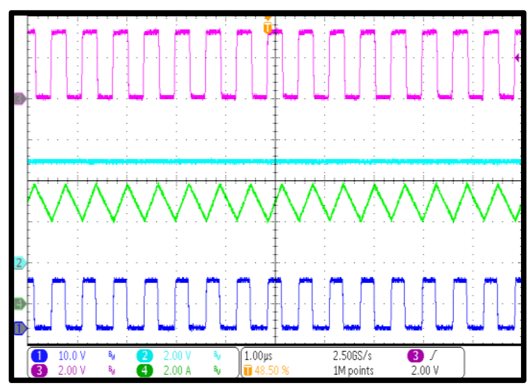
SYNCIN Operation

I_{OUT} = 6A, SYNC frequency = 1800kHz



SYNCIN Operation

I_{OUT} = 5A, SYNC frequency = 1800kHz

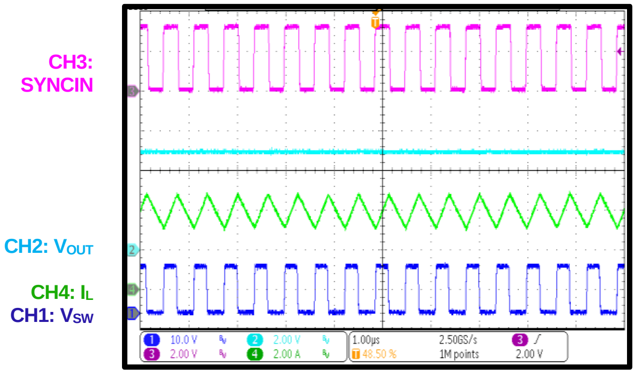


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 1µH, f_{SW} = 2.2MHz, AAM mode, T_A = 25°C, unless otherwise noted.

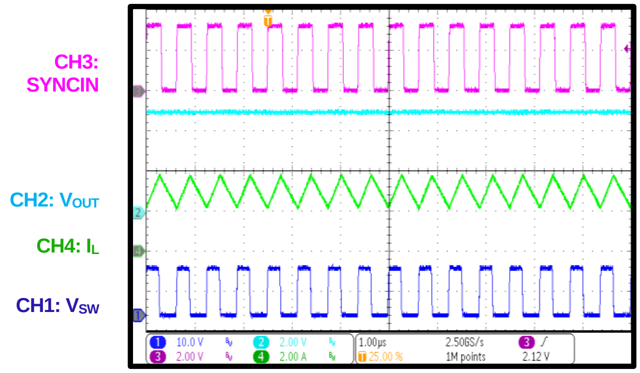
SYNCIN Operation

I_{OUT} = 4A, SYNC frequency = 1800kHz



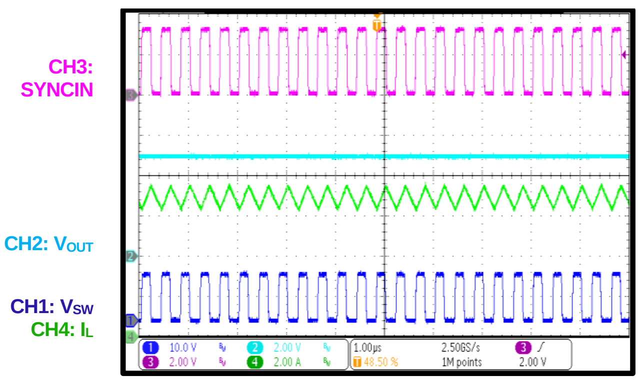
SYNCIN Operation

I_{OUT} = 3A, SYNC frequency = 1800kHz



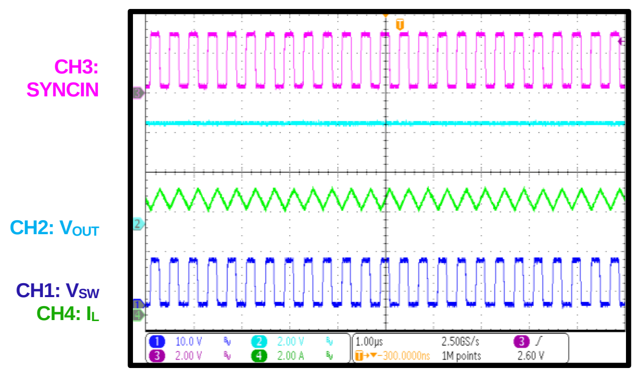
SYNCIN Operation

I_{OUT} = 7A, SYNC frequency = 2500kHz



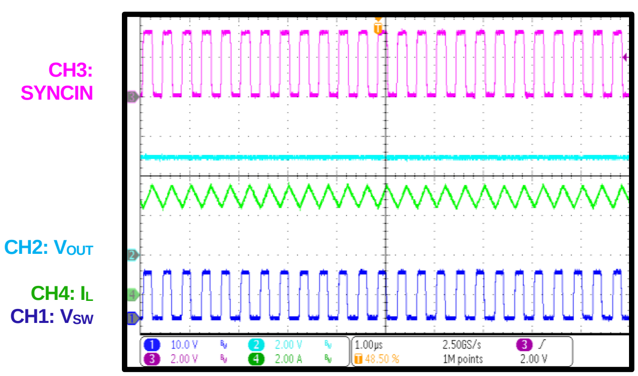
SYNCIN Operation

I_{OUT} = 6A, SYNC frequency = 2500kHz



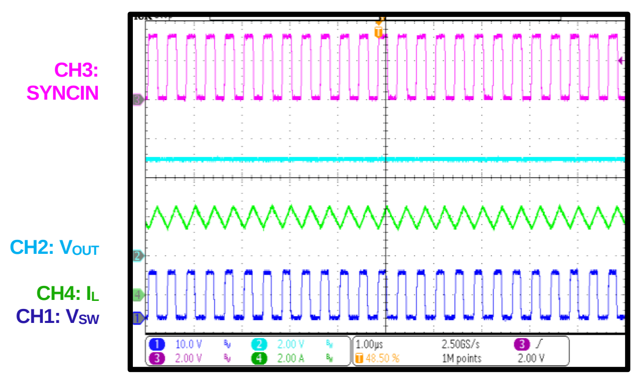
SYNCIN Operation

I_{OUT} = 5A, SYNC frequency = 2500kHz



SYNCIN Operation

I_{OUT} = 4A, SYNC frequency = 2500kHz

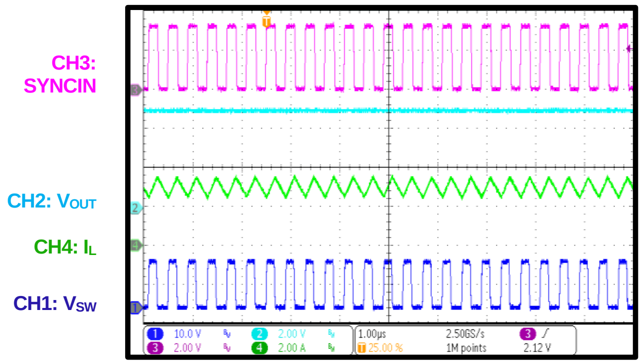


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 1µH, f_{SW} = 2.2MHz, AAM mode, T_A = 25°C, unless otherwise noted.

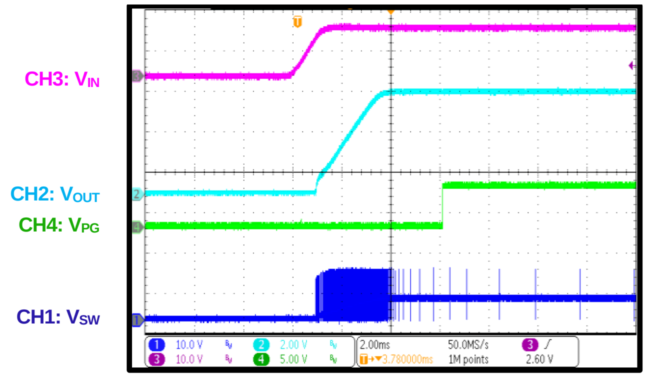
SYNCIN Operation

I_{OUT} = 3A, SYNC frequency = 2500kHz



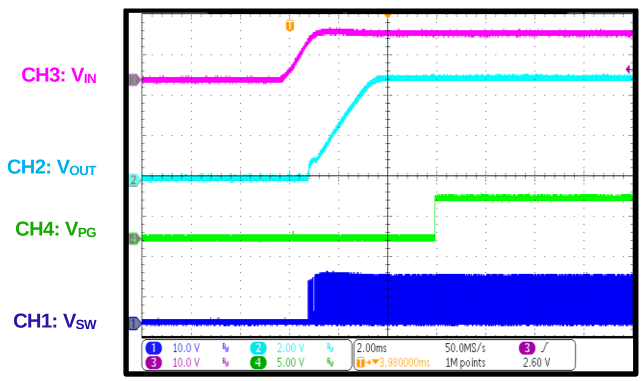
PG in Start-Up through VIN

I_{OUT} = 0A, AAM mode



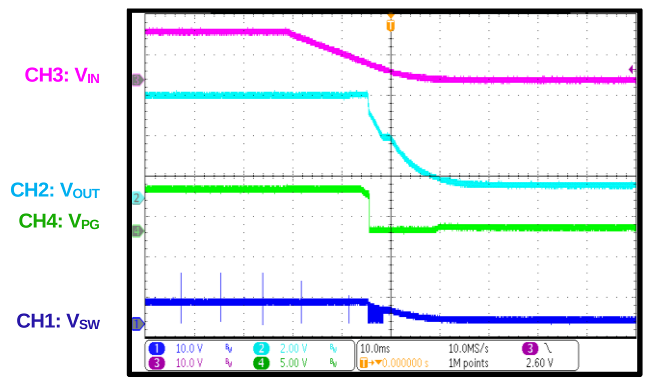
PG in Start-Up through VIN

I_{OUT} = 3A to 7A



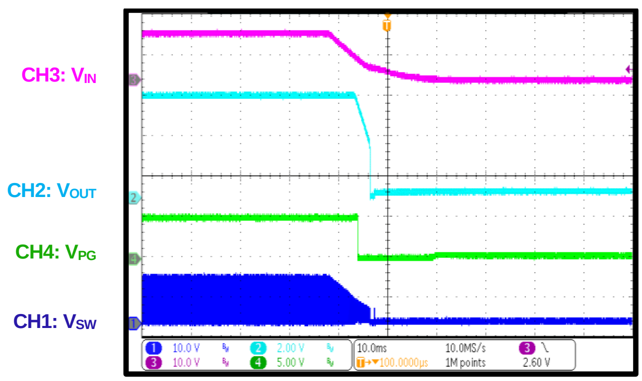
PG in Shutdown through VIN

I_{OUT} = 0A, AAM mode



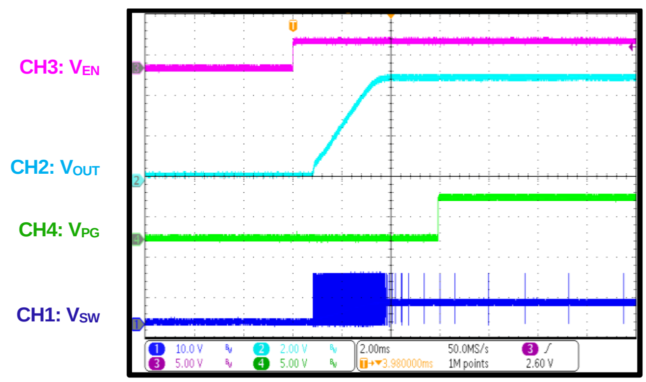
PG in Shutdown through VIN

I_{OUT} = 3A to 7A



PG in Start-Up through EN

I_{OUT} = 0A, AAM mode

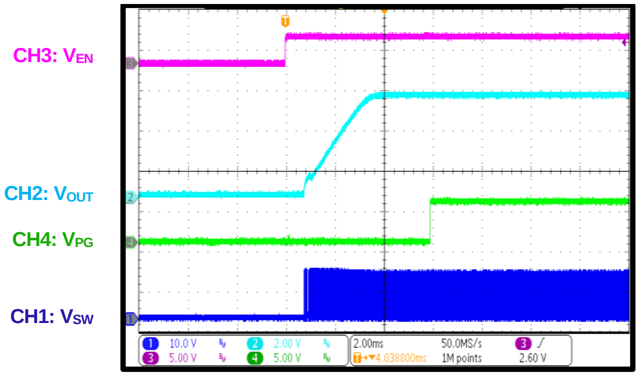


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 1µH, f_{SW} = 2.2MHz, AAM mode, T_A = 25°C, unless otherwise noted.

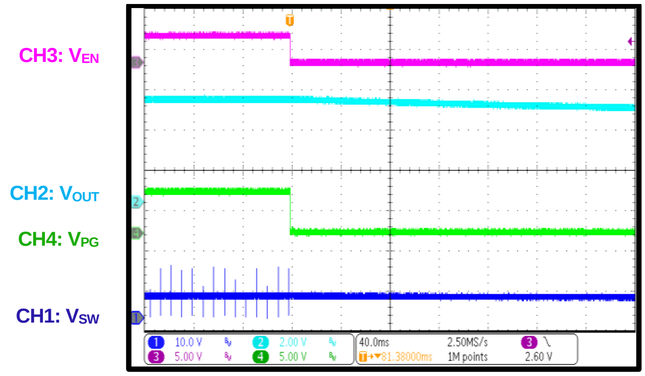
PG in Start-Up through EN

I_{OUT} = 3A to 7A



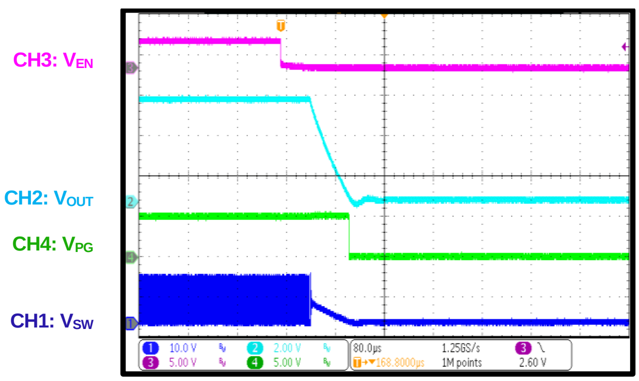
PG in Shutdown through EN

I_{OUT} = 0A, AAM mode



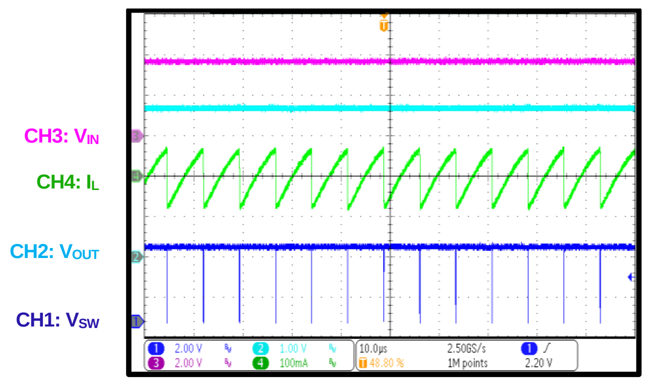
PG in Shutdown through EN

I_{OUT} = 3A to 7A



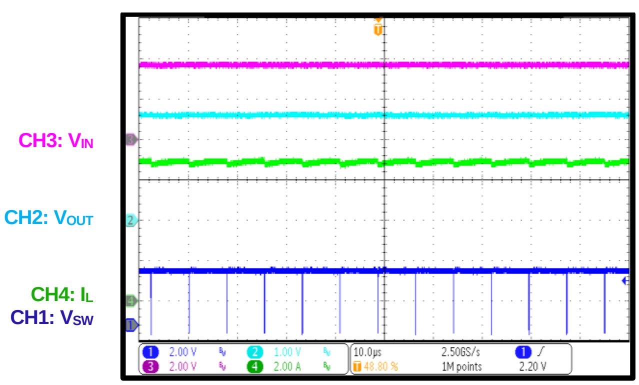
Low-Dropout Mode

V_{IN} = 3.7V, I_{OUT} = 0A



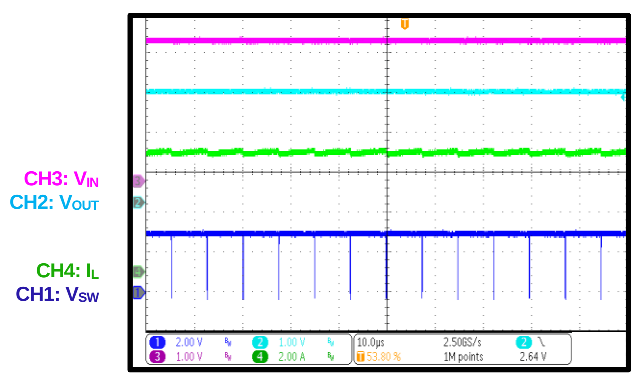
Low-Dropout Mode

V_{IN} = 3.7V, I_{OUT} = 7A, MPQ4326B-7000



Low-Dropout Mode

V_{IN} = 3.7V, I_{OUT} = 6A, MPQ4326B-6000

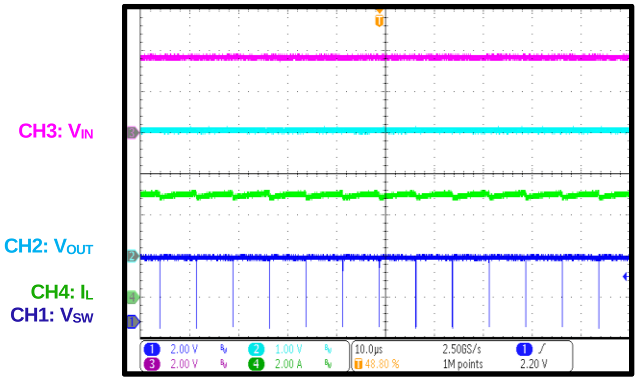


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 1µH, f_{SW} = 2.2MHz, AAM mode, T_A = 25°C, unless otherwise noted.

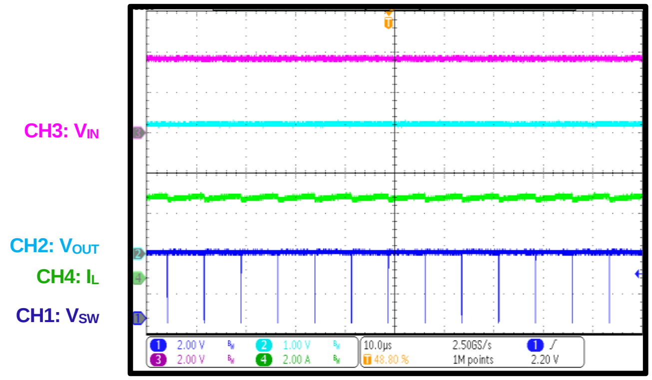
Low-Dropout Mode

V_{IN} = 3.7V, I_{OUT} = 5A, MPQ4326B-5000



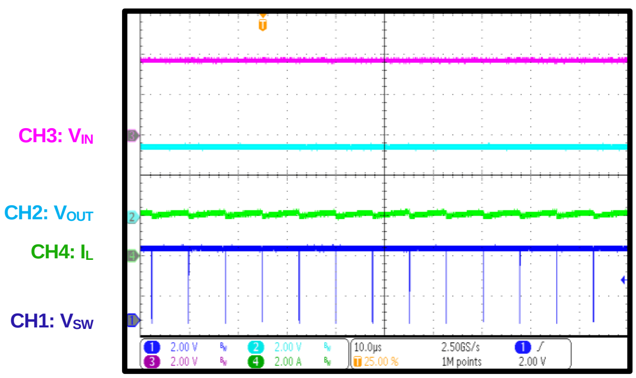
Low-Dropout Mode

V_{IN} = 3.7V, I_{OUT} = 4A, MPQ4326B-4000



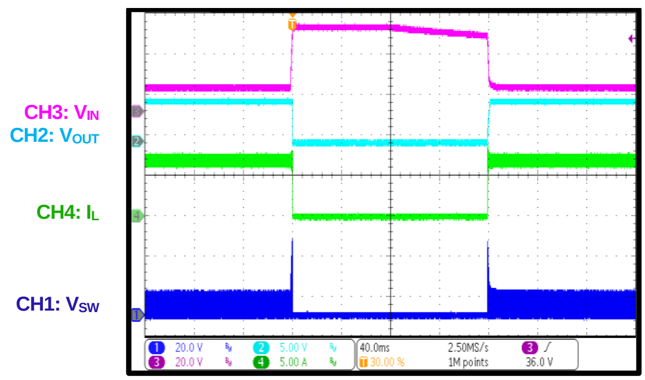
Low-Dropout Mode

V_{IN} = 3.7V, I_{OUT} = 3A, MPQ4326B-3000



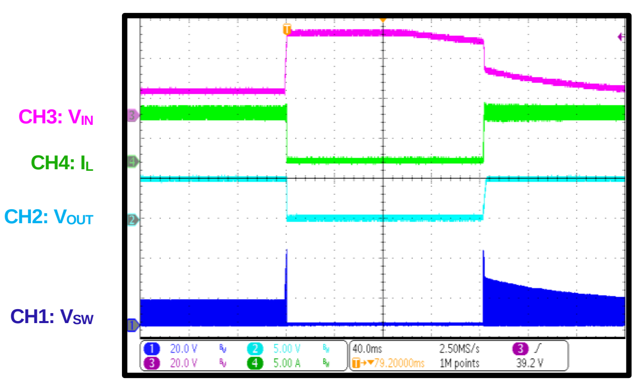
Load Dump

V_{IN} = 12V to 42V, I_{OUT} = 7A, MPQ4326B-7000



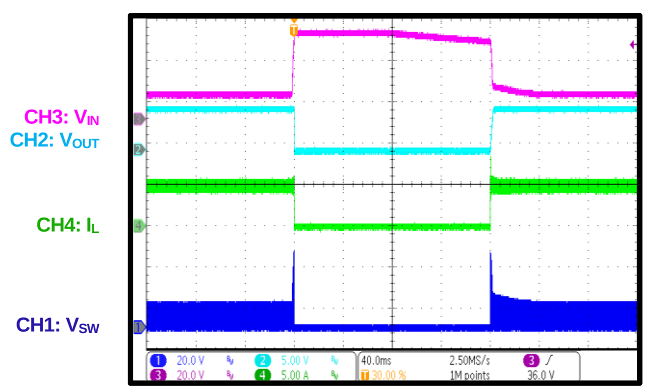
Load Dump

V_{IN} = 12V to 42V, I_{OUT} = 6A, MPQ4326B-6000



Load Dump

V_{IN} = 12V to 42V, I_{OUT} = 5A, MPQ4326B-5000

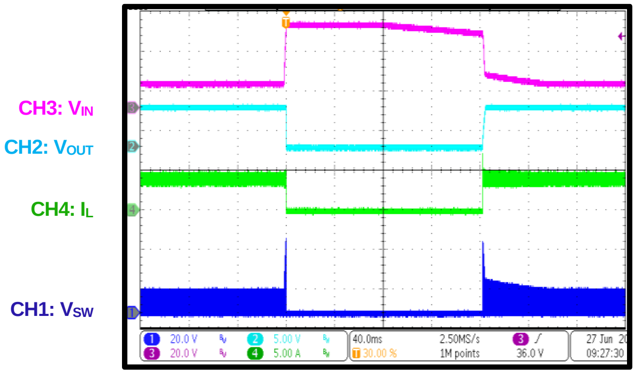


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 1µH, f_{SW} = 2.2MHz, AAM mode, T_A = 25°C, unless otherwise noted.

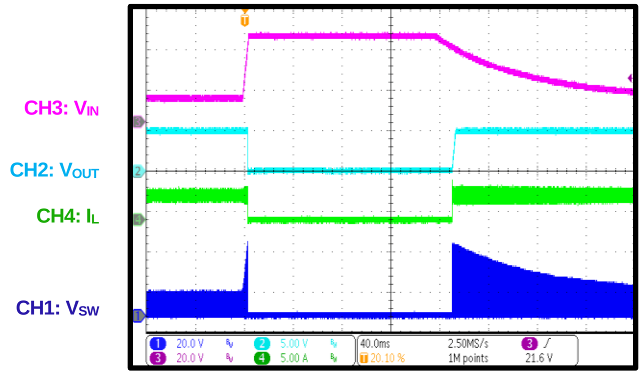
Load Dump

V_{IN} = 12V to 42V, I_{OUT} = 4A, MPQ4326B-4000



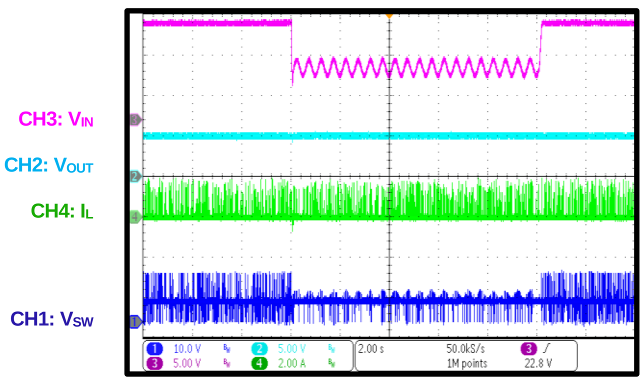
Load Dump

V_{IN} = 12V to 42V, I_{OUT} = 3A, MPQ4326B-3000



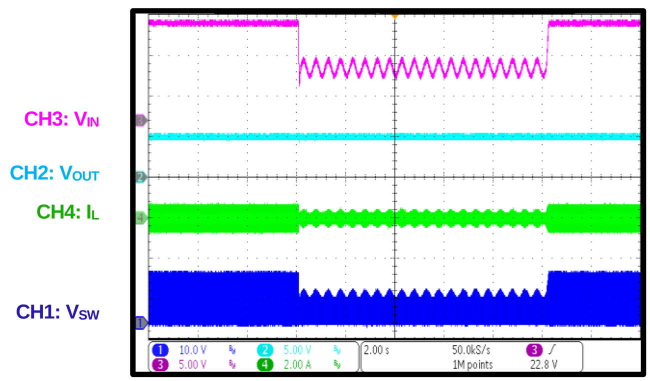
Cold Crank

I_{OUT} = 0A, AAM mode



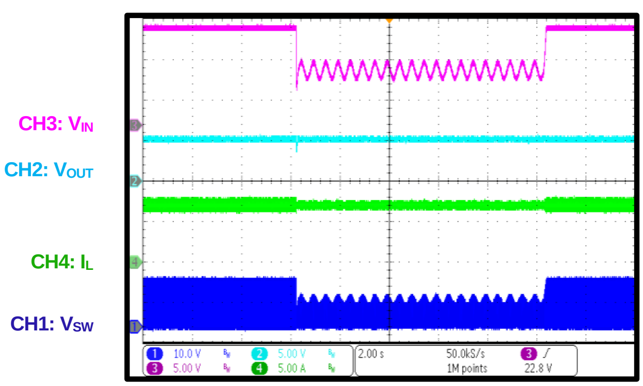
Cold Crank

I_{OUT} = 0A, FCCM



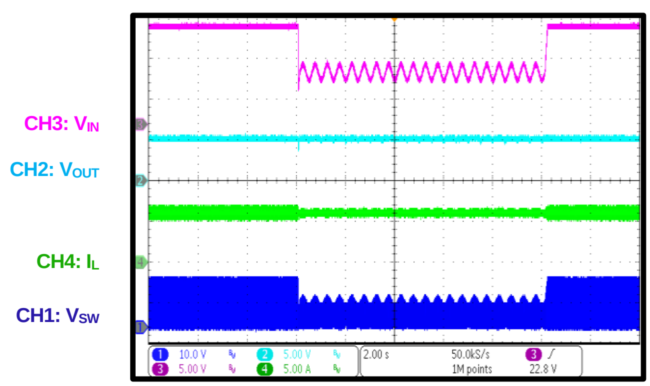
Cold Crank

I_{OUT} = 7A, MPQ4326B-7000



Cold Crank

I_{OUT} = 6A, MPQ4326B-6000

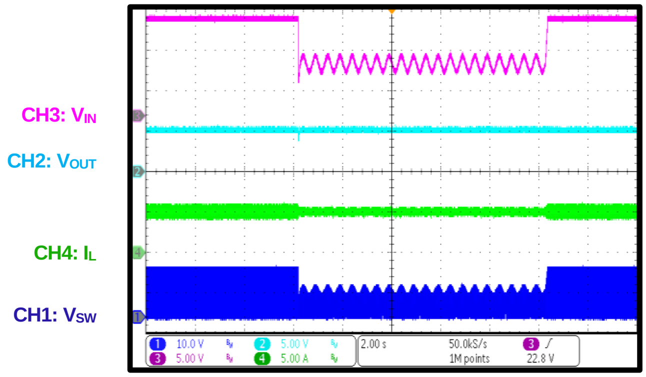


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 1µH, f_{SW} = 2.2MHz, AAM mode, T_A = 25°C, unless otherwise noted.

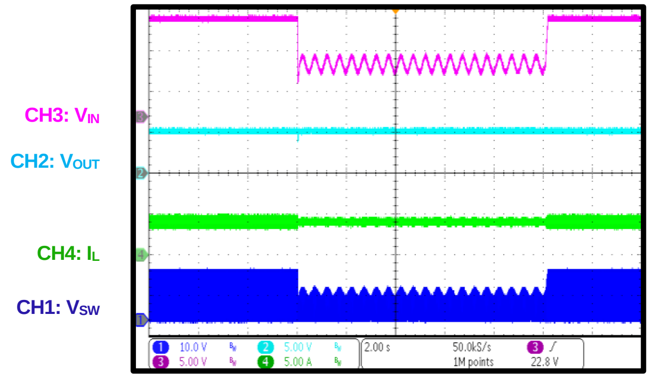
Cold Crank

I_{OUT} = 5A, MPQ4326B-5000



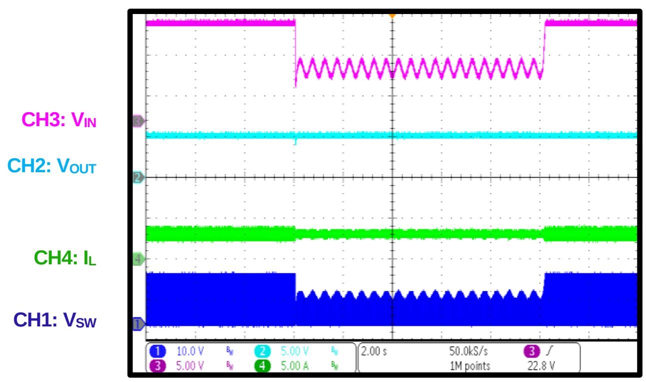
Cold Crank

I_{OUT} = 4A, MPQ4326B-4000



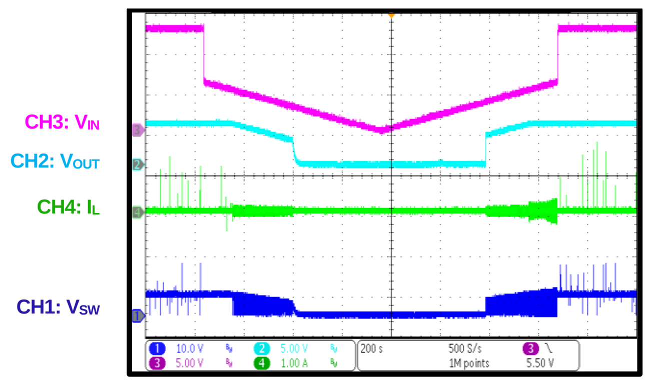
Cold Crank

I_{OUT} = 3A, MPQ4326B-3000



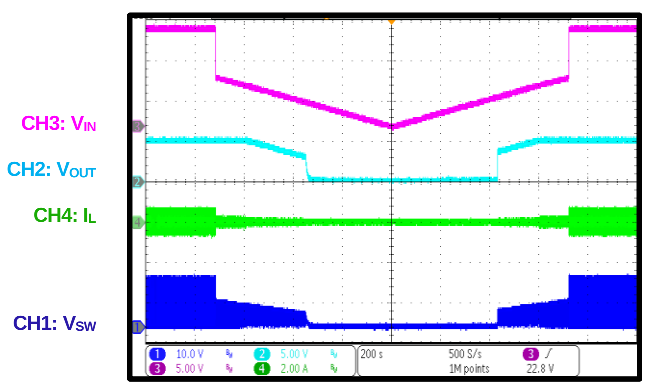
V_{IN} Ramping Down and Up

I_{OUT} = 0A, AAM mode



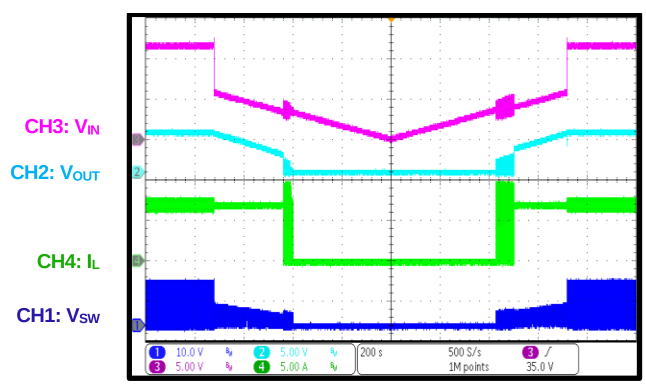
V_{IN} Ramping Down and Up

I_{OUT} = 0A, FCCM



V_{IN} Ramping Down and Up

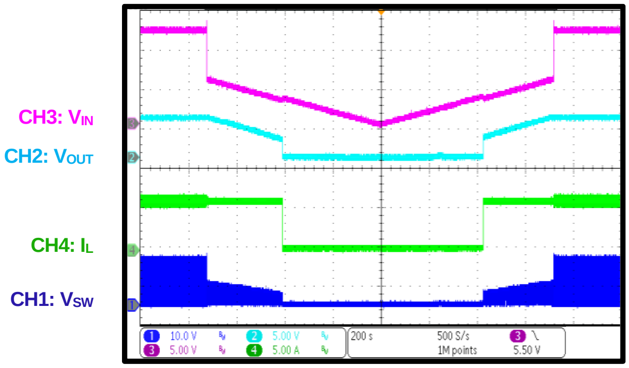
I_{OUT} = 7A, MPQ4326B-7000



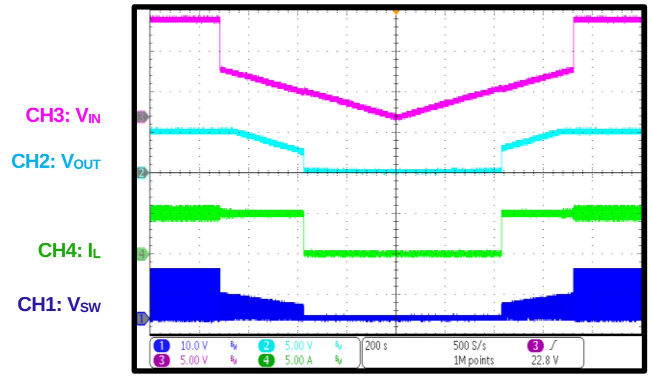
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 1µH, f_{SW} = 2.2MHz, AAM mode, T_A = 25°C, unless otherwise noted.

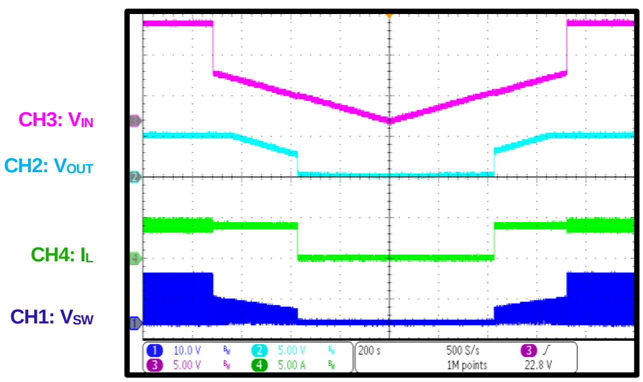
V_{IN} Ramping Down and Up
I_{OUT} = 6A, MPQ4326B-6000



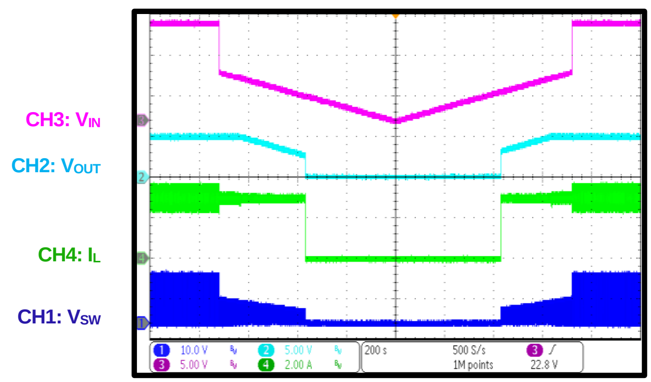
V_{IN} Ramping Down and Up
I_{OUT} = 5A, MPQ4326B-5000



V_{IN} Ramping Down and Up
I_{OUT} = 4A, MPQ4326B-4000



V_{IN} Ramping Down and Up
I_{OUT} = 3A, MPQ4326B-3000



FUNCTIONAL BLOCK DIAGRAMS

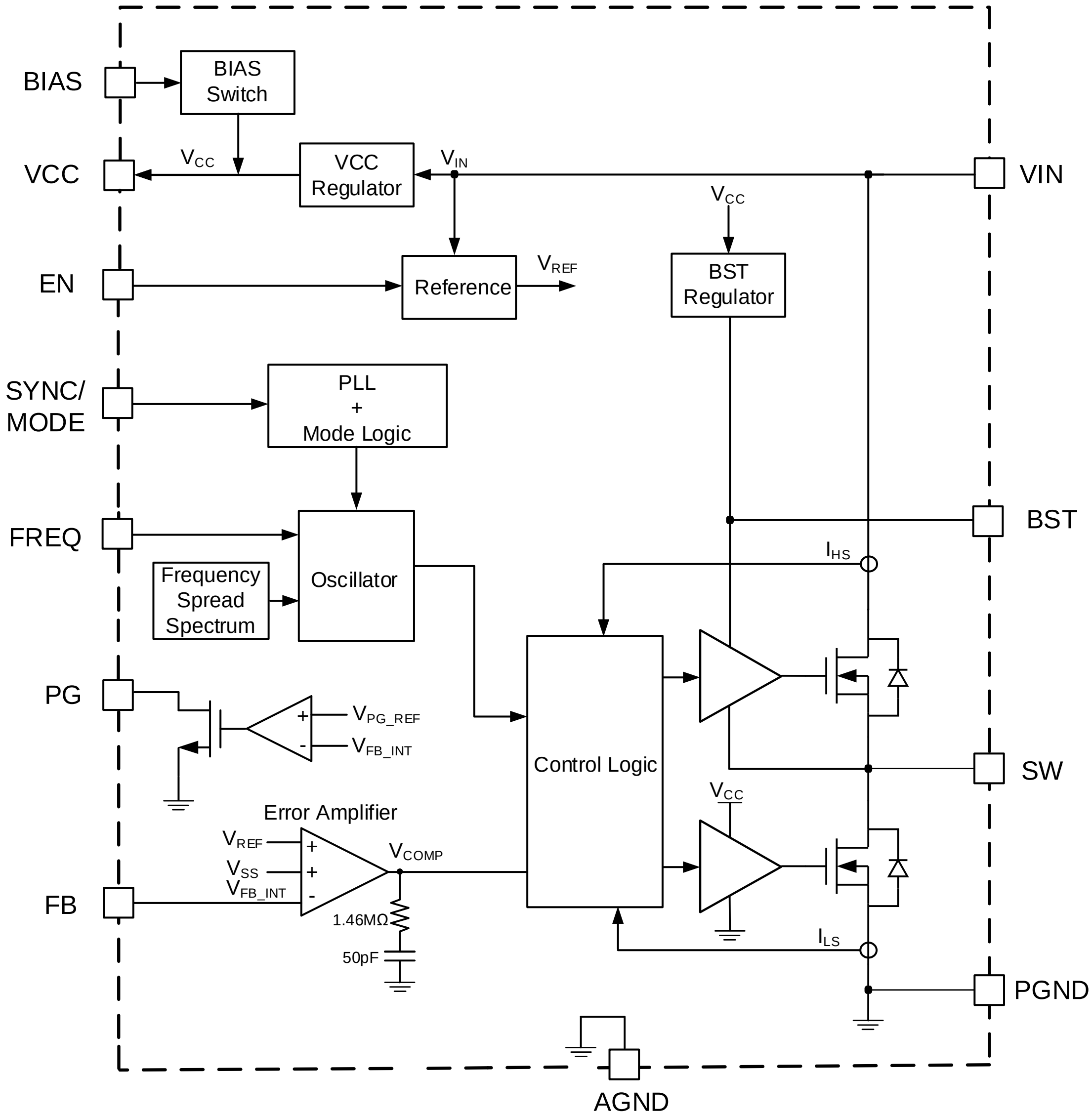


Figure 3: Functional Block Diagram for Adjustable-Output Version

FUNCTIONAL BLOCK DIAGRAMS *(continued)*

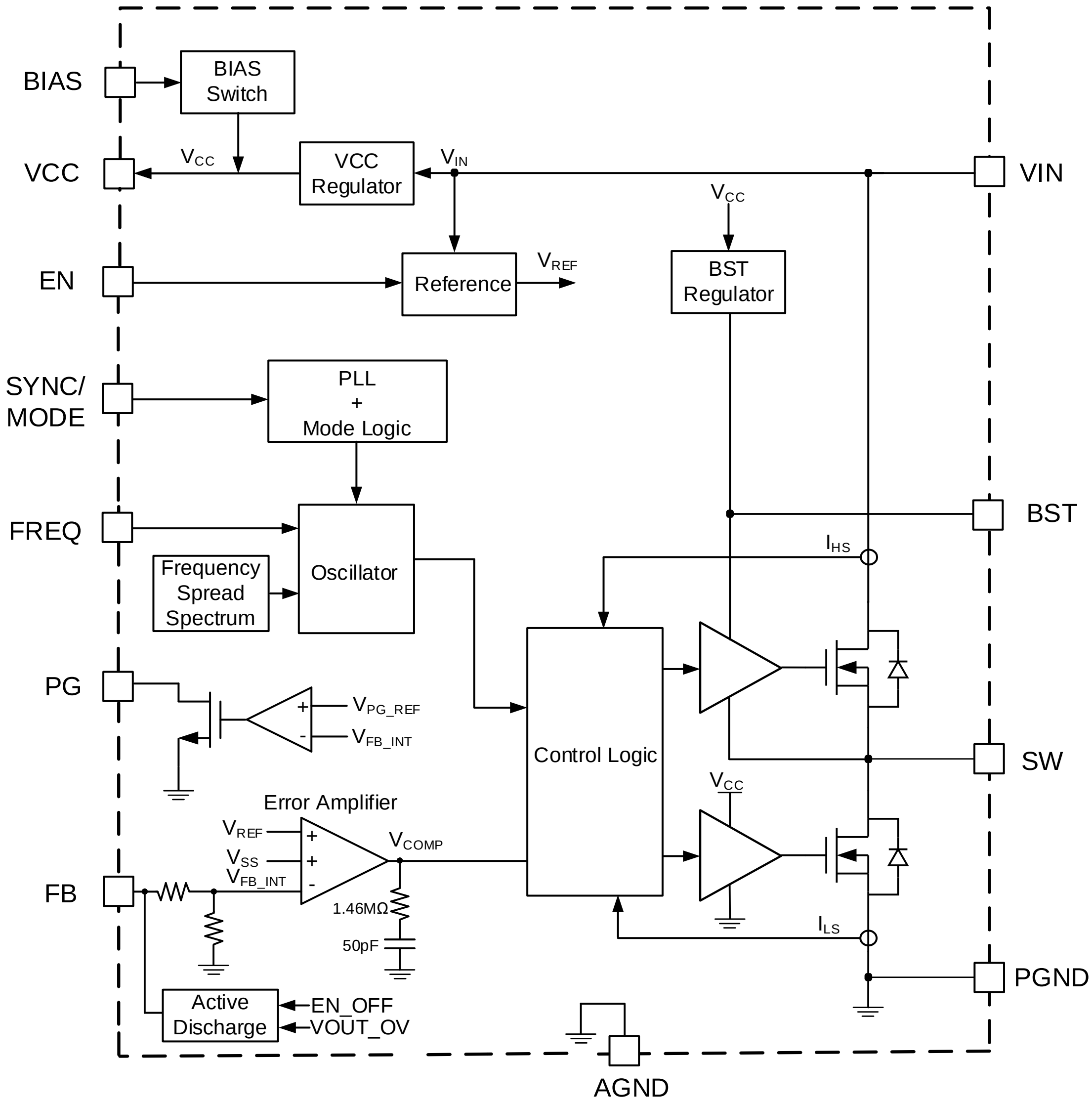


Figure 4: Functional Block Diagram for Fixed-Output Version

OPERATION

The MPQ4326B is a synchronous, step-down switching regulator with integrated internal high-side and low-side power MOSFETs (HS-FETs and LS-FETs, respectively). The family provides 3A to 7A of highly efficient output current (I_{OUT}) with peak current mode control.

The MPQ4326B features a wide input voltage (V_{IN}) range, configurable 200kHz to 2.5MHz switching frequency (f_{SW}), internal soft start (SS), and precise current limiting. The MPQ4326B's very low operational quiescent current (I_Q) makes it well-suited for battery-powered applications.

Pulse-Width Modulation (PWM) Control

At moderate to high output currents, the MPQ4326B operates with fixed-frequency, peak current mode control to regulate the output voltage (V_{OUT}). A pulse-width modulation (PWM) cycle is initiated by the internal clock. At the clock's rising edge, the HS-FET turns on and remains on until the control signal reaches the value set by the internal COMP voltage (V_{COMP}).

When the HS-FET is off, the LS-FET turns on immediately and remains on until the next cycle starts or until the inductor current (I_L) drops below the zero-current detection (ZCD) threshold. The LS-FET remains off for at least the minimum off time (t_{OFF_MIN}) before the next cycle starts.

If the current in the HS-FET cannot reach the value set by V_{COMP} within one PWM period, then the HS-FET remains on and skips a turn-off operation. The HS-FET is forced off until the current reaches the value set by V_{COMP}, or once its 7µs maximum on time is reached. This mode extends the duty cycle, which achieves a low dropout when V_{IN} is almost equal to V_{OUT}.

Mode Selection and Light-Load Operation

The MPQ4326B provides forced continuous conduction mode (FCCM), advanced asynchronous modulation (AAM) mode, and on-the-fly mode selection (see Figure 5).

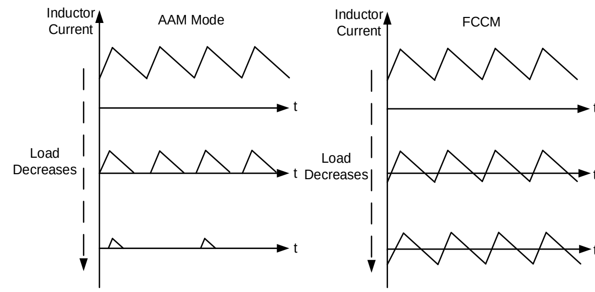


Figure 5: AAM Mode and FCCM

Under light-load conditions, the MPQ4326B can work in two different modes by setting the state of the SYNC/MODE pin.

If SYNC/MODE is pulled above 1.4V or an external clock is used, then the MPQ4326B enters FCCM. In FCCM, the device works with a fixed frequency from no-load to full-load conditions. The advantages of FCCM are its constant frequency and lower output ripple at light loads.

If SYNC/MODE is pulled below 0.4V, then the MPQ4326B enters AAM mode, which optimizes efficiency under light-load and no-load conditions.

The MPQ4326B enters asynchronous operation as I_L approaches 0A under light-load conditions. If the load decreases, V_{COMP} drops to its set value, and the device enters AAM mode. In AAM mode, the internal clock resets once V_{COMP} reaches its set value. The crossover time is used as a benchmark for the next clock. If the load decreases further, the MPQ4326B enters sleep mode, which turns off some internal circuits to achieve a low input quiescent current. If the load increases and V_{COMP} exceeds its set value, the device operates in discontinuous conduction mode (DCM) or continuous conduction mode (CCM) with a constant f_{SW}.

Error Amplifier (EA)

The error amplifier (EA) compares the FB pin voltage (V_{FB}) with the internal reference voltage (V_{REF}) (typically 0.8V) and outputs a current proportional to the difference between the two voltages. This current charges the compensation network to form V_{COMP}, which controls the power MOSFET's duty cycle.

During normal operation, the minimum V_{COMP} is clamped to 0.9V, and the maximum V_{COMP} is clamped to 2V. If the IC shuts down, V_{COMP} is internally pulled down to ground.

Frequency Spread Spectrum (FSS)

The MPQ4326B employs a 7.5kHz modulation frequency with a 128-step triangular profile to spread the internal oscillator frequency across a 20% (±10%) window. The steps vary with the set oscillator frequency to ensure that the exact f_{SW} steps cycle by cycle (see Figure 6).

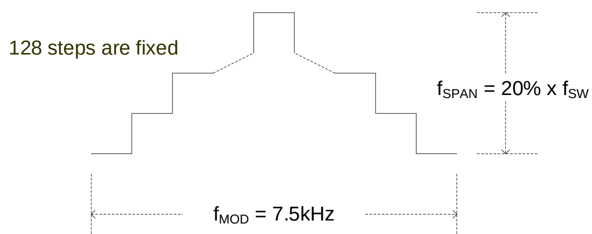


Figure 6: Frequency Spread Spectrum

Sidebands are created by modulating f_{SW} via the triangle modulation waveform. The emission power of the fundamental f_{SW} and its harmonics are distributed into smaller pieces. This significantly reduces peak EMI noise.

Low-Dropout Operation

To improve dropout, the MPQ4326B is designed to operate at close to 100% duty cycle when the BST-to-SW voltage exceeds 2.7V.

When the device works in low-dropout mode, the EA's gain becomes larger, which can reduce V_{COMP} quickly to optimize the V_{OUT} overshoot when exiting dropout mode. Even if V_{IN} rapidly increases, inductor spikes are also minimized.

The effective duty cycle during the regulator's dropout period is mainly influenced by the voltage drops across the power MOSFET, the inductor resistance, the low-side (LS) diode, and the PCB resistance.

Soft Start (SS)

Soft start (SS) prevents V_{OUT} from overshooting during start-up. The SS time (t_{SS}) is fixed internally.

Once t_{SS} starts, the SS voltage (V_{SS}) rises from 0V to 1.2V with a set slew rate. If V_{SS} drops below the 0.8V internal V_{REF}, then V_{SS} takes over and the EA uses V_{SS} as its reference. If V_{SS} exceeds V_{REF}, the EA uses V_{REF} as its reference.

During t_{SS}, the converter operates in AAM mode for smooth SS, regardless of the MODE setting.

During start-up through EN, the first pulse occurs after about 710µs. During this period, the VCC voltage (V_{CC}) is regulated, the internal bias is generated, and the compensator network is charged. After another 2.9ms, V_{OUT} ramps up and reaches its set value. SS is complete after about 1.1ms. PG is also pulled high after a 1.2ms delay.

Pre-Biased Start-Up

If V_{FB} exceeds V_{SS} during start-up ($V_{FB} > V_{SS}$ - 150mV), this means that the output has a pre-biased voltage. Both the HS-FET and LS-FET remain off until V_{SS} exceeds V_{FB}.

Thermal Shutdown

Thermal shutdown is implemented to prevent the chip from thermal runaway. If the silicon die temperature exceeds its upper threshold (170°C), the power MOSFETs shut down. Once the temperature drops below its lower threshold (150°C), the thermal shutdown condition is removed and the chip is enabled again.

Start-Up and Shutdown

If both V_{IN} and the EN voltage (V_{EN}) exceed their respective thresholds, the chip starts up. The reference block starts up first to generate a stable V_{REF} and reference currents. Then the internal regulator is enabled to provide a stable supply for the remaining circuitries.

Once the internal supply rail is up, the LS-FET turns on to charge the BST pin if the voltage between BST and SW (V_{BST-SW}) does not exceed the BST refresh rising threshold (typically 2.7V). The HS-FET remains off during this time. When the SS block is enabled, it first holds its SS output low to ensure that the remaining circuits are ready. Then the SS block slowly ramps up.

Three events shut down the chip: EN going low, V_{IN} falling beneath its UVLO threshold, and thermal shutdown. During the shutdown procedure, the signaling path is blocked first to avoid any fault triggering. Then V_{COMP} pulls down. The floating driver works to disable the HS-FET.

APPLICATION INFORMATION

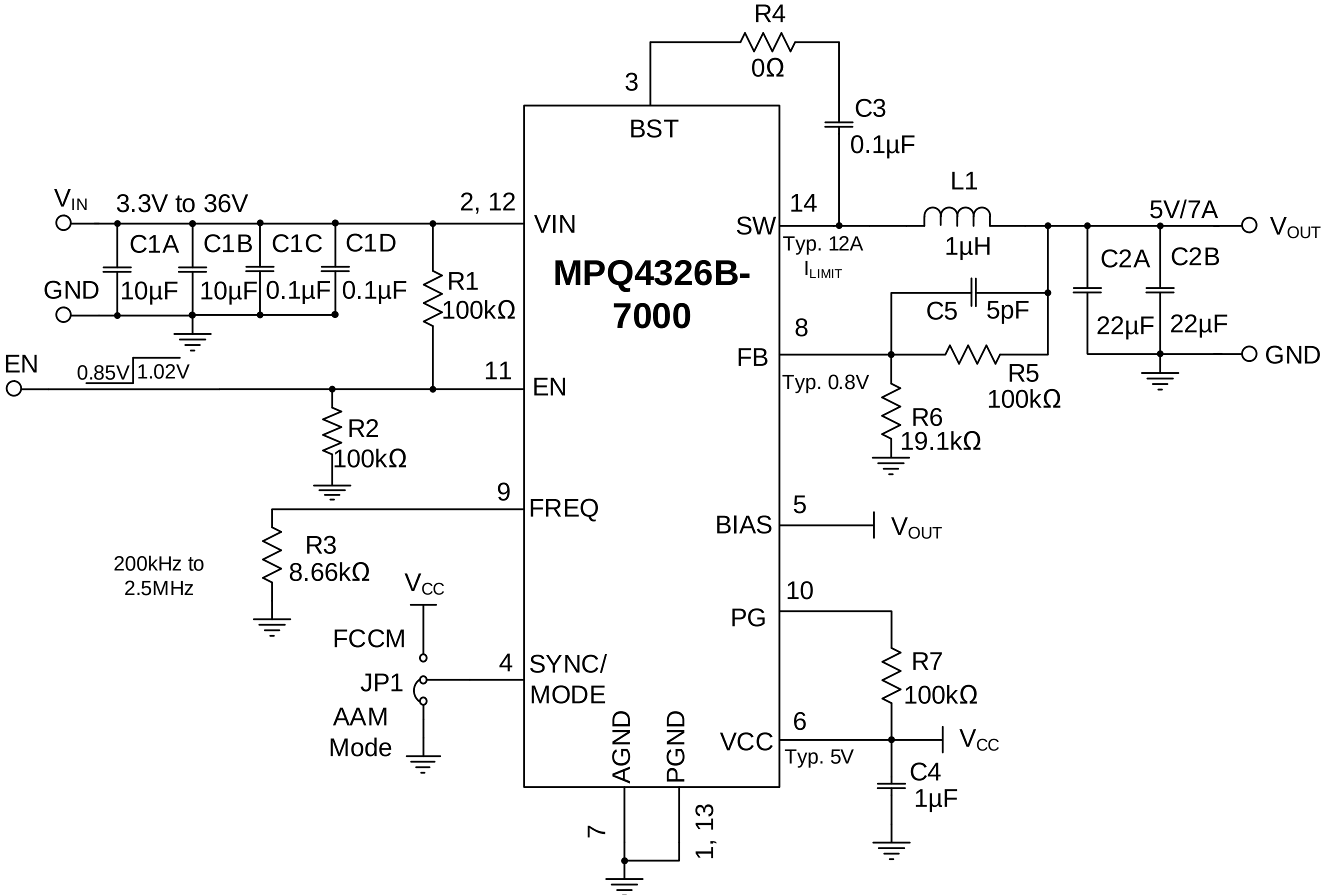


Figure 7: Typical Application Circuit for the MPQ4326B-7000 (V_{OUT} = 5V, f_{SW} = 2.2MHz)

Table 2: Design Guide Index

Pin #	Pin Name	Component	Design Guide Index
2, 12	VIN	C1A, C1B, C1C, C1D	Selecting the Input Capacitors (VIN, Pins 2 and 12)
3	BST	R4, C3	Floating Driver and Bootstrap Charging (BST, Pin 3)
4	SYNC/MODE		SYNC Input and Mode Selection (SYNC/MODE, Pin 4)
5	BIAS		External Bias (BIAS, Pin 5)
6	VCC	C4	Internal Bias Supply (VCC, Pin 6)
8	FB	R5, R6, C5	Feedback (FB, Pin 8)
9	FREQ	R3	Switching Frequency Setting (FREQ, Pin 9)
10	PG	R7	Power Good Indicator (PG, Pin 10)
11	EN	R1, R2	Enable and Under-Voltage Lockout (UVLO) (EN, Pin 11)
14	SW	L1, C2A, C2B	Selecting the Inductor and Output Capacitors (SW, Pin 14)
7	AGND		Connection GND (AGND, Pin 7; PGND, Pins 1 and 3)
1, 13	PGND		Connection GND (AGND, Pin 7; PGND, Pins 1 and 3)

Selecting the Input Capacitors (VIN, Pins 2 and 12)

The step-down converter has a discontinuous input current (I_{IN}) and requires a capacitor to supply AC current to the converter while maintaining the DC input voltage. Use low-ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are highly recommended due to their low ESR and small temperature coefficients.

For most applications, a 4.7µF to 10µF capacitor is sufficient. It is strongly recommended to use an additional, lower-value capacitor (e.g. 0.1µF) with a small package size (0603) to absorb high-frequency switching noise. Place the smaller capacitor as close to VIN and PGND as possible.

Since the input capacitor (C_{IN}) absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in C_{IN} (I_{CIN}) can be estimated with Equation (1):

$$I_{CIN} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (1)$$

The worst-case condition occurs at V_{IN} = 2 x V_{OUT}, which can be calculated with Equation (2):

$$I_{CIN} = \frac{I_{LOAD}}{2} \quad (2)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current. The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, add a small, high-quality ceramic capacitor (e.g. 0.1µF) as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide a sufficient charge to prevent excessive voltage ripple at the input. The input voltage ripple caused by the capacitance can be estimated with Equation (3):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (3)$$

V_{IN} Over-Voltage Protection (OVP)

The MPQ4326B stops switching when V_{IN} exceeds its over-voltage rising threshold (typically 38V). The device resumes switching and normal regulation when V_{IN} drops to the over-voltage falling threshold (typically 37V). For the MPQ4326B-xxx1, the V_{IN} OVP function is disabled.

Floating Driver and Bootstrap Charging (BST, Pin 3)

The bootstrap (BST) capacitor (C3, also called C_{BST}) is recommended to be between 0.1µF and 0.22µF.

It is not recommended to place a resistor (R_{BST}) in series with C_{BST}, unless there is a strict EMI requirement. R_{BST} reduces EMI and voltage stress at high input voltages. A higher resistance is better for switching spike reduction but compromises efficiency. If necessary, R_{BST} should be below 5Ω.

The voltage between the BST and SW pins (V_{BST-SW}) is regulated to about 5V by the dedicated internal bootstrap regulator. If V_{BST-SW} drops below its regulated value, then an N-channel MOSFET pass transistor connected between VCC and BST turns on to charge C_{BST}. The external circuit should provide enough voltage headroom to facilitate charging.

When the HS-FET is on, V_{BST} exceeds V_{CC}, so C_{BST} cannot charge. At higher duty cycles, the time available for bootstrap charging is shorter, so C_{BST} may not be charged sufficiently. If the external circuit has an insufficient voltage and time to charge C_{BST}, additional external circuitry can be used to ensure that V_{BST} remains within its normal operating region.

If V_{BST} reaches its UVLO threshold, then the HS-FET turns off, and the LS-FET turns on for t_{OFF_MIN} to refresh V_{BST} via the set f_{SW}.

SYNC Input and Mode Selection (SYNC/MODE, Pin 4)

The switching frequency (f_{SW}) can be synchronized to the rising edge of a clock signal applied at SYNCIN. The recommended SYNCIN frequency range is between 200kHz and 2.5MHz.

Switching can be synchronized to an external clock within a SCYNCIN clock locking time (128 cycles), ranging from ±10% of the set clock frequency.

When SYNC/MODE is used for mode selection, pull this pin high to allow the part to enter FCCM; pull this pin low to allow the part to enter AAM mode.

Table 3 shows the details for mode selection.

Table 3: Mode Selection

SYNC/MODE Input	Operation
<0.4V	AAM mode
>1.4V	FCCM
External clock in	FCCM

External Bias (BIAS, Pin 5)

BIAS is the external bias pin. When BIAS is connected to the 5V voltage, the internal LDO turns off, and a smaller input supply current enables higher efficiency. If the BIAS pin voltage (V_{BIAS}) exceeds 4.6V, the pin starts to work; if V_{BIAS} drops below 4.36V, the pin is disabled. For the 5V output version, connect BIAS to V_{OUT} directly. For the other lower (<4.6V) or higher (>6V) output versions, connect BIAS to the external 5V source to achieve a lower input supply current, or connect BIAS to ground to disable the bias function. It is recommended to avoid providing V_{BIAS} before V_{IN}.

Internal Bias Supply (VCC, Pin 6)

The VCC capacitance (C4) is recommended to be 1µF.

Most of the internal circuitry is powered by the internal 5V VCC regulator. This regulator uses V_{IN} as its input and operates across the entire V_{IN} range. If V_{IN} exceeds 5V, then V_{CC} is in full regulation. If V_{IN} drops below 5V, then the VCC output degrades.

FB, Feedback (FB, Pin 8)

For the adjustable-output version, the typical feedback voltage (V_{FB}) is 0.8V. The external resistor dividers (R5 and R6) connected to FB sets V_{OUT} (see Figure 8).

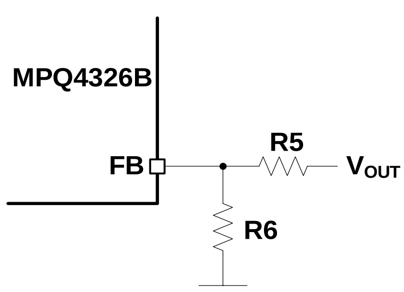


Figure 8: Feedback Divider Network of Adjustable Output Version

R6 can be calculated with Equation (4):

$$R6 = \frac{R5}{\frac{V_{OUT}}{0.8V} - 1} \quad (4)$$

Table 4 shows the recommended feedback resistances for common output voltages.

Table 4: Resistor Selection for Output Voltages

V_{OUT} (V)	R5 (kΩ)	R6 (kΩ)
3.3	100 (0.1%)	31.6 (0.1%)
5	100 (0.1%)	19.1 (0.1%)

For the fixed-output version, the FB resistor dividers (R_{FB1} and R_{FB2}) are integrated internally (see Figure 9). Connect FB directly to the output to set V_{OUT}. The following fixed outputs can be selected: 1V, 1.8V, 2.5V, 3.0V, 3.3V, 3.8V, or 5V.

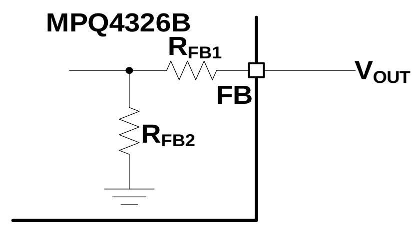


Figure 9: Feedback Divider Network of Fixed Output Version

Table 5 shows the relationship between the internal R_{FBx} and V_{OUT}.

Table 5: R_{FBx} vs. V_{OUT}

V_{OUT} (V)	R_{FB1} (kΩ)	R_{FB2} (kΩ)
1	64	256
1.8	320	256
2.5	544	256
3.0	704	256
3.3	800	256
3.8	960	256
5	1344	256

Switching Frequency Setting (FREQ, Pin 9)

A frequency resistor (R3, also called R_{FREQ}) can be used to set f_{SW} (see Figure 10 and Figure 11 on page 59).

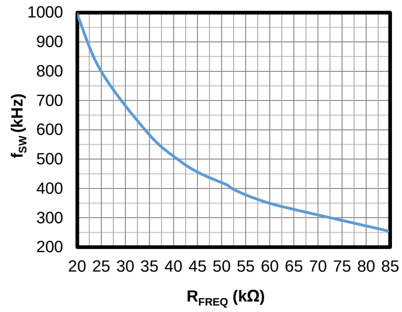


Figure 10: Setting f_{SW} = 200kHz to 1000kHz

Figure 11 shows when f_{SW} is set between 1000kHz and 2500kHz.

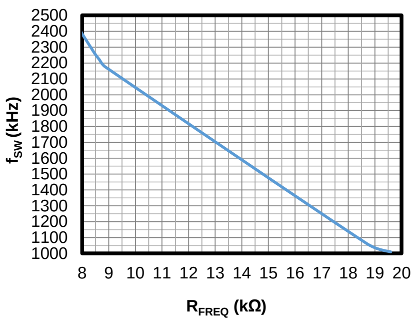


Figure 11: Setting f_{SW} = 1000kHz to 2500kHz

Table 6 shows the relationship between f_{SW} and R_{FREQ}.

Table 6: f_{SW} vs. R_{FREQ}

R_{FREQ} (kΩ)	f_{SW} (kHz)
7.87	2500
8.66	2200
14.3	1500
18.7	1060
19.6	1000
24.9	800
34.8	590
43.2	470
49.9	410
52.3	400
56.2	370
62	340
84.5	255
100	210

Power Good Indicator (PG, Pin 10)

The MPQ4326B includes an open-drain power good output that indicates whether V_{OUT} is within a specific window of its nominal range. The PG resistor (R7, also called R_{PG}) is recommended to have a resistance of about 100kΩ.

If PG is used, connect it to a logic high power source in the system via a pull-up resistor. If V_{OUT} is within 94.5% to 105.5% of the nominal voltage, PG goes high; if V_{OUT} exceeds 107% or drops below 93% of the nominal voltage, PG goes low. Float PG if it is not used.

Enable and Under-Voltage Lockout (UVLO) (EN, Pin 11)

EN is a digital control pin that turns the regulator on and off.

Enabled by an External Logic High/Low Signal

If V_{EN} reaches about 0.7V, the bandgap (BG) does not turn on until V_{IN} exceeds about 2.7V. The BG then provides an accurate V_{REF} for the EN threshold. Pull EN above its rising threshold (1.02V) to enable the device. Pull EN below 0.85V to shut down the device. There is no internal pull-up or pull-down resistor connected to EN. Do not float EN to avoid uncertain states. If the control signal cannot give an accurate high or low logic, then an external pull-up or pull-down resistor is required.

Configurable V_{IN} Under-Voltage Lockout (UVLO) Threshold

The MPQ4326B has an internal, fixed UVLO threshold. The rising threshold is 3.7V, and the falling threshold is about 2.9V. For applications that require a higher UVLO level, place an external resistor divider between VIN and EN to raise the equivalent UVLO threshold (see Figure 12).

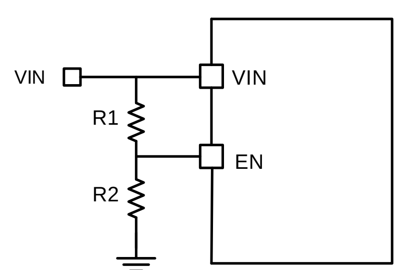


Figure 12: Adjustable UVLO Using EN Divider

The UVLO rising and falling thresholds can be calculated with Equation (5) and Equation (6), respectively:

$$V_{IN\_RISING}=(1+\frac{R1}{R2})\times V_{EN\_RISING} \quad (5)$$

$$V_{IN\_FALLING}=(1+\frac{R1}{R2})\times V_{EN\_FALLING} \quad (6)$$

Where V_{EN_RISING} is 1.02V, and $V_{EN\_FALLING}$ is 0.85V.

If EN is not used to turn the device on and off, connect EN to a high-voltage source (e.g. VIN) to turn the device on by default.

Selecting the Inductor and Output Capacitors (SW, Pin 14)

The inductance (L1) can be calculated with Equation (7):

$$L1 = \frac{V_{OUT}}{f_{SW} \times \Delta I_L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (7)$$

Where ΔI_L is the peak-to-peak inductor ripple current.

A 1µH to 68µH inductor with a DC current rating at least 25% higher than the maximum load current is recommended for most applications. For higher efficiency, choose an inductor with a lower DC resistance. A larger-value inductor results in less ripple current and a lower output ripple voltage; however, it also has a larger physical size, higher series resistance, and lower saturation current. A small-sized inductor provides benefits for EMI. A good rule to determine the inductance is to allow the inductor ripple current to be approximately 30% of the maximum load current.

The peak inductor current (I_{LP}) can be calculated with Equation (8):

$$I_{LP} = I_{LOAD} + \frac{V_{OUT}}{2 \times f_{SW} \times L1} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (8)$$

Choose an inductor that does not saturate under I_{LP}.

Peak and Valley Current Limits

Both the HS-FET and LS-FET have cycle-by-cycle current limit protection. If I_L reaches the high-side (HS) peak current limit (typically 12A for the MPQ4326B-7xxx) while the HS-FET is on, then the HS-FET is immediately forced off to prevent the current from rising further.

When the LS-FET is on, the next clock's rising edge is held until I_L drops below the LS valley current limit (typically 8A for the MPQ4326B-7xxx). Once the HS-FET turns on again, I_L drops to a sufficiently low value. This current limit scheme prevents current runaway if an overload or short-circuit event occurs.

Short-Circuit Protection (SCP)

If the output is shorted to ground, and V_{OUT} drops below 70% of its nominal output, then the IC shuts down momentarily and begins discharging V_{SS}. The device restarts with a full soft start after about 32ms. This hiccup process is repeated until the fault is removed.

During the hiccup period, if V_{FB} reaches 50% of the internal V_{REF}, the device triggers short-circuit protection (SCP) recovery and initiates SS to avoid large spikes. When applying the SCP function, V_{IN} is recommended to be below 28V.

The output voltage ripple (ΔV_{OUT}) can be estimated with Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L1} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}}) \quad (9)$$

Where L1 is the inductance, and R_{ESR} is the output capacitor's equivalent series resistance (ESR).

C_{OUT} maintains the DC output voltage. Use ceramic, tantalum, or low-ESR electrolytic capacitors. For the best results, use low-ESR capacitors to keep ΔV_{OUT} low.

For ceramic capacitors, the capacitance dominates the impedance at f_{SW} and causes the majority of ΔV_{OUT}. For simplification, ΔV_{OUT} can be estimated with Equation (10):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^2 \times L1 \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (10)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at f_{SW}. For simplification, ΔV_{OUT} can be estimated with Equation (11):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L1} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (11)$$

When selecting C_{OUT}, consider the allowable overshoot in V_{OUT} if the load is suddenly removed. In this scenario, energy stored in the inductor is transferred to C_{OUT}, causing its voltage to rise.

To achieve an optimal overshoot relative to the regulated voltage, C_{OUT} can be estimated with Equation (12):

$$C_{OUT} = \frac{I_{OUT}^2 \times L1}{V_{OUT}^2 \times ((V_{OUTMAX} / V_{OUT})^2 - 1)} \quad (12)$$

Where V_{OUT_MAX} / V_{OUT} is the allowable maximum overshoot.

After calculating the capacitance that meets both the ripple and overshoot requirements, choose the larger capacitance.

The C_{OUT} characteristics also affect the stability of the regulation system. The MPQ4326B can be optimized for a wide range of capacitances and ESR values.

Output Over-Voltage Protection (OVP) and Discharge

If V_{OUT} exceeds 130% of its nominal regulation value, the MPQ4326B stops switching. An internal discharge path from FB to ground discharges V_{OUT}. This discharge path is only activated if the output is fixed. Once V_{OUT} drops back to 125% of its nominal voltage, the discharge path is disabled, and the device resumes switching.

For the fixed-output version, the V_{OUT} discharge path is also activated if a shutdown through EN occurs. Once V_{CC} drops to its UVLO threshold, the discharge path is disabled.

Connection GND (AGND, Pin 7; PGND, Pins 1 and 13)

See the PCB Layout Guidelines section on page 62 for more details.

PCB Layout Guidelines [16]

Efficient PCB layout, especially for input capacitor placement, is critical for stable operation. A 4-layer layout is strongly recommended to improve thermal performance. For the best results, refer to Figure 13 and follow the guidelines below:

1. Place the symmetric input capacitors as close to VIN and PGND as possible.
2. Use a large ground plane to connect directly to PGND.
3. Add vias near PGND if the bottom layer is a ground plane.
4. Ensure that the high-current paths at GND and VIN have short, direct, and wide traces.
5. Place the ceramic input capacitor, especially the small package size (0603) input bypass capacitor, as close to VIN and PGND as possible to minimize high-frequency noise.
6. Keep the connection of the input capacitor and VIN as short and wide as possible.
7. Place the VCC capacitor as close to VCC and AGND as possible.
8. Route SW and BST away from sensitive analog areas, such as FB.
9. Reduce the SW node's routing size for better EMI.
10. Place the feedback resistors close to the chip to ensure the trace that connects to FB is as short as possible.
11. Use multiple vias to connect the power planes to the internal layers.

Note:

16) The recommended PCB layout is based on Figure 7 on page 56.

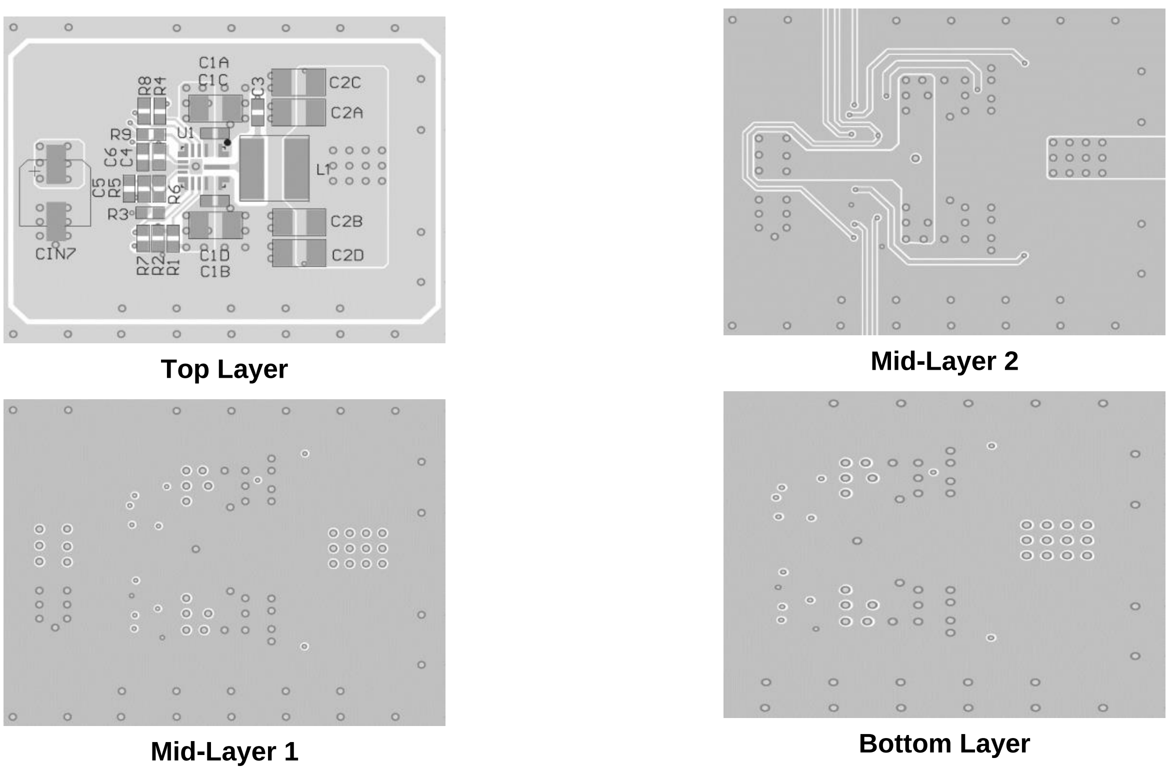


Figure 13: Recommended PCB Layout

TYPICAL APPLICATION CIRCUITS

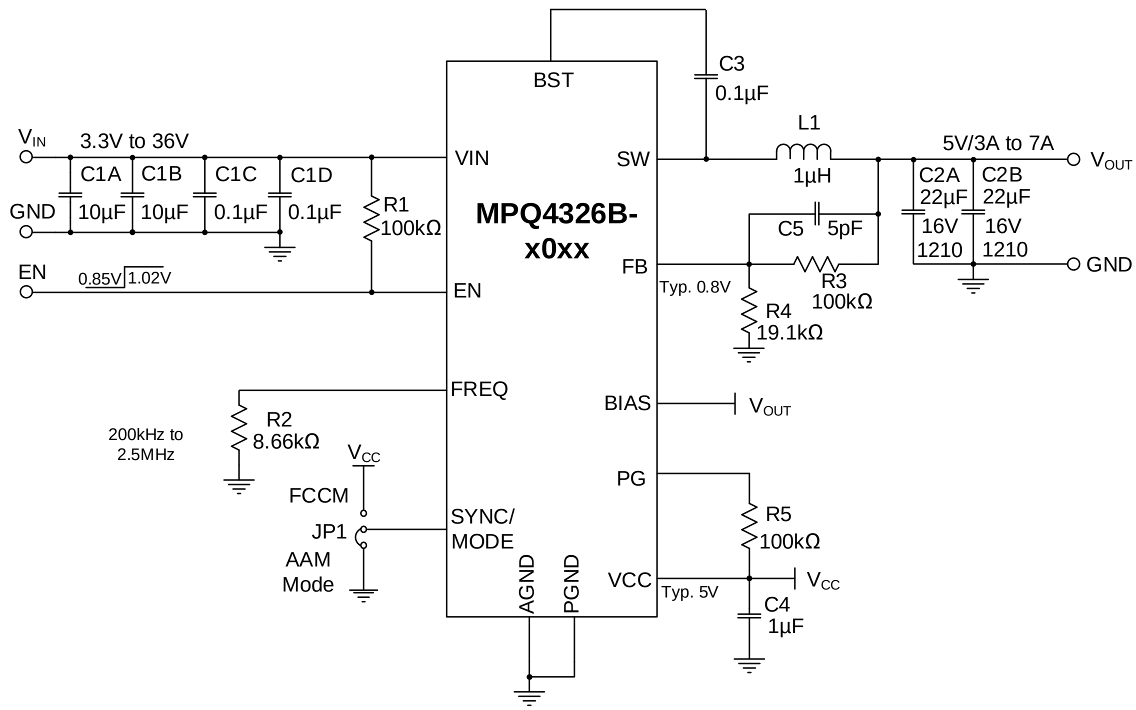


Figure 14: MPQ4326B-xxxx Typical Application Circuit (Adjustable Output, V_{OUT} = 5V, f_{SW} = 2.2MHz)

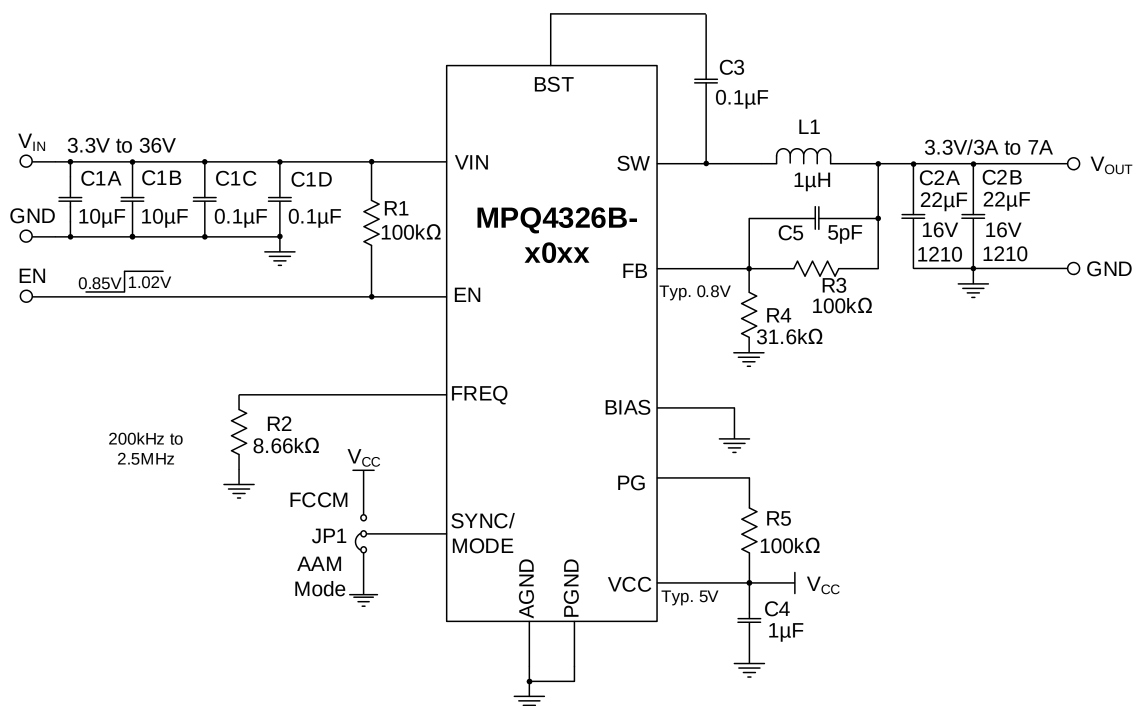


Figure 15: MPQ4326B-xxxx Typical Application Circuit (Adjustable Output, V_{OUT} = 3.3V, f_{SW} = 2.2MHz)

TYPICAL APPLICATION CIRCUITS *(continued)*

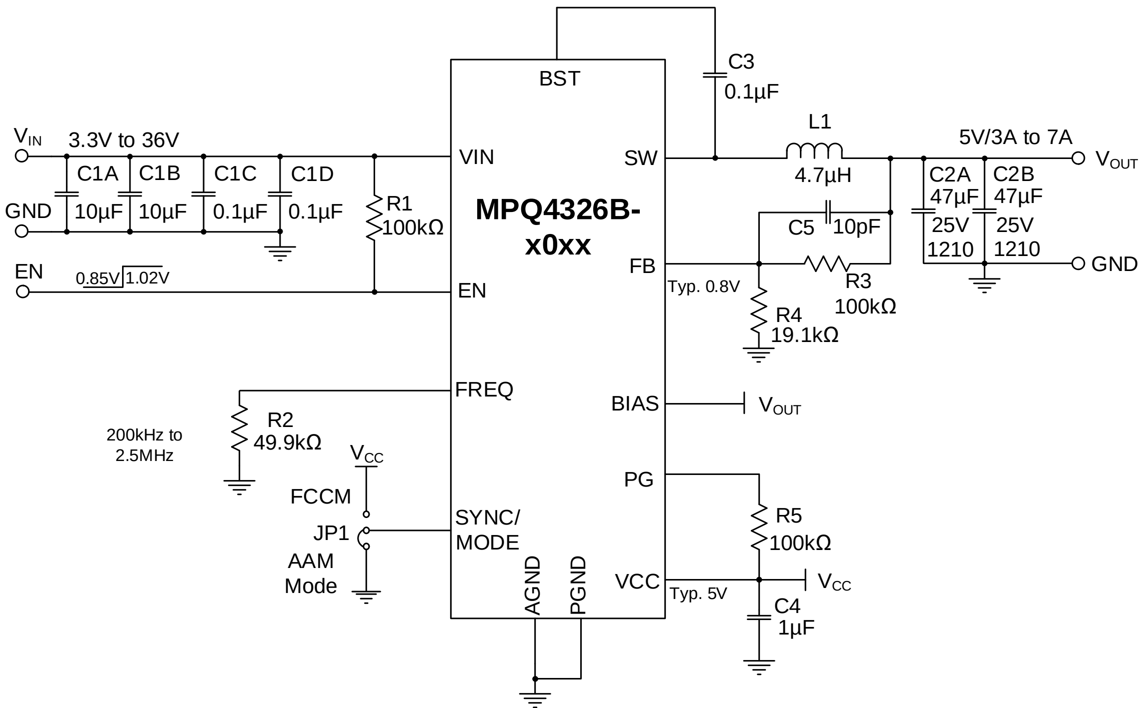


Figure 16: MPQ4326B-xxxx Typical Application Circuit (Adjustable Output, V_{OUT} = 5V, f_{SW} = 410kHz)

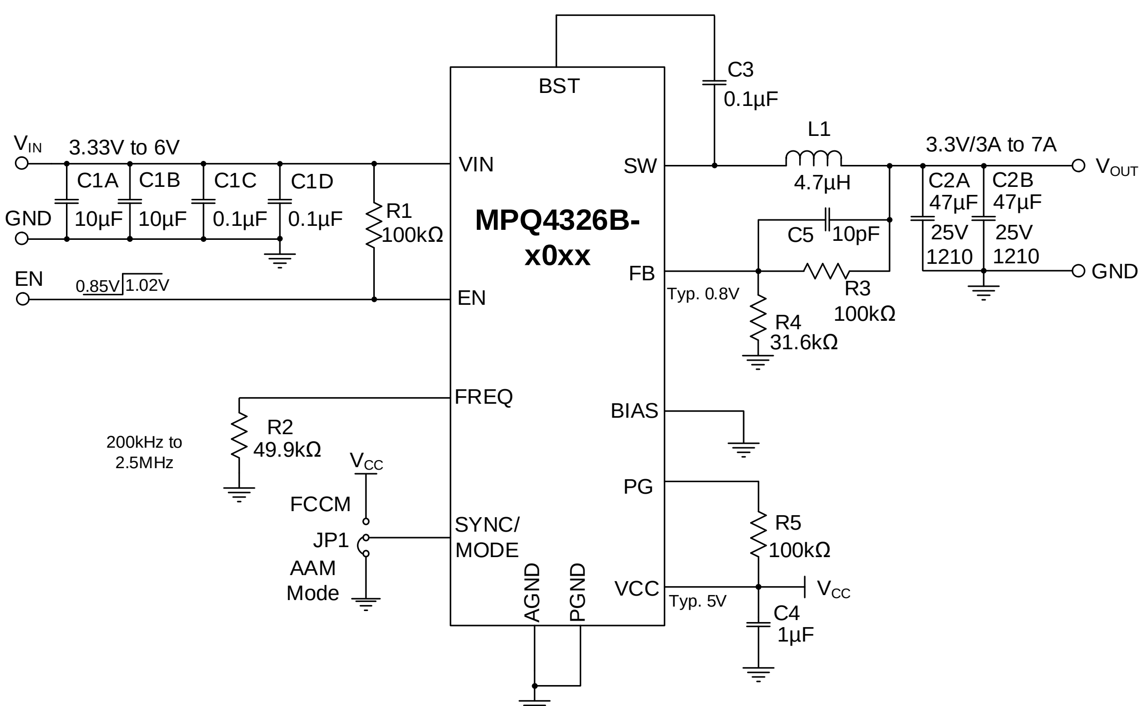


Figure 17: MPQ4326B-xxxx Typical Application Circuit (Adjustable Output, V_{OUT} = 3.3V, f_{SW} = 410kHz)

TYPICAL APPLICATION CIRCUITS *(continued)*

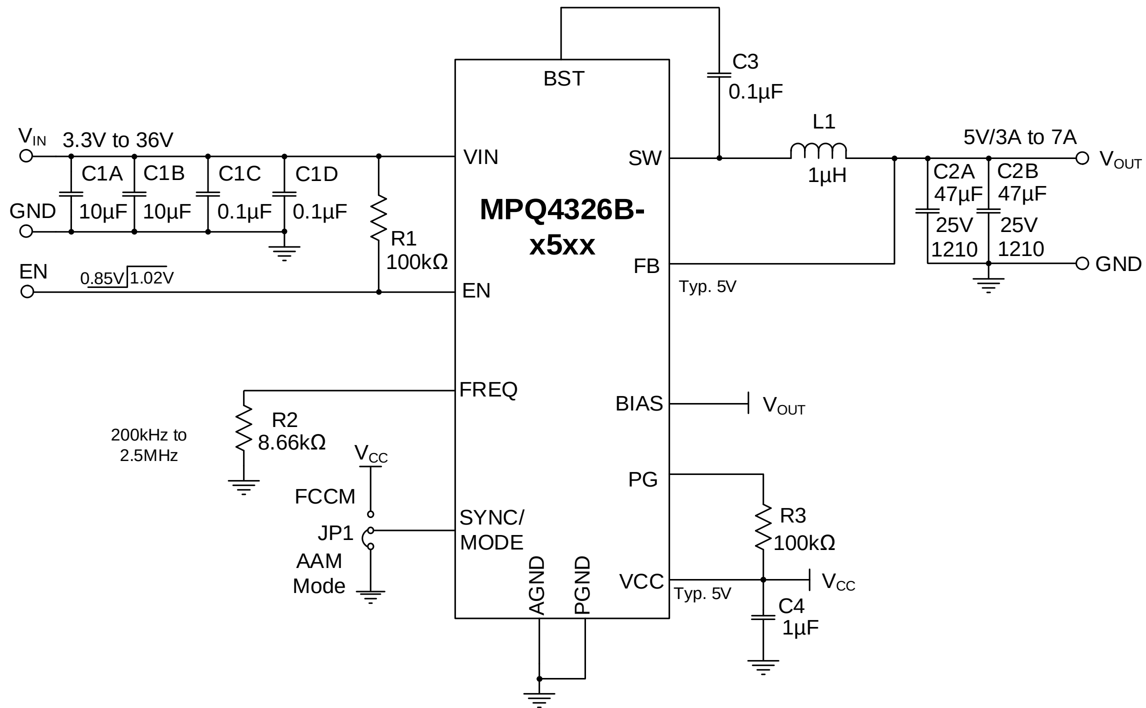


Figure 18: MPQ4326B-xxxx Typical Application Circuit (Fixed Output, V_{OUT} = 5V, f_{SW} = 2.2MHz)

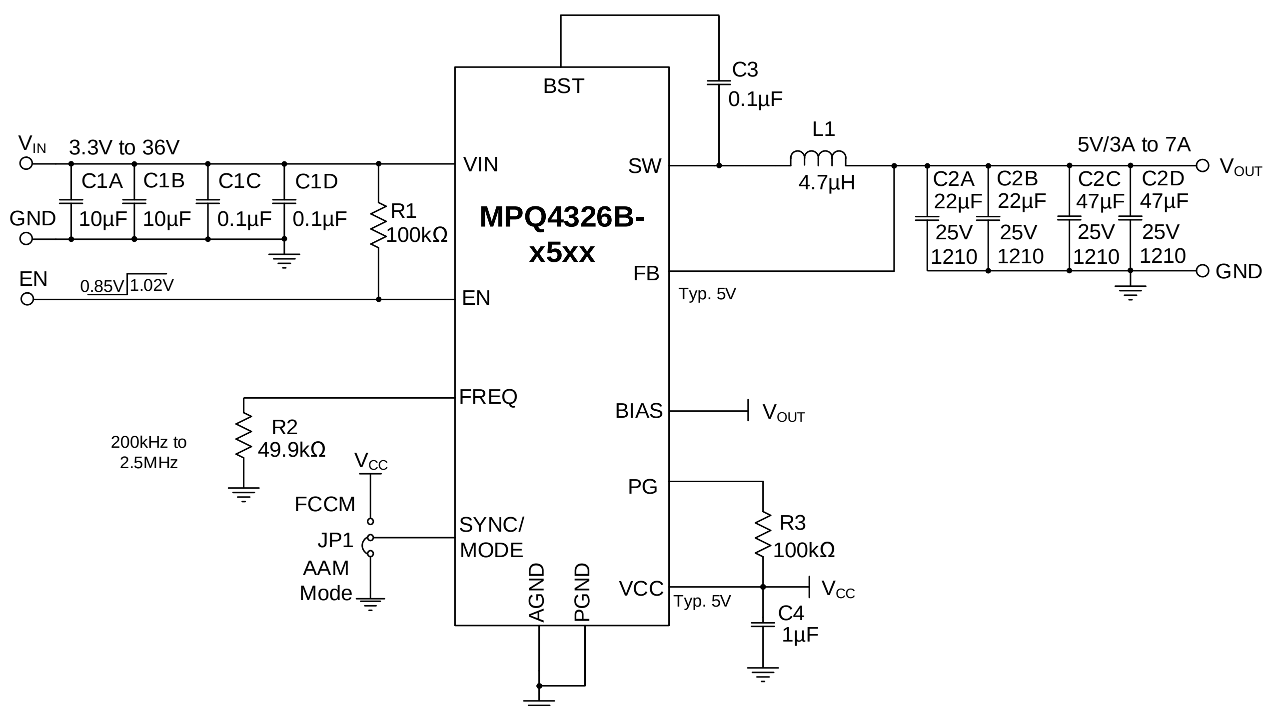


Figure 19: MPQ4326B-xxxx Typical Application Circuit (Fixed Output, V_{OUT} = 5V, f_{SW} = 410kHz)

TYPICAL APPLICATION CIRCUITS *(continued)*

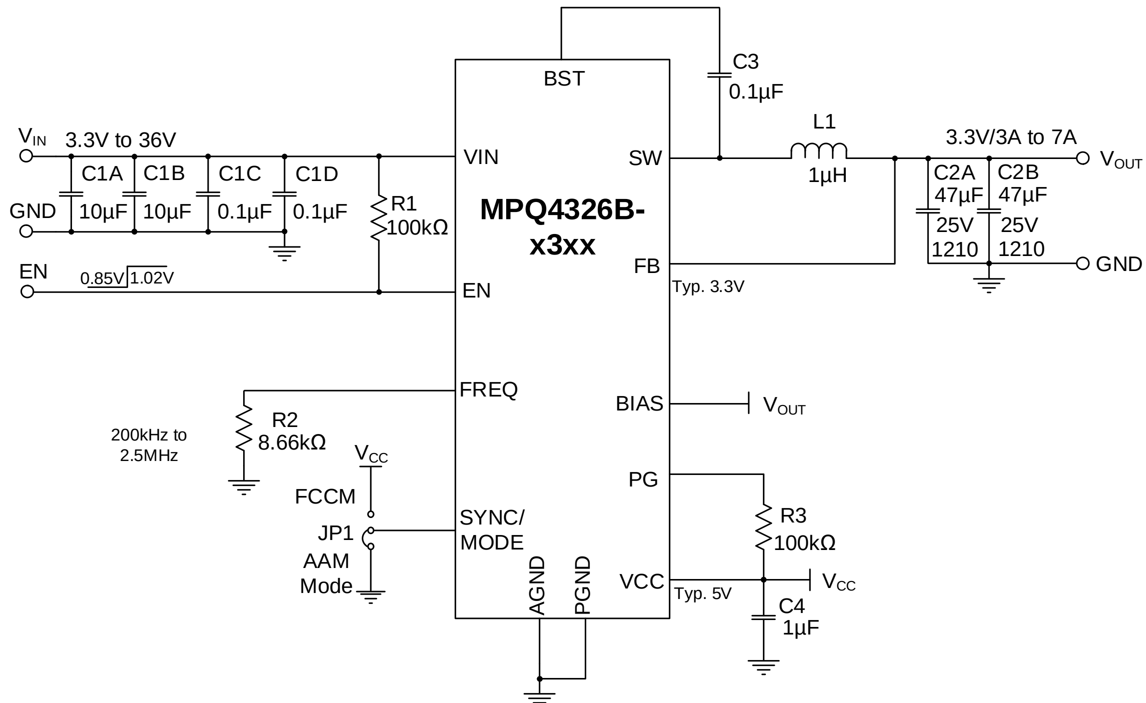


Figure 20: MPQ4326B-xxxx Typical Application Circuit (Fixed Output, V_{OUT} = 3.3V, f_{SW} = 2.2MHz)

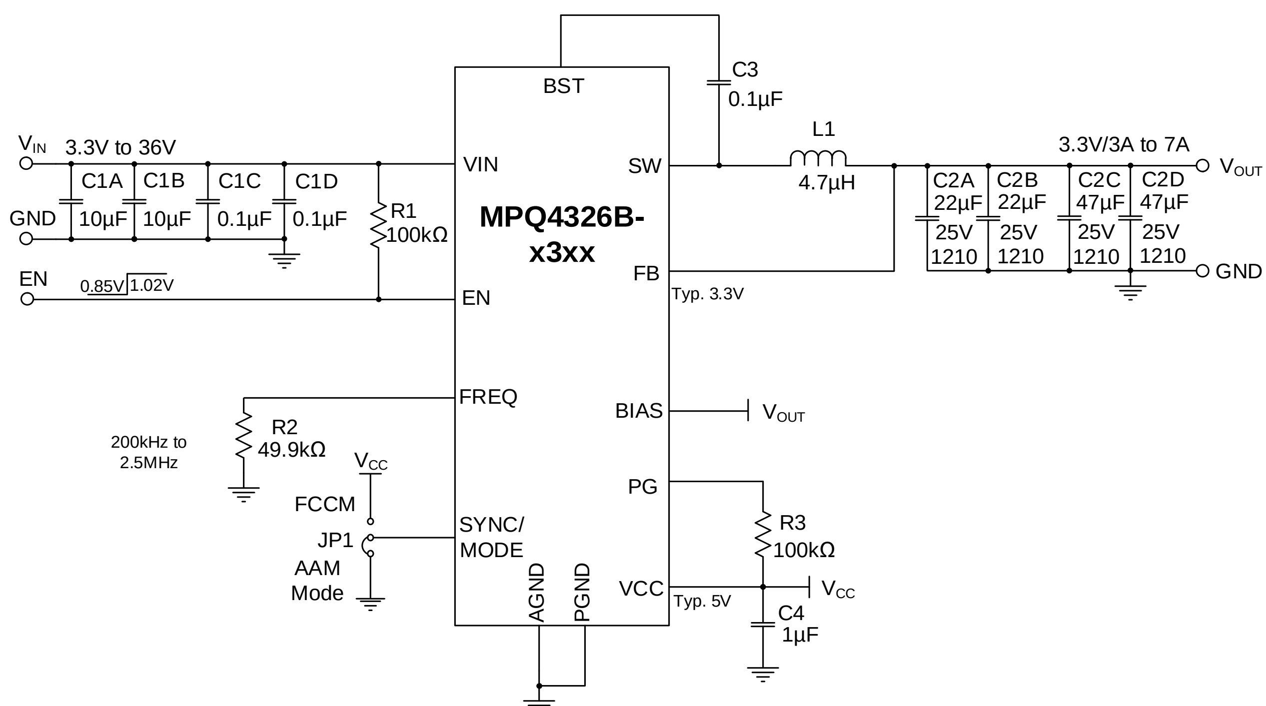


Figure 21: MPQ4326B-xxxx Typical Application Circuit (Fixed Output, V_{OUT} = 3.3V, f_{SW} = 410kHz)

TYPICAL APPLICATION CIRCUITS *(continued)*

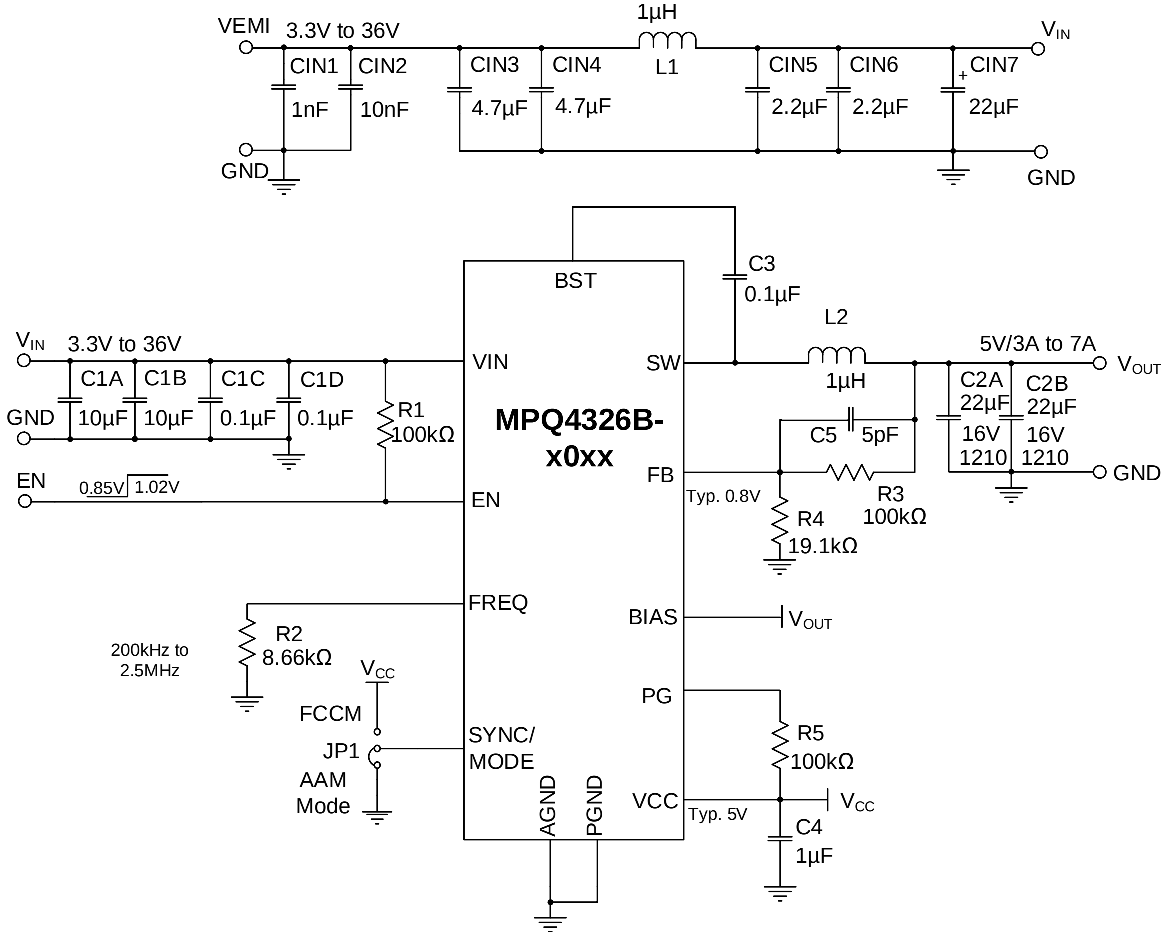


Figure 22: MPQ4326B-xxxx Typical Application Circuit (Adjustable Output, V_{OUT} = 5V, f_{SW} = 2.2MHz with EMI Filters)

TYPICAL APPLICATION CIRCUITS *(continued)*

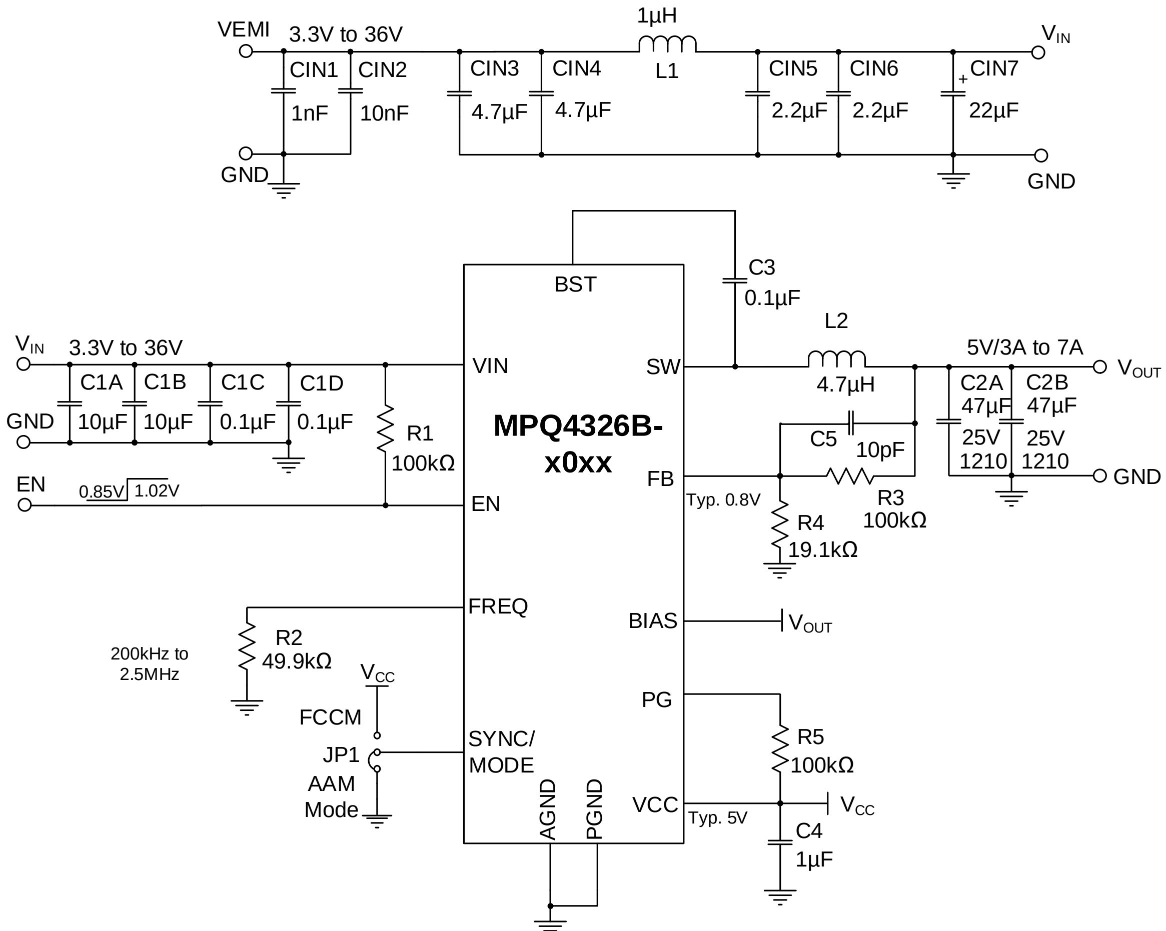
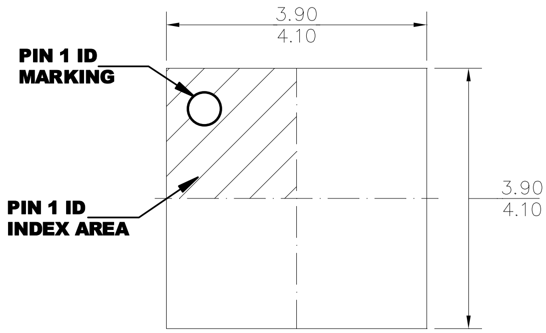


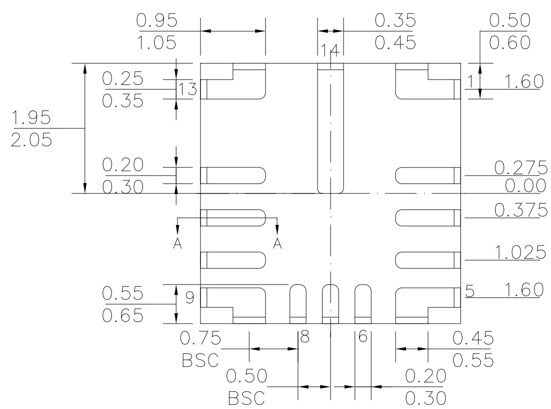
Figure 23: MPQ4326B-xxxx Typical Application Circuit (Adjustable Output, V_{OUT} = 5V, f_{SW} = 410kHz with EMI Filters)

PACKAGE INFORMATION

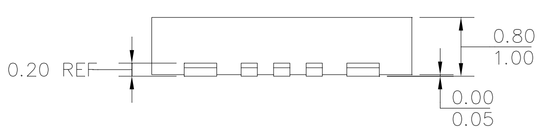
QFN-14 (4mmx4mm)
Wettable Flank



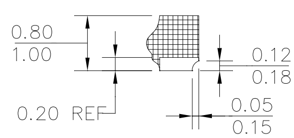
TOP VIEW



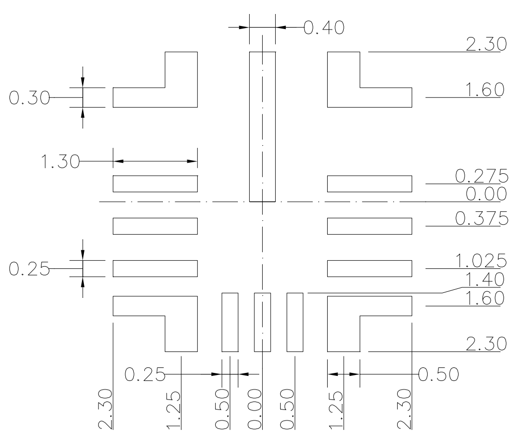
BOTTOM VIEW



SIDE VIEW



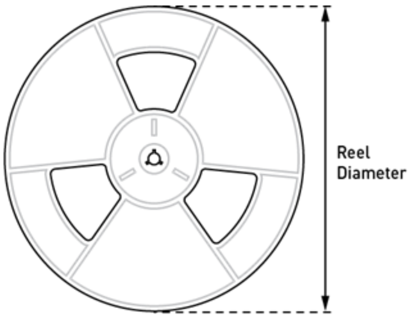
SECTION A-A

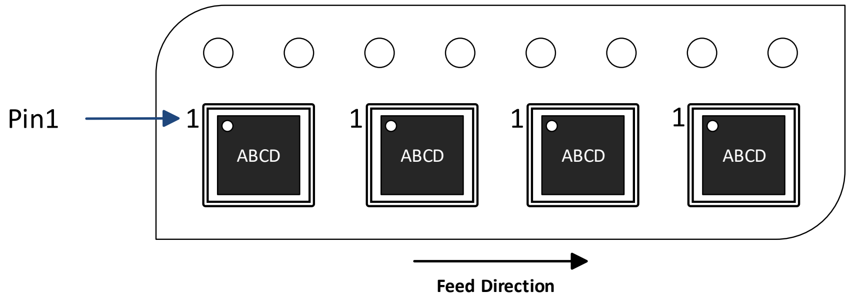


RECOMMENDED LAND PATTERN

NOTE:
1) THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION





Part Number	Package Description	Quantity/ Reel	Quantity/ Tube (17)	Quantity/ Tray (17)	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ4326BGRE-xxxx-AEC1-Z	QFN-14 (4mmx4mm)	5000	N/A	N/A	13in	12mm	8mm

Note:

17) N/A indicates "not available" in tube and tray. For 500-piece tape & reel prototype quantities, contact the factory. (The order code for a 500-piece partial reel order is "-P". Tape & reel dimensions are the same as the full reel.)

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	7/9/2024	Initial Release	-