MPQ4232A

36V, 6A, Buck-Boost Converter with Four Integrated MOSFETs and I²C Interface, AEC-Q100 Qualified

DESCRIPTION

The MPQ4232A is a synchronous, four-switch buck-boost converter with integrated MOSFETs. The device can deliver up to 6A of output current (I_{OUT}) at certain input voltage (V_{IN}) supply ranges with excellent efficiency.

The MPQ4232A is suitable for USB power delivery (PD) and wireless charging applications. It can work well with external PD or wireless charging controllers via the I²C interface.

The I²C interface and one-time programmable (OTP) memory provide flexibility for configurable parameters.

Fault condition protections include constant-current (CC) limiting, output and input over-voltage protection (OVP), and thermal shutdown (TSD).

The MPQ4232A requires a minimal number of readily available, standard external components, and is available in a small QFN-19 (4mmx5mm) package with wettable flanks. The MPQ4232A is available in AEC-Q100 Grade 1.

FEATURES

- 6A Buck-Boost Converter with Four Integrated MOSFETs
- 3V to 36V Operating Input Voltage (V_{IN}) Range, 2.7V Falling Voltage
- 1V to 24V Output Voltage (V_{OUT}) Range
- I²C-Configurable Reference Voltage (V_{REF}) Range: 0.1V to 2.147V with 1mV Resolution
- Up to 98.14% Peak Efficiency
- Integrated 5V/60mA Low-Dropout (LDO) Regulator to Supply External Microcontroller Unit (MCU)
- Selectable Input or Output Constant-Current (CC) Limit with 5% Accuracy via Factory Trimming

FEATURES *(continued)*

- Accurate Output Current (I_{OUT}) Monitor
- Selectable 280kHz, 400kHz, or 530kHz Switching Frequency (f_{SW}) with Frequency Spread Spectrum (FSS)
- Selectable Automatic Pulse-Frequency Modulation (PFM) or Pulse-Width Modulation (PWM) Mode and Forced PWM (FPWM) Mode
- Configurable I²C Target Address Supported by the ADDR Pin and I²C Register
- Line Drop Compensation
- I²C, Alert, and One-Time Programmable (OTP) Memory
- Enable (EN) Shutdown Passive Discharge
- Available in a QFN-19 (4mmx5mm) Package with Wettable Flanks
- Available in AEC-Q100 Grade 1

APPLICATIONS

- Generic Buck-Boost Applications
- USB Power Delivery (PD)
- Wireless Charging
- Automotive Camera Electronic Control Units (ECUs)
- Automotive Lighting
- Automotive Advanced Driver-Assistance Systems (ADAS)

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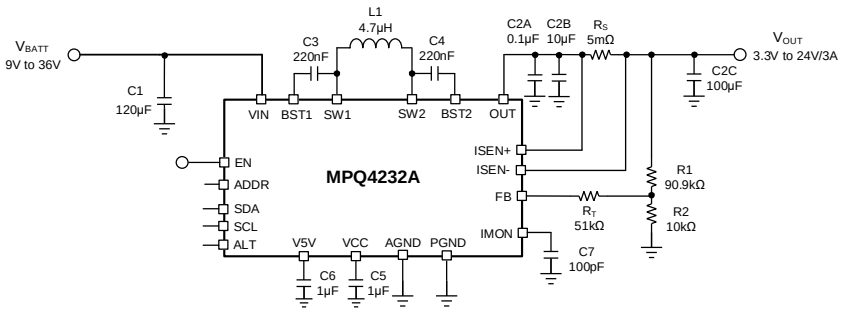
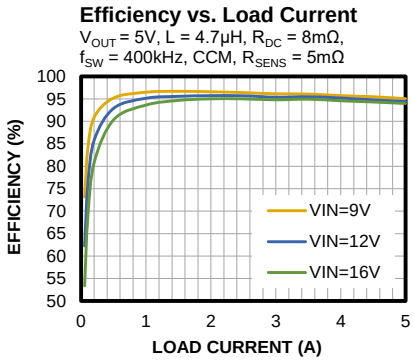
TYPICAL APPLICATION





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ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MPQ4232AGVE-0000-AEC1	QFN-19 (4mmx5mm)	*See Below*	1
MPQ4232AGVE-xxxx-AEC1**			
EVKT-MPQ4232A	Evaluation kit	-	-

* For Tape & Reel, add suffix -Z (e.g. MPQ4232AGVE-xxxx-AEC1-Z).

** “xxxx” is the configuration code identifier for the register setting stored in the one-time programmable (OTP) memory, and it cannot be configured by the user again. Each “x” can be a hexadecimal value between 0 and F. The default code is “0000”. Work with an MPS FAE to create this unique number.

TOP MARKING

MPSYWW
M4232A
LLLLLL
E

MPS: MPS prefix
Y: Year code
WW: Week code
M4232A: Part number
LLLLLL: Lot number
E: Wettable flank

EVALUATION KIT EVKT-MPQ4232A

EVKT-MPQ4232A kit contents (items below can be ordered separately):

#	Part Number	Item	Quantity
1	EVQ4232A-VE-00A	MPQ4232A evaluation board	1
2	EVKT-USBI2C-02 bag	Includes one USB-to-I²C communication interface, one USB cable, and one ribbon cable	1
3	MPQ4232AGVE-0000-AEC1	The MPQ4232A cannot be configured by the user again.	1
4	Online resources	Include the datasheet, user guide, product brief, and GUI	-

Order directly from MonolithicPower.com or our distributors.

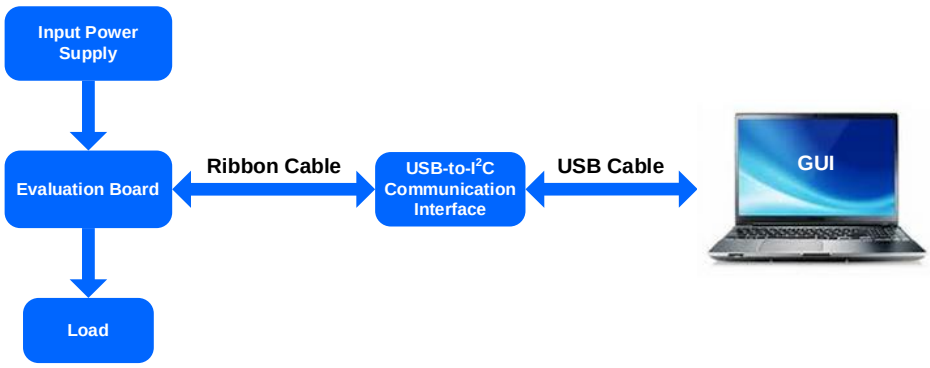

Figure 1: EVKT-MPQ4232A Evaluation Kit Set-Up

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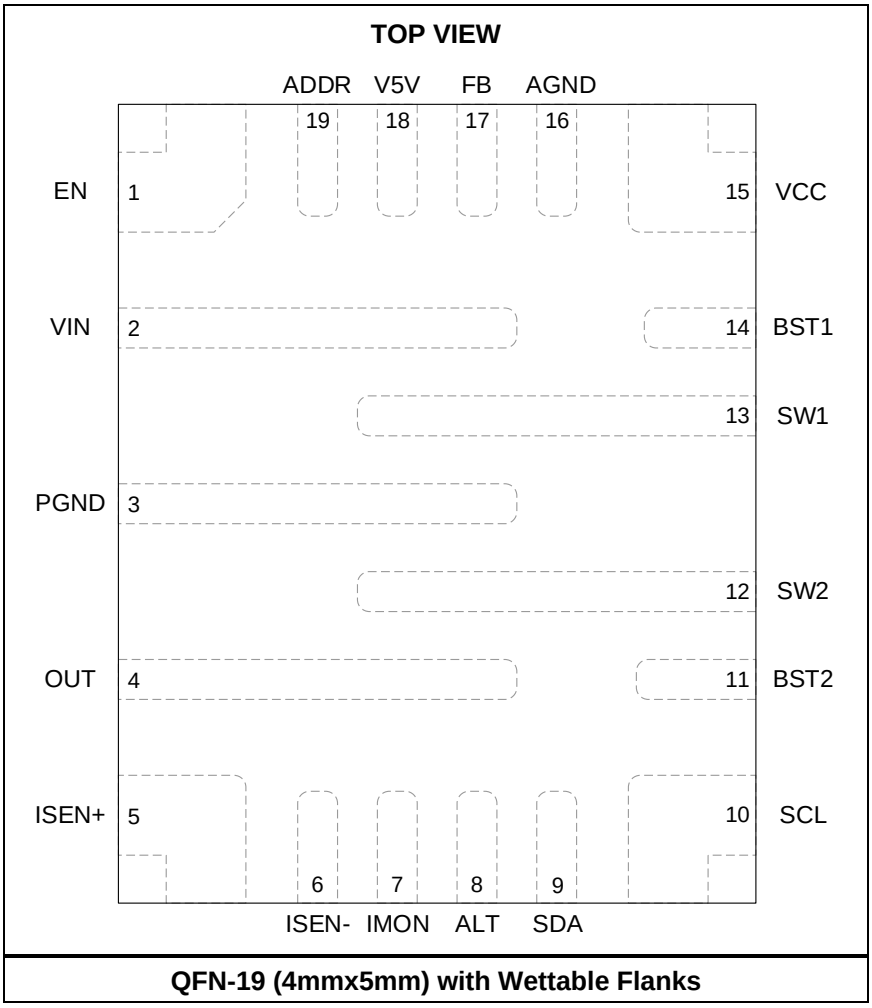
PACKAGE REFERENCE



QFN-19 (4mmx5mm) with Wettable Flanks

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PIN FUNCTIONS

Pin #	Name	Description
1	EN	**Enable input.** Apply logic high on the EN pin to enable the chip.
2	VIN	**Power supply voltage.** The MPQ4232A operates from a 3V to 36V input voltage (V_{IN}). The VIN pin is the drain of the first half-bridge's internal power device. The input capacitor (C_{IN}) is required to prevent large voltage spikes at the input. Place C_{IN} as close to the IC as possible.
3	PGND	**Power ground.** The PGND pin requires additional care during the PCB layout. Connect the PGND pin to ground using copper traces and vias.
4	OUT	**Buck-boost output.** The OUT pin is the drain of switch D (SWD). The output capacitor (C_{OUT}) prevents large voltage spikes at the output. Place C_{OUT} as close to the IC as possible.
5	ISEN+	**Positive node of the current-sense input.** The ISEN+ pin can be used for the output current (I_{OUT}) or input current (I_{IN}) limit.
6	ISEN-	**Negative node of the current-sense input**. The ISEN- pin can be used for the I_{OUT} or I_{IN} limit.
7	IMON	**Output current monitor.** The IMON pin outputs a voltage signal, which is proportional to I_{OUT}.
8	ALT	**I²C alert.** The ALT pin is an open-drain output that is pulled low to indicate the unmasked STATUS register bits.
9	SDA	**I²C data line.**
10	SCL	**I²C clock signal input.**
11	BST2	**Bootstrap.** A 0.22µF capacitor (C_{BST2}) is connected between the SW2 and BST2 pins to form a floating supply across the high-side MOSFET (HS-FET) driver.
12	SW2	**Buck-boost switch 2 node.** Connect the SW2 pin to SW1 via a power inductor using a wide PCB trace.
13	SW1	**Buck-boost switch 1 node.** Connect the SW1 pin to SW2 via a power inductor using a wide PCB trace.
14	BST1	**Bootstrap.** A 0.22µF capacitor (C_{BST1}) is connected between the SW1 and BST1 pins to form a floating supply across the HS-FET driver.
15	VCC	**Internal 3.54V low-dropout (LDO) regulator output.** Decouple the VCC pin using a 1µF capacitor.
16	AGND	**Analog ground.** Connect the AGND pin to PGND and the ground node of the VCC capacitor (C_{VCC}).
17	FB	**Feedback.** Connect the FB pin to an external resistor divider's tap from the output to AGND to set the output voltage (V_{OUT}).
18	V5V	**5V LDO output.** Bypass the V5V pin using a 1µF capacitor. V5V can supply a 60mA I_{OUT}. The 5V LDO turns on once V_{IN} and the EN pin voltage (V_{EN}) exceed their under-voltage lockout (UVLO) thresholds (V_{IN_UVLO} and $V_{EN_RISING1}$, respectively); it turns off when the VCC voltage (V_{CC}) falls below its UVLO threshold (V_{CC_UVLO}), meaning EN is pulled low, or V_{IN} is below 2.4V (typically). The status of the OPERATION bit (01h, bit[7]) has no effect on V5V.
19	ADDR	**Multi-function pin.** The ADDR pin can set the I²C target address and default state of the OPERATION bit. The status of ADDR is latched once V_{IN} and V_{EN} exceed V_{IN_UVLO} and $V_{EN_RISING1}$, respectively. ADDR only resets when V_{CC} is below V_{CC_UVLO}. This pin cannot be floated.

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ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}) .....-0.3V to +40V
V_{OUT}, V_{ISEN+}, V_{ISEN-} .....
.....-0.3V to +26V (+28V for <10ns)
V_{SW1}.....
-0.3V (-5V for <10ns) to +40V (+43V for <10ns)
V_{SW2}.....
-0.3V (-5V for <10ns) to +25V (+29V for <10ns)
V_{BST1}, V_{BST2}..... V_{SW1}, V_{SW2} + 4V
V_{EN}.....-0.3V to +40V
V_{5V}.....-0.3V to +5.5V
V_{SCL}, V_{SDA}, V_{ALT} .....-0.3V to +6.5V
All other pins .....-0.3V to +4V
Continuous power dissipation (T_A = 25°C) (2)
QFN-19 (4mmx5mm)..... 5.3W
Junction temperature (T_J) .....150°C
Lead temperature .....260°C
Storage temperature..... -65°C to +150°C

ESD Ratings (3)

Human body model (HBM) (4)..... ±2kV
Charged-device model (CDM) ..... ±750V

Recommended Operating Conditions (5)

Operating input voltage (V_{IN}) range .....
.....3V to 36V
Operating output voltage (V_{OUT}) range.....
.....1V to 24V
Output current (I_{OUT})..... 6A
V5V low-dropout (LDO) output 5V/60mA
Operating junction temp (T_J).... -40°C to +150°C

Thermal Resistance θ_{JA} θ_{JB}

QFN-19 (4mm x 5mm)
JESD51-7 (7) .....37.2.....2.8.....°C/W
EVQ4232A-VE-00A (6).....23.6.....°C/W

	θ_{JC_TOP}	θ_{JC_BOT}
JESD51-7 (7)	25.9	0.9 °C/W

	Ψ_{JT}	Ψ_{JB}
JESD51-7 (7)	1.6	3.3 °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can produce an excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) HBM, per JEDEC specification JESD22-A114; CDM, per JEDEC specification JESD22-C101, AEC specification AECQ100-011. JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process. JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.
4) HBM with regards to ground.
5) The device is not guaranteed to function outside of its operating conditions.
6) Measured on the EVQ4232A-VE-00A.
7) Measured on a JESD51-7, 4-layer PCB. The θ_{JA} value given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7 and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, V_{EN} = 5V, T_J = -40°C to +150°C, typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Shutdown supply current	I_{Q_STD}	V_{EN} = 0V			10	μA
Quiescent supply current	I_{Q1}	No switching, I²C-configured OPERATION (01h), bit[7] enabled, EN enabled, automatic pulse-frequency modulation (PFM) or pulse-width modulation (PWM) mode		900		μA
	I_{Q2}	I²C-configured OPERATION disabled, EN enabled		130		μA
Enable (EN) rising threshold1	$V_{EN_RISING1}$	EN enables VCC and V5V		0.57		V
EN hysteresis 1	V_{EN_HYS1}			30		mV
EN rising threshold 2	$V_{EN_RISING2}$	EN enables switching	1	1.1	1.2	V
EN hysteresis 2	V_{EN_HYS2}			120		mV
EN pull-down resistance	R_{EN}	EN = 2V		1.25		MΩ
Thermal shutdown (8)	T_{STD}			165		°C
Thermal warning (8)	T_{OTW}			135		°C
Thermal hysteresis (8)	T_{STD_HYS}			20		°C
V5V low-dropout (LDO) regulator	V_{5V}		-5%	5	+5%	V
V5V load regulation	V_{5V_LOG}	I_{CC} = 0mA to 60mA		2	5	%
VCC LDO regulator	V_{CC}		-5%	3.54	+5%	V
VCC load regulation	V_{CC_LOG}	I_{CC} = 20mA		2	5	%
V_{CC} under-voltage lockout (UVLO) rising threshold	$V_{CC_UVLO_R}$		2.4	2.55	2.7	V
V_{CC} UVLO threshold hysteresis	$V_{CC_UVLO_HYS}$			260		mV
Input voltage (V_{IN}) UVLO rising threshold	$V_{IN_UVLO_R}$	Trim option (2.8 version)		2.8		V
V_{IN} UVLO hysteresis	$V_{IN_UVLO_HYS}$			100		mV
V_{IN} UVLO rising threshold	$V_{IN_UVLO_R}$	Default trim	3.58	3.73	3.88	V
V_{IN} UVLO hysteresis	$V_{IN_UVLO_HYS}$			300		mV
V_{IN} UVLO rising threshold	$V_{IN_UVLO_R}$	Trim option (4.24 version)	4.04	4.24	4.44	V
V_{IN} UVLO hysteresis	$V_{IN_UVLO_HYS}$			400		mV
Buck-Boost Converter						
MOSFET A (SWA) on resistance	$R_{DS(ON)_A}$			12		mΩ
MOSFET B (SWB) on resistance	$R_{DS(ON)_B}$			16		mΩ
MOSFET C (SWC) on resistance	$R_{DS(ON)_C}$			7		mΩ
MOSFET D (SWD) on resistance	$R_{DS(ON)_D}$			7		mΩ

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{EN} = 5V, T_J = -40°C to +150°C, typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Feedback voltage	V_{FB1}		-3%	0.33	+3%	V
	V_{FB2}		-2.5%	0.5	+2.5%	V
	V_{FB3}		-2.5%	2	+2.5%	V
Output over-voltage protection (OVP) rising threshold	$V_{FB_OVP_R}$		113	118	123	% of V_{FB}
Output OVP falling threshold	$V_{FB_OVP_F}$		102	107	112	% of V_{FB}
Input OVP rising threshold	$V_{IN_OVP_R}$		36.6	38.6		V
Input OVP hysteresis	$V_{IN_OVP_HYS}$			2.6		V
Switch leakage	SW_{LKG}	V_{EN} = 0V, V_{SW1} = 36V, V_{SW2} = 24V, T_J = 25°C			1	µA
		V_{EN} = 0V, V_{SW1} = 36V, V_{SW2} = 24V, T_J = -40°C to +150°C			30	µA
Hiccup off-timer	t_{HICCUP}		470	570	670	ms
Switching frequency	f_{SW1}		-20%	280	+20%	kHz
	f_{SW2}		-20%	400	+20%	kHz
	f_{SW3}		-20%	530	+20%	kHz
Frequency dithering span	f_{SW_RANGE}	2kHz triangle modulation, f_{SW} = 400kHz, buck or boost		±7		%
Soft-start time	t_{SS}	Output from 10% to 90%, V_{REF} = 0.5V, constant slew rate for other V_{REF} values		1		ms
Minimum on time (8)	$t_{ON_MIN_BT}$			180		ns
Minimum off time (8)	t_{OFF_MIN}			180		ns
ISEN+- threshold (8)	I_{OC1}	OC threshold = 1A, R_{SENS} = 5mΩ, T_J = -40°C to +85°C	4.25	5	5.75	mV
	I_{OC2}	OC threshold = 3.6A, R_{SENS} = 5mΩ, T_J = -40°C to +85°C	-5%	18	+5%	mV
IMON gain	G_{IMON3A}	T_J = 25°C, I_{OUT} = 3A, R_{SENS} = 5mΩ	-5%	246	+5%	mV/A
Low-side (LS) SWB valley current limit	I_{LIMIT2}	D3h, bits[7:6] = 01b	6.5	8.7	11.7	A
LS SWC peak current limit	I_{LIMIT3}	D3h, bits[7:6] = 01b	8.2	12	17.4	A
Line drop compensation	V_{DROP}	I_{OUT} = 3A	-20%	300	+20%	mV
Output discharge resistance	R_{DISCHG}	T_J = 25°C	45	75	120	Ω
Mode Transition Threshold						
Buck-boost to buck transition threshold	V_{MODE_TH1}	V_{IN} / V_{OUT}		120		%
Buck-boost to boost transition threshold	V_{MODE_TH2}	V_{IN} / V_{OUT}		82		%
ALT pin leakage	I_{ALT_LKG}	V_{ALT} = 5V			1	µA
ALT pin pull-down resistance	R_{ALT}				50	Ω

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{EN} = 5V, T_J = -40°C to +150°C, typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
I²C Interface Specification (8)						
ADDR setting threshold 1	V_{ADDR1}	Set I²C address 67h, EN disabled			0.2	V_{CC}
ADDR setting threshold 2	V_{ADDR2}	Set I²C address 47h, EN disabled	0.29		0.45	V_{CC}
ADDR setting threshold 3	V_{ADDR3}	Set I²C address 27h, EN enabled	0.57		0.67	V_{CC}
ADDR setting threshold 4	A_{DDR4}	Set I²C address 07h, EN enabled	0.76			V_{CC}
Input logic high	V_{IH}		1.4			V
Input logic low	V_{IL}				0.6	V
Output voltage logic low	V_{OUT_L}	Sink 10µA current			0.4	V
SCL clock frequency	f_{SCL}			400	1000	kHz
SCL high time	t_{HIGH}		60			ns
SCL low time	t_{LOW}		160			ns
Data set-up time	t_{SU_DAT}		10			ns
Data hold time	t_{HD_DAT}		0	60		ns
Set-up time for (repeated) start command	t_{SU_STA}		160			ns
Hold time for (repeated) start command	t_{HD_STA}		160			ns
Bus free time between a start and stop command	t_{BUF}		160			ns
Set-up time for stop command	t_{SU_STO}		160			ns
SCL and SDA rising time	t_R		10		300	ns
SCL and SDA falling time	t_F		10		300	ns
Suppressed spike pulse width	t_{SP}		0		50	ns
Capacitance for each bus line	C_B				400	pF
Power Good (PG) Indication						
PG lower rising threshold	$V_{PG_R_L}$	PG switches high	86.5	91	96.5	% of V_{FB}
PG lower falling threshold	$V_{PG_F_L}$	PG switches low	75	80.5	86	% of V_{FB}
PG upper rising threshold	$V_{PG_R_H}$	PG switches low	113	118	123	% of V_{FB}
PG upper falling threshold	$V_{PG_F_H}$	PG switches high	102	107	112	% of V_{FB}

Note:

8) Guaranteed by characterization sample testing.

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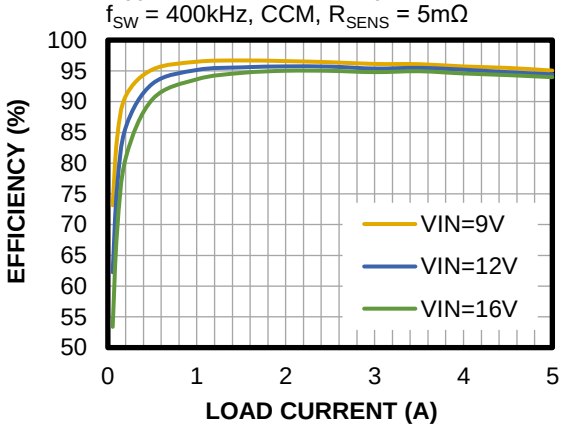
TYPICAL CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, f_{SW} = 400kHz, FPWM mode, T_A = 25°C, unless otherwise noted.

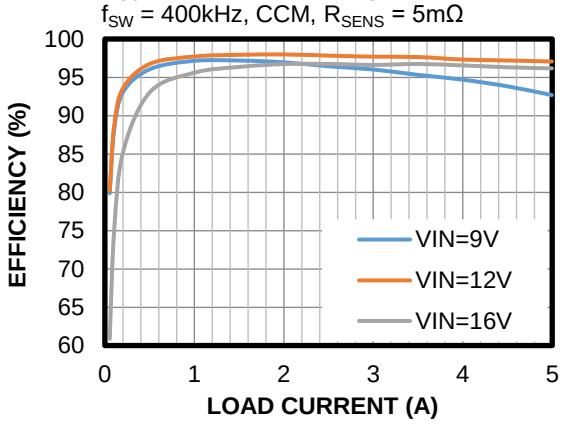
Efficiency vs. Load Current

V_{OUT} = 5V, L = 4.7µH, R_{DC} = 8mΩ, f_{SW} = 400kHz, CCM, R_{SENS} = 5mΩ



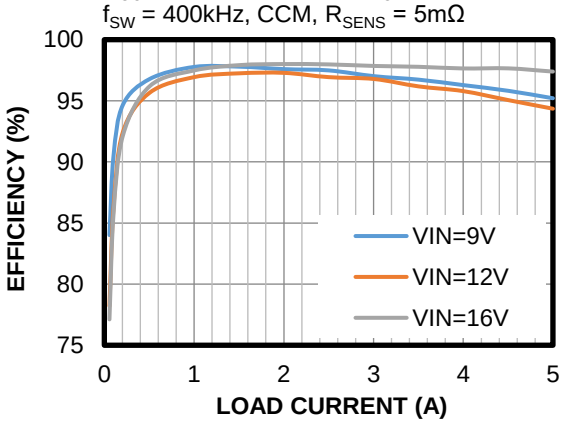
Efficiency vs. Load Current

V_{OUT} = 9V, L = 4.7µH, R_{DC} = 8mΩ, f_{SW} = 400kHz, CCM, R_{SENS} = 5mΩ



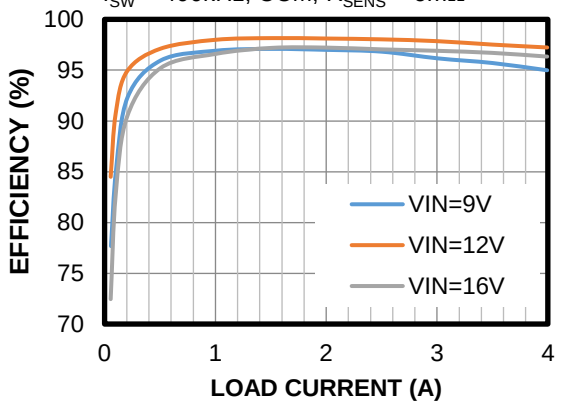
Efficiency vs. Load Current

V_{OUT} = 12V, L = 4.7µH, R_{DC} = 8mΩ, f_{SW} = 400kHz, CCM, R_{SENS} = 5mΩ



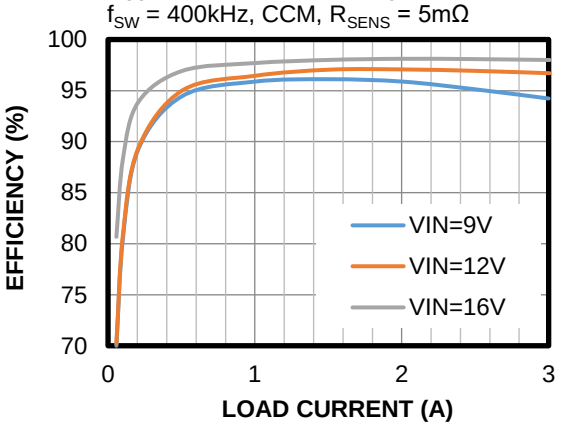
Efficiency vs. Load Current

V_{OUT} = 15V, L = 4.7µH, R_{DC} = 8mΩ, f_{SW} = 400kHz, CCM, R_{SENS} = 5mΩ



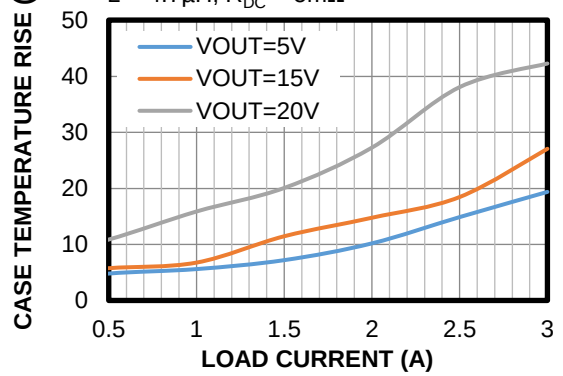
Efficiency vs. Load Current

V_{OUT} = 20V, L = 4.7µH, R_{DC} = 8mΩ, f_{SW} = 400kHz, CCM, R_{SENS} = 5mΩ



Case Temperature Rise vs. Load Current

V_{IN} = 12V, V_{OUT} = 5V/12V/20V, f_{SW} = 400kHz, based on 5cmx5cm board, L = 4.7µH, R_{DC} = 8mΩ



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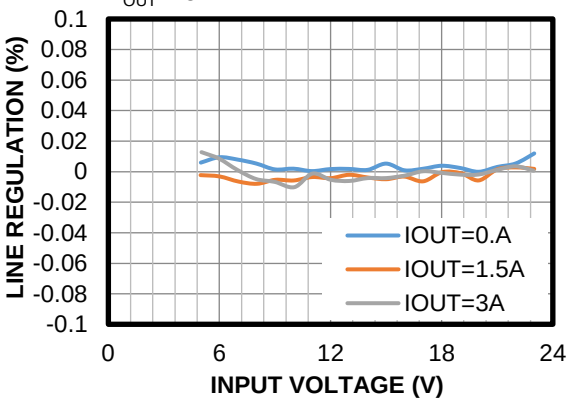
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, f_{SW} = 400kHz, FPWM mode, T_A = 25°C, unless otherwise noted.

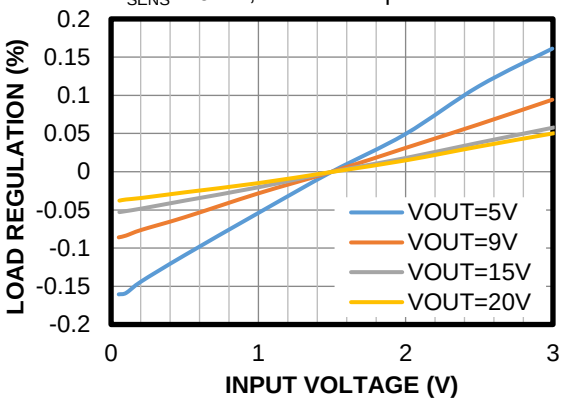
Line Regulation

V_{OUT} = 5V

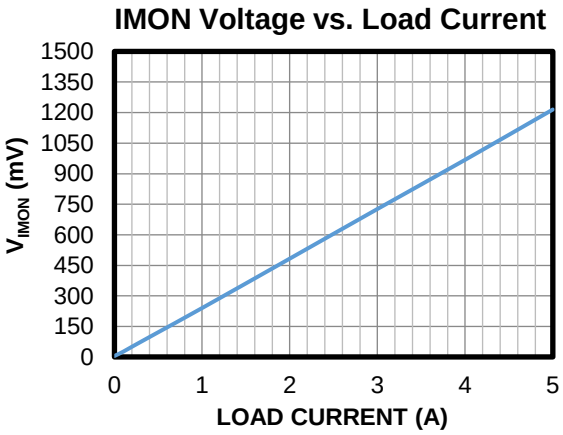


Load Regulation

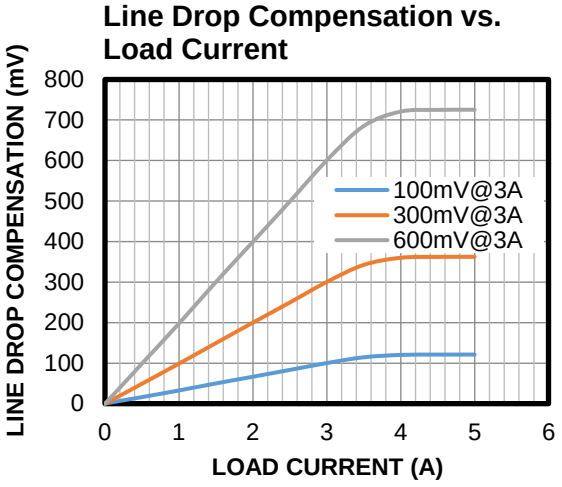
R_{SENS} = 5mΩ, no line compensation



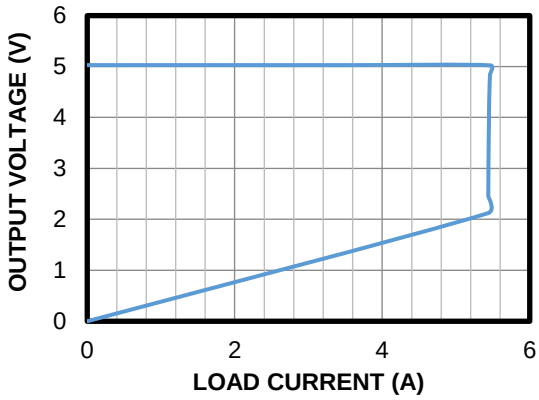
IMON Voltage vs. Load Current



Line Drop Compensation vs. Load Current

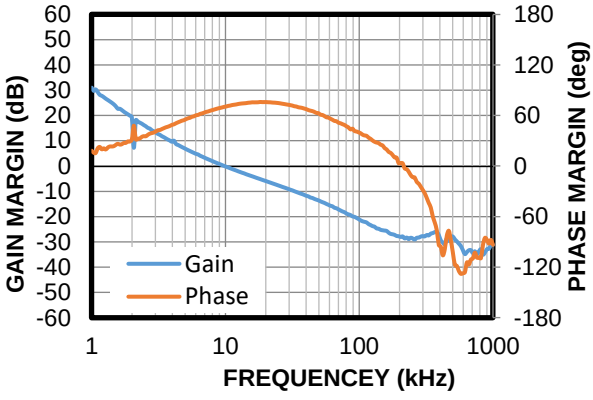


CC/CV Curve



Bode Plot

V_{OUT} = 5V, I_{OUT} = 3A, BW = 10kHz, PM = 70°



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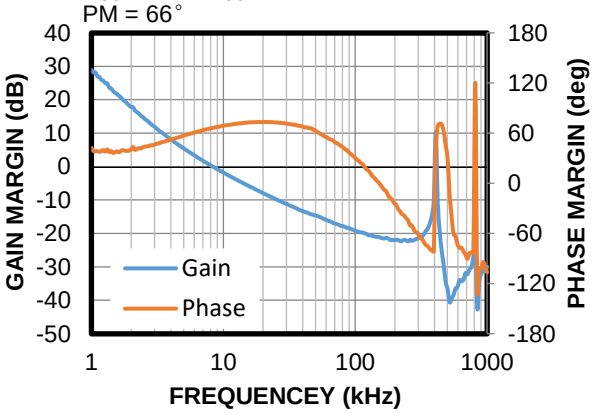
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, f_{SW} = 400kHz, FPWM mode, T_A = 25°C, unless otherwise noted.

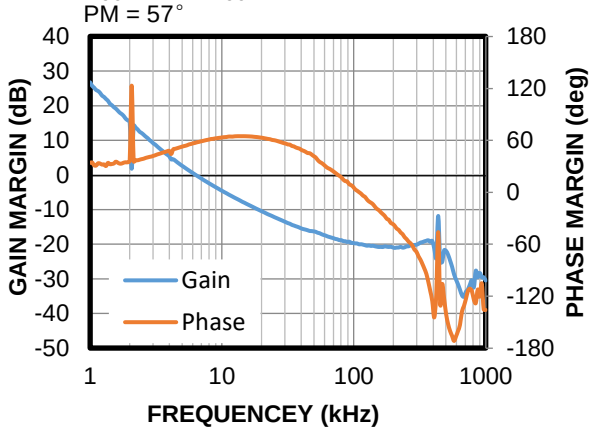
Bode Plot

V_{OUT} = 12V, I_{OUT} = 3A, BW = 8kHz,
PM = 66°



Bode Plot

V_{OUT} = 20V, I_{OUT} = 3A, BW = 6kHz,
PM = 57°



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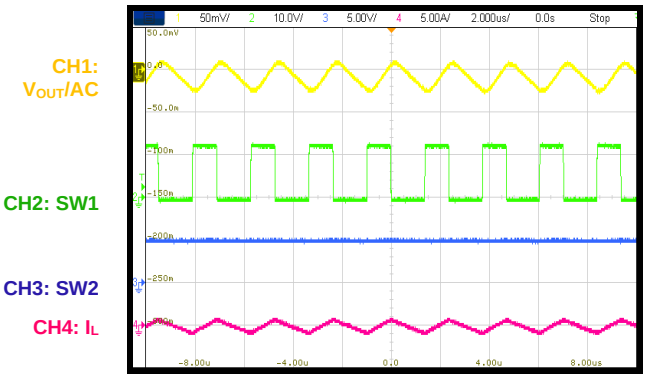
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, f_{SW} = 400kHz, FPWM mode, T_A = 25°C, unless otherwise noted.

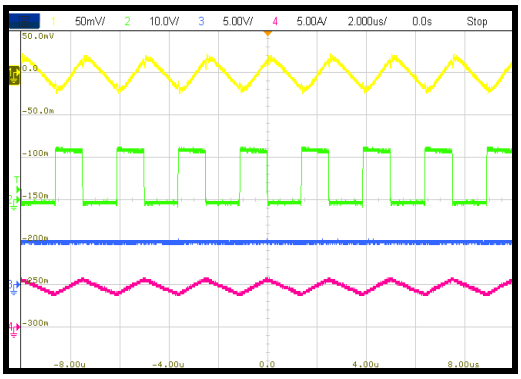
Output Voltage Ripple

V_{OUT} = 5V, load = 0A



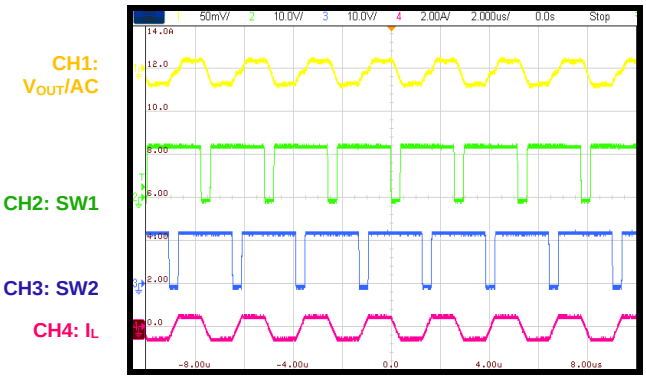
Output Voltage Ripple

V_{OUT} = 5V, load = 5A



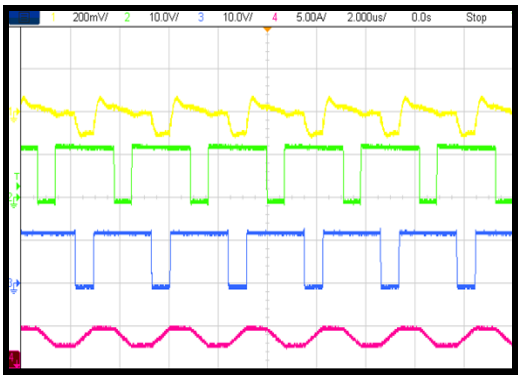
Output Voltage Ripple

V_{OUT} = 12V, load = 0A



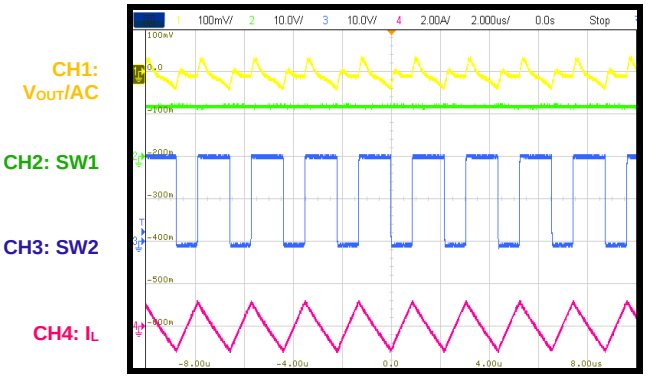
Output Voltage Ripple

V_{OUT} = 12V, load = 3A



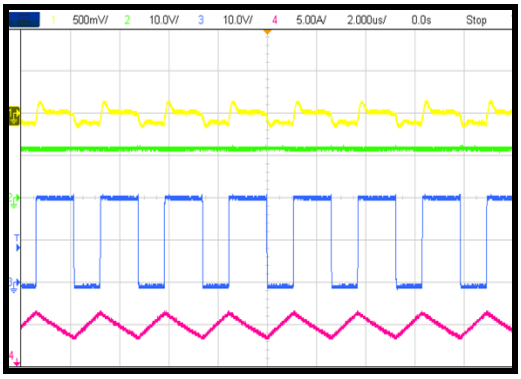
Output Voltage Ripple

V_{OUT} = 20V, load = 0A



Output Voltage Ripple

V_{OUT} = 20V, load = 3A



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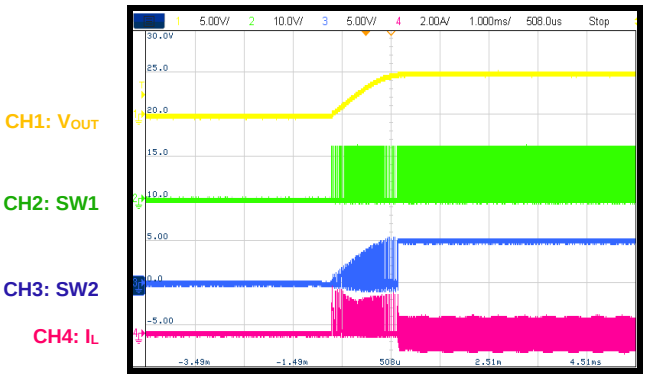
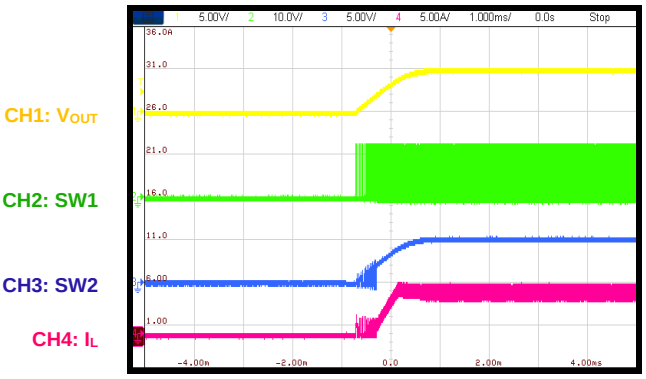
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, f_{SW} = 400kHz, FPWM mode, T_A = 25°C, unless otherwise noted.

I²C Operation Enabled
Load = 0A



I²C Operation Enabled
Load = 5A



I²C Operation Disabled
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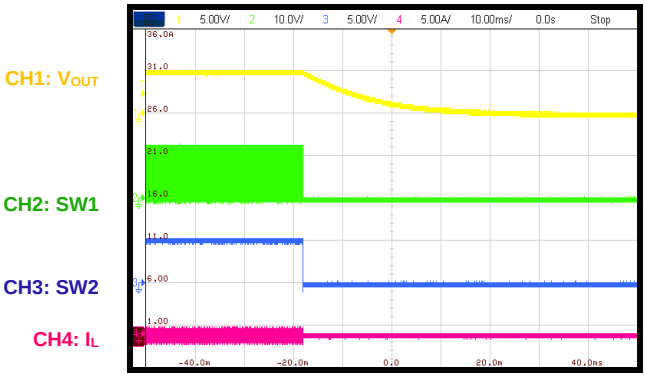
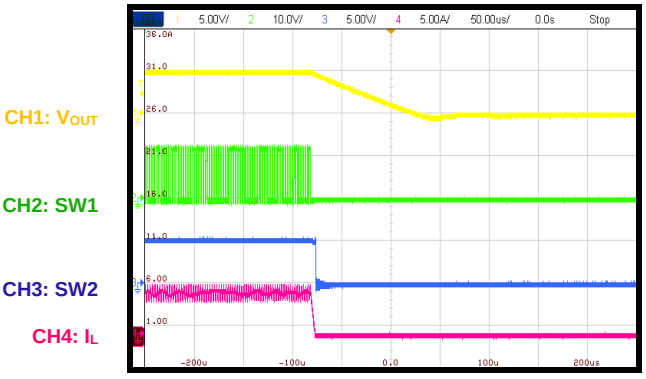
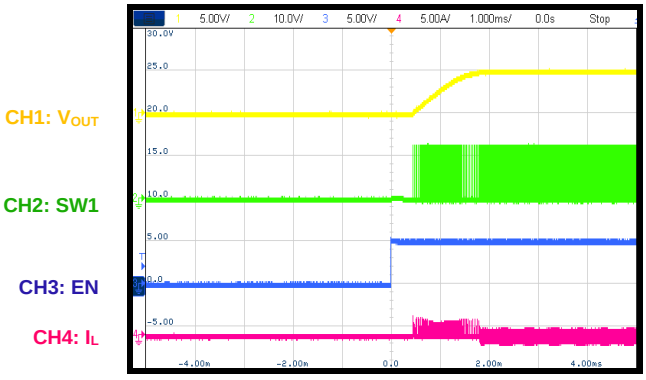


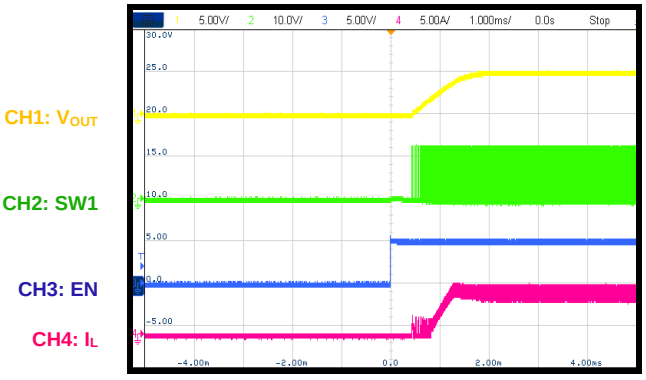
I²C Operation Disabled
Load = 5A



Start-Up through EN
Load = 0A



Start-Up through EN
Load = 5A



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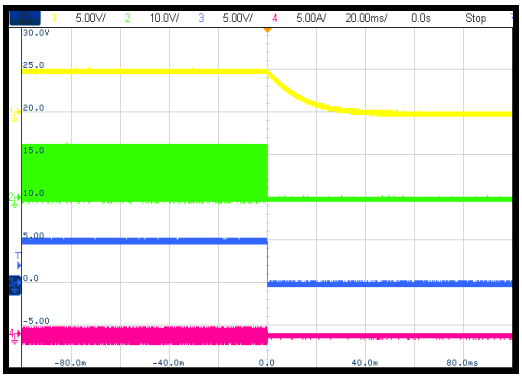
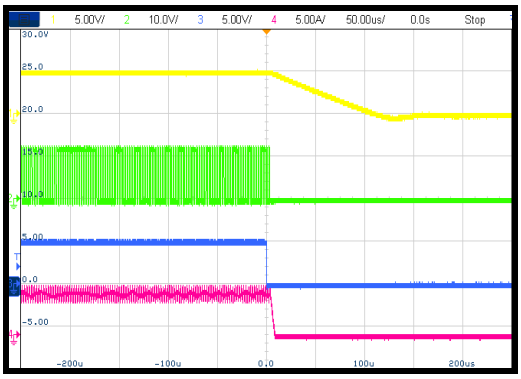
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, f_{SW} = 400kHz, FPWM mode, T_A = 25°C, unless otherwise noted.

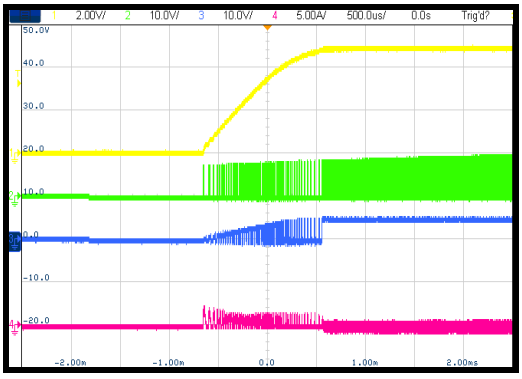
Shutdown through EN
Load = 0A



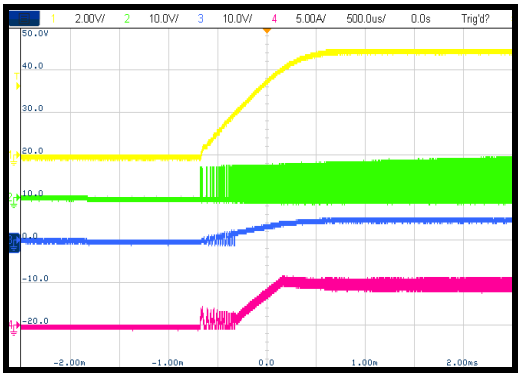
Shutdown through EN
Load = 5A



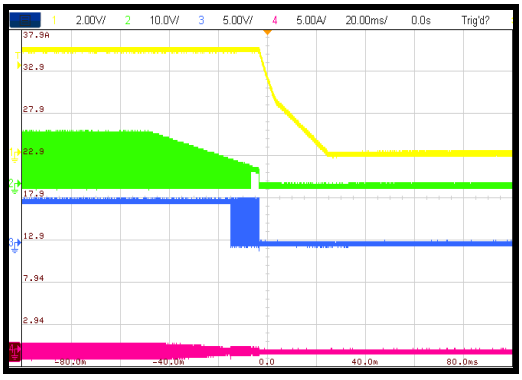
Start-Up through VIN
Load = 0A



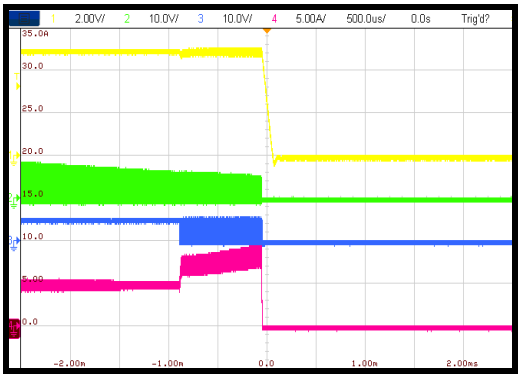
Start-Up through VIN
Load = 5A



Shutdown through VIN
Load = 10mA, EN divider ratio = 1:5



Shutdown through VIN
Load = 5A, EN divider ratio = 1:5



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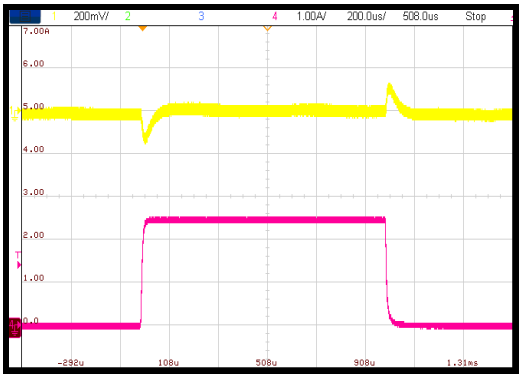
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, f_{SW} = 400kHz, FPWM mode, T_A = 25°C, unless otherwise noted.

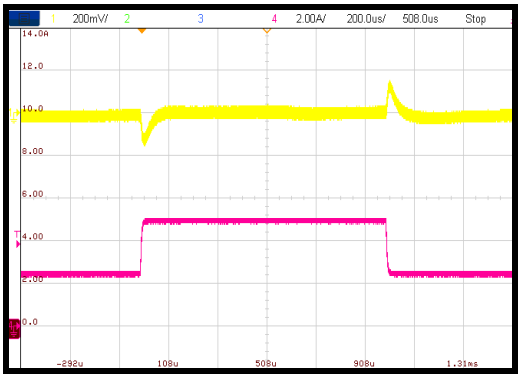
Load Transient Response

V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 0A to 2.5A, 150mA/µs



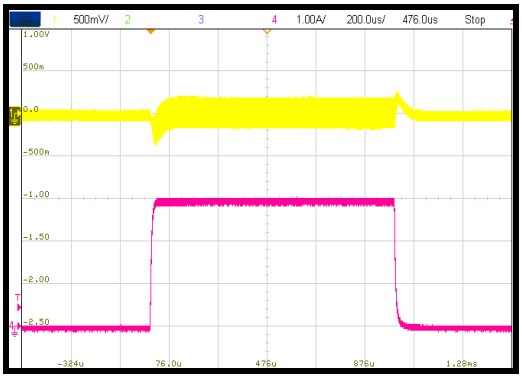
Load Transient Response

V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 2.5A to 5A, 150mA/µs



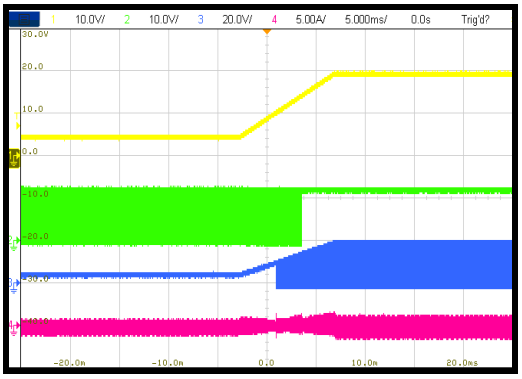
Load Transient Response

V_{IN} = 12V, V_{OUT} = 20V, I_{OUT} = 0A to 3A, 150mA/µs



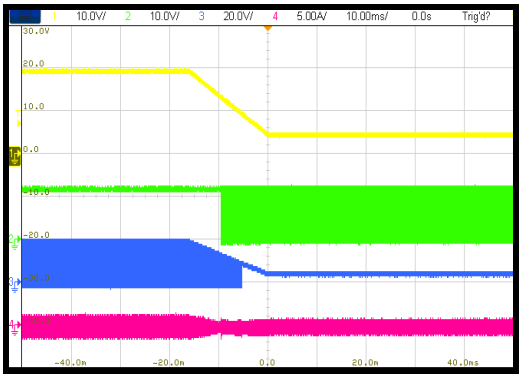
Output Voltage Transition

V_{OUT} = 5V to 20V, I_{OUT} = 0A



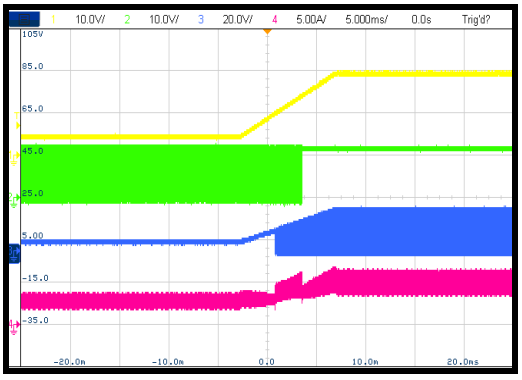
Output Voltage Transition

V_{OUT} = 20V to 5V, I_{OUT} = 0A



Output Voltage Transition

V_{OUT} = 5V to 20V, I_{OUT} = 3A



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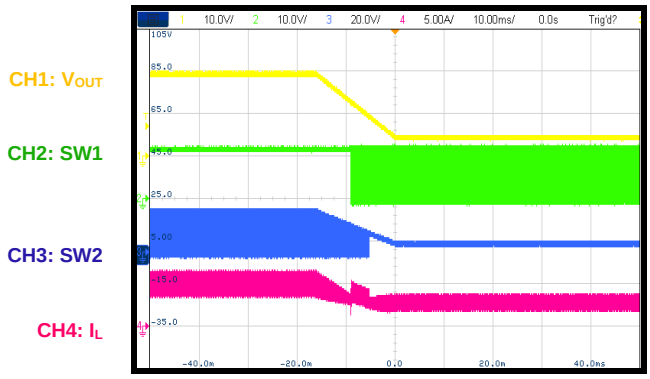
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, f_{SW} = 400kHz, FPWM mode, T_A = 25°C, unless otherwise noted.

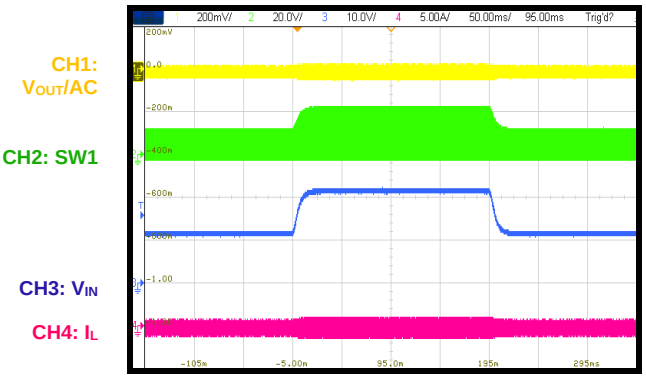
Output Voltage Transition

V_{OUT} = 20V to 5V, I_{OUT} = 3A



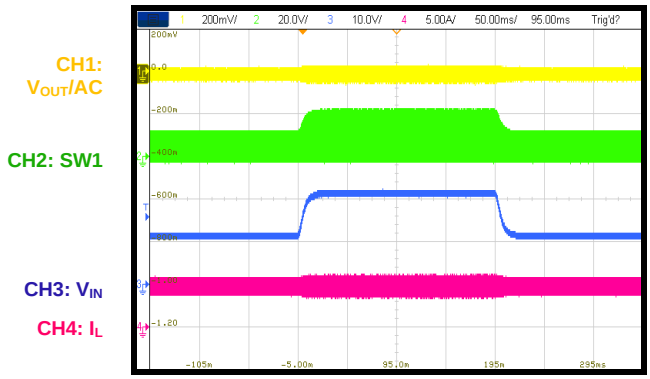
Input Voltage Transient Response

V_{IN} = 12V to 22V, V_{OUT} = 5V, load = 0A



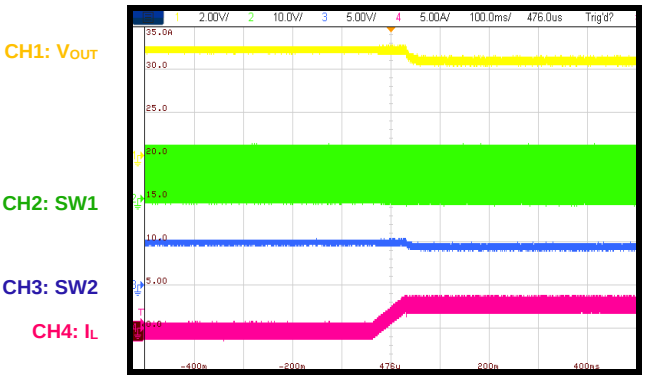
Input Voltage Transient Response

V_{IN} = 12V to 22V, V_{OUT} = 5V, load = 5A

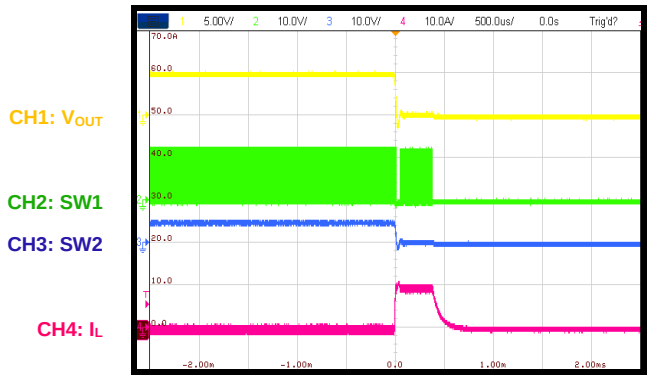


Constant-Current Entry

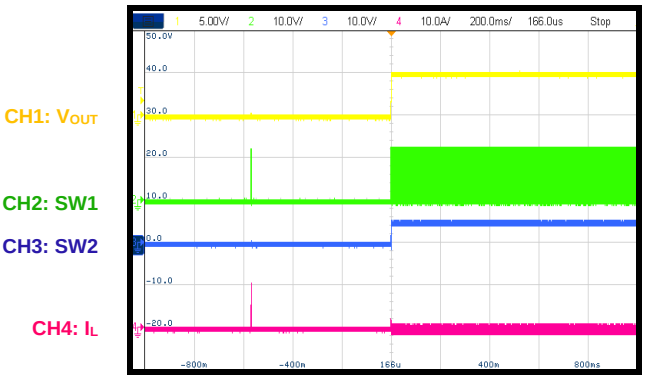
CV load = 4.5V, CC limit = 3A



Short-Circuit Protection Entry



Short-Circuit Protection Recovery



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FUNCTIONAL BLOCK DIAGRAM

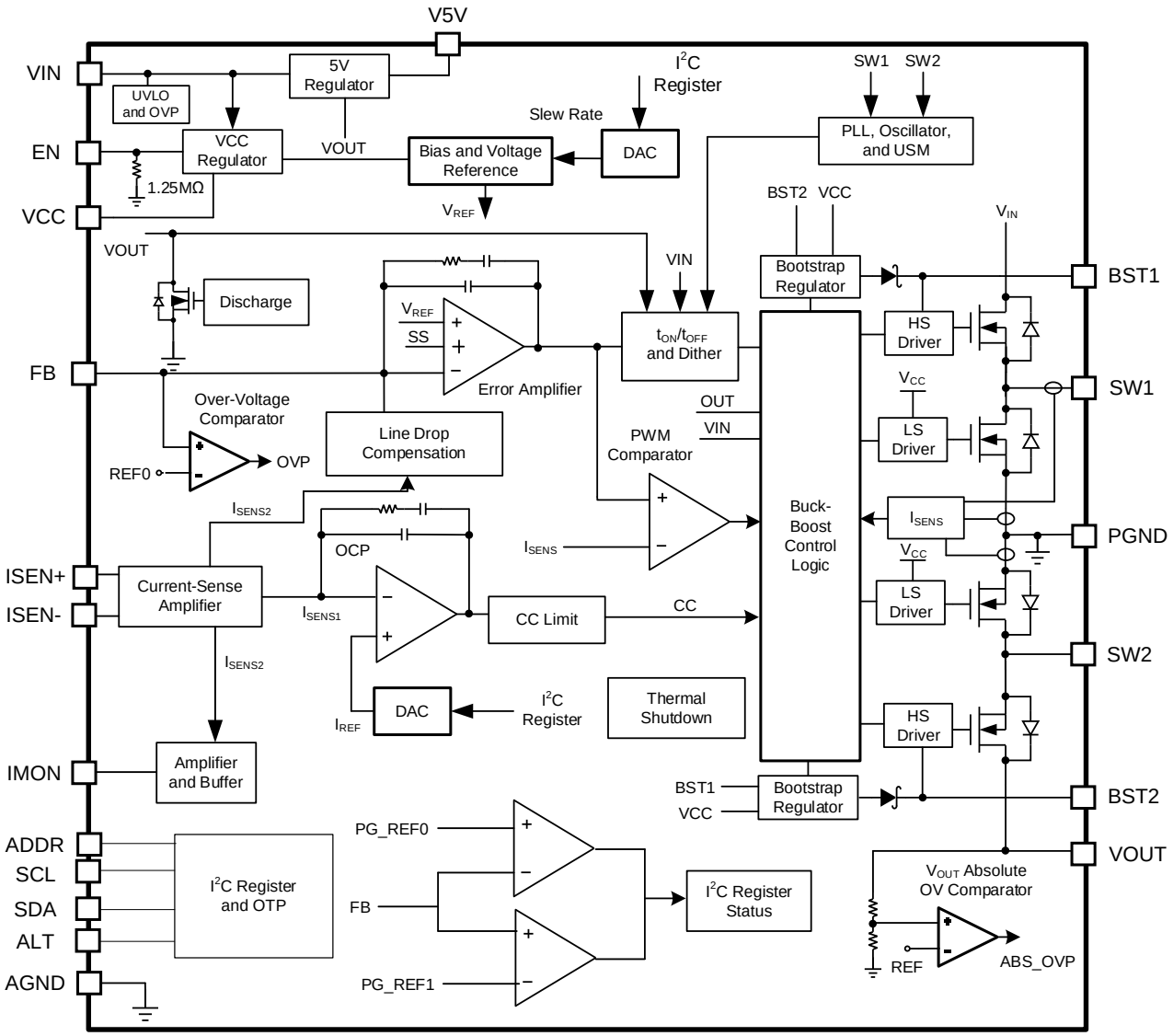

Figure 2: Functional Block Diagram

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OPERATION

The MPQ4232A is a buck-boost converter with four integrated MOSFETs. The device works with a fixed frequency for buck, boost, and buck-boost modes. A special buck-boost control strategy provides high efficiency across the full input voltage (V_{IN}) range and smooths transients between different modes. Figure 2 on page 18 shows the functional block diagram, and the sections below describe the MPQ4232A's functions.

Buck-Boost Operation

The MPQ4232A can regulate the output voltage (V_{OUT}) to be above, equal to, or below V_{IN}. Figure 3 shows a buck-boost power structure with one inductor and four MOSFET switches (SWA, SWB, SWC, and SWD).

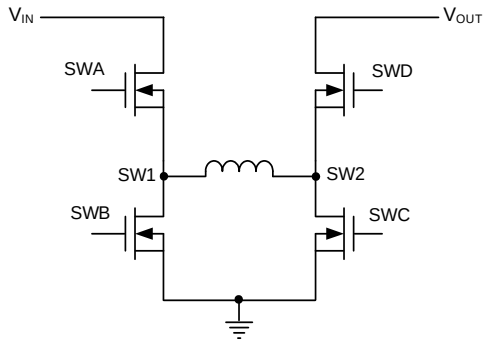

Figure 3: Buck-Boost Topology

The MPQ4232A can operate in buck mode, boost mode, or buck-boost mode with different V_{IN} inputs (see Figure 4).

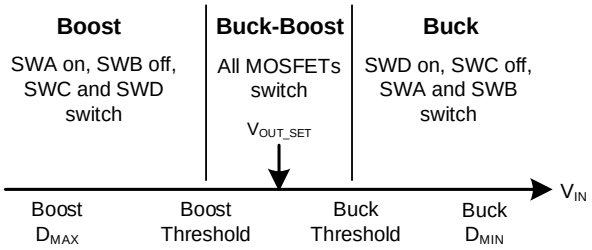

Figure 4: Buck-Boost Operating Range

Buck Mode (V_{IN} > V_{OUT})

If V_{IN} significantly exceeds V_{OUT}, the MPQ4232A works in buck mode. In this mode, switch A (SWA) and switch B (SWB) switch for buck regulation, switch C (SWC) is off, and switch D (SWD) remains on to conduct the inductor current (I_L).

In each cycle of buck mode, SWA turns on first once the FB voltage (V_{FB}) drops below the reference voltage (V_{REF}). After SWA turns off, SWB turns on to conduct I_L until the COMP control signal is triggered. By repeating this operation, the converter regulates V_{OUT}.

Boost Mode (V_{IN} < V_{OUT})

If V_{IN} drops significantly below V_{OUT}, the MPQ4232A works in boost mode. In this mode, SWC and SWD switch for boost regulation, SWB is off, and SWA remains on to conduct I_L.

In each cycle of boost mode, SWC turns on to conduct I_L. If I_L rises and triggers the control signal, then SWC turns off and SWD turns on for the freewheeling current. Then SWC turns on and off repeatedly to regulate V_{OUT} in boost mode.

Buck-Boost Mode (V_{IN} ≈ V_{OUT})

If V_{IN} is close to V_{OUT}, the converter cannot provide sufficient energy to the load in buck mode due to SWA's minimum off time (t_{OFF_MIN}). In boost mode, the converter supplies too much power to the load due to SWC's minimum on time (t_{ON_MIN}). Under these conditions, the MPQ4232A adopts buck-boost control to regulate V_{OUT} (see Figure 5).

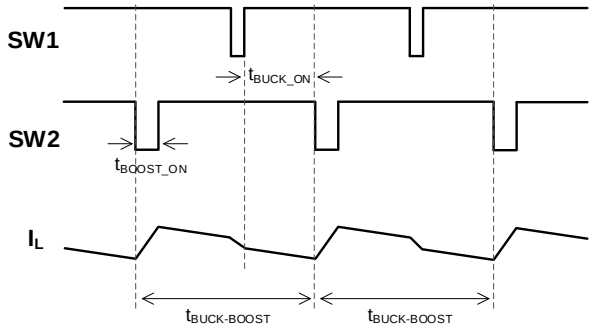

Figure 5: Buck-Boost Waveform

If V_{IN} is close to V_{OUT}, the MPQ4232A enters buck-boost mode, and a boost switching period is inserted into each buck switching period. The MOSFETs switch in the following sequence:

1. SWA and SWC
2. SWA and SWD
3. SWB and SWD
4. SWA and SWD

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Throughout this process, I_L can meet the COMP voltage (V_{COMP}) requirement and supply sufficient current to the output.

VCC Power Supply

The MPQ4232A's internal circuit is powered by VCC, including the gate drivers. When VIN power is supplied and EN is high (V_{IN} > 3.73V and V_{EN} > 0.57V), the MPQ4232A attempts to regulate the VCC voltage (V_{CC}) at 3.54V. VCC is only supplied by V_{IN}. VCC and BST1/BST2 have separate under-voltage lockout (UVLO) thresholds that keep the gate signal off.

Enable (EN) Control

The MPQ4232A provides a high-voltage EN pin that can be connected to VIN via a resistor. The V_{IN} on and off thresholds can be set by configuring the EN resistor divider (see Figure 6).

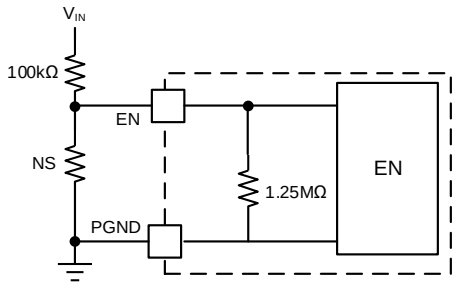

Figure 6: EN Connection

The EN pin has two thresholds. If the EN voltage (V_{EN}) exceeds 0.57V, then VCC and V5V start working. If V_{EN} exceeds 1.1V, then switching is enabled (see Figure 7).

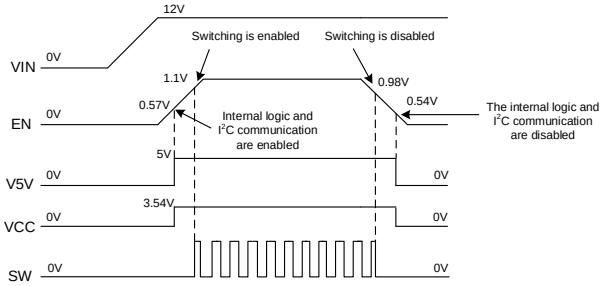

Figure 7: EN On/Off Sequence

Under-Voltage Lockout (UVLO)

UVLO protects the chip from operating at an insufficient supply voltage. The UVLO comparator monitors V_{IN} and V_{CC}. The MPQ4232A is enabled when V_{IN} and V_{CC} exceed their UVLO rising thresholds ($V_{IN_UVLO_R}$ and $V_{CC_UVLO_R}$, respectively); when V_{IN} triggers the UVLO falling threshold, the IC stops switching and starts V_{OUT} discharge until V_{CC} drops below its UVLO threshold (V_{CC_UVLO}). Then the entire IC is disabled.

Internal Soft Start (SS)

Soft start (SS) prevents the converter's V_{OUT} from overshooting during start-up. When the chip starts up, the internal circuitry generates an SS voltage (V_{SS}) that ramps up from 0V to V_{CC}. If V_{SS} is below V_{REF}, the error amplifier (EA) uses V_{SS} as the reference. If V_{SS} exceeds V_{REF}, the EA uses V_{REF} as the reference. The MPQ4232A fixes the SS time (t_{SS}) at 1ms when V_{REF} is set to 0.5V.

If the MPQ4232A's output is pre-biased to a set voltage during start-up, then the IC disables switching for both the high-side MOSFET (HS-FET) and low-side MOSFET (LS-FET) until the voltage on the internal SS capacitor (C_{SS}) exceeds the internal V_{FB}.

Constant-Current Limit Mode (CC Mode) and Over-Current Protection (OCP)

The MPQ4232A senses the output current (I_{OUT}) or input current (I_{IN}) via the ISEN+ and ISEN- pins. If I_{OUT} or I_{IN} exceed the set current-limit threshold, then the MPQ4232A enters constant-current limit mode (CC mode). In this mode, the current amplitude is limited. Once I_{OUT} or I_{IN} reaches the current-limit threshold, V_{OUT} drops as the load resistance decreases until V_{FB} falls below the under voltage (UV) threshold (typically 40% of V_{REF}). Once the UV threshold is triggered and V_{OUT} is below 2.97V, the MPQ4232A enters hiccup mode to periodically restart the part. This protection mode is especially useful when the output terminal is dead-shorted to ground. As a result, the average short-circuit current is reduced significantly, which alleviates thermal issues and protects the regulator. The MPQ4232A exits hiccup mode once the over-current (OC) condition is removed.

Select CC mode on the input side or output side via factory trimming. See Figure 15 on page 38 for the output side connection, and see Figure 16 on page 38 for the input side connection.

The I²C bit HICCUP_EN (MFR_CTRL4 (D4h), bit[5]) can disable hiccup mode.

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Switching Current Limit

The MPQ4232A senses the LS-FET current in loop control, then provides the valley current limit in buck mode and peak current limit in boost mode during each cycle-by-cycle switching. In buck mode, the next period does not start before I_L drops to the valley current limit. This folds back the frequency when the valley current limit is triggered.

Based on the cycle-by-cycle switching current limit, the MPQ4232A's maximum I_{IN} (I_{IN_MAX}) in buck mode can be calculated with Equation (1):

$$I_{IN_MAX}(A) = \frac{V_{OUT}}{V_{IN} \times \eta} \times (I_{VALLEY_BUCK}(A) + \frac{V_{IN} - V_{OUT}}{2 \times L(\mu H) \times f_{SW}(kHz)} \times \frac{V_{OUT}}{V_{IN}} \times 10^3) \quad (1)$$

Where η is the efficiency.

I_{IN_MAX} in boost mode can be calculated with Equation (2):

$$I_{IN_MAX}(A) = I_{PEAK_BOOST}(A) - \frac{V_{IN}}{2 \times L(\mu H) \times f_{SW}(kHz)} \times \frac{V_{OUT} - V_{IN}}{V_{OUT}} \times 10^3 \quad (2)$$

The buck valley current limit (I_{VALLEY_BUCK}) is typically 8.7A, and the boost peak current limit (I_{PEAK_BOOST}) is typically 12A. These limits are configurable via the I²C register (MFR_CTRL3 (D3h), bits[7:6]).

Output Over-Voltage Protection (Output OVP)

The MPQ4232A provides V_{OUT} over-voltage protection (OVP). If V_{FB} exceeds 118% of V_{REF}, then SWA, SWB, SWC, and SWD turn off. There is a resistor discharge path from the OUT pin to ground that turns on. If V_{FB} drops to 107% of V_{REF}, the chip resumes normal operation.

In addition, the MPQ4232A provides absolute output OVP. If V_{OUT} exceeds the absolute output OVP threshold (typically 27V rising, 25V falling), then absolute OVP is triggered, switching is disabled, and the discharge resistor turns on.

Input Over-Voltage Protection (Input OVP)

The MPQ4232A provides V_{IN} OVP. If V_{IN} exceeds the V_{IN} OVP threshold (V_{IN_OVP}) (typically 38.6V) for >2µs, then SWA, SWB, SWC, and SWD turn off to disable V_{OUT}.

Bootstrap (BST) Power

Capacitors placed between BST1 and SW1, as well as between BST2 and SW2 (C_{BST1} and C_{BST2}, respectively), are required to supply power. These capacitors are powered by either the internal diode from VCC or by charging each other. The regulated voltages of BST1 and BST2 are typically 3.54V. The bootstrap (BST) power provides its own UVLO control.

Forced Continuous Conduction Mode (FCCM)

In forced continuous conduction mode (FCCM), the buck on time (t_{ON_BUCK}) and boost off time (t_{OFF_BOOST}) are determined by the internal circuit to achieve a fixed frequency based on the V_{IN} / V_{OUT} ratio. When the load decreases, the average I_{IN} drops, and I_L may go negative from V_{OUT} to V_{IN} during the off time (SWD on). This forces I_L to work in continuous conduction mode with a fixed frequency, generating a lower V_{OUT} ripple compared to automatic pulse-frequency modulation (PFM) or pulse-width modulation (PWM) mode.

Automatic Pulse-Frequency Modulation (PFM)/Pulse-Width Modulation (PWM) or Pulse-Skip Mode (PSM)

In automatic PFM/PWM mode, once I_L drops to 0A, SWD turns off to prevent I_L from flowing from V_{OUT} to PGND. This forces I_L to work in discontinuous conduction mode (DCM). At the same time, the internal off time clock stretches once the MPQ4232A enters DCM. f_{SW} drops when the I_L conduction period decreases, which helps reduce power loss and the V_{OUT} ripple.

If V_{COMP} drops to the PSM threshold, then the MPQ4232A stops switching to minimize switching power loss. The MPQ4232A recovers switching once V_{COMP} exceeds the PSM threshold. The switching pulse skips based on V_{COMP} under very light-load conditions. PSM provides significantly higher efficiency compared to FCCM under light-load conditions; however, the V_{OUT} ripple may be higher due to the group switching pulse.

Switching Frequency (f_{SW}) and Frequency Spread Spectrum (FSS)

The MPQ4232A configures f_{SW} via the FREQ bits (MFR_CTRL1 (D0h), bits[6:5]). f_{SW} can be set to 280kHz, 400kHz, or 530kHz. A 400kHz f_{SW} is typically recommended.

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The MPQ4232A provides a frequency spread spectrum (FSS) function to minimize the peak emissions at set frequencies. Set the DITHER_ENABLE bit (D0h, bit[7]) to 1 to enable FSS. Set it to 0 to disable FSS.

The MPQ4232A uses a 2kHz triangle wave to modulate the internal oscillator. The frequency span for FSS operation is ±7% (see Figure 8).

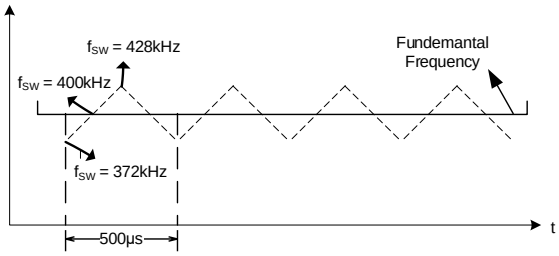

Figure 8: Frequency Spread Spectrum

FSS can be enabled for a 280kHz, 400kHz, or 530kHz f_{SW}.

Start-Up and Shutdown

If both V_{IN} and V_{EN} exceed their respective thresholds, the chip is enabled. The bandgap (BG) reference block starts up first, generating a stable V_{REF} and reference currents, then the internal VCC regulator is enabled. The regulator provides a stable supply for the remaining circuitries.

To enable the buck-boost output, I2C_EN must be turned on. I2C_EN is the logic or result of two signals: ADDR and the OPERATION bit (OPERATION (01h), bit[7]). For more details, see the ADDR Function section on page 23 and the OPERATION (01h) section on page 27.

Several events can shut down the chip: EN going low, V_{IN} going low, or thermal shutdown.

Figure 9 shows the start-up and shutdown state machine.

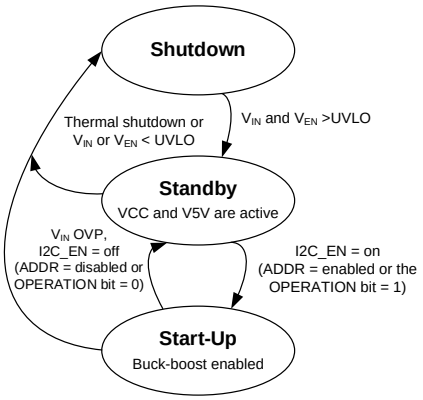

Figure 9: Start-Up and Shutdown State Machine

Slew Rate Control and Output Discharge

The MPQ4232A sets the V_{OUT} change slew rate via the internal SR bits. MFR_CTRL3 (D3h), bits[4:3] configure the rising slew rate, while MFR_CTRL3 (D3h), bits[2:1] configure the falling slew rate. Four V_{REF} change (rising and falling) slew rates can be selected according to different application requirements.

During voltage transients, the discharge function is enabled. After the V_{REF} change finishes, this function is automatically disabled. If V_{OUT} is not discharged to the target voltage by the time V_{REF} finishes changing due to excessive output capacitance (C_{OUT}), then the OVP discharge function continues discharging C_{OUT}.

The output discharge function is enabled if the following conditions are met:

- V_{REF} changes.
- The output OVP threshold (118% of V_{FB}) is triggered.
- The I²C OPERATION bit or the EN pin is disabled. Discharge works until the 250ms delay elapses.
- If V_{IN} UVLO is triggered while VCC has a residual voltage, the MPQ4232A discharges for a limited time. This discharge function is disabled after V_{CC} is below V_{CC_UVLO}.

V5V Low-Dropout (LDO) Regulator

The V5V LDO regulator uses V_{IN} as the input supply and outputs a fixed 5V voltage that can supply up to 60mA of load current. This regulator is enabled once V_{IN} exceeds V_{IN_UVLO} and V_{EN} exceeds $V_{EN_RISING1}$ (0.57V). The V5V LDO can also use V_{OUT} as the input supply

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when V_{IN} is below 6V, but V_{OUT} exceeds 6V. V5V remains on even when V_{IN} is below V_{IN_UVLO}, and it stays on until V_{CC} is below V_{CC_UVLO}.

Output Line Drop Compensation

The MPQ4232A can compensate for a V_{OUT} drop (e.g. high impedance caused by a long trace) to maintain a fairly constant load-side voltage.

See the MFR_CTRL2 (D2h) section on page 31 for more details regarding the line drop compensation amplitude.

ADDR Function

The ADDR pin configures the I²C target address and sets the default I2C_EN status. I2C_EN is the logic OR result of the OPERATION bit value in the I²C and the ADDR pin's status. The resistor divider on the ADDR pin determines the A7:A6 bit values of the 7-bit I²C address, and bits A5:A1 are configurable via the I²C or one-time programmable (OTP) memory. Figure 10 shows the ADDR connection.

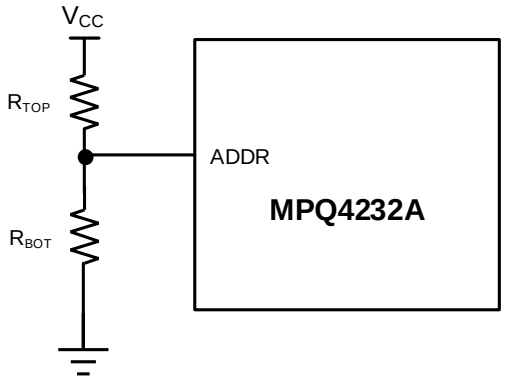

Figure 10: ADDR Connection

Table 1 shows the ADDR logic for the device address, top resistor (R_{TOP}), bottom resistor (R_{BOT}), and I2C_EN.

Table 1: ADDR Logic

Device Address	R_{TOP}	R_{BOT}	I2C_EN (9) (10)
67h	NS	0Ω	Off
47h	100kΩ	66.5kΩ	Off
27h	60.4kΩ	100kΩ	On
07h	0Ω	NS	On

Note:

9) If I2C_EN is on, V_{OUT} is on by default once V_{IN} and V_{EN} exceed their respective UVLO thresholds.

10) If I2C_EN is off, V_{OUT} is off by default. The user must set the OPERATION bit to 1 (either via the I²C or OTP) to enable V_{OUT}.

After V_{IN} and V_{EN} exceed their respective UVLO thresholds, the ADDR status is latched. ADDR only resets when V_{CC} drops below V_{CC_UVLO} (EN is pulled low or V_{IN} falls below 2.4V, typically).

SYSTEM

Thermal Shutdown (TSD)

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the silicon die temperature exceeds 165°C, the entire chip shuts down. Once the temperature falls below its lower threshold (typically 145°C), the chip is enabled.

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I²C INTERFACE

I²C Serial Interface

The power management bus (I²C) is an open-standard power management protocol that defines a means of communication with power conversion and other devices.

The I²C is a two-wire, bidirectional serial interface, consisting of a data line (SDA) and a clock line (SCL). The lines are pulled to a bus voltage (V_{BUS}) externally when they are idle. When connecting to the lines, an initiator device generates an SCL signal and device address, then arranges the communication sequence. This is based on I²C operation principles.

Start and Stop Commands

The start and stop commands are signaled by the initiator device, which signifies the beginning and end of the I²C transfer. A start (S) command is defined as the SDA signal transitioning from high to low while SCL is high. A stop (P) command is defined as the SDA signal transitioning from low to high while SCL is high (see Figure 11).

The initiator then generates the SCL clocks and transmits the device address and the read/write (R/W) direction bit on the SDA line. Data is transferred in 8-bit bytes by the SDA line. Each byte of data is followed by an acknowledge (ACK) bit.

I²C Update Sequence

The MPQ4232A requires a start command, a valid I²C address, a register address byte, and a data byte for a single data update. The device acknowledges receiving each byte by pulling the SDA line low during the high period of a single clock pulse. A valid I²C address selects the MPQ4232A. The device performs an update on the falling edge of the least significant bit (LSB) byte.

I²C Bus Message Format

Figure 12 on page 25 shows the I²C message format. The unshaded cells indicate that the bus host is actively driving the bus, and the shaded cells indicate that the MPQ4232A is driving the bus.

- S = Start command
- Sr = Repeated start command
- P = Stop command
- R = Read bit
- $\overline{W}$ = Write bit
- A = Acknowledge bit (0)
- $\overline{A}$ = Acknowledge bit (1)

A represents the ACK bit, which is typically active low (logic 0) if the transmitted byte is received successfully by a device.

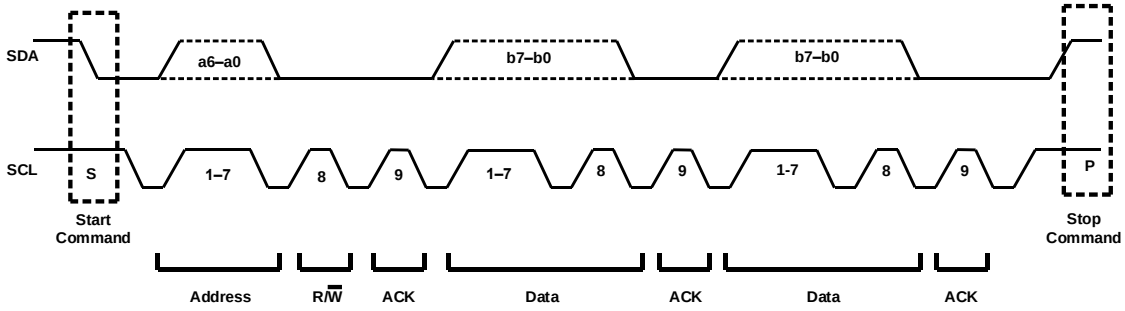

Figure 11: Data Transfer across the I²C

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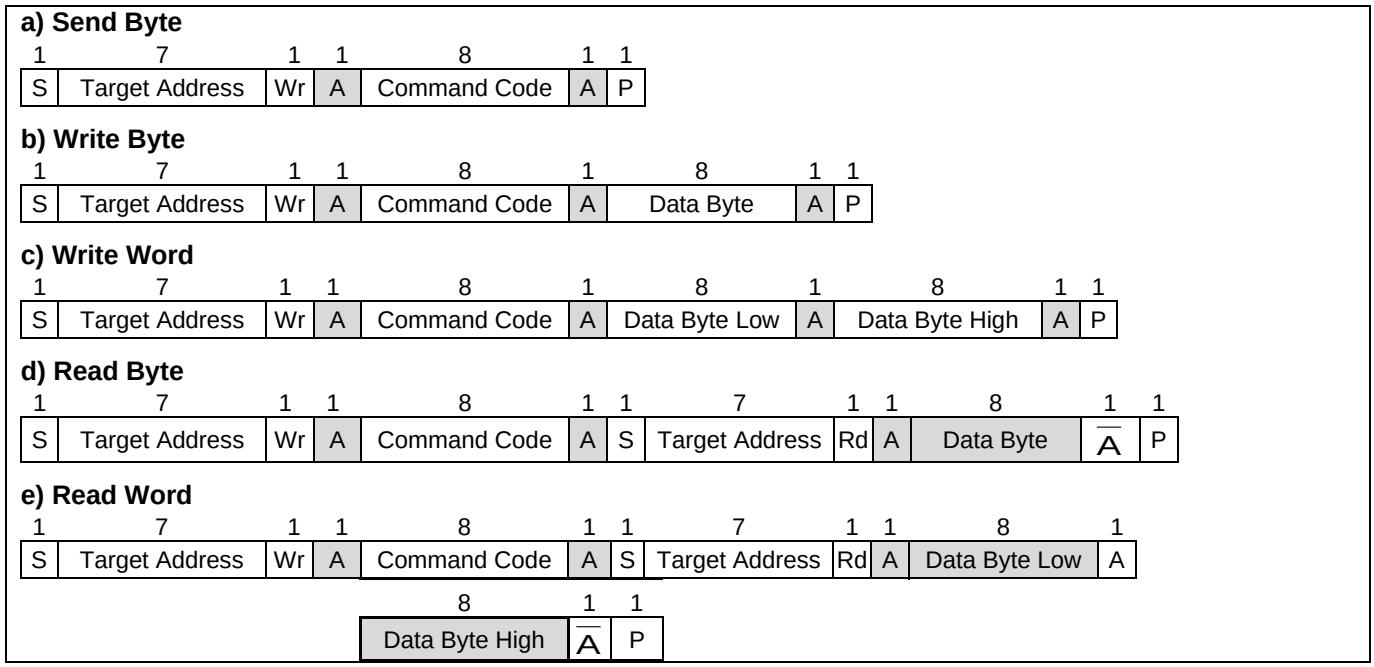

Figure 12: I²C Message Format

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REGISTER DESCRIPTION

I²C Register

The I²C is active once V_{IN} and V_{EN} exceed their respective UVLO thresholds. The default register values are based on the MPQ4232A-0000.

Command Code	Command Name	Description	Type	Data Format	Unit	OTP	Default Value
01h	OPERATION	On/off state	R/W byte	Reg	-	Yes	0
03h	CLEAR_FAULTS	-	Send byte	Reg	-	No	
21h	VOUT_COMMAND	-	R/W word	Linear L16	V	Yes	V_{REF} = 0.5V
79h	STATUS_WORD	-	R word	Reg	-	No	
7Dh	STATUS_TEMPERATURE	-	R byte	Reg	-	No	
D0h	MFR_CTRL1	-	R/W byte	Reg	-	Yes	
D1h	MFR_CURRENT_LIMIT	Sets the constant-current (CC) limit	R/W byte	Reg	-	Yes	5.4A
D2h	MFR_CTRL2	-	R/W byte	Reg	-	Yes	
D3h	MFR_CTRL3	-	R/W byte	Reg	-	Yes	
D4h	MFR_CTRL4	-	R/W byte	Reg	-	Yes	
D8h	MFR_STATUS_MASK	Masks the ALT# pin indication	R/W byte	Reg	-	Yes	
D9h	MFR_OTP_ CONFIGURATION_CODE	OTP configuration code	R/W byte	Reg	-	Yes	
DAh	MFR_OTP_REVISION_ NUMBER	OTP software revision	R/W byte	Reg	-	Yes	

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I²C COMMAND DESCRIPTION

OPERATION (01h)

Format: Unsigned binary

The OPERATION command configures the converter's operational state. The default OPERATION value is set via both the one-time programmable (OTP) memory and ADDR pin. If this command is set to 80h or ADDR enables EN, then the chip automatically turns on the output. The default OPERATION command value is 00h. After start-up, the OPERATION bit can be changed via the I²C.

Bits	Access	Bit Name	Default	Description
7	R/W	OPERATION	1'b0	Sets the on/off state. The EN pin has a higher control priority than this bit. 1'b0: The output is off (default) 1'b1: The output is on
6:0	R/W	RESERVED	7'b0000000	Reserved.

CLEAR_FAULTS (03h)

Format: Unsigned binary

The CLEAR_FAULTS command simultaneously clears any fault bits that have been set in all status registers. At the same time, the device clears its ALT# signal output if the device asserts the ALT# signal. This command cannot restart the device when it has latched off due to a fault condition.

If the fault remains once the bit is cleared, then the fault bit is immediately set again and the host is notified by the usual means. This command is write-only. For more details, see the send byte format in Figure 12 on page 25.

VOUT_COMMAND (21h)

Format: Unsigned binary

The VOUT_COMMAND command sets the output voltage (V_{OUT}). It follows the L16 linear data format. V_{OUT} (in V) can be calculated with Equation (3):

$$V_{OUT} = V \times 2^{-10} \quad (3)$$

Where *V* is the 16-bit unsigned binary integer of VOUT_COMMAND (21h), bits[15:0].

The valid V_{OUT} range is 1V to 21.47V. V_{OUT} is abnormal when it is beyond this range. The feedback (FB) resistor ratio should be V_{OUT} / V_{FB} = 10. The VOUT_COMMAND resolution is 10mV.

The internal reference voltage (V_{REF}) is V_{OUT} / 10 and ranges between 0.1V and 2.147V, with a 1mV step (total of 2,047 steps). This value is set by an 11-bit digital-to-analog converter (DAC) when the DAC input of the 11 bits is 0, and the DAC output is 0.1V.

Bits	Access	Bit Name	Default	Description
15:0	R/W	VOUT_COMMAND	16'b0001010000000000	Sets V_{REF}. V_{REF} = 0.5V (default).

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STATUS_WORD (79h)

Format: Unsigned binary

The STATUS_WORD command returns 2 bytes of information with a summary of the MPQ4232A's fault condition(s). Based on the information in these bytes, the host can obtain more information by reading the appropriate status registers. The PG_STATUS# bits are the exception to the rule that the status bit remains set, as they always reflect the current state of the POWER_GOOD signal (if present).

Byte	Bits	Access	Bit Name	Default	Description
Low	7	R	RESERVED	1'b0	Reserved. The default value is 0b.
	6	R	RESERVED	1'b0	Reserved. The default value is 0b.
	5	R	VOUT_OV_FAULT	1'b0	Indicates whether an output over-voltage (OV) fault has occurred.
	4	R	IOUT_OC_FAULT	1'b0	Indicates whether an output over-current (OC) fault has occurred. If the MPQ4232A reaches either the constant-current (CC) limit or peak current limit, or the device enters hiccup mode, then this bit is set.
	3	R	VIN_OV_FAULT	1'b0	Indicates whether an input voltage (V_{IN}) OV fault has occurred.
	2	R	TEMPERATURE	1'b0	Indicates whether a temperature fault or warning has occurred.
	1	R	RESERVED	1'b0	Reserved. The default value is 0b.
	0	R	RESERVED	1'b0	Reserved. The default value is 0b.
High	7	R	VOUT	1'b0	Indicates whether a V_{OUT} fault or warning has occurred.
	6	R	IOUT/POUT	1'b0	Indicates whether an output current (I_{OUT}) fault has occurred. If the MPQ4232A reaches either the CC or peak current limit, or the device enters hiccup mode, then this bit is set.
	5	R	RESERVED	1'b0	Reserved. The default value is 0b.
	4	R	OC_EXIT	1'b0	Indicates whether I_{OUT} has exited the CC limit. This bit is only set high when I_{OUT} changes from CC mode (before entering hiccup) to non-CC mode. Recovering from hiccup mode does not set this bit.
	3	R	PG_STATUS#	1'b0	If present, the POWER_GOOD signal is cleared. If this bit is set to 1, V_{OUT} is not good. If this bit is cleared, V_{OUT} is power good.
	2	R	RESERVED	1'b0	Reserved. The default value is 0b.
	1	R	RESERVED	1'b0	Reserved. The default value is 0b.
	0	R	RESERVED	1'b0	Reserved. The default value is 0b.

STATUS_TEMPERATURE (7Dh)

The STATUS_TEMPERATURE command returns 1 data byte to indicate an over-temperature (OT) fault or warning.

Bits	Access	Bit Name	Default	Description
7	R	OT_FAULT	1'b0	Indicates whether an OT fault has occurred. The over-temperature protection entry threshold is 165°C.
6	R	OT_WARNING	1'b0	Indicates whether an OT warning has occurred. The OT warning entry threshold is 135°C.
5	R	RESERVED	1'b0	Reserved.

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4	R	RESERVED	1’b0	Reserved.
3	R	RESERVED	1’b0	Reserved.
2	R	RESERVED	1’b0	Reserved.
1	R	RESERVED	1’b0	Reserved.
0	R	RESERVED	1’b0	Reserved.

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I²C REGISTER MAP

Name	REG (0x)	R/W	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
MFR_CTRL1	D0	R/W	DITHER_ ENABLE	FREQ		PWM/PFM_ MODE		OUTPUT_ OVP_EN	OUTPUT_ DISCHARGE_ EN	RSENS
MFR_CURRENT_ LIMIT	D1	R/W	LDC_ DISABLE	CONSTANT_CURRENT_LIMIT (0.5A to 6.35A/50mA step)						
MFR_CTRL2	D2	R/W	RESERVED						LINE_DROP_ COMPENSATION	
MFR_CTRL3	D3	R/W	SWITCHING_ CURRENT_LIMIT		CC_ ADJ	SLEW_ RATE_ RISE		SLEW_RATE_FALLI		FREQ_ MODE
MFR_CTRL4	D4	R/W	CC_BLANK_ TIMER		HICCUP _EN	I²C Address (A5:A1)				
MFR_STATUS_ MASK	D8	R/W	Masks the ALT# pin indication if a fault or event occurs.							
MFR_OTP_ CONFIGURATIO N_ CODE	D9	R/W	OTP configuration code, which is defined by MPS.							
MFR_OTP_ REVISION_ NUMBER	DA	R/W	OTP software revision number, which is defined by MPS.							

MFR_CTRL1 (D0h)

Format: Unsigned binary

The MFR_CTRL1 command sets the frequency mode, enables output over-voltage protection (OVP) and discharge, and selects the sense resistance (R_{SENS}).

Bits	Access	Bit Name	Default	Description
7	R/W	DITHER_ENABLE	1’b1	1’b0: No dither 1’b1: Enables frequency spread spectrum (FSS) (default)
6:5	R/W	FREQ	2’b 01	Sets the buck-boost switching frequency (f_{SW}). 2’b00: 280kHz 2’b01: 400kHz(default) 2’b10: 530kHz 2’b11: Reserved
4:3	R/W	PWM/PFM_MODE	2’b 01	Sets buck-boost operation. 2’b00: Reserved 2’b01: Forced pulse-width modulation (FPWM) mode (default) 2’b10: Automatic pulse-frequency modulation (PFM) or PWM mode 2’b11: Reserved
2	R/W	OUTPUT_OVP_EN	1’b1	Sets the output OVP enable or disable control. 1’b0: Disables output OVP 1’b1: Enables output OVP (default)

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1	R/W	OUTPUT_ DISCHARGE_EN	1'b1	Enables the output discharge function for a fixed 250ms. 1'b0: Disables output discharge during EN, V_{IN}, or I²C operation off 1'b1: Enables output discharge during EN, V_{IN}, or I²C operation off (default)
0	R/W	RSENS	1'b0	Selects the external current-sense (CS) resistance. 1'b0: 5mΩ (default) 1'b1: 10mΩ

MFR_CURRENT_LIMIT (D1h)

Format: Unsigned binary

The MFR_CURRENT_LIMIT command sets the output CC limit threshold and controls line drop compensation. The real-world over-current output current (I_{OUT_OC}) (in A) can be calculated with the following equation:

$$I_{OUT_OC}\ (A) = IOUT_LIM \times 0.05 \quad (4)$$

Where IOUT_LIM is the 7-bit unsigned binary integer of CONSTANT_CURRENT_LIMIT (bits[6:0] of this command).

The 0.05 ratio is proportional to R_{SENS}. To obtain an accurate I_{OUT_OC}, the value of MFR_CTRL1 (D0h), bit[0] requires matching the actual R_{SENS}. The I_{OUT_OC} resolution or minimum step is 50mA. The maximum value is 6.35A.

Bits	Access	Bit Name	Default	Description
7	R/W	LDC_DISABLE	1'b0	Enables line drop compensation. 1'b0: Enabled (default) 1'b1: Disabled
6:0	R/W	CONSTANT_ CURRENT_LIMIT	7'b1101100	Sets the CC limit. The default value is 5.4A.

MFR_CTRL2 (D2h)

Format: Unsigned binary

The MFR_CTRL2 command sets V_{OUT} compensation vs. I_{OUT}.

Bits	Access	Bit Name	Default	Description
7:2	R	RESERVED	6'b000000	Reserved.
1:0	R/W	LINE_DROP_ COMPENSATION	2'b00	Sets V_{OUT} compensation vs. I_{OUT}. 2'b00: No compensation (default) 2'b01: V_{OUT} compensates 100mV at a 3A I_{OUT} 2'b10: V_{OUT} compensates 300mV at a 3A I_{OUT} 2'b11: V_{OUT} compensates 600mV at a 3A I_{OUT} The above compensation amplitudes are fixed for any V_{OUT}. Line drop compensation is enabled when $V_{OUT} \geq 3V$. It is clamped when I_{OUT} exceeds 3.6A.

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MFR_CTRL3 (D3h)

Format: Unsigned binary

The MFR_CTRL3 command sets the switching current limit, V_{OUT} slew rate, and frequency mode in buck-boost mode.

<table>
<tr><th>Bits</th><th>Access</th><th>Bit Name</th><th>Default</th><th>Description</th></tr>
<tr><td>7:6</td><td>R/W</td><td>SWITCHING_
CURRENT_LIMIT</td><td>2’b01</td><td>Sets the current limit of switch B (SWB) and switch C (SWC).
<table>
<tr><th>Bits[7:6]</th><th>SWC Peak Current Limit</th><th>SWB Valley Current Limit</th></tr>
<tr><td>00</td><td>9A</td><td>6.6A</td></tr>
<tr><td>01 (default)</td><td>12A</td><td>8.7A</td></tr>
<tr><td>10</td><td>17.9A</td><td>12.6A</td></tr>
<tr><td>11</td><td>Reserved</td><td>Reserved</td></tr>
</table></td></tr>
<tr><td>5</td><td>R/W</td><td>CC_ADJ</td><td>1’b0</td><td>Adjusts the CC limit compared to the V_{OUT} gain.

1’b0: Does not add 50mA to the CC limit (default)
1’b1: Adds 50mA to the CC limit</td></tr>
<tr><td>4:3</td><td>R/W</td><td>SLEW_RATE_RISE</td><td>2’b01</td><td>Sets the V_{OUT}-adjusted rising slew rate.

2’b00: 0.08mv/µs V_{REF} rising slew rate
2’b01: 0.16mv/µs V_{REF} rising slew rate (default)
2’b10: 0.4mv/µs V_{REF} rising slew rate
2’b11: 0.8mv/µs V_{REF} rising slew rate

The V_{OUT} slew rate can be calculated with the following equation:

V_{OUT} Slew Rate = V_{REF} Slew Rate x Feedback Ratio

Where the FB ratio is 10 (see Figure 15 and Figure 16 on page 38).</td></tr>
<tr><td>2:1</td><td>R/W</td><td>SLEW_RATE_FALL</td><td>2’b10</td><td>Sets the V_{OUT}-adjusted falling slew rate.

2’b00: 0.02mv/µs V_{REF} falling slew rate
2’b01: 0.04mv/µs V_{REF} falling slew rate
2’b10: 0.1mv/µs V_{REF} falling slew rate (default)
2’b11: 0.2mv/µs V_{REF} falling slew rate

The V_{OUT} slew rate can be calculated with the following equation:

V_{OUT} Slew Rate = V_{REF} Slew Rate x Feedback Ratio

Where the FB ratio is 10 (see Figure 15 and Figure 16 on page 38).</td></tr>
<tr><td>0</td><td>R/W</td><td>FREQ_MODE</td><td>1’b1</td><td>Sets the frequency mode under buck-boost conditions.

1’b0: Reduces the frequency to 50% of that in buck and boost mode
1’b1: Reduces the frequency to 90% of that in buck and boost mode (default)</td></tr>
</table>

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MFR_CTRL4 (D4h)

Format: Unsigned binary

The MFR_CTRL4 command sets the CC blank timer and I²C address, and controls hiccup mode at the current limit. The I²C target address is 07h by default. The ADDR pin controls the A7 to A6 bits value, and the OTP controls the A5 to A1 bits value.

Bits	Access	Bit Name	Default	Description
7:6	R/W	CC_BLANK_TIMER	2'b01	Sets the blank time before the MPQ4232A enters CC mode: 2'b00: 320µs 2'b01: 2ms (default) 2'b10: 16ms 2'b11: 80ms
5	R/W	HICCUP_EN	1'b1	Enables hiccup mode at the current limit. 1'b0: Disabled 1'b1: Enabled (default)
4:0	R/W	I2C_ADDRESS	5'b0011 1	Sets the I²C target address of the A5:A1 bits. A7:A6 are determined by the ADDR pin. The default value is 00111b. The I²C target address is 07h when ADDR is pulled to VCC.

Table 2 shows the I²C target address and OPERATION bit setting.

Table 2: I²C Target Address and OPERATION Bit

ADDR Pin Voltage (V_{ADDR})	I²C Address (A7:A1)		OPERATION Bit Default Value
	Binary	Hex	
Pull low	1100 111 (default)	67h	Off
37% of V_{CC}	1000 111 (default)	47h	Off
62% of V_{CC}	0100 111 (default)	27h	On
V_{CC}	0000 111 (default)	07h	On

MFR_STATUS_MASK (D8h)

Format: Unsigned binary

This MFR_STATUS_MASK command can only mask off the ALT# pin behavior, but the STATUS register still indicates each event.

Bits	Access	Bit Name	Default	Description
7	R/W	VOUT_MSK	1'b1	1'b0: Not masked 1'b1: Mask enabled for V_{OUT} faults and warnings (default)
6	R/W	IOUT/POUT_MSK	1'b0	Masks IOUT_OC_FAULT, IOUT/POUT, and OC_EXIT. 1'b0: Not masked (default) 1'b1: Mask enabled
5	R/W	VIN_MSK	1'b1	1'b0: Not masked 1'b1: Mask enabled for V_{IN} faults and warnings (default)
4	R/W	TEMP_MSK	1'b1	Sets the temperature-related mask. 1'b0: Not masked 1'b1: Mask enabled (default)

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3:2	R/W	PG_MSK	2'b11	Sets the mask control of the power good (PG) rising and falling edges. PG rising means V_{OUT} goes from not good to good. 2'b00: Not masked. The ALT pin indicates both the PG rising and PG falling edges 2'b01: ALT only indicates rising PG, which means PG_STATUS# changes from 1 to 0 2'b10: ALT only indicates the PG falling edge, which means PG_STATUS# changes from 0 to 1 2'b11: ALT does not indicate any PG edge changes (default) ALT is not pulled down during the first time that PG rises.
1	R/W	RESERVED	1'b1	Reserved. The default value is 1b.
0	R/W	UNKNOWN_MSK	1'b1	1'b0: Not masked 1'b1: Mask enabled (default)

MFR_OTP_CONFIGURATION_CODE (D9h)

Format: Unsigned binary

The MFR_OTP_CONFIGURATION_CODE command returns the OTP configuration code.

Bits	Access	Bit Name	Description
7:0	R/W	OTP_ CONFIGURATION_ CODE	Returns the OTP configuration code, which is defined by MPS.

MFR_OTP_REVISION_NUMBER (DAh)

Format: Unsigned binary

The MFR_OTP_REVISION_NUMBER command returns the OTP software revision.

Bits	Access	Bit Name	Description
7:0	R/W	OTP_REVISION_ NUMBER	Returns the OTP software revision number, which is defined by MPS.

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APPLICATION INFORMATION

Selecting the Inductor

Inductor selection is based on the mode. The inductance in buck mode (L_{BUCK}) can be calculated with Equation (5):

$$L_{BUCK} = \frac{V_{OUT}}{f_{SW} \times \Delta I_L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (5)$$

Where ΔI_L is the peak-to-peak inductor ripple current, which is 30% to 50% of the maximum load current.

In boost mode, the inductor selection is based on limiting ΔI_L to 30% to 50% of the I_{IN_MAX}. The target inductance in boost mode (L_{BOOST}) can be calculated with Equation (6):

$$L_{BOOST} = \frac{V_{IN} \times (V_{OUT} - V_{IN})}{V_{OUT} \times f_{SW} \times \Delta I_L} \quad (6)$$

Where ΔI_L is the peak-to-peak ripple current and is about 30% to 50% of I_{IN_MAX}.

I_{IN_MAX} can be calculated with Equation (7):

$$I_{IN_MAX} = \frac{V_{OUT} \times I_{LOAD_MAX}}{V_{IN} \times \eta} \quad (7)$$

Where I_{LOAD_MAX} is the maximum load current, and η is the efficiency.

Choosing a larger inductance reduces the ripple current but also increases the inductor size. A larger inductance also reduces the converter's achievable bandwidth by moving the right half-plane zero to lower frequencies. Therefore, a compromise must made based on the application requirements.

Selecting the Input Capacitor

The input current (I_{IN}) in buck mode is discontinuous and continuous in boost mode, requiring a capacitor to supply the AC current in buck mode while maintaining the DC V_{IN}. Ceramic capacitors are recommended for the best performance and should be placed as close to the VIN pin as possible. Ceramic capacitors with X5R or X7R dielectrics are recommended because they are fairly stable amid temperature fluctuations. The capacitors must also have a ripple current rating greater than the converter's maximum input ripple current.

The input ripple current in buck mode (I_{CIN}) can be estimated with Equation (8):

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (8)$$

The worst-case condition in buck mode occurs at V_{IN} = 2x V_{OUT}, where I_{CIN} can be calculated with Equation (9):

$$I_{CIN} = \frac{I_{OUT}}{2} \quad (9)$$

For simplification, choose an input capacitor (C_{IN}) with an RMS current rating greater than half of the maximum load current.

C_{IN} determines the converter's input voltage ripple (ΔV_{IN}). If there is a ΔV_{IN} requirement in the system, choose C_{IN} to meet the specifications.

ΔV_{IN} in buck mode can be estimated with Equation (10):

$$\Delta V_{IN} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (10)$$

The worst-case condition occurs at V_{IN} = 2 x V_{OUT}, where ΔV_{IN} can be calculated with Equation (11):

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{f_{SW} \times C_{IN}} \quad (11)$$

ΔV_{IN} in boost mode can be estimated with Equation (12):

$$\Delta V_{IN} = \frac{V_{IN}}{8 \times f_{SW}^2 \times L \times C_{IN}} \times (1 - \frac{V_{IN}}{V_{OUT}}) \quad (12)$$

If using polymer, hybrid, or low-ESR electrolytic capacitors, the ESR dominates the impedance at f_{SW}. ΔV_{IN} in boost mode can be estimated with Equation (13):

$$\Delta V_{IN} = \frac{V_{IN}}{f_{SW} \times L} \times (1 - \frac{V_{IN}}{V_{OUT}}) \times (R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{IN}}) \quad (13)$$

Selecting the Output Capacitor

In boost mode, I_{OUT} is discontinuous, meaning the output capacitor (C_{OUT}) must be capable of reducing the output voltage ripple (ΔV_{OUT}).

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X5R or X7R dielectrics are recommended. If using ceramic capacitors, the capacitor's impedance at f_{SW} is dominated by the capacitance, meaning ΔV_{OUT} is independent of the ESR. ΔV_{OUT} in buck mode can be estimated with Equation (14):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^2 \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (14)$$

If using polymer, hybrid, or low-ESR electrolytic capacitors, the ESR dominates the impedance at f_{SW}. ΔV_{OUT} in buck mode can be estimated with Equation (15):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}}) \quad (15)$$

Where R_{ESR} is the equivalent series resistance (ESR) of C_{OUT}.

ΔV_{OUT} in boost mode can be estimated with Equation (16):

$$\Delta V_{OUT} = \frac{(1 - \frac{V_{IN}}{V_{OUT}}) \times I_{LOAD}}{C_{OUT} \times f_{SW}} \quad (16)$$

If using polymer, hybrid, or low-ESR electrolytic capacitors, the ESR dominates the impedance at f_{SW}. ΔV_{OUT} in boost mode can be estimated with Equation (17):

$$\Delta V_{OUT} = \frac{(1 - \frac{V_{IN}}{V_{OUT}}) \times I_{OUT}}{C_{OUT} \times f_{SW}} + \frac{I_{OUT} \times R_{ESR} \times V_{OUT}}{V_{IN}} \quad (17)$$

Choose C_{OUT} to meet the ΔV_{OUT} and load transient response requirements of the design. Consider the capacitance derating when designing applications with a high V_{OUT}.

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PCB Layout Guidelines (11)

Efficient PCB layout is critical for standard operation and thermal dissipation. For the best results, refer to Figure 14 and follow the guidelines below:

1. In buck mode, place the input filter capacitor (C_{IN}) as close to the VIN pin as possible.
2. In boost mode, place the output filter capacitor (C_{OUT}) and the OUT pin as close as possible.
3. Use short, direct, and wide traces to make the OUT pin connections.
4. If necessary, add vias to ground after the output filter.
5. Use a large copper plane for PGND and add multiple vias to improve thermal dissipation. Avoid using thin and long copper to connect to the PGND pins (see Figure 13).

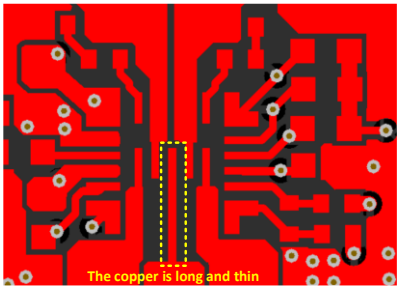
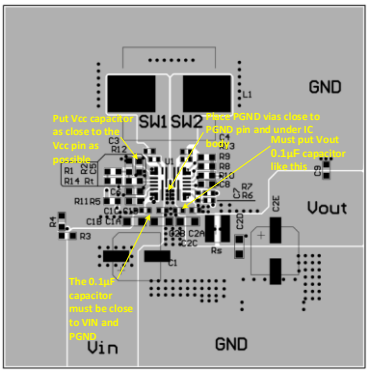


Figure 13: Poor PCB Layout

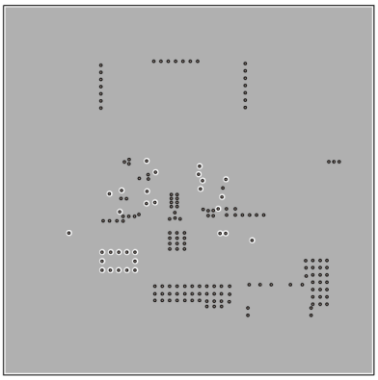
6. Connect AGND to PGND.
7. To improve EMI performance, place two decoupling ceramic input capacitors as close as possible to VIN, OUT, and PGND.
8. Place the input filter at the bottom layer for improved EMI performance.
9. Place the VCC decoupling capacitor (C_{VCC}) as close as possible to VCC.
10. The output current-sense traces (ISEN+ and ISEN-) must use a Kelvin connection.
11. The switching nodes of the BST1/BST2 capacitors (C_{BST1} and C_{BST2}, respectively) must be Kelvin connected to the SW1 and SW2 pins using a wide PCB trace.

Note:

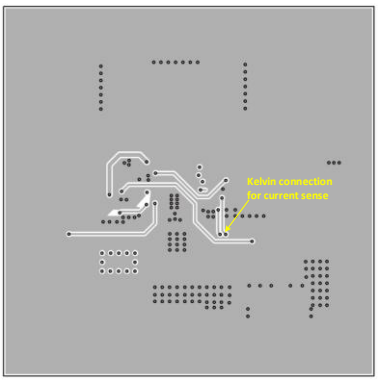
11) The recommended layout is based on Figure 15 on page 38.



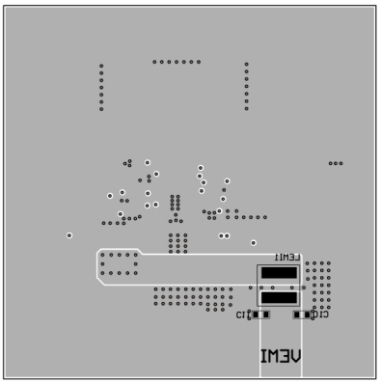
Top Layer



Mid-Layer 1



Mid-Layer 2



Bottom Layer

Figure 14: Recommended PCB Layout

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TYPICAL APPLICATION CIRCUITS (12) (13)

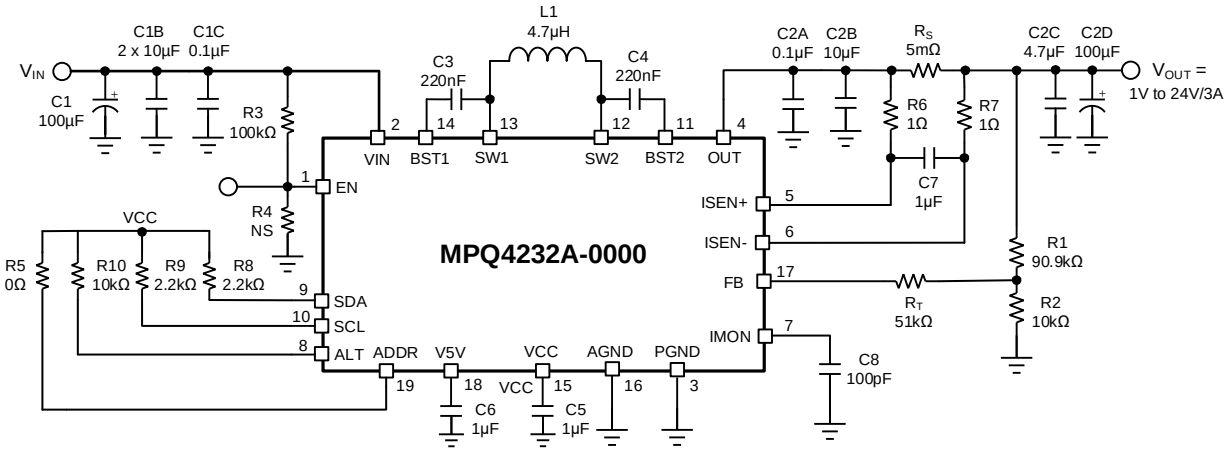

Figure 15: Typical Application Circuit (V_{IN} = 9V to 16V, V_{OUT} = 5V, 1V to 21.47V Adjustable via the I²C, I2C_EN On by Default)

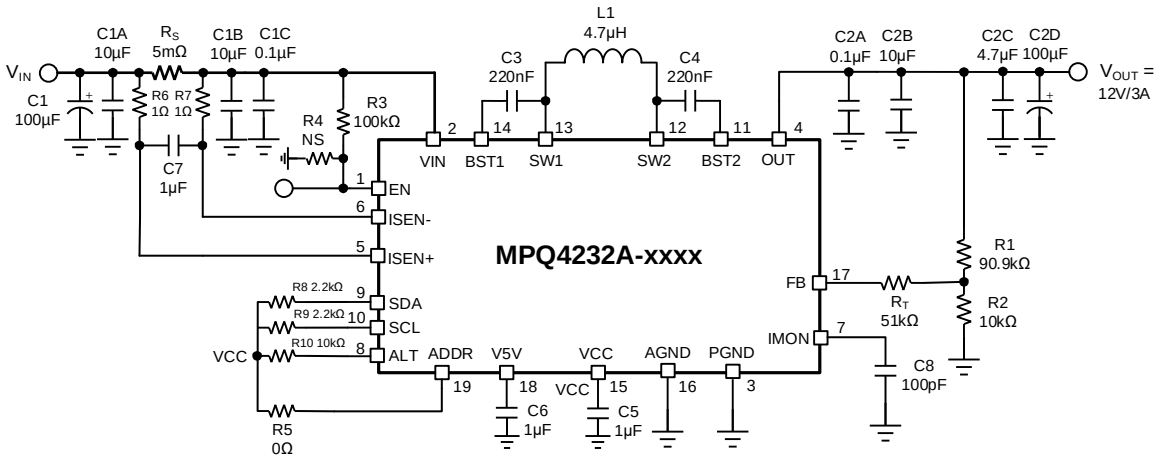

Figure 16: Typical Application Circuit (V_{IN} = 9V to 16V, V_{OUT} = 12V/3A Application with R_S On the Input Side)

Notes:

12) ADDR sets the I²C address and I2C_EN status. I2C_EN is the logic OR result of the OPERATION bit and ADDR status. When ADDR is connected to VCC, I2C_EN is on. V_{OUT} starts up automatically when V_{IN} and V_{EN} exceed their respective UVLO thresholds. When ADDR is connected to AGND, I2C_EN is off. When V_{IN} and V_{EN} exceed their respective UVLO thresholds, V_{OUT} does not start up until the OPERATION bit is written to 1. See Table 1 on page 23 for more details.

13) V5V outputs 5V and can supply an external MCU with a 60mA capability.

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MPQ4232AGVE-0000-AEC1 CONFIGURATION TABLE

OTP Items	Description	Value
OPERATION	Selects whether the MPQ4232A is on or off by default.	0: Off (14) (default)
VOUT_COMMAND	V_{OUT}, voltage reference (V_{REF}) = 0.5V.	5V (default)
DITHER_ENABLE	Enables frequency spread spectrum (FSS).	1: Enabled
FREQ	Sets the switching frequency (f_{SW}).	01: 400kHz (default)
PFM/PWM_MODE	Selects automatic pulse-frequency modulation (PFM) or pulse-width modulation (PWM) mode or forced PWM (FPWM) mode.	01: Forced PWM mode (default)
OUTPUT_OVP_EN	Enables output over-voltage protection (OVP).	1: Enabled (default)
OUTPUT_DISCHARGE_EN	Enables the output discharge function during the V_{IN}, I^2C, or EN disabled period.	1: Enabled (default)
RSENS	Selects R_{SENS}.	0: 5mΩ (default)
LDC_DISABLE	Enables line drop compensation.	0: Enables line drop compensation (default)
CONSTANT_CURRENT_LIMIT	Sets the output current (I_{OUT}) limit.	5.4 (default)
LINE_DROP_COMPENSATION	Sets V_{OUT} compensation vs. I_{OUT}.	00: No compensation (default)
SWITCHING_CURRENT_LIMIT	Sets the switch B (SWB) valley current limit and switch C (SWC) peak current limit.	01: SWC peak 12A, SWB valley 8.7A
CC_ADJ	Adjusts the CC limit vs. V_{OUT} gain.	0: Does not add 50mA to the CC limit (default)
SLEW_RATE_RISE	Sets the V_{REF} adjusted rising slew rate. The V_{OUT} slew rate can be calculated with the following equation: V_{OUT} Slew Rate = V_{REF} Slew Rate x Feedback Ratio Where the feedback ratio is 10.	01: 0.16mV/μs (default)
SLEW_RATE_FALL	Sets the V_{REF} adjusted falling slew rate. The V_{OUT} slew rate can be calculated with the following equation: V_{OUT} Slew Rate = V_{REF} Slew Rate x Feedback Ratio Where the feedback ratio is 10.	10: 0.1mV/μs (default)
FREQ_MODE	Sets the frequency mode under buck-boost conditions.	1: Maintains the same frequency as buck and boost mode
CC_BLANK_TIMER	Sets the blank time before the MPQ4232A enters CC mode.	01: 2ms (default)
HICCUP_EN	Enables hiccup mode during the current limit.	1: Enabled
OT_WARNING	Enables the over-temperature (OT) warning.	135°C (default)
I2C_ADDRESS	Sets the I^2C target address.	00111: 07h
VOUT_MSK	Masks ALT pin indication.	1: Masked
IOUT/POUT_MSK		0: Not masked
VIN_MSK		1: Masked
TEMP_MSK		1: Masked
PG_MSK		11: The ALT pin does not indicate any PG edge changes
RESERVED		1: Masked
UNKNOWN_MSK		1: Masked

Note:

14) Pull the ADDR pin above 57% of V_{CC} to enable V_{OUT}.

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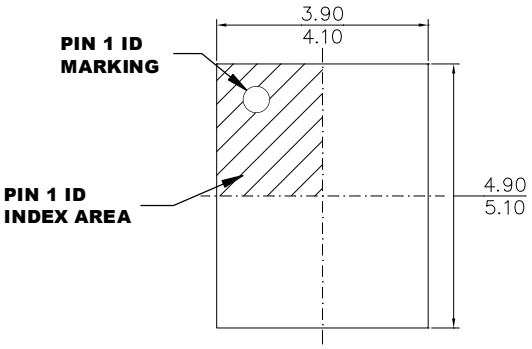
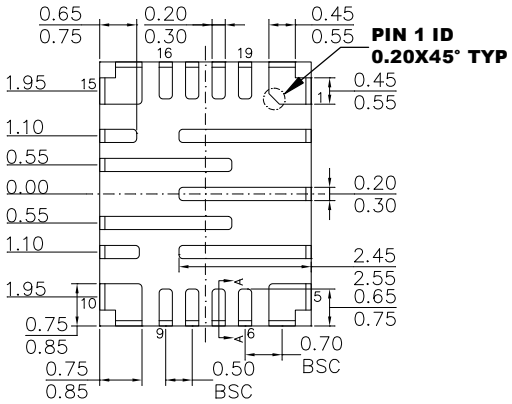
PACKAGE INFORMATION

QFN-19 (4mmx5mm)

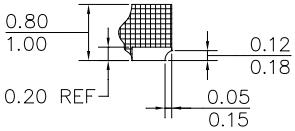


TOP VIEW

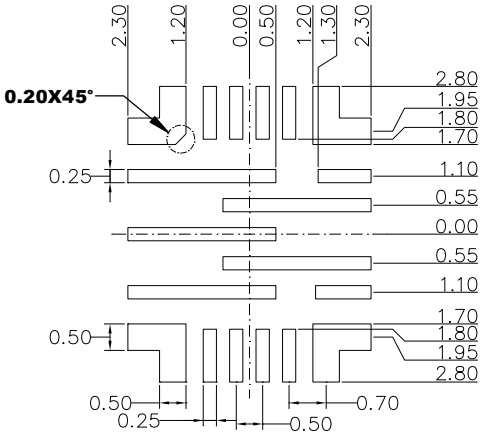


BOTTOM VIEW

SIDE VIEW



SECTION A-A



RECOMMENDED LAND PATTERN

NOTE:

1) THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

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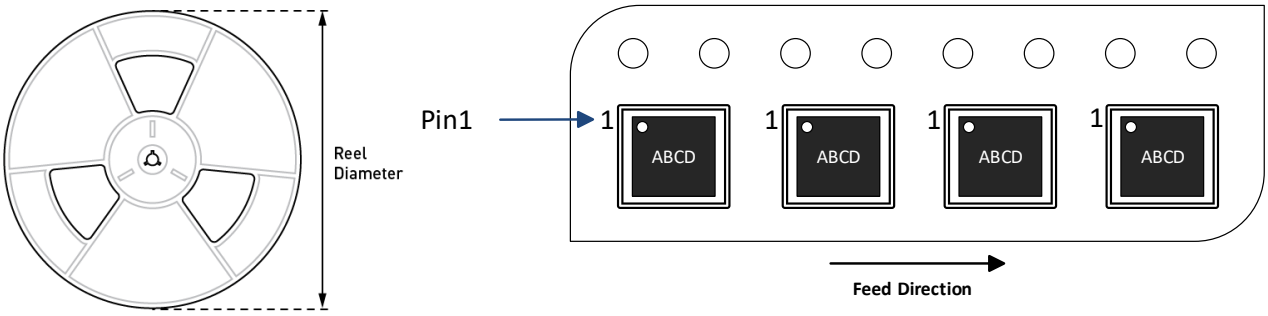
CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ4232AGVE-0000-AEC1-Z	QFN-19 (4mmx5mm)	5000	N/A	N/A	13in	12mm	8mm
MPQ4232AGVE-xxxx-AEC1-Z	QFN-19 (4mmx5mm)	5000	N/A	N/A	13in	12mm	8mm

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REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	6/11/2025	Initial Release	-

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