



MPQ3524

20V, 0.5A to 4A Peak,
Ultra-Compact, Low- I_Q , Synchronous
Step-Down Converter, AEC-Q100 Qualified

DESCRIPTION

The MPQ3524 family of converters are configurable-frequency (350kHz to 2.5MHz), synchronous, step-down switching regulators with integrated, internal high-side and low-side power MOSFETs (HS-FET and LS-FET, respectively). The MPQ3524 provides 0.5A to 3A of continuous output current (I_{OUT}) and a 4A peak, highly efficient I_{OUT} with peak current mode control.

The wide 3.3V to 20V input voltage (V_{IN}) range accommodates a variety of step-down applications in automotive and industrial input environments from 12V and 5V buses as well as multi-cell Li-ion batteries. A 1 μ A shutdown-mode quiescent current (I_Q) allows the device to be used in battery-powered applications.

High power conversion efficiency across a wide load range is achieved by scaling down the switching frequency (f_{SW}) under light-load conditions to reduce the switching and gate driving losses.

An open-drain power good (PG) signal indicates whether the output is within 94.5% to 105.5% of its nominal voltage.

Frequency foldback helps prevent inductor current (I_L) runaway during start-up. Thermal shutdown provides reliable, fault-tolerant operation.

The MPQ3524 is available in a QFN-12 (2mmx3mm) package, and is available in AEC-Q100 Grade 1.

FEATURES

- Designed for Automotive Applications
 - Continuous Operation Up to 20V
 - Supports Cold Crank Down to 3.1V
 - Low-Dropout Mode with Soft Recovery
 - 0.5A to 3A Continuous Output Current (I_{OUT}) and 4A Peak I_{OUT} Version in Pin-Compatible Family
 - 65ns Minimum On Time (t_{ON_MIN}) and 50ns Minimum Off Time (t_{OFF_MIN})
 - Available in AEC-Q100 Grade 1

FEATURES (continued)

- Increases Battery Life
 - 1 μ A Shutdown Supply Current
 - 20 μ A Sleep-Mode I_Q
 - Advanced Asynchronous Modulation (AAM) Mode Increases Efficiency under Light Loads
 - Integrated 70m Ω High-Side MOSFET (HS-FET) and 50m Ω Low-Side MOSFET (LS-FET)
- Optimized for EMC/EMI
 - CISPR 25 Class 5 Compliant
 - 350kHz to 2.5MHz Configurable f_{SW}
 - Frequency Spread Spectrum (FSS) Modulation
 - Symmetric VIN Pinout
 - MeshConnect™ Flip-Chip Package
- Additional Features
 - Power Good (PG) Output
 - Over-Current Protection (OCP) with Hiccup Mode
 - Fixed-Output Options ⁽¹⁾: 1V, 1.8V, 2.5V, 3.0V, 3.3V, 3.8V, or 5V
 - Available in a QFN-12 (2mmx3mm) Package with Wettable Flanks
- Functional Safety System Design Capability
 - MPSafe™ Compatible: Functional Safety Supporting Document Available



APPLICATIONS

- Automotive Infotainment
- Automotive Clusters
- Advanced Driver-Assistance Systems (ADAS)
- Industrial Power Systems
- Power over Coaxial (PoC) Systems

Note:

- See the Ordering Information section on page 3 regarding the fixed-output versions. Additional output voltages may be available. Contact MPS for details.

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TYPICAL APPLICATION

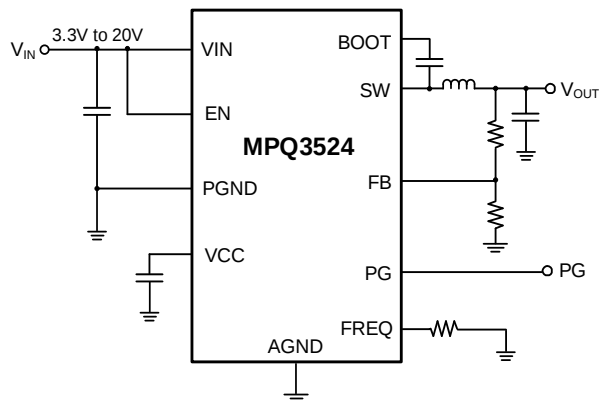


Figure 1: Typical Application (Adjustable-Output Version)

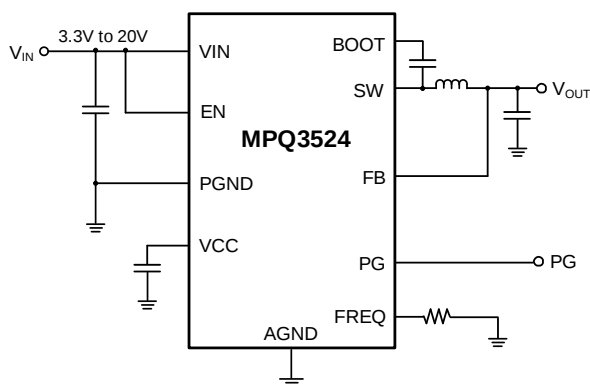
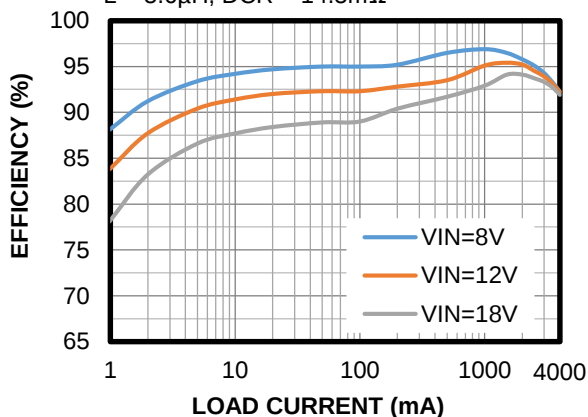


Figure 2: Typical Application (Fixed-Output Version)

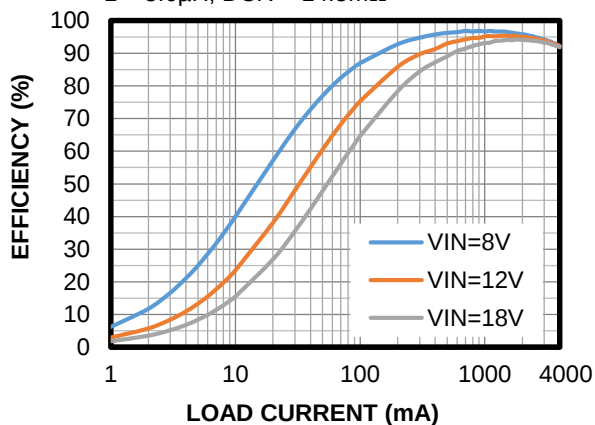
Efficiency vs. Load Current for MPQ3524-4000

AAM mode, $V_{OUT} = 5V$, $f_{SW} = 415kHz$,
 $L = 5.6\mu H$, $DCR = 14.5m\Omega$



Efficiency vs. Load Current for MPQ3524-4001

FCCM, $V_{OUT} = 5V$, $f_{SW} = 415kHz$,
 $L = 5.6\mu H$, $DCR = 14.5m\Omega$



ORDERING INFORMATION

Part Number ⁽²⁾ ^{(3)*}	Package	Top Marking	MSL Rating**
MPQ3524GDE-xxxx-AEC1***	QFN-12 (2mmx3mm)	See Below	1

* For Tape & Reel, add suffix -Z (e.g. MPQ3524GDE-xxxx-AEC1-Z).

** Moisture Sensitivity Level Rating

*** Wettable flanks

Notes:

- 2) Part numbers following the naming rule in Table 1 but not listed in the Ordering Information section may be also available. Contact MPS for details.
- 3) "MPQ3524-XYZ" is used as the part number, where -XYZ follow the naming rule of the four-digit code from Table 1.

Table 1: Part Number Digit Code Naming Rule

Digit Code	Naming Rule
XX: Defines the supported load current	05: 0.5A
	10: 1A
	15: 1.5A
	20: 2A
	30: 3A
	40: 4A (4A peak, 3A continuous)
Y: Defines the output voltage	0: Adjustable output
	1: 1V fixed output
	2: 2.5V fixed output
	3: 3.3V fixed output
	4: 3.8V fixed output
	5: 5V fixed output
	B: 1.8V fixed output
	C: 3V fixed output
Z: Defines the control mode	0: Advanced asynchronous modulation (AAM) mode with frequency spread spectrum (FSS)
	1: Forced continuous conduction mode (FCCM) with FSS
	2: AAM mode without FSS
	3: FCCM without FSS
	4: AAM mode with FSS, low dropout with soft recovery
	5: FCCM with FSS, low dropout with soft recovery
	6: AAM mode without FSS, low dropout with soft recovery
	7: FCCM without FSS, low dropout with soft recovery

TOP MARKING

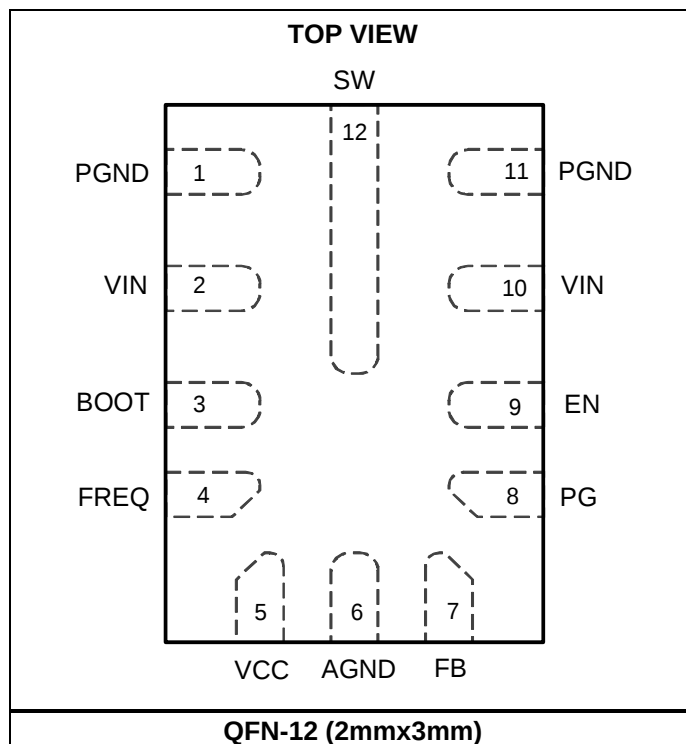
CDA

YWW

LLLL

CDA: Product code
Y: Year code
WW: Week code
LLLL: Lot number

PACKAGE REFERENCE



PIN FUNCTIONS

Pin #	Name	Description
1, 11	PGND	Power ground. Connect the PGND pin to a large PGND plane to ensure good heat dissipation.
2, 10	VIN	Input supply. The VIN pin supplies power to all the internal control circuitry and the power switch connected to SW. The two VIN pins are connected internally. Connect a decoupling capacitor from each VIN pin to ground, placed as close as possible, to minimize switching spikes and improve EMI performance.
3	BOOT	Bootstrap. The BOOT pin is the positive power supply for the high-side MOSFET (HS-FET) driver connected to SW. Connect a bypass capacitor between the BOOT and SW pins.
4	FREQ	Switching frequency configuration. Connect a resistor from the FREQ pin to ground to set the switching frequency (f_{SW}). See Table 3 on page 63 for more details on the relationship between the FREQ resistor (R_{FREQ}) and f_{SW} .
5	VCC	Bias supply. The VCC pin is the internal regulator's output that supplies power to the internal control circuit and gate drivers. Connect a minimum 1 μ F decoupling capacitor from VCC to ground. The capacitor should be placed as close as possible to VCC.
6	AGND	Analog ground. Connect the AGND pin close to the VCC capacitor (C_{VCC}).
7	FB	Feedback input. The FB pin is the negative input of the error amplifier (EA), and its typical value is 0.8V. For a fixed-output version, connect FB directly to the output voltage (V_{OUT}). For the adjustable-output version, connect FB to the external feedback divider's middle point, between the output and AGND, to set V_{OUT} .
8	PG	Power good (PG) output. The PG output is an open drain. If the PG pin is used, it must be connected to a power source via a pull-up resistor. PG goes high if V_{OUT} is within 94.5% to 105.5% of the nominal voltage; PG goes low if V_{OUT} exceeds 107% or drops below 93% of the nominal voltage. Float PG if it is not used.
9	EN	Enable. Pull the EN pin below the specified threshold (about 0.85V) to shut down the chip; pull EN above the specified threshold (about 1.02V) to enable the chip. EN does not have an internal pull-up or pull-down resistor. Do not float EN.
12	SW	Switch node. The SW pin is the HS-FET source and the low-side MOSFET (LS-FET) drain.

ABSOLUTE MAXIMUM RATINGS ⁽⁴⁾

V _{IN} , EN.....	-0.3V to +22V
SW.....	-0.3V to V _{IN_MAX} + 0.3V
BOOT.....	V _{SW} + 5.5V
FREQ, VCC.....	5.5V
All other pins.....	-0.3V to +6V
Continuous power dissipation (T _A = 25°C) ⁽⁵⁾	
QFN-12 (2mmx3mm).....	3.5W ⁽⁹⁾
Operating junction temperature (T _J).....	150°C
Lead temperature.....	260°C
Storage temperature.....	-65°C to +150°C

ESD Ratings

Human body model (HBM).....	Class 2 ⁽⁶⁾
Charged-device model (CDM).....	Class C2b ⁽⁷⁾

Recommended Operating Conditions

Supply voltage (V _{IN}).....	3.3V to 20V
Minimum V _{IN} for start-up.....	3.9V
Minimum V _{IN} after start-up.....	3.1V
Output voltage (V _{OUT}).....	0.8V to 0.95 x V _{IN}
Operating junction temp (T _J)	
.....	-40°C to +150°C

Thermal Resistance θ_{JA} θ_{JC}

QFN-12 (2mmx3mm)		
JESD51-7.....	60.....	7.3... °C/W ⁽⁸⁾
EVQ3524-D-00A.....	35.5.....	°C/W ⁽⁹⁾
		Ψ_{JT}
JESD51-7.....	1.1.....	°C/W ⁽⁸⁾
EVQ3524-D-00A.....	3.5.....	°C/W ⁽⁹⁾

Notes:

- 4) The absolute maximum ratings are rated under room temperature, unless otherwise noted. Exceeding these ratings may damage the device.
- 5) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA} , and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA} . Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the device may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- 6) Per AEC-Q100-002.
- 7) Per AEC-Q100-011.
- 8) Based on JESD51-7, a 4-layer PCB. The values given in this table are only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7 and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application. The θ_{JC} value shows the thermal resistance from the junction-to-case bottom, and the Ψ_{JT} value shows the characterization parameter from the junction-to-case top
- 9) Measured on the EVQ3524-D-00A, a 2oz copper thickness, 4-layer PCB (8.3cmx8.3cm). The Ψ_{JT} value shows the characterization parameter from the junction-to-case top.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, V_{EN} = 2V, T_J = -40°C to +150°C, typical values are at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Supply						
Input voltage (V _{IN}) under-voltage lockout (UVLO) rising threshold	V _{IN_UVLO_RISING}		3.4	3.65	3.9	V
V _{IN} UVLO falling threshold	V _{IN_UVLO_FALLING}		2.6	2.9	3.1	V
V _{IN} UVLO hysteresis	V _{IN_UVLO_HYS}			750		mV
VIN quiescent current	I _Q	V _{FB} = 0.85V, AAM mode, no load, T _J = 25°C		20	28	μA
		V _{FB} = 0.85V, AAM mode, no load, T _J = -40°C to +125°C ⁽¹⁰⁾			34	μA
		V _{FB} = 0.85V, AAM mode, no load, T _J = -40°C to +150°C			80	μA
VIN quiescent current (switching) ⁽¹⁰⁾	I _{Q_SWITCHING}	AAM mode, switching, R _{FB1} = 1MΩ, R _{FB2} = 191kΩ, no load		25		μA
VIN active current (switching) ⁽¹⁰⁾	I _{Q_ACTIVE}	FCCM, no load		1200		μA
VIN shutdown current	I _{SHDN}	V _{EN} = 0V		1	10	μA
Switches and Frequency						
Switching frequency without frequency spread spectrum (FSS)	f _{SW}	R _{FREQ} = 86.6kΩ	332	415	498	kHz
		R _{FREQ} = 34.8kΩ	900	1000	1100	kHz
		R _{FREQ} = 15kΩ	1980	2200	2420	kHz
Frequency SS span				±10		%
FSS modulation frequency				15		kHz
Minimum on time ⁽¹⁰⁾	t _{ON_MIN}			65	80	ns
Minimum off time ⁽¹⁰⁾	t _{OFF_MIN}			50	70	ns
Maximum duty cycle	D _{MAX}		98	99.5		%
Switch leakage current	I _{SW_LKG}	V _{EN} = 0V, V _{SW} = V _{BOOT} = 0V or V _{IN} (T _J = 25°C)		0.01	1	μA
		V _{EN} = 0V, V _{SW} = V _{BOOT} = 0V or V _{IN} (T _J = -40°C to +150°C)		0.01	5	μA
High-side MOSFET (HS-FET) on resistance	R _{DS(ON)_HS}	V _{BOOT} - V _{SW} = 5V		70	130	mΩ
Low-side MOSFET (LS-FET) on resistance	R _{DS(ON)_LS}	V _{CC} = 5V		50	90	mΩ
Output and Regulation						
FB voltage (adjustable-output version)	V _{FB}	T _J = 25°C	0.794	0.8	0.806	V
		T _J = -40°C to +150°C	0.790	0.8	0.810	V
FB input current	I _{FB}	Adjustable-output version		0	100	nA
		Fixed-output version		3.8		μA
Output voltage (V _{OUT}) discharge current	I _{DISCHARGE}	V _{EN} = 0V, V _{OUT} = 0.3V	2	4		mA

ELECTRICAL CHARACTERISTICS (continued)

V_{IN} = 12V, V_{EN} = 2V, T_J = -40°C to +150°C, typical values are at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
V _{OUT} accuracy of 3.3V fixed-output version	V _{OUT_3.3V}	T _J = 25°C	3250	3300	3350	mV
		T _J = -40°C to +150°C	3234	3300	3366	mV
V _{OUT} accuracy of 3.8V fixed-output version	V _{OUT_3.8V}	T _J = 25°C	3743	3800	3857	mV
		T _J = -40°C to +150°C	3724	3800	3876	mV
V _{OUT} accuracy of 5V fixed-output version	V _{OUT_5V}	T _J = 25°C	4925	5000	5075	mV
		T _J = -40°C to +150°C	4900	5000	5100	mV
BOOT						
BOOT to SW refresh rising	V _{BOOT-TO-SW_RISING}			2.5	2.9	V
BOOT to SW refresh falling	V _{BOOT-TO-SW_FALLING}			2.3	2.7	V
BOOT to SW refresh hysteresis	V _{BOOT-TO-SW_HYS}			0.2		V
Enable (EN)						
EN rising threshold	V _{EN_RISING}		0.97	1.02	1.07	V
EN falling threshold	V _{EN_FALLING}		0.8	0.85	0.9	V
EN threshold hysteresis	V _{EN_HYS}			170		mV
Soft Start (SS) and VCC						
Soft-start time	t _{SS}	EN high to SS finishes	3	5	7	ms
VCC voltage	V _{CC}	I _{VCC} = 0	4.7	5	5.3	V
VCC regulation		I _{VCC} = 30mA		1		%
VCC current limit	I _{LIMIT_VCC}	V _{CC} = 4V	50	70		mA
Power Good (PG)						
PG rising threshold (adjustable-output version)	PG _{VTH_RISING}	V _{OUT} rising, V _{FB} / V _{REF}	93	94.5	96	% of V _{REF}
		V _{OUT} falling, V _{FB} / V _{REF}	104	105.5	107	
PG rising threshold (fixed-output version)	PG _{VTH_RISING}	V _{OUT} rising, V _{FB} / V _{OUT}	93	94.5	96.5	% of V _{OUT}
		V _{OUT} falling, V _{FB} / V _{OUT}	104	105.5	108	
PG falling threshold (adjustable-output version)	PG _{VTH_FALLING}	V _{OUT} falling, V _{FB} / V _{REF}	91.5	93	94.5	% of V _{REF}
		V _{OUT} rising, V _{FB} / V _{REF}	105.5	107	108.5	
PG falling threshold (fixed-output version)	PG _{VTH_FALLING}	V _{OUT} rising, V _{FB} / V _{OUT}	91.5	93	95	% of V _{OUT}
		V _{OUT} falling, V _{FB} / V _{OUT}	105.5	107	109.5	
PG threshold hysteresis	PG _{VTH_HYS}	V _{FB} / V _{REF}		1.5		% of V _{REF}
PG output voltage low	V _{PG_LOW}	I _{SINK} = 1mA		0.1	0.3	V
PG rising deglitch time	t _{PG_R}			160		μs
PG falling deglitch time	t _{PG_F}			160		μs

ELECTRICAL CHARACTERISTICS (continued)

V_{IN} = 12V, V_{EN} = 2V, T_J = -40°C to +150°C, typical values are at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Protections						
High-side (HS) peak current limit	I _{LIMIT_HS}	Duty cycle = 30%, 0.5A version	0.8	1.35	2	A
		Duty cycle = 30%, 1A version	1.5	2	2.6	A
		Duty cycle = 30%, 1.5A version	2.0	2.6	3.1	A
		Duty cycle = 30%, 2A version	2.7	3.4	4.6	A
		Duty cycle = 30%, 3A version	4.3	5.8	7.3	A
		Duty cycle = 30%, 4A version	4.9	6.5	7.9	A
Low-side (LS) valley current limit	I _{LIMIT_LS}	0.5A version	0.5	1	1.5	A
		1A version	1	1.5	2	A
		1.5A version	1.4	2	2.7	A
		2A version	2	2.7	3.8	A
		3A version	3	4.4	5.7	A
		4A version	3.8	5	6.8	A
Zero-current detection (ZCD) current	I _{ZCD}	AAM mode	-0.1	0.05	+0.2	A
LS reverse current limit	I _{LIMIT_REVERSE}			2		A
Thermal shutdown ⁽¹⁰⁾	T _{SD}		160	175	185	°C
Thermal shutdown hysteresis ⁽¹⁰⁾	T _{SD_HYS}			20		°C

Note:

10) Not tested in production. Guaranteed by design and characterization.

TIMING SEQUENCE DIAGRAM

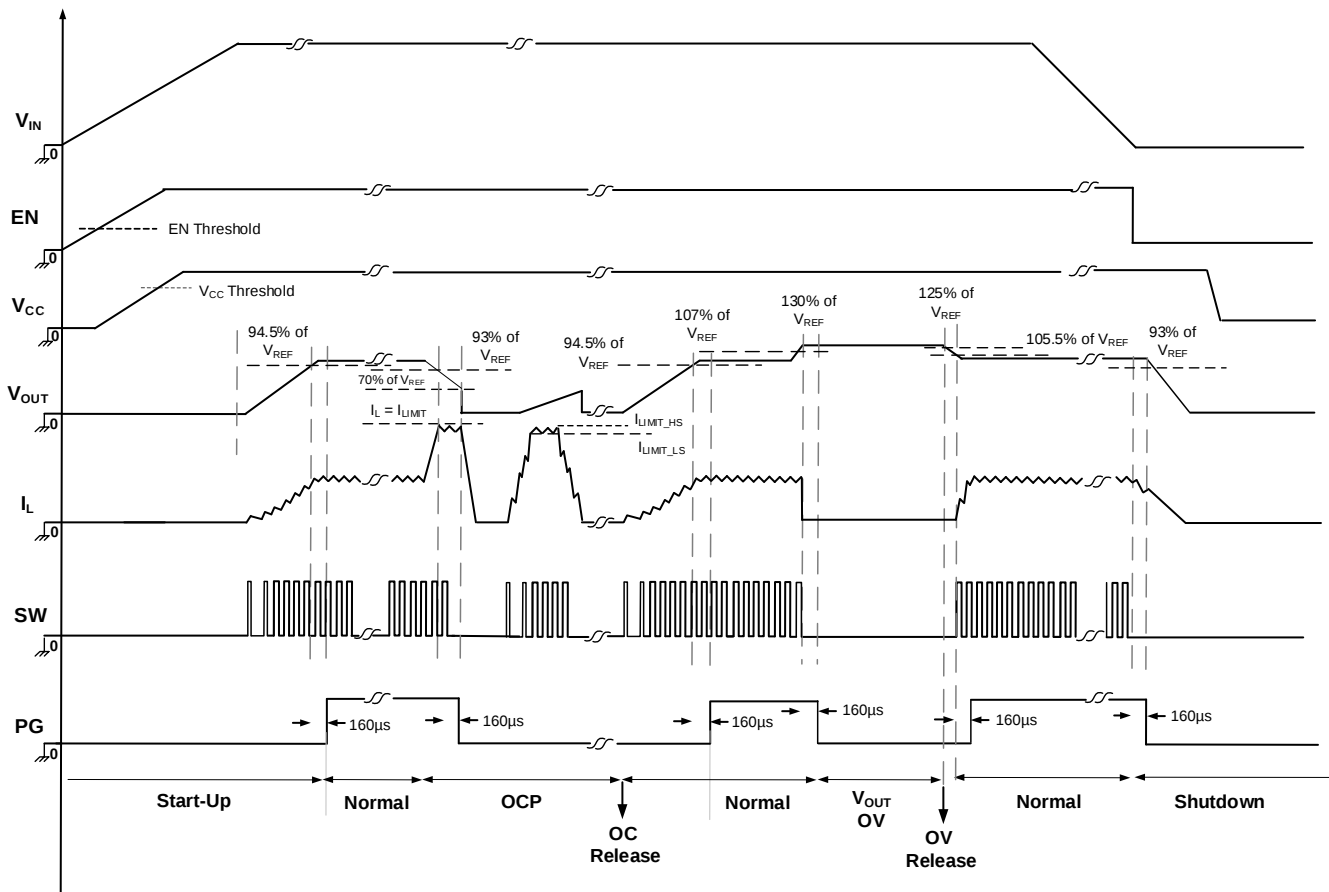
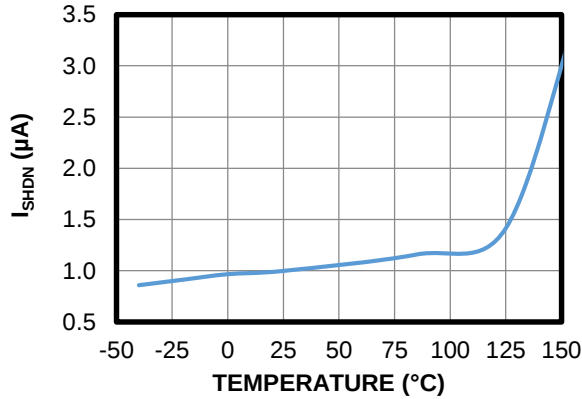


Figure 3: Timing Sequence Diagram

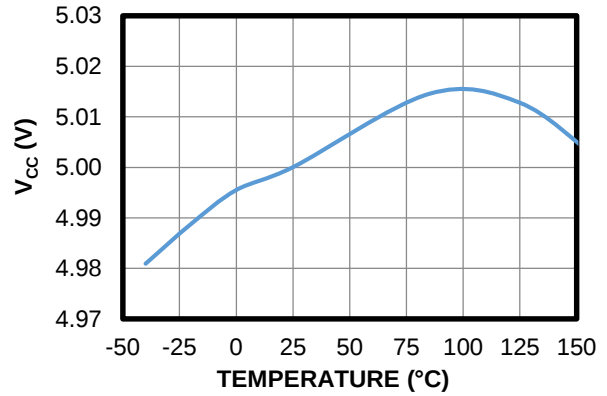
TYPICAL CHARACTERISTICS

$V_{IN} = 12V$, unless otherwise noted.

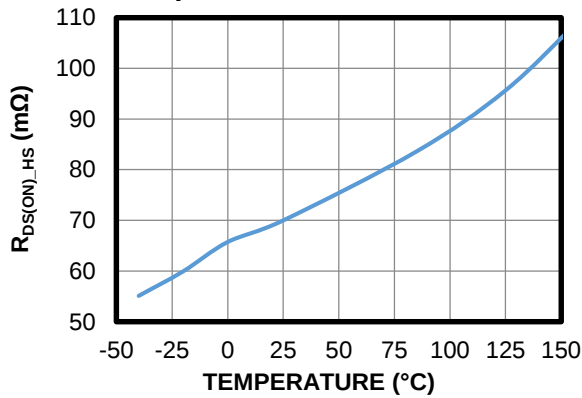
VIN Shutdown Current vs. Temperature



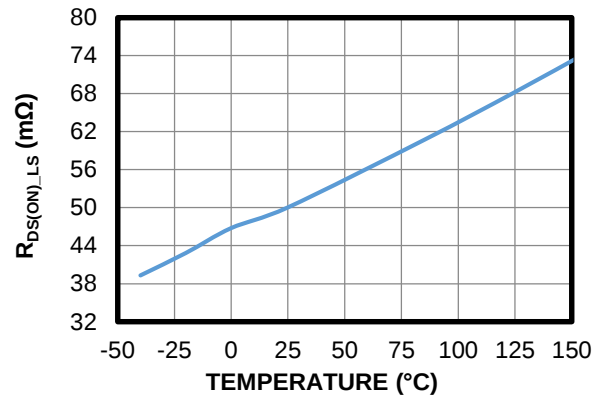
VCC Voltage vs. Temperature



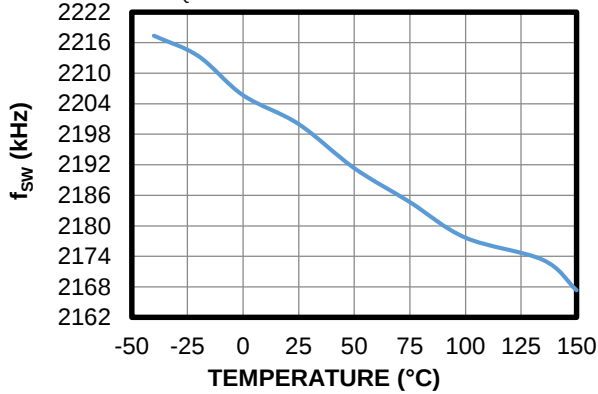
HS-FET On Resistance vs. Temperature



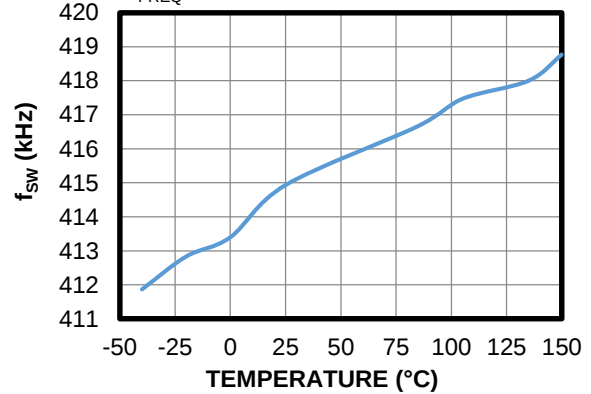
LS-FET On Resistance vs. Temperature



f_{SW} vs. Temperature
 $R_{FREQ} = 15k\Omega$

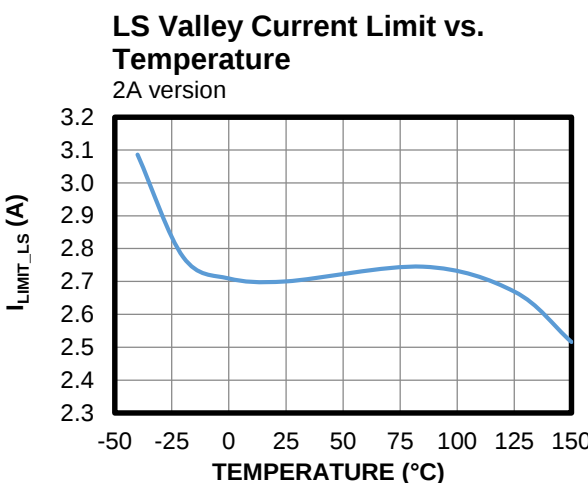
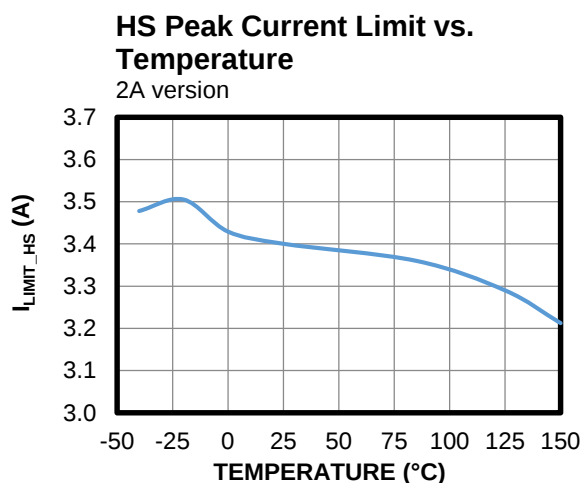
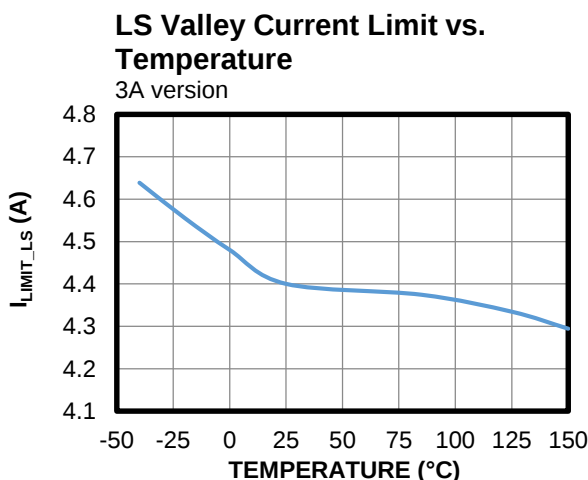
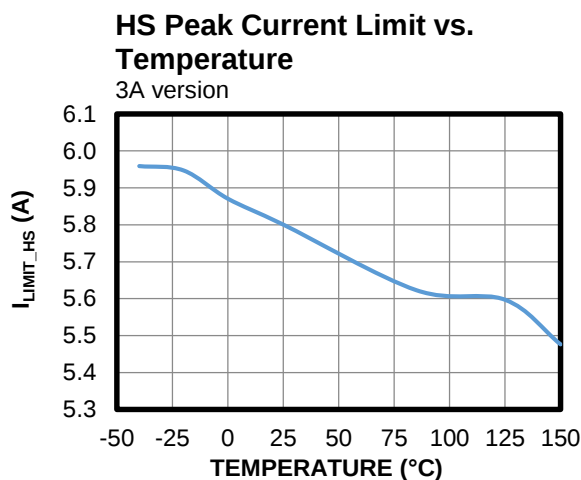
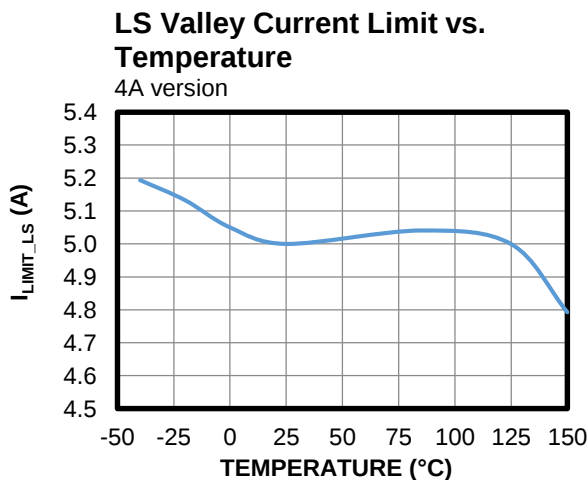
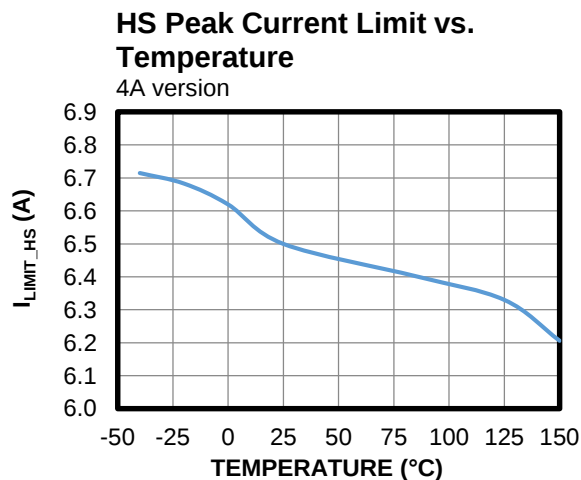


f_{SW} vs. Temperature
 $R_{FREQ} = 86.6k\Omega$



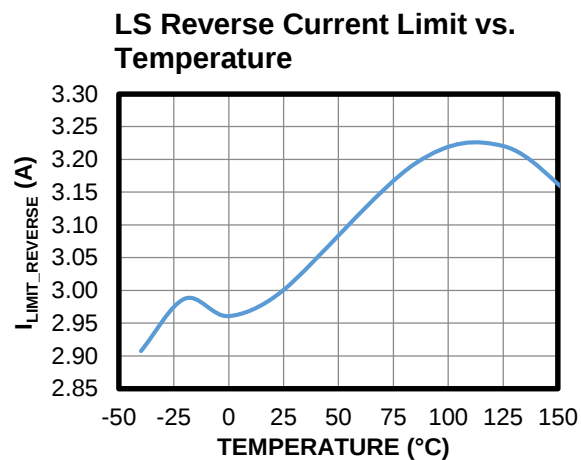
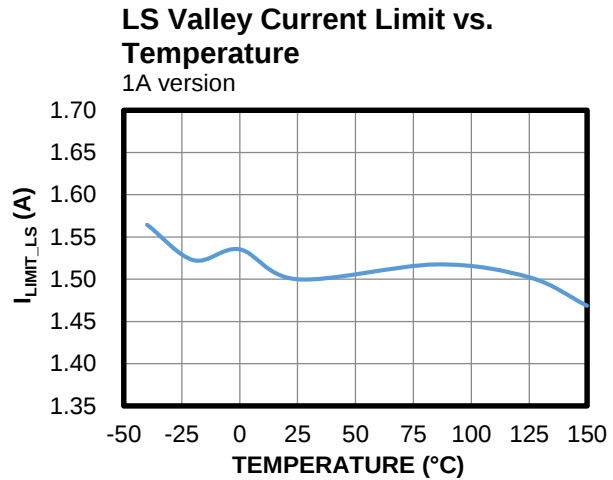
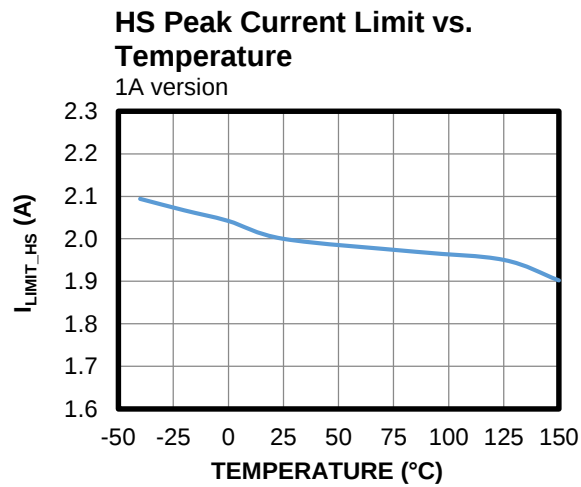
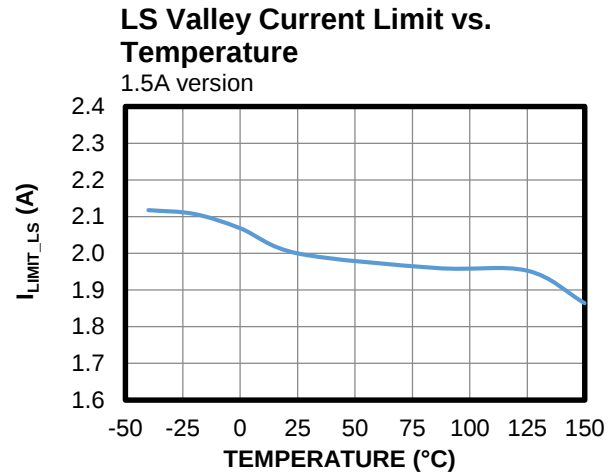
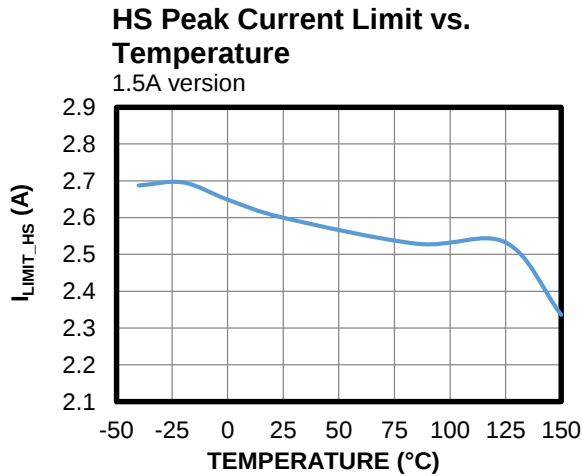
TYPICAL CHARACTERISTICS (continued)

V_{IN} = 12V, unless otherwise noted.



TYPICAL CHARACTERISTICS (continued)

V_{IN} = 12V, unless otherwise noted.

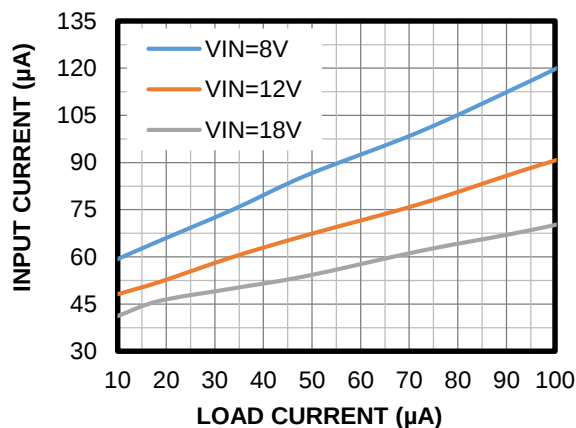


TYPICAL PERFORMANCE CHARACTERISTICS

$V_{IN} = 12V$, $V_{OUT} = 5V$, $f_{SW} = 2.2MHz$, $L = 2.2\mu H$, $C_{OUT} = 2 \times 22\mu F$, $T_A = 25^\circ C$, unless otherwise noted.

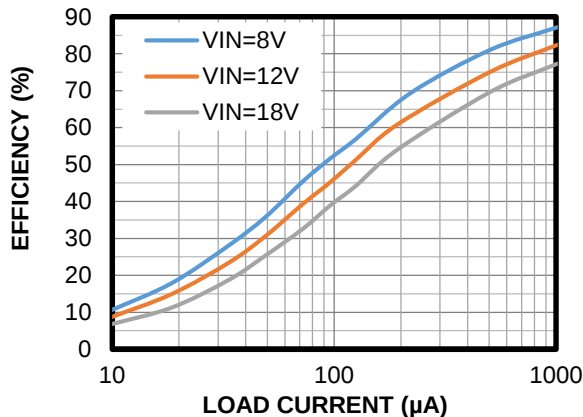
Input Current vs. Load Current for MPQ3524-4000/3000

AAM mode, $R_{FB1} = 100k\Omega$,
 $R_{FB2} = 19.1k\Omega$, DCR = 22.1m Ω



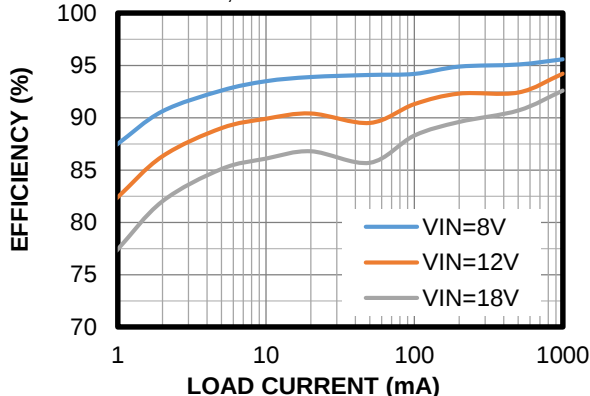
Efficiency vs. Load Current for MPQ3524-4000/3000

AAM mode, $R_{FB1} = 100k\Omega$,
 $R_{FB2} = 19.1k\Omega$, DCR = 22.1m Ω



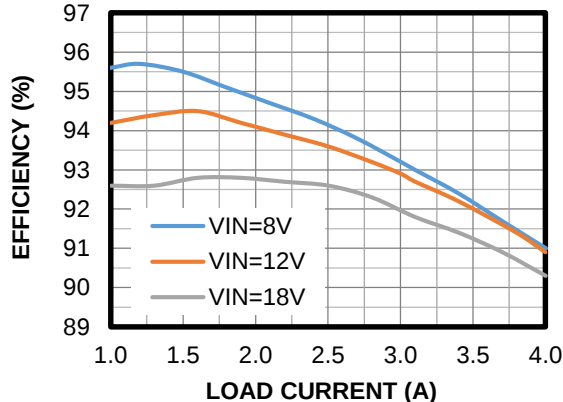
Efficiency vs. Load Current for MPQ3524-4000/3000

AAM mode, DCR = 22.1m Ω



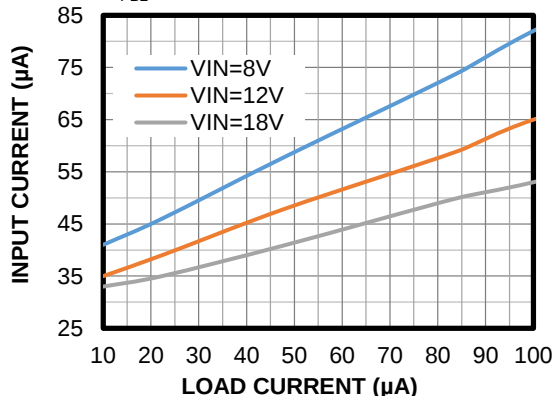
Efficiency vs. Load Current for MPQ3524-4000/3000

AAM mode, DCR = 22.1m Ω



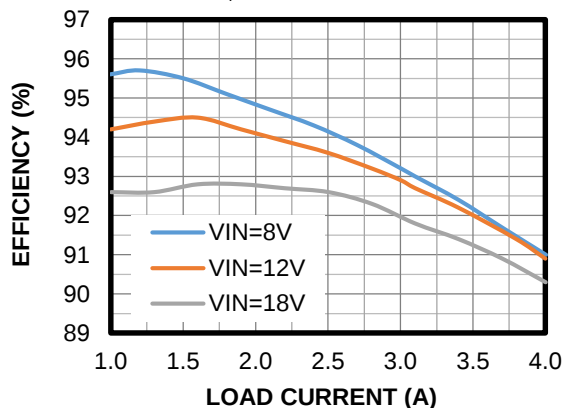
Input Current vs. Load Current for MPQ3524-4000/3000

AAM mode, $V_{OUT} = 3.3V$, $R_{FB1} = 100k\Omega$,
 $R_{FB2} = 31.6k\Omega$, DCR = 22.1m Ω



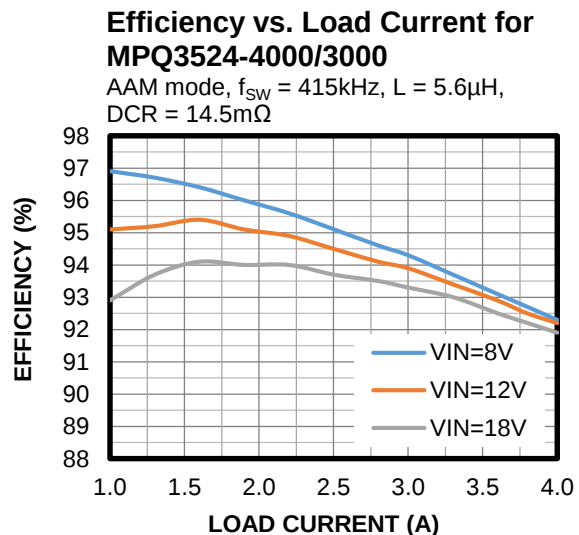
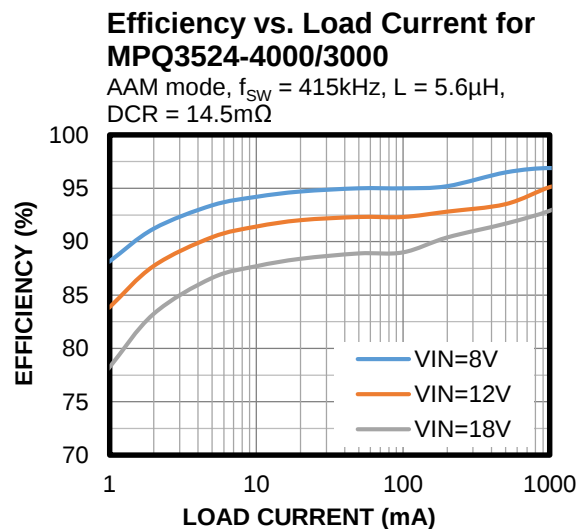
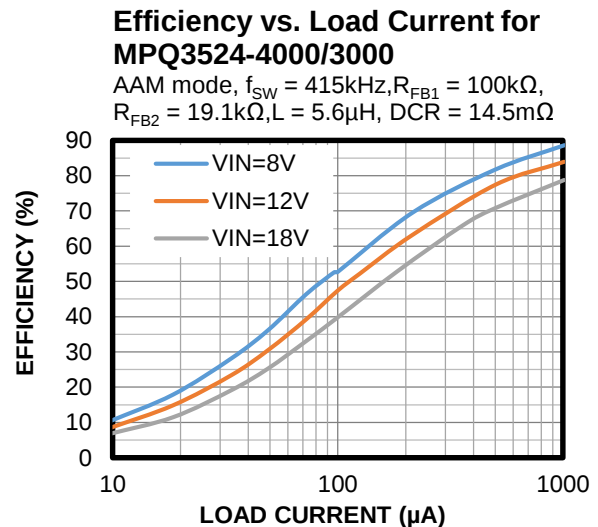
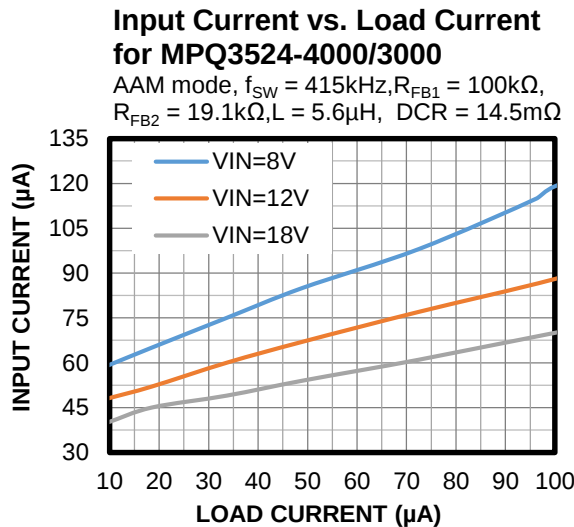
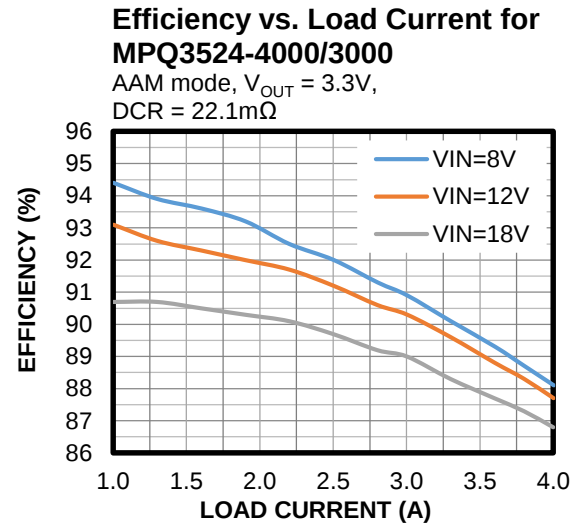
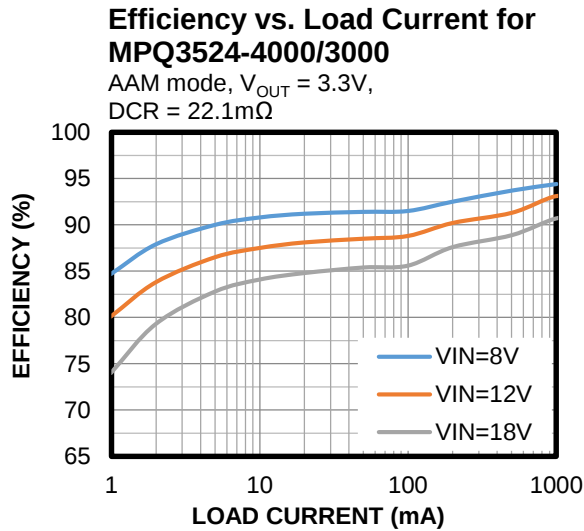
Efficiency vs. Load Current for MPQ3524-4000/3000

AAM mode, DCR = 22.1m Ω



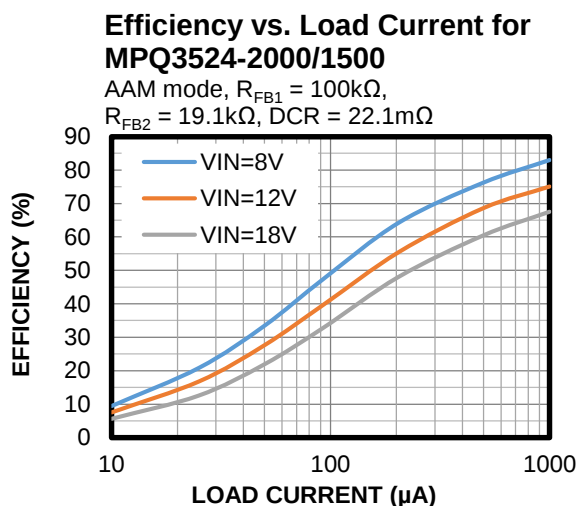
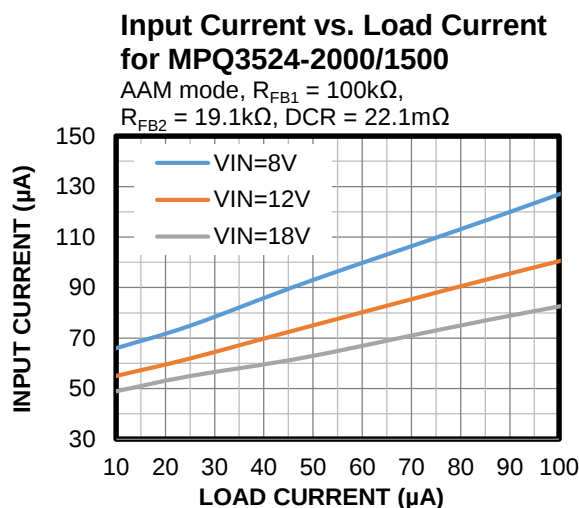
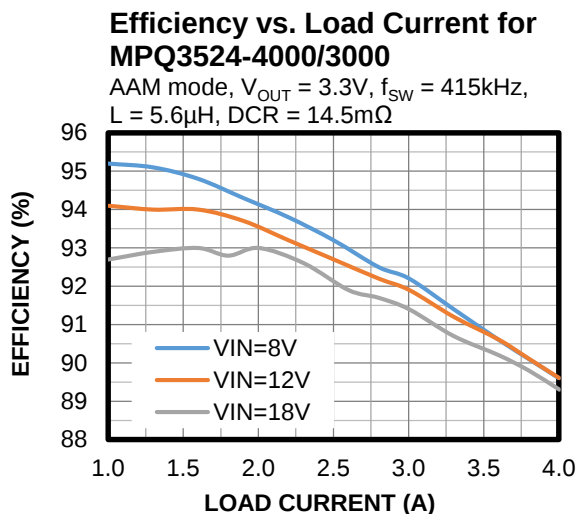
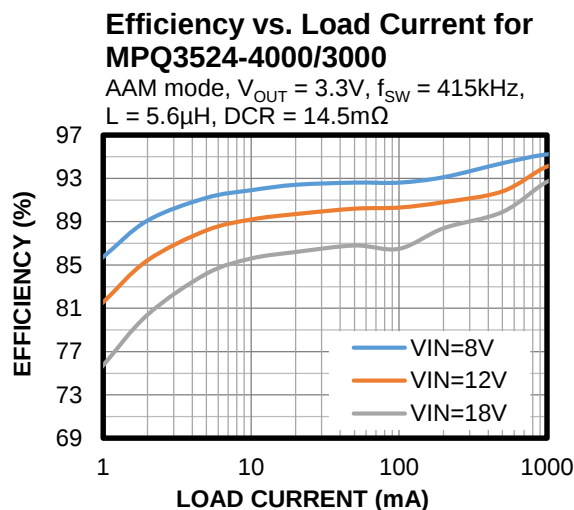
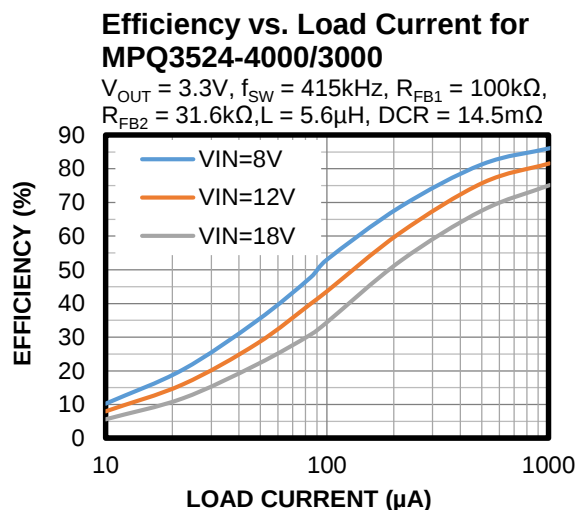
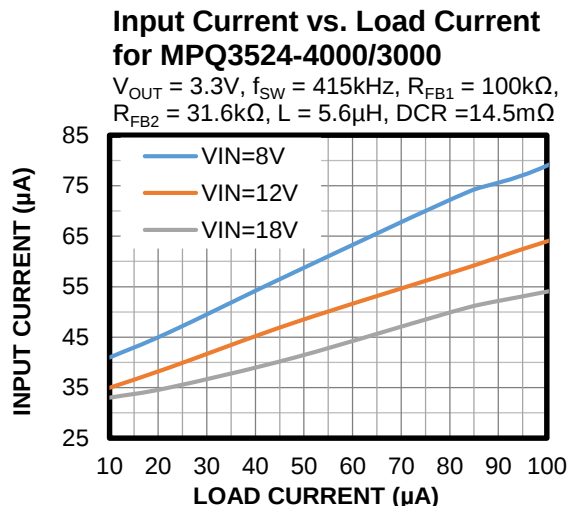
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 2.2μH, C_{OUT} = 2 x 22μF, T_A = 25°C, unless otherwise noted.



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 2.2μH, C_{OUT} = 2 x 22μF, T_A = 25°C, unless otherwise noted.

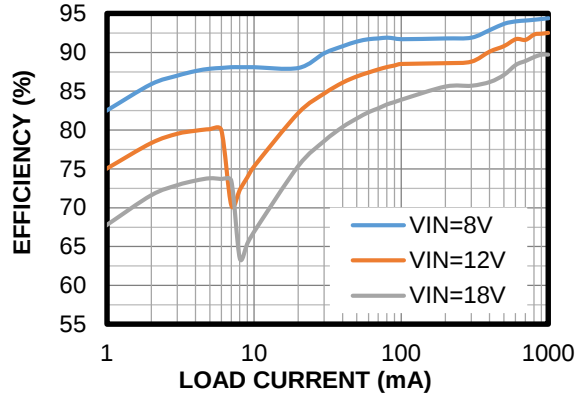


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN} = 12V$, $V_{OUT} = 5V$, $f_{SW} = 2.2MHz$, $L = 2.2\mu H$, $C_{OUT} = 2 \times 22\mu F$, $T_A = 25^\circ C$, unless otherwise noted.

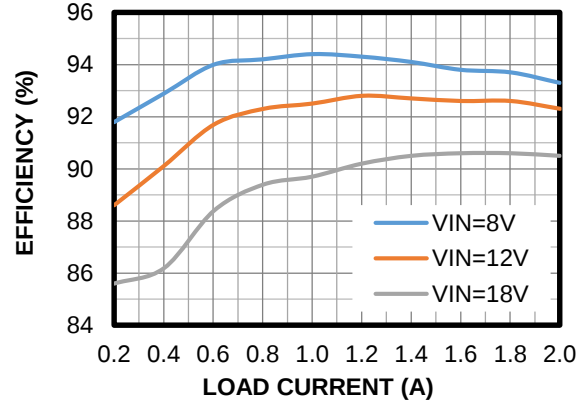
Efficiency vs. Load Current for MPQ3524-2000/1500

AAM mode, DCR = 22.1m Ω



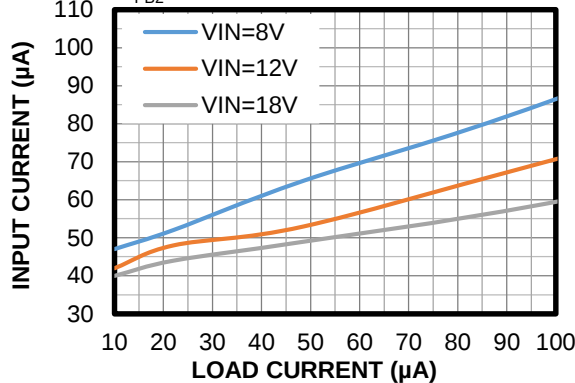
Efficiency vs. Load Current for MPQ3524-2000/1500

AAM mode, DCR = 22.1m Ω



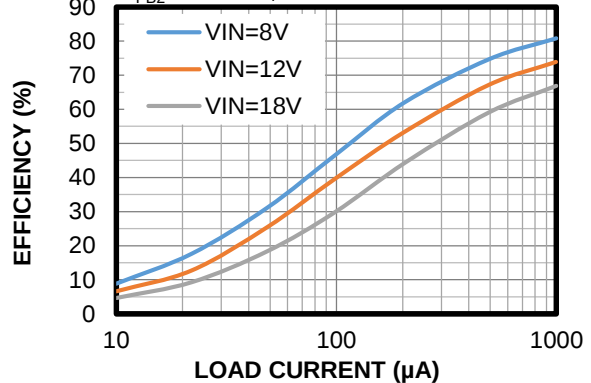
Input Current vs. Load Current for MPQ3524-2000/1500

AAM mode, $V_{OUT} = 3.3V$, $R_{FB1} = 100k\Omega$, $R_{FB2} = 31.6k\Omega$, DCR = 22.1m Ω



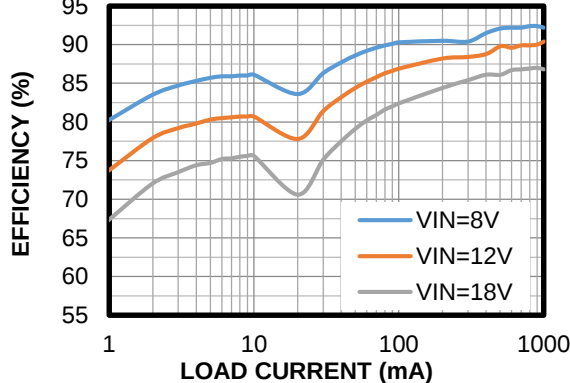
Efficiency vs. Load Current for MPQ3524-2000/1500

AAM mode, $V_{OUT} = 3.3V$, $R_{FB1} = 100k\Omega$, $R_{FB2} = 31.6k\Omega$, DCR = 22.1m Ω



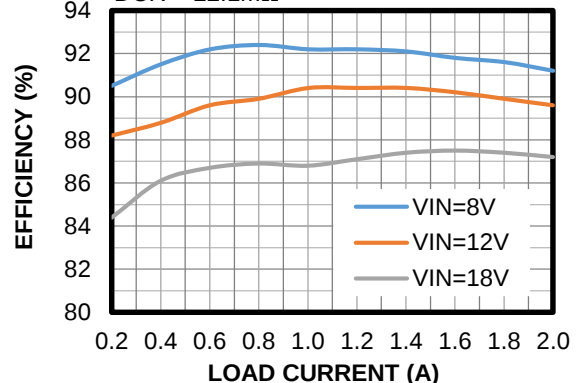
Efficiency vs. Load Current for MPQ3524-2000/1500

AAM mode, $V_{OUT} = 3.3V$, DCR = 22.1m Ω



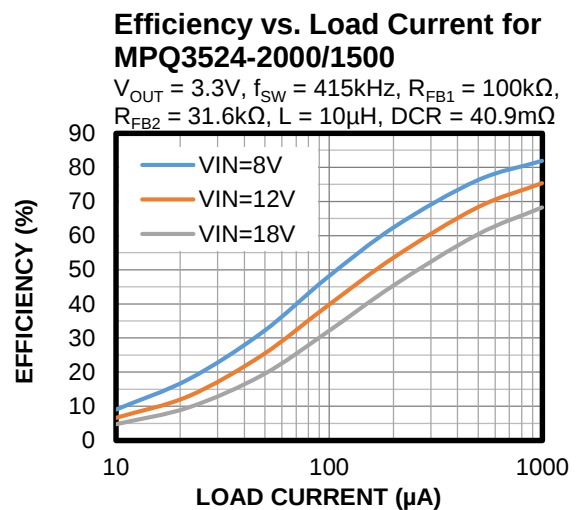
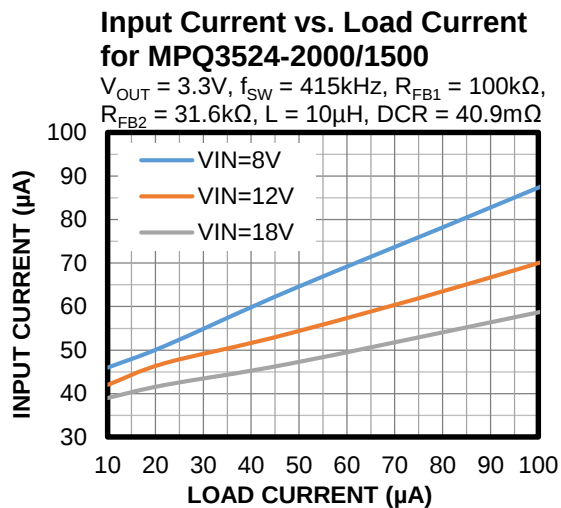
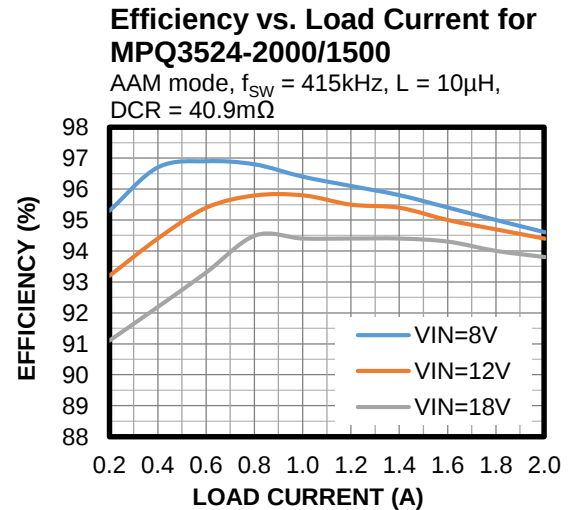
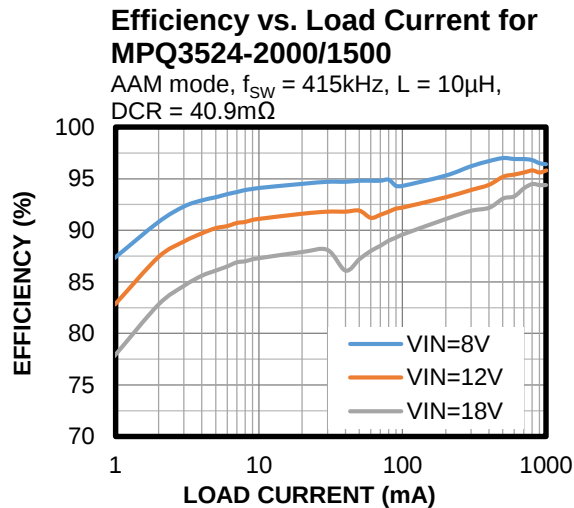
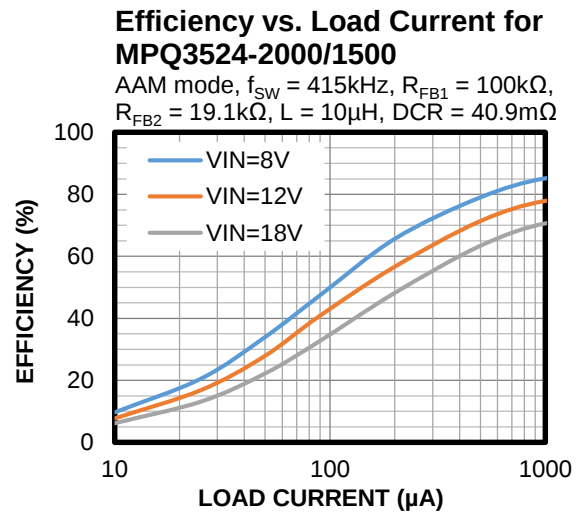
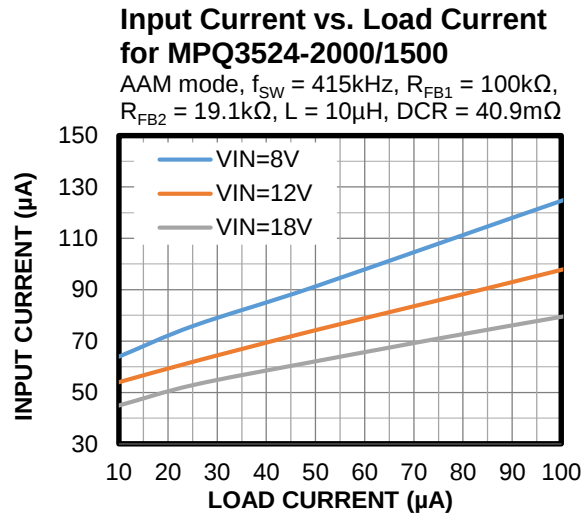
Efficiency vs. Load Current for MPQ3524-2000/1500

AAM mode, $V_{OUT} = 3.3V$, DCR = 22.1m Ω



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN} = 12V$, $V_{OUT} = 5V$, $f_{SW} = 2.2MHz$, $L = 2.2\mu H$, $C_{OUT} = 2 \times 22\mu F$, $T_A = 25^\circ C$, unless otherwise noted.

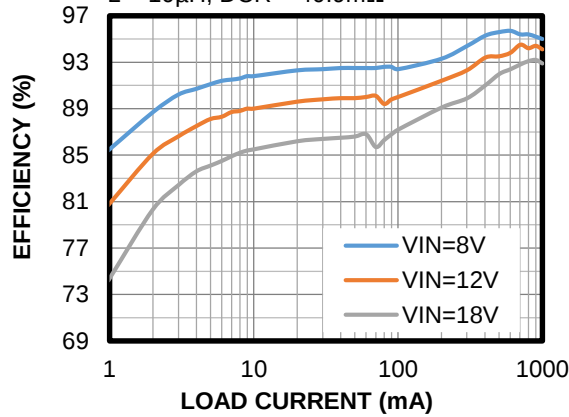


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN} = 12V$, $V_{OUT} = 5V$, $f_{SW} = 2.2MHz$, $L = 2.2\mu H$, $C_{OUT} = 2 \times 22\mu F$, $T_A = 25^\circ C$, unless otherwise noted.

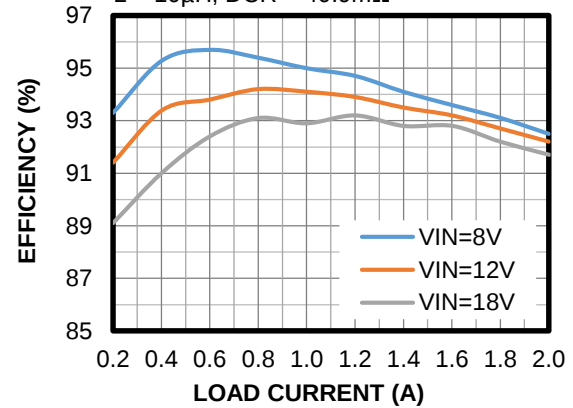
Efficiency vs. Load Current for MPQ3524-2000/1500

AAM mode, $V_{OUT} = 3.3V$, $f_{SW} = 415kHz$,
 $L = 10\mu H$, $DCR = 40.9m\Omega$



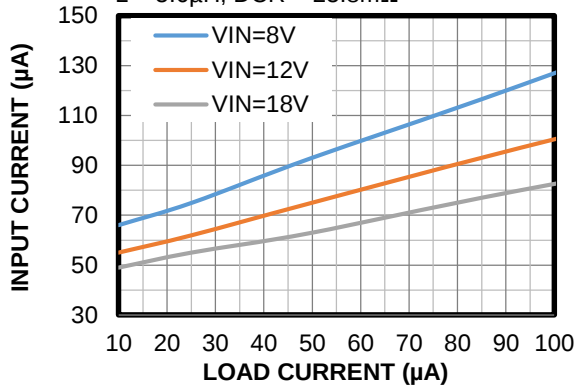
Efficiency vs. Load Current for MPQ3524-2000/1500

AAM mode, $V_{OUT} = 3.3V$, $f_{SW} = 415kHz$,
 $L = 10\mu H$, $DCR = 40.9m\Omega$



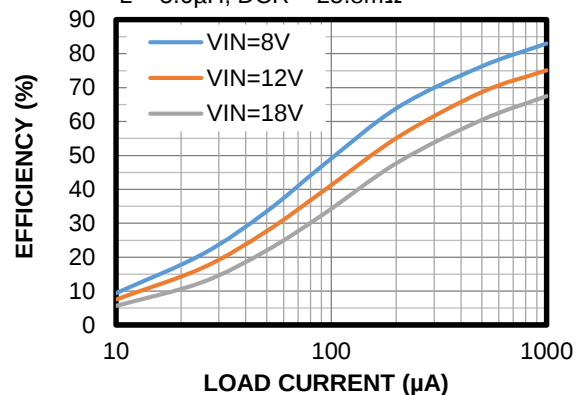
Input Current vs. Load Current for MPQ3524-1000/0500

AAM mode, $R_{FB1} = 100k\Omega$, $R_{FB2} = 19.1k\Omega$,
 $L = 5.6\mu H$, $DCR = 25.8m\Omega$



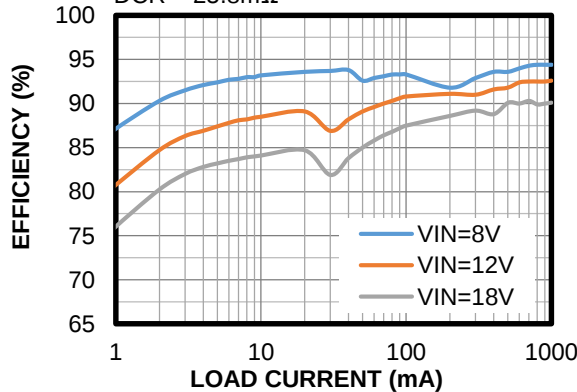
Efficiency vs. Load Current for MPQ3524-1000/0500

AAM mode, $R_{FB1} = 100k\Omega$, $R_{FB2} = 19.1k\Omega$,
 $L = 5.6\mu H$, $DCR = 25.8m\Omega$



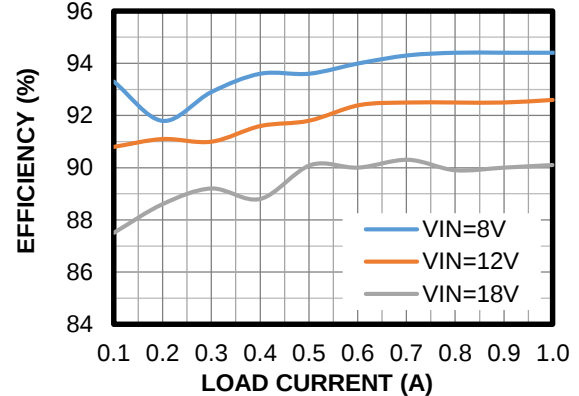
Efficiency vs. Load Current for MPQ3524-1000/0500

AAM mode, $L = 5.6\mu H$,
 $DCR = 25.8m\Omega$



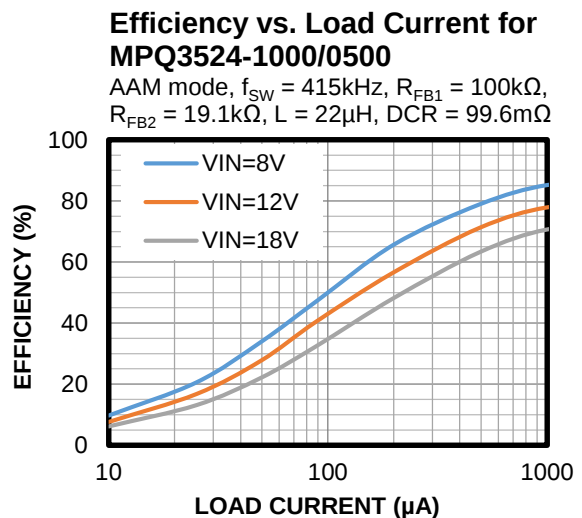
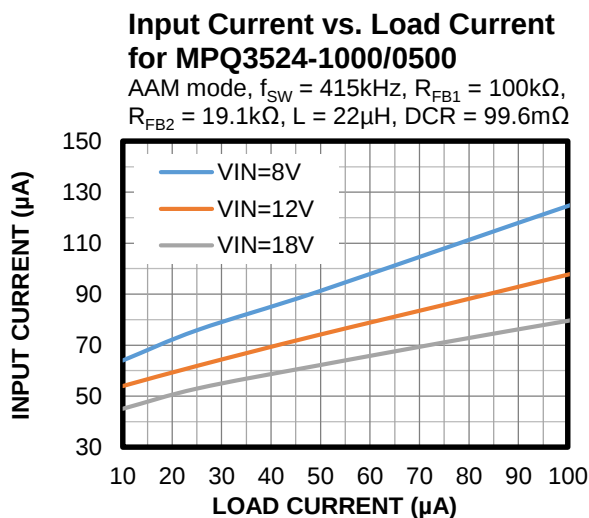
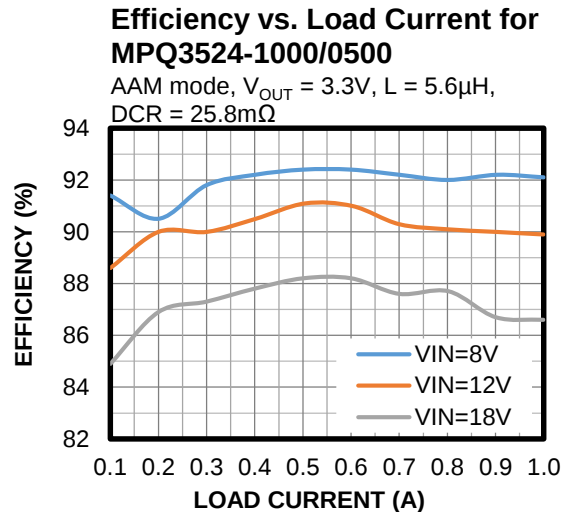
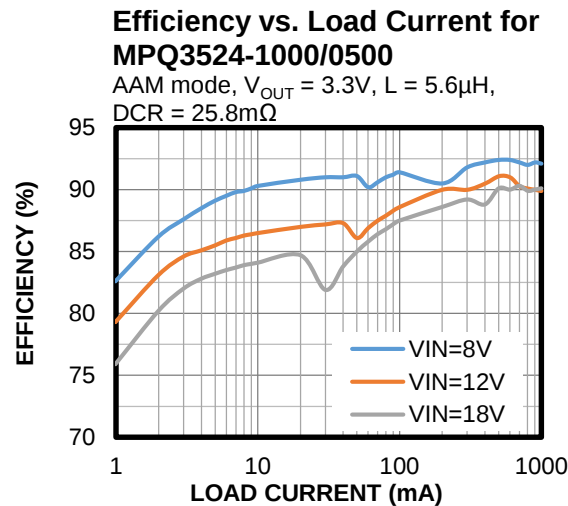
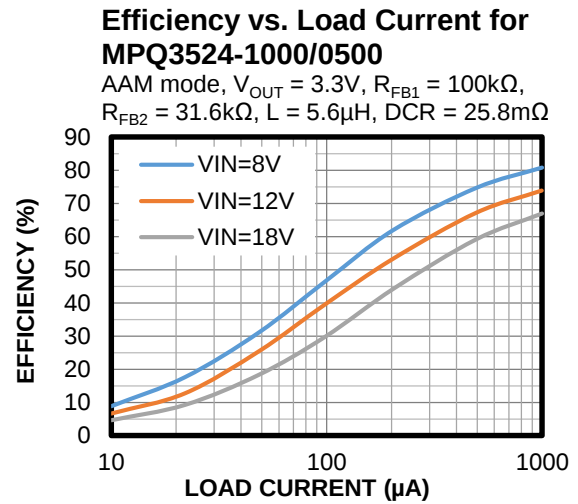
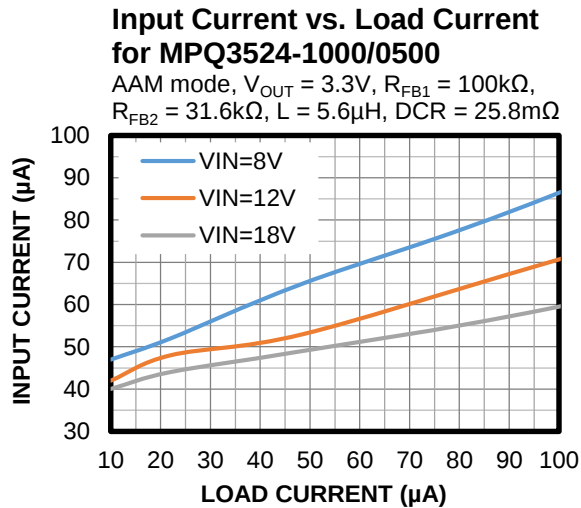
Efficiency vs. Load Current for MPQ3524-1000/0500

AAM mode, $L = 5.6\mu H$,
 $DCR = 25.8m\Omega$



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN} = 12V$, $V_{OUT} = 5V$, $f_{SW} = 2.2MHz$, $L = 2.2\mu H$, $C_{OUT} = 2 \times 22\mu F$, $T_A = 25^\circ C$, unless otherwise noted.

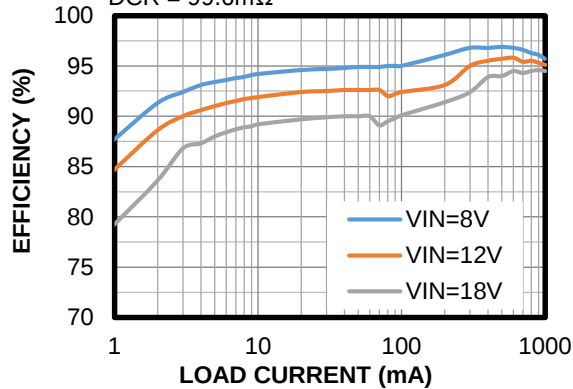


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN} = 12V$, $V_{OUT} = 5V$, $f_{SW} = 2.2MHz$, $L = 2.2\mu H$, $C_{OUT} = 2 \times 22\mu F$, $T_A = 25^\circ C$, unless otherwise noted.

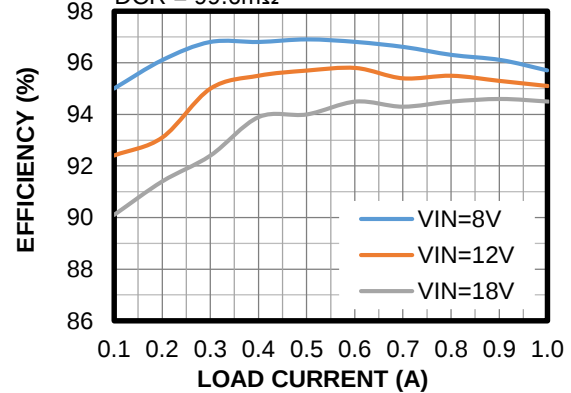
Efficiency vs. Load Current for MPQ3524-1000/0500

AAM mode, $f_{SW} = 415kHz$, $L = 22\mu H$,
DCR = 99.6m Ω



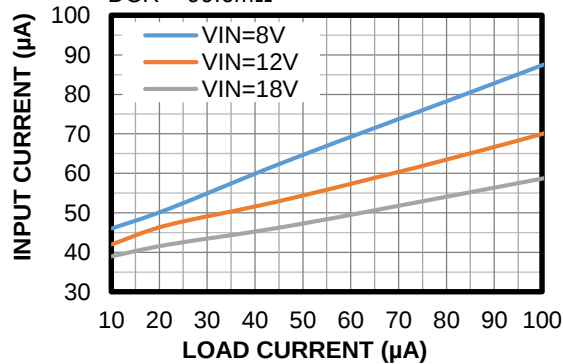
Efficiency vs. Load Current for MPQ3524-1000/0500

AAM mode, $f_{SW} = 415kHz$, $L = 22\mu H$,
DCR = 99.6m Ω



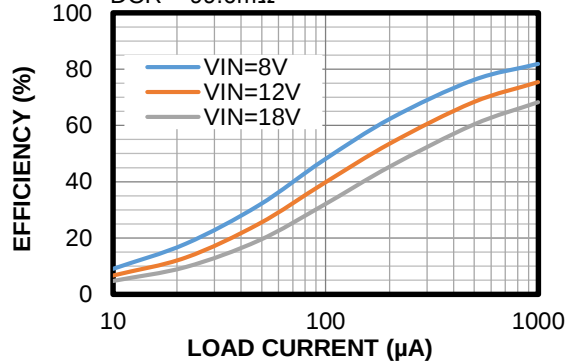
Input Current vs. Load Current for MPQ3524-1000/0500

$V_{OUT} = 3.3V$, $f_{SW} = 415kHz$, $R_{FB1} = 100k\Omega$,
 $R_{FB2} = 31.6k\Omega$, $L = 22\mu H$,
DCR = 99.6m Ω



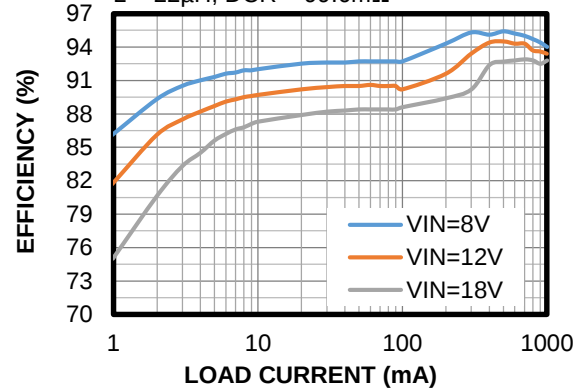
Efficiency vs. Load Current for MPQ3524-1000/0500

$V_{OUT} = 3.3V$, $f_{SW} = 415kHz$,
 $R_{FB1} = 100k\Omega$, $R_{FB2} = 31.6k\Omega$, $L = 22\mu H$,
DCR = 99.6m Ω



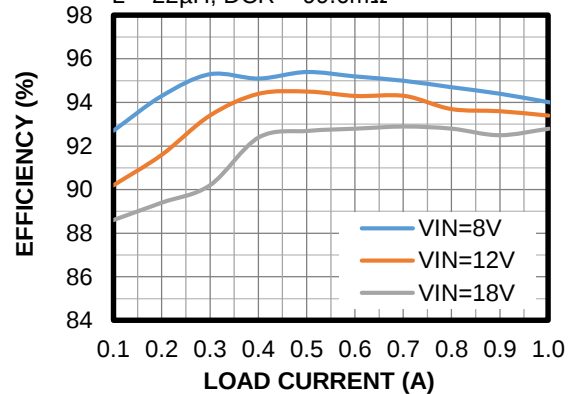
Efficiency vs. Load Current for MPQ3524-1000/0500

AAM mode, $V_{OUT} = 3.3V$, $f_{SW} = 415kHz$,
 $L = 22\mu H$, DCR = 99.6m Ω



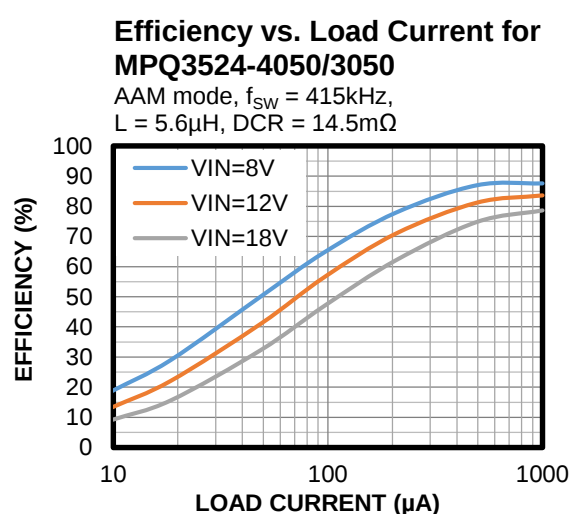
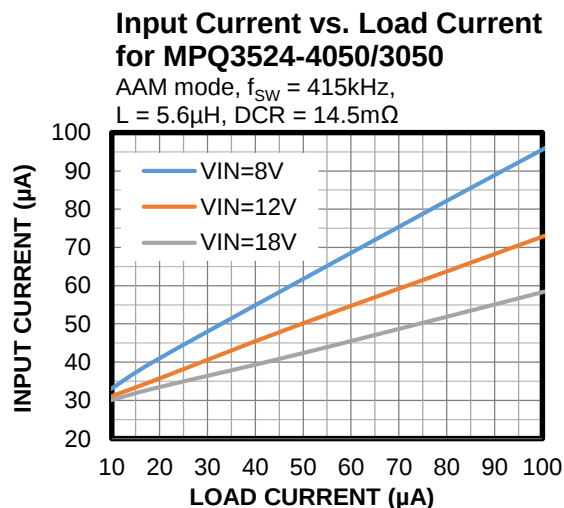
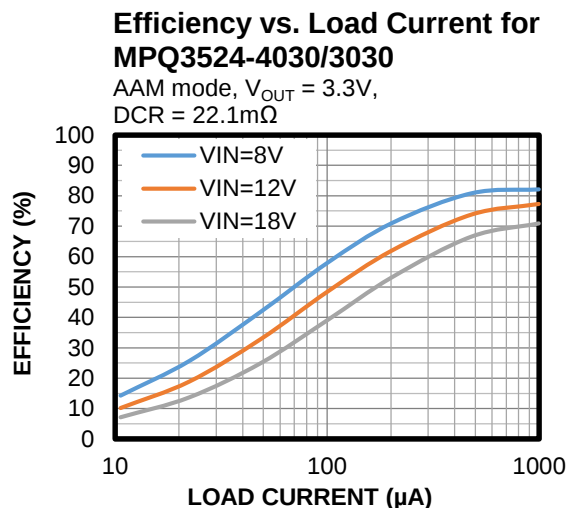
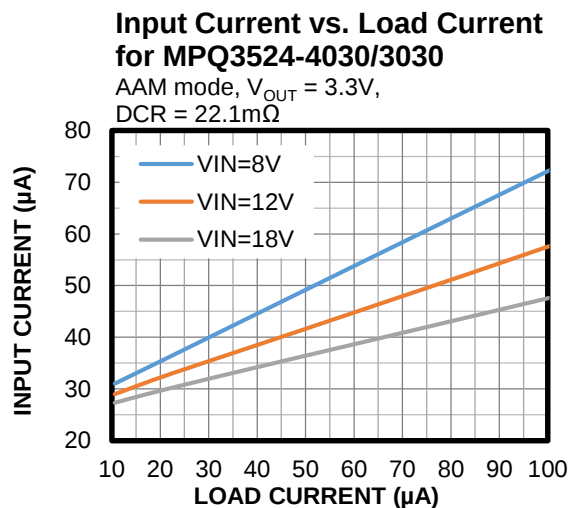
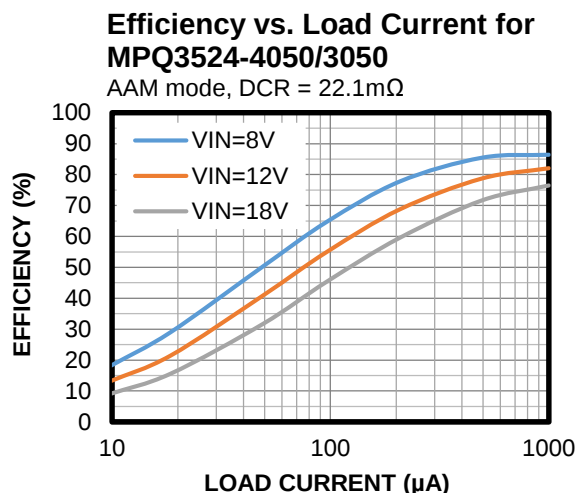
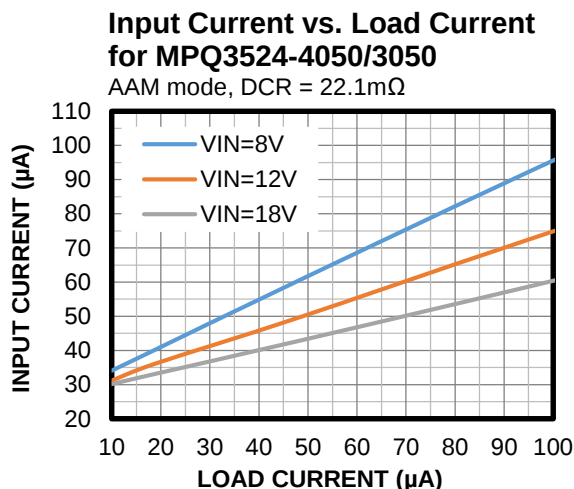
Efficiency vs. Load Current for MPQ3524-1000/0500

AAM mode, $V_{OUT} = 3.3V$, $f_{SW} = 415kHz$,
 $L = 22\mu H$, DCR = 99.6m Ω



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN} = 12V$, $V_{OUT} = 5V$, $f_{SW} = 2.2MHz$, $L = 2.2\mu H$, $C_{OUT} = 2 \times 22\mu F$, $T_A = 25^\circ C$, unless otherwise noted.

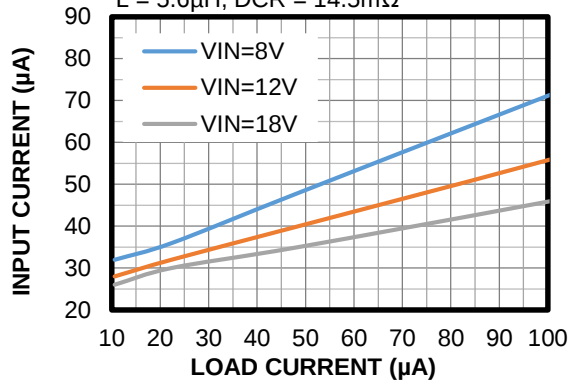


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 2.2μH, C_{OUT} = 2 x 22μF, T_A = 25°C, unless otherwise noted.

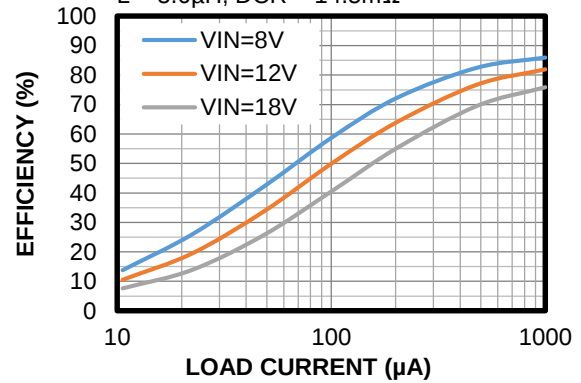
Input Current vs. Load Current for MPQ3524-4030/3030

AAM mode, V_{OUT} = 3.3V, f_{SW} = 415kHz, L = 5.6μH, DCR = 14.5mΩ



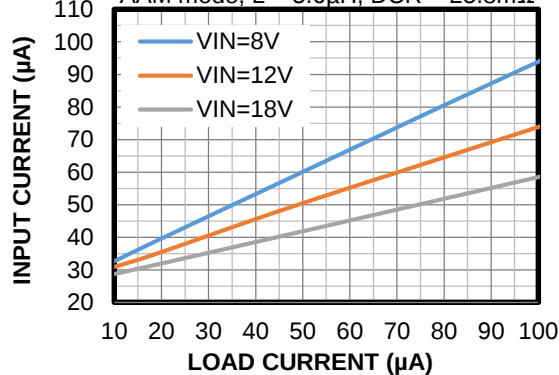
Efficiency vs. Load Current for MPQ3524-4030/3030

AAM mode, V_{OUT} = 3.3V, f_{SW} = 415kHz, L = 5.6μH, DCR = 14.5mΩ



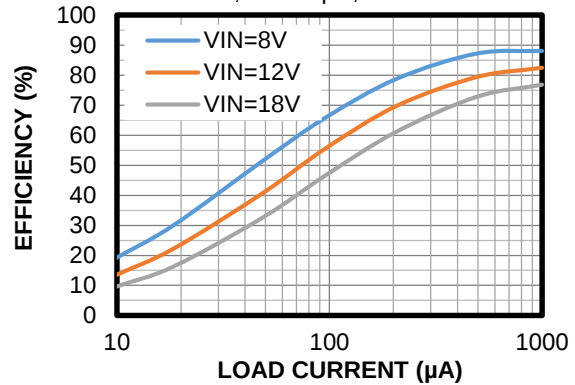
Input Current vs. Load Current for MPQ3524-2050/1550/1050/0550

AAM mode, L = 5.6μH, DCR = 25.8mΩ



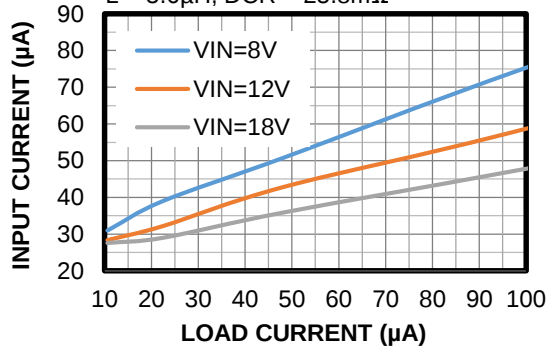
Efficiency vs. Load Current for MPQ3524-2050/1550/1050/0550

AAM mode, L = 5.6μH, DCR = 25.8mΩ



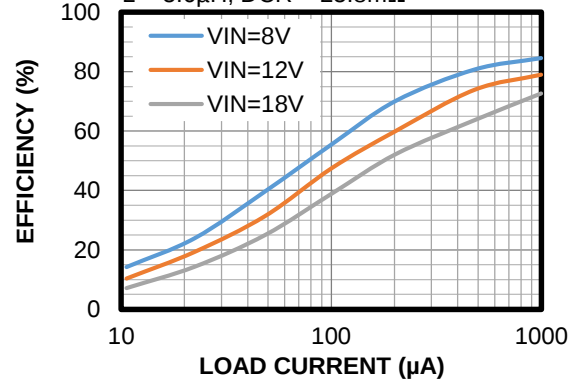
Input Current vs. Load Current for MPQ3524-2030/1530/1030/0530

AAM mode, V_{OUT} = 3.3V, L = 5.6μH, DCR = 25.8mΩ



Efficiency vs. Load Current for MPQ3524-2030/1530/1030/0530

AAM mode, V_{OUT} = 3.3V, L = 5.6μH, DCR = 25.8mΩ

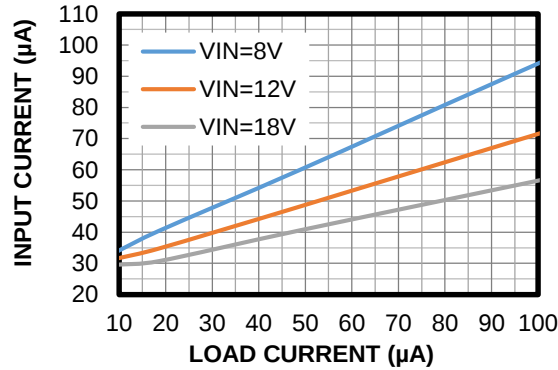


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN} = 12V$, $V_{OUT} = 5V$, $f_{SW} = 2.2MHz$, $L = 2.2\mu H$, $C_{OUT} = 2 \times 22\mu F$, $T_A = 25^\circ C$, unless otherwise noted.

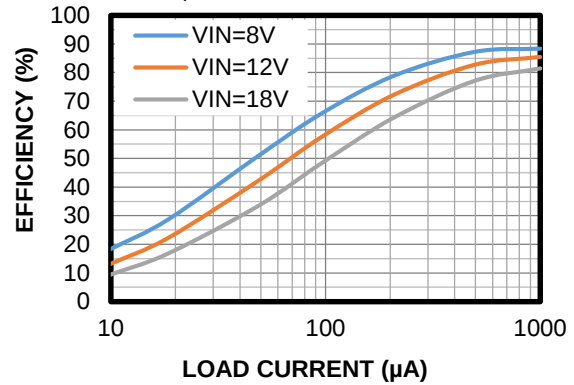
**Input Current vs. Load Current
for MPQ3524-
2050/1550/1050/0550**

AAM mode, $f_{SW} = 415kHz$,
 $L = 22\mu H$, $DCR = 99.6m\Omega$



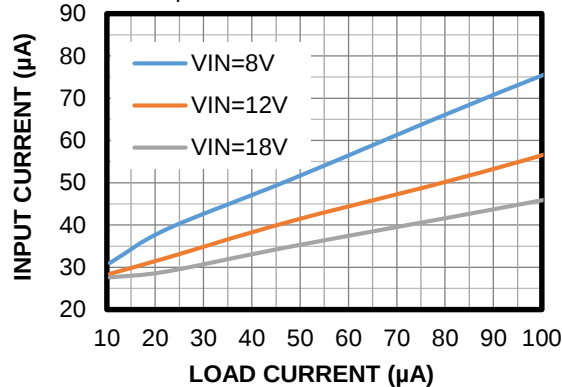
**Efficiency vs. Load Current for
MPQ3524-2050/1550/1050/0550**

AAM mode, $f_{SW} = 415kHz$,
 $L = 22\mu H$, $DCR = 99.6m\Omega$



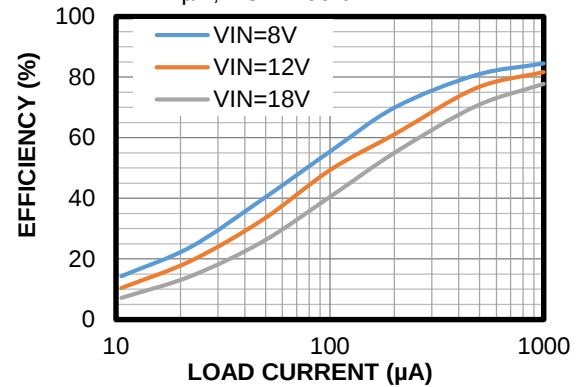
**Input Current vs. Load Current
for MPQ3524-030/1530/
1030/0530**

AAM mode, $f_{SW} = 415kHz$, $V_{OUT} = 3.3V$,
 $L = 22\mu H$, $DCR = 99.6m\Omega$



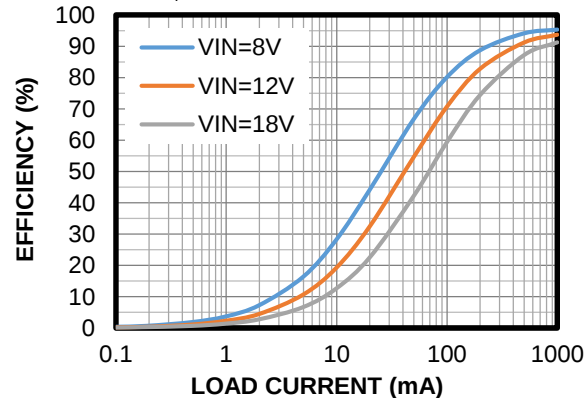
**Efficiency vs. Load Current for
MPQ3524-2030/1530/
1030/0530**

AAM mode, $f_{SW} = 415kHz$, $V_{OUT} = 3.3V$,
 $L = 22\mu H$, $DCR = 99.6m\Omega$



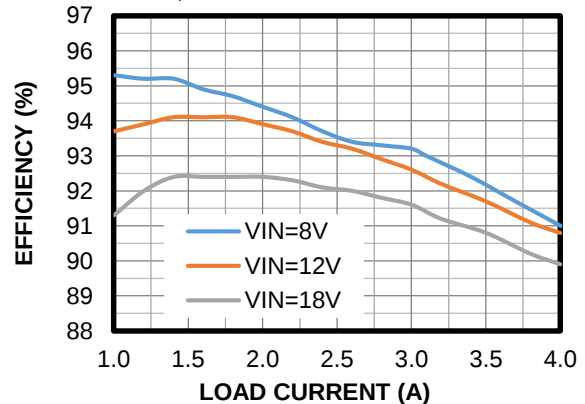
**Efficiency vs. Load Current for
MPQ3524-4001/3001**

FCCM, $DCR = 22.1m\Omega$



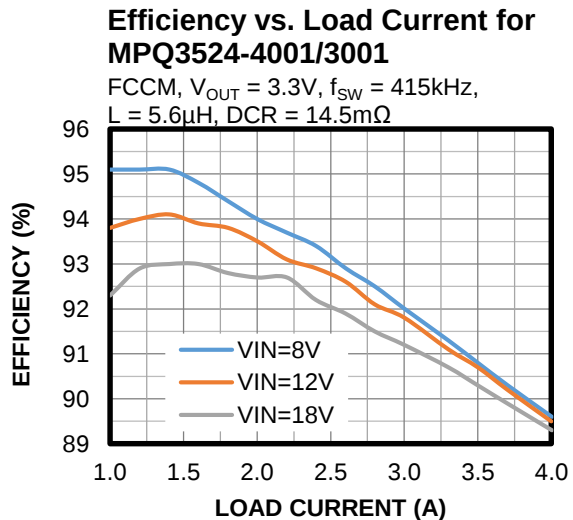
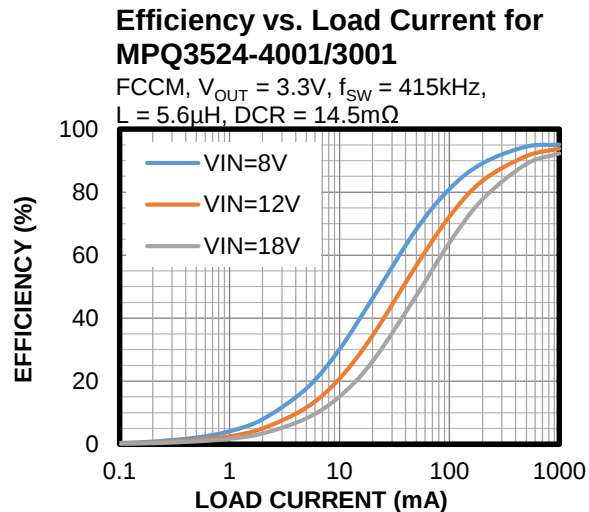
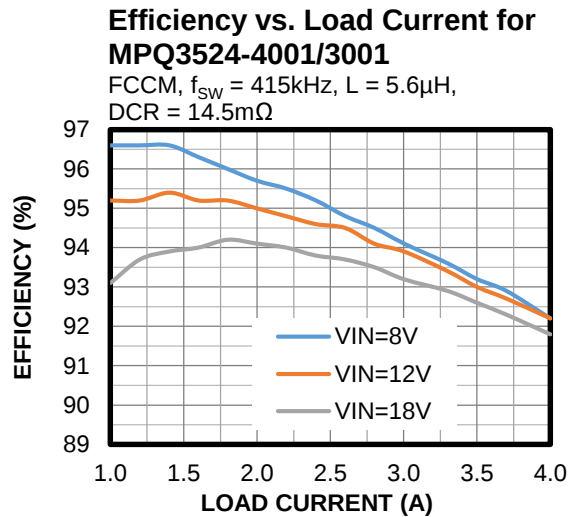
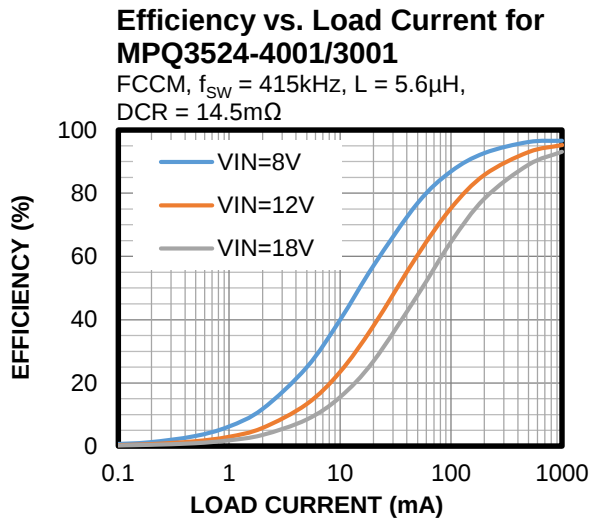
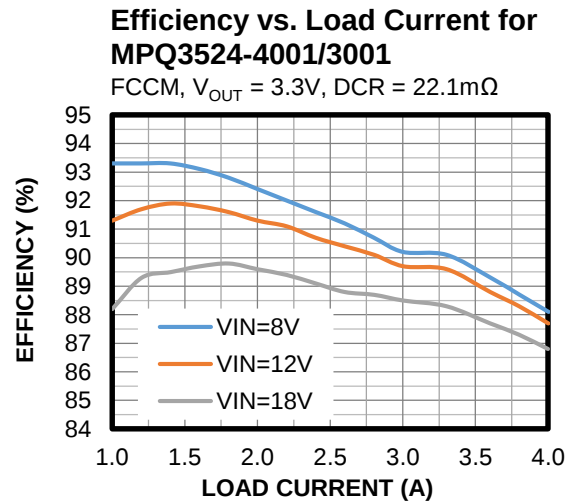
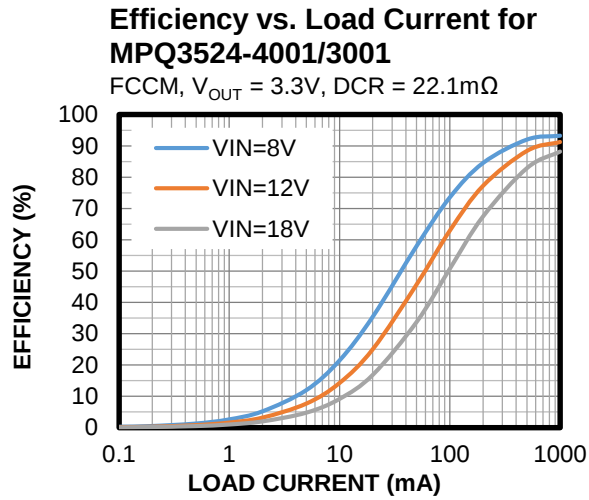
**Efficiency vs. Load Current for
MPQ3524-4001/3001**

FCCM, $DCR = 22.1m\Omega$



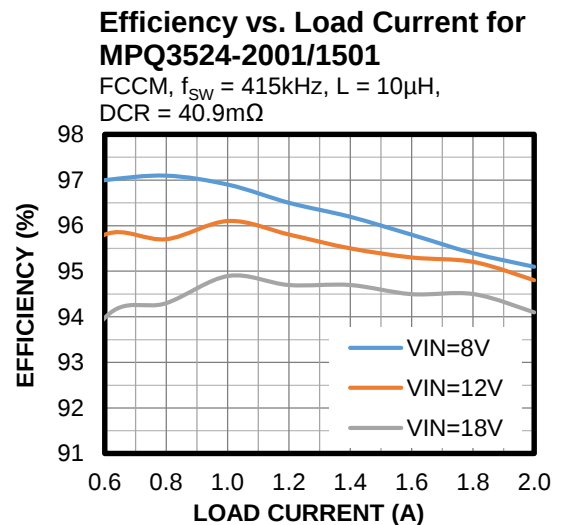
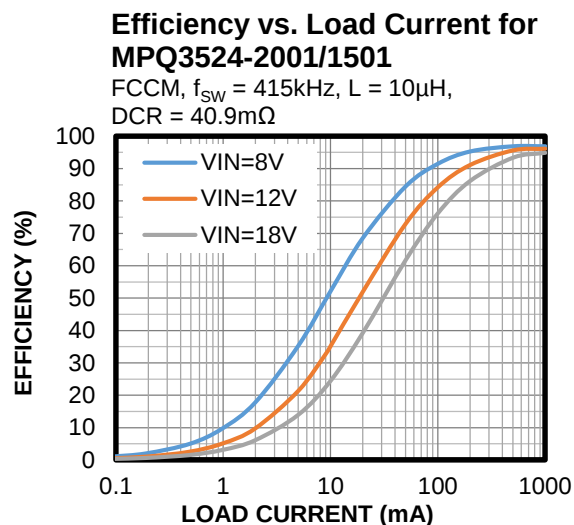
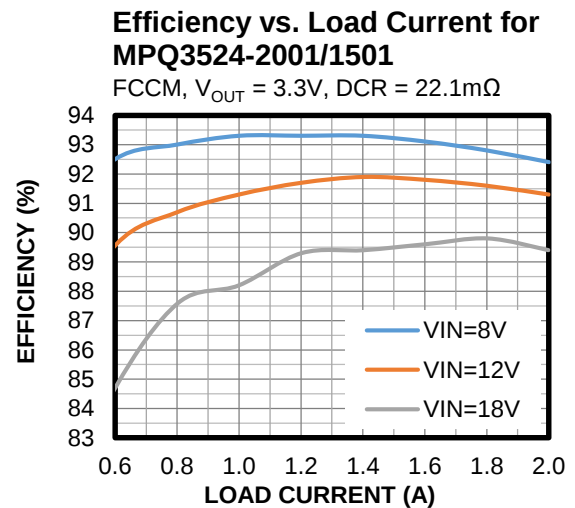
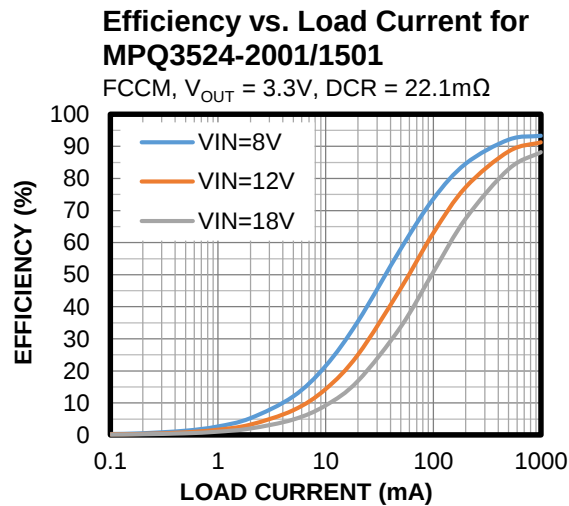
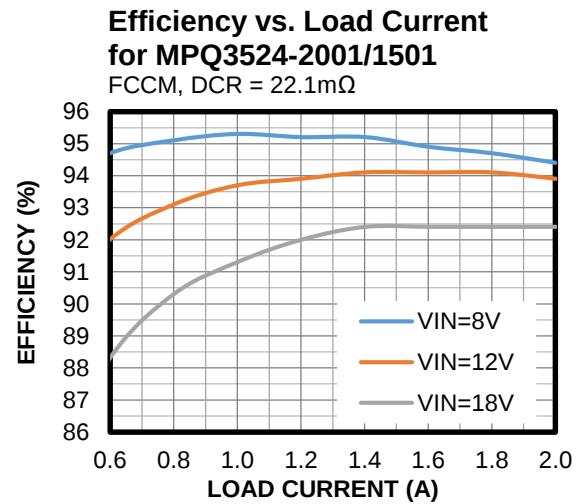
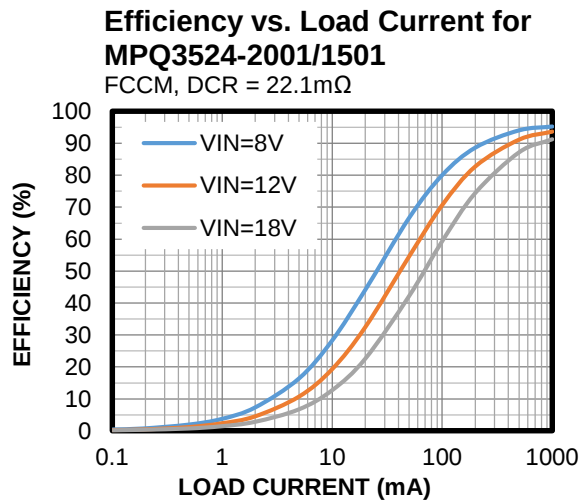
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 2.2μH, C_{OUT} = 2 x 22μF, T_A = 25°C, unless otherwise noted.



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 2.2μH, C_{OUT} = 2 x 22μF, T_A = 25°C, unless otherwise noted.

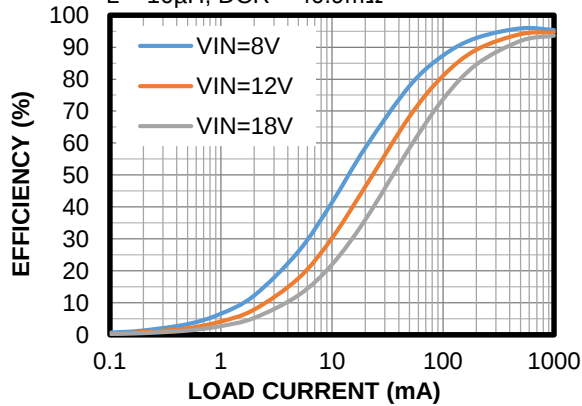


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN} = 12V$, $V_{OUT} = 5V$, $f_{SW} = 2.2MHz$, $L = 2.2\mu H$, $C_{OUT} = 2 \times 22\mu F$, $T_A = 25^\circ C$, unless otherwise noted.

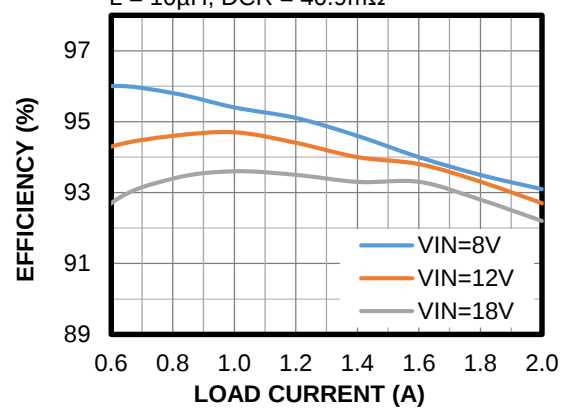
Efficiency vs. Load Current for MPQ3524-2001/1501

FCCM, $V_{OUT} = 3.3V$, $f_{SW} = 415kHz$,
 $L = 10\mu H$, $DCR = 40.9m\Omega$



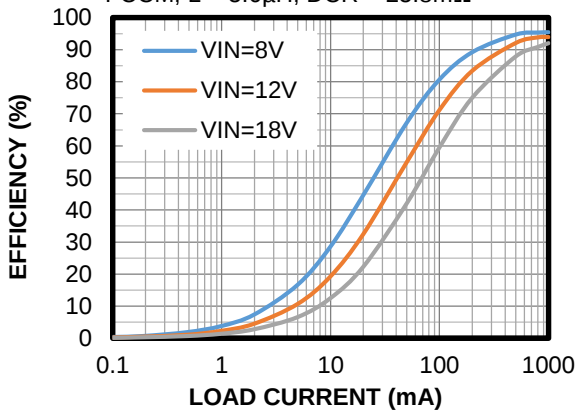
Efficiency vs. Load Current for MPQ3524-2001/1501

FCCM, $V_{OUT} = 3.3V$, $f_{SW} = 415kHz$,
 $L = 10\mu H$, $DCR = 40.9m\Omega$



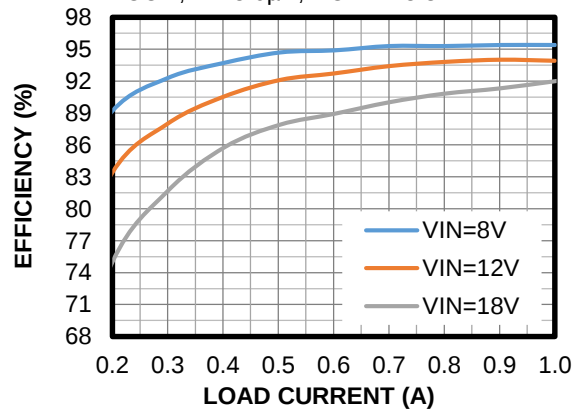
Efficiency vs. Load Current for MPQ3524-1001/0501

FCCM, $L = 5.6\mu H$, $DCR = 25.8m\Omega$



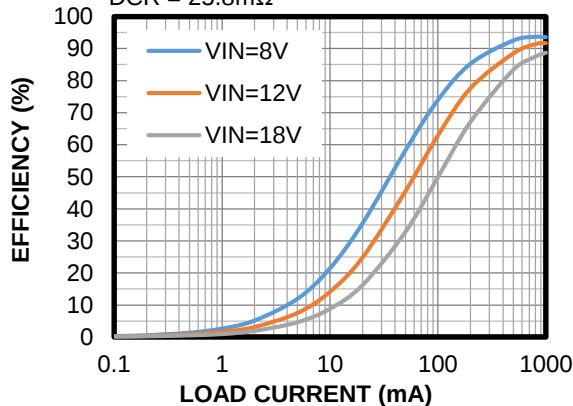
Efficiency vs. Load Current for MPQ3524-1001/0501

FCCM, $L = 5.6\mu H$, $DCR = 25.8m\Omega$



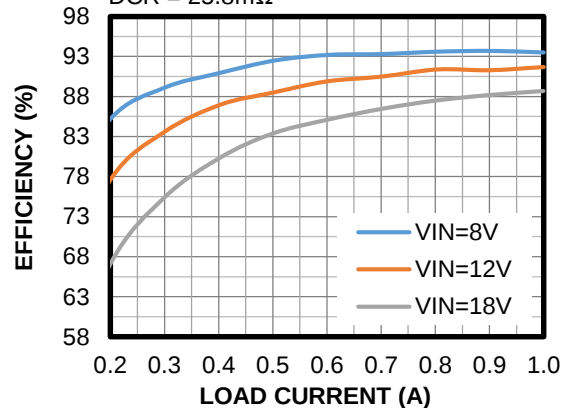
Efficiency vs. Load Current for MPQ3524-1001/0501

FCCM, $V_{OUT} = 3.3V$, $L = 5.6\mu H$,
 $DCR = 25.8m\Omega$



Efficiency vs. Load Current for MPQ3524-1001/0501

FCCM, $V_{OUT} = 3.3V$, $L = 5.6\mu H$,
 $DCR = 25.8m\Omega$

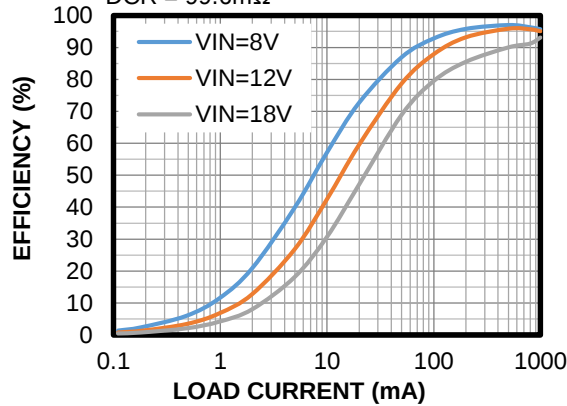


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 2.2μH, C_{OUT} = 2 x 22μF, T_A = 25°C, unless otherwise noted.

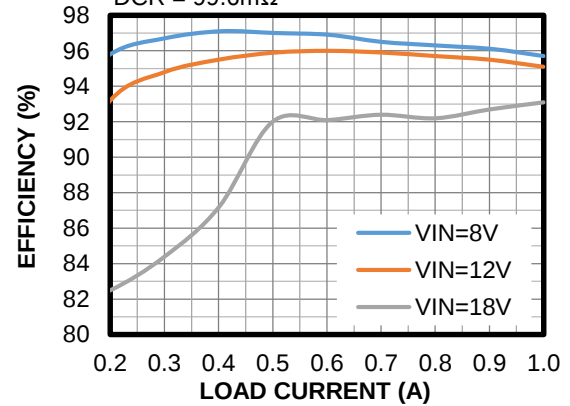
Efficiency vs. Load Current for MPQ3524-1001/0501

FCCM, f_{SW} = 415kHz, L = 22μH, DCR = 99.6mΩ



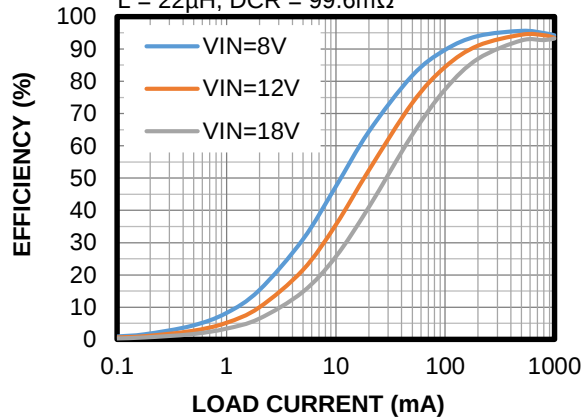
Efficiency vs. Load Current for MPQ3524-1001/0501

FCCM, f_{SW} = 415kHz, L = 22μH, DCR = 99.6mΩ



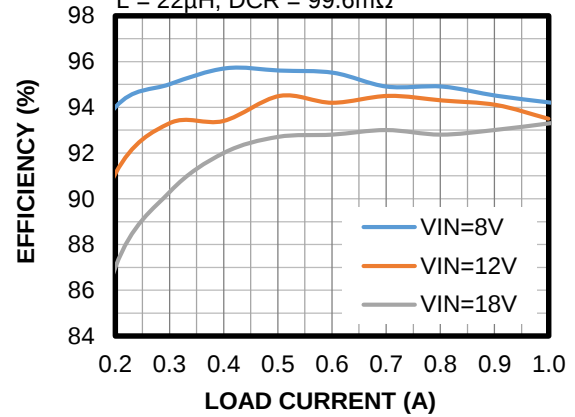
Efficiency vs. Load Current for MPQ3524-1001/0501

FCCM, V_{OUT} = 3.3V, f_{SW} = 415kHz, L = 22μH, DCR = 99.6mΩ



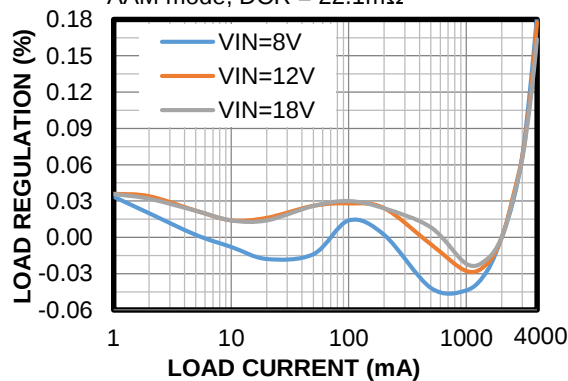
Efficiency vs. Load Current for MPQ3524-1001/0501

FCCM, V_{OUT} = 3.3V, f_{SW} = 415kHz, L = 22μH, DCR = 99.6mΩ



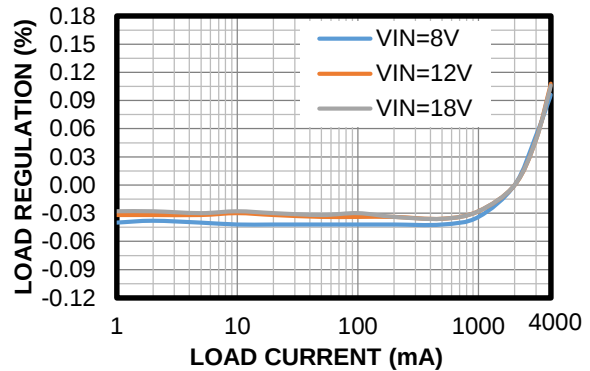
Load Regulation for MPQ3524-4000

AAM mode, DCR = 22.1mΩ



Load Regulation for MPQ3524-4001

FCCM, DCR = 22.1mΩ

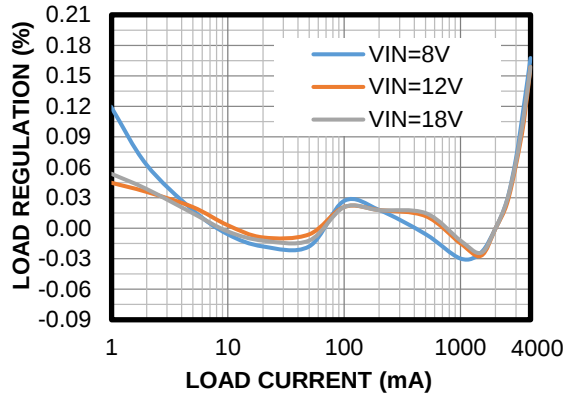


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN} = 12V$, $V_{OUT} = 5V$, $f_{SW} = 2.2MHz$, $L = 2.2\mu H$, $C_{OUT} = 2 \times 22\mu F$, $T_A = 25^\circ C$, unless otherwise noted.

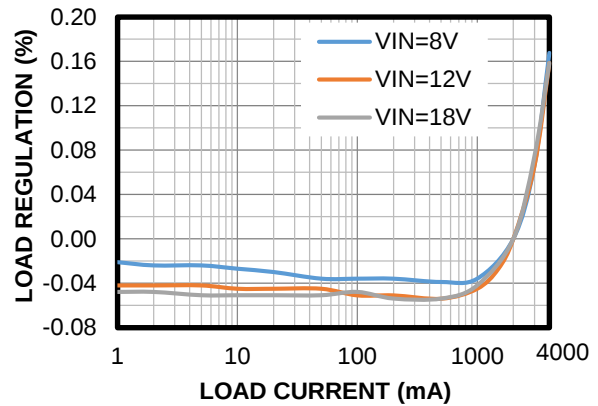
Load Regulation for MPQ3524-4000

AAM mode, $V_{OUT} = 3.3V$,
DCR = 22.1m Ω



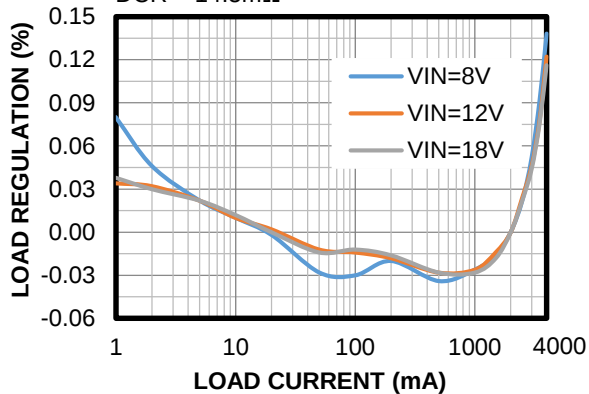
Load Regulation for MPQ3524-4001

FCCM, $V_{OUT} = 3.3V$, DCR = 22.1m Ω



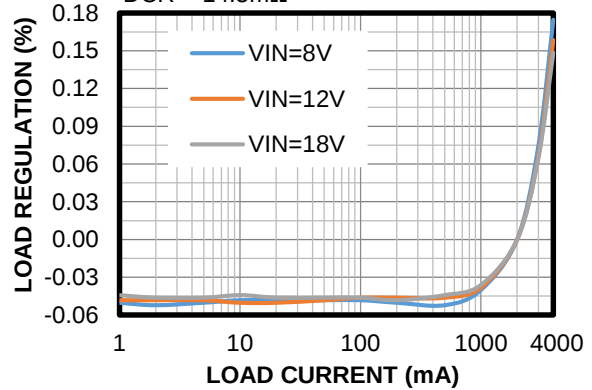
Load Regulation for MPQ3524-4000

AAM mode, $f_{SW} = 415kHz$,
 $C_{OUT} = 2 \times 47\mu F$, $L = 5.6\mu H$,
DCR = 14.5m Ω



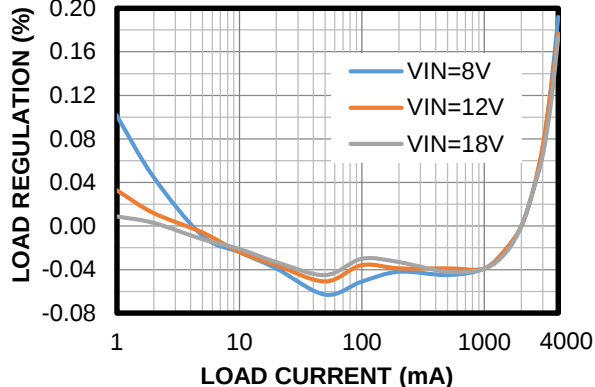
Load Regulation for MPQ3524-4001

FCCM, $f_{SW} = 415kHz$,
 $C_{OUT} = 2 \times 47\mu F$, $L = 5.6\mu H$,
DCR = 14.5m Ω



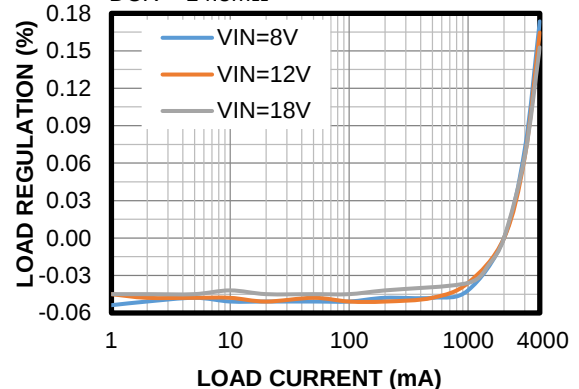
Load Regulation for MPQ3524-4000

AAM mode, $V_{OUT} = 3.3V$, $f_{SW} = 415kHz$,
 $C_{OUT} = 2 \times 47\mu F$, $L = 5.6\mu H$,
DCR = 14.5m Ω



Load Regulation for MPQ3524-4001

FCCM, $V_{OUT} = 3.3V$, $f_{SW} = 415kHz$,
 $C_{OUT} = 2 \times 47\mu F$, $L = 5.6\mu H$,
DCR = 14.5m Ω

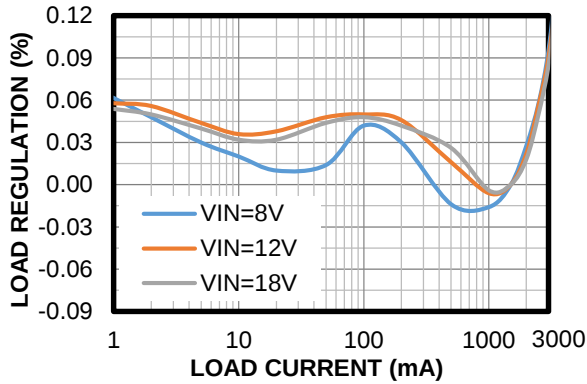


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN} = 12V$, $V_{OUT} = 5V$, $f_{SW} = 2.2MHz$, $L = 2.2\mu H$, $C_{OUT} = 2 \times 22\mu F$, $T_A = 25^\circ C$, unless otherwise noted.

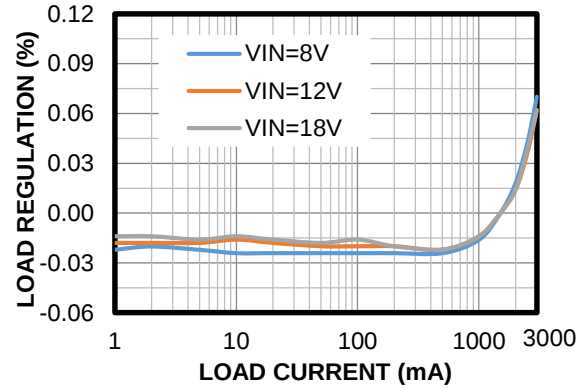
Load Regulation for MPQ3524-3000

AAM mode, DCR = 22.1m Ω



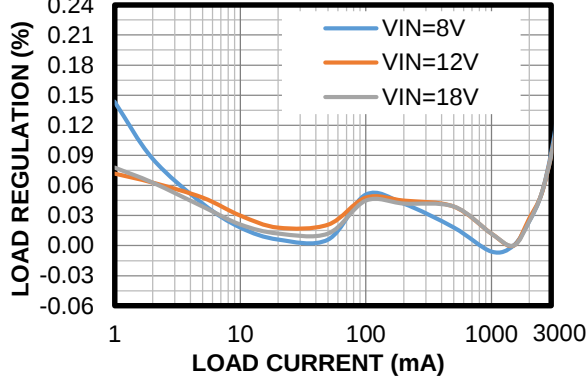
Load Regulation for MPQ3524-3001

FCCM, DCR = 22.1m Ω



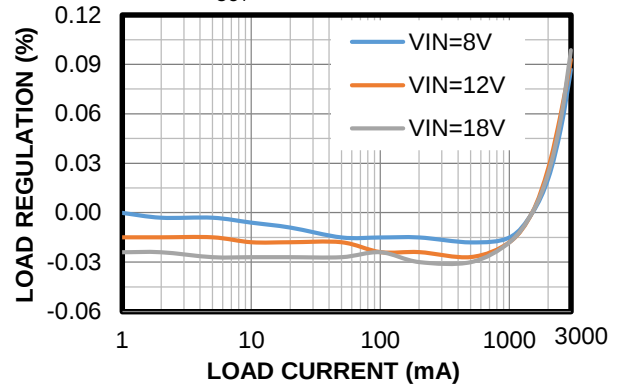
Load Regulation for MPQ3524-3000

AAM mode, $V_{OUT} = 3.3V$,
DCR = 22.1m Ω



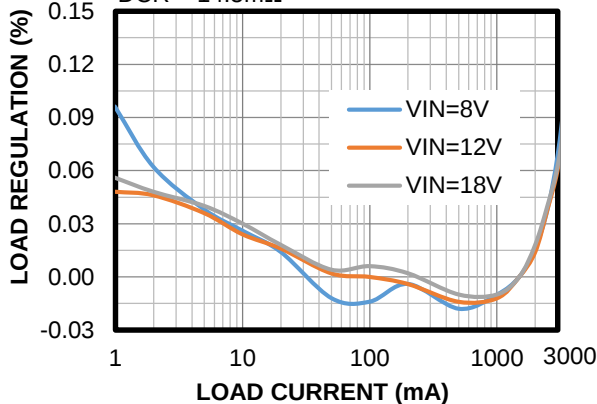
Load Regulation for MPQ3524-3001

FCCM, $V_{OUT} = 3.3V$, DCR = 22.1m Ω



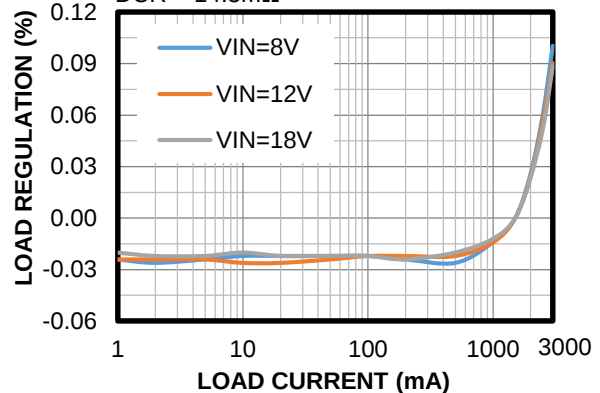
Load Regulation for MPQ3524-3000

AAM mode, $f_{SW} = 415kHz$,
 $C_{OUT} = 2 \times 47\mu F$, $L = 5.6\mu H$,
DCR = 14.5m Ω



Load Regulation for MPQ3524-3001

FCCM, $f_{SW} = 415kHz$,
 $C_{OUT} = 2 \times 47\mu F$, $L = 5.6\mu H$,
DCR = 14.5m Ω

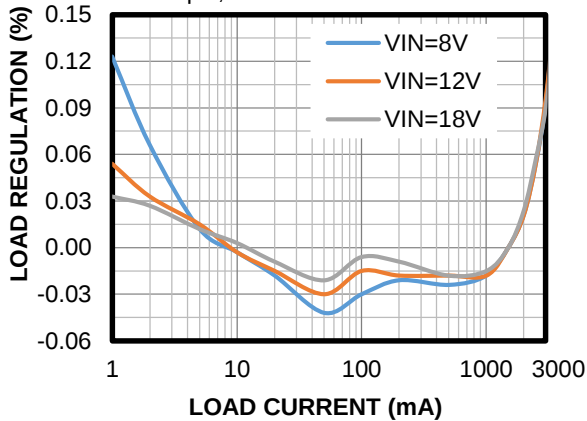


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN} = 12V$, $V_{OUT} = 5V$, $f_{SW} = 2.2MHz$, $L = 2.2\mu H$, $C_{OUT} = 2 \times 22\mu F$, $T_A = 25^\circ C$, unless otherwise noted.

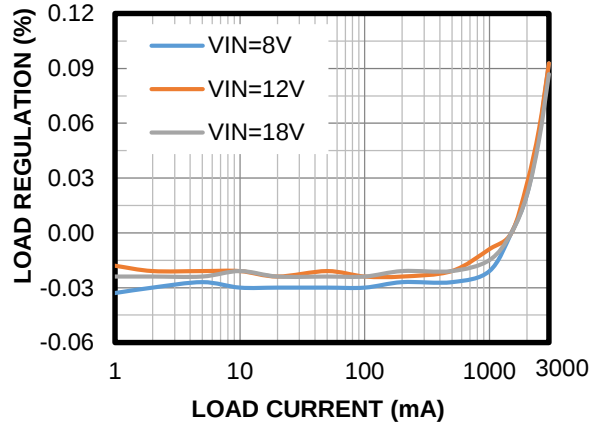
Load Regulation for MPQ3524-3000

AAM mode, $V_{OUT} = 3.3V$,
 $f_{SW} = 415kHz$, $C_{OUT} = 2 \times 47\mu F$,
 $L = 5.6\mu H$, $DCR = 14.5m\Omega$



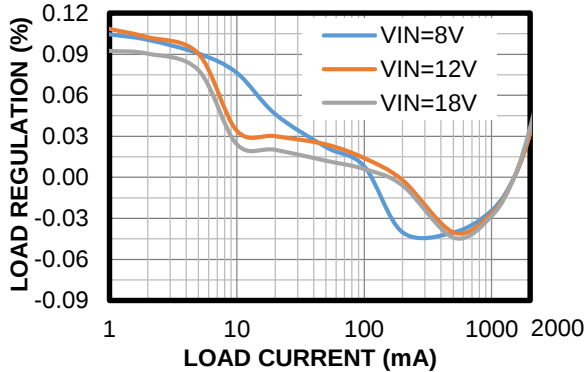
Load Regulation for MPQ3524-3001

FCCM, $V_{OUT} = 3.3V$, $f_{SW} = 415kHz$,
 $C_{OUT} = 2 \times 47\mu F$, $L = 5.6\mu H$,
 $DCR = 14.5m\Omega$



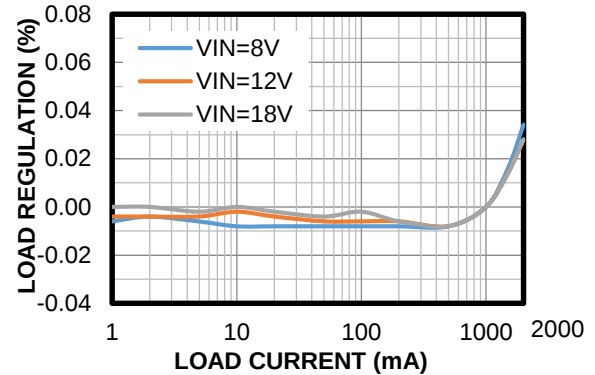
Load Regulation for MPQ3524-2000

AAM mode, $DCR = 22.1m\Omega$



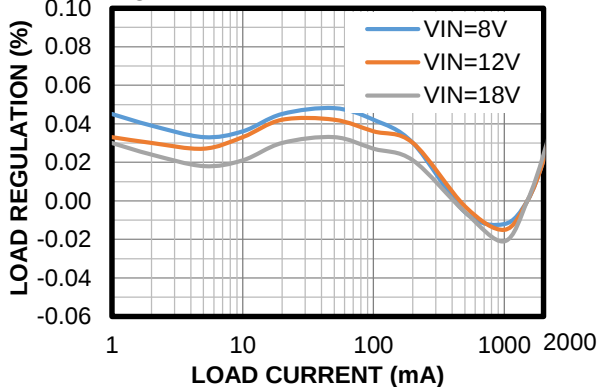
Load Regulation for MPQ3524-2001

FCCM, $DCR = 22.1m\Omega$



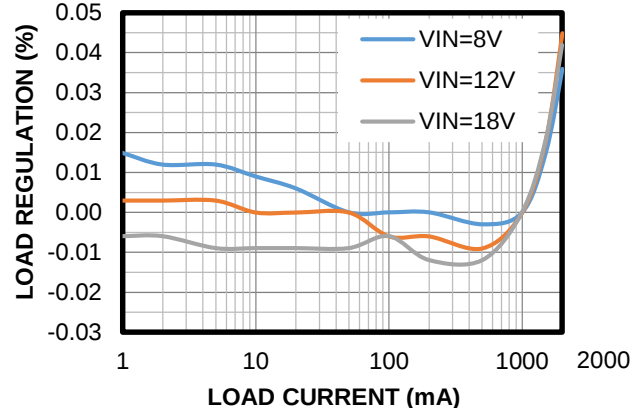
Load Regulation for MPQ3524-2000

AAM mode, $V_{OUT} = 3.3V$,
 $DCR = 22.1m\Omega$



Load Regulation for MPQ3524-2001

FCCM, $V_{OUT} = 3.3V$, $DCR = 22.1m\Omega$

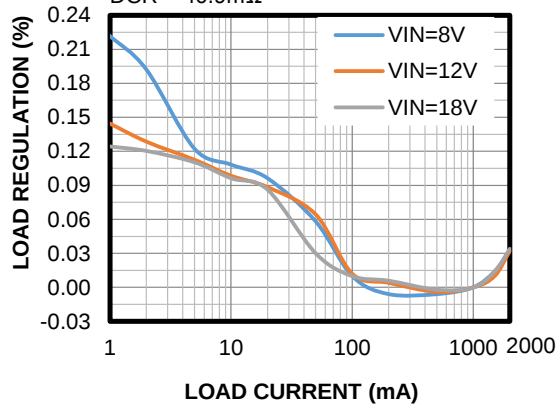


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 2.2μH, C_{OUT} = 2 x 22μF, T_A = 25°C, unless otherwise noted.

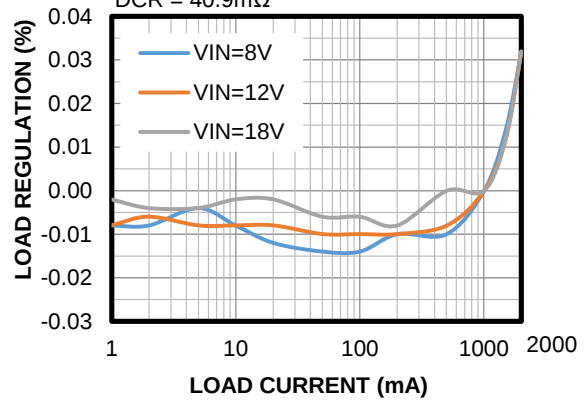
Load Regulation for MPQ3524-2000

AAM mode, f_{SW} = 415kHz,
C_{OUT} = 2 x 47μF, L = 10μH,
DCR = 40.9mΩ



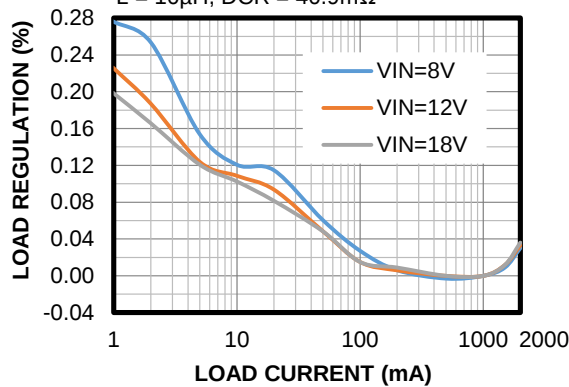
Load Regulation for MPQ3524-2001

FCCM, f_{SW} = 415kHz,
C_{OUT} = 2 x 47μF, L = 10μH,
DCR = 40.9mΩ



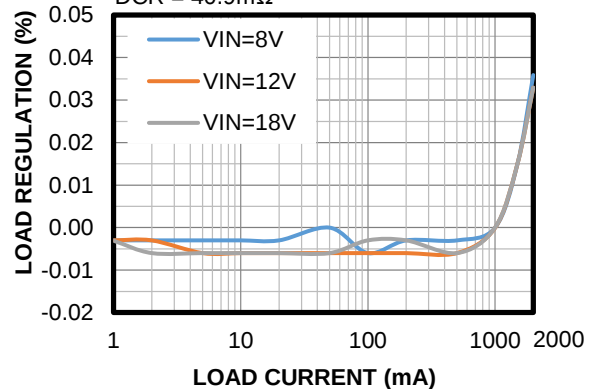
Load Regulation for MPQ3524-2000

AAM mode, V_{OUT} = 3.3V,
f_{SW} = 415kHz, C_{OUT} = 2 x 47μF,
L = 10μH, DCR = 40.9mΩ



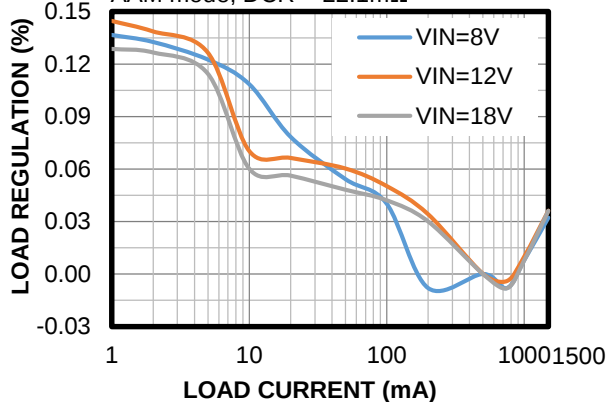
Load Regulation for MPQ3524-2001

FCCM, V_{OUT} = 3.3V, f_{SW} = 415kHz,
C_{OUT} = 2 x 47μF, L = 10μH,
DCR = 40.9mΩ



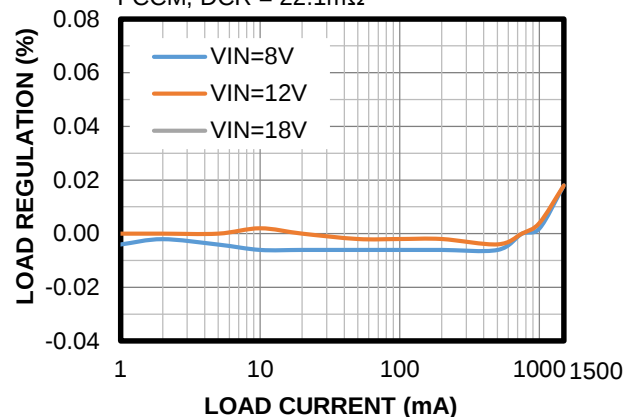
Load Regulation for MPQ3524-1500

AAM mode, DCR = 22.1mΩ



Load Regulation for MPQ3524-1501

FCCM, DCR = 22.1mΩ

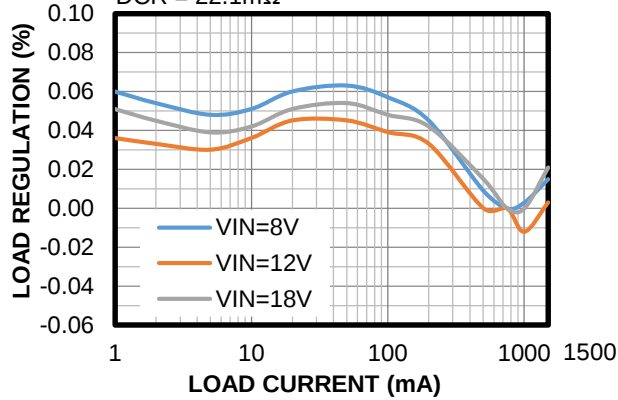


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 2.2μH, C_{OUT} = 2 x 22μF, T_A = 25°C, unless otherwise noted.

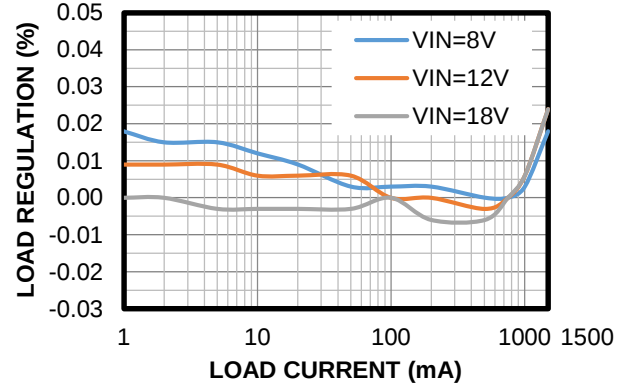
Load Regulation for MPQ3524-1500

AAM mode, V_{OUT} = 3.3V,
DCR = 22.1mΩ



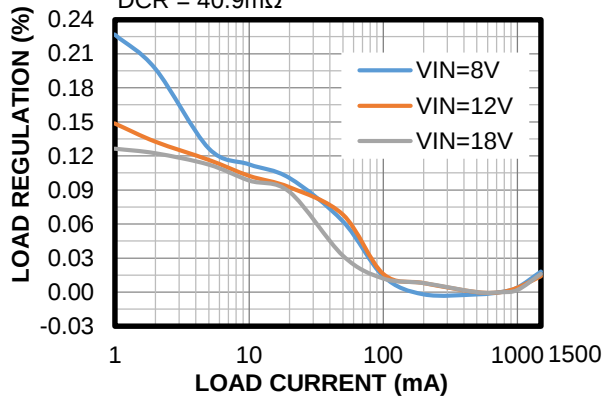
Load Regulation for MPQ3524-1501

FCCM, V_{OUT} = 3.3V, DCR = 22.1mΩ



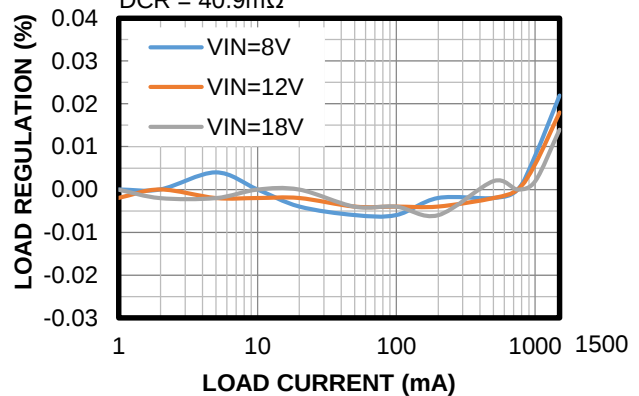
Load Regulation for MPQ3524-1500

AAM mode, f_{SW} = 415kHz,
C_{OUT} = 2 x 47μF, L = 10μH,
DCR = 40.9mΩ



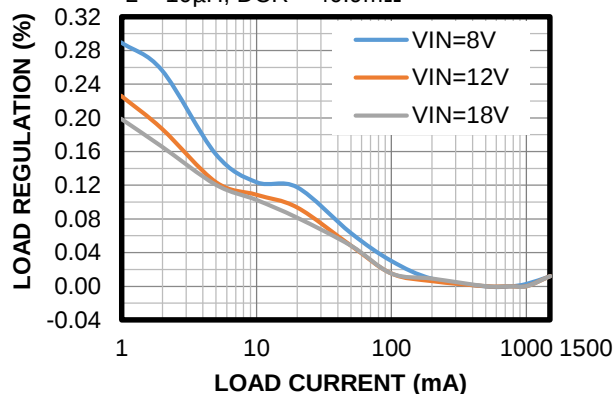
Load Regulation for MPQ3524-1501

FCCM, f_{SW} = 415kHz,
C_{OUT} = 2 x 47μF, L = 10μH,
DCR = 40.9mΩ



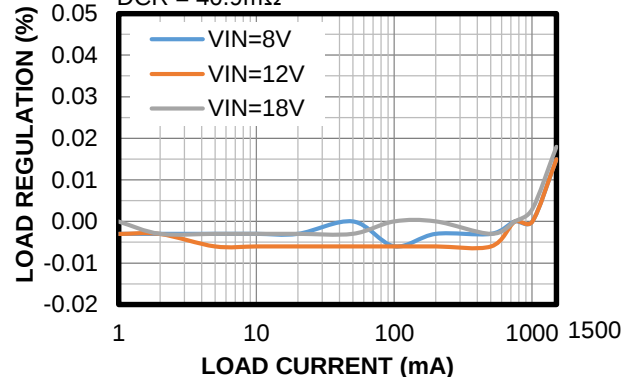
Load Regulation for MPQ3524-1500

AAM mode, V_{OUT} = 3.3V,
f_{SW} = 415kHz, C_{OUT} = 2 x 47μF,
L = 10μH, DCR = 40.9mΩ



Load Regulation for MPQ3524-1501

FCCM, V_{OUT} = 3.3V, f_{SW} = 415kHz,
C_{OUT} = 2 x 47μF, L = 10μH,
DCR = 40.9mΩ

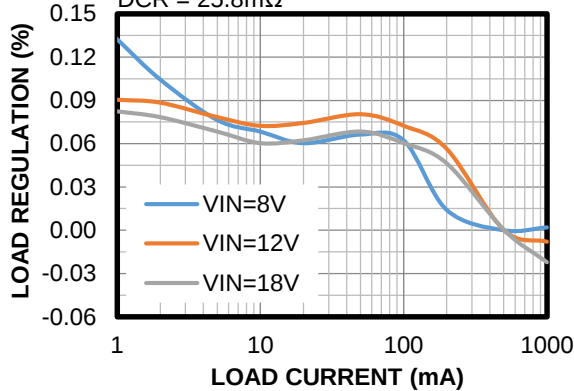


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN} = 12V$, $V_{OUT} = 5V$, $f_{SW} = 2.2MHz$, $L = 2.2\mu H$, $C_{OUT} = 2 \times 22\mu F$, $T_A = 25^\circ C$, unless otherwise noted.

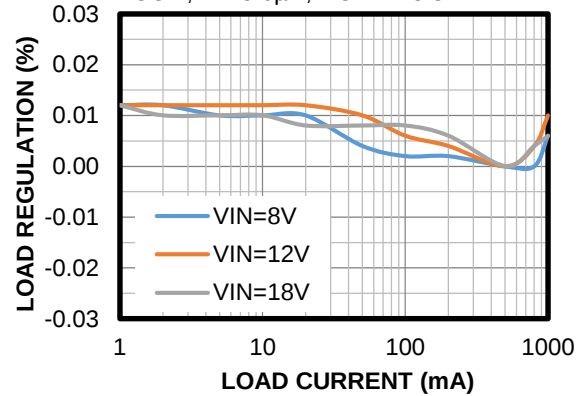
Load Regulation for MPQ3524-1000

AAM mode, $L = 5.6\mu H$,
DCR = 25.8m Ω



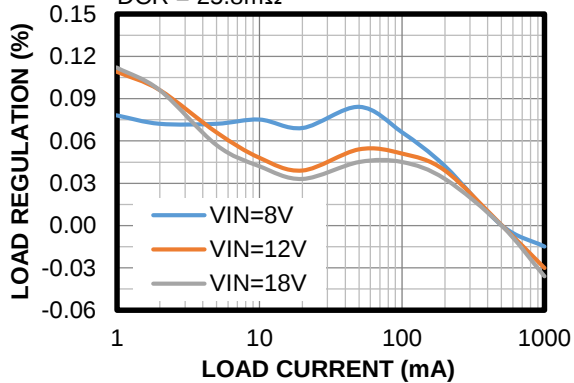
Load Regulation for MPQ3524-1001

FCCM, $L = 5.6\mu H$, DCR = 25.8m Ω



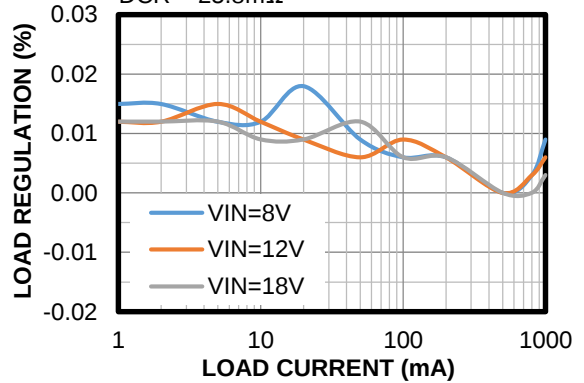
Load Regulation for MPQ3524-1000

AAM mode, $V_{OUT} = 3.3V$, $L = 5.6\mu H$,
DCR = 25.8m Ω



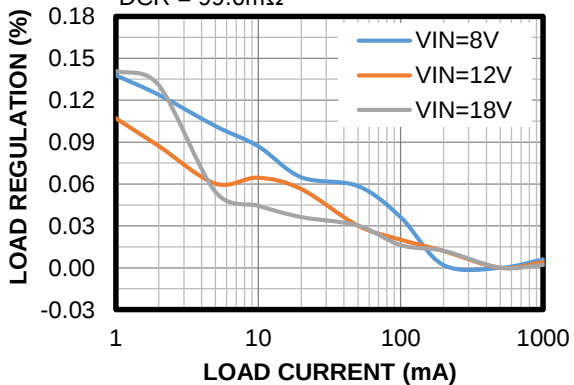
Load Regulation for MPQ3524-1001

FCCM, $V_{OUT} = 3.3V$, $L = 5.6\mu H$,
DCR = 25.8m Ω



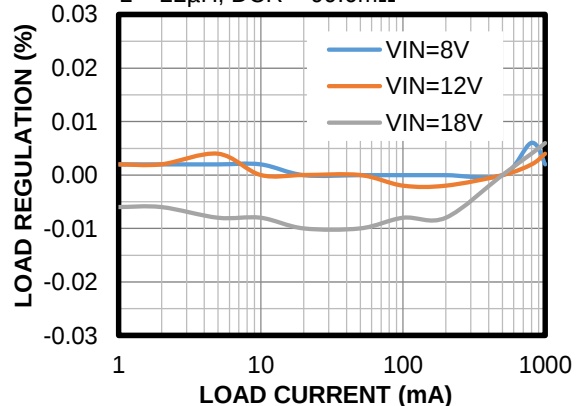
Load Regulation for MPQ3524-1000

AAM mode, $f_{SW} = 415kHz$,
 $C_{OUT} = 2 \times 47\mu F$, $L = 22\mu H$,
DCR = 99.6m Ω



Load Regulation for MPQ3524-1001

FCCM, $f_{SW} = 415kHz$, $C_{OUT} = 2 \times 47\mu F$,
 $L = 22\mu H$, DCR = 99.6m Ω

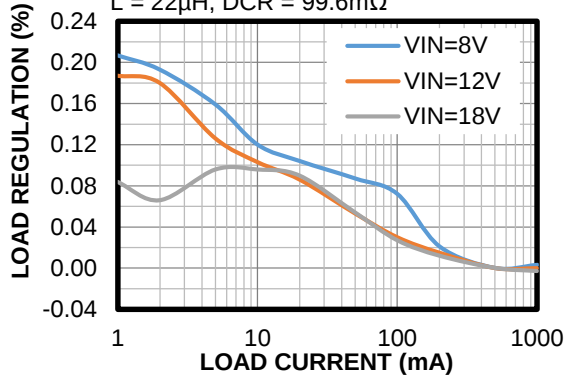


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 2.2μH, C_{OUT} = 22μF x 2, T_A = 25°C, unless otherwise noted.

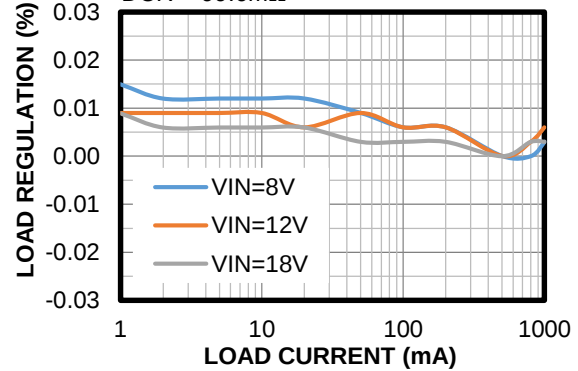
Load Regulation for MPQ3524-1000

AAM mode, V_{OUT} = 3.3V, f_{SW} = 415kHz, C_{OUT} = 2 x 47μF, L = 22μH, DCR = 99.6mΩ



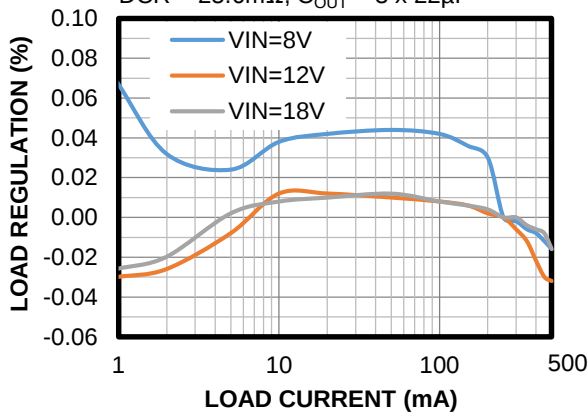
Load Regulation for MPQ3524-1001

FCCM, V_{OUT} = 3.3V, f_{SW} = 415kHz, C_{OUT} = 2 x 47μF, L = 22μH, DCR = 99.6mΩ



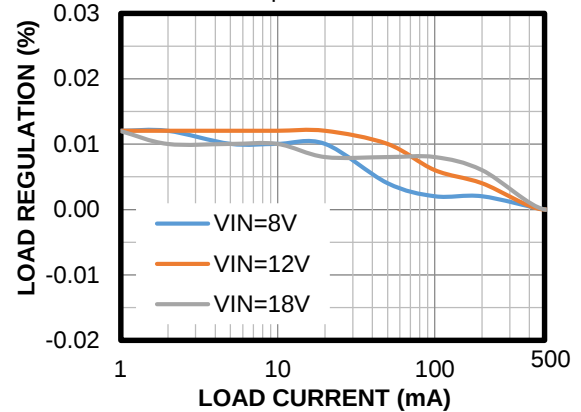
Load Regulation for MPQ3524-0500

AAM mode, R_{FREQ} = 15kΩ, L = 5.6μH, DCR = 25.6mΩ, C_{OUT} = 3 x 22μF



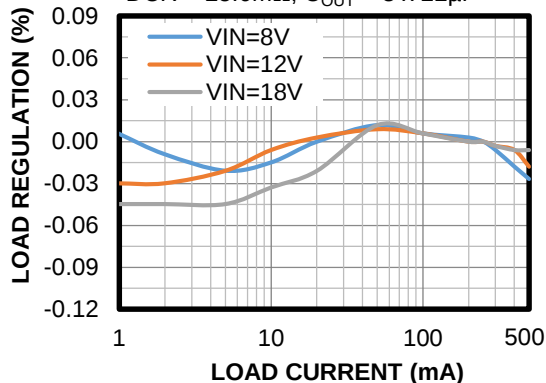
Load Regulation for MPQ3524-0501

FCCM, L = 5.6μH, DCR = 25.8mΩ



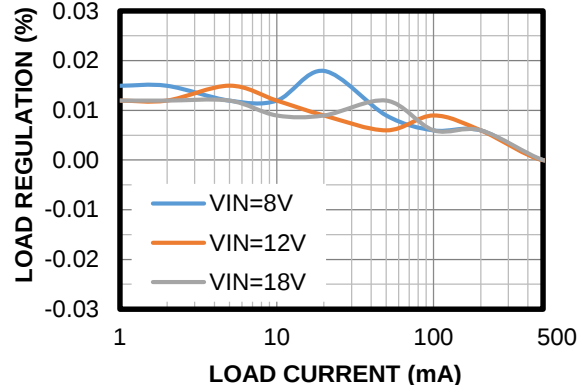
Load Regulation for MPQ3524-0500

AAM mode, R_{FREQ} = 15kΩ, V_{OUT} = 3.3V, L = 5.6μH, DCR = 25.6mΩ, C_{OUT} = 3 x 22μF



Load Regulation for MPQ3524-0501

FCCM, V_{OUT} = 3.3V, L = 5.6μH, DCR = 25.8mΩ

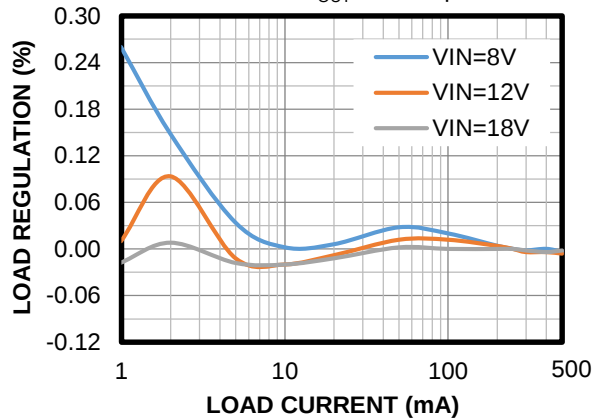


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 2.2μH, C_{OUT} = 2 x 22μF, T_A = 25°C, unless otherwise noted.

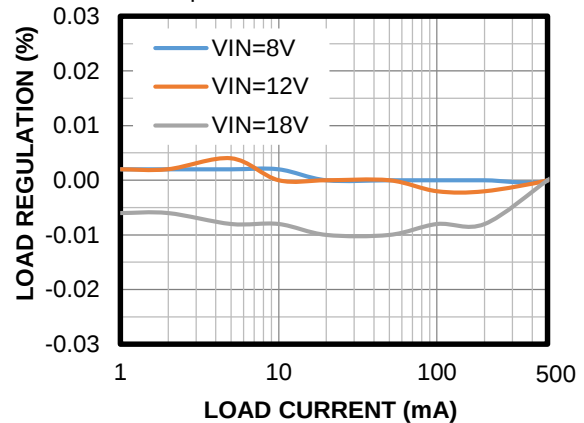
Load Regulation for MPQ3524-0500

AAM mode, R_{FREQ} = 86.6kΩ, L = 22μH, DCR = 99.6mΩ, C_{OUT} = 2 x 47μF



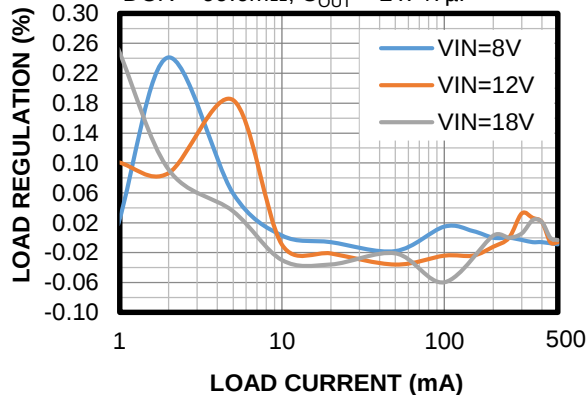
Load Regulation for MPQ3524-0501

FCCM, f_{SW} = 415kHz, C_{OUT} = 2 x 47μF, L = 22μH, DCR = 99.6mΩ



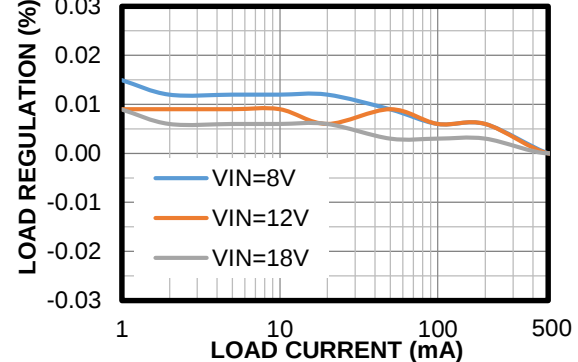
Load Regulation for MPQ3524-0500

AAM mode, V_{OUT} = 3.3V, R_{FREQ} = 86.6kΩ, L = 22μH, DCR = 99.6mΩ, C_{OUT} = 2 x 47μF



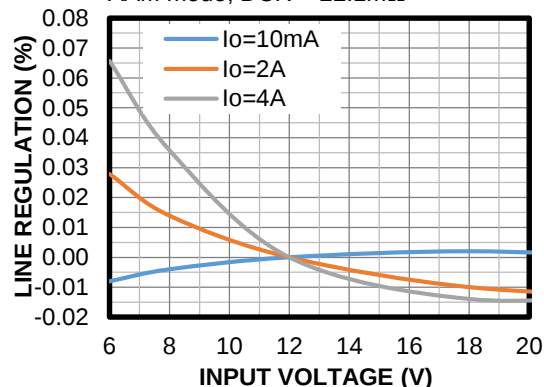
Load Regulation for MPQ3524-0501

FCCM, V_{OUT} = 3.3V, f_{SW} = 415kHz, C_{OUT} = 2 x 47μF, L = 22μH, DCR = 99.6mΩ



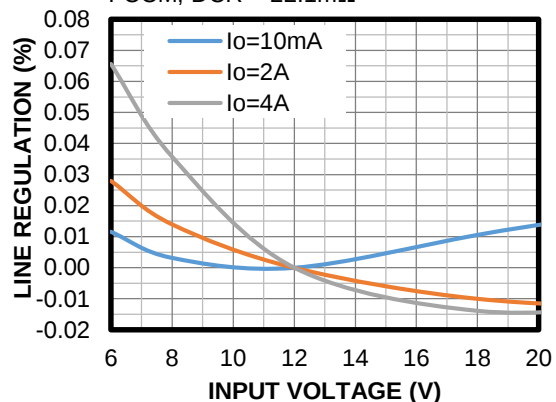
Line Regulation for MPQ3524-4000

AAM mode, DCR = 22.1mΩ



Line Regulation for MPQ3524-4001

FCCM, DCR = 22.1mΩ

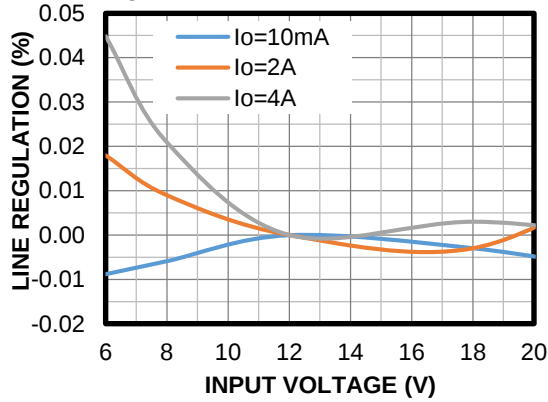


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN} = 12V$, $V_{OUT} = 5V$, $f_{SW} = 2.2MHz$, $L = 2.2\mu H$, $C_{OUT} = 2 \times 22\mu F$, $T_A = 25^\circ C$, unless otherwise noted.

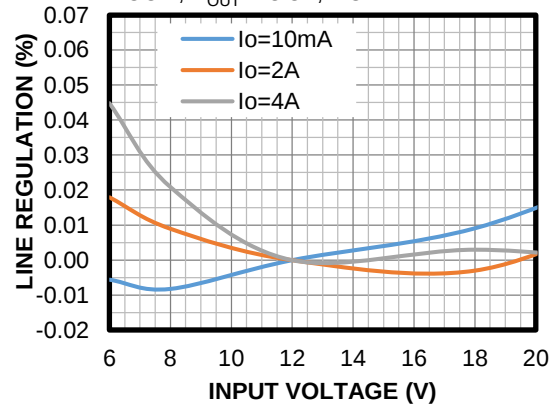
Line Regulation for MPQ3524-4000

AAM mode, $V_{OUT} = 3.3V$,
DCR = 22.1m Ω



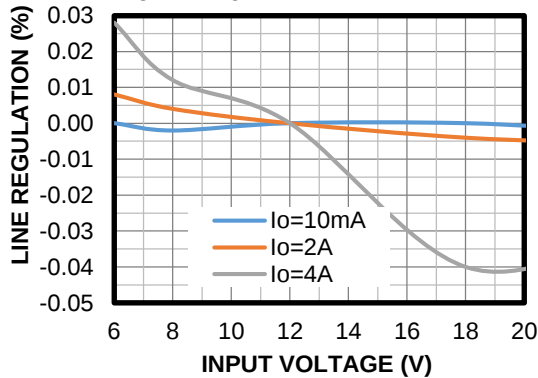
Line Regulation for MPQ3524-4001

FCCM, $V_{OUT} = 3.3V$, DCR = 22.1m Ω



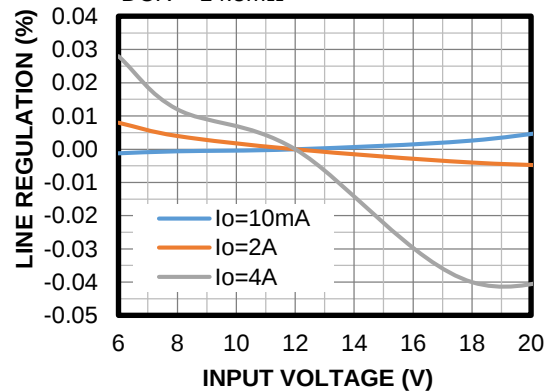
Line Regulation for MPQ3524-4000

AAM mode, $f_{SW} = 415kHz$,
 $C_{OUT} = 2 \times 47\mu F$, $L = 5.6\mu H$,
DCR = 14.5m Ω



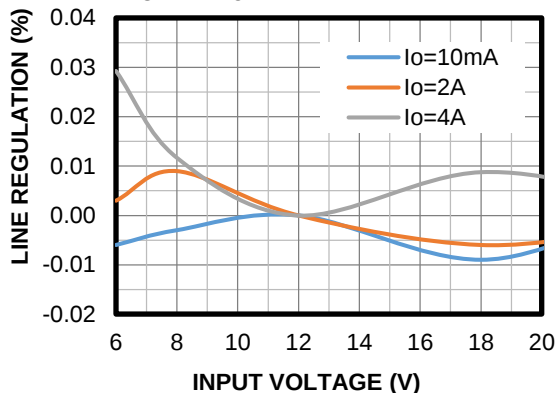
Line Regulation for MPQ3524-4001

FCCM, $f_{SW} = 415kHz$,
 $C_{OUT} = 2 \times 47\mu F$, $L = 5.6\mu H$,
DCR = 14.5m Ω



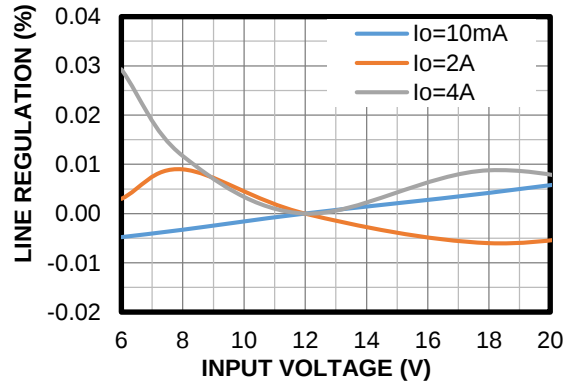
Line Regulation for MPQ3524-4000

AAM mode, $V_{OUT} = 3.3V$, $f_{SW} = 415kHz$,
 $C_{OUT} = 2 \times 47\mu F$, $L = 5.6\mu H$,
DCR = 14.5m Ω



Line Regulation for MPQ3524-4001

FCCM, $V_{OUT} = 3.3V$, $f_{SW} = 415kHz$,
 $C_{OUT} = 2 \times 47\mu F$, $L = 5.6\mu H$,
DCR = 14.5m Ω

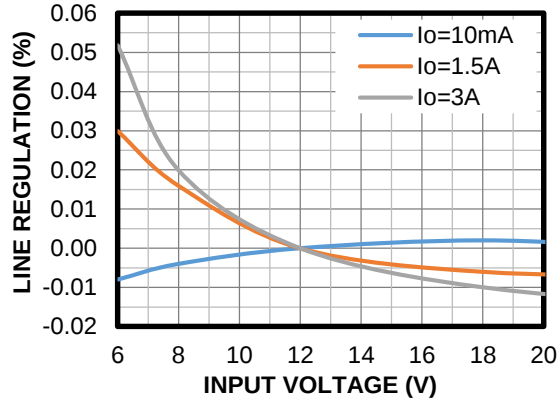


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN} = 12V$, $V_{OUT} = 5V$, $f_{SW} = 2.2MHz$, $L = 2.2\mu H$, $C_{OUT} = 22\mu F \times 2$, $T_A = 25^\circ C$, unless otherwise noted.

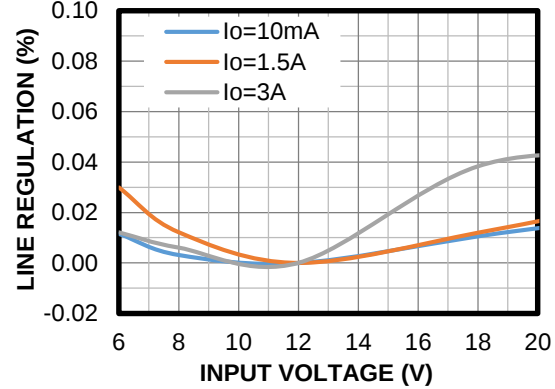
Line Regulation for MPQ3524-3000

AAM mode, DCR = 22.1m Ω



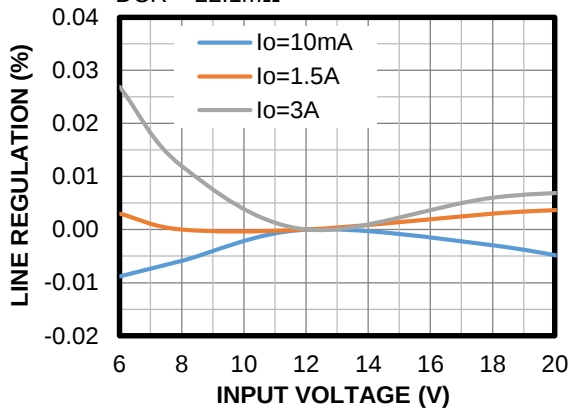
Line Regulation for MPQ3524-3001

FCCM, DCR = 22.1m Ω



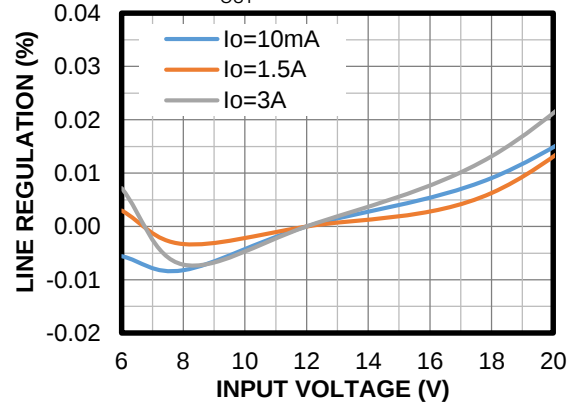
Line Regulation for MPQ3524-3000

AAM mode, $V_{OUT} = 3.3V$, DCR = 22.1m Ω



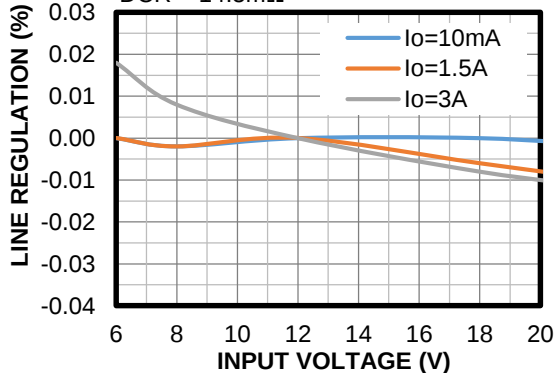
Line Regulation for MPQ3524-3001

FCCM, $V_{OUT} = 3.3V$, DCR = 22.1m Ω



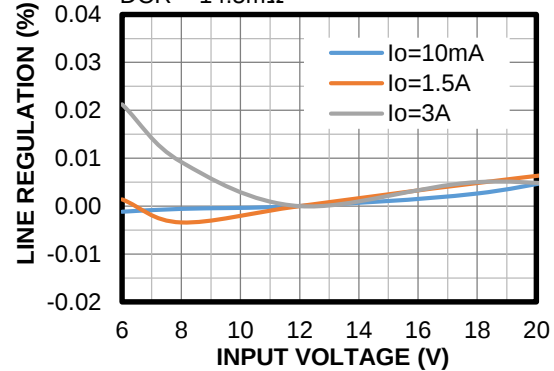
Line Regulation for MPQ3524-3000

AAM mode, $f_{SW} = 415kHz$, $C_{OUT} = 3 \times 47\mu F$, $L = 5.6\mu H$, DCR = 14.5m Ω



Line Regulation for MPQ3524-3001

FCCM, $f_{SW} = 415kHz$, $C_{OUT} = 2 \times 47\mu F$, $L = 5.6\mu H$, DCR = 14.5m Ω

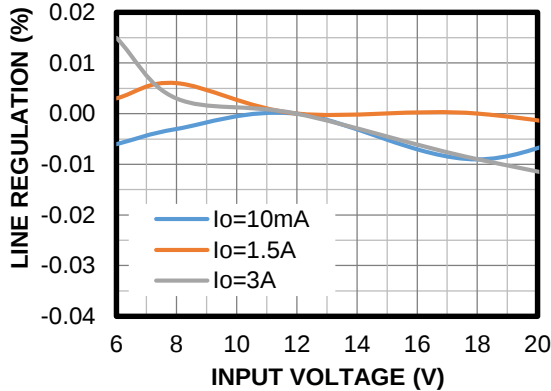


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN} = 12V$, $V_{OUT} = 5V$, $f_{SW} = 2.2MHz$, $L = 2.2\mu H$, $C_{OUT} = 2 \times 22\mu F$, $T_A = 25^\circ C$, unless otherwise noted.

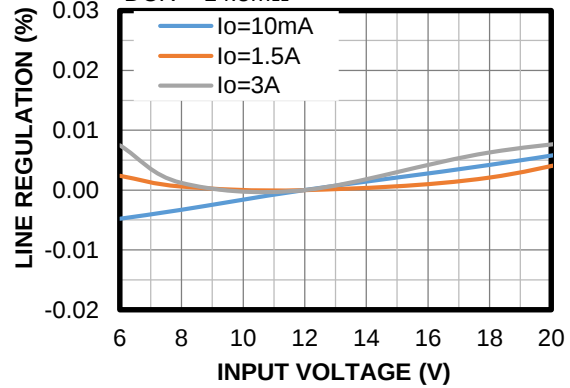
Line Regulation for MPQ3524-3000

AAM mode, $V_{OUT} = 3.3V$,
 $f_{SW} = 415kHz$, $C_{OUT} = 2 \times 47\mu F$,
 $L = 5.6\mu H$, $DCR = 14.5m\Omega$



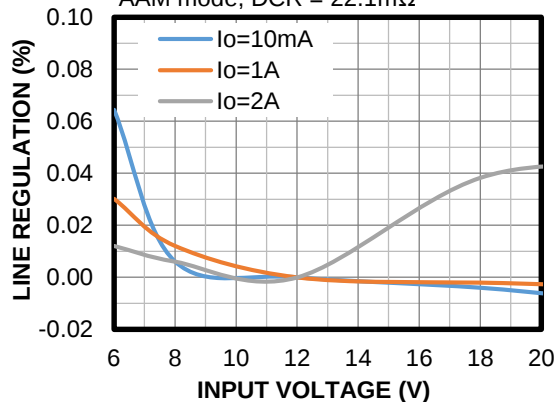
Line Regulation for MPQ3524-3001

FCCM, $V_{OUT} = 3.3V$, $f_{SW} = 415kHz$,
 $C_{OUT} = 47\mu F \times 2$, $L = 5.6\mu H$,
 $DCR = 14.5m\Omega$



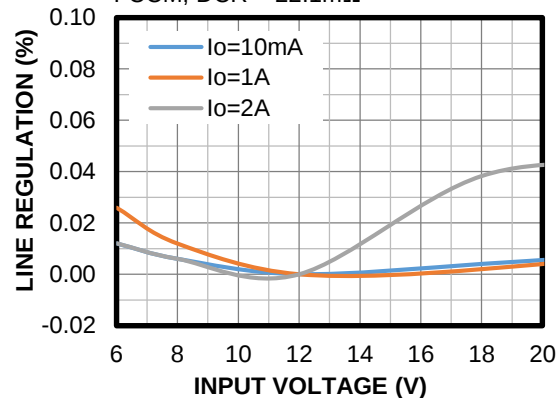
Line Regulation for MPQ3524-2000

AAM mode, $DCR = 22.1m\Omega$



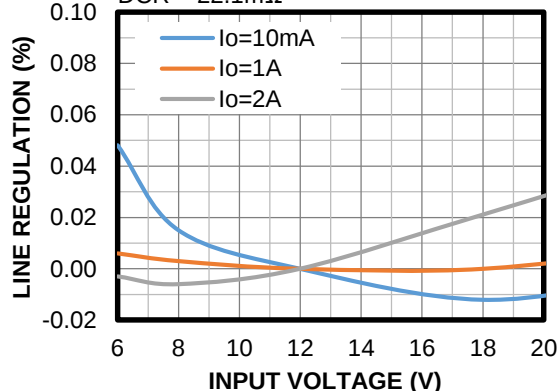
Line Regulation for MPQ3524-2001

FCCM, $DCR = 22.1m\Omega$



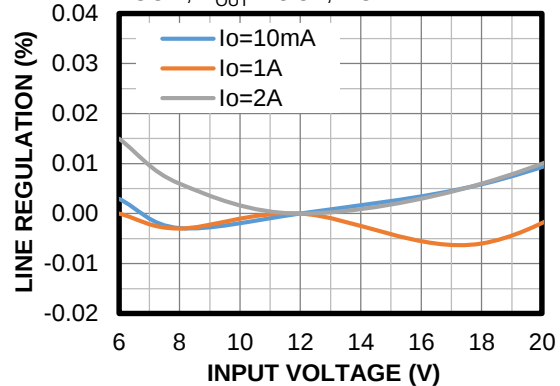
Line Regulation for MPQ3524-2000

AAM mode, $V_{OUT} = 3.3V$,
 $DCR = 22.1m\Omega$



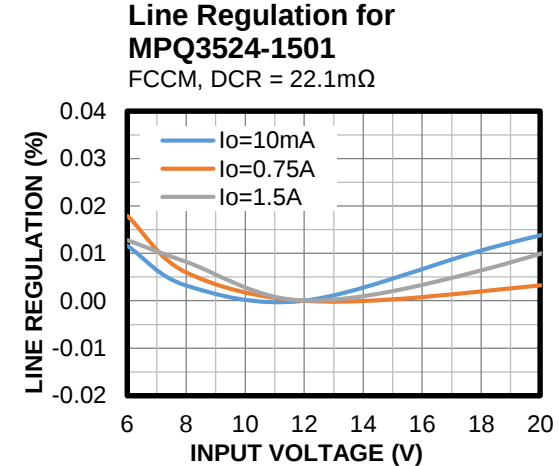
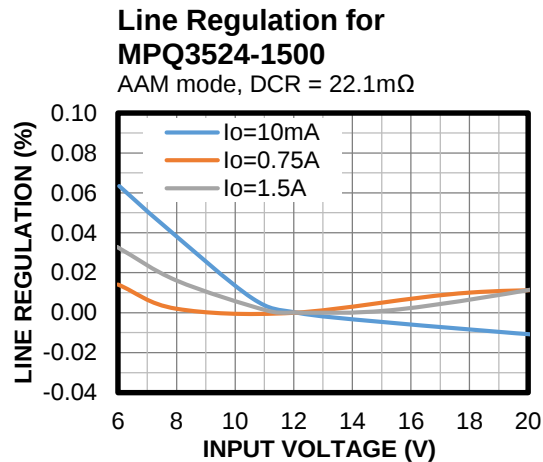
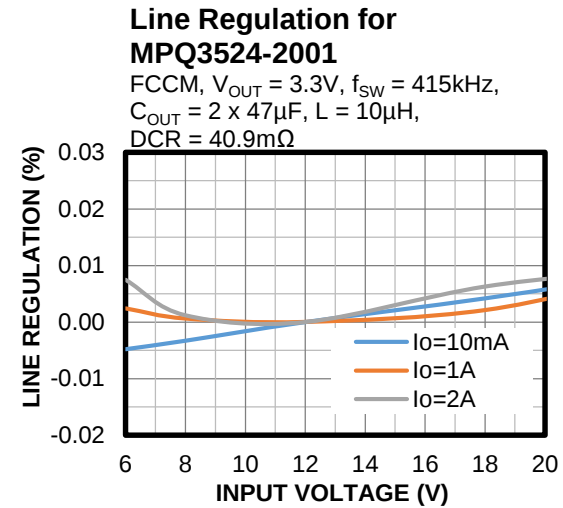
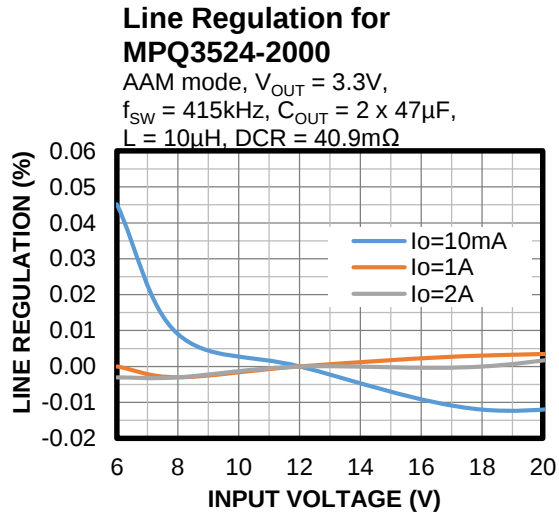
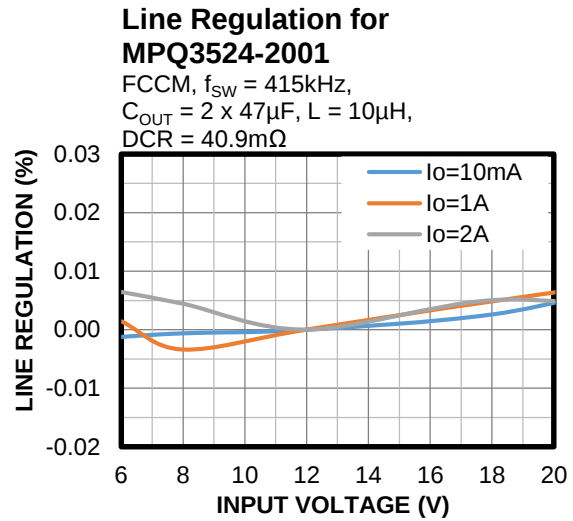
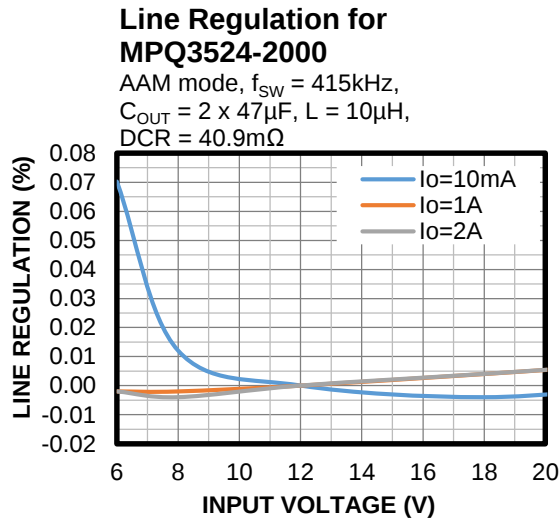
Line Regulation for MPQ3524-2001

FCCM, $V_{OUT} = 3.3V$, $DCR = 22.1m\Omega$



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN} = 12V$, $V_{OUT} = 5V$, $f_{SW} = 2.2MHz$, $L = 2.2\mu H$, $C_{OUT} = 2 \times 22\mu F$, $T_A = 25^\circ C$, unless otherwise noted.

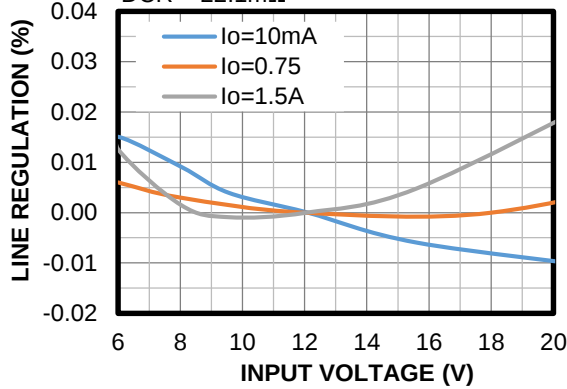


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN} = 12V$, $V_{OUT} = 5V$, $f_{SW} = 2.2MHz$, $L = 2.2\mu H$, $C_{OUT} = 2 \times 22\mu F$, $T_A = 25^\circ C$, unless otherwise noted.

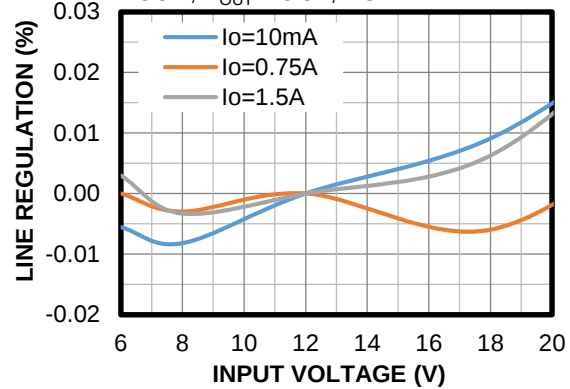
Line Regulation for MPQ3524-1500

AAM mode, $V_{OUT} = 3.3V$,
DCR = 22.1m Ω



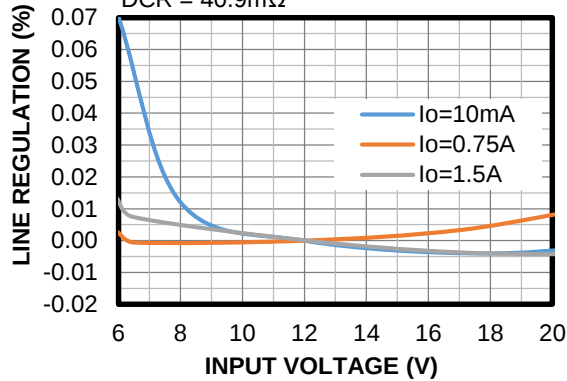
Line Regulation for MPQ3524-1501

FCCM, $V_{OUT} = 3.3V$, DCR = 22.1m Ω



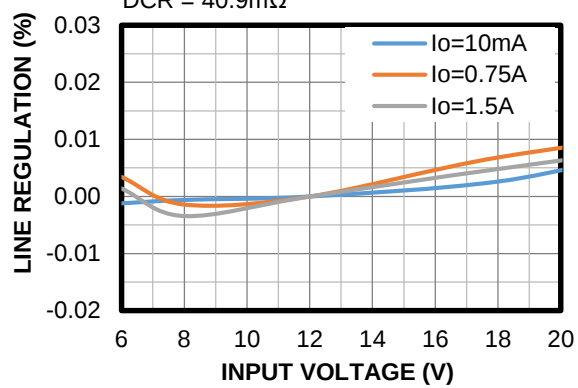
Line Regulation for MPQ3524-1500

AAM mode, $f_{SW} = 415kHz$,
 $C_{OUT} = 2 \times 47\mu F$, $L = 10\mu H$,
DCR = 40.9m Ω



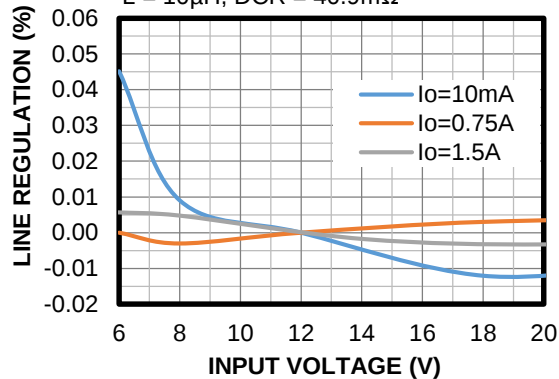
Line Regulation for MPQ3524-1501

FCCM, $f_{SW} = 415kHz$,
 $C_{OUT} = 2 \times 47\mu F$, $L = 10\mu H$,
DCR = 40.9m Ω



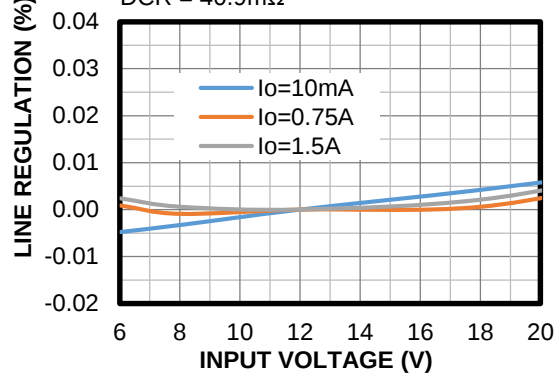
Line Regulation for MPQ3524-1500

AAM mode, $V_{OUT} = 3.3V$,
 $f_{SW} = 415kHz$, $C_{OUT} = 2 \times 47\mu F$,
 $L = 10\mu H$, DCR = 40.9m Ω



Line Regulation for MPQ3524-1501

FCCM, $V_{OUT} = 3.3V$, $f_{SW} = 415kHz$,
 $C_{OUT} = 2 \times 47\mu F$, $L = 10\mu H$,
DCR = 40.9m Ω

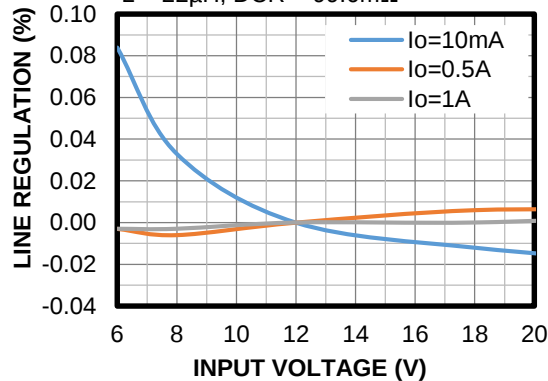


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN} = 12V$, $V_{OUT} = 5V$, $f_{SW} = 2.2MHz$, $L = 2.2\mu H$, $C_{OUT} = 2 \times 22\mu F$, $T_A = 25^\circ C$, unless otherwise noted.

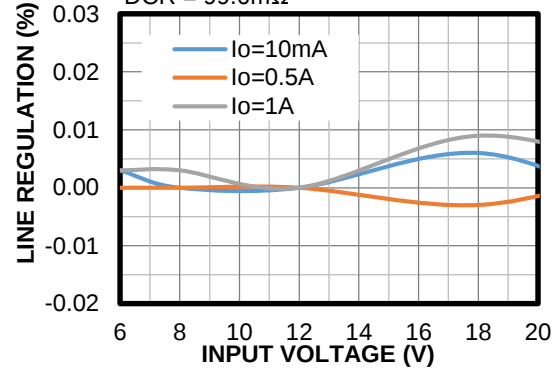
Line Regulation for MPQ3524-1000

AAM mode, $V_{OUT} = 3.3V$,
 $f_{SW} = 415kHz$, $C_{OUT} = 2 \times 47\mu F$,
 $L = 22\mu H$, $DCR = 99.6m\Omega$



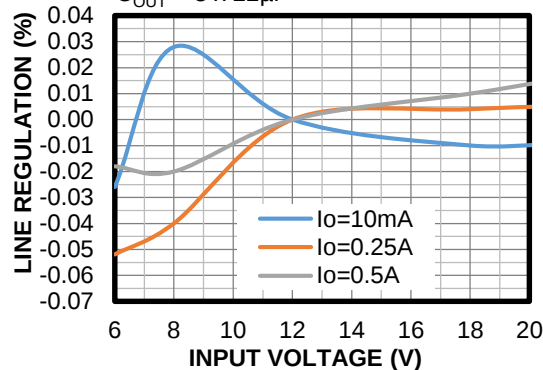
Line Regulation for MPQ3524-1001

FCCM, $V_{OUT} = 3.3V$, $f_{SW} = 415kHz$,
 $C_{OUT} = 2 \times 47\mu F$, $L = 22\mu H$,
 $DCR = 99.6m\Omega$



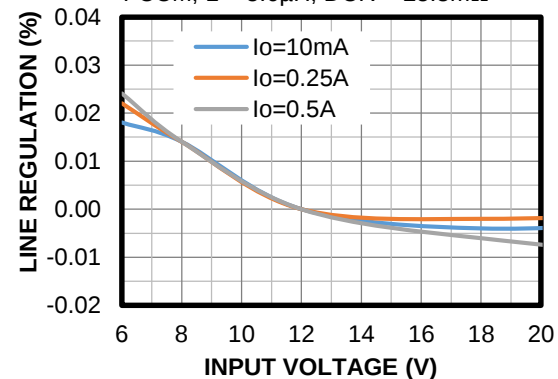
Line Regulation for MPQ3524-0500

AAM mode, $R_{FREQ} = 15k\Omega$,
 $L = 5.6\mu H$, $DCR = 25.6m\Omega$,
 $C_{OUT} = 3 \times 22\mu F$



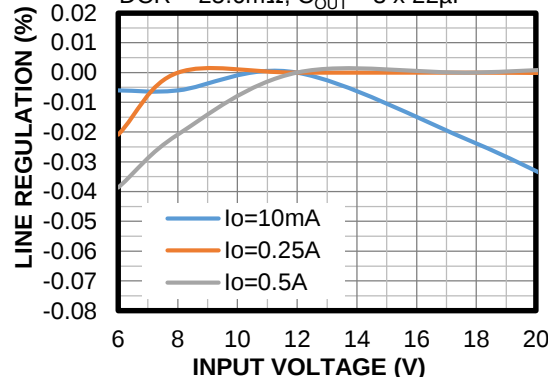
Line Regulation for MPQ3524-0501

FCCM, $L = 5.6\mu H$, $DCR = 25.8m\Omega$



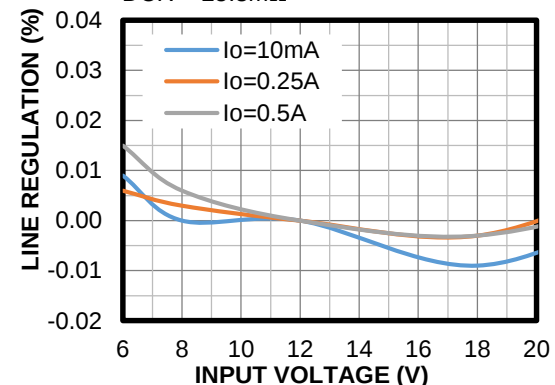
Line Regulation for MPQ3524-0500

AAM mode, $R_{FREQ} = 15k\Omega$,
 $V_{OUT} = 3.3V$, $L = 5.6\mu H$,
 $DCR = 25.6m\Omega$, $C_{OUT} = 3 \times 22\mu F$



Line Regulation for MPQ3524-0501

FCCM, $V_{OUT} = 3.3V$, $L = 5.6\mu H$,
 $DCR = 25.8m\Omega$

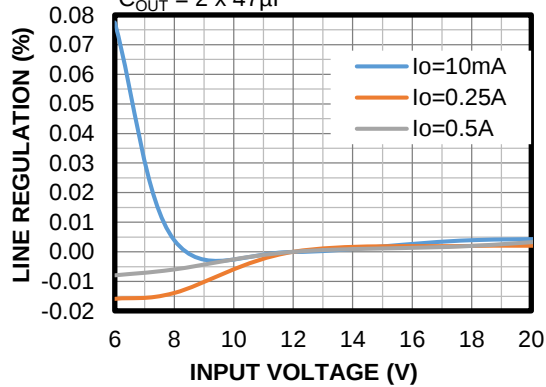


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 2.2μH, C_{OUT} = 2 x 22μF, T_A = 25°C, unless otherwise noted.

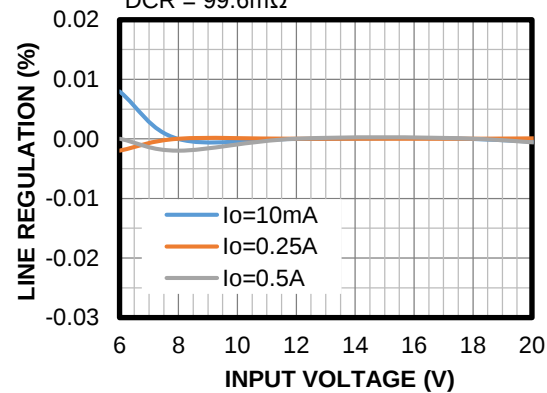
Line Regulation for MPQ3524-0500

AAM mode, R_{FREQ} = 86.6kΩ,
L = 22μH, DCR = 99.6mΩ,
C_{OUT} = 2 x 47μF



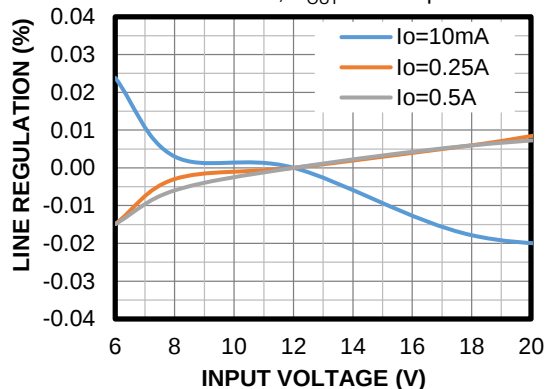
Line Regulation for MPQ3524-0501

FCCM, f_{SW} = 415kHz,
C_{OUT} = 2 x 47μF, L = 22μH,
DCR = 99.6mΩ



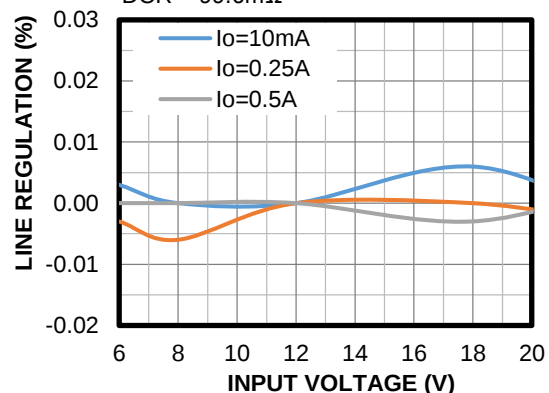
Line Regulation for MPQ3524-0500

AAM mode, V_{OUT} = 3.3V,
R_{FREQ} = 86.6kΩ, L = 22μH,
DCR = 99.6mΩ, C_{OUT} = 2 x 47μF



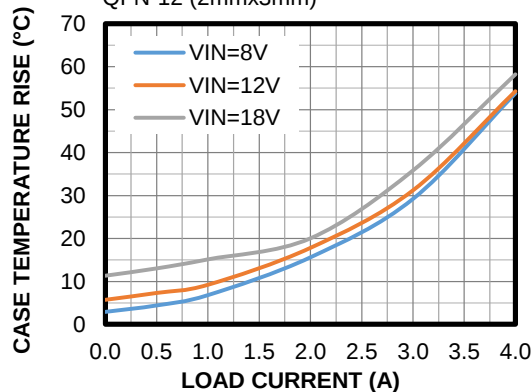
Line Regulation for MPQ3524-0501

FCCM, V_{OUT} = 3.3V, f_{SW} = 415kHz,
C_{OUT} = 2 x 47μF, L = 22μH,
DCR = 99.6mΩ



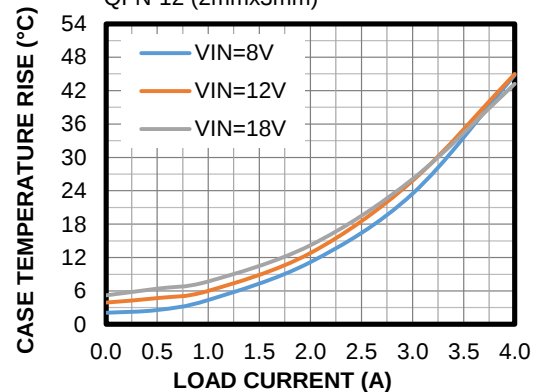
Case Temperature Rise

V_{OUT} = 5V, f_{SW} = 2.2MHz, FCCM,
QFN-12 (2mmx3mm)



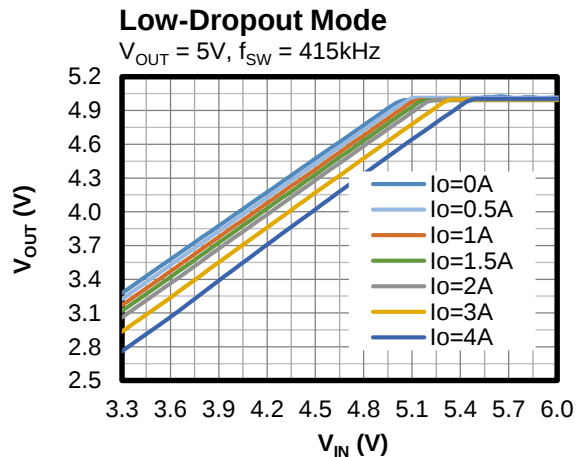
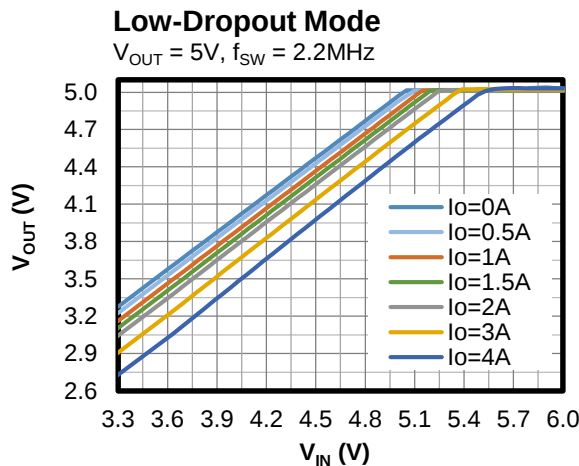
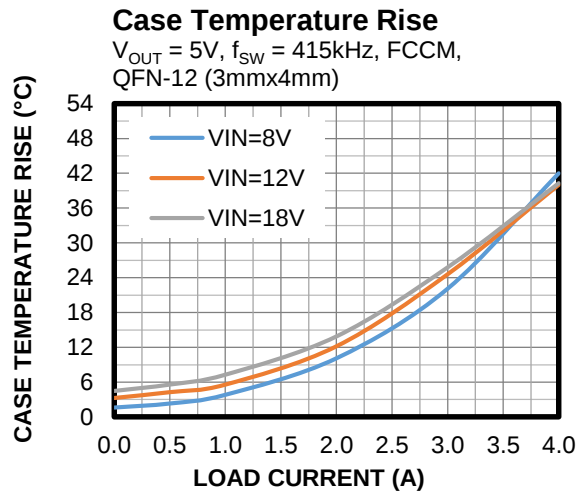
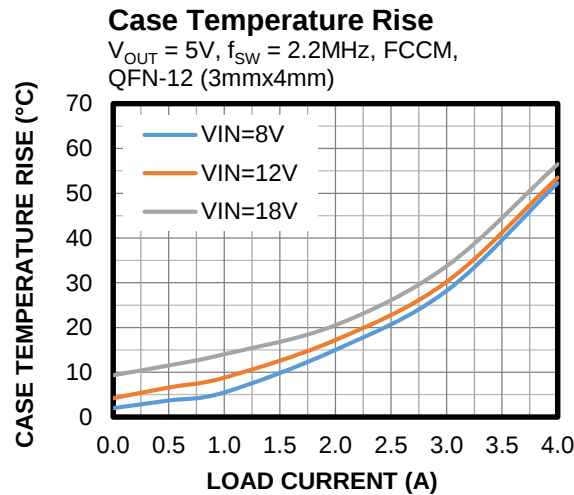
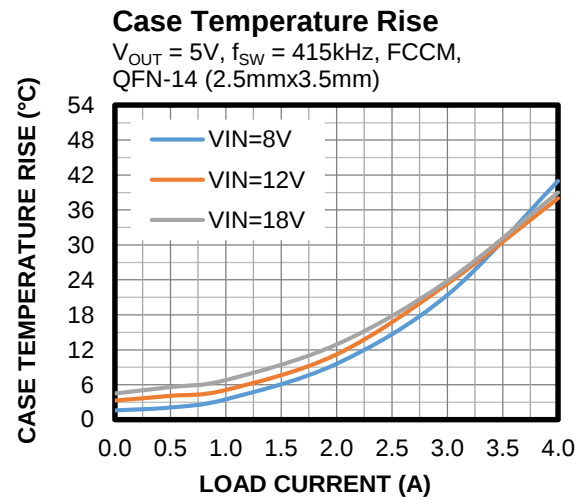
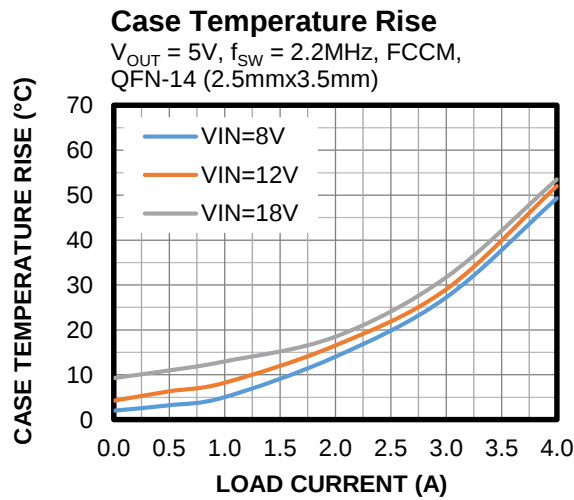
Case Temperature Rise

V_{OUT} = 5V, f_{SW} = 415kHz, FCCM,
QFN-12 (2mmx3mm)



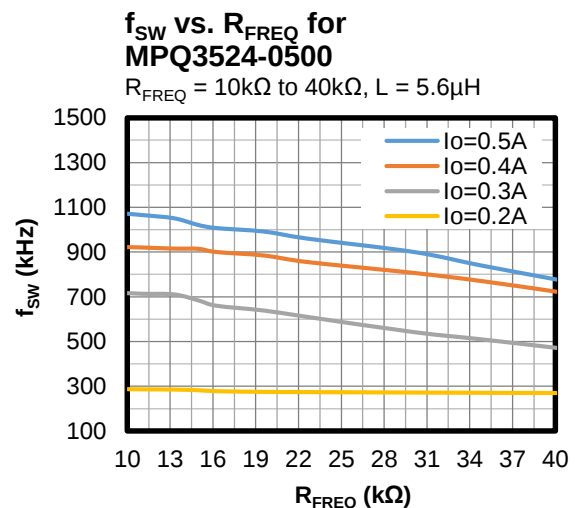
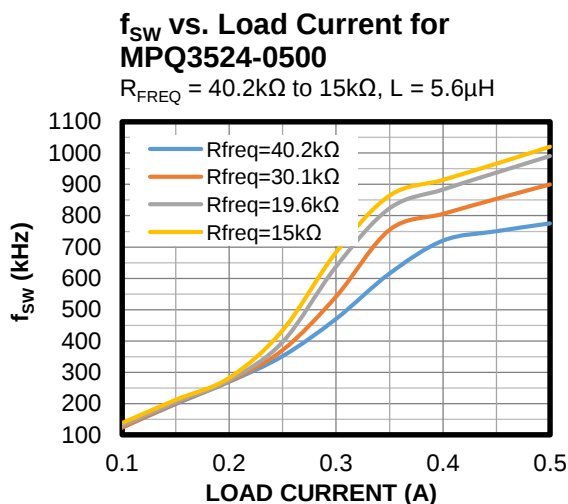
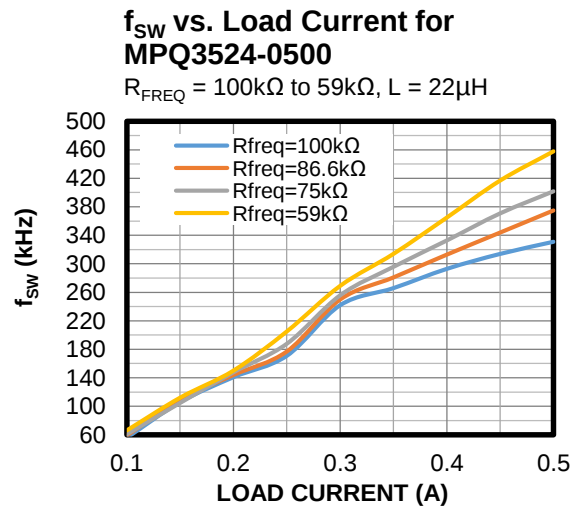
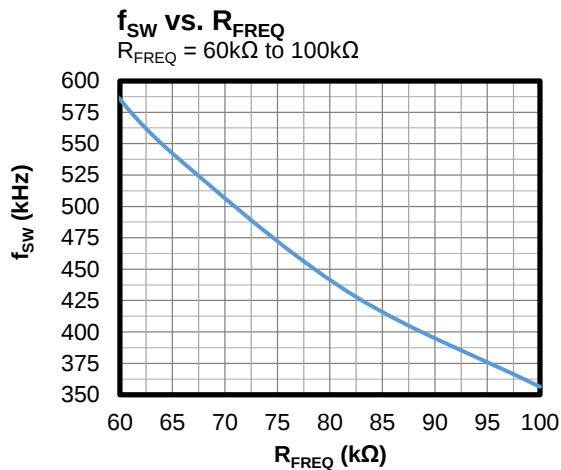
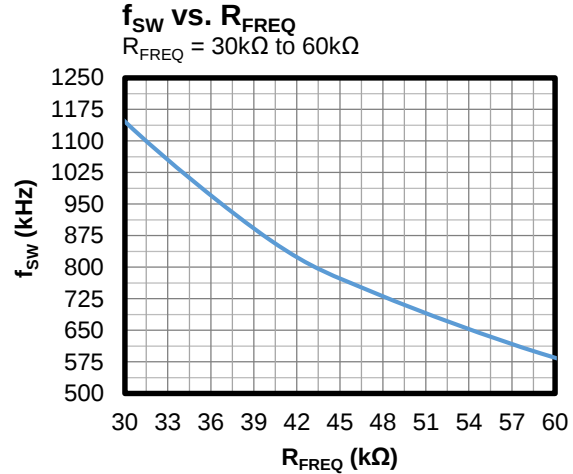
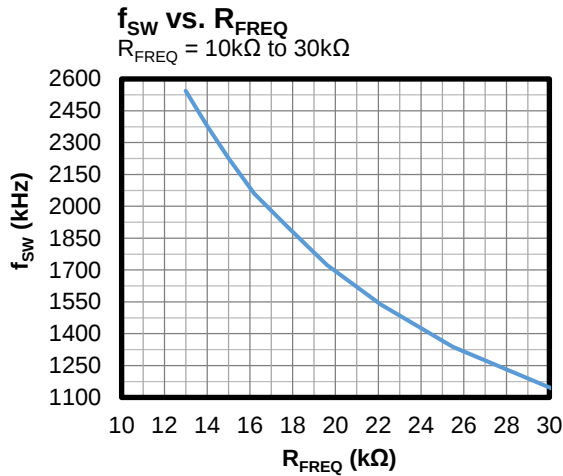
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN} = 12V$, $V_{OUT} = 5V$, $f_{SW} = 2.2MHz$, $L = 2.2\mu H$, $C_{OUT} = 2 \times 22\mu F$, $T_A = 25^\circ C$, unless otherwise noted.



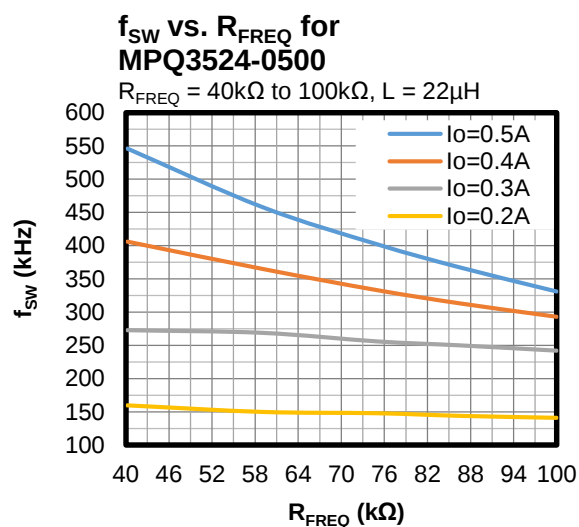
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 2.2μH, C_{OUT} = 2 x 22μF, T_A = 25°C, unless otherwise noted.



TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

$V_{IN} = 12V$, $V_{OUT} = 5V$, $f_{SW} = 2.2MHz$, $L = 2.2\mu H$, $C_{OUT} = 2 \times 22\mu F$, $T_A = 25^\circ C$, unless otherwise noted.

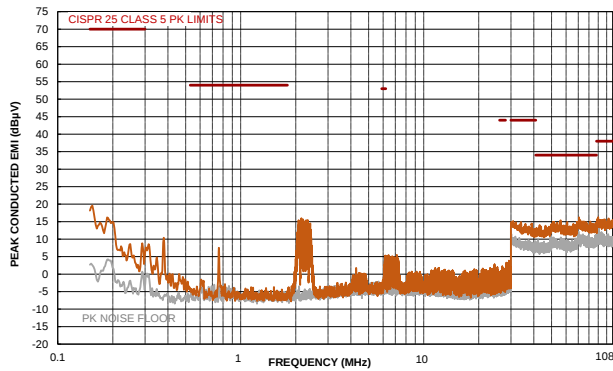


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

$V_{IN} = 12V$, $V_{OUT} = 5V$, $f_{SW} = 2.2MHz$, $L = 2.2\mu H$, $C_{OUT} = 2 \times 22\mu F$, $T_A = 25^\circ C$, unless otherwise noted. ⁽¹¹⁾

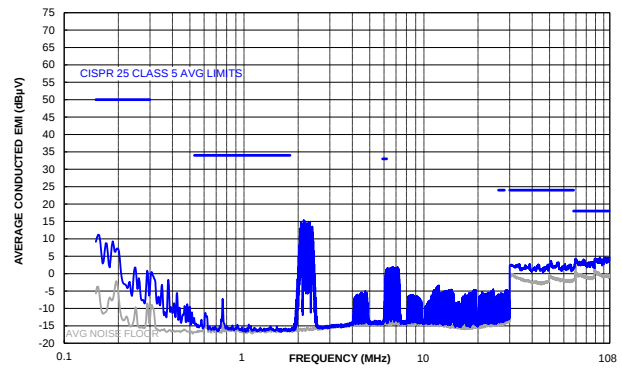
CISPR 25 Class 5 Peak Conducted Emissions

150kHz to 108MHz



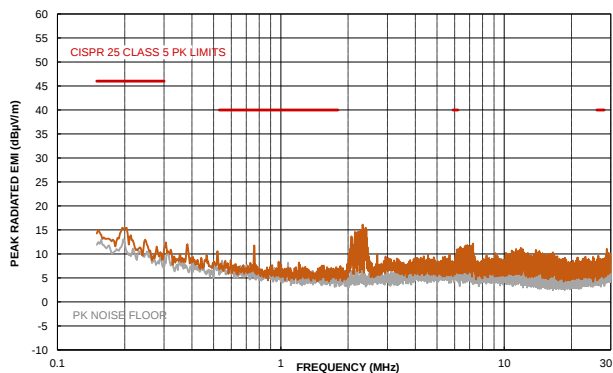
CISPR 25 Class 5 Average Conducted Emissions

150kHz to 108MHz



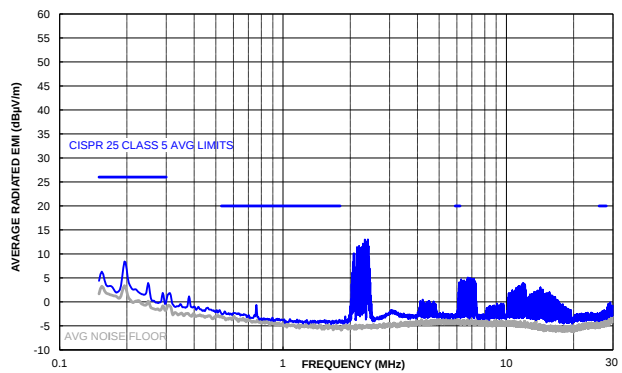
CISPR 25 Class 5 Peak Radiated Emissions

150kHz to 30MHz



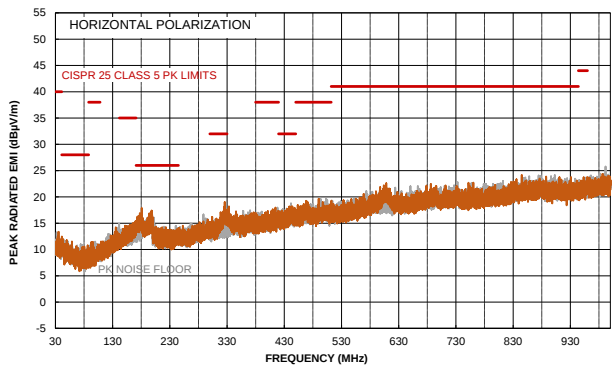
CISPR 25 Class 5 Average Radiated Emissions

150kHz to 30MHz



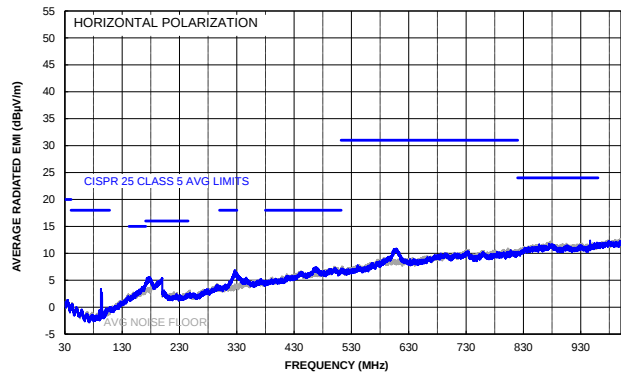
CISPR 25 Class 5 Peak Radiated Emissions

Horizontal, 30MHz to 1GHz



CISPR 25 Class 5 Average Radiated Emissions

Horizontal, 30MHz to 1GHz

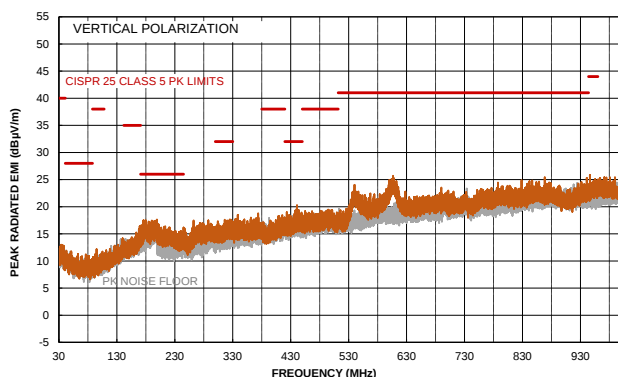


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 2.2μH, C_{OUT} = 2 x 22μF, T_A = 25°C, unless otherwise noted. ⁽¹¹⁾

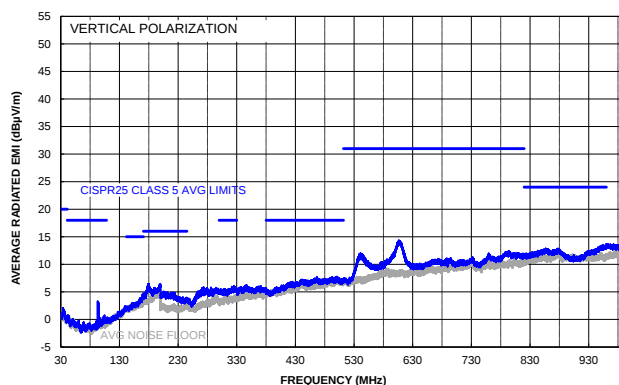
CISPR 25 Class 5 Peak Radiated Emissions

Vertical, 30MHz to 1GHz



CISPR 25 Class 5 Average Radiated Emissions

Vertical, 30MHz to 1GHz



Note:

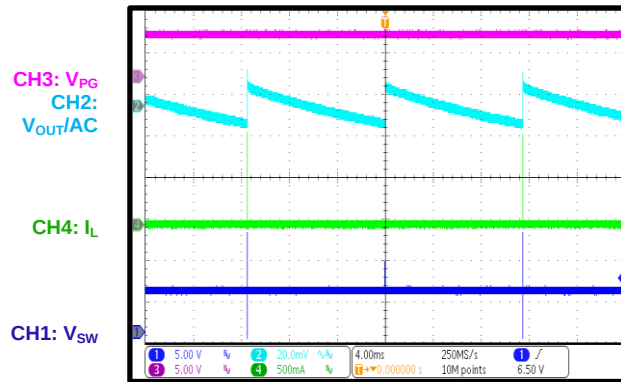
11) The EMC test results are based on the application circuit with EMI filters (see Figure 35 on page 79).

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 2.2μH, C_{OUT} = 2 x 22μF, T_A = 25°C, unless otherwise noted.

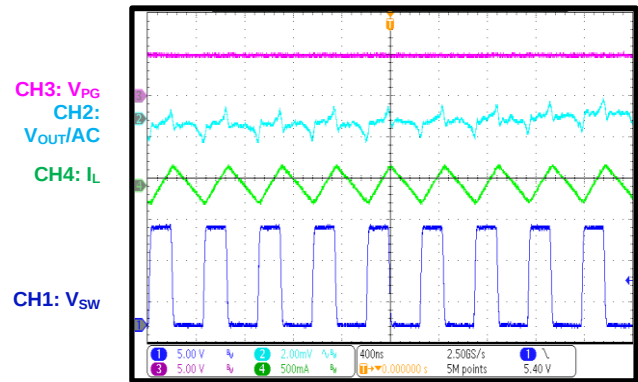
Steady State

AAM mode, I_{OUT} = 0A



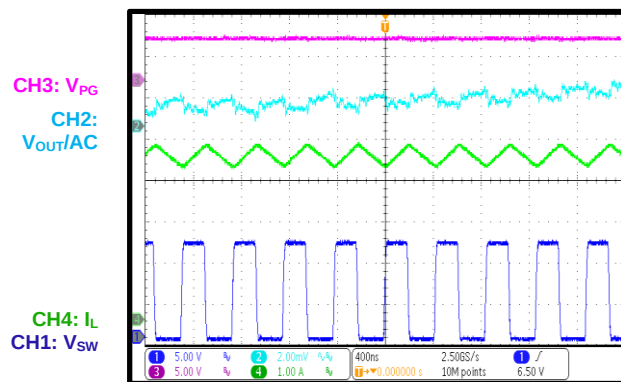
Steady State

FCCM, I_{OUT} = 0A



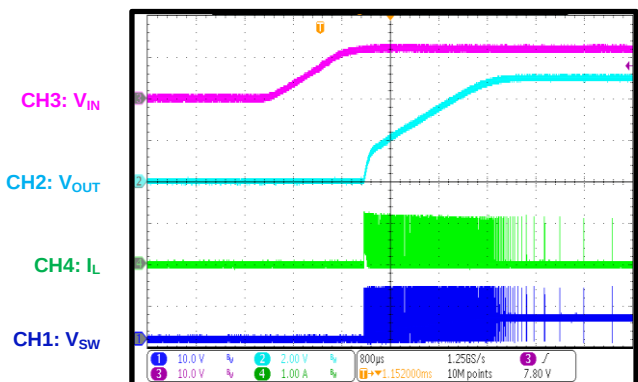
Steady State

I_{OUT} = 4A



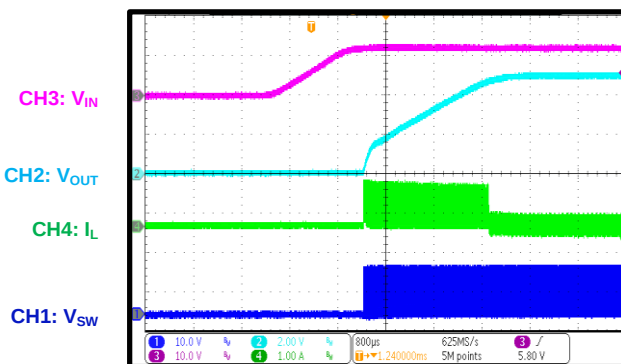
Start-Up through VIN

AAM mode, I_{OUT} = 0A



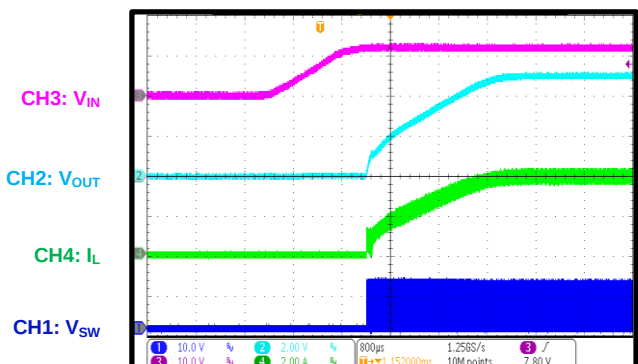
Start-Up through VIN

FCCM, I_{OUT} = 0A



Start-Up through VIN

I_{OUT} = 4A

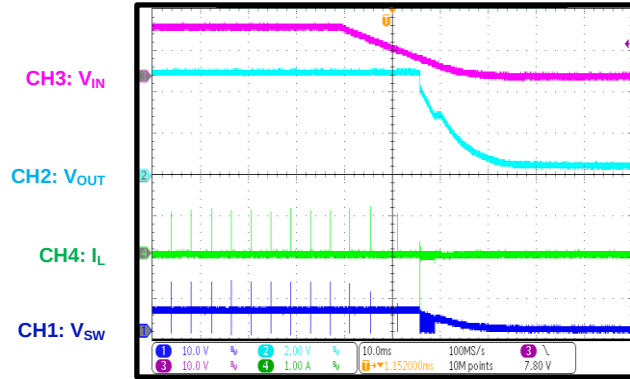


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 2.2μH, C_{OUT} = 2 x 22μF, T_A = 25°C, unless otherwise noted.

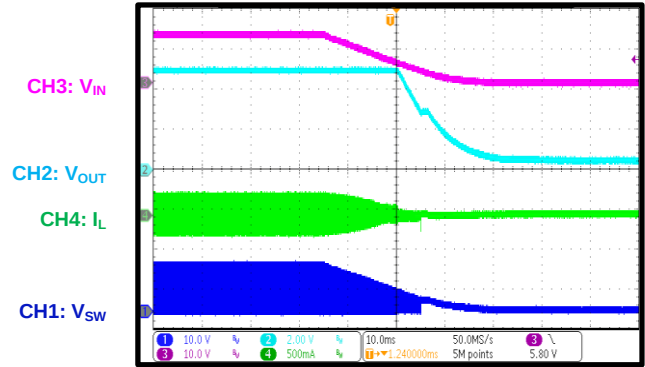
Shutdown through VIN

AAM mode, I_{OUT} = 0A



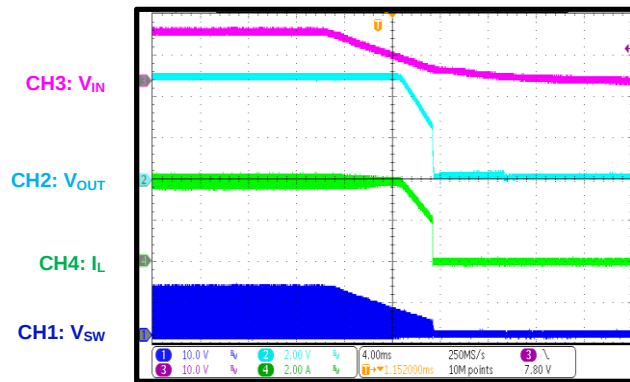
Shutdown through VIN

FCCM, I_{OUT} = 0A



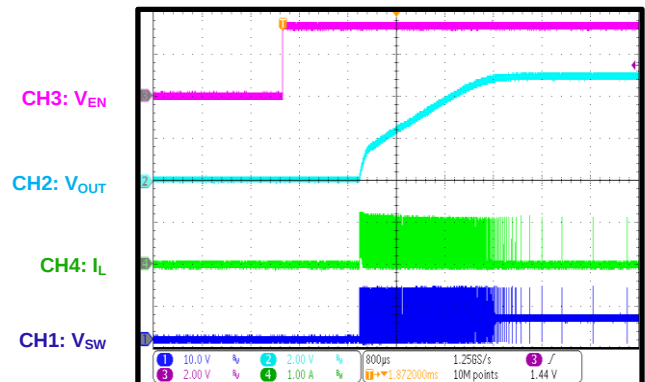
Shutdown through VIN

I_{OUT} = 4A



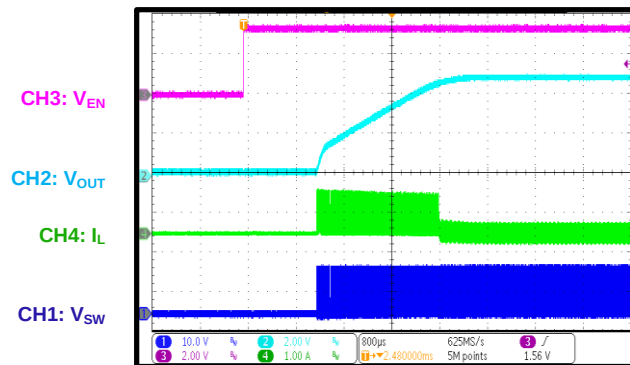
Start-Up through EN

AAM mode, I_{OUT} = 0A



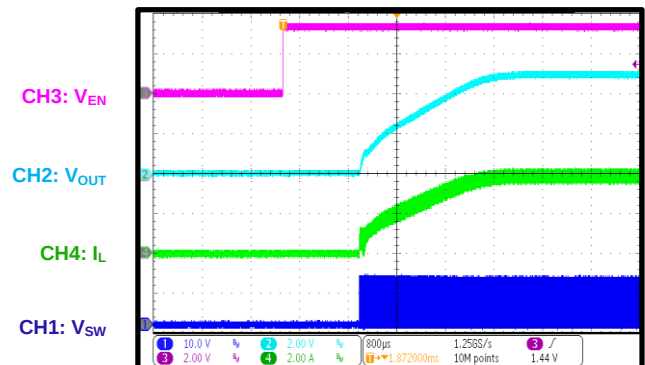
Start-Up through EN

FCCM, I_{OUT} = 0A



Start-Up through EN

I_{OUT} = 4A

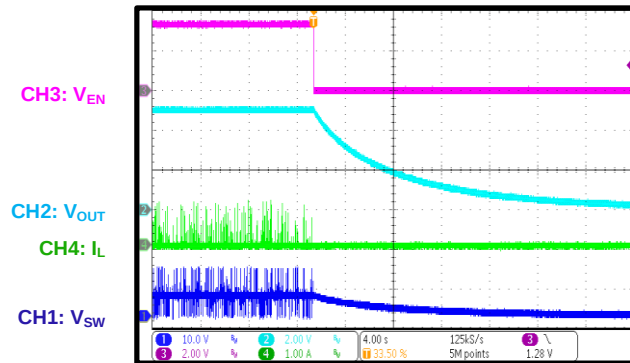


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 2.2μH, C_{OUT} = 2 x 22μF, T_A = 25°C, unless otherwise noted.

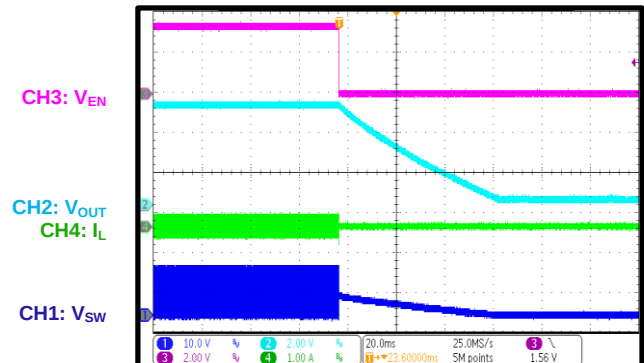
Shutdown through EN

AAM mode, I_{OUT} = 0A



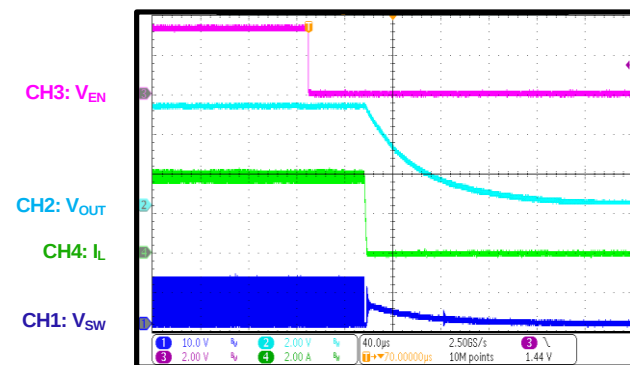
Shutdown through EN

FCCM, I_{OUT} = 0A



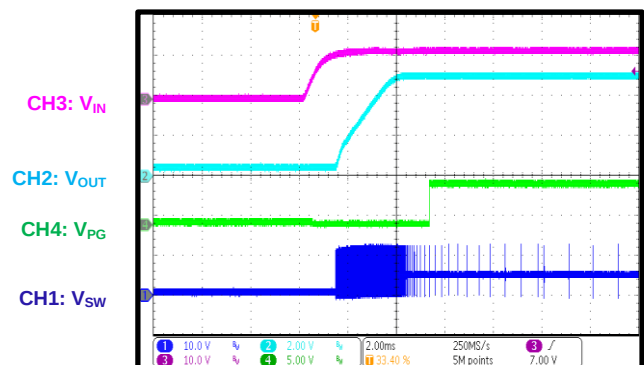
Shutdown through EN

I_{OUT} = 4A



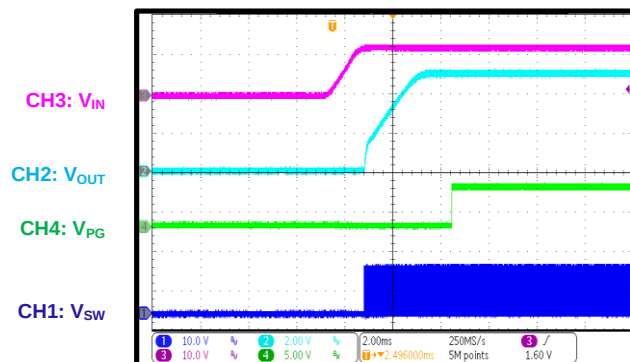
PG Start-Up through VIN

AAM mode, I_{OUT} = 0A



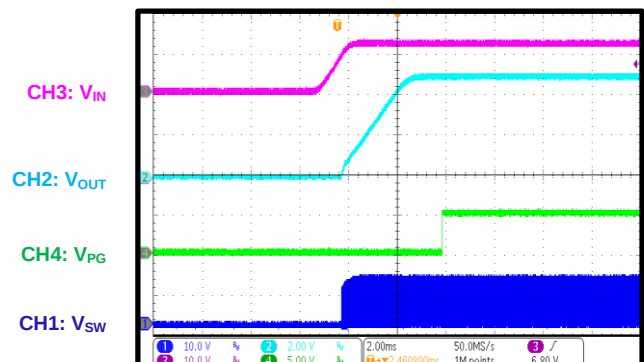
PG Start-Up through VIN

FCCM, I_{OUT} = 0A



PG Start-Up through VIN

I_{OUT} = 4A

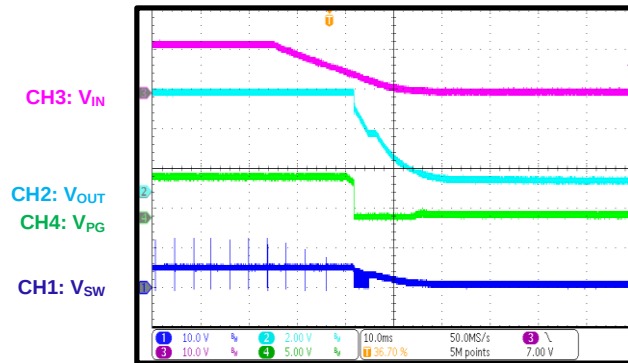


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 2.2μH, C_{OUT} = 2 x 22μF, T_A = 25°C, unless otherwise noted.

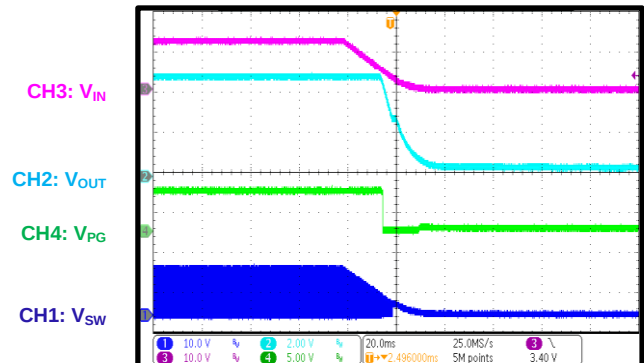
PG Shutdown through VIN

AAM mode, I_{OUT} = 0A



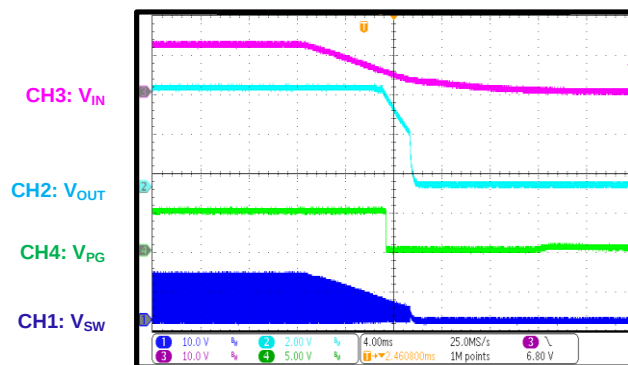
PG Shutdown through VIN

FCCM, I_{OUT} = 0A



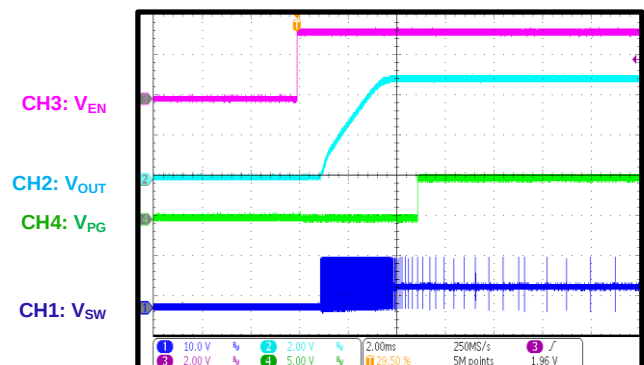
PG Shutdown through VIN

I_{OUT} = 4A



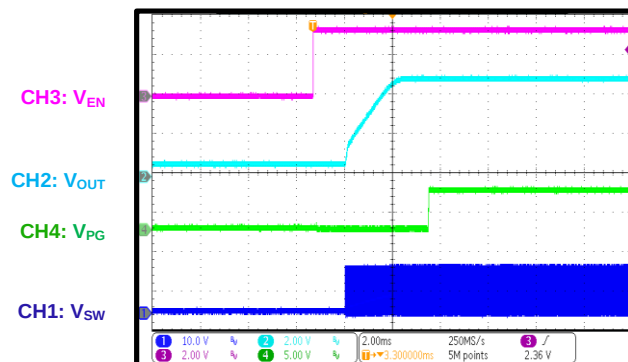
PG Start-Up through EN

AAM mode, I_{OUT} = 0A



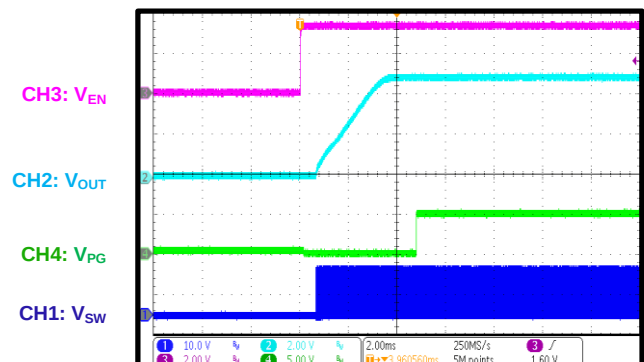
PG Start-Up through EN

FCCM, I_{OUT} = 0A



PG Start-Up through EN

I_{OUT} = 4A

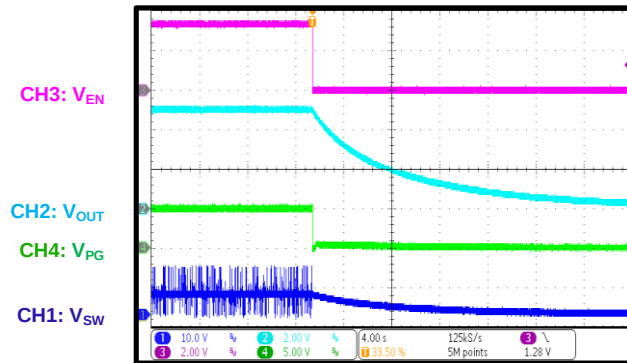


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN} = 12V$, $V_{OUT} = 5V$, $f_{SW} = 2.2MHz$, $L = 2.2\mu H$, $C_{OUT} = 2 \times 22\mu F$, $T_A = 25^\circ C$, unless otherwise noted.

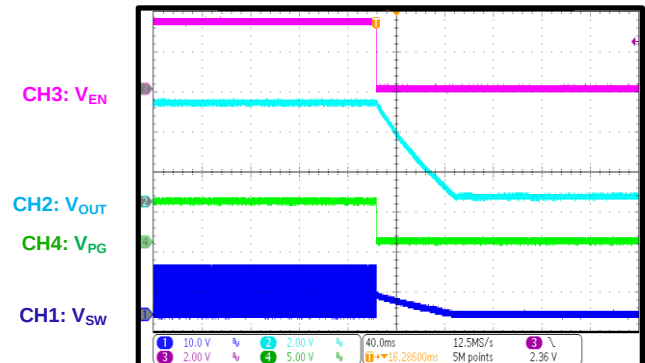
PG Shutdown through EN

AAM mode, $I_{OUT} = 0A$



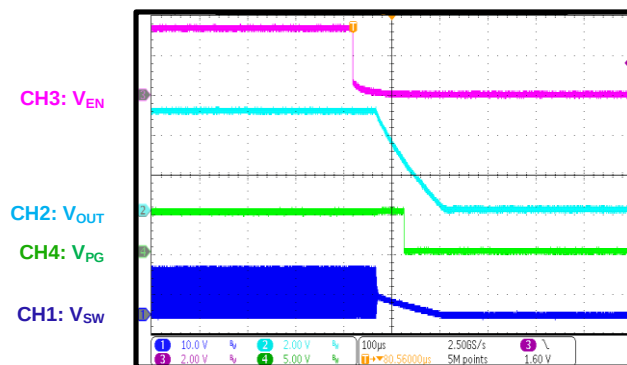
PG Shutdown through EN

FCCM, $I_{OUT} = 0A$



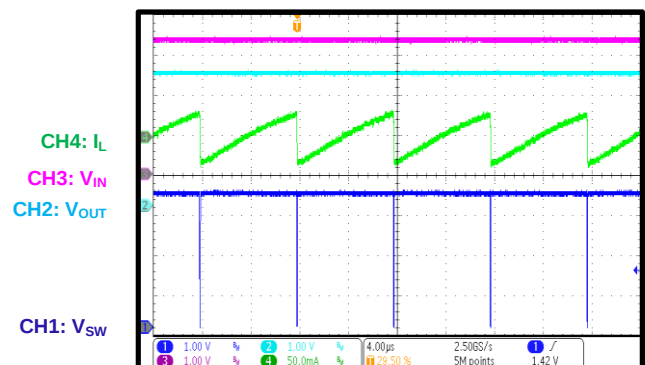
PG Shutdown through EN

$I_{OUT} = 4A$



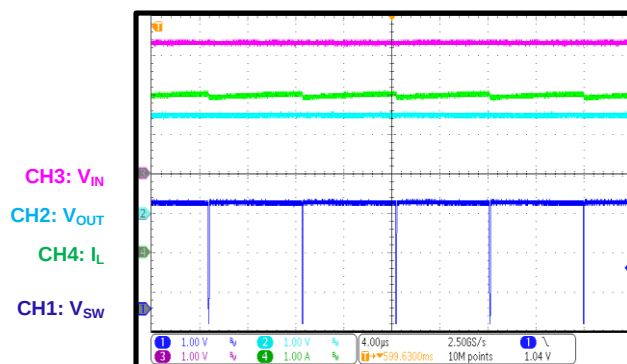
Low-Dropout Mode

$I_{OUT} = 0A$, $V_{IN} = 3.3V$



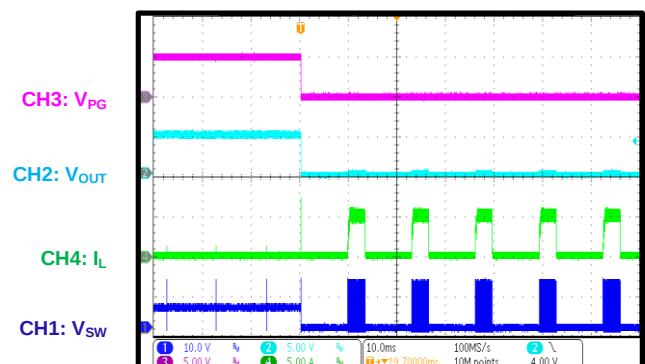
Low-Dropout Mode

$I_{OUT} = 4A$, $V_{IN} = 3.3V$



SCP Entry

AAM mode, $I_{OUT} = 0A$

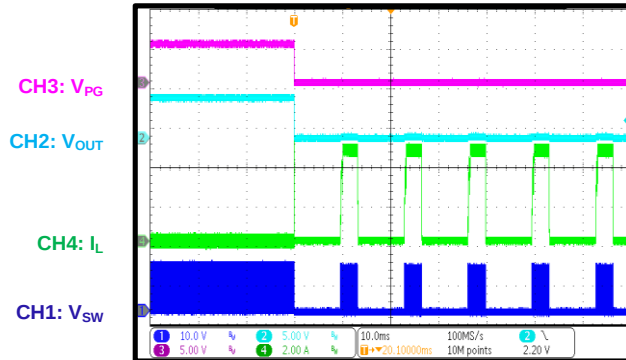


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN} = 12V$, $V_{OUT} = 5V$, $f_{SW} = 2.2MHz$, $L = 2.2\mu H$, $C_{OUT} = 2 \times 22\mu F$, $T_A = 25^\circ C$, unless otherwise noted.

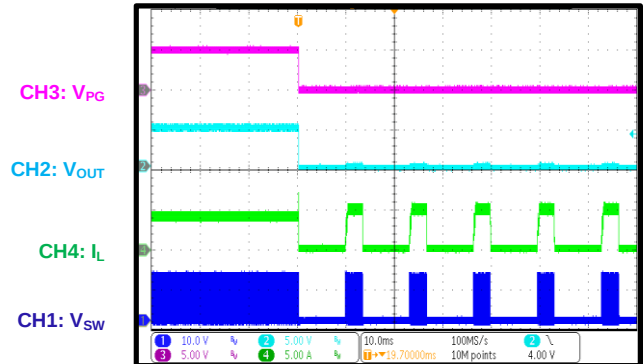
SCP Entry

FCCM, $I_{OUT} = 0A$



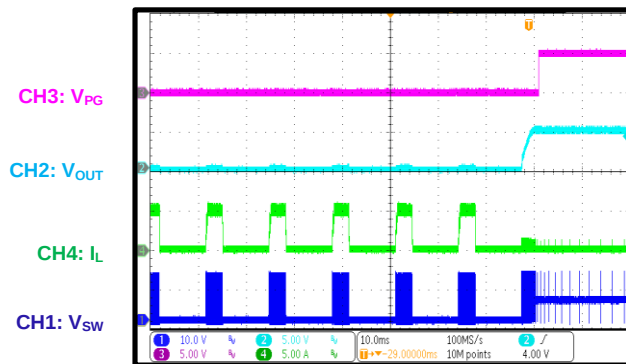
SCP Entry

$I_{OUT} = 4A$



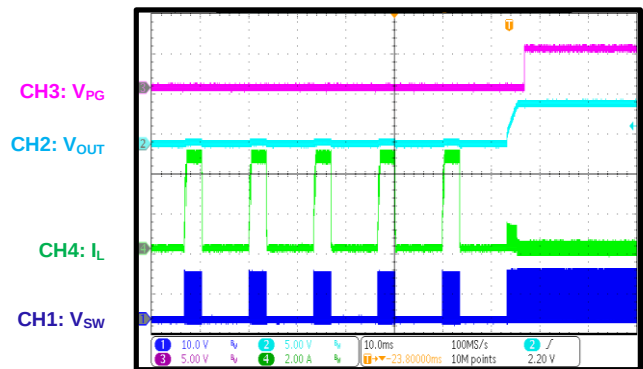
SCP Recovery

AAM mode, $I_{OUT} = 0A$



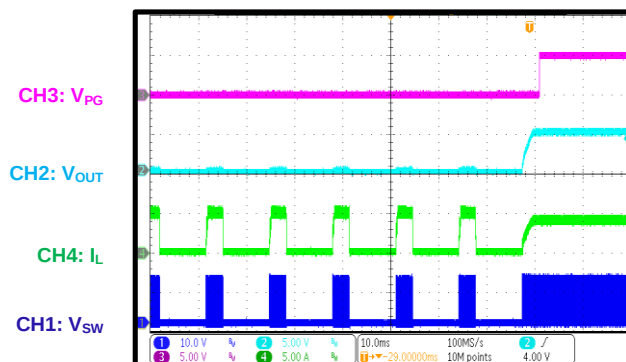
SCP Recovery

FCCM, $I_{OUT} = 0A$



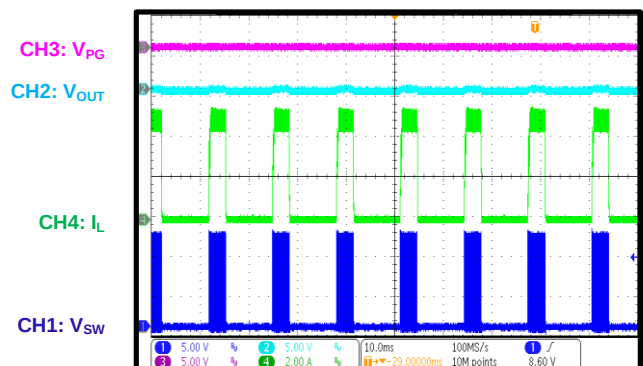
SCP Recovery

$I_{OUT} = 4A$



SCP Steady State

$I_{OUT} = 0A$

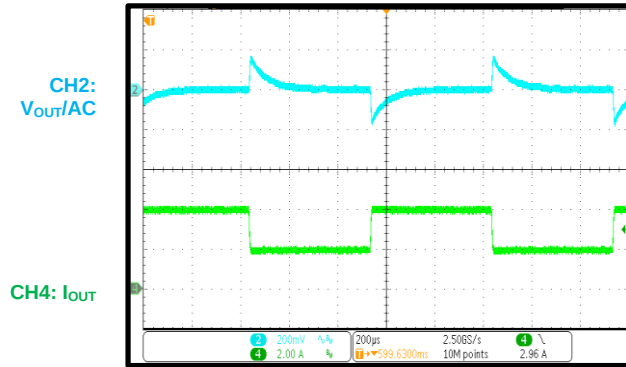


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN} = 12V$, $V_{OUT} = 5V$, $f_{SW} = 2.2MHz$, $L = 2.2\mu H$, $C_{OUT} = 2 \times 22\mu F$, $T_A = 25^\circ C$, unless otherwise noted.

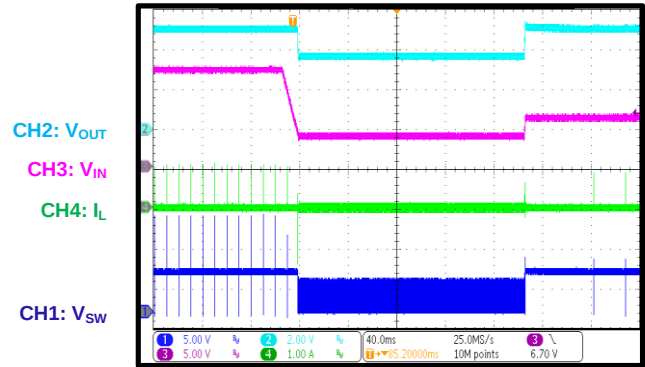
Load Transient

$I_{OUT} = 2A$ to $4A$, $1.6A/\mu s$



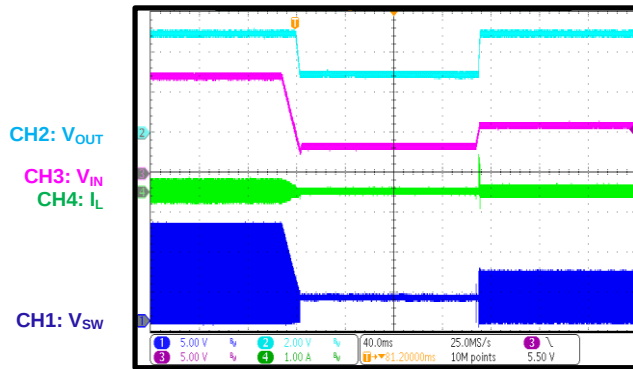
Cold Crank

$V_{IN} = 12V$ to $3.3V$ to $6V$, AAM mode, $I_{OUT} = 0A$



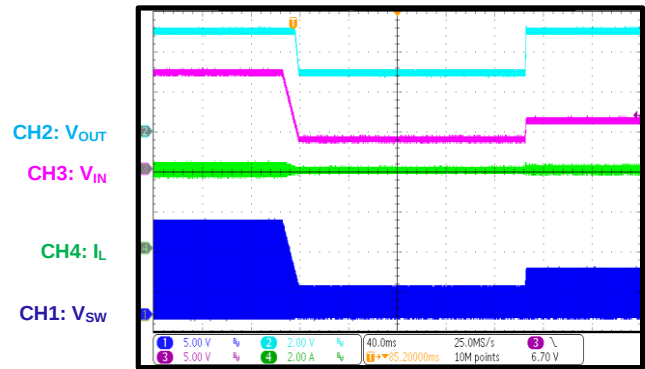
Cold Crank

$V_{IN} = 12V$ to $3.3V$ to $6V$, FCCM, $I_{OUT} = 0A$



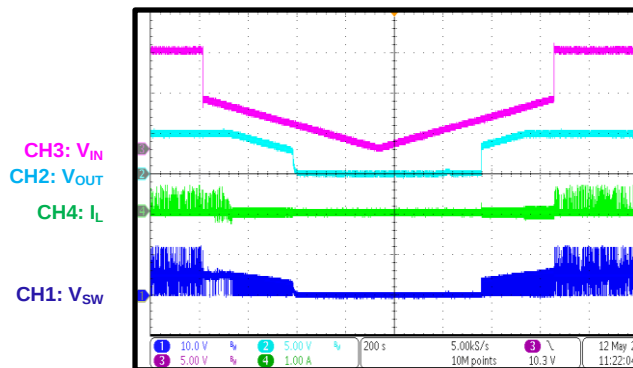
Cold Crank

$V_{IN} = 12V$ to $3.3V$ to $6V$, $I_{OUT} = 4A$



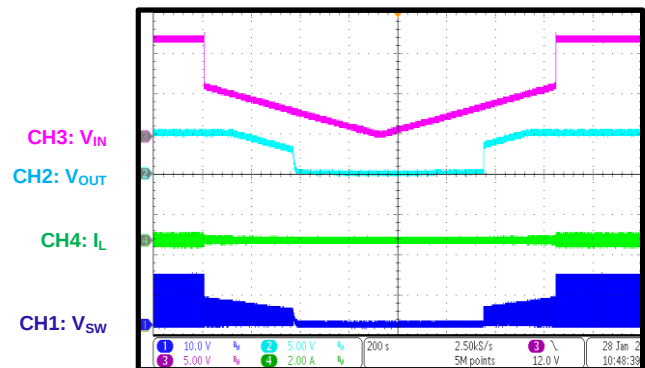
V_{IN} Ramps Down and Up

$V_{IN} = 6V$ to $0V$, $0.5V/min$, AAM mode, $I_{OUT} = 0A$



V_{IN} Ramps Down and Up

$V_{IN} = 6V$ to $0V$, $0.5V/min$, FCCM, $I_{OUT} = 0A$

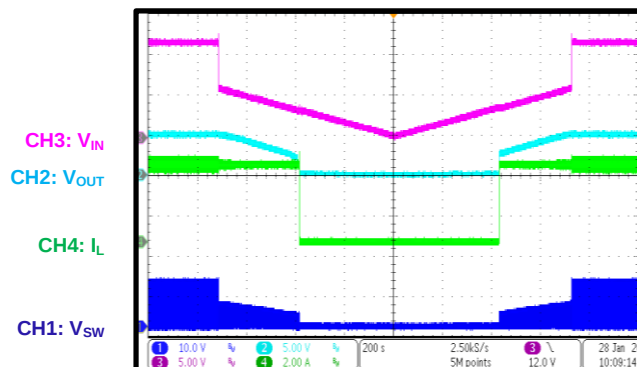


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

$V_{IN} = 12V$, $V_{OUT} = 5V$, $f_{SW} = 2.2MHz$, $L = 2.2\mu H$, $C_{OUT} = 2 \times 22\mu F$, $T_A = 25^\circ C$, unless otherwise noted.

V_{IN} Ramps Down and Up

$V_{IN} = 6V$ to $0V$, $0.5V/min$, $I_{OUT} = 4A$



FUNCTIONAL BLOCK DIAGRAMS

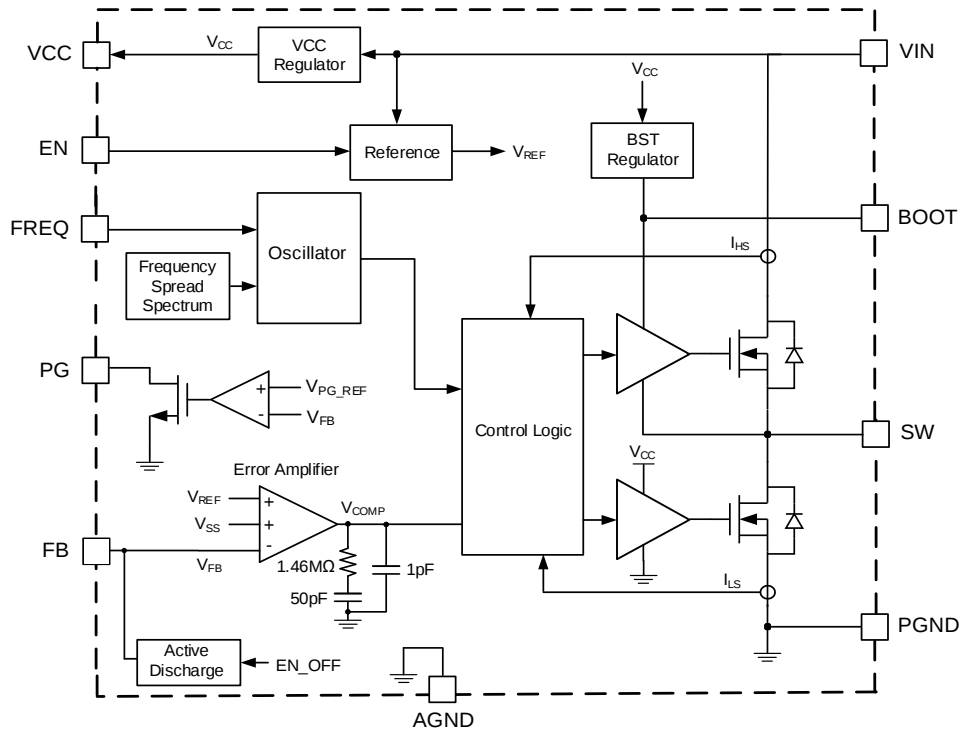


Figure 4: Functional Block Diagram (Adjustable-Output Version)

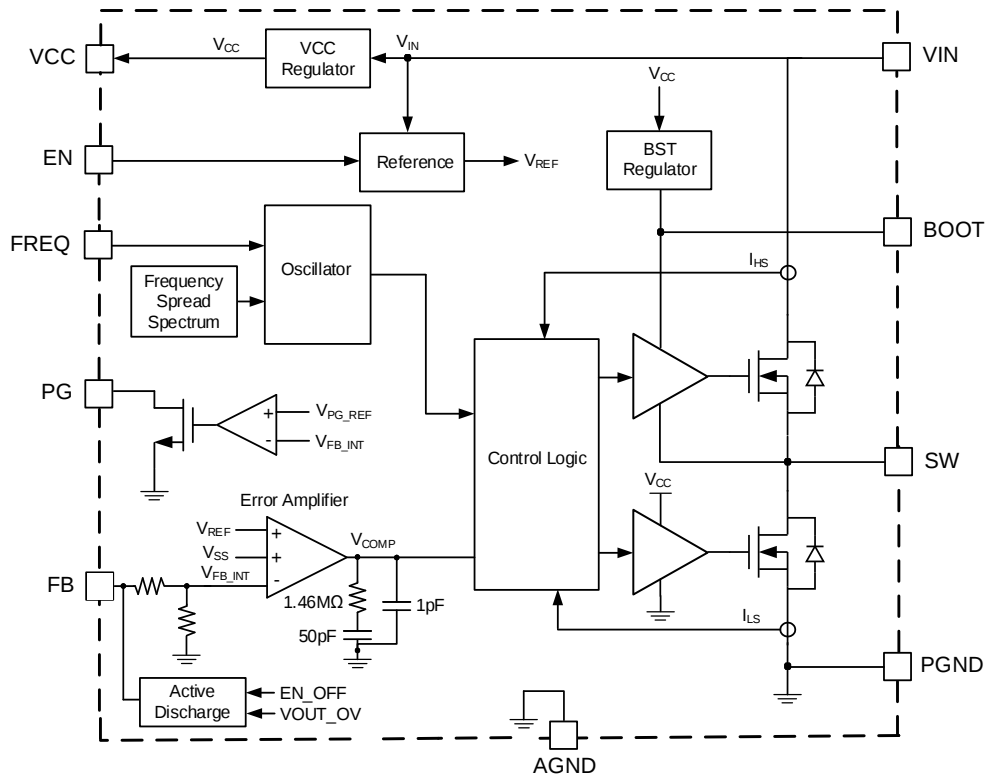


Figure 5: Functional Block Diagram (Fixed-Output Version)

OPERATION

The MPQ3524 is a synchronous, step-down switching regulator with integrated, internal high-side and low-side power MOSFETs (HS-FET and LS-FET, respectively). It provides 0.5A to 3A of continuous output current (I_{OUT}) and up to 4A of highly efficient I_{OUT} with peak current mode control.

The device features a wide input voltage (V_{IN}) range, a 350kHz to 2.5MHz configurable switching frequency (f_{SW}), internal soft start (SS), and precise current limiting. The MPQ3524's low operational quiescent current (I_Q) makes it well-suited for battery-powered applications.

Pulse-Width Modulation (PWM) Control

At moderate to high output currents, the MPQ3524 operates with fixed-frequency, peak current mode control to regulate the output voltage (V_{OUT}). A PWM cycle is initiated by the internal clock. At the rising edge of the clock, the HS-FET turns on and remains on until the control signal reaches the value set by the internal COMP voltage (V_{COMP}). If the control signal reaches V_{COMP} within 65ns, then the HS-FET remains on for at least the minimum on time (t_{ON_MIN}) (65ns).

When the HS-FET is off, the LS-FET turns on immediately and remains on until the next cycle starts or until the inductor current (I_L) drops below the zero-current detection (ZCD) threshold. The LS-FET remains off for at least the minimum off time (t_{OFF_MIN}) before the next cycle starts.

If the current in the HS-FET cannot reach the value set by V_{COMP} within one PWM period, then the HS-FET remains on and skips a turn-off operation. The HS-FET is forced off until it reached the value set by V_{COMP} , or its maximum on time (t_{ON_MAX}) (7 μ s) is reached. This mode extends the duty cycle, which achieves low dropout while $V_{IN} \approx V_{OUT}$.

Advanced Asynchronous Modulation (AAM) Mode and Forced Continuous Conduction Mode (FCCM)

When "Z" in the four-digit code "XXYZ" (see Table 1 on page 3) is configured as 0, 2, 4, or 6, the MPQ3524 works in advanced asynchronous

modulation (AAM) mode to optimize efficiency under light-load and no-load conditions.

When I_L approaches 0A under light loads, the MPQ3524 initiates asynchronous operation. If the load further decreases and V_{COMP} drops below the set value, then the MPQ3524 enters AAM mode (see Figure 6).

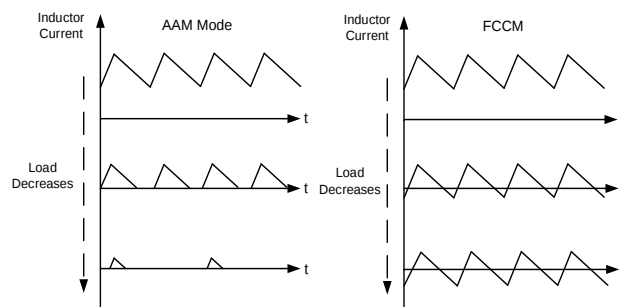


Figure 6: AAM Mode and FCCM

In AAM mode, the internal clock is reset once V_{COMP} reaches its set value, and the crossover time is used as a benchmark for the next clock. When the load increases and V_{COMP} exceeds its set value, the device operates in continuous conduction mode (CCM) or discontinuous conduction mode (DCM) with a constant f_{SW} .

When "Z" in the four-digit code "XXYZ" (see Table 1 on page 3) is configured as 1, 3, 5, or 7, the MPQ3524 works in forced continuous conduction mode (FCCM). The device works with a fixed frequency across a no-load to full-load range (see Figure 6). The advantages of FCCM are its controllable frequency and lower output voltage ripple (ΔV_{OUT}) under light-load conditions.

Error Amplifier (EA)

The error amplifier (EA) compares the FB pin voltage (V_{FB}) to the internal reference (0.8V), and outputs a current proportional to the difference between the two voltages. This I_{OUT} charges the compensation network to generate V_{COMP} , which provides the control signal for the power MOSFET's duty cycle.

During normal operation, the minimum V_{COMP} is clamped to 0.5V, and the maximum V_{COMP} is clamped to 2.5V. If the IC shuts down, V_{COMP} is pulled down to AGND internally.

Low-Dropout Mode

To improve dropout, the MPQ3524 is designed to operate at close to 100% duty cycle when the BOOT-to-SW voltage exceeds 2.5V.

When the MPQ3524 works in low-dropout mode, V_{COMP} is clamped to the maximum 2.5V. When V_{IN} suddenly increases from a lower voltage, the chip recovers from low-dropout mode. Due to the speed of the loop response, V_{COMP} cannot change rapidly accordingly. This may cause V_{OUT} overshoot.

The MPQ3524 provides a mechanism to reduce V_{OUT} overshoot when the control mode “Z” in the four-digit code “XYZ” (see Table 1 on page 3) is configured as 4, 5, 6, or 7. Once the device exits low-dropout mode using this mechanism, it initiates SS and V_{COMP} to reduce the HS-FET’s conduction duty cycle. Even if V_{IN} rapidly increases, V_{OUT} overshoot is minimized. Due to SS restarting, V_{OUT} experiences a drop during this period until SS reaches the set value again.

Frequency Spread Spectrum (FSS)

The MPQ3524 employs a 15kHz modulation frequency with a maximum 128-step triangular profile to spread the internal f_{SW} across a 20% ($\pm 10\%$) window. The steps vary with the set f_{SW} to ensure that the exact f_{SW} steps cycle by cycle (see Figure 7).

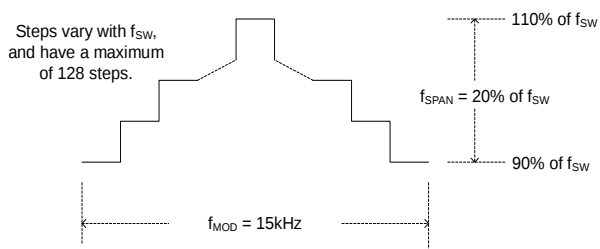


Figure 7: Frequency Spread Spectrum

Sidebands are created by modulating f_{SW} via the triangle modulation waveform. The emission power of the fundamental f_{SW} and its harmonics is reduced. This significantly reduces peak EMI noise.

This function can also be configured on or off using the control mode “Z” in the four-digit code, “XYZ” (see Table 1 on page 3).

Soft Start (SS)

Soft start (SS) is implemented to prevent the converter’s V_{OUT} from overshooting during start-up. The soft-start time (t_{SS}) is fixed internally.

When t_{SS} starts, the soft-start voltage (V_{SS}) rises from 0V to 1.2V with a set slew rate. If V_{SS} drops below the internal reference voltage (V_{REF}) (0.8V), then V_{SS} takes over, and the EA uses V_{SS} as its reference. If V_{SS} exceeds V_{REF} , the EA uses V_{REF} as its reference.

When the IC is enabled by the EN pin, the first pulse is received after 830 μ s. During this period, VCC is regulated and the internal bias and charging of the compensator network are completed. After another 2.9ms, V_{OUT} ramps up and reaches the set value. Then SS completes after 1.5ms. The PG pin is also pulled high after a 70 μ s delay.

Start-Up and Shutdown

If both V_{IN} and the EN voltage (V_{EN}) exceed their respective thresholds, the IC starts up. The reference block starts up first to generate a stable V_{REF} and reference currents. Then the internal regulator is enabled to provide a stable supply for the remaining circuitries.

Once the internal supply rail is up, the internal circuits start to work. If the BOOT voltage (V_{BOOT}) does not reach its refresh rising threshold (about 2.5V), then the LS-FET turns on to charge BOOT. The HS-FET remains off during this charging period. When the SS block is enabled, V_{OUT} starts to ramp up slowly and smoothly reaches its target within 5ms.

Three events can shut down the chip: EN going low, V_{IN} falling below its under-voltage lockout (UVLO) threshold, and thermal shutdown. During shutdown, the signaling path is blocked first to avoid any fault triggering. Then V_{COMP} is pulled down and the floating driver disables the HS-FET.

Bootstrap Charging

The voltage between BOOT and SW ($V_{BOOT-SW}$) is regulated to about 5V by the dedicated internal bootstrap regulator. If $V_{BOOT-SW}$ is below its regulated value, then an N-channel MOSFET pass transistor connected between VCC and BOOT turns on to charge the bootstrap capacitor (C_{BOOT}).

The external circuit must provide sufficient voltage headroom to facilitate charging. When the HS-FET is on, V_{BOOT} exceeds the VCC voltage (V_{CC}), meaning C_{BOOT} cannot be charged.

Under conditions with higher duty cycles, the time available for bootstrap charging is shorter, meaning C_{BOOT} may not be charged sufficiently. In this case, the external circuit has insufficient voltage and time to charge C_{BOOT} . External circuitry can be used to ensure that the bootstrap voltage remains in the normal operation region.

If V_{BOOT} reaches its UVLO threshold, the HS-FET turns off, and the LS-FET turns on with t_{OFF_MIN} to refresh V_{BOOT} with the set f_{SW} .

Pre-Biased Start-Up

If V_{FB} exceeds V_{SS} during start-up, this means that the output has a pre-biased voltage. Neither the HS-FET nor LS-FET turns on until V_{SS} exceeds V_{FB} .

Peak and Valley Current Limits

Both the HS-FET and LS-FET have cycle-by-cycle current-limit protection. When I_L reaches the high-side (HS) peak current limit while the HS-FET is on, the HS-FET is forced off immediately to prevent the current from rising further. The LS-FET remains on until I_L drops below the valley current limit.

When the LS-FET is on, the next clock's rising edge is held until I_L drops below the low-side (LS) valley current limit. Then I_L can drop to a sufficiently low value when the HS-FET turns on again. This current limit scheme prevents current runaway if an overload or short-circuit event occurs.

Reverse Current Limit

The reverse current direction is from the SW node to the PGND node. The LS reverse current limit ($I_{LIMIT_REVERSE}$) threshold is 2A. Once I_L reaches the current limit, the LS-FET immediately turns

off and the HS-FET turns on. After the control signal reaches V_{COMP} , the HS-FET turns off and the LS-FET turns on again. The current limit prevents the negative current from dropping too low and potentially damaging the components.

Short-Circuit Protection (SCP)

If the output is shorted to ground, V_{OUT} drops below 93% of its nominal output and the valley current limit is triggered, then the MPQ3524 shuts down and begins discharging V_{SS} . The device restarts with a full SS when V_{SS} is fully discharged. This hiccup process is repeated until the fault is removed.

Output Over-Voltage Protection (OVP) and Discharge

In AAM mode, the MPQ3524 stops switching when V_{OUT} exceeds its nominal V_{OUT} . In FCCM, the MPQ3524 stops switching if V_{OUT} exceeds 130% of its nominal regulation value.

If V_{OUT} exceeds 130% of its nominal regulation value, an internal 270 Ω discharge path (with a 4mA saturation current) between FB and PGND is activated to discharge V_{OUT} . This discharge path only can be activated with the fixed-output version. In FCCM, the MPQ3524 resumes switching when V_{OUT} drops back to 125% of its nominal value, then the discharge path is disabled. In AAM mode, the discharge path is also disabled when V_{OUT} drops back to 125% of its nominal value but resumes switching only when V_{OUT} drops below its nominal value.

The V_{OUT} discharge path is also activated if an EN shutdown occurs, whether it is a fixed-output version or an adjustable-output version.

Thermal Shutdown

Thermal shutdown protects the device from thermal runaway. If the silicon die temperature exceeds its upper threshold (about 175°C), the device shuts down the power MOSFETs. If the temperature drops below its lower threshold (about 155°C), the thermal shutdown condition is removed, and the device is enabled again.

APPLICATION INFORMATION

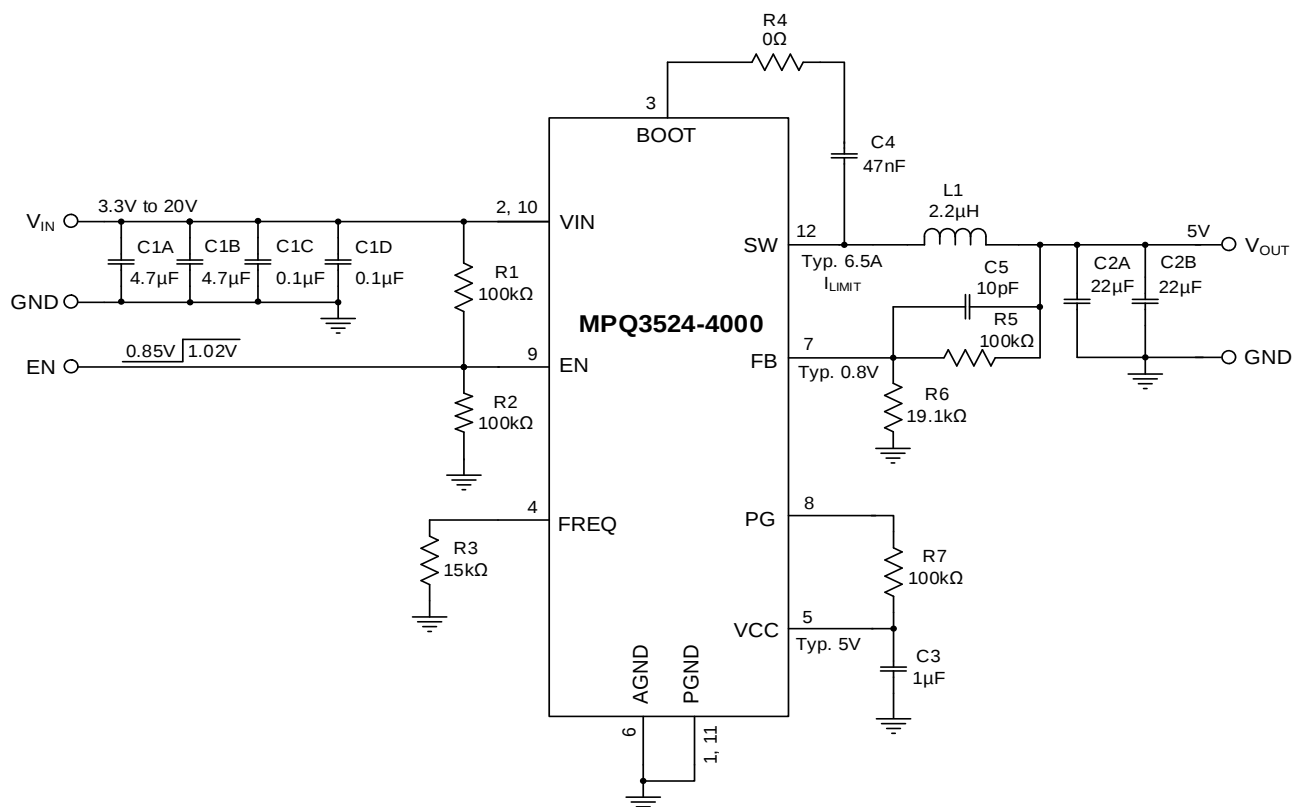


Figure 8: Typical Application Circuit ($V_{OUT} = 5V$, $f_{SW} = 2.2MHz$, 4A Version)

Table 2: Design Guide Index

Pin #	Pin Name	Component	Value	Design Guide Index
1, 11	PGND	-	-	Power Ground and Analog Ground Connection (Pins 1, 6, and 11)
2, 10	VIN	C1A, C1B, C1C, C1D	4.7µF, 4.7µF, 100nF, 100nF	Selecting the Input Capacitors (VIN, Pins 2 and 10)
3	BOOT	R4, C4	0Ω, 47nF	Floating Driver and Bootstrap Charging (BOOT, Pin 3)
4	FREQ	R3	15kΩ	Setting the Switching Frequency (FREQ, Pin 4)
5	VCC	C3	1µF	Internal VCC (VCC, Pin 5)
6	AGND	-	-	Power Ground and Analog Ground Connection (Pins 1, 6, and 11)
7	FB	R5, R6, C5	100kΩ, 19.1kΩ, 10pF	Feedback (FB, Pin 7)
8	PG	R7	100kΩ	Power Good (PG) Indicator (PG, Pin 8)
9	EN	R1, R2	100kΩ, 100kΩ	Enable (EN) and Under-Voltage Lockout (UVLO) (EN, Pin 9)
12	SW	L1, C2A, C2B	2.2µH, 22µF, 22µF	Selecting the Inductor (SW, Pin 12), Selecting the Output Capacitors (SW, Pin 12)

Power Ground and Analog Ground Connection (Pins 1, 6, and 11)

See the PCB Layout Guidelines on page 67 for more details.

Selecting the Input Capacitors (VIN, Pins 2 and 10)

The step-down converter has a discontinuous input current (I_{IN}) and requires a capacitor to supply AC current to the converter while maintaining the DC input voltage (V_{IN}). Use low-ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are highly recommended due to their low ESR and small temperature coefficients.

For most applications, use a 4.7μF to 10μF capacitor. It is strongly recommended to use an additional, lower-value capacitor (e.g. 0.1μF) with a small package size (e.g. 0603) to absorb high-frequency switching noise. Place the smaller capacitor as close to VIN and PGND as possible.

Since the input capacitor (C_{IN}) absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in C_{IN} (I_{CIN}) can be estimated with Equation (1):

$$I_{CIN} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (1)$$

The worst-case condition occurs at V_{IN} = 2 × V_{OUT}, which can be calculated with Equation (2):

$$I_{CIN} = \frac{I_{LOAD}}{2} \quad (2)$$

For simplification, choose C_{IN} with an RMS current rating greater than half of the maximum load current. C_{IN} can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, add a small, high-quality ceramic capacitor (e.g. 0.1μF) as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide a sufficient charge for preventing excessive voltage ripple at the input. The input voltage ripple (ΔV_{IN}) caused by the capacitance can be estimated with Equation (3):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (3)$$

Floating Driver and Bootstrap Charging (BOOT, Pin 3)

The bootstrap capacitor (C4, also called C_{BOOT}) is recommended to be between 22nF and 100nF.

It is not recommended to place a resistor (R_{BOOT}) in series with C_{BOOT}, unless there is a strict EMI requirement. R_{BOOT} enhances EMI performance and reduces voltage stress at high input voltages; however, it also generates additional power consumption and reduces efficiency. If necessary, R_{BOOT} should be below 4Ω.

Setting the Switching Frequency (FREQ, Pin 4)

A frequency resistor (R3, also called R_{FREQ}) can set f_{SW} (see Table 3 as well as the f_{SW} vs. R_{FREQ} curves on pages 46 and 47).

The MPQ3524's f_{SW} can be configured by an external resistor (R_{FREQ}) connected between the FREQ pin and ground. R_{FREQ} should be located between the FREQ pin and AGND, placed as close as possible to the device. Table 3 shows the relationship between f_{SW} and R_{FREQ}.

Table 3: f_{SW} vs. R_{FREQ}

R _{FREQ} (kΩ)	f _{SW} (kHz)	R _{FREQ} (kΩ)	f _{SW} (kHz)
100	355	30.1	1150
93.1	385	26.1	1300
86.6	415	22.6	1450
80.6	450	20.5	1600
75	480	19.6	1750
68.1	520	17.8	1900
59	600	16.2	2050
51.1	700	15	2200
40.2	850	14.3	2350
34.8	1000	13.3	2500

For MPQ3524-05x0, the part works in AAM mode to optimize efficiency under light-load conditions, where its real f_{SW} also depends on the depth of its AAM mode. The depth of AAM mode is related to the inductance and load. See the Typical Performance Characteristics curves on pages 46 and 47 for more details on the relationship between f_{SW} and R_{FREQ} under different loads and inductances.

It is not possible to have both a high f_{SW} and V_{IN} due to the HS-FET's limited minimum on time

(t_{ON_MIN}). The MPQ3524 control loop automatically sets the maximum possible f_{SW} to the set frequency, which also reduces excessive power loss. The output voltage (V_{OUT}) is regulated by varying the duration of the HS-FET's off time, which automatically reduces f_{SW} .

The device is guaranteed to comply with the HS-FET's t_{ON_MIN} . An advantage of this method is that the device works at the target f_{SW} for as long as possible, and f_{SW} only changes when the device operates at high input voltages.

Internal VCC (VCC, Pin 5)

The VCC capacitance (C3) is recommended to be 1 μ F.

Most of the internal circuitry is powered by the internal 5V VCC regulator. This regulator uses V_{IN} as its input and operates across the full V_{IN} range. If V_{IN} exceeds 5V, then V_{CC} is in full regulation. If V_{IN} drops below 5V, then the VCC output degrades.

Feedback (FB, Pin 7)

The feedback (FB) voltage (V_{FB}) is typically 0.8V, and its output can be adjusted. The external resistor divider connected to FB sets V_{OUT} (see Figure 9).

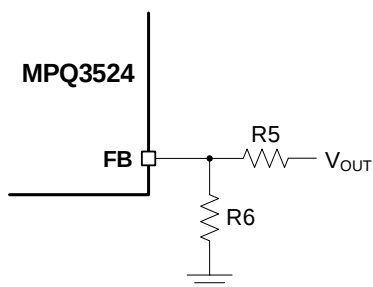


Figure 9: Feedback Divider Network for Adjustable-Output Version

R6 can be calculated with Equation (4):

$$R6 = \frac{R5}{\frac{V_{OUT}}{0.8V} - 1} \quad (4)$$

For the fixed-output version, the FB resistor dividers (R_{FB1} and R_{FB2}) are integrated internally. Connect FB directly to the output to set V_{OUT} . The following fixed outputs can be selected: 1V, 1.8V, 2.5V, 3V, 3.3V, 3.8V, and 5V (see Figure 10).

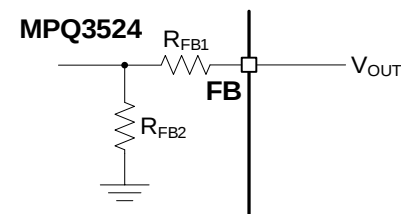


Figure 10: Feedback Divider Network for Fixed-Output Version

Table 4 shows the relationship between the internal R_{FB} and V_{OUT} .

Table 4: R_{FB} vs. V_{OUT}

V_{OUT} (V)	R_{FB1} (k Ω)	R_{FB2} (k Ω)
1	64	256
1.8	320	256
2.5	544	256
3	704	256
3.3	800	256
3.8	960	256
5	1344	256

A feedforward capacitor (C5) improves the phase margin and transient response of circuits that have output capacitors with low ESR.

Power Good (PG) Indicator (PG, Pin 8)

The power good (PG) resistor (R7, also called R_{PG}) should have a resistance of about 100k Ω .

The MPQ3524 includes an open-drain PG output that indicates whether the regulator's output is within a specific window of its nominal value. The PG indicator only works when V_{CC} exceeds its UVLO threshold.

If using PG, connect it to a logic high level power source (e.g. 3.3V) via a pull-up resistor. If V_{OUT} is within 94.5% to 105.5% of the nominal voltage, then PG goes high; if V_{OUT} exceeds 107% or drops below 93% of the nominal voltage, then PG goes low. Float PG if it is not used.

Enable (EN) and Under-Voltage Lockout (UVLO) (EN, Pin 9)

EN is a digital control pin that turns the regulator on and off.

Enabled by an External Logic High/Low Signal

If the EN voltage (V_{EN}) reaches 0.7V, the bottom gate (BG) does not turn on until V_{IN} exceeds 2.7V. BG then provides an accurate reference voltage (V_{REF}) for the EN threshold.

Pull EN above its rising threshold (about 1.02V) to start up the device. Pull EN below 0.85V to shut down the device. There is no internal pull-up or pull-down resistor connected to the EN pin. Do not float EN. If the control signal cannot give an accurate high or low logic, then an external pull-up or pull-down resistor is required.

Configurable V_{IN} Under-Voltage Lockout (UVLO) Threshold

The MPQ3524 has an internal, fixed under-voltage lockout (UVLO) threshold. The rising threshold is 3.65V, and the falling threshold is about 2.9V. For applications that require a higher UVLO threshold, an external resistor divider can be placed between VIN and EN to achieve a higher equivalent UVLO threshold (see Figure 11).

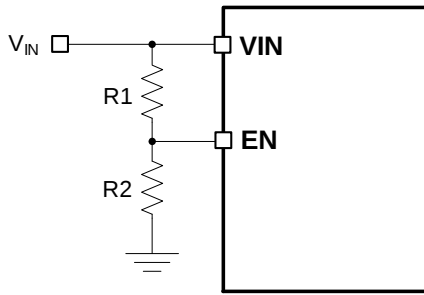


Figure 11: Adjustable UVLO Using the EN Divider

The UVLO rising threshold (V_{IN_UVLO_RISING}) can be calculated with Equation (5):

$$V_{IN_UVLO_RISING} = \left(1 + \frac{R1}{R2}\right) \times V_{EN_RISING} \quad (5)$$

The UVLO falling threshold (V_{IN_UVLO_FALLING}) can be calculated with Equation (6):

$$V_{IN_UVLO_FALLING} = \left(1 + \frac{R1}{R2}\right) \times V_{EN_FALLING} \quad (6)$$

Where V_{EN_RISING} is 1.02V, and V_{EN_FALLING} is 0.85V.

If EN is not used to turn the device on and off, then connect EN to a high-voltage source (e.g. VIN) to turn the device on by default.

Selecting the Inductor (SW, Pin 12)

The inductance (L1) can be estimated with Equation (7):

$$L1 = \frac{V_{OUT}}{f_{SW} \times \Delta I_L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (7)$$

Where ΔI_L is the peak-to-peak inductor ripple current.

A 1μH to 10μH inductor with a DC current rating at least 25% higher than the maximum load current is recommended for most applications. For higher efficiency, choose an inductor with a lower DC resistance. A larger-value inductor results in less ripple current and a lower output ripple voltage; however, it also has a larger physical size, higher series resistance, and lower saturation current. A good rule to determine the inductance is to allow the inductor ripple current to be approximately 30% of the maximum load current.

The peak inductor current (I_{L_PEAK}) can be calculated with Equation (8)

$$I_{L_PEAK} = I_{LOAD} + \frac{V_{OUT}}{2 \times f_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (8)$$

Choose an inductor that does not saturate under I_{L_PEAK}.

The output voltage ripple (ΔV_{OUT}) can be estimated with Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}}\right) \quad (9)$$

Where L is the inductance, and R_{ESR} is the equivalent series resistance (ESR) of the output capacitor.

Selecting the Output Capacitors (SW, Pin 12)

The output capacitor (C_{OUT}) maintains the DC V_{OUT}. Use ceramic, tantalum, or low-ESR electrolytic capacitors. For the best results, use low-ESR capacitors to keep ΔV_{OUT} low.

For ceramic capacitors, the capacitance dominates the impedance at f_{SW} and causes the majority of ΔV_{OUT}. For simplification, ΔV_{OUT} can be calculated with Equation (10):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^2 \times L \times C_{OUT}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (10)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at f_{SW}. For simplification, ΔV_{OUT} can be estimated with Equation (11):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (11)$$

When selecting C_{OUT}, consider the allowable overshoot in V_{OUT} if the load is suddenly removed. In this scenario, energy stored in the inductor is transferred to C_{OUT}, causing its voltage to rise. To achieve an optimal overshoot relative to the regulated voltage, C_{OUT} can be estimated with Equation (12):

$$C_{OUT} = \frac{I_{OUT}^2 \times L}{V_{OUT}^2 \times ((V_{OUT_MAX} / V_{OUT})^2 - 1)} \quad (12)$$

Where V_{OUT_MAX} / V_{OUT} is the allowable maximum overshoot.

After calculating the capacitance that meets both the ripple and overshoot requirements, choose the larger capacitance.

The C_{OUT} characteristics also affect the stability of the regulation system. The MPQ3524 can be optimized for a wide range of capacitances and ESR values.

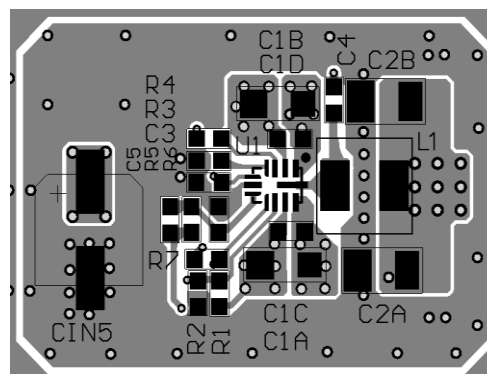
PCB Layout Guidelines ⁽¹²⁾

Efficient PCB layout, especially for C_{IN} placement, is critical for stable operation. A 4-layer layout is strongly recommended to improve thermal performance. For the best results, refer to Figure 12 and follow the guidelines below:

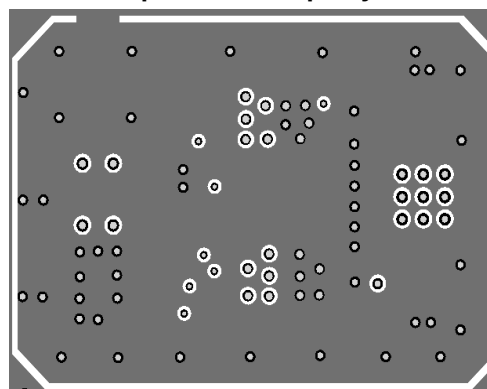
1. Place the symmetric input capacitors as close to VIN and PGND as possible.
2. Connect a large ground plane directly to PGND.
3. If the bottom layer is a ground plane, add vias near PGND.
4. Ensure that the high-current paths at PGND and VIN have short, direct, and wide traces.
5. Place the ceramic input capacitor, especially the small package size (0603) input bypass capacitor, as close to VIN and PGND as possible to minimize high-frequency noise.
6. Keep the connection between the input capacitor and VIN as short and wide as possible.
7. Place the VCC capacitor as close to VCC and AGND as possible.
8. Route SW and BOOT away from sensitive analog areas, such as FB.
9. Place the feedback resistors close to the chip to ensure that the trace connected to FB is as short as possible.
10. Use multiple vias to connect the power planes to the internal layers.

Note:

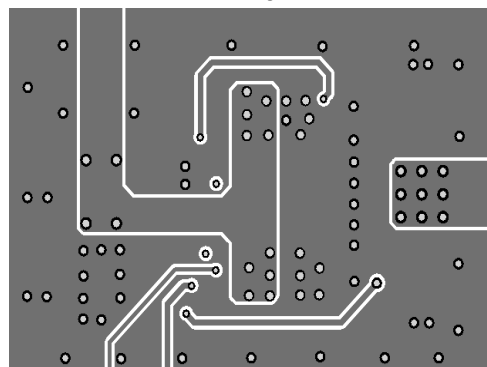
- 12) The recommended PCB layout is based on Figure 8 on page 62.



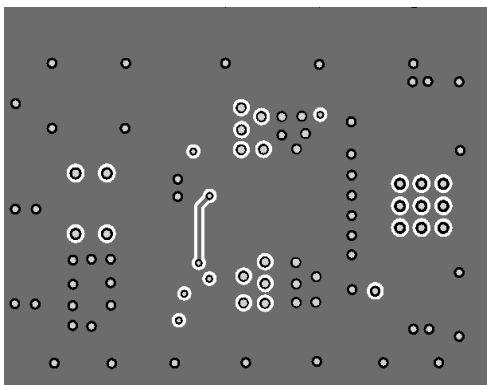
Top Silk and Top Layer



Mid-Layer 1



Mid-Layer 2



Bottom Layer and Bottom Silk

Figure 12: Recommended PCB Layout

TYPICAL APPLICATION CIRCUITS

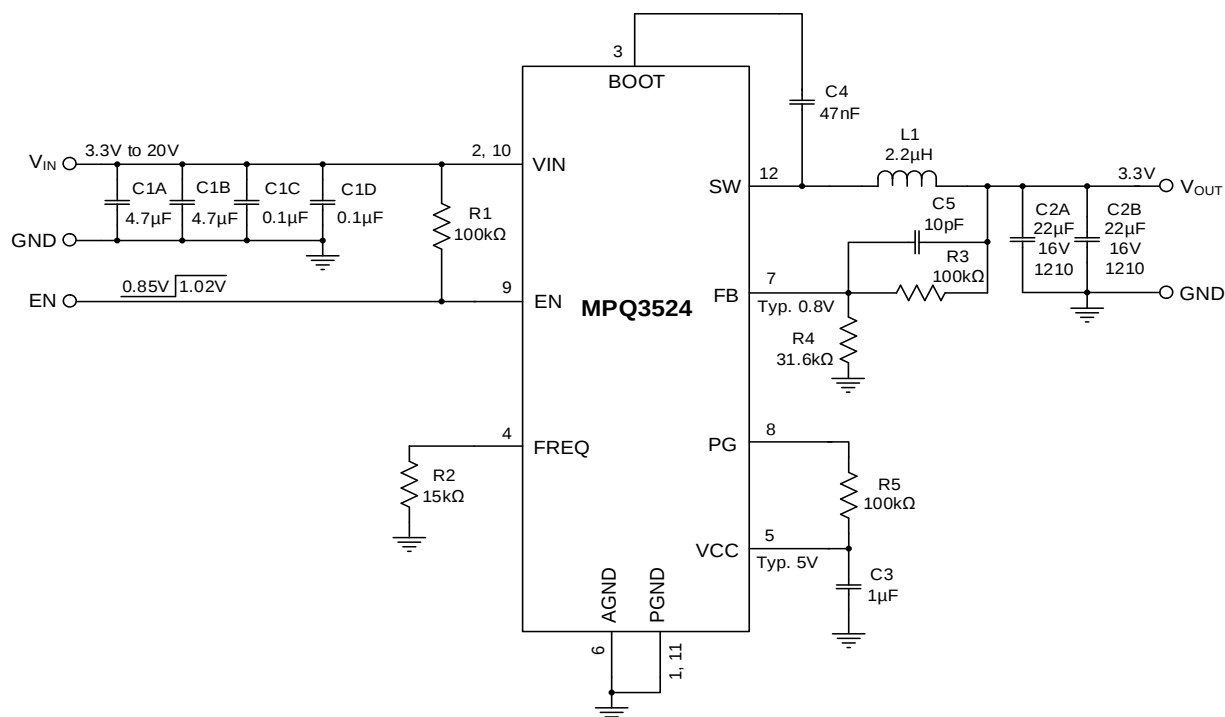


Figure 13: Typical Application Circuit ($V_{OUT} = 3.3V$, $f_{SW} = 2.2MHz$, 1.5A/2A/3A/4A Version)

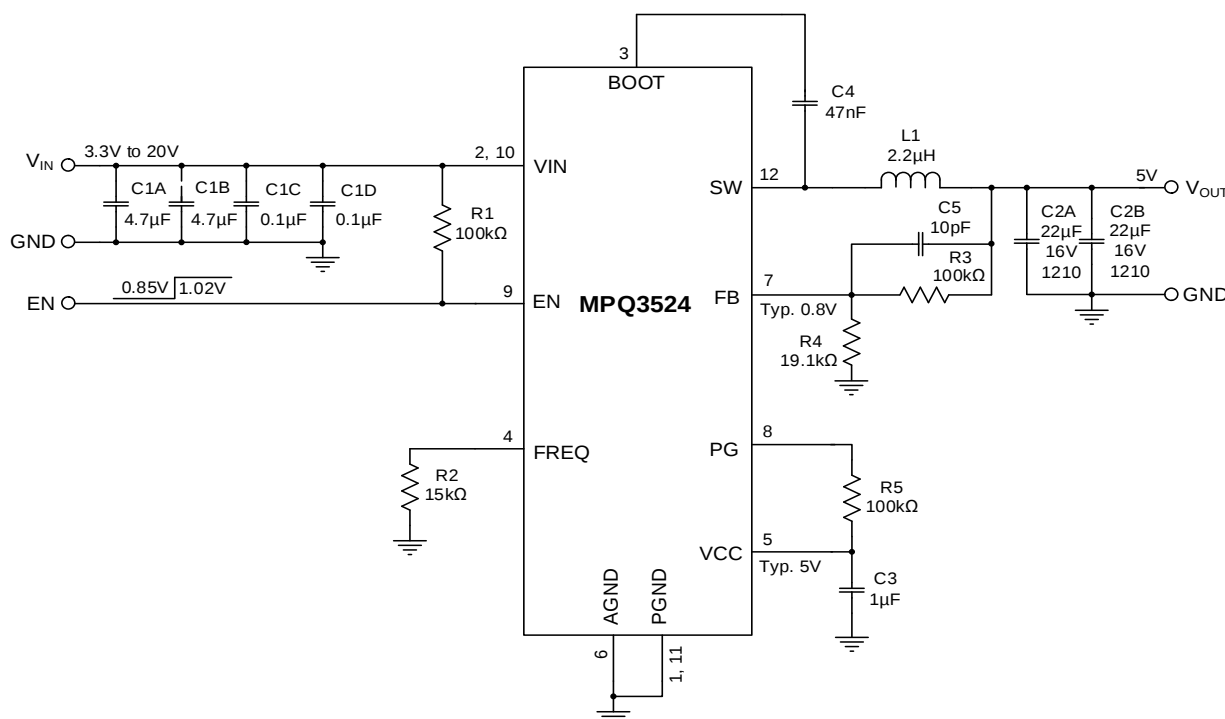


Figure 14: Typical Application Circuit ($V_{OUT} = 5V$, $f_{SW} = 2.2MHz$, 1.5A/2A/3A/4A Version)

TYPICAL APPLICATION CIRCUITS (continued)

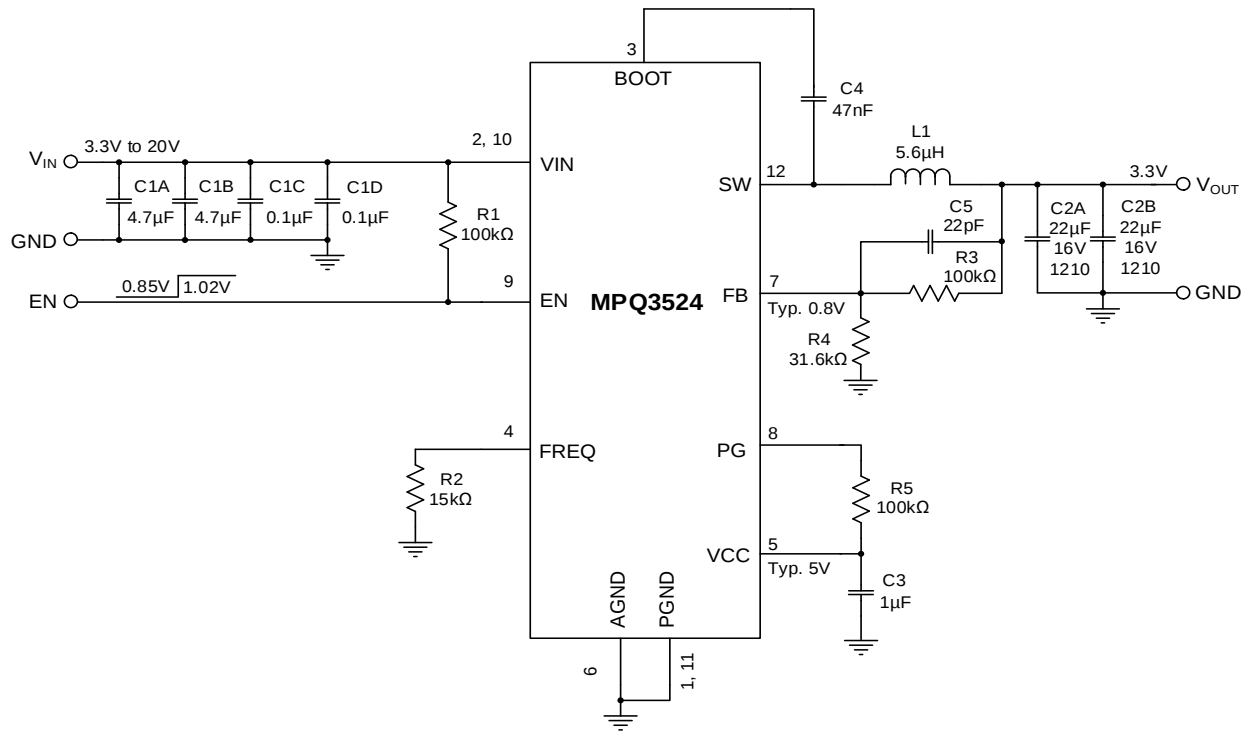


Figure 15: Typical Application Circuit ($V_{OUT} = 3.3V$, $f_{SW} = 2.2MHz$, 1A Version)

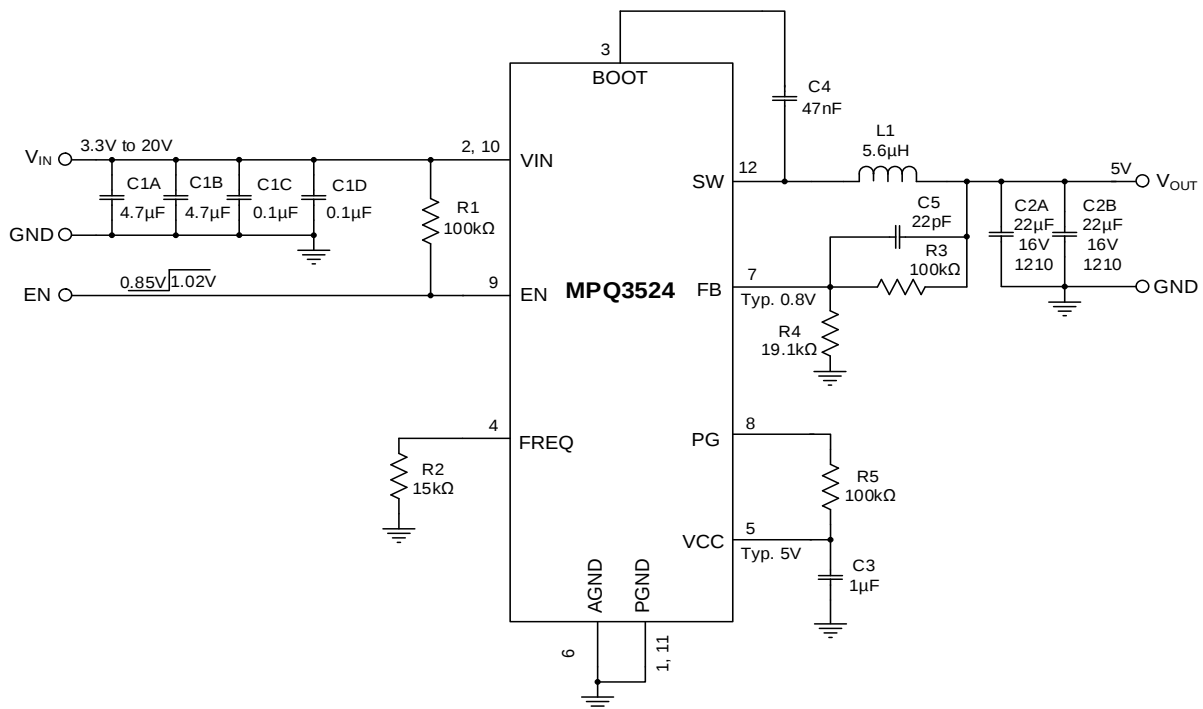


Figure 16: Typical Application Circuit ($V_{OUT} = 5V$, $f_{SW} = 2.2MHz$, 1A Version)

TYPICAL APPLICATION CIRCUITS (continued)

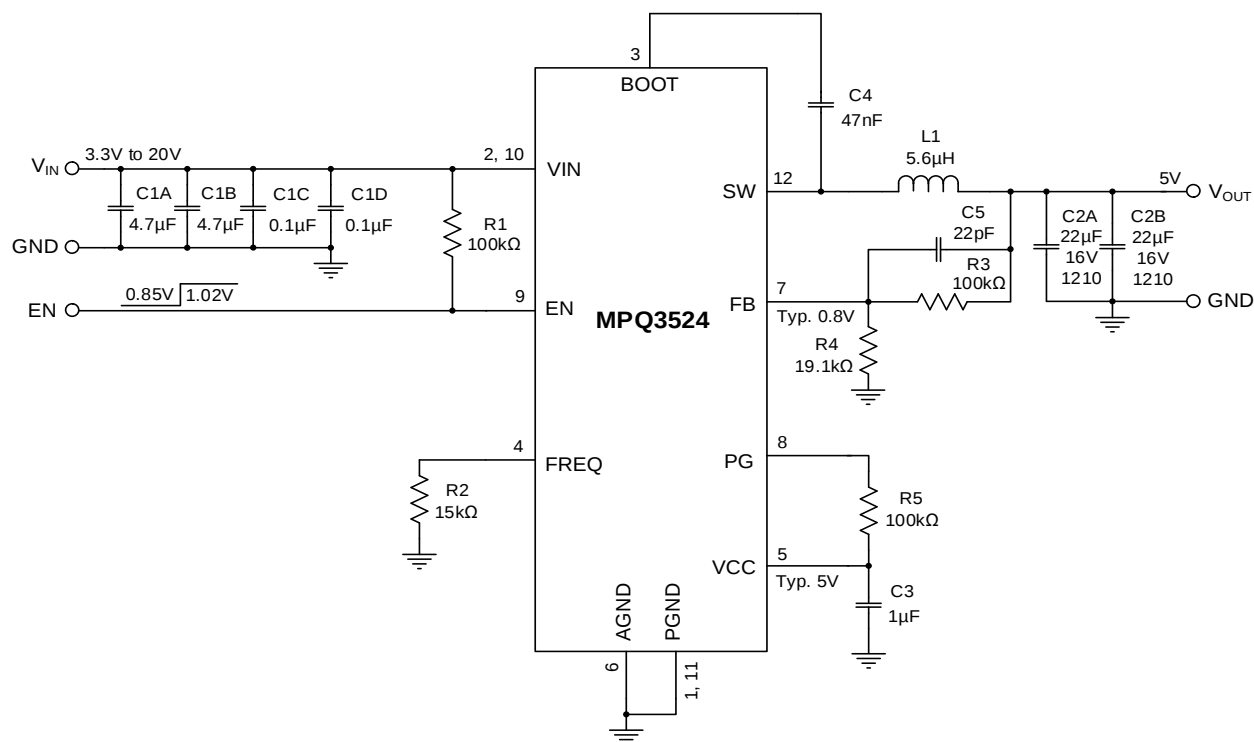


Figure 17: Typical Application Circuit ($V_{OUT} = 5V$, $f_{SW} = 2.2MHz$, FCCM, 0.5A Version)

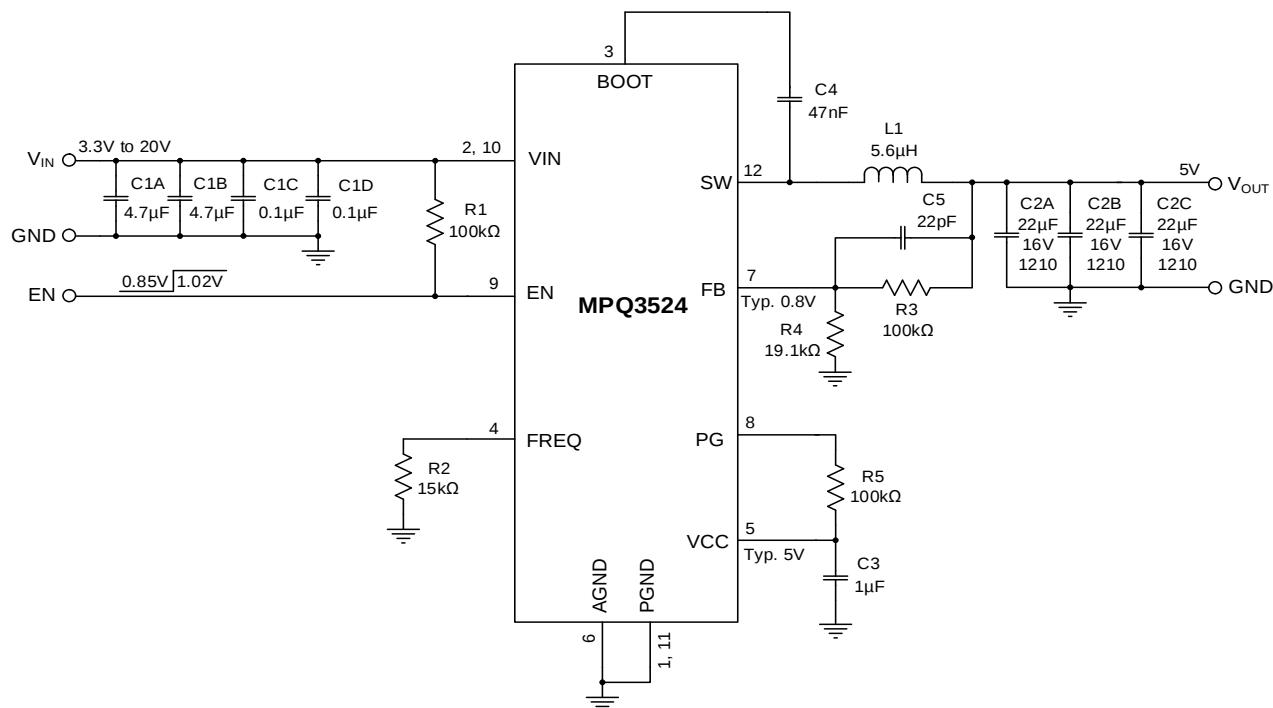


Figure 18: Typical Application Circuit ($V_{OUT} = 5V$, $R_{FREQ} = 15k\Omega$, AAM Mode, 0.5A Version)

TYPICAL APPLICATION CIRCUITS (continued)

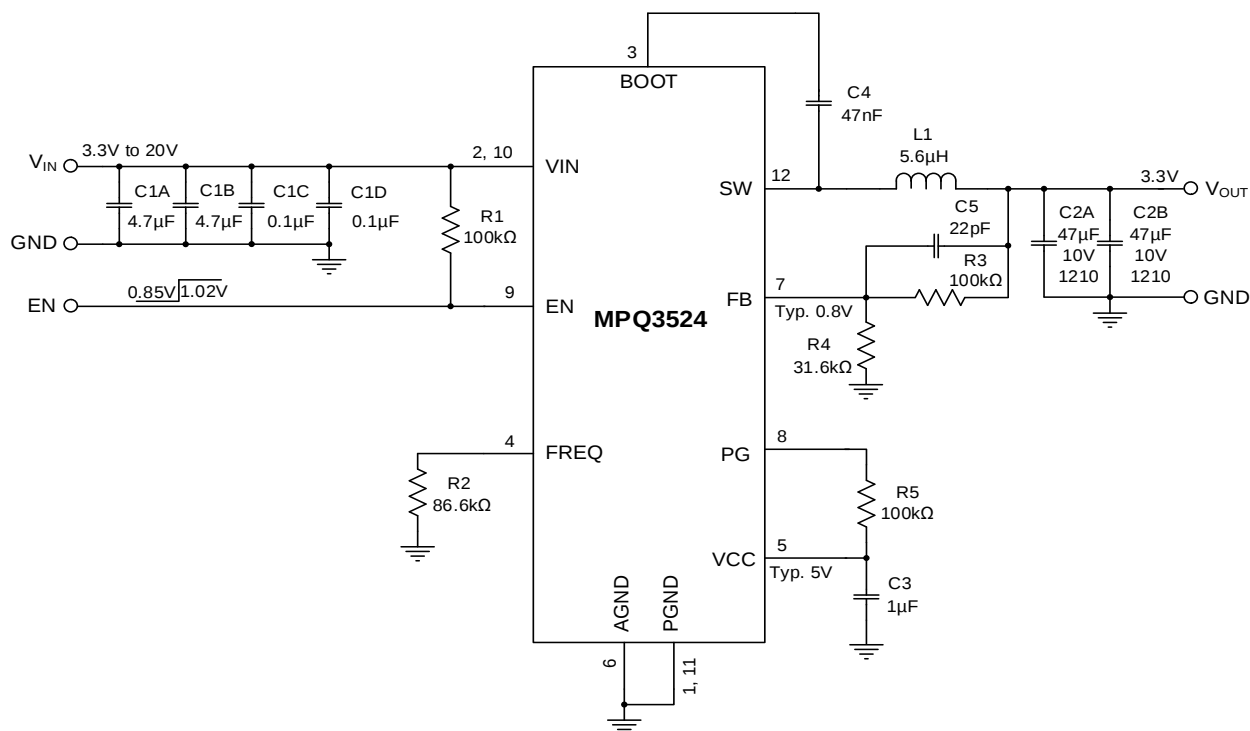


Figure 19: Typical Application Circuit ($V_{OUT} = 3.3V$, $f_{SW} = 415kHz$, $I_{OUT} = 3A/4A$)

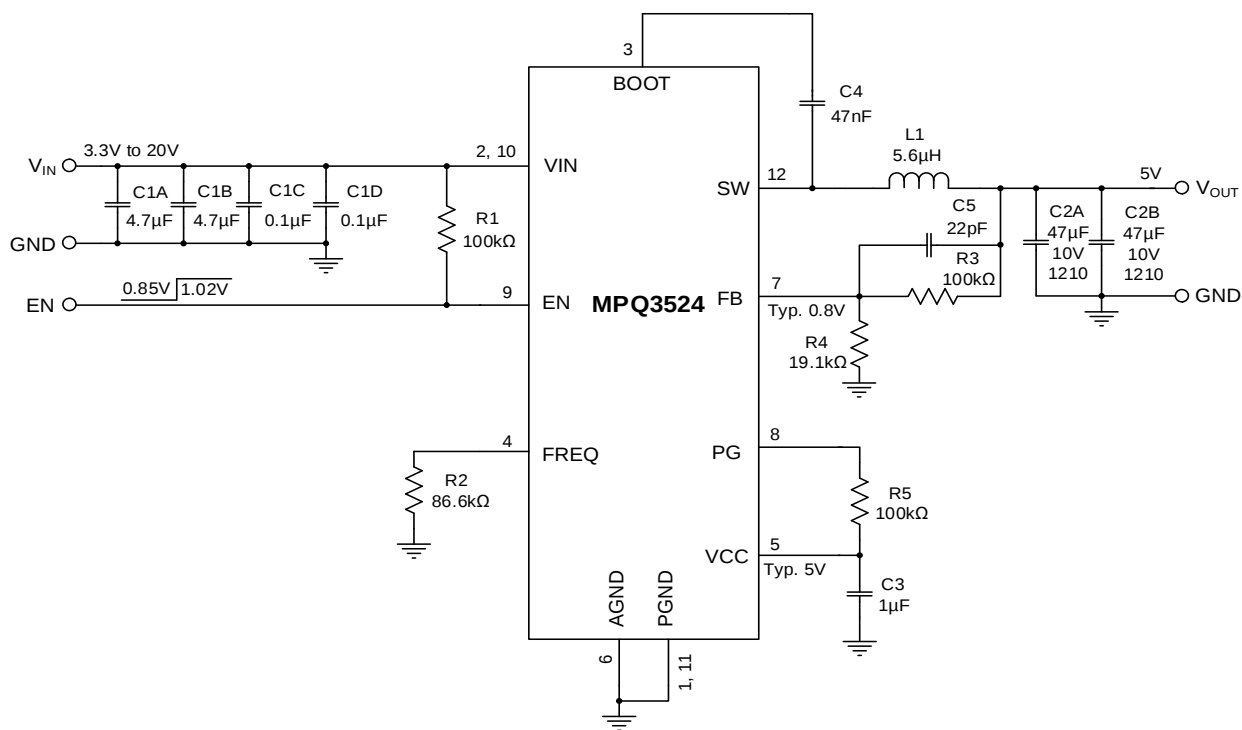


Figure 20: Typical Application Circuit ($V_{OUT} = 5V$, $f_{SW} = 415kHz$, $I_{OUT} = 3A/4A$)

TYPICAL APPLICATION CIRCUITS (continued)

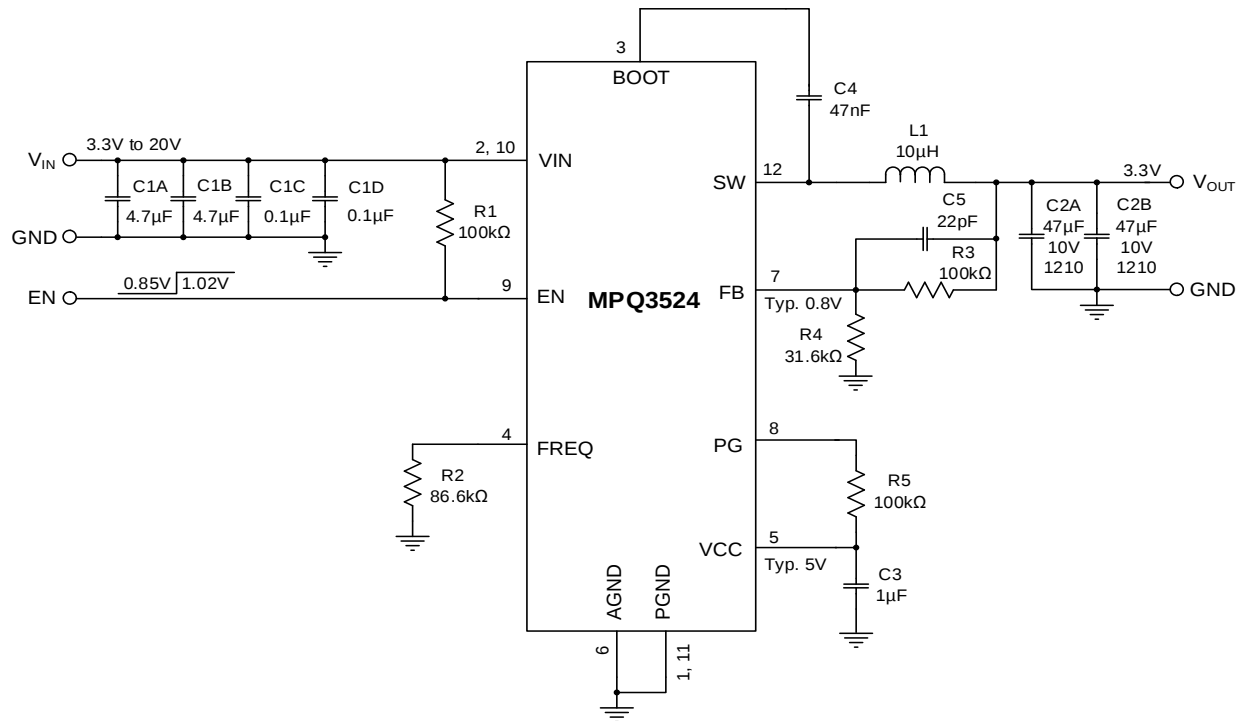


Figure 21: Typical Application Circuit ($V_{OUT} = 3.3V$, $f_{SW} = 415kHz$, $I_{OUT} = 2A/1.5A$)

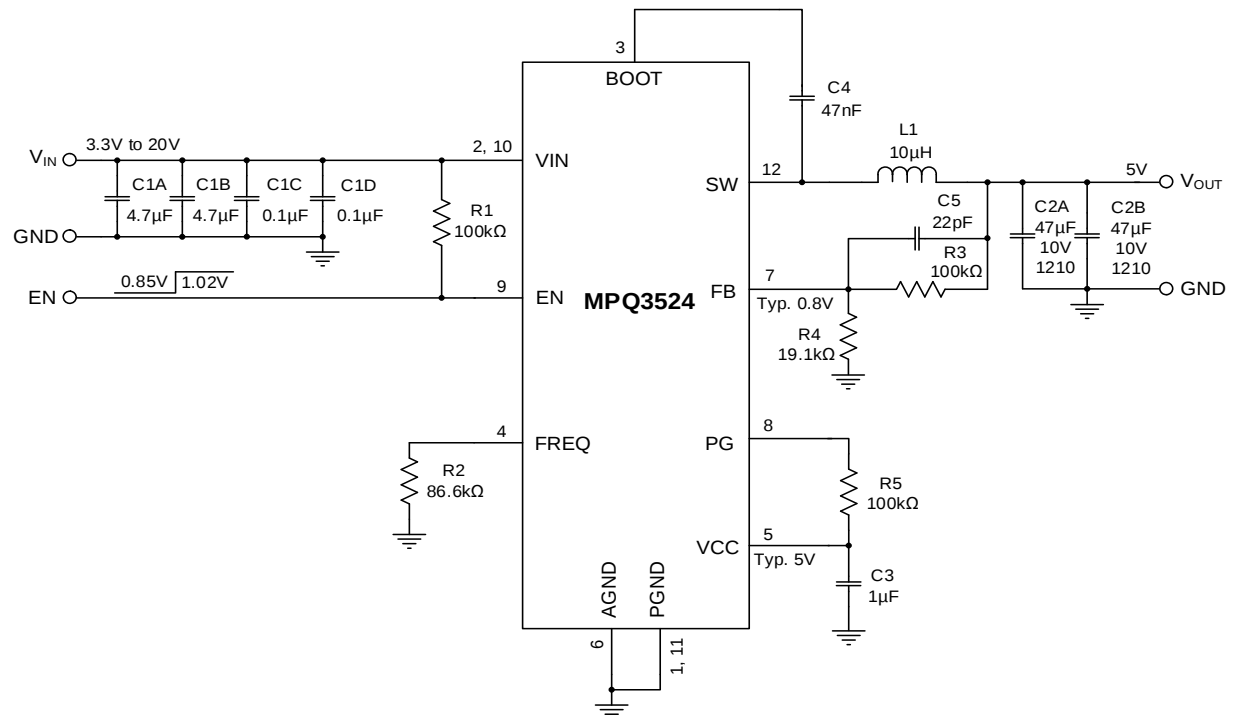


Figure 22: Typical Application Circuit ($V_{OUT} = 5V$, $f_{SW} = 415kHz$, $I_{OUT} = 2A/1.5A$)

TYPICAL APPLICATION CIRCUITS (continued)

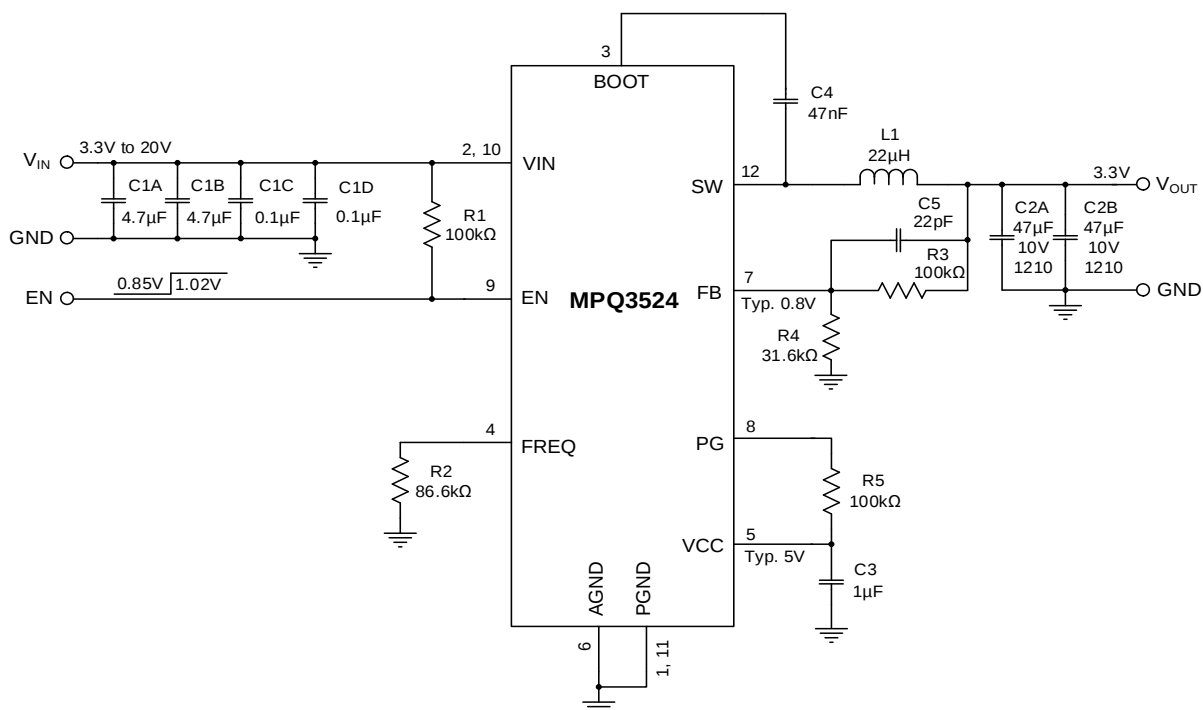


Figure 23: Typical Application Circuit ($V_{OUT} = 3.3V$, $f_{SW} = 415kHz$, 0.5A/1A Version)

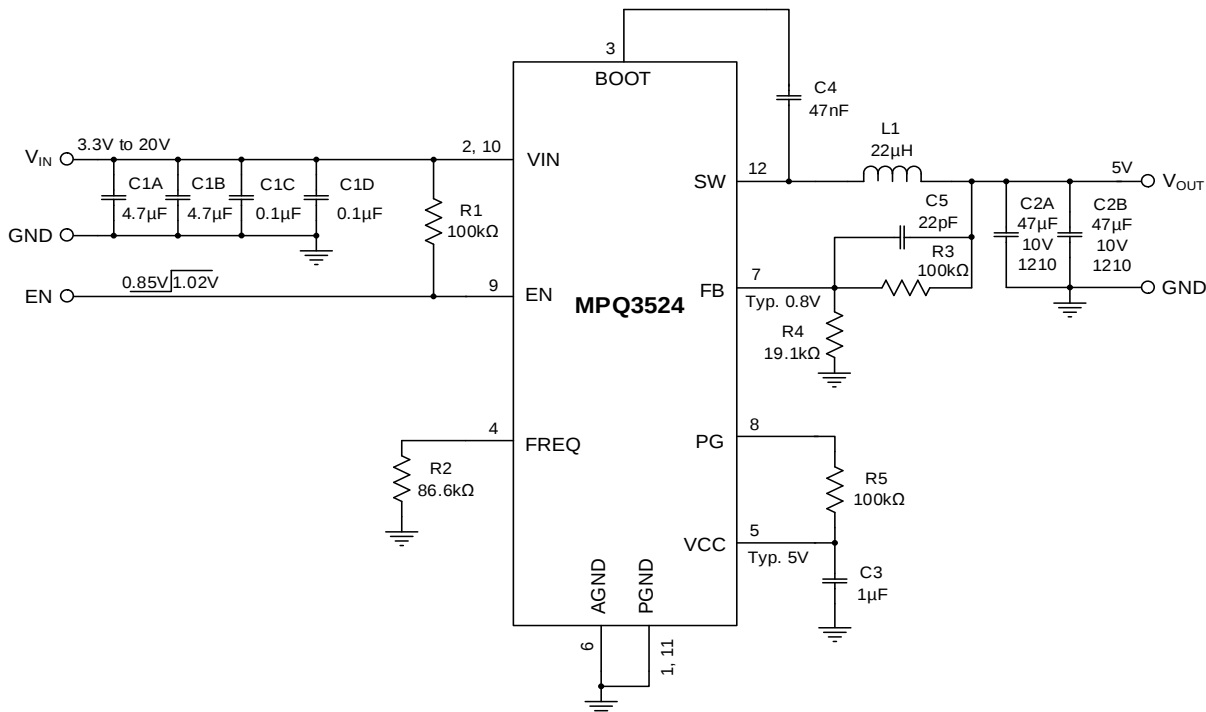


Figure 24: Typical Application Circuit ($V_{OUT} = 5V$, $f_{SW} = 415kHz$, 0.5A/1A Version)

TYPICAL APPLICATION CIRCUITS (continued)

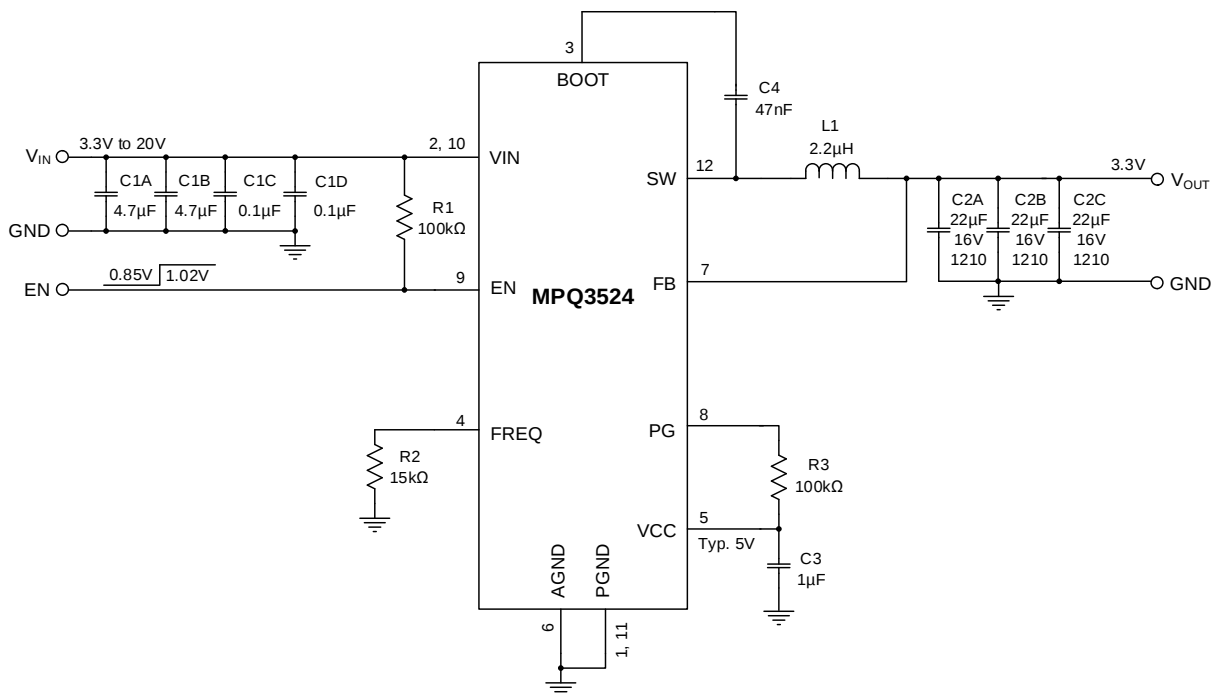


Figure 25: Typical Application Circuit (3.3V Fixed-Output, $f_{SW} = 2.2\text{MHz}$, 1.5A/2A/3A/4A Version)

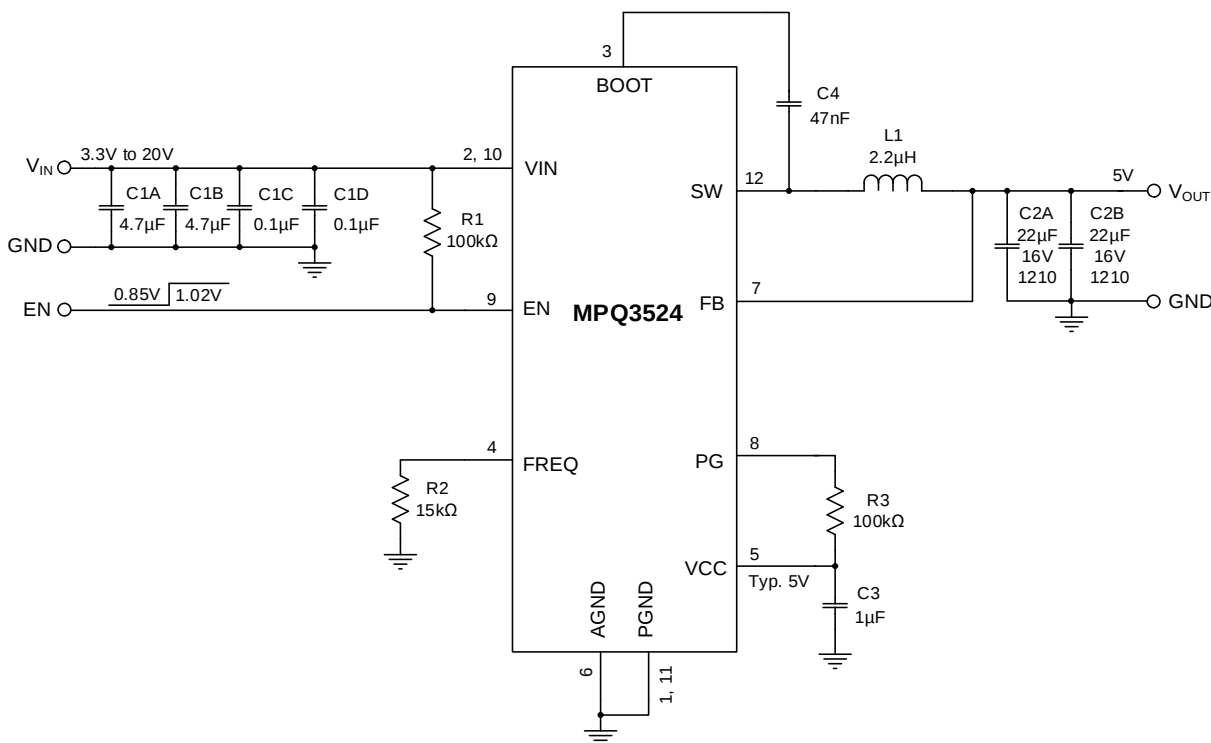


Figure 26: Typical Application Circuit (5V Fixed-Output, $f_{SW} = 2.2\text{MHz}$, $I_{OUT} = 1.5\text{A}/2\text{A}/3\text{A}/4\text{A}$ Version)

TYPICAL APPLICATION CIRCUITS (continued)

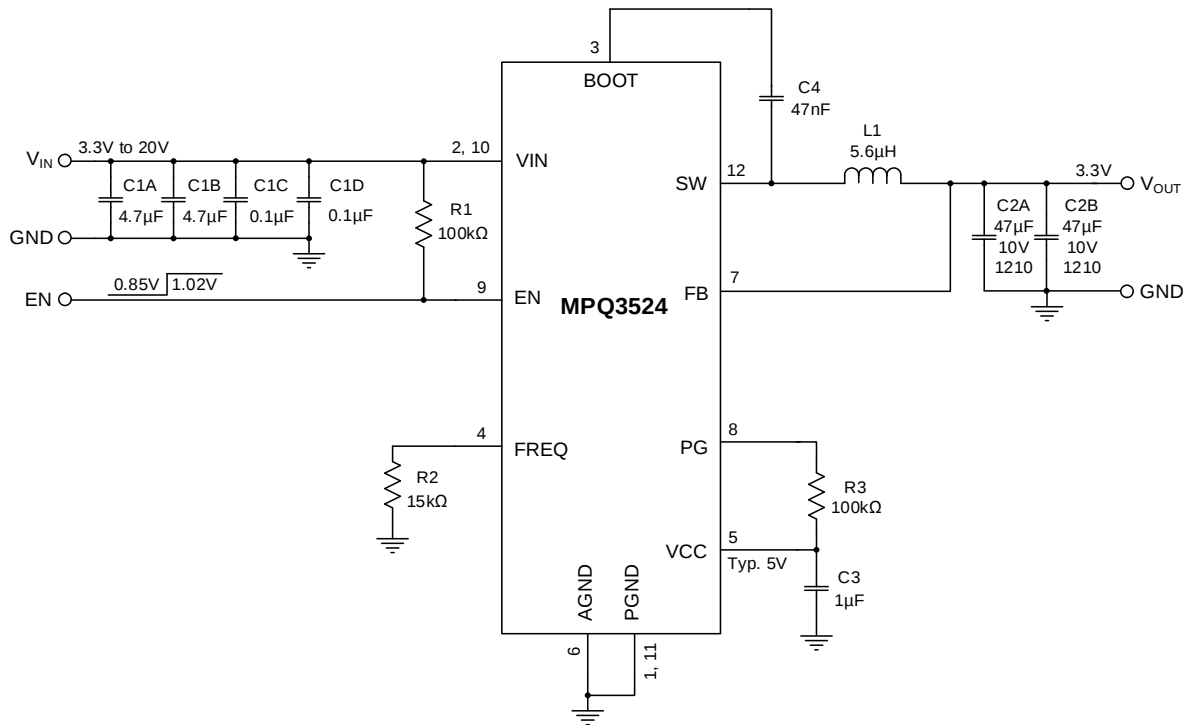


Figure 27: Typical Application Circuit (3.3V Fixed-Output, $f_{SW} = 2.2\text{MHz}$, 0.5A/1A Version)

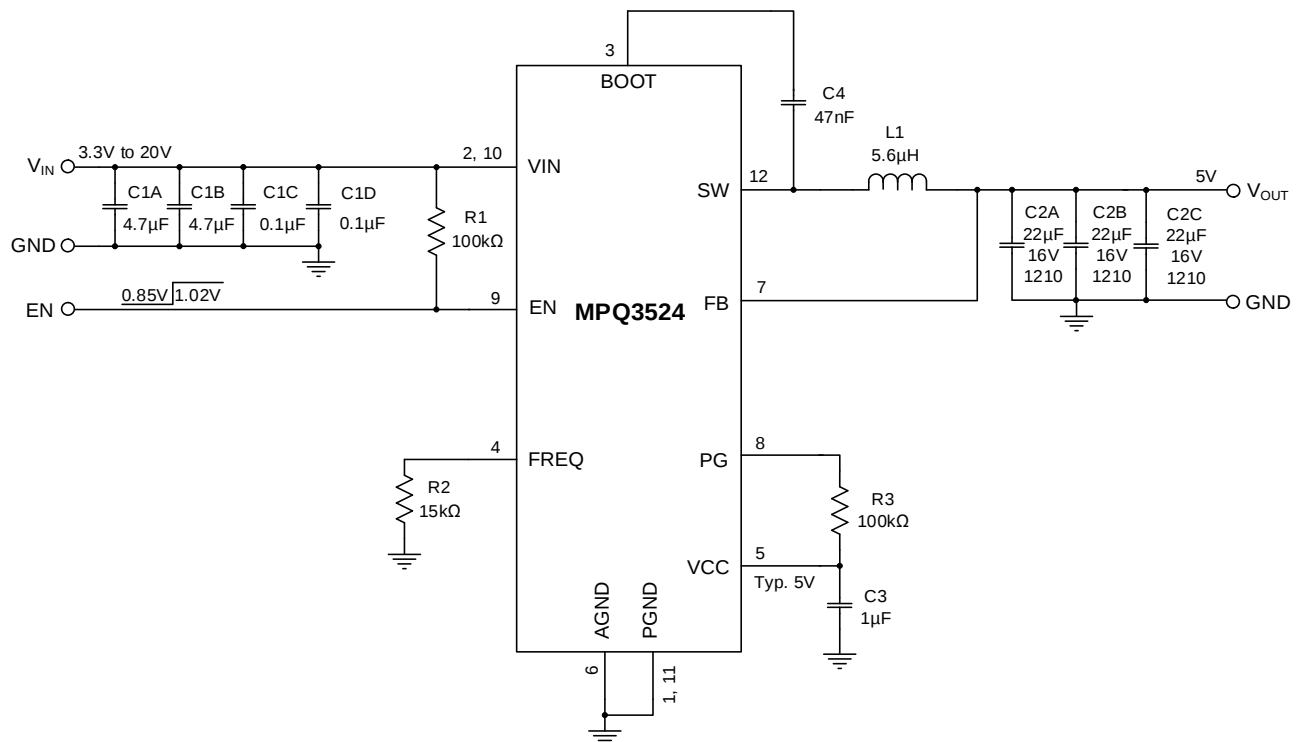


Figure 28: Typical Application Circuit (5V Fixed-Output, $f_{SW} = 2.2\text{MHz}$, 0.5A/1A Version)

TYPICAL APPLICATION CIRCUITS (continued)

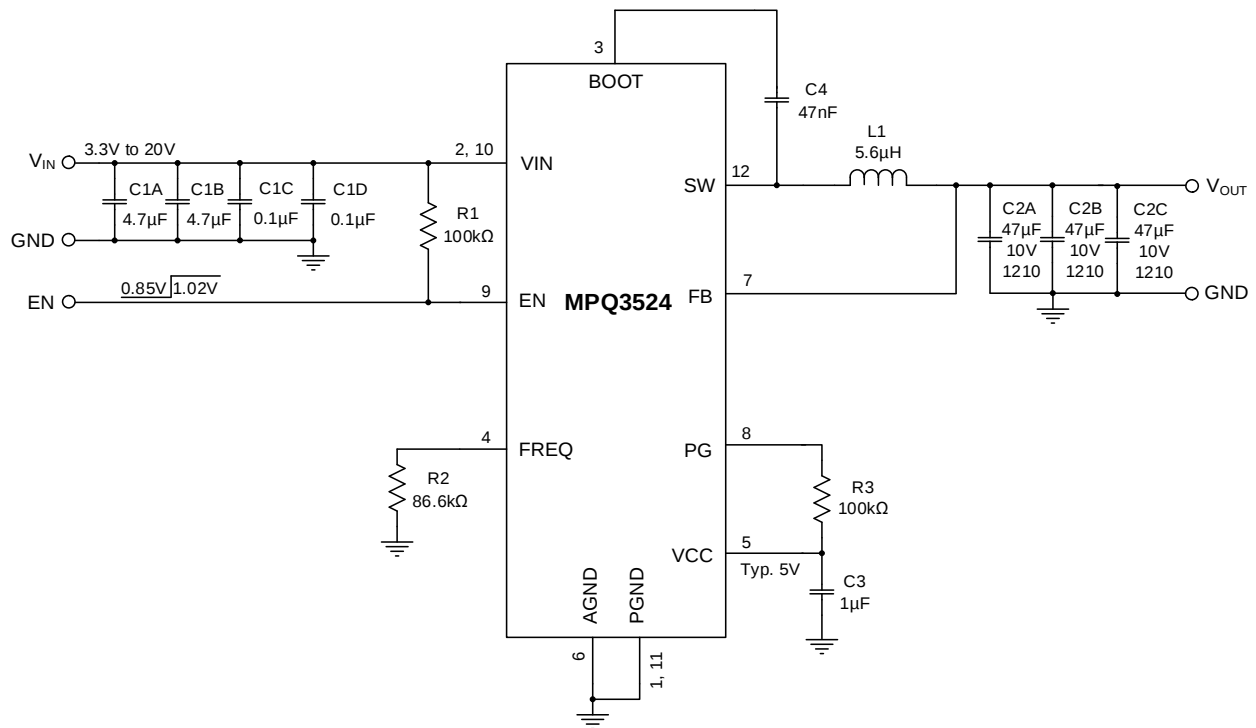


Figure 29: Typical Application Circuit (3.3V Fixed-Output, $f_{sw} = 415\text{kHz}$, 3A/4A Version)

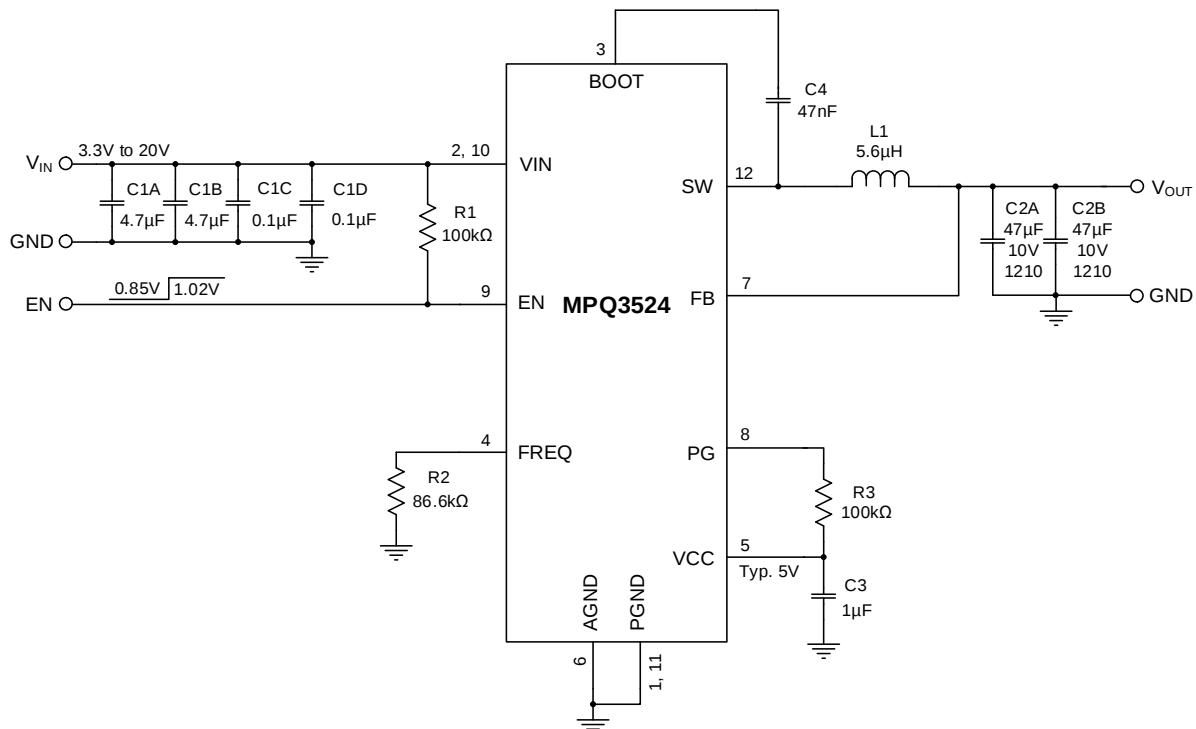


Figure 30: Typical Application Circuit (5V Fixed-Output, $f_{sw} = 415\text{kHz}$, 3A/4A Version)

TYPICAL APPLICATION CIRCUITS (continued)

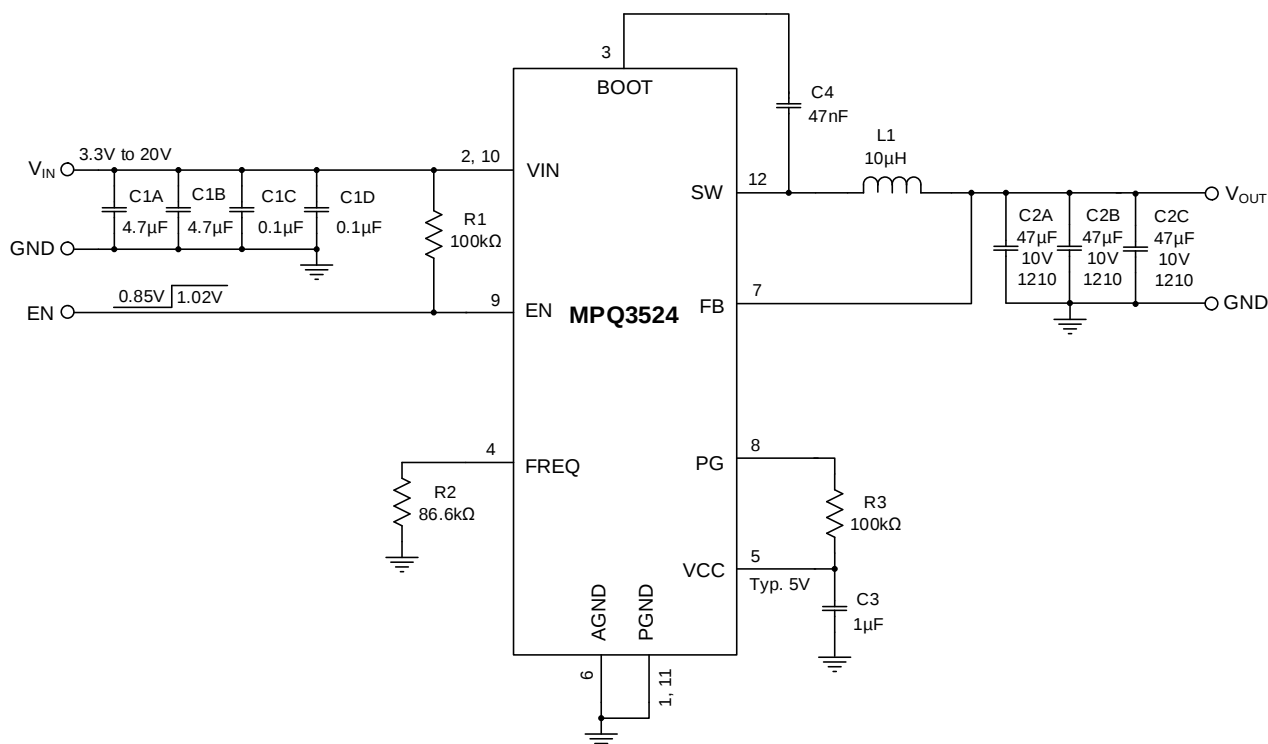


Figure 31: Typical Application Circuit (3.3V Fixed-Output, $f_{SW} = 415\text{kHz}$, 2A/1.5A Version)

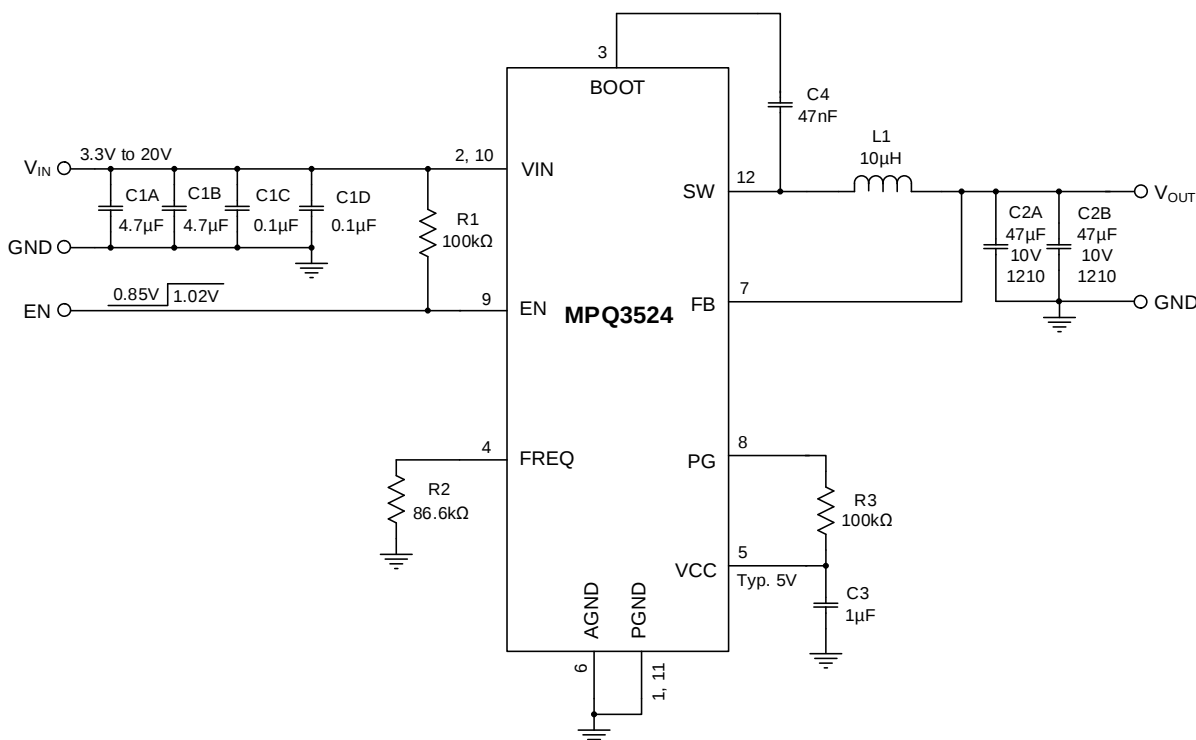


Figure 32: Typical Application Circuit (5V Fixed-Output, $f_{SW} = 415\text{kHz}$, 2A/1.5A Version)

TYPICAL APPLICATION CIRCUITS (continued)

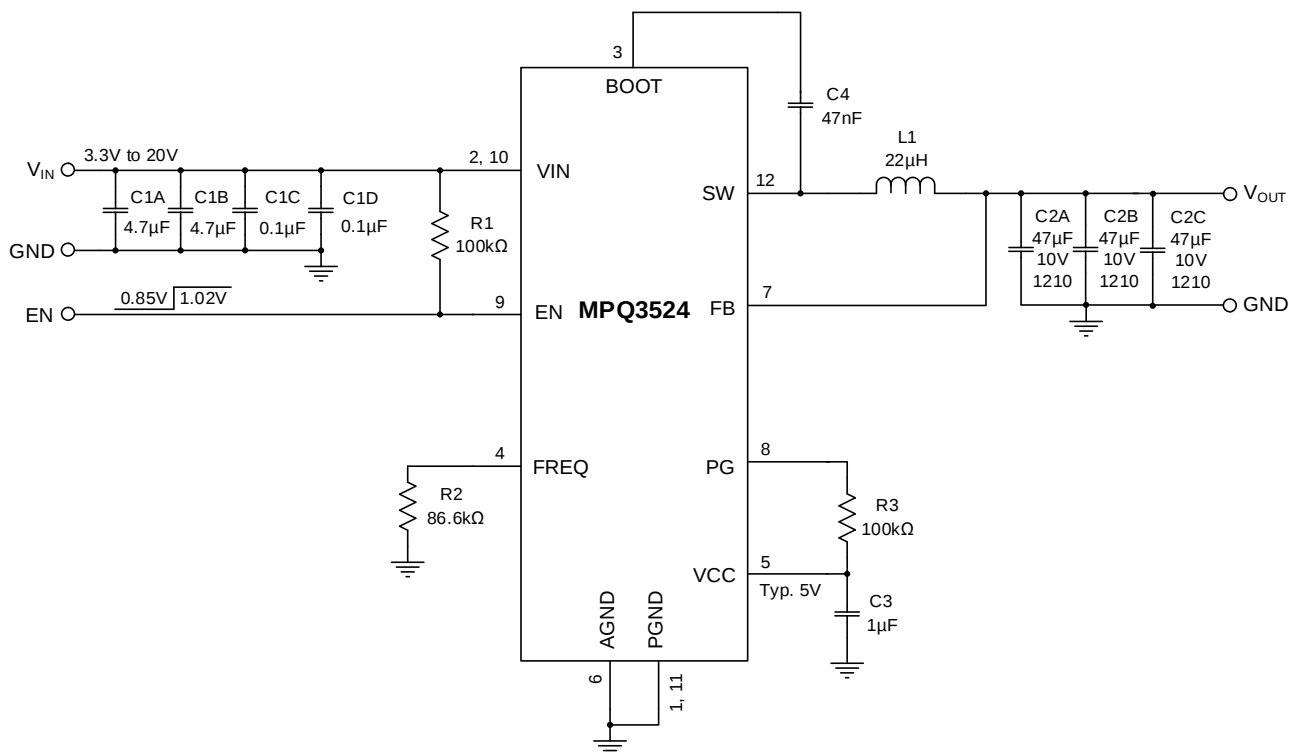


Figure 33: Typical Application Circuit (3.3V Fixed-Output, $f_{sw} = 415\text{kHz}$, 0.5A/1A Version)

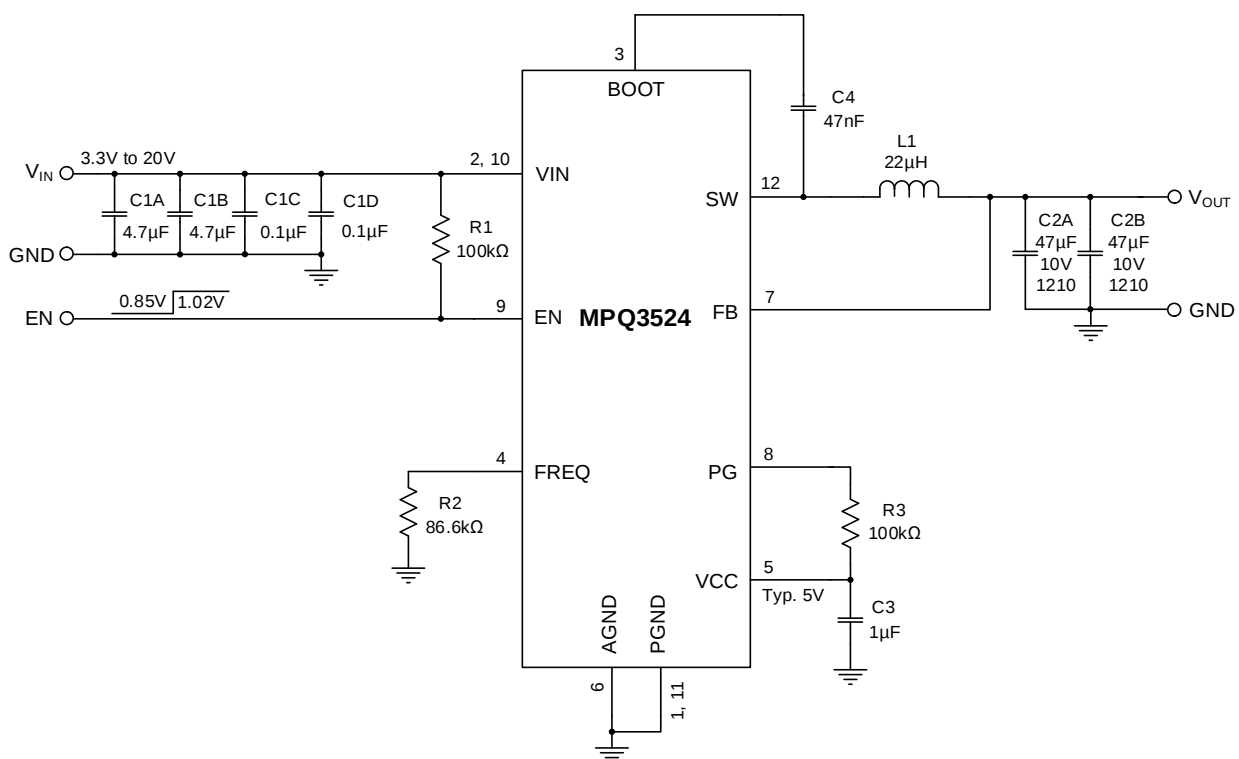


Figure 34: Typical Application Circuit (5V Fixed-Output, $f_{sw} = 415\text{kHz}$, 0.5A/1A Version)

TYPICAL APPLICATION CIRCUITS *(continued)*

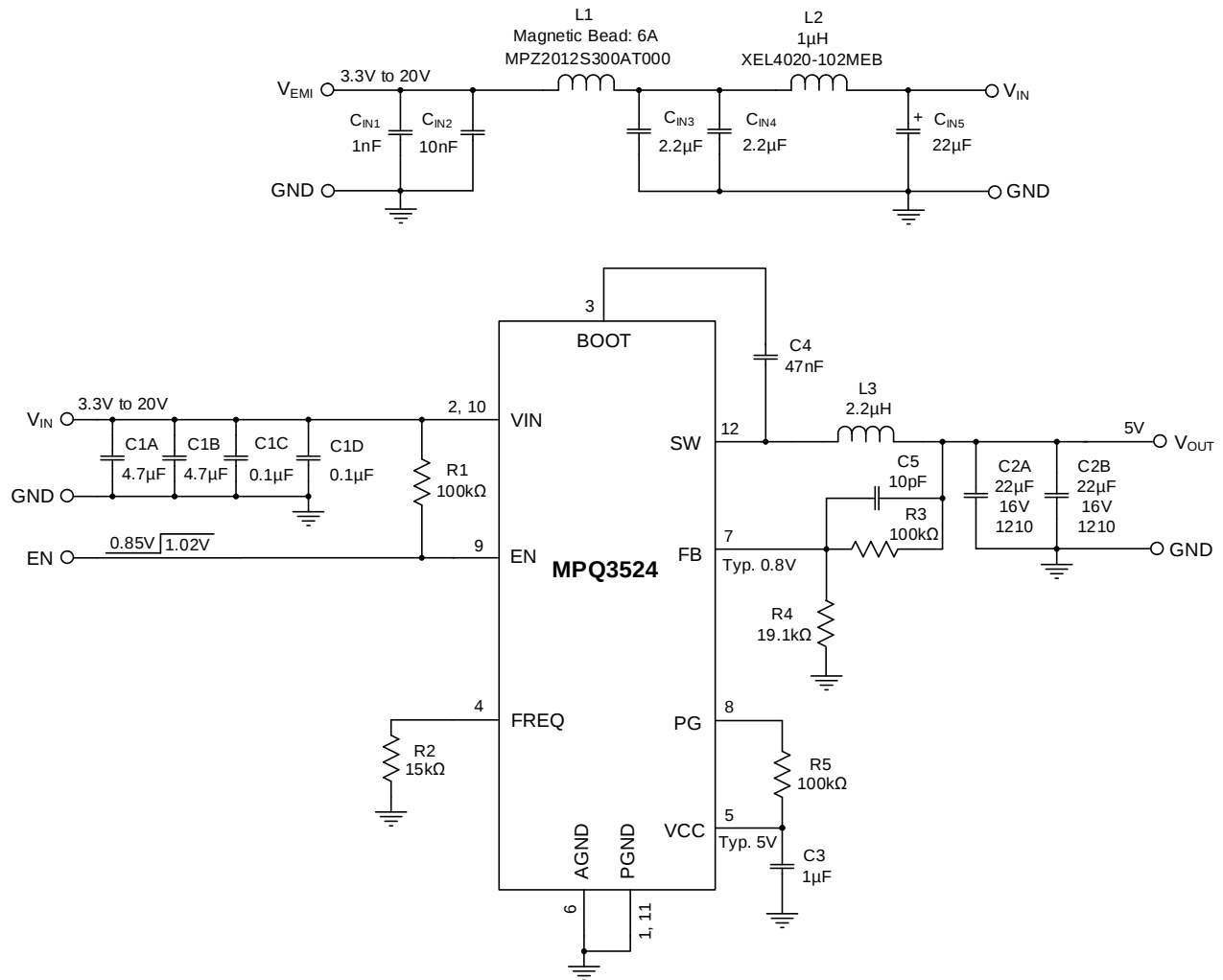


Figure 35: Typical Application Circuit ($V_{OUT} = 5V$, $f_{SW} = 2.2MHz$ with EMI Filters, 4A Version)

TYPICAL APPLICATION CIRCUITS *(continued)*

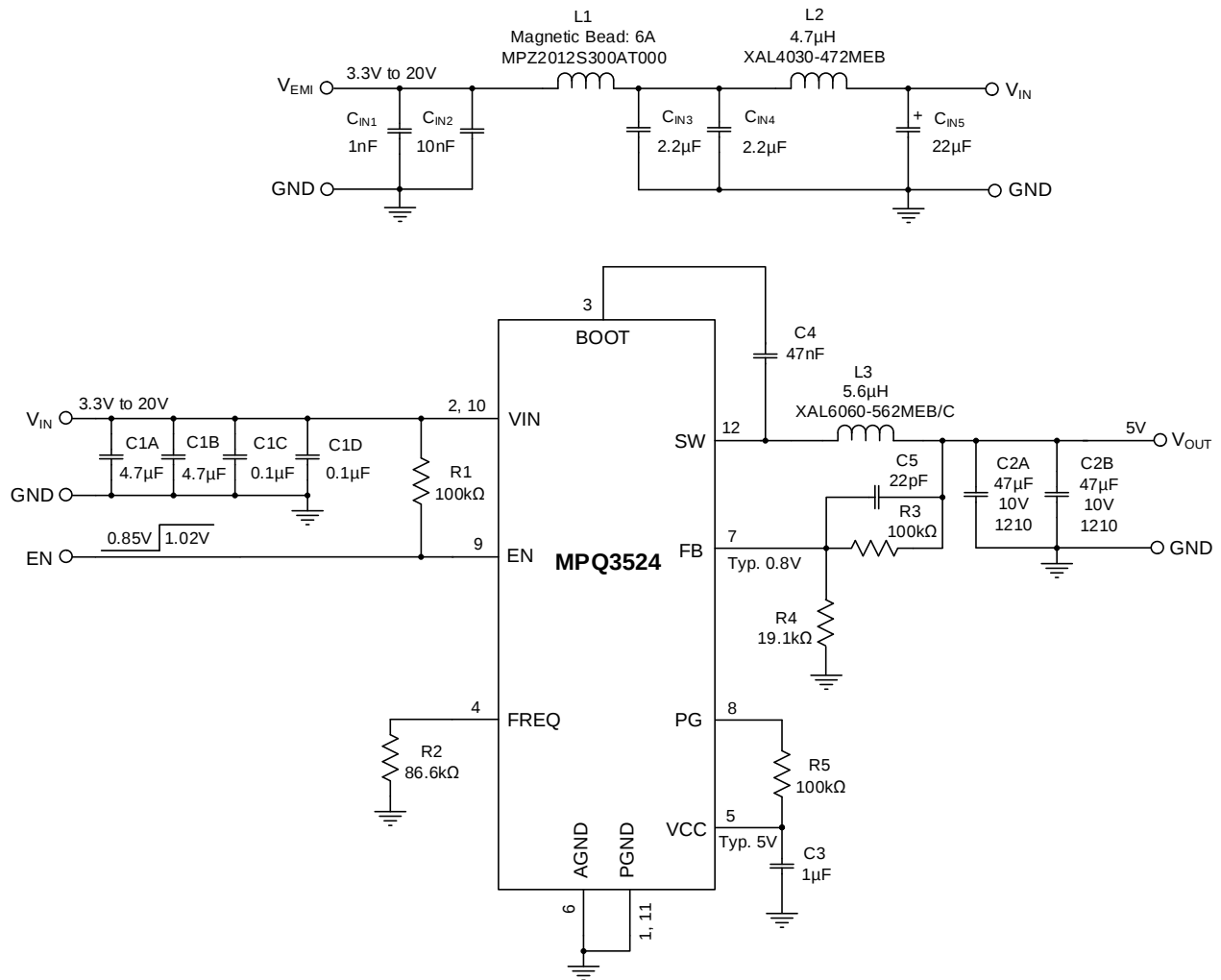
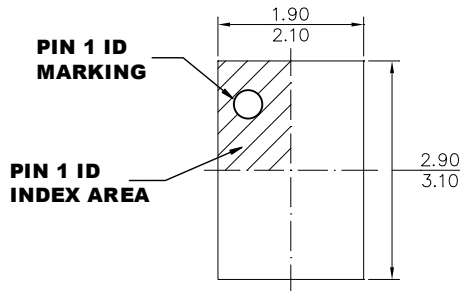


Figure 36: Typical Application Circuit ($V_{OUT} = 5V$, $f_{SW} = 415kHz$ with EMI Filters, 4A Version)

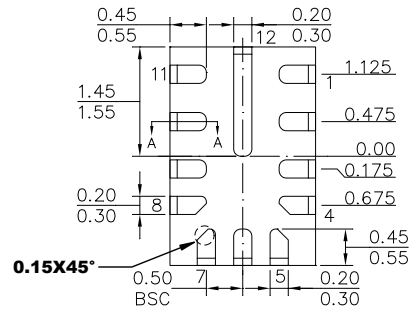
PACKAGE INFORMATION

QFN-12 (2mmx3mm)

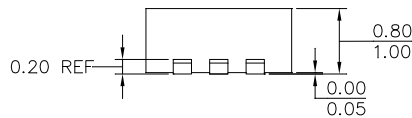
Wettable Flanks



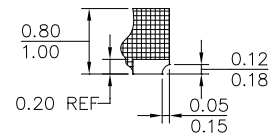
TOP VIEW



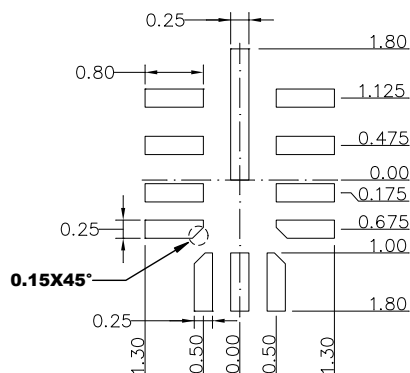
BOTTOM VIEW



SIDE VIEW



SECTION A-A

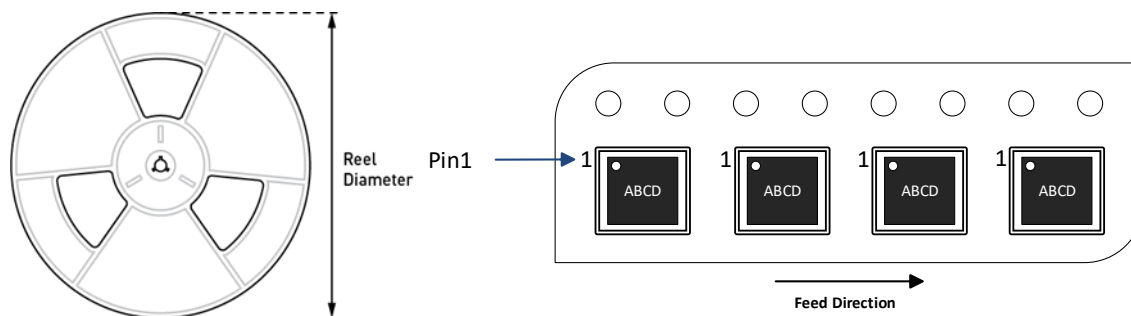


RECOMMENDED LAND PATTERN

NOTE:

- 1) THE LEAD SIDE IS WETTABLE.
- 2) ALL DIMENSIONS ARE IN MILLIMETERS.
- 3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
- 4) JEDEC REFERENCE IS MO-220.
- 5) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube ⁽¹³⁾	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ3524GDE-xxxx-AEC1-Z	QFN-12 (2mmx3mm)	5000	N/A	N/A	13in	12mm	8mm

Note:

13) N/A indicates “not available” in tubes. For 500-piece tape & reel prototype quantities, contact the factory. (The order code for a 500-piece partial reel is “-P”; the tape & reel dimensions remain the same as the full reel.)



REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	12/2/2024	Initial Release	-

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