MPQ3369-AEC1

6-Channel, Max 100mA/Ch Boost WLED Driver with 15000:1 Dim Ratio and I^2C

DESCRIPTION

The MPQ3369-AEC1 is a step-up converter with six channel current sources, designed to drive white LED arrays as backlighting in small-to-mid-size LCD panels.

The MPQ3369-AEC1 uses peak current mode as its PWM control architecture to regulate the boost converter. Six channel current sources are applied into the LED cathode to adjust the LED brightness. It regulates the current in each LED string to the value set via an external current-setting resistor, with 2.5% current regulation accuracy between strings.

The MPQ3369-AEC1 employs a low on-resistor MOSFET and a low headroom voltage, designed for higher efficiency. It has a standard I^2C digital interface for ease of use. The switching frequency can be programmed by a resistor, I^2C interface, or external clock.

The device provides analog, PWM, and mix dimming mode with a PWM input. The dimming mode can be selected with the I^2C interface or the MIX/AD pin. It also has a phase shift function to eliminate noise during PWM dimming.

Robust protections are included to guarantee safe operation of the device. Protection modes include over-current protection (OCP), over-voltage protection (OVP), over-temperature protection (OTP), LED short, and open protection. There is also an option that decreases the LED current automatically at higher temperatures.

The MPQ3369-AEC1 is available in QFN-24 (4mmx4mm) and TSSOP28-EP packages.

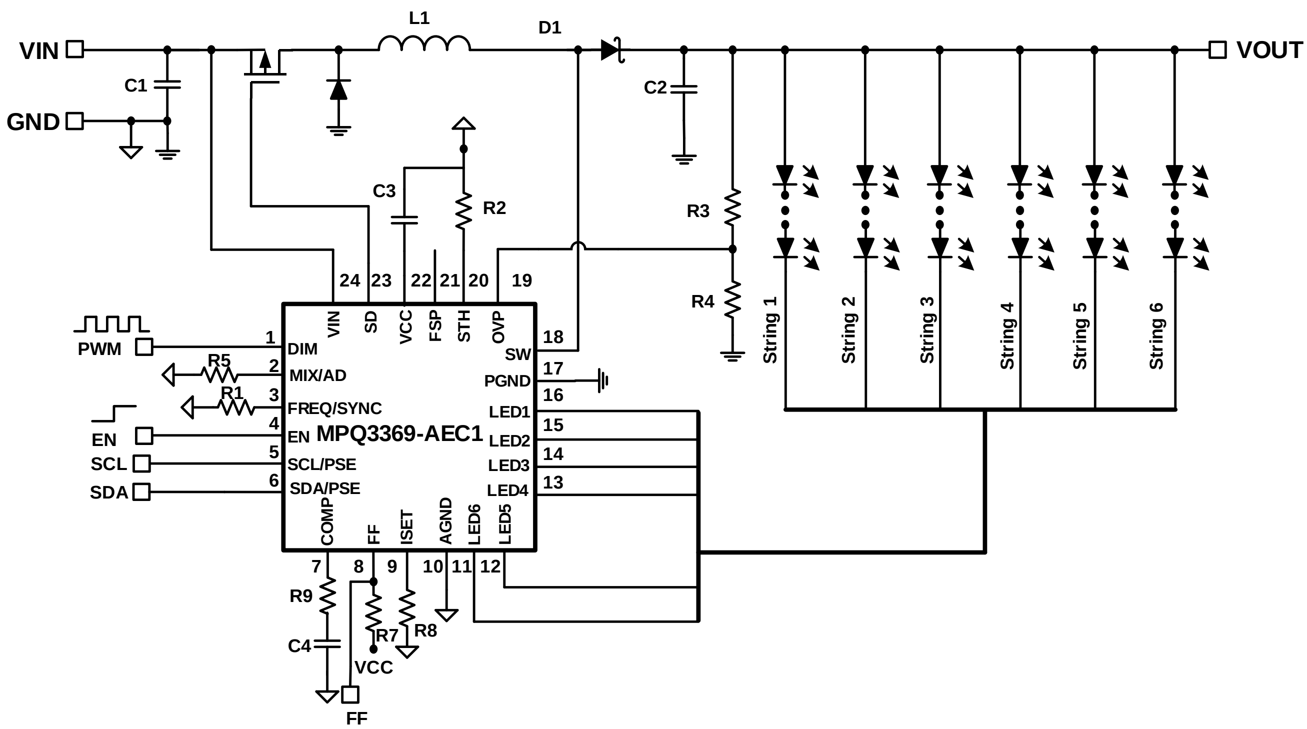
FEATURES

- 3.5V to 36V Input Voltage Range
- 6 Channels with Max 100mA per Channel
- Internal 100mΩ, 50V MOSFET
- Programmable Up to 2.2MHz f_{SW}
- External Sync SW Function
- Multi-Dimming Operation Mode through PWM Input, Including:
    - Direct PWM Dimming
    - Analog Dimming
    - Mix Dimming with 25%/12.5% Transfer Point
- 15000:1 Dim Ratio in PWM Dim at $f_{PWM} \leq$ 200Hz
- 200:1 Dim Ratio at Analog Dim through PWM Dim Signal Input
- Excellent EMI Performance, Frequency Spread Spectrum
- I^2C Interface
- Phase Shift Function for PWM Dimming
- 2.5% Current Matching
- Cycle-by-Cycle Current Limit
- Disconnect VOUT from VIN
- Optional LED Current Auto-Decrement at High Temperature
- LED Short/Open, OTP, OCP, Inductor Short Protection
- Programmable LED Short Threshold
- Programmable OVP Threshold
- Fault Indicator Signal Output
- Available in QFN-24 (4mmx4mm) and TSSOP28-EP Packages
- AEC-Q100 Qualified

APPLICATIONS

- Tablet/Notebook
- Automotive Display

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking
MPQ3369GR-AEC1*	QFN-24 (4mmx4mm)	*See Below*
MPQ3369GF-AEC1**	TSSOP28-EP	*See Below*

* For Tape & Reel, add suffix –Z (e.g. MPQ3369GR–AEC1-Z).
** For Tape & Reel, add suffix –Z (e.g. MPQ3369GF–AEC1-Z).

TOP MARKING (MPQ3369GR-AEC1)

MPSYWW
MP3369
LLLLLL

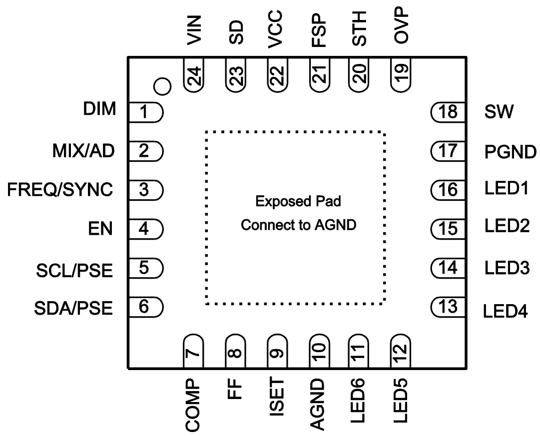
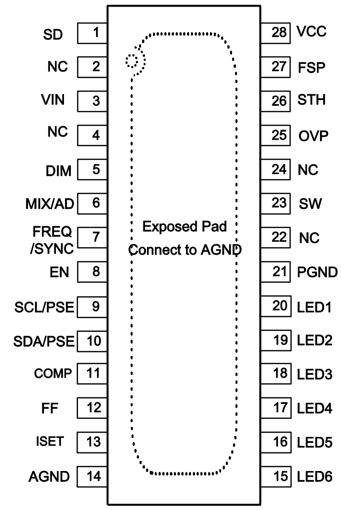
MPS: MPS prefix
Y: Year code
WW: Week code
MP3369: Part number
LLLLLL: Lot number

TOP MARKING (MPQ3369GF-AEC1)

MPSYYWW
MP3369
LLLLLLLLL

MPS: MPS prefix
YY: Year code
WW: Week code
MP3369: Part number
LLLLLLLLL: Lot number

PACKAGE REFERENCE

TOP VIEW	TOP VIEW
	
QFN-24 (4mmx4mm)	TSSOP28-EP

PIN FUNCTIONS

QFN-24 Pin #	TSSOP28-EP Pin #	Name	Description
1	5	DIM	**PWM signal input pin.** Apply a PWM signal on DIM for brightness control. Pulled low internally. A 100Hz to 20kHz PWM signal is recommended.
2	6	MIX/AD	**Dimming mode set pin.** MIX/AD is a current-source output (18μA). Connect a resistor to program its voltage. When MIX/AD is low-level (<0.3V), mix dimming is adopted. When MIX/AD is mid-level (0.5V to 0.8V), PWM dimming is adopted. When MIX/AD is high-level (1.0V to 1.3V), analog dimming is adopted. When MIX/AD is floated, the dimming mode is set by the internal MODE register.
3	7	FREQ/SYNC	**Switching frequency setting and SYNC pin.** The switching frequency is decided by the voltage and current on this pin. Connect a resistor between FREQ/SYNC and GND to set the converter's switching frequency, or connect an external clock to the sync boost switching frequency. Leave FREQ/SYNC floating if the internal switching frequency set register FSW1:0 is used.
4	8	EN	**IC enable pin.** Pull EN high to enable the IC. When EN is pulled low, the IC enters shutdown.
5	9	SCL/PSE	**I^{2}C interface clock input pin.** Tie SDA/PSE together with SCL/PSE and pull up to 0.75V to 1V to enable the phase-shift PWM dimming function. If it isn't used, please pull it to GND.
6	10	SDA/PSE	**I^{2}C interface data input pin.** Tie SCL/PSE together with SDA/PSE and pull up to 0.75V to 1V to enable the phase-shift PWM dimming function. If it isn't used, please pull it to GND.
7	11	COMP	**Compensation pin.**
8	12	FF	**Fault flag pin.** Open drain during normal operation, pulled low in any fault mode.
9	13	ISET	**LED current setting.** Tie a current-setting resistor from ISET to GND to program the current in each LED string.
10	14	AGND	**Analog ground.**
11	15	LED6	**LED string 6 current input.** Connect the LED string 6 cathode to this pin.
12	16	LED5	**LED string 5 current input.** Connect the LED string 5 cathode to this pin.
13	17	LED4	**LED string 4 current input.** Connect the LED string 4 cathode to this pin.
14	18	LED3	**LED string 3 current input.** Connect the LED string 3 cathode to this pin.
15	19	LED2	**LED string 2 current input.** Connect the LED string 2 cathode to this pin.
16	20	LED1	**LED string 1 current input.** Connect the LED string 1 cathode to this pin.
17	21	PGND	**Step-up converter power ground.**
18	23	SW	**Drain for the internal low-side MOSFET switch.** Connect the power inductor to SW.
19	25	OVP	**Over-voltage protection pin.** Connect a resistor divider from OVP to GND to program the OVP threshold.
20	26	STH	**Short LED protection threshold set pin.** STH is a current-source output (18μA). Connect a resistor to program its voltage. Float this pin if the internal short LED protection threshold set register TH_S 1:0 is used.
21	27	FSP	**Switching frequency spread spectrum pin.** FSP is a current-source output (18μA). Connect a resistor to program its voltage. Float this pin to follow the internal register setting.

PIN FUNCTIONS *(continued)*

QFN-24 Pin #	TSSOP28-EP Pin #	Name	Description
22	28	VCC	**5V LDO output pin.** VCC provides power for the internal logic and gate driver. Place a ceramic capacitor as close to this pin as possible to reduce noise.
23	1	SD	**External disconnect PMOS gate drive pin.** Turns off the external PMOS in a fault condition. Float this pin if not used.
24	3	VIN	**Power supply input.** VIN supplies power to the IC.
	2, 4, 22, 24	NC	**No connection.**
Exposed pad	Exposed pad	AGND	**Chip ground.** Connect exposed pad to AGND.

ABSOLUTE MAXIMUM RATINGS (1)

V_{IN} .... -0.3V to +42V
V_{SW}, V_{LED1} to V_{LED6} .... -0.5V to +50V
V_{SW} .... -1.0V for <100ns
V_{SD} .... V_{IN} - 6V to V_{IN}
All other pins .... -0.3V to +6V
LED1-6 ESD ....>7kV
Junction temperature .... 150°C
Lead temperature .... 260°C
Storage temperature range ...... -65°C to +150°C
Continuous power dissipation (T_A = 25°C) (2)
QFN-24 (4mmx4mm) 2.97W
TSSOP28-EP 3.9W

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) .... 3.5V to 36V
Operating junction temp .... -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

QFN-24 (4mmx4mm)…….....…42…….9....°C/W
TSSOP28-EP…...….......………32…….6....°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, V_{EN} = 2V, T_J = -40°C to +125°C, typical value is at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Operating input voltage	V_{IN}		3.5		36	V
Supply current (quiescent)	I_Q	No switching		5		mA
Supply current (shutdown)	I_{ST}	V_{EN} = 0V, V_{IN} = 12V			1	μA
Input UVLO threshold	V_{IN_UVLO}	Rising edge		3.1		V
Input UVLO hysteresis				100		mV
LDO output voltage	V_{CC}	V_{EN} = 2V, 6V < V_{IN} < 36V, 0 < I_{VCC} < 10mA		5		V
EN on threshold	V_{EN_ON}	V_{EN} rising	1.2			V
EN off threshold	V_{EN_OFF}	V_{EN} falling			0.4	V
EN pull-down resistance	R_{EN}			1		MΩ
Step-Up Converter						
Low-side MOSFET on resistance	R_{DS_LS}	V_{IN} = 12V		100		mΩ
SW leakage current	I_{SW_LK}	V_{SW} = 45V			1	μA
Switching frequency	f_{SW}	R_{FREQ} = 10kΩ	1.98	2.2	2.42	MHz
		R_{FREQ} = 40kΩ	495	550	605	kHz
		FSW1:0 = 01, FREQ float	340	400	460	kHz
FREQ voltage	V_{FREQ}		0.57	0.6	0.63	V
FSP pull-up current	I_{FSP}			18		μA
Maximum duty cycle	D_{MAX}	f_{SW} = 1MHz	90			%
Cycle-by-cycle current limit	I_{SW_LIMIT}	T_J = 25°C, duty = 90%	2.6			A
		Duty = 90%	2.3			A
Current limit protection	I_{CL}	To trigger current limit protection		7.5		A
SYNC input low threshold	V_{SYNC_LO}	V_{SYNC} falling			0.4	V
SYNC input high threshold	V_{SYNC_HI}	V_{SYNC} rising	1.2			V
PSE active threshold	V_{PSE}	Phase shift enabled	0.75	0.9	1.0	V
COMP transconductance	G_{COMP}	$\Delta I_{COMP} \le 10\mu A$		100		μA/V
COMP source current limit	I_{COMP_SO}			90		μA
COMP sink current limit	I_{COMP_SI}			30		μA
Current Dimming						
DIM input low threshold	V_{DIM_LO}	V_{DIM} falling			0.4	V
DIM input high threshold	V_{DIM_HI}	V_{DIM} rising	1.2			V
MIX/AD input low threshold	V_{MIX_LO}	Mix dimming threshold			0.3	V
MIX/AD input middle threshold	V_{MIX_MID}	PWM dimming threshold	0.5		0.8	V
MIX/AD input high threshold	V_{MIX_HI}	Analog dimming threshold	1.0		1.3	V

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{EN} = 2V, T_J = -40°C to +125°C, typical value is at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
MIX/AD pull-up current	I_{MIX}	MIX/AD pull-up current		18		µA
Mix dimming transfer point		MIXTP bit = 0		25		%
Transfer point hysteresis				0.5		%
Mix dimming output dimming frequency	f_{MIX}	MIXFR bit = 0		200		Hz
LED Current Regulator						
LEDX regulation voltage	V_{HD}	I_{LED} = 20mA		350		mV
		I_{LED} = 100mA		850	1000	mV
Current matching [5]		I_{LED} = 20mA	-2.5		+2.5	%
		I_{LED} = 100mA	-2.5		+2.5	%
ISET voltage	V_{ISET}			1.2		V
LED current	I_{LED}	R_{ISET} = 24.9kΩ, T_J = 25°C	48.75	50	51.25	mA
		ILED = 1 / 50 * 50mA = 1mA	0.9	1.05	1.2	mA
Phase shift degree		LED1–6 enable		60		°
		LED1–4 enable		90		°
Protection						
Over-voltage protection threshold	V_{OVP}		1.9	2	2.1	V
OVP hysteresis				200		mV
OVP UVLO threshold	V_{OVP_UV}	Step-up converter fails		100		mV
LEDX over-voltage threshold	V_{LEDX_OV}	LEDS bits = 01		5		V
LEDX over-voltage fault timer				7.7		ms
LEDX UVLO threshold	V_{LEDX_UV}			100		mV
Thermal shutdown threshold [6]	T_{ST}	Rising edge		170		°C
		Hysteresis		20		°C
SD pull-down current	I_{SD}			60		µA
SD voltage (respective to V_{IN})	V_{SD-IN}	V_{IN} = 12V, V_{IN} - V_{SD}		6		V
STH pull-up current	I_{STH}	STH pull-up current		18		µA
I2C Interface						
Input logic low	V_{IL}				0.4	V
Input logic high	V_{IH}		1.2			V
Output logic low	V_{OL}	I_{LOAD} = 3mA			0.4	V
SCL clock frequency	f_{SCL}				400	kHz
SCL high time	t_{HIGH}		0.6			µs
SCL low time	t_{LOW}		1.3			µs
Data set-up time	$t_{SU,DAT}$		100			ns
Data hold time	$t_{HD,DAT}$		0		0.9	µs
Set-up time for repeated start	$t_{SU,STA}$		0.6			µs

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{EN} = 2V, T_J = -40°C to +125°C, typical value is at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Hold time for start	$t_{HD,STA}$		0.6			µs
Bus free time between start and stop condition	t_{BUF}		1.3			ms
Set-up time for stop condition	$t_{SU,STO}$		0.6			µs
Rise time of SCL and SDA	t_R		20 + 0.1 × C_B		300	ns
Fall time of SCL and SDA	t_F		20 + 0.1 × C_B		300	ns
Pulse width of suppressed spike	t_{SP}		0		50	ns
Capacitance bus for each bus line	C_B				400	pF

Notes:

5) Matching is defined as the difference of the maximum to minimum current divided by 2 times the average current.
6) Guaranteed by design.

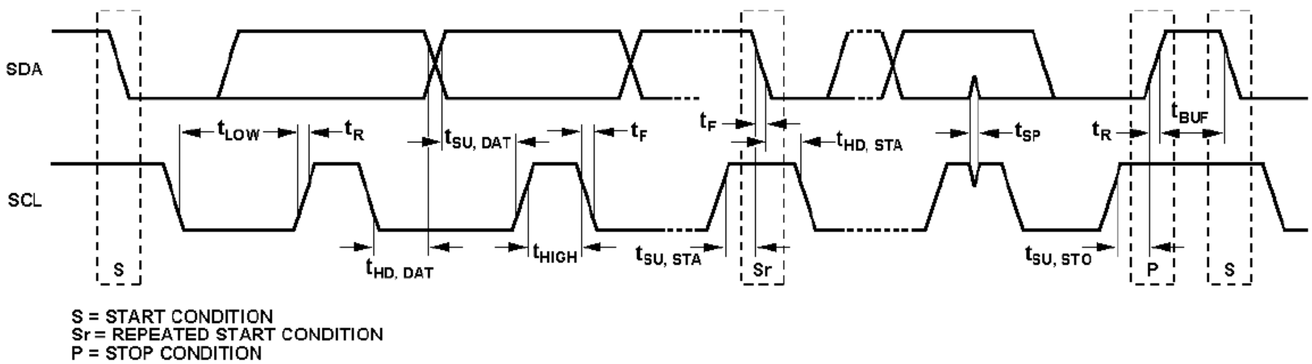


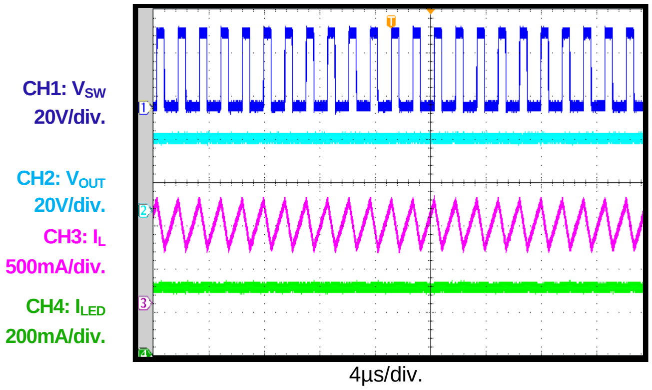
Figure 1: I²C-Compatible Interface Timing Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, L = 22µH, LED = 6P12S, f_{SW} = 400kHz, I_{SET} = 50mA, T_A = 25°C, unless otherwise noted.

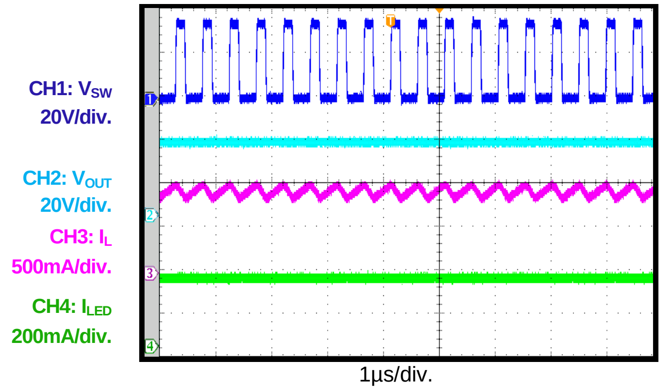
Steady State

f_{SW} = 400kHz

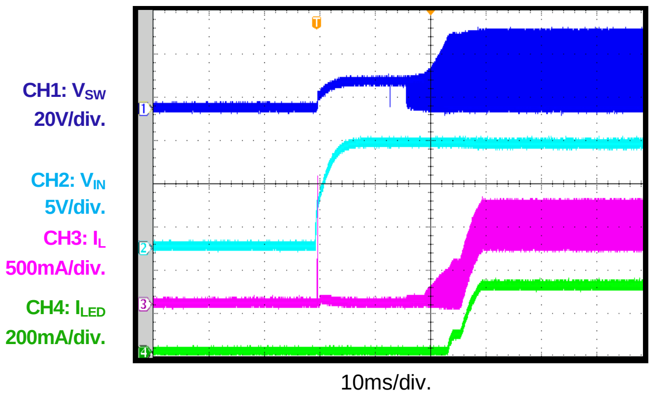


Steady State

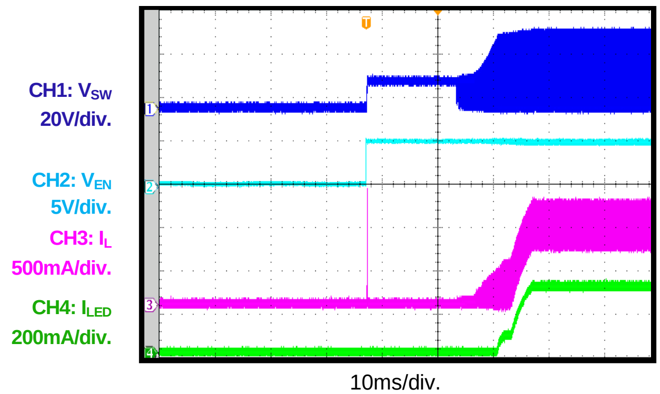
f_{SW} = 2.2MHz



VIN Power-On

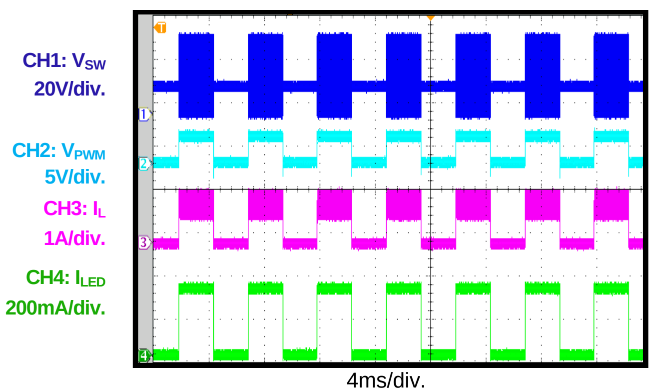


EN Power-On



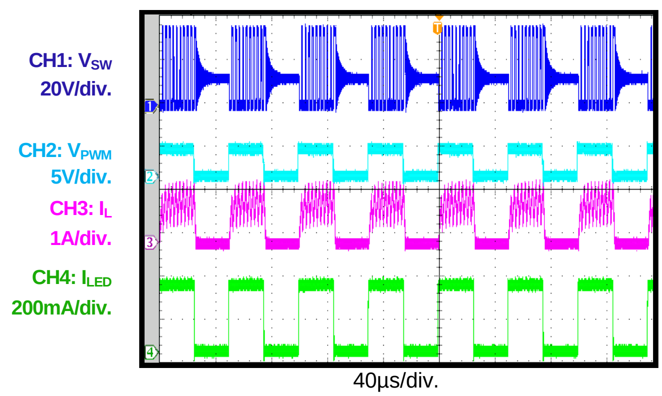
PWM Dimming

f_{PWM} = 200Hz, D_{PWM} = 50%



PWM Dimming

f_{PWM} = 20kHz, D_{PWM} = 50%

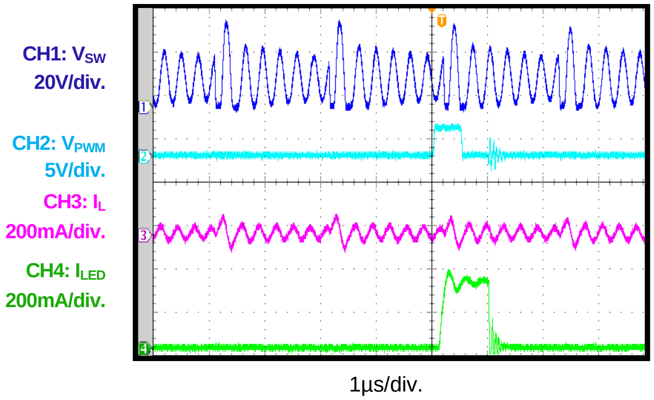


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, L = 22µH, LED = 6P12S, f_{SW} = 400kHz, I_{SET} = 50mA, T_A = 25°C, unless otherwise noted.

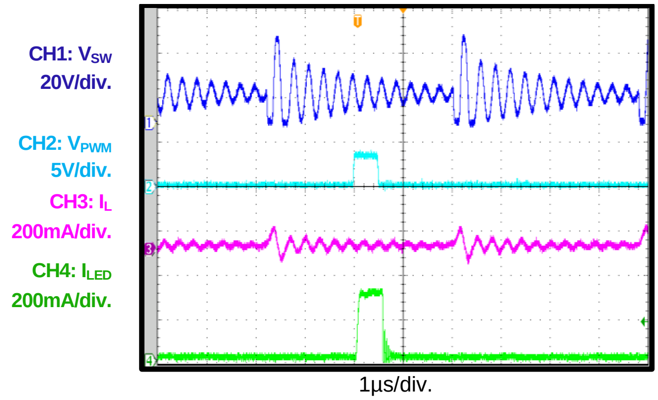
PWM Dimming

f_{PWM} = 200Hz, D_{PWM} = 0.01%



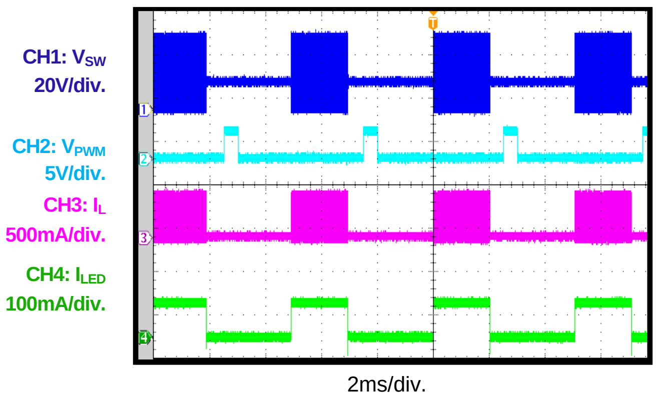
PWM Dimming

f_{PWM} = 100Hz, D_{PWM} = 0.005%



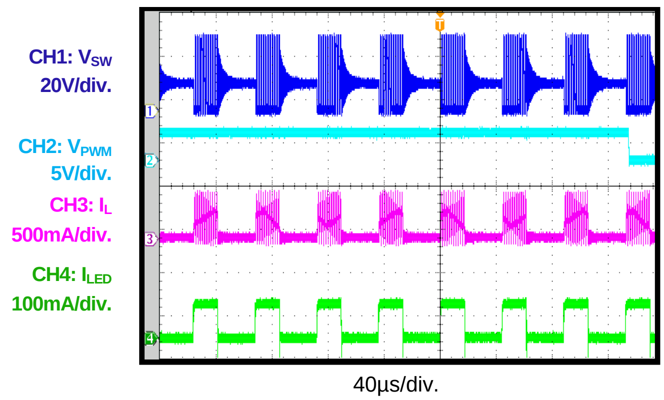
Mix Dimming

f_{PWM} = $f_{(ILED)}$ = 200Hz, D_{PWM} = 10%



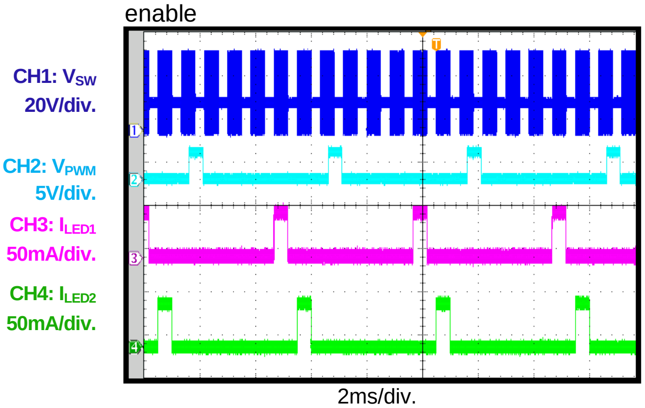
Mix Dimming

f_{PWM} = 200Hz, $f_{(ILED)}$ = 23kHz, D_{PWM} = 10%



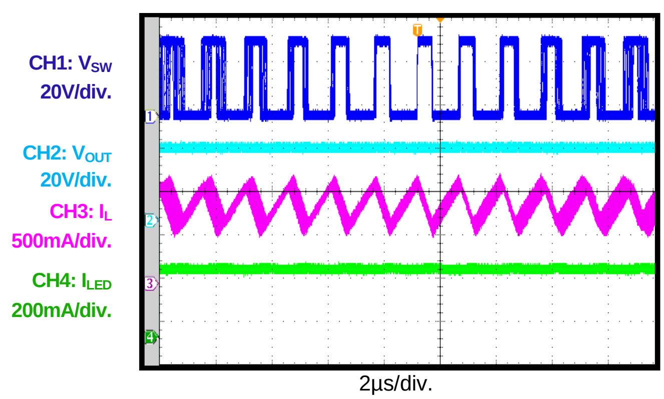
Phase Shift Function

f_{PWM} = 200Hz, PWM dimming, 6-channel enable



Frequency Spread Spectrum

1/100 of center frequency



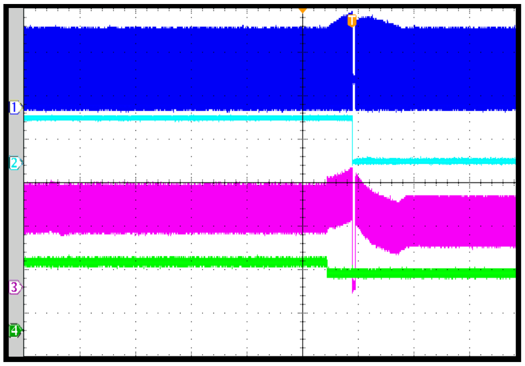
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, L = 22µH, LED = 6P12S, f_{SW} = 400kHz, I_{SET} = 50mA, T_A = 25°C, unless otherwise noted.

Open LED Protection

Open 1 string at working

CH1: V_{SW} 20V/div.
CH2: V_{FF} 5V/div.
CH3: I_L 500mA/div.
CH4: I_{LED} 200mA/div.

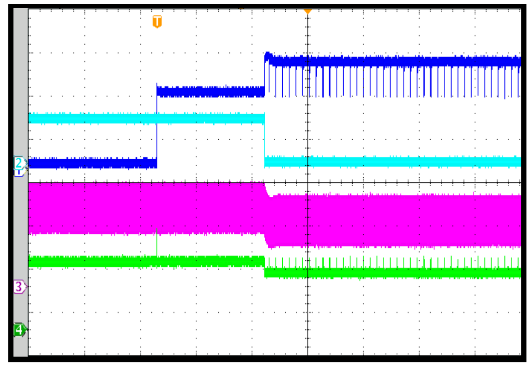


2ms/div.

Short LED Protection

Short 1 string at working

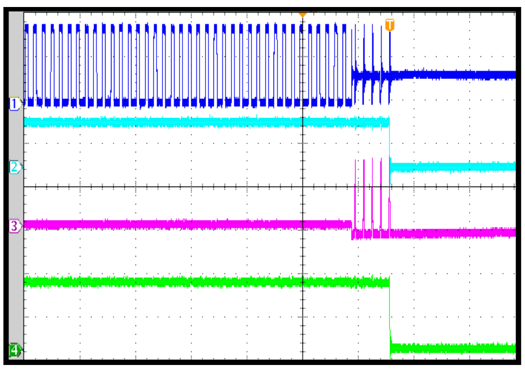
CH1: V_{LED6} 5V/div.
CH2: V_{FF} 5V/div.
CH3: I_L 500mA/div.
CH4: I_{LED} 200mA/div.



4ms/div.

Short Inductor Protection

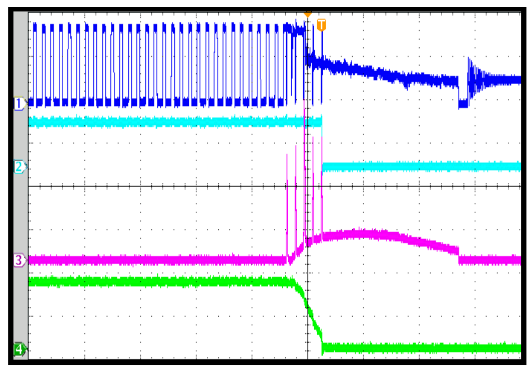
CH1: V_{SW} 20V/div.
CH2: V_{FF} 5V/div.
CH3: I_{L_SHORT} 5A/div.
CH4: I_{LED} 200mA/div.



10µs/div.

Short Diode Protection

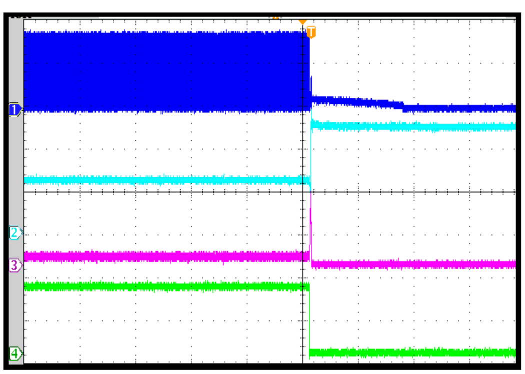
CH1: V_{SW} 20V/div.
CH2: V_{FF} 5V/div.
CH3: I_{L_SHORT} 5A/div.
CH4: I_{LED} 200mA/div.



10µs/div.

Short VOUT to GND Protection

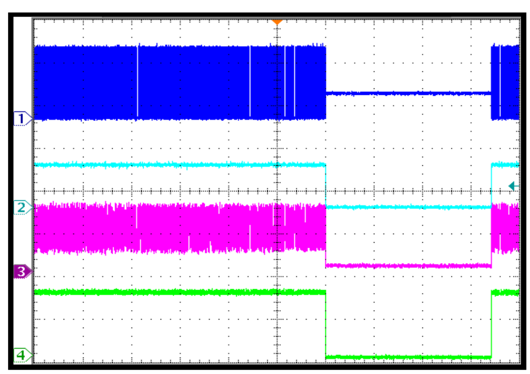
CH1: V_{SW} 20V/div.
CH2: V_{SD} 5V/div.
CH3: I_L 5A/div.
CH4: I_{LED} 200mA/div.



1ms/div.

Thermal Protection

CH1: V_{SW} 20V/div.
CH2: V_{FF} 5V/div.
CH3: I_L 1A/div.
CH4: I_{LED} 200mA/div.



1s/div.

FUNCTIONAL BLOCK DIAGRAM

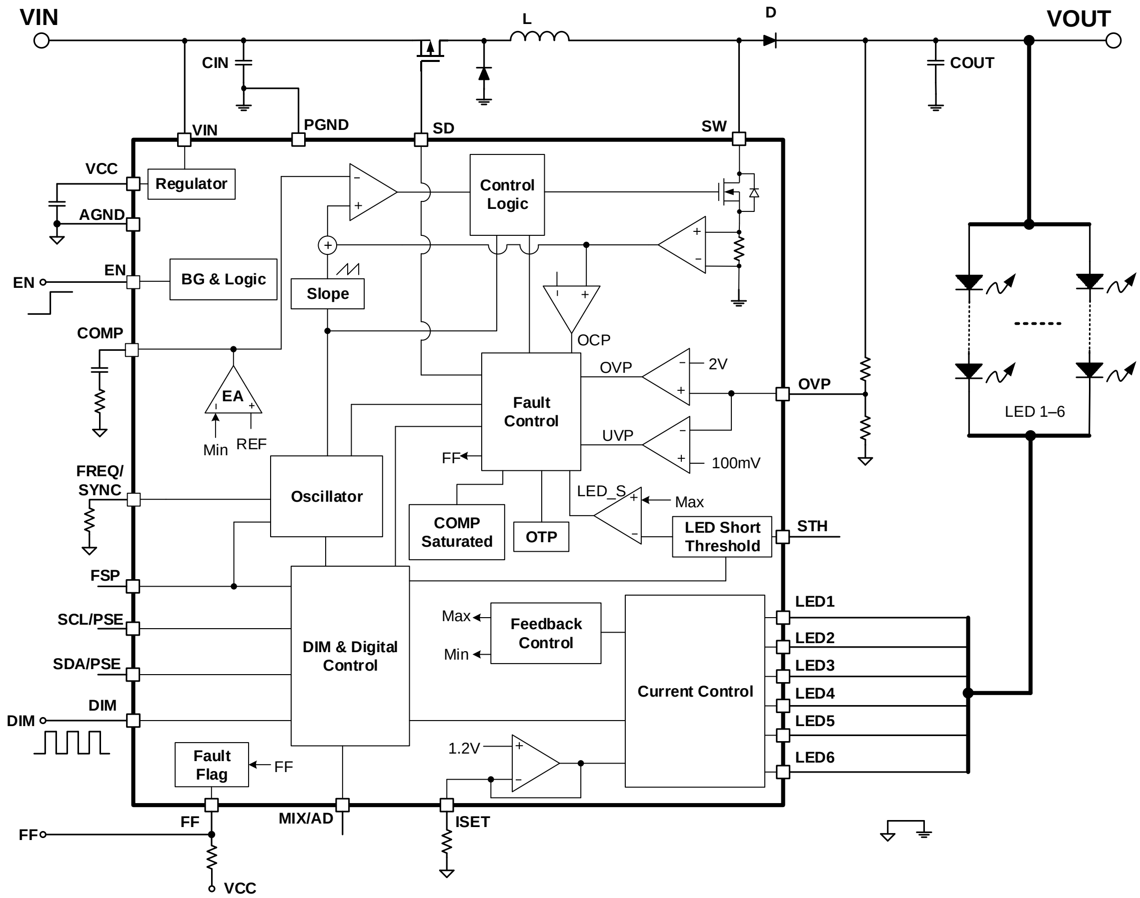


Figure 2: Functional Block Diagram

OPERATION

The MPQ3369-AEC1 is a programmable, constant-frequency, peak current mode step-up converter with up to six channels of regulated current sources to drive the array of white LEDs.

Internal 5V Regulator

The MPQ3369-AEC1 includes an internal linear regulator (VCC). When V_{IN} exceeds 6V, this regulator outputs a 5V power supply to the internal MOSFET switch gate driver and the internal control circuitry. The VCC voltage drops to 0V when the chip shuts down. The chip remains disabled until VCC exceeds the UVLO threshold.

System Start-Up

When enabled, the MPQ3369-AEC1 checks the topology connection. The IC draws current from SD to enable the input disconnect PMOS to be turned on (if this PMOS is used). After a 500μs delay, the IC monitors OVP to see if the output is shorted to GND. If the OVP voltage is less than 100mV, the IC disables and latches off. The MPQ3369-AEC1 then continues to check other safety limits (e.g. LED open, over-voltage protection). If all protection tests pass, the IC starts boosting the step-up converter with an internal soft start.

The recommended power-on sequence is V_{IN} → EN → I^2C (optional) → PWM dim signal.

Step-Up Converter

The MPQ3369-AEC1 employs peak-current mode control to regulate the output energy. At the beginning of each switching cycle, the internal clock turns on the internal N-MOSFET. In normal operation, the minimum turn-on time is about 100ns. A stabilizing ramp added to the output of the current-sense amplifier prevents sub-harmonic oscillations for duty cycles greater than 50%. This result is fed into the PWM comparator. When the summed voltage reaches the output voltage of the error amplifier, the internal MOSFET turns off.

The output voltage of the internal error amplifier is an amplified signal of the difference between the reference voltage and the feedback voltage. The converter automatically chooses the lowest active LEDx pin voltage to provide a high enough output voltage to power all the LED arrays.

If the feedback voltage drops below the reference voltage, the output of the error amplifier increases. More current then flows through the MOSFET, increasing the power delivered to the output. This forms a closed loop that regulates the output voltage.

During light-load operation, especially in the case of VOUT ≈ VIN, the converter runs in pulse-skipping mode. In this mode, the MOSFET turns on for a minimum on time, then the converter discharges the power to the output for the remaining period. The external MOSFET remains off until the output voltage needs to be boosted again.

Dimming Control

The MPQ3369-AEC1 provides analog, PWM, and mix dimming methods. The dimming mode can be set with the I^2C or by connecting a different resistor at MIX/AD. The voltage of MIX/AD is calculated with Equation (1):

$$V_{\_MIX/AD}(mV) = 18(\mu A) \times R_{\_MIX/AD}(k\Omega) \quad (1)$$

Where $V_{\_MIX/AD}$ is the voltage and $R_{\_MIX/AD}$ is the resistor at MIX/AD.

Mix Dimming Mode

There are two different ways the MPQ3369-AEC1 works in mix dimming mode, with 25% or 12.5% as its transfer point (selected through the internal register).

The first way is to connect a resistor and set MIX/AD to low (<0.3V).

The second is to float MIX/AD, and set the internal mode select register MODE1:0 = 00 through the I^2C.

A PWM dimming signal is applied to DIM. When the dimming duty is greater than 25%, analog dimming is adopted, and the LED current amplitude follows the duty of PWM. When the dimming duty is less than 25%, PWM dimming is used (see Figure 3). The LED current amplitude remains at 1/4 of the full-scale current, and the output dimming duty is 4 times the duty of the input PWM signal. There are two options for output dimming frequency when using mix dimming: 200Hz (default) or 23kHz (no audible noise, but larger minimum dimming duty).

This does not change based on the input PWM dimming frequency. The output dimming frequency is selected with the mix dimming output frequency selection bit through the I^2C.

This function eliminates audible noise and improves the dimming performance in a small dimming ratio.

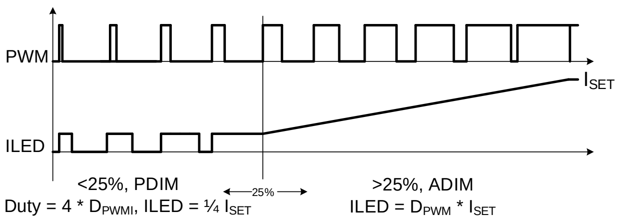


Figure 3: Mix Dimming with 25% Transfer Point

Direct PWM Dimming

Connect a resistor to set MIX/AD to a middle level (0.5V to 0.8V), or float MIX/AD and set the internal mode select register MODE1:0 = 01 through the I^2C.

When a PWM signal is applied to DIM, the amplitude of the LED current remains at the LED full-scale, and the LED current is chopped by the input PWM signal. The LED current duty follows the PWM input duty, and the LED current frequency is the same as the PWM input.

Analog Dimming Mode

Connect a resistor to set MIX/AD to a high level (1V to 1.3V), or float MIX/AD and set the internal mode select register MODE = 10 through the I^2C.

The PWM input signal is calculated by an internal counter. The amplitude of the LED current is equal to I_{SET} * D_{DIM}, where I_{SET} is the full-scale LED current and D_{DIM} is the duty of the input PWM signal. For better analog dimming performance, a 100Hz to 20kHz PWM signal is recommended.

To ensure good performance with a small dimming ratio, the minimum LEDx voltage shifts up to 2V when the dimming duty is below 10%. Analog dimming supports a 200:1 dimming ratio.

Deep Dimming Ratio for PWM Dimming

When the output dimming on time is less than 7µs, the output voltage is regulated to 0.93 of the OVP voltage (see Figure 4).

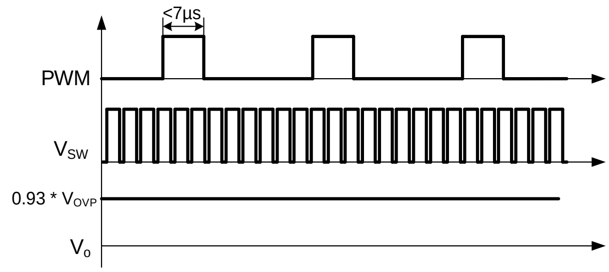


Figure 4: Deep Dimming Ratio for PWM Dimming

Unused LED Channel Setting

If the LEDx pin of an unused channel is connected to GND, the MPQ3369-AEC1 can automatically detect the unused LED string and remove it from the control loop during start-up. If employing five strings, connect LED6 to GND. If using four strings, connect LED5 and LED6 to GND, and so on.

The MPQ3369-AEC1 can also disable the unused string(s) with the internal register (CH2:0 bit):

- CH2:0 = 000: All 6 channels are in use
- CH2:0 = 001: LED1 – 5 are in use
- CH2:0 = 010: LED1–4 are in use
- CH2:0 = 011: LED1–3 are in use
- CH2:0 = 100: LED1–2 are in use
- CH2:0 = 101: LED1 is in use

Phase Shift Function

To reduce inrush current and eliminate audible noise during PWM dimming, the MPQ3369-AEC1 employs a phase shift function. Two methods can be used to enable the phase shift function:

The first is to connect SCL/PSE and SDA/PSE together to about 0.75V to 1V.

The second is to set the internal register PSE bit to 1 via the I^2C.

The LED channels' current source is phase-shifted when the IC employs PWM dimming. The shifted phase depends on which LED channels are in use, determined using Equation (2):

$$\text{Phase}(^\circ) = \frac{360}{n}(^\circ) \quad (2)$$

Where *n* is the LED channel in use. If all six channels are in use, the shifted phase is 60°. LED1 directly follows the input PWM signal, and LED2 lags 60° behind (see Figure 5).

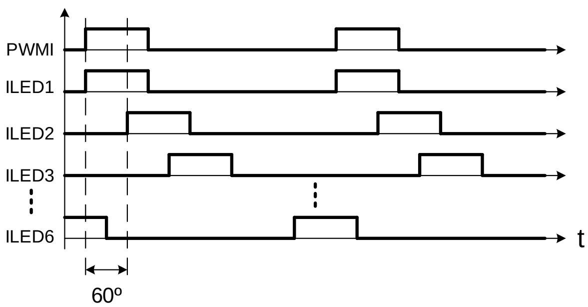


Figure 5: Phase Shift with Six Channels

Figure 6 shows the phase shift function with four channels enabled. The shifted phase in this case is 90°.

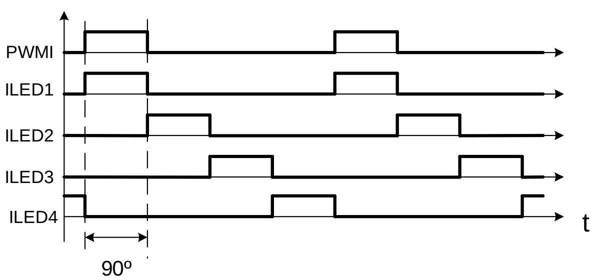


Figure 6: Phase Shift with Four Channels

In phase shift operation, the channels must be disabled in descending order of channel number. For example, if three strings are employed in application, then channels 6, 5, and 4 are disabled.

It is not recommended to tie two channels for one string of LED with the phase shift function.

Frequency Spread Spectrum

The MPQ3369-AEC1 uses switching frequency jitter to spread the switching frequency spectrum. This reduces the spectrum spike around the switching frequency and its harmonic frequencies.

The FSP pin can program the dithering range, and the modulation frequency is fixed to 1/150 of switching frequency:

- When FSP < 0.3V, the jitter frequency is 1/20 of the central frequency
- When FSP = 0.4V to 1.4V, the jitter frequency is 1/32 of the central frequency
- Float FSP to follow the internal I²C setting

The frequency jitter range selected by the FSPR bit determines the range:

- When FSPR = 0 (default), the jitter frequency is 1/20 of the central frequency
- When FSPR = 1, the jitter frequency is 1/32 of the central frequency

The modulation frequency is selected by the FSPMF1:0 bit:

- When FSPMF1:0 = 00, the modulation frequency is 1/100 of the switching frequency
- When FSPMF1:0 = 01, the modulation frequency is 1/150 of the switching frequency
- When FSPMF1:0 = 10, the modulation frequency is 1/200 of the central frequency
- When FSPMF1:0 = 11, default, the function is disabled

Protection

The MPQ3369-AEC1 includes open LED protection, short LED protection, short LEDx to GND protection, over-current protection, short VOUT to GND protection, and thermal protection. Once the protection is triggered, FF pulls to GND and the corresponding fault bit is set to 1. After the IC recovers from protection, FF releases to high with a 750µs delay.

Open LED Protection

Open string protection is achieved through detecting the voltage of OVP and LEDx. During operation, if one string is open, the respective LEDx voltage is low to ground, and the IC keeps charging the output voltage until it reaches the OVP threshold.

If OVP has been triggered, the chip stops switching and marks off the fault string, which has an LEDx pin voltage below 100mV. Once marked, the remaining LED strings force the output voltage back into normal regulation. The string with the largest voltage drop determines the output regulation value.

The marked-off string sends a 10µs pulse current to check whether an open fault is removed after every 500µs delay, so open string protection is recoverable.

Short String Protection

The MPQ3369-AEC1 monitors the LEDx voltages to determine whether a short string fault has occurred. When one or more strings are shorted, the respective LEDx pins tolerate high voltage stress. If an LEDx voltage is higher than the short protection threshold, an internal counter starts. When this fault condition lasts for 7.7ms (D_{PWM} = 100%), the fault string is marked off. Once a string is marked off, it disconnects from the output voltage loop until the short is removed.

The short protection threshold can be set one of two ways:

The first option is to connect a resistor at STH.

STH outputs a 18µA current source. The short protection threshold is 10 times the voltage on STH. The threshold is calculated using Equation (3):

$$V_{\_STH}(V) = 0.18 \times R_{\_STH}\ (k\Omega) \tag{3}$$

The second option is to set the internal register TH_S1:0 when STH is floating.

When the LEDx voltage exceeds the threshold for 480ms (D_{PWM} = 100%), all strings are marked off. The IC remains on standby until the strings release from shorting. Enable or disable this function through SEN.

The marked-off string sends a 10µs pulse current to check if a short fault is removed after every 500µs delay, so short string protection is recoverable.

Short LEDx to GND Protection

When LEDx shorts to GND, the COMP voltage increases and saturates. When the COMP saturation time lasts for 20ms or 40ms (the time can be selected by the internal register bit TCOMP), protection is triggered. Then FF pulls low and SD pulls high to turn on the external P-MOSFET. The IC also latches off.

Short VOUT to GND Protection

When VOUT shorts to GND, the output voltage decreases. When the voltage of the OVP pin reaches the OVP UVLO threshold for 10µs, the protection is triggered and SD pulls high to turn off the external P-MOSFET. VOUT disconnects from VIN, and the IC latches off.

Cycle-by-Cycle Current Limit

To prevent the external components from exceeding the current stress rating, the IC has cycle-by-cycle current limit protection. When the current exceeds the current limit value, the IC stops switching until the next clock cycle.

Latch-Off Current Limit Protection

Extreme conditions, such as an inductor or diode short, may cause damage to the device. To avoid this, the MPQ3369-AEC1 provides a latch-off current limit protection when the current flowing through the internal MOSFET reaches the threshold (7.5A), and lasts for five switching cycles.

Thermal Protections

To prevent the IC from damage when operating at exceedingly high temperatures, the MPQ3369-AEC1 implements thermal protections by detecting the silicon die temperature.

Over-Temperature LED Current Decrement

When the die temperature exceeds 140°C, the MPQ MPQ3369-AEC1 3369 automatically decreases the LED current amplitude (see Figure 7).

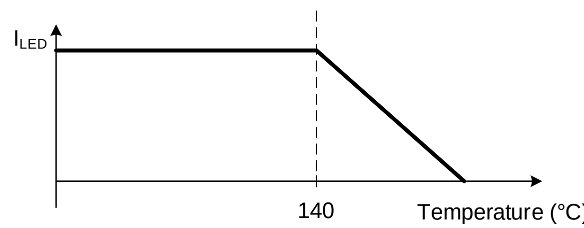


Figure 7: I_{LED} Decrease with Temperature

This function is enabled by the over-temperature current decrement bit OTID:

- When OTID = 0, the over-temperature current decrement is disabled
- When OTID = 1 (default), the over-temperature current decrement is enabled

Thermal Shutdown

When the die temperature exceeds the upper threshold (T_{ST}), the IC shuts down and recovers to normal operation. When the temperature drops below the lower threshold, the IC recovers. The hysteresis value is typically 20°C.

I²C Interface Register Description

I²C Chip Address

The 7-bit MSB device address is 0x38. After the start condition, the I²C-compatible master sends a 7-bit address followed by an eighth read (1) or write (0) bit.

The following bit indicates the register address to/from which the data will be written/read.

0	1	1	1	0	0	0	R/W

The I²C-Compatible Device Address

Register Mapping:

Add	D7	D6	D5	D4	D3	D2	D1	D0
00H	OTID	MODE1	MODE0	MIXTP	MIXFR	FSPMF1	FSPMF0	FSPR
01H	PSEN	TH_S1	TH_S0	FSW1	FSW0	CH2	CH1	CH0
02H	SEN	TCOMP	FT_LEDG	FT_OTP	FT_UVP	FT_OCP	FT_LEDS	FT_LEDO
03H	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0

Note: Leave corresponding pins floating if internal registers are used.

Table 1: Function Set Register 1

Addr: 0x00				
Bit	**Bit Name**	**Access**	**Default**	**Description**
7	OTID	RW	1	Over-temperature LED current decrement function enable bit. 0: Disabled 1: Enabled
6:5	MODE	RW	00	Dimming mode selection bit. 00: Mix dimming 01: PWM dimming 10: Analog dimming 11: Reserved Float MIX/AD if this register is adopted.
4	MIXTP	RW	0	Mix dimming transfer point selection bit. 0: 25% transfer point 1:12.5% transfer point
3	MIXFR	RW	0	Mix dimming output frequency selection bit. 0: 200Hz 1: 23kHz
2:1	FSPMF1:0	RW	11	Frequency spread spectrum modulation frequency selection bit. 00: 1/100 of central frequency 01: 1/150 of central frequency 10: 1/200 of central frequency 11: Frequency spread spectrum function disabled Float FSP if this register is used.
0	FSPR	RW	0	Frequency spread spectrum jitter range selection bit. 0: 1/20 of central frequency 1: 1/32 of central frequency Float FSP if this register is used.

Table 2: Function Set Register 2

Addr: 0x01				
Bit	**Bit Name**	**Access**	**Default**	**Description**
7	PSE	RW	0	Phase shift enable bit. 0: Phase shift disabled 1: Phase shift enabled
6:5	TH_S1:0	RW	01	LED short protection threshold set bit. 00: 2.5V 01: 5V 10: 7.5V 11: 10V
4:3	FSW1:0	RW	01	Switching frequency set bit. 00: 200kHz 01: 400kHz 10: 1MHz 11: 2.2MHz Float FREQ if this register is used.
2:0	CH2:0	RW	000	Channel selection bit. 000: All 6 channels are in use 001: LED1–5 are in use 010: LED1–4 are in use 011: LED1–3 are in use 100: LED1–2 are in use 101: LED1 is in use 110, 111: Reserved

Table 3: Fault Register

Addr: 0x02				
Bit	**Bit Name**	**Access**	**Default**	**Description**
7	SEN	RW	0	Short all LED protection @ D_{PWM} > 2%. 0: Disable 1: Enable
6	TCOMP	RW	0	COMP-saturated time select bit for short LEDx to GND. 0: 20ms 1: 40ms
5	FT_LEDG	R	0	LEDx short to GND protection fault indication bit. If a fault occurs, the fault bit remains 1 until readback or power reset. 0: No fault 1: Fault The fault status can latch off until it is reset to 0 after this bit is read.
4	FT_OTP	R	0	Over-temperature protection fault indication bit. If a fault occurs, the fault bit remains 1 until readback or power reset. 0: No fault 1: Fault The fault status can latch off until it is reset to 0 after this bit is read.
3	FT_UVP	R	0	Output under-voltage protection fault indication bit. If a fault occurs, the fault bit remains 1 until readback or power reset. 0: No fault 1: Fault The fault status can latch off until it is reset to 0 after this bit is read.
2	FT_OCP	R	0	Over-current protection fault indication bit. If a fault occurs, the fault bit remains 1 until readback or power reset. 0: No fault 1: Fault The fault status can latch off until it is reset to 0 after this bit is read.
1	FT_LEDS	R	0	LED current source short fault indication bit. If a fault occurs, the fault bit remains 1 until readback or power reset. 0: No fault 1: Fault The fault status can latch off until it is reset to 0 after this bit is read.

0	FT_LEDO	R	0	LED current source open fault indication bit. If a fault occurs, the fault bit remains 1 until readback or power reset. 0: No fault 1: Fault The fault status can latch off until it is reset to 0 after this bit is read.

Table 4: ID Register

Addr: 0x03				
Bit	**Bit Name**	**Access**	**Default**	**Description**
7:0	ID7:0	R	01100111	Device ID bits.

APPLICATION INFORMATION

LED Current Setting

The LED current amplitude is set by an external resistor connected from ISET to GND. The LED current amplitude setting is determined with Equation (4):

$$I_{LED}(mA) = \frac{1245}{R_{ISET}(k\Omega)} \quad (4)$$

For R_{ISET} = 24.9kΩ, the LED current is 50mA.

Switching Frequency

The switching frequency can be programmed with a resistor, the I²C interface, or an external clock.

To program the frequency through an external resistor on FREQ/SYNC, use Equation (5) to determine the switching frequency:

$$f_{SW}(kHz) = \frac{22000}{R_{OSC}(k\Omega)} \quad (5)$$

For R_{OSC} = 44.2kΩ, the switching frequency is set to 500kHz.

Synchronize the switching frequency through an external clock to improve EMI, efficiency, and thermal performance.

For setting the switching frequency bit (fSW1:0):

- 00: 200kHz
- 01: 400kHz
- 10: 1MHz
- 11: 2.2MHz

Float FREQ if the fSW1:0 bit is used.

Selecting the Input Capacitor

The input capacitor reduces the surge current drawn from the input supply and the switching noise from the device. The input capacitor impedance at the switching frequency should be less than the input source impedance to prevent the high-frequency switching current from passing through to the input. Use ceramic capacitors with X5R or X7R dielectrics for their low ESR and small temperature coefficients. For most applications, a 10μF ceramic capacitor is sufficient.

Selecting the Inductor

The MPQ3369-AEC1 requires an inductor to supply a higher output voltage while being driven by the input voltage. A larger-value inductor results in less ripple current, lower peak inductor current, and less stress on the internal N-channel MOSFET. However, the larger-value inductor has a larger physical size, higher series resistance, and lower saturation current.

Choose an inductor that does not saturate under worst-case load conditions. Select the minimum inductor value to ensure that the boost converter works in continuous conduction mode with high efficiency and good EMI performance.

Calculate the required inductance values using Equation (6) and Equation (7):

$$L \geq \frac{\eta \times V_{OUT} \times D \times (1-D)^2}{2 \times f_{SW} \times I_{LOAD}} \quad (6)$$

$$D = 1 - \frac{V_{IN}}{V_{OUT}} \quad (7)$$

Where V_{IN} and V_{OUT} are the input and output voltages, f_{SW} is the switching frequency, I_{LOAD} is the LED load current, and η is the efficiency.

With the given inductor value, the inductor DC current rating is at least 40% greater than the maximum input peak inductor current for most applications. The inductor's DC resistance should be as small as possible for higher efficiency.

Selecting the Output Capacitor

The output capacitor keeps the output voltage ripple small and ensures feedback loop stability. The output capacitor impedance must be low at the switching frequency. Ceramic capacitors with X7R dielectrics are recommended for their low ESR. For most applications, a 10μF ceramic capacitor is sufficient.

TYPICAL APPLICATION CIRCUITS

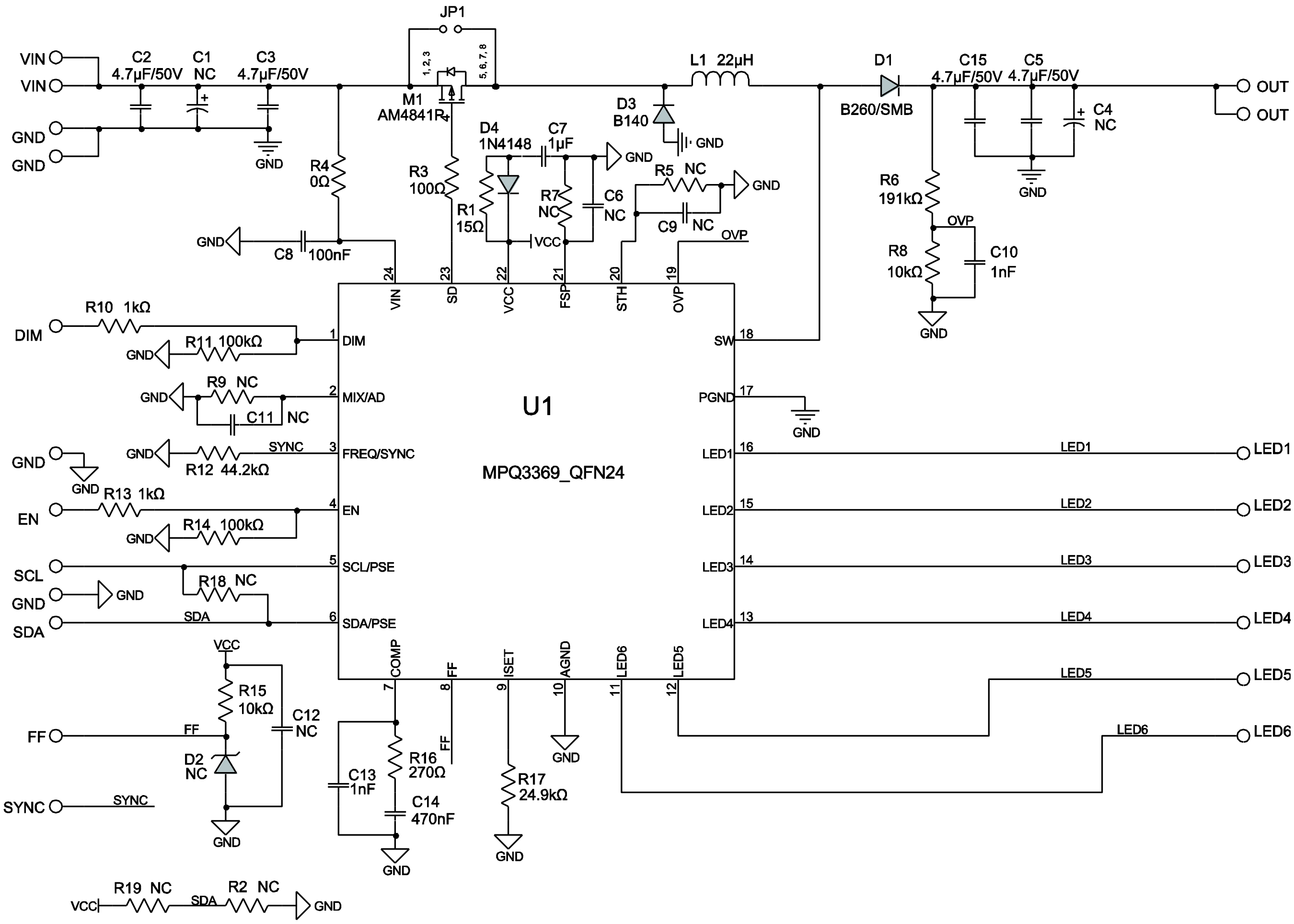
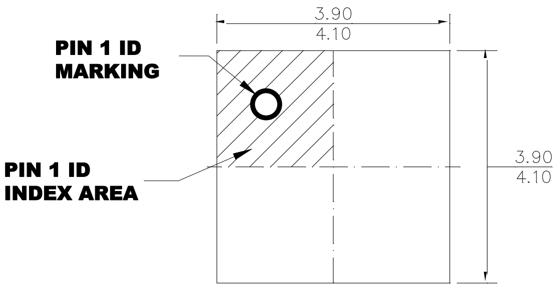


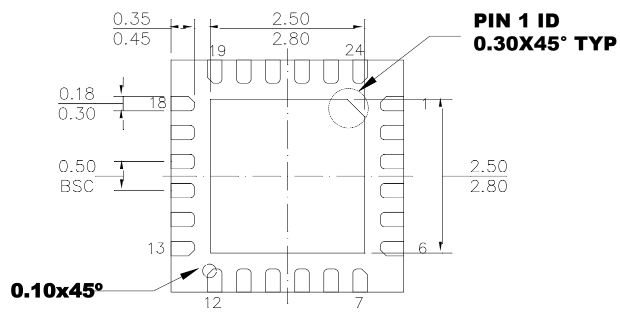
Figure 8: Typical Application Circuit

PACKAGE INFORMATION

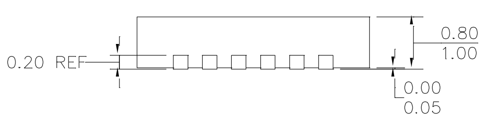
QFN-24 (4mmx4mm)



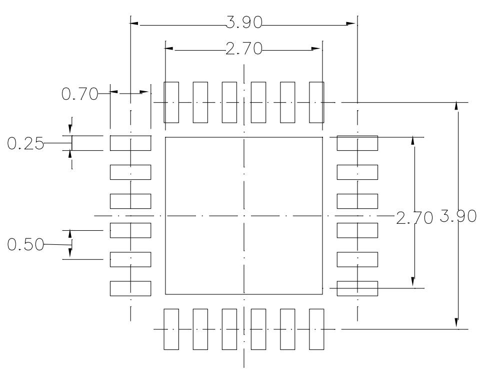
TOP VIEW



BOTTOM VIEW



SIDE VIEW



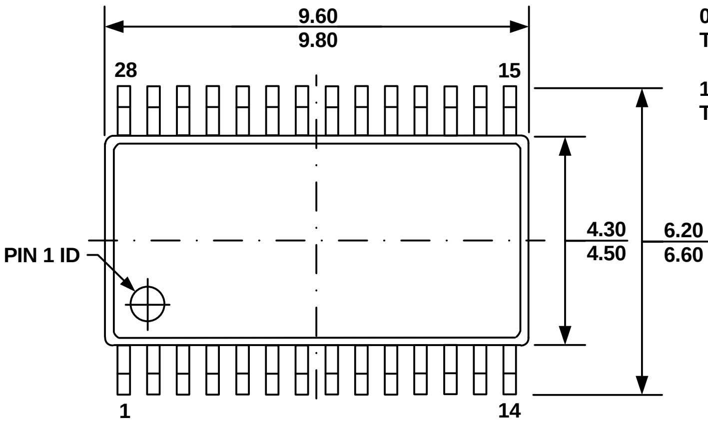
RECOMMENDED LAND PATTERN

NOTE:

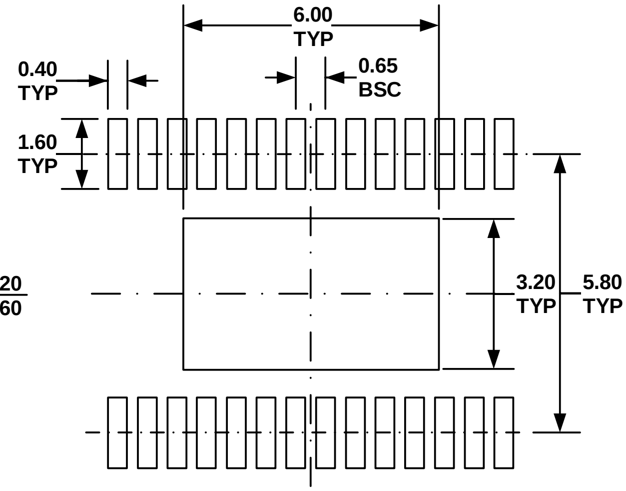
1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220
5) DRAWING IS NOT TO SCALE.

PACKAGE INFORMATION

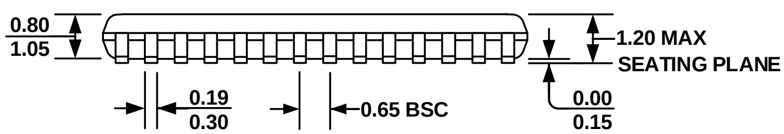
TSSOP28-EP



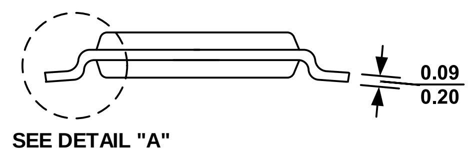
TOP VIEW



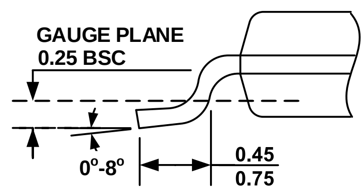
RECOMMENDED LAND PATTERN



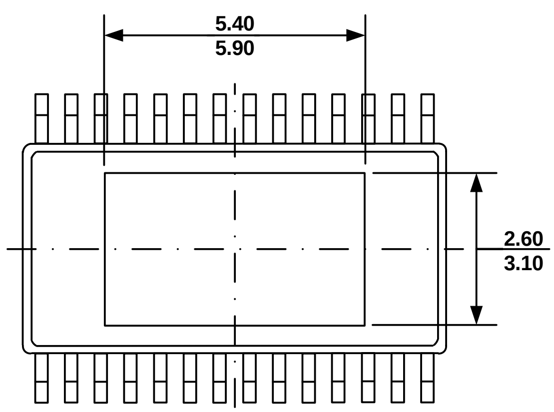
FRONT VIEW



SIDE VIEW



DETAIL “A”



BOTTOM VIEW

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION, OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING CONFORMS TO JEDEC MO-153, VARIATION AET.
6) DRAWING IS NOT TO SCALE.

REVISION HISTORY

Revision #	Revision date	Description	Pages Updated
R1.01	2020.07.03	1. In the SCL/PSE and SDA/PSE pin description, add a sentence “If it isn’t used, please pull it to GND” 2. Add the storage temperature range 3. updating a waveform(PWM dimming, 100Hz, duty=0.005%) of TPC 4. updating the Typical application circuit	1. P5 2. P6 3. P11 4. P24