# MPQ3323B

## 4-Channel, 320mA/Ch, LED Driver with Separated PWM/Analog Dimming and $I^2C$ Interface, AEC-Q100 Qualified

## DESCRIPTION

The MPQ3323B is a 4-channel LED driver that can operate from a wide 4.5V to 16V input voltage ($V_{IN}$) range. The MPQ3323B applies four internal current sources in each LED string terminal. The LED current ($I_{LED}$) of each channel is set by an external current-setting resistor. The maximum current for each channel is 320mA.

The MPQ3323B integrates an $I^2C$ interface with up to 10 configurable $I^2C$ addresses via an external resistor. This means the MPQ3323B can support up to 10 ICs cascaded ICs to drive the LED array. Each channel can be enabled or disabled via the $I^2C$.

The MPQ3323B employs both separated pulse-width modulation (PWM) dimming and analog dimming for each LED channel, as well as 12-bit PWM dimming and 6-bit analog dimming for each channel. The $I_{LED}$ ramping rate and phase shift can be configured to reduce EMI.

The MPQ3323B can output a refresh signal from the RFSH/FLT pin. The refresh signal frequency ($f_{REFRESH}$) can be set via the $I^2C$.

Full protections features include LED open protection, LED short protection, and over-temperature protection (OTP). The device also features a fault indicator. If a protection is triggered, then the RFSH/FLT pin is pulled low, and the corresponding fault register is set.

The MPQ3323B is AEC-Q100 qualified, and is available in a QFN-24 (4mmx4mm) package.

## FEATURES

- Wide 4.5V to 16V Input Voltage ($V_{IN}$) Range
- 4 Channels, Max 320mA/Ch
- LED Current ($I_{LED}$) Configured via External Resistor
- 6-Bit Analog Dimming for Each Channel
- 12-Bit Pulse-Width Modulation (PWM) Dimming for Each Channel
- Selectable 220Hz, 250Hz, 280Hz, or 330Hz PWM Dimming Frequency ($f_{PWM}$)
- Refresh Signal Output
- $I^2C$ Interface
- 10 Addresses Configurable via External Resistor
- Configurable $I_{LED}$ Slew Rate
- Fault Indicator
- LED Open Protection
- LED Short Protection with Configurable Threshold
- Under-Voltage Lockout (UVLO) Protection
- Over-Temperature Protection (OTP)
- Available in a QFN-24 (4mmx4mm) Package
- Available in a Wettable Flank Package
- Available in AEC-Q100 Grade 1

## APPLICATIONS

- Automotive Displays
- Instruments Clusters
- General Industrial Displays

# TYPICAL APPLICATION

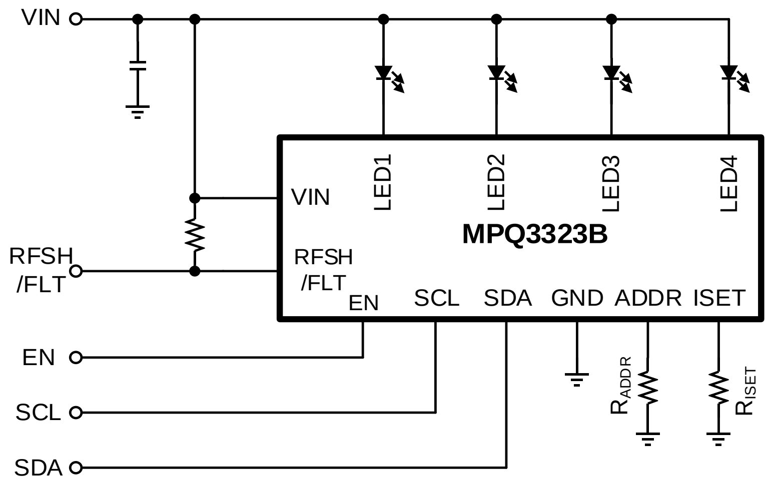



**Figure 1: Typical Application**

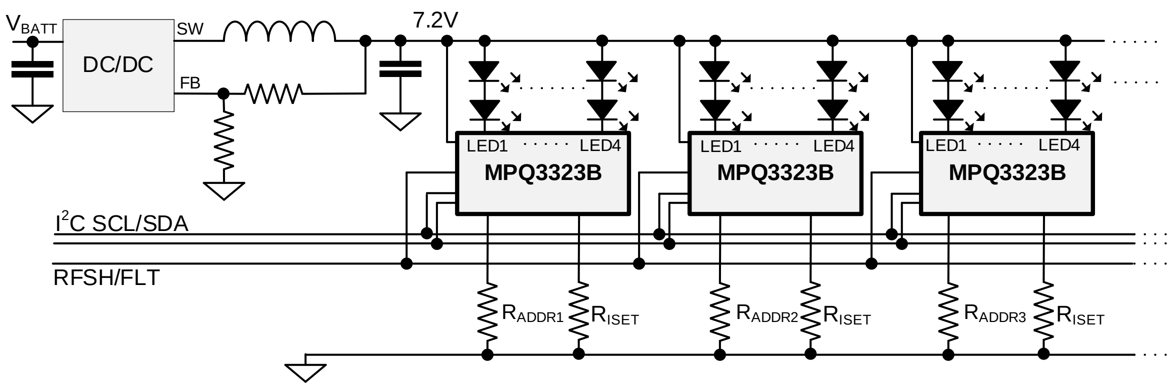



**Figure 2: System Application Circuit with 2 LEDs in Series**

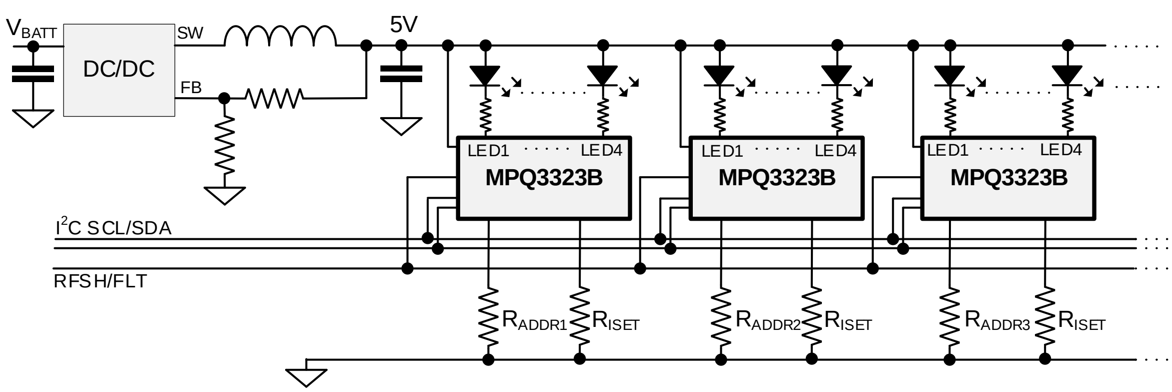



**Figure 3: System Application Circuit with 1 LED and Resistor in Series**

## ORDERING INFORMATION

| Part Number* | Package | Top Marking | MSL Level** |
|---|---|---|---|
| MPQ3323BGRE-AEC1*** | QFN-24 (4mmx4mm) | *See Below* | 1 |

* For Tape & Reel, add suffix -Z (e.g. MPQ3323BGRE-AEC1-Z).

** Moisture Sensitivity Level Rating

*** Wettable flank

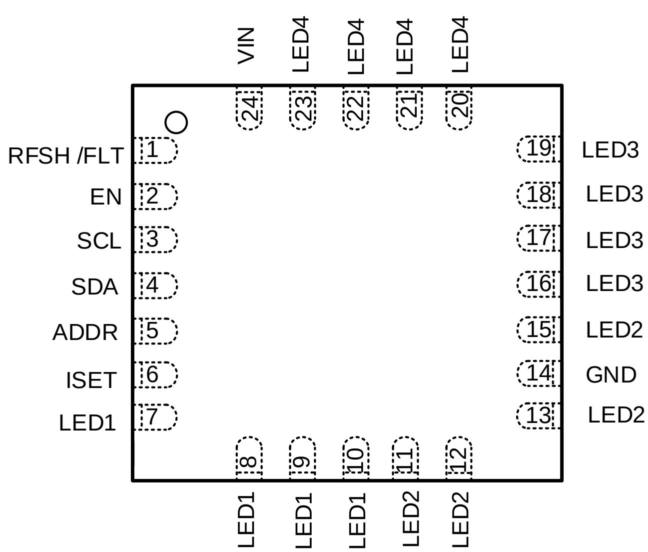
## TOP MARKING

MPSYWW
M3323B
LLLLLL
E

MPS: MPS prefix
Y: Year code
WW: Week code
M3323B: Part number
LLLLLL: Lot number
E: Wettable Flank

## PACKAGE REFERENCE

**TOP VIEW**




**QFN-24 (4mmx4mm)**

## PIN FUNCTIONS

| Pin # | Name | Description |
|---|---|---|
| 1 | RFSH/FLT | **Refresh signal output or fault flag.** If the FLTEN bit = 0, then the RFSH/FLT pin outputs a synchronized signal that is set by the FRFSH[9:0] register. If FLTEN = 1, RFSH/FLT is used to indicate fault conditions and is pulled low if a fault occurs. |
| 2 | EN | **Enable control.** Pull the EN pin high to turn the LED driver on; pull EN low to turn it off. |
| 3 | SCL | **I²C interface clock input.** |
| 4 | SDA | **I²C interface data input.** |
| 5 | ADDR | **I²C address setting.** Configure the I²C addresses by attaching different resistors between the ADDR and GND pins. ADDR sets the 4 least significant bits (LSB) of the I²C address. There are 10 configurable addresses. |
| 6 | ISET | **LED current setting.** Connect a current-setting resistor between the ISET and GND pins to configure the current in each LED string. |
| 7, 8, 9, 10 | LED1 | **LED channel 1 current input.** Connect the LED channel 1 cathode to this pin. There are four LED1 pins per channel. Connect these four pins together. |
| 11, 12, 13, 15 | LED2 | **LED channel 2 current input.** Connect the LED channel 2 cathode to this pin. There are four LED2 pins per channel. Connect these four pins together. |
| 14 | GND | **Ground.** |
| 16, 17, 18, 19 | LED3 | **LED channel 3 current input.** Connect the LED channel 3 cathode to this pin. There are four LED3 pins per channel. Connect these four pins together. |
| 20, 21, 22, 23 | LED4 | **LED channel 4 current input.** Connect the LED channel 4 cathode to this pin. There are four LED4 pins per channel. Connect these four pins together. |
| 24 | VIN | **Power supply input.** The VIN pin supplies power to the IC. Connect a capacitor between the VIN and GND pins. |

## ABSOLUTE MAXIMUM RATINGS (1)

$V_{IN}$ ....................................................-0.3V to +22V
$V_{LED1}$ to $V_{LED4}$.................................-0.5V to +22V
All other pins ..................................-0.3V to +5V
Junction temperature ...............................150°C
Lead temperature ....................................260°C
Storage temperature ................ -65°C to +150°C
Continuous power dissipation ($T_A$ = 25°C) (2)
QFN-24 (4mmx4mm).............................. 2.97W

### *ESD Ratings*

Human body model (HBM)............... Class 1C (3)
Charged device model (CDM)......... Class C2b (4)

### *Recommended Operating Conditions*

Input voltage ($V_{IN}$) ............................4.5V to 16V
Operating junction temp ($T_J$) (5)........................
.........................................-40°C to +125°C

### *Thermal Resistance* $\theta_{JA}$ $\theta_{JC}$

QFN-24 (4mmx4mm)
JESD51-7 (6) ........................... 42 ....... 9.... °C/W

**Notes:**

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature $T_J$ (MAX), the junction-to-ambient thermal resistance $\theta_{JA}$, and the ambient temperature $T_A$. The maximum allowable continuous power dissipation at any ambient temperature is calculated by $P_D$ (MAX) = ($T_J$ (MAX) - $T_A$) / $\theta_{JA}$. Exceeding the maximum allowable power dissipation can generate an excessive die temperature, which may cause the device to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) Per AEC-Q100-002.
4) Per AEC-Q100-011.
5) Operating devices at a junction temperature up to 150°C is possible. Please contact an MPS FAE for details.
6) Measured on a JESD51-7, 4-layer PCB. The values given in this table are only valid for comparison with other packages and cannot be used for design purposes. These values are calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application. The $\theta_{JC}$ value shows the thermal resistance from the junction to case bottom.

# ELECTRICAL CHARACTERISTICS

**$V_{IN}$ = 5V, $V_{EN}$ = 5V, $T_J$ = -40°C to +125°C, typical values are tested at $T_J$ = 25°C, unless otherwise noted.**

| Parameter | Symbol | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Input Supply Voltage** | | | | | | |
| Input voltage | $V_{IN}$ | | 4.5 | | 16 | V |
| Quiescent supply current | $I_Q$ | | | | 5 | mA |
| Shutdown supply current | $I_{SD}$ | $V_{EN}$ = 0V, $V_{IN}$ = 16V | | | 2 | μA |
| $V_{IN}$ under-voltage lockout (UVLO) rising threshold | $V_{IN\_UVLO\_RISING}$ | Rising edge | 3.5 | 3.7 | 3.9 | V |
| $V_{IN}$ UVLO falling threshold | $V_{IN\_UVLO\_FALLING}$ | Falling edge | 3.2 | 3.4 | 3.6 | V |
| **Enable (EN)** | | | | | | |
| EN rising threshold | $V_{EN\_RISING}$ | $V_{EN}$ rising | 2.1 | | | V |
| EN falling threshold | $V_{EN\_FALLING}$ | $V_{EN}$ falling | | | 0.8 | V |
| EN pull-down resistance | $R_{EN}$ | | | 1 | | MΩ |
| **RFSH/FLT** | | | | | | |
| Refresh signal frequency | $f_{REFRESH}$ | FRFSH[9:0] = 0x1A9, FPWM[1:0] = 01 | 285 | 300 | 315 | Hz |
| RFSH/FLT pull-down resistance | $R_{RFSH/FLT}$ | FLTEN = 1, a fault has occurred | | | 100 | Ω |
| **LED Regulator** | | | | | | |
| ISET voltage | $V_{ISET}$ | $T_A$ = 25°C | 1.176 | 1.2 | 1.224 | V |
| LED current 1 | $I_{LED1}$ | $R_{ISET}$ = 24kΩ, ICHx[5:0] = 0x3F | -5% | 200 | +5% | mA |
| | | $R_{ISET}$ = 24kΩ, ICHx[5:0] = 0x3F, $T_A$ = 25°C | -3% | 200 | +3% | mA |
| LED current 2 | $I_{LED2}$ | $R_{ISET}$ = 15kΩ, ICHx[5:0] = 0x3F | -5% | 320 | +5% | mA |
| | | $R_{ISET}$ = 15kΩ, ICHx[5:0] = 0x3F, $T_A$ = 25°C | -3% | 320 | +3% | mA |
| Current sink headroom | $V_{LEDX}$ | $I_{LED}$ = 200mA | | 200 | 300 | mV |
| | | $I_{LED}$ = 320mA | | 380 | 480 | mV |
| **Dimming** | | | | | | |
| Pulse-width modulation (PWM) frequency | $f_{PWM}$ | FPWM[1:0] = 01 | 240 | 250 | 260 | Hz |
| PWM duty step | $t_{PWM}$ | 12-bit resolution, $f_{PWM}$ = 250Hz | | 1 | | μs |
| Phase shift | $t_{DELAY}$ | PS_EN = 1 | | 160 | | μs |
| LED current step | | $I_{LED}$ = 320mA, analog dimming step | | 5 | | mA |
| LED current slew rate during PWM dimming | | SLEW[1:0] = 01, rising edge | | 5 | | μs |
| | | SLEW[1:0] = 11, rising edge | | 20 | | μs |
| **Protections** | | | | | | |
| LED short string protection threshold | $V_{SLP}$ | STH[1:0] = 01 | 2.85 | 3 | 3.15 | V |
| LED short string protection time | $t_{SLP}$ | $V_{LEDx}$ > STH[1:0] | | 4 | | ms |
| LED short string protection hiccup time | $t_{SLP\_HICCUP}$ | | | 1 | | ms |

## ELECTRICAL CHARACTERISTICS *(continued)*

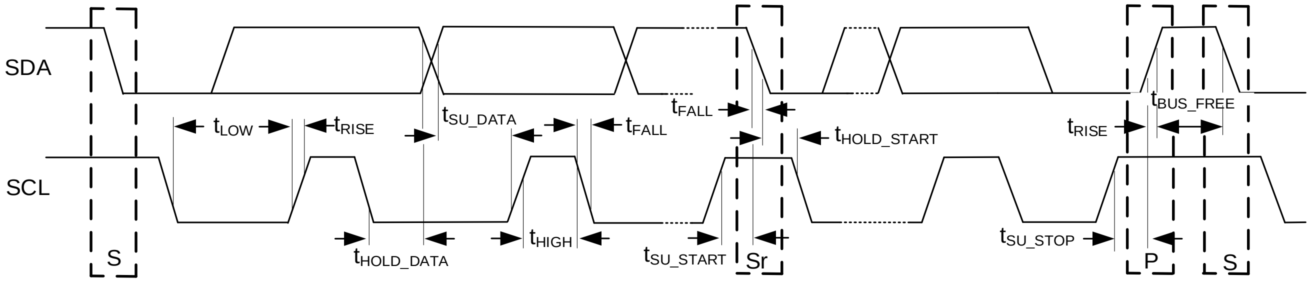
**$V_{IN}$ = 5V, $V_{EN}$ = 5V, $T_J$ = -40°C to +125°C, typical values are tested at $T_J$ = 25°C, unless otherwise noted.**

| Parameter | Symbol | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| LED short string protection hiccup detection time | $t_{SLP\_DET}$ | | | 32 | | μs |
| LED open string protection threshold | $V_{OLP}$ | | | 100 | 150 | mV |
| LED open string protection time | $t_{OLP}$ | $V_{LEDx}$ < 100mV | | 4 | | ms |
| LED open string protection hiccup time | $t_{OLP\_HICCUP}$ | | | 1 | | ms |
| LED open string protection hiccup detection time | $t_{OLP\_DET}$ | | | 32 | | μs |
| Thermal shutdown threshold (7) | $T_{SD}$ | | | 170 | | °C |
| Thermal shutdown hysteresis (7) | $T_{SD\_HYS}$ | | | 20 | | °C |
| **I²C Interface** | | | | | | |
| Logic-low input voltage | $V_{IN\_LOW}$ | | 0 | | 0.8 | V |
| Logic-high input voltage | $V_{IN\_HIGH}$ | | 1.5 | | | V |
| Logic-low output voltage (7) | $V_{OUT\_LOW}$ | $I_{LOAD}$ = 3mA | | | 0.4 | V |
| SCL clock frequency (7) | $f_{SCL}$ | | 10 | | 1000 | kHz |
| Bus free time (7) | $t_{BUF\_FREE}$ | Between stop and start conditions | 0.5 | | | μs |
| Holding time after start/ repeated start condition (7) | $t_{HOLD\_START}$ | After this period, the first clock is generated | 0.26 | | | μs |
| Repeated start condition set-up time (7) | $t_{SU\_START}$ | | 0.26 | | | μs |
| Stop condition set-up time (7) | $t_{SU\_STOP}$ | | 0.26 | | | μs |
| Data hold time (7) | $t_{HOLD\_DATA}$ | | 0 | | | ns |
| Data set-up time (7) | $t_{SU\_DATA}$ | | 50 | | | ns |
| Clock low timeout (7) | $t_{TIMEOUT}$ | | 25 | | 35 | ms |
| Clock low time (7) | $t_{LOW}$ | | 0.5 | | | μs |
| Clock high time (7) | $t_{HIGH}$ | | 0.26 | | | μs |
| Clock/data fall time (7) | $t_{FALL}$ | | | | 120 | ns |
| Clock/data rise time (7) | $t_{RISE}$ | | | | 120 | ns |

**Note:**

7) Guaranteed by characterization. Not tested in production.

# I²C INTERFACE TIMING DIAGRAM




S = Start Condition
Sr = Repeated Start Condition
P = Stop Condition

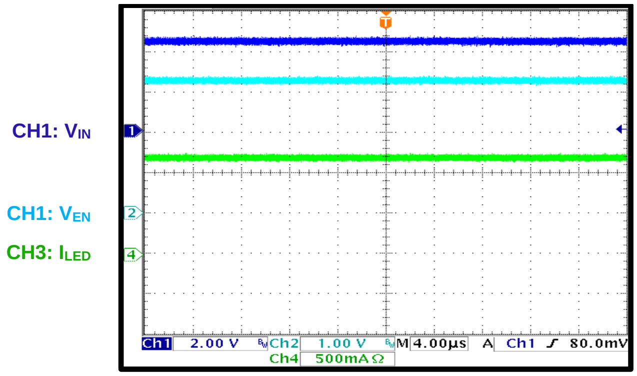
**Figure 4: I²C Interface Timing Diagram**

## TYPICAL PERFORMANCE CHARACTERISTICS

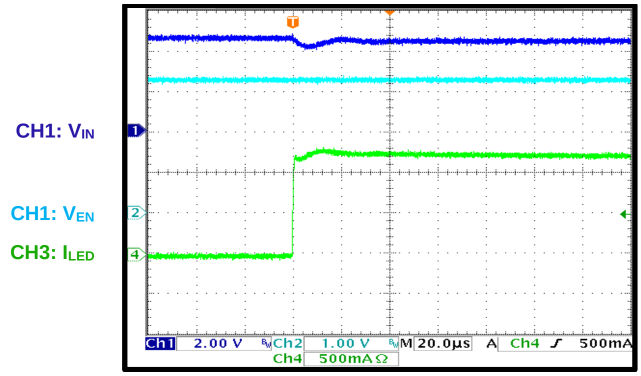
**$V_{IN}$ = 4.5V, $I_{LED}$ = 320mA per string, LED = 4P1S, $T_A$ = 25°C, unless otherwise noted.**

**Steady State**

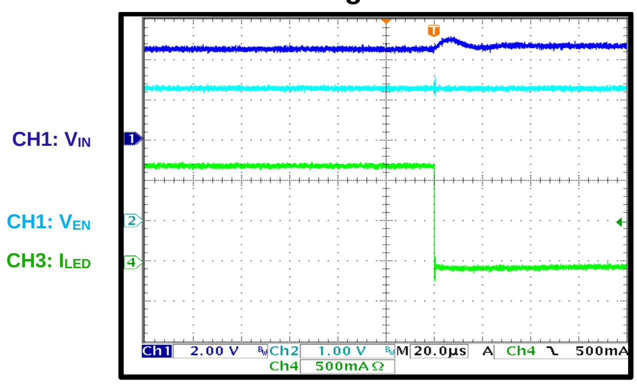
$V_{IN}$ = 4.5V, 4P1S, 320mA/string




**Start-Up through the EN Bit**

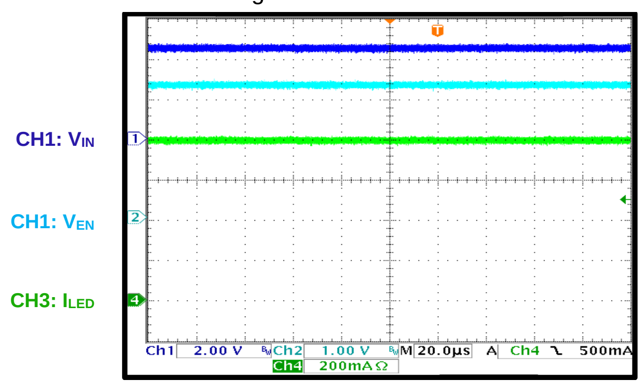



**Shutdown through the EN Bit**



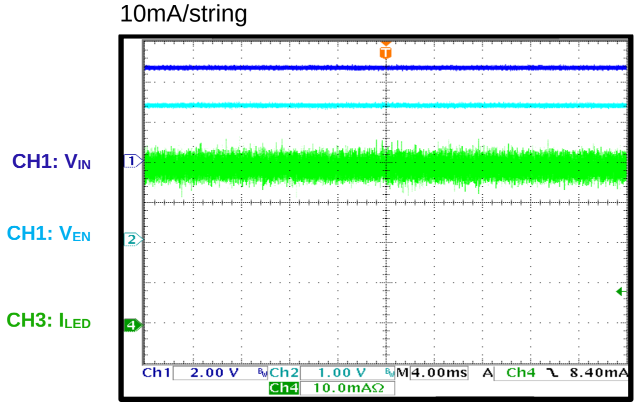

**Analog Dimming**

200mA/string



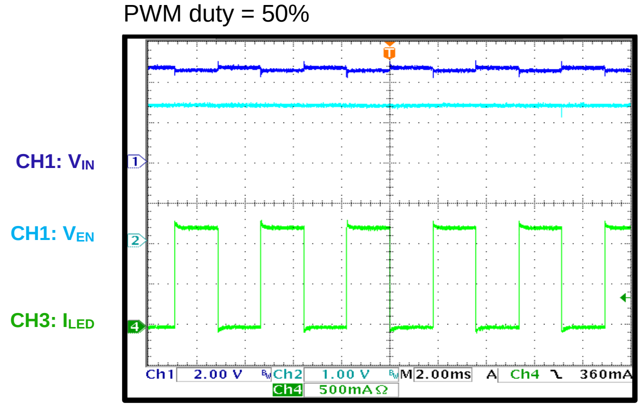

**Analog Dimming**

10mA/string




**PWM Dimming**

PWM duty = 50%

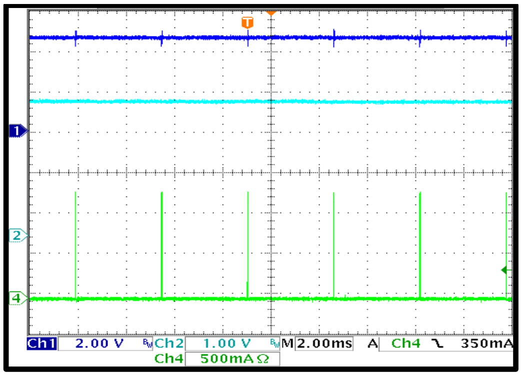


## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

**$V_{IN}$ = 4.5V, $I_{LED}$ = 320mA per string, LED = 4P1S, $T_A$ = 25°C, unless otherwise noted.**

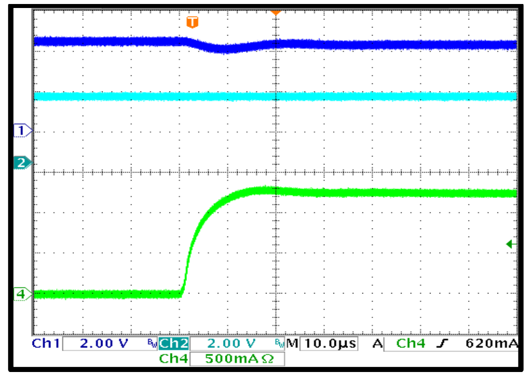
### PWM Dimming

PWM duty = 0.5%



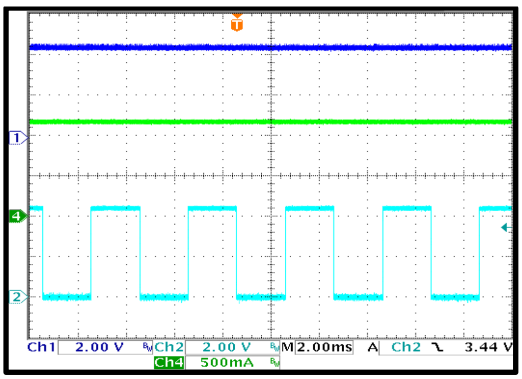

### Slew Rate

PWM dimming, slew rate = 5μs



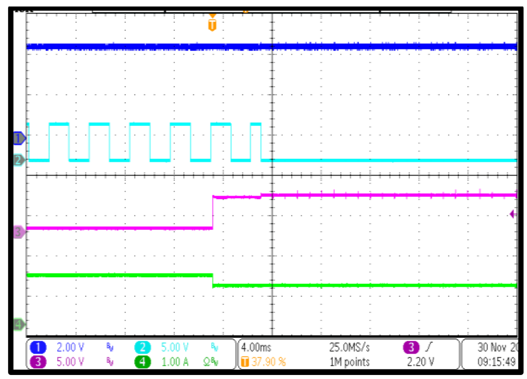

### Refresh Function

$f_{PWM}$ = 250Hz, RFRSH[9:0] = 0x1FF



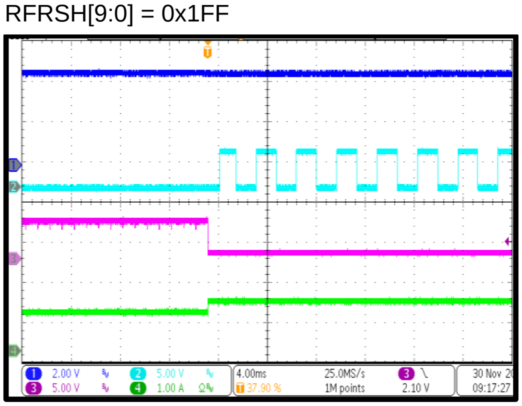

### Short LEDx Entry

RFSH/FLT fault enabled, $f_{PWM}$ = 330Hz, RFRSH[9:0] = 0x1FF



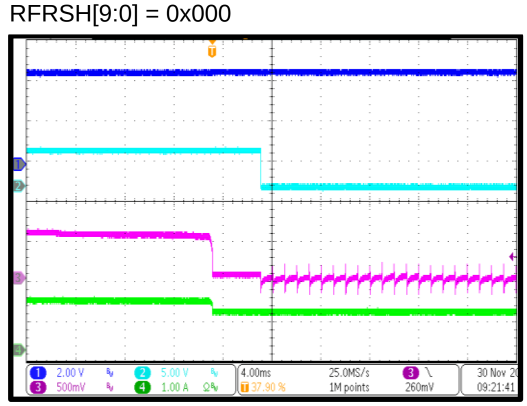

### Short LEDx Recovery

RFSH/FLT fault enabled, $f_{PWM}$ = 330Hz, RFRSH[9:0] = 0x1FF




### Open LEDx Entry

RFSH/FLT fault enabled, $f_{PWM}$ = 250Hz, RFRSH[9:0] = 0x000



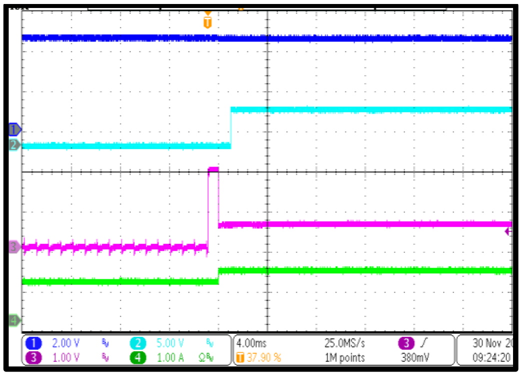
## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

**$V_{IN}$ = 4.5V, $I_{LED}$ = 320mA per string, LED = 4P1S, $T_A$ = 25°C, unless otherwise noted.**

**Open LEDx Recovery**

RFSH/FLT fault enabled, $f_{PWM}$ = 250Hz,
RFRSH[9:0] = 0x000

CH1: $V_{IN}$
CH2: RFSH/FLT
CH3: $V_{LED1}$
CH4: $I_{LED}$



## FUNCTIONAL BLOCK DIAGRAM

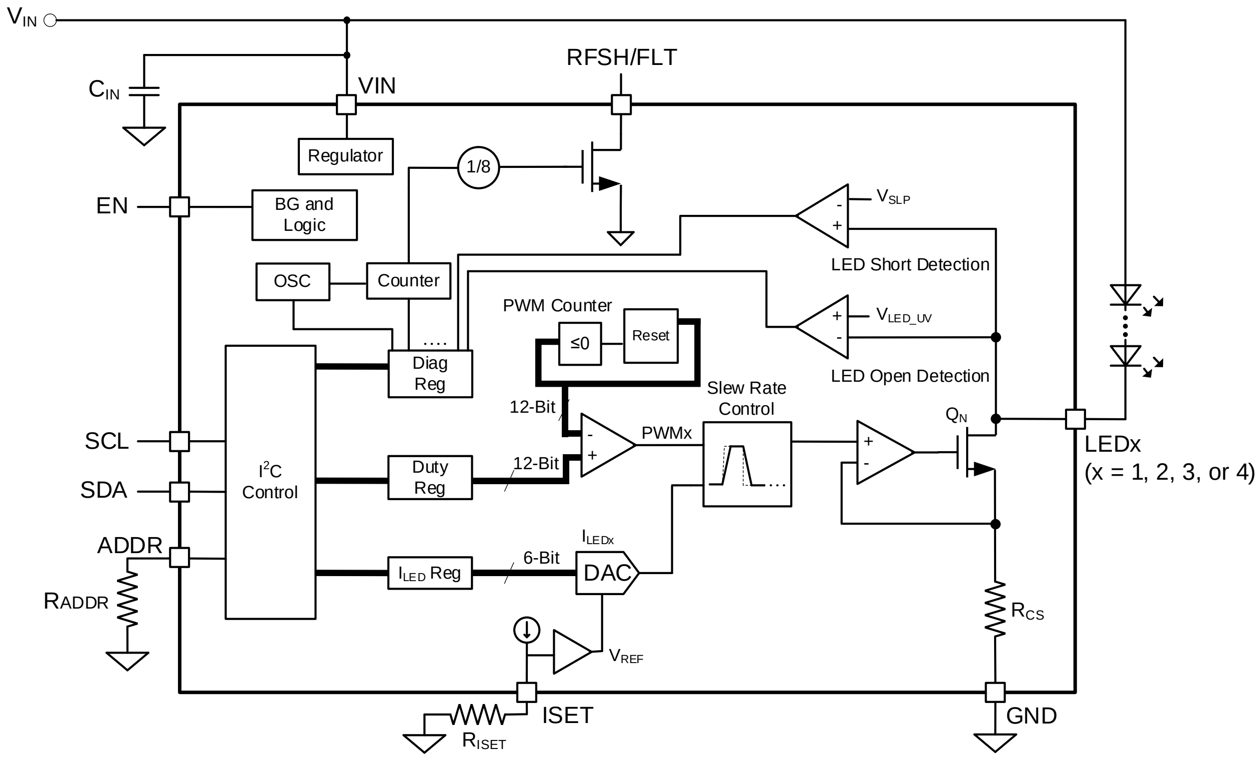



**Figure 5: Functional Block Diagram**

# OPERATION

The MPQ3323B applies 4 internal current sources in each LED string terminal. The LED current ($I_{LED}$) of all channels is set via an external current-setting resistor, with a maximum current up to 320mA.

### Enable (EN) and Start-Up

Once the input voltage ($V_{IN}$) exceeds its under-voltage lockout (UVLO) rising threshold ($V_{IN\_UVLO\_RISING}$) and the EN pin's voltage ($V_{EN}$) exceeds its rising threshold ($V_{EN\_RISING}$), the system starts up.

### Channel Selection

The channels can be disabled by pulling the corresponding CHxEN bit (where x = 1, 2, 3, or 4) low.

### Dimming

Each channel includes a separate 6-bit analog dimming register and 12-bit pulse-width modulation (PWM) dimming register. The MPQ3323B can support analog dimming and PWM dimming for each channel.

In analog dimming, the $I_{LED}$ amplitude changes when the analog dimming register changes. Change the code in ICHx (x = 1, 2, 3, or 4) to apply analog dimming for the corresponding channel. $I_{LED}$ can be estimated with Equation (1):

$$I_{LED} = \frac{ICHx}{63} \times I_{SET} \quad (1)$$

Where ICHx is the analog dimming for channel x (where x = 1, 2, 3, or 4). If ICHx is set to 0, then the corresponding $I_{LED}$ is 0A.

In PWM dimming, $I_{LED}$ is a PWM waveform, the $I_{LED}$ amplitude remains the same, and the $I_{LED}$ duty varies with the PWM dimming register.

The PWM dimming duty ($D_{PWM}$) is set by the PWMx (x = 1, 2, 3, or 4) register. $D_{PWM}$ can be calculated with Equation (2):

$$D_{PWM} = \frac{PWMx}{4095} \quad (2)$$

Where PWMx is the $D_{PWM}$ code for channel x (where x = 1, 2, 3, or 4).

The duty changes only when the PWM duty register's 8 most significant bits (MSB) are written. If PWMx is set to 0, then the corresponding $I_{LED}$ is 0A.

The PWM dimming frequency ($f_{PWM}$) can be selected via register FPWM[1:0]. Table 1 shows the FPWM[1:0] register settings for the different PWM frequencies.

**Table 1: PWM Frequency Setting**

| FPWM[1:0] | $f_{PWM}$ |
|---|---|
| 00 | 220Hz |
| 01 | 250Hz (default) |
| 10 | 280Hz |
| 11 | 330Hz |

To avoid glitches during normal operation, follow the steps below:

1. Change the FPWM[1:0] value only when the EN bit is set 0.
2. Write the FPWM register, then resume writing to the other registers after a 10µs delay.

### Phase Shift

The channel-by-channel phase shift function is enabled by setting the PS_EN bit high.

When the phase shift is enabled, the rising edge of each channel occurs 160µs after the previous channel. This means that the rising edge of the channel x + 1 (where x = 1, 2, or 3) $I_{LED}$ occurs after the rising edge of channel x's $I_{LED}$.

### Synchronized Output for the LCD Refresh Frequency

The fault indication function can be enabled by the FLTEN bit.

If FLTEN = 0, the fault indication function is disabled and the RFSH/FLT pin maintains the output refresh signal, even when a protection is triggered.

If FLTEN = 1, the fault indication function is enabled and RFSH/FLT is pulled low when a fault occurs.

Table 2 shows RFSH/FLT's output status.

**Table 2: RFSH/FLT Pin Output Status**

| FLTEN | FRFSH[9:0] = 0x000 (default) | | FRFSH[9:0] = 0x001 to 0x3FF | |
|---|---|---|---|---|
| | No Fault | Fault | No Fault | Fault |
| 1 | Pulled high externally | Low | Rectangular signal | Low |
| 0 | Pulled high externally | | Rectangular signal | |

The refresh signal frequency ($f_{REFRESH}$) is set by FRFSH[9:0]. If FRFSH[9:0] = 0x000, then RFSH/FLT outputs high. If FRFSH[9:0] = 0x001~0x3FF, then RFSH/FLT outputs a rectangular signal. $f_{REFRESH}$ can be calculated with Equation (3):

$$f_{REFRESH} = \frac{127500}{FRFSH} \times \frac{f_{PWM}}{250} \ (Hz) \tag{3}$$

Where FRFSH is the FRFSH[9:0] value (>0), and $f_{PWM}$ is set by register FPWM[1:0] to 220Hz, 250Hz, 280Hz, or 330Hz.

Note that all values in Equation (3) are decimal-based and $f_{REFRESH}$ does not change until the 8MSB are written.

If FRFSH[9:0] is written to 0x000, then the read back value is 0x1A9 to avoid a zero denominator in the internal calculation (see Equation 3).

The internal oscillator is divided by 8. As the clock refreshes the frequency generation, the FRFSH[9:0] register sets the counter number (see Figure 6).

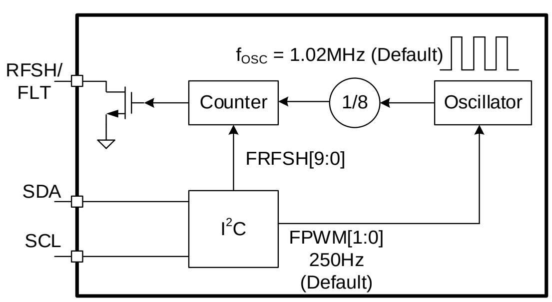



**Figure 6: Refresh Frequency Generation**

## LED Current Slew Rate Control

To reduce EMI, change the $I_{LED}$ rising and falling slew rate in PWM dimming. The $I_{LED}$ rising and falling slew rate is controlled by the SLEW[1:0] register. Table 3 shows the SLEW[1:0] register settings for the different slew rates.

**Table 3: Slew Rate Setting**

| SLEW[1:0] | Slew Rate |
|---|---|
| 00 | No slew rate |
| 01 | 5µs |
| 10 | 10µs |
| 11 | 20µs |

## Protections

The MPQ3323B employs UVLO protection, LED short protection, LED open protection, and thermal shutdown.

The RFSH/FLT pin is an active-low, open-drain output that is pulled high to an external voltage source. If a fault occurs, the corresponding fault bit is set and RFSH/FLT is pulled low.

For LED open and short protection, hiccup mode or latch-off mode can be selected via the LATCH bit via the I²C.

If LATCH = 1, the MPQ3323B initiates latch-off mode once a fault occurs. The fault channel remains off until either VIN or EN turns off and resets. After the fault bit is read, FRSH/FLT is pulled high and the fault bit sets. If the fault bit is read again, then the fault bit resets.

If LATCH = 0, the MPQ3323B enters hiccup mode, during which the fault channel tries to conduct for 32µs every 1ms to detect whether the fault has been cleared. Once the fault is removed, FRSH/FLT is pulled high automatically and the fault bit resets when it is read.

### *$V_{IN}$ Under-Voltage Lockout (UVLO) Protection*

If $V_{IN}$ drops to the $V_{IN}$ UVLO threshold, then the IC shuts down and the I²C registers are reset.

### *LED Open Protection*

The LEDx (x = 1, 2, 3, or 4) voltage ($V_{LEDx}$) drops when an LED is open. If $V_{LEDx}$ drops below the protection threshold (about 100mV) for 4ms, then LED open protection is triggered. In this scenario, the fault channel turns off, the corresponding open fault bit (CHxO, where x = 1, 2, 3, or 4) is set, and RFSH/FLT is pulled low.

### *LED Short Protection*

If an LED short occurs, and $V_{LEDx}$ (x = 1, 2, 3, or 4) exceeds the voltage set by STH[1:0] for 4ms, then LED short protection is triggered. The short channel turns off, the corresponding fault bit (CHxS, where x = 1, 2, 3, or 4) is set, and RFSH/FLT is pulled low.

The LED short protection threshold ($V_{SLP}$) can be configured via the STH[1:0] register. Table 4 shows the STH[1:0] register setting for different LED short protection thresholds.

**Table 4: LED SCP Threshold Setting**

| STH[1:0] | $V_{SLP}$ |
|---|---|
| 00 | 2V |
| 01 | 3V |
| 10 | 4V |
| 11 | 5V |

### Over Temperature Protection (OTP)

If the IC temperature exceeds 170°C, then over-temperature protection (OTP) is triggered, all channels turn off, RFSH/FLT is pulled low, and FT_OTP is set. Once the temperature drops to about 150°C, all channels turn on again and the IC resumes normal operation.

# I²C INTERFACE

## I²C Chip Address

The device address is 0x30~0x39, which can be configured via the ADDR resistor ($R_{ADDR}$). The internal current source flows to $R_{ADDR}$, and the ADDR voltage ($V_{ADDR}$) determines the I²C address. Ten different addresses can be configured via $R_{ADDR}$.

Table 5 shows the various resistor ratio ($R_{ADDR}$ / $R_{ISET}$) configurations to set the I²C address.

**Table 5: I²C Address Setting**

| $R_{ADDR}$, $R_{ISET}$ | I²C Address (A3, A2, A1, A0) |
|---|---|
| <0.05 | 0000 |
| >0.05, <0.15 | 0001 |
| >0.15, <0.25 | 0010 |
| >0.25, <0.35 | 0011 |
| >0.35, <0.45 | 0100 |
| >0.45, <0.55 | 0101 |
| >0.55, <0.65 | 0110 |
| >0.65, <0.75 | 0111 |
| >0.75, <0.85 | 1000 |
| >0.85, <0.95 | 1001 |

At start-up, the IC checks the I²C address first. This address remains the same during operation until the IC's power is reset.

After a start (S) condition, the I²C-compatible master sends a 7-bit address, followed by an eighth data direction bit (where 1 = read and 0 = write). The eighth bit indicates the register address to/from which the data is written/read (see Figure 7).

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0 | 1 | 1 | A3 | A2 | A1 | A0 | R/W |

**Figure 7: The I²C-Compatible Device Address**

To avoid glitches during normal operation, follow the steps below:

1. Change the FPWM[1:0] value only when the EN bit is set to 0.
2. Write the FPWM[1:0] register, then resume writing to the other registers after a 10µs delay.

# I2C REGISTER MAP

| Name | R/W | Add | Default | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| ILED_FRE | R/W | 00h | 01 | RESERVED | | | | | | FPWM[1:0] | |
| DEV_CON | R/W | 01h | 91 | FLTEN | LATCH | STH[1:0] | | SLEW[1:0] | | PS_EN | EN |
| REFRESH_1 | R/W | 02h | 01 | RESERVED | | | | | FT_OTP | FRFSH[1:0] | |
| REFRESH_2 | R/W | 03h | 6A | FRFSH[9:2] | | | | | | | |
| CHN_EN1 | R/W | 04h | FF | CH4EN[3:0] | | | | CH3EN[3:0] | | | |
| CHN_EN2 | R/W | 05h | FF | CH2EN[3:0] | | | | CH1EN[3:0] | | | |
| FAU_OP1 | R | 06h | 00 | RESERVED | | | CH4O | RESERVED | | | CH3O |
| FAU_OP2 | R | 07h | 00 | RESERVED | | | CH2O | RESERVED | | | CH1O |
| FAU_SH1 | R | 08h | 00 | RESERVED | | | CH4S | RESERVED | | | CH3S |
| FAU_SH2 | R | 09h | 00 | RESERVED | | | CH2S | RESERVED | | | CH1S |
| ILED_CH1 | R/W | 0Ah | 3F | RESERVED | | ICH1[5:0] | | | | | |
| DPWM_CH1_1 | R/W | 0Bh | 0F | RESERVED | | | | PWM1[3:0] | | | |
| DPWM_<br>CH1_2 | R/W | 0Ch | FF | PWM1[11:4] | | | | | | | |
| ILED_CH1 | R/W | 0Dh | 3F | RESERVED | | ICH1[5:0] | | | | | |
| DPWM_CH1_1 | R/W | 0Eh | 0F | RESERVED | | | | PWM1[3:0] | | | |
| DPWM_<br>CH1_2 | R/W | 0Fh | FF | PWM1[11:4] | | | | | | | |
| ILED_CH1 | R/W | 10h | 3F | RESERVED | | ICH1[5:0] | | | | | |
| DPWM_CH1_1 | R/W | 11h | 0F | RESERVED | | | | PWM1[3:0] | | | |
| DPWM_CH1_2 | R/W | 12h | FF | PWM1[11:4] | | | | | | | |
| ILED_CH1 | R/W | 13h | 3F | RESERVED | | ICH1[5:0] | | | | | |
| DPWM_CH1_1 | R/W | 14h | 0F | RESERVED | | | | PWM1[3:0] | | | |
| DPWM_CH1_2 | R/W | 15h | FF | PWM1[11:4] | | | | | | | |
| ILED_CH2 | R/W | 16h | 3F | RESERVED | | ICH2[5:0] | | | | | |
| DPWM_CH2_1 | R/W | 17h | 0F | RESERVED | | | | PWM2[3:0] | | | |
| DPWM_CH2_2 | R/W | 18h | FF | PWM2[11:4] | | | | | | | |
| ILED_CH2 | R/W | 19h | 3F | RESERVED | | ICH2[5:0] | | | | | |
| DPWM_CH2_1 | R/W | 1Ah | 0F | RESERVED | | | | PWM2[3:0] | | | |
| DPWM_CH2_2 | R/W | 1Bh | FF | PWM2[11:4] | | | | | | | |
| ILED_CH2 | R/W | 1Ch | 3F | RESERVED | | ICH2[5:0] | | | | | |
| DPWM_CH2_1 | R/W | 1Dh | 0F | RESERVED | | | | PWM2[3:0] | | | |
| DPWM_CH2_2 | R/W | 1Eh | FF | PWM2[11:4] | | | | | | | |
| ILED_CH2 | R/W | 1Fh | 3F | RESERVED | | ICH2[5:0] | | | | | |
| DPWM_CH2_1 | R/W | 20h | 0F | RESERVED | | | | PWM2[3:0] | | | |
| DPWM_CH2_2 | R/W | 21h | FF | PWM2[11:4] | | | | | | | |
| ILED_CH3 | R/W | 22h | 3F | RESERVED | | ICH3[5:0] | | | | | |
| DPWM_CH3_1 | R/W | 23h | 0F | RESERVED | | | | PWM3[3:0] | | | |
| DPWM_CH3_2 | R/W | 24h | FF | PWM3[11:4] | | | | | | | |
| ILED_CH3 | R/W | 25h | 3F | RESERVED | | ICH3[5:0] | | | | | |
| DPWM_CH3_1 | R/W | 26h | 0F | RESERVED | | | | PWM3[3:0] | | | |
| DPWM_CH3_2 | R/W | 27h | FF | PWM3[11:4] | | | | | | | |
| ILED_CH3 | R/W | 28h | 3F | RESERVED | | ICH3[5:0] | | | | | |
| DPWM_CH3_1 | R/W | 29h | 0F | RESERVED | | | | PWM3[3:0] | | | |
| DPWM_CH3_2 | R/W | 2Ah | FF | PWM3[11:4] | | | | | | | |
| ILED_CH3 | R/W | 2Bh | 3F | RESERVED | | ICH3[5:0] | | | | | |
| DPWM_CH3_1 | R/W | 2Ch | 0F | RESERVED | | | | | PWM3[3:0] | | |
| DPWM_CH3_2 | R/W | 2Dh | FF | PWM3[11:4] | | | | | | | |
| ILED_CH4 | R/W | 2Eh | 3F | RESERVED | | ICH4[5:0] | | | | | |
| DPWM_CH4_1 | R/W | 2Fh | 0F | RESERVED | | | | | PWM4[3:0] | | |
| DPWM_CH4_2 | R/W | 30h | FF | PWM4[11:4] | | | | | | | |
| ILED_CH4 | R/W | 31h | 3F | RESERVED | | ICH4[5:0] | | | | | |
| DPWM_CH4_1 | R/W | 32h | 0F | RESERVED | | | | | PWM4[3:0] | | |
| DPWM_CH4_2 | R/W | 33h | FF | PWM4[11:4] | | | | | | | |
| ILED_CH4 | R/W | 34h | 3F | RESERVED | | ICH4[5:0] | | | | | |
| DPWM_CH4_1 | R/W | 35h | 0F | RESERVED | | | | | PWM4[3:0] | | |

## I²C REGISTER MAP *(continued)*

<table>
<tr><th>Name</th><th>R/W</th><th>Add</th><th>Default</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td>DPWM_CH4_2</td><td>R/W</td><td>36h</td><td>FF</td><td colspan="8">PWM4[11:4]</td></tr>
<tr><td>ILED_CH4</td><td>R/W</td><td>37h</td><td>3F</td><td colspan="2">RESERVED</td><td colspan="6">ICH4[5:0]</td></tr>
<tr><td>DPWM_CH4_1</td><td>R/W</td><td>38h</td><td>0F</td><td colspan="5">RESERVED</td><td colspan="3">PWM4[3:0]</td></tr>
<tr><td>DPWM_CH4_2</td><td>R/W</td><td>39h</td><td>FF</td><td colspan="8">PWM4[11:4]</td></tr>
</table>

# I2C REGISTER DESCRIPTION

## ILED_FRE (00h)

The ILED_FRE command sets the LED current ($I_{LED}$) frequency.

| Bits | Name | Access | Default | Description |
|---|---|---|---|---|
| 7:2 | RESERVED | R | N/A | Reserved. |
| 1:0 | FPWM[1:0] | R/W | 2'b 01 | Sets the pulse-width modulation (PWM) dimming frequency.<br>00: 220Hz<br>01: 250Hz<br>10: 280Hz<br>11: 330Hz<br>To avoid glitches during operation, follow the steps below:<br>• Change the FPWM[1:0] value only when the EN bit is set to 0.<br>• Write the FPWM[1:0] register, then resume writing to the other registers after a 10µs delay. |

## DEV_CON (01h)

The DEV_CON command controls the device.

| Bits | Name | Access | Default | Description |
|---|---|---|---|---|
| 7 | FLTEN | R/W | 1'b1 | Enables the RFSH/FLT fault indicator.<br>0: Disabled. RFSH/FLT refreshes the signal output<br>1: Enabled. RFSH/FLT indicates if a fault has occurred |
| 6 | LATCH | R/W | 1'b0 | Enables latch-off mode.<br>0: Disabled. Hiccup mode enabled if a fault occurs<br>1: Enabled. Latch-off mode enabled if a fault occurs |
| 5:4 | STH[1:0] | R/W | 2'b 01 | Sets the LED short protection threshold ($V_{SLP}$).<br>00: 2V<br>01: 3V<br>10: 4V<br>11: 5V |
| 3:2 | SLEW[1:0] | R/W | 2'b 00 | Sets the LED current ($I_{LED}$) slew rate.<br>00: No slew rate<br>01: 5µs<br>10:10µs<br>11: 20µs |
| 1 | PS_EN | R/W | 1'b0 | Enables the phase shift.<br>0: Disabled<br>1: Enabled. The rising edge of channel x + 1 (where x = 1, 2, or 3) $I_{LED}$ occurs 160µs after the rising edge of channel x's $I_{LED}$ |
| 0 | EN | R/W | 1'b1 | Enables the IC.<br>0: Disabled<br>1: Enabled |

### REFRESH_1 (02h)

The REFRESH_1 command sets the RFSH/FLT refresh frequency ($f_{REFRESH}$) (2LSB).

| Bits | Name | Access | Default | Description |
|---|---|---|---|---|
| 7:3 | RESERVED | R | - | Reserved. |
| 2 | FT_OTP | R | 1'b0 | Indicates whether an over-temperature (OT) fault has occurred.<br>0: An OT fault has not occurred<br>1: An OT fault has occurred |
| 1:0 | FRFSH[1:0] | R/W | 2'b 01 | Sets the 2 least significant bits (LSB) of $f_{REFRESH}$.<br>FRFSH[9:0] = 0x000, outputs a high voltage<br>FRFSH[9:0] > 0, $f_{REFRESH}$ can be calculated with the following equation:<br>$f_{REFRESH} = \frac{127500}{FRFSH} \times \frac{f_{PWM}}{250} (Hz)$<br>Note that all of the numbers in the equation have a decimal base. $f_{REFRESH}$ does not change until the 8MSB is written. The default FRFSH[1:0] = 00, but read back is 01. |

### REFRESH_2 (03h)

The REFRESH_2 command sets the RFSH/FLT $f_{REFRESH}$ (8MSB).

| Bits | Name | Access | Default | Description |
|---|---|---|---|---|
| 7:3 | FRFSH[9:2] | R/W | 8'b 01101010 | Sets the 8MSB of $f_{REFRESH}$.<br>FRFSH[9:0] = 0x000, outputs a high voltage<br>FRFSH[9:0] > 0, $f_{REFRESH}$ can be calculated with the following equation:<br>$f_{REFRESH} = \frac{127500}{FRFSH} \times \frac{f_{PWM}}{250} (Hz)$<br>Note that all of the numbers in the equation have a decimal base. $f_{REFRESH}$ does not change until the 8MSB is written. The default FRFSH[9:2] = 0x00, but read back is 6A. |

### CHN_EN1 (04h)

The CHN_EN1 command sets the channel 3~4 enable bits.

| Bits | Name | Access | Default | Description |
|---|---|---|---|---|
| 7:4 | CH4EN | R/W | 4'b1111 | Enables channel 4.<br>0000: Disabled<br>1111: Enabled |
| 3:0 | CH3EN | R/W | 4'b1111 | Enables channel 3.<br>0000: Disabled<br>1111: Enabled |

### CHN_EN2 (05h)

The CHN_EN2 command sets the channel 1~2 enable bits.

| Bits | Name | Access | Default | Description |
|---|---|---|---|---|
| 7:4 | CH2EN | R/W | 4'b1111 | Enables channel 2.<br>0000: Disabled<br>1111: Enabled |
| 3:0 | CH1EN | R/W | 4'b1111 | Enables channel 1.<br>0000: Disabled<br>1111: Enabled |

### FAU_OP1 (06h)

The FAU_OP1 command reads the channel 3~4 open fault bits.

| Bits | Name | Access | Default | Description |
|---|---|---|---|---|
| 7:5 | RESERVED | R | - | Reserved. |
| 4 | CH4O | R | 1'b0 | Channel 4 open protection fault flag.<br>0: No fault<br>1: Fault |
| 3:1 | RESERVED | R | - | Reserved. |
| 0 | CH3O | R | 1'b0 | Channel 3 open protection fault flag.<br>0: No fault<br>1: Fault |

### FAU_OP2 (07h)

The FAU_OP2 command reads the channel 1~2 open fault bits.

| Bits | Name | Access | Default | Description |
|---|---|---|---|---|
| 7:5 | RESERVED | R | - | Reserved. |
| 4 | CH2O | R | 1'b0 | Channel 2 open protection fault flag.<br>0: No fault<br>1: Fault |
| 3:1 | RESERVED | R | - | Reserved. |
| 0 | CH1O | R | 1'b0 | Channel 1 open protection fault flag.<br>0: No fault<br>1: Fault |

### FAU_SH1 (08h)

The FAU_SH1 command reads the channel 3~4 short fault bits.

| Bits | Name | Access | Default | Description |
|---|---|---|---|---|
| 7:5 | RESERVED | R | - | Reserved. |
| 4 | CH4S | R | 1'b0 | Channel 4 short protection fault flag.<br>0: No fault<br>1: Fault |
| 3:1 | RESERVED | R | - | Reserved. |

| | | | | |
|---|---|---|---|---|
| 0 | CH3S | R | 1'b0 | Channel 3 short protection fault flag.<br>0: No fault<br>1: Fault |

### FAU_SH2 (09h)

The FAU_SH2 command reads the channel 1~2 short fault bits.

| Bits | Name | Access | Default | Description |
|---|---|---|---|---|
| 7:5 | RESERVED | R | - | Reserved. |
| 4 | CH2S | R | 1'b0 | Channel 2 short protection fault flag.<br>0: No fault<br>1: Fault |
| 3:1 | RESERVED | R | - | Reserved. |
| 0 | CH1S | R | 1'b0 | Channel 1 short protection fault flag.<br>0: No fault<br>1: Fault |

### ILED_CH1 (0Ah, 0Dh, 10h, and 13h)

The ILED_CH1 command sets the channel 1 $I_{LED}$.

| Bits | Name | Access | Default | Description |
|---|---|---|---|---|
| 7:6 | RESERVED | R | - | Reserved. |
| 5:0 | ICH1[5:0] | R/W | 6'b 111111 | Sets the channel 1 $I_{LED}$ for analog dimming, which can be calculated with the following equation:<br>$I_{LED}=\frac{Code}{63}\times I_{SET}$ |

### DPWM_CH1_1 (0Bh, 0Eh, 11h, and 14h)

The DPWM_CH1_1 command sets the 4LSB for the channel 1 $I_{LED}$ PWM dimming duty ($D_{PWM}$).

| Bits | Name | Access | Default | Description |
|---|---|---|---|---|
| 7:4 | RESERVED | R | - | Reserved. |
| 3:0 | PWM1[3:0] | R/W | 4'b 1111 | Sets the 4LSB for the channel 1 $I_{LED}$ $D_{PWM}$. $D_{PWM}$ only changes when the 8MSB are written. |

### DPWM_CH1_2 (0Ch, 0Fh, 12h, and 15h)

The DPWM_CH1_2 command sets the 8MSB for the channel 1 $I_{LED}$ $D_{PWM}$.

| Bits | Name | Access | Default | Description |
|---|---|---|---|---|
| 7:0 | PWM1[11:4] | R/W | 8'b 11111111 | Sets the 8MSB for the channel 1 $I_{LED}$ $D_{PWM}$. $D_{PWM}$ only changes when the 8MSB are written. |

### ILED_CH2 (16h, 19h, 1Ch, and 1Fh)

The ILED_CH2 command sets the channel 2 $I_{LED}$.

| Bits | Name | Access | Default | Description |
|---|---|---|---|---|
| 7:6 | RESERVED | R | - | Reserved. |
| 5:0 | ICH2[5:0] | R/W | 6'b 111111 | Sets the channel 2 $I_{LED}$ for analog dimming, which can be calculated with the following equation:<br>$I_{LED}=\frac{Code}{63}\times I_{SET}$ |

### DPWM_CH2_1 (17h, 1Ah, 1Dh, and 20h)

The DPWM_CH2_1 command sets the 4LSB for the channel 2 $I_{LED}$ $D_{PWM}$.

| Bits | Name | Access | Default | Description |
|---|---|---|---|---|
| 7:4 | RESERVED | R | - | Reserved. |
| 3:0 | PWM2[3:0] | R/W | 4'b 1111 | Sets the 4LSB for the channel 2 $I_{LED}$ $D_{PWM}$. $D_{PWM}$ only changes when the 8MSB are written. |

### DPWM_CH2_2 (18h, 1Bh, 1Eh, and 21h)

The DPWM_CH2_2 command sets the 8MSB for the channel 2 $I_{LED}$ $D_{PWM}$.

| Bits | Name | Access | Default | Description |
|---|---|---|---|---|
| 7:0 | PWM2[11:4] | R/W | 8'b 11111111 | Sets the 8MSB for the channel 2 $I_{LED}$ $D_{PWM}$. $D_{PWM}$ only changes when the 8MSB are written. |

### ILED_CH3 (22h, 25h, 28h, and 2Bh)

The ILED_CH3 command sets the channel 3 $I_{LED}$.

| Bits | Name | Access | Default | Description |
|---|---|---|---|---|
| 7:6 | RESERVED | R | - | Reserved. |
| 5:0 | ICH3[5:0] | R/W | 6'b 111111 | Sets the channel 3 $I_{LED}$ for analog dimming, which can be calculated with the following equation: $I_{LED}=\frac{Code}{63}\times I_{SET}$ |

### DPWM_CH3_1 (23h, 26h, 29h, and 2Ch)

The DPWM_CH3_1 command sets the 4LSB for the channel 3 $I_{LED}$ $D_{PWM}$.

| Bits | Name | Access | Default | Description |
|---|---|---|---|---|
| 7:4 | RESERVED | R | - | Reserved. |
| 3:0 | PWM3[3:0] | R/W | 4'b 1111 | Sets the 4LSB for the channel 3 $I_{LED}$ $D_{PWM}$. $D_{PWM}$ only changes when the 8MSB are written. |

### DPWM_CH3_2 (24h, 27h, 2Ah, and 2Dh)

The DPWM_CH3_2 command sets the 8MSB for the channel 3 $I_{LED}$ $D_{PWM}$.

| Bits | Name | Access | Default | Description |
|---|---|---|---|---|
| 7:0 | PWM3[11:4] | R/W | 8'b 11111111 | Sets the 8MSB for the channel 3 $I_{LED}$ $D_{PWM}$. $D_{PWM}$ only changes when the 8MSB are written. |

### ILED_CH4 (2Eh, 31h, 34h, and 37h)

The ILED_CH4 command sets channel 4 $I_{LED}$.

| Bits | Name | Access | Default | Description |
|---|---|---|---|---|
| 7:6 | RESERVED | R | - | Reserved. |
| 5:0 | ICH4[5:0] | R/W | 6'b 111111 | Sets the channel 4 $I_{LED}$ for analog dimming, which can be calculated with the following equation: $I_{LED}=\frac{Code}{63}\times I_{SET}$ |

### DPWM_CH4_1 (2Fh, 32h, 35h, and 38h)

The DPWM_CH4_1 command sets the 4LSB for the channel 4 $I_{LED}$ $D_{PWM}$.

| Bits | Name | Access | Default | Description |
|---|---|---|---|---|
| 7:4 | RESERVED | R | - | Reserved. |
| 3:0 | PWM4[3:0] | R/W | 4'b 1111 | Sets the 4LSB for the channel 4 $I_{LED}$ $D_{PWM}$. $D_{PWM}$ only changes when the 8MSB are written. |

### DPWM_CH4_2 (30h, 33h, 36h, 39h)

The DPWM_CH4_2 command sets the 8MSB for the channel 4 $I_{LED}$ $D_{PWM}$.

| Bits | Name | Access | Default | Description |
|---|---|---|---|---|
| 7:0 | PWM4[11:4] | R/W | 8'b 11111111 | Sets the 8MSB for the channel 4 $I_{LED}$ $D_{PWM}$. $D_{PWM}$ only changes when the 8MSB are written. |

# APPLICATION INFORMATION

## Setting the LED Current

Connect a resistor from the ISET pin to GND to set $I_{LED}$ for all four channels. $I_{LED}$ can be calculated with Equation (4):

$$I_{LED}(mA) = \frac{4800}{R_{ISET}(k\Omega)} \tag{4}$$

## PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For the best results, refer to Figure 8 and following the guidelines below:

1) Place the VIN capacitor close to the VIN pin.
2) Add multiple vias to the capacitor's GND.
3) Ensure that the traces from the LED anode to the LEDx pins are wide enough to support the set current (up to 320mA).

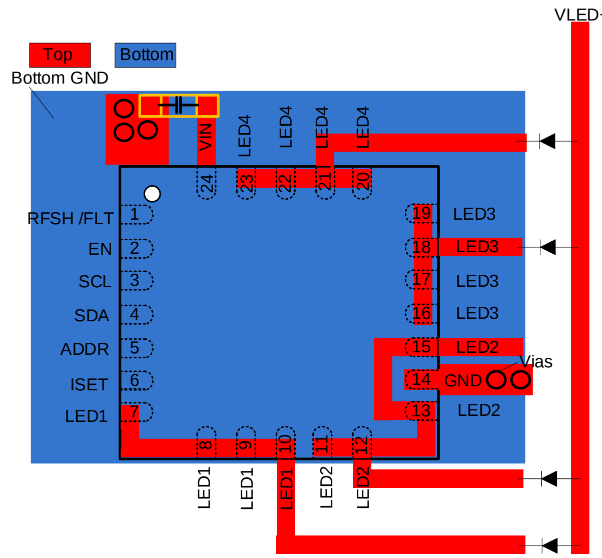



**Figure 8: Recommended PCB Layout**

## TYPICAL APPLICATION CIRCUITS

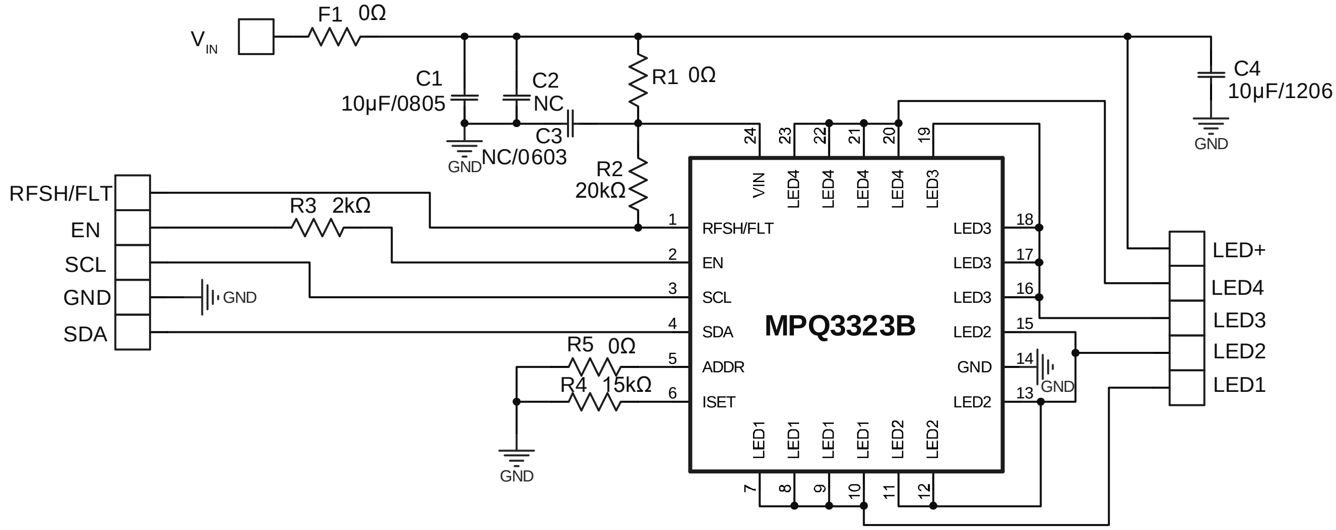



**Figure 9: Typical Application Circuit ($I_{LED}$ = 320mA/Channel)**

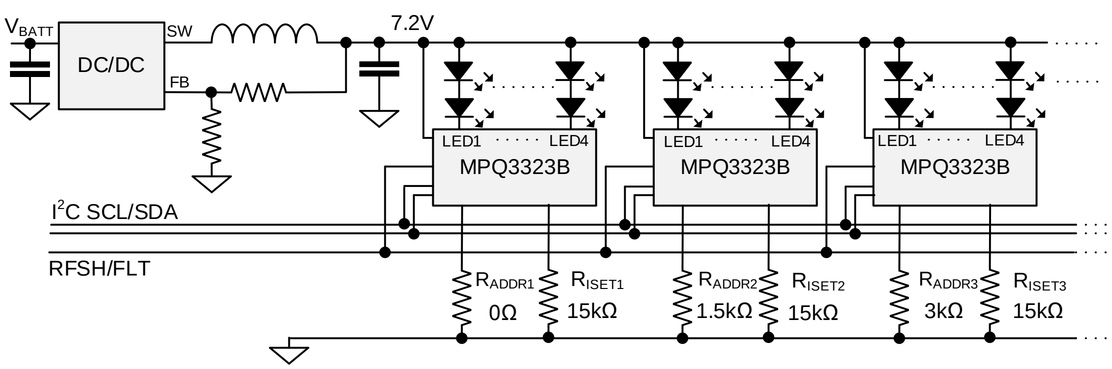
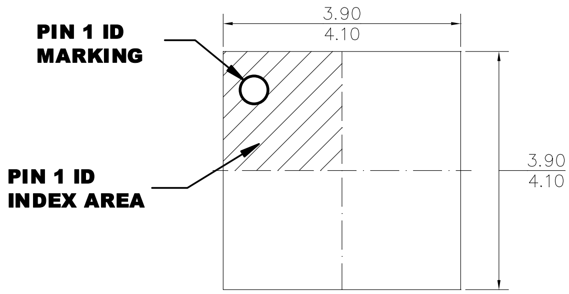


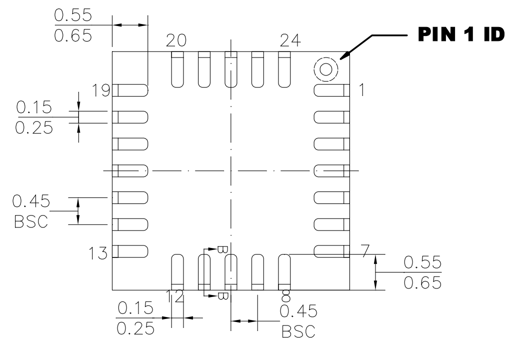

**Figure 10: Typical System Application Circuit (2 LED in Series, $I_{LED}$ = 320mA/Channel)**

# PACKAGE INFORMATION

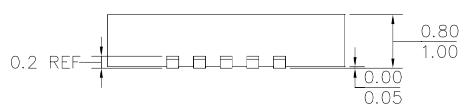
**QFN-24 (4mmx4mm)**
**Wettable Flank**



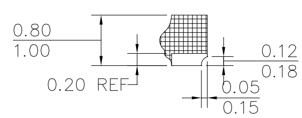

**TOP VIEW**



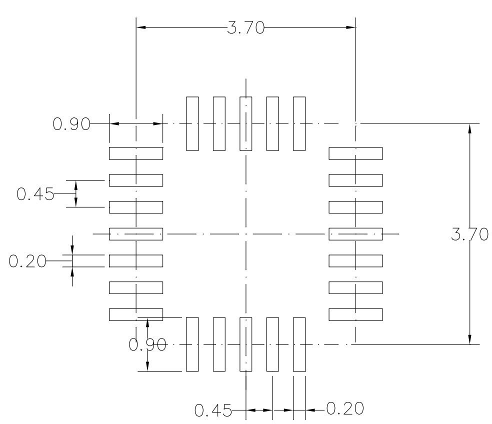

**BOTTOM VIEW**




**SIDE VIEW**




**SECTION B-B**

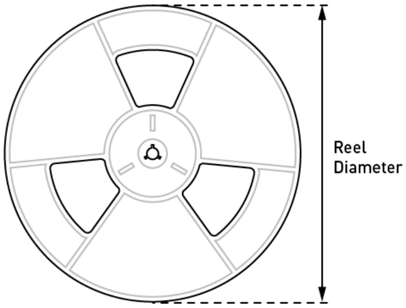


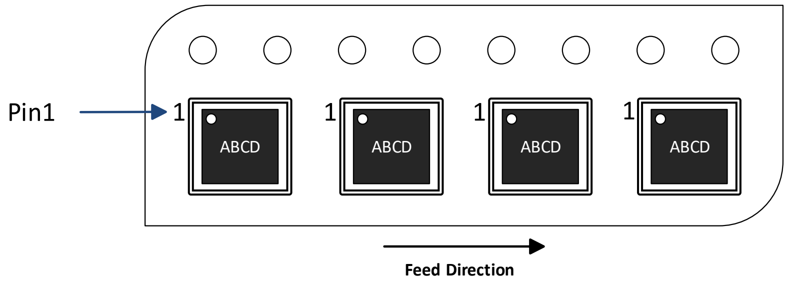

**RECOMMENDED LAND PATTERN**

**NOTE:**

1) THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

# CARRIER INFORMATION




| Part Number | Package Description | Quantity/ Reel | Quantity/ Tube | Quantity/ Tray | Reel Diameter | Carrier Tape Width | Carrier Tape Pitch |
|---|---|---|---|---|---|---|---|
| MPQ3323BGRE-AEC1-Z | QFN-24 (4mmx4mm) | 5000 | N/A | N/A | 13in | 12mm | 8mm |

# REVISION HISTORY

| Revision # | Revision Date | Description | Pages Updated |
|---|---|---|---|
| 1.0 | 4/13/2023 | Initial Release | - |