MPQ28261

21V, 3A, 500kHz Synchronous Step-Down Converter

The Future of Analog IC Technology

DESCRIPTION

The MPQ28261 is a synchronous, rectified, step-down, switch-mode converter with built-in 120mΩ high-side MOSFET and 20mΩ low-side MOSFET. It offers a very compact solution to achieve a continuous 3A output current over a wide input supply range, with excellent load and line regulation. Its synchronous mode operation increases its efficiency over its output current load range, and uses a fixed 500kHz switching frequency.

Current mode operation provides a fast transient response and improves loop stabilization. Full protection features include over-current protection and thermal shut down.

The MPQ28261 has an external SS pin to program the soft-start time and power-good signal output.

The MPQ28261 requires a minimal number of readily-available standard external components and is available in a space saving 3mmx4mm 14-pin QFN package.

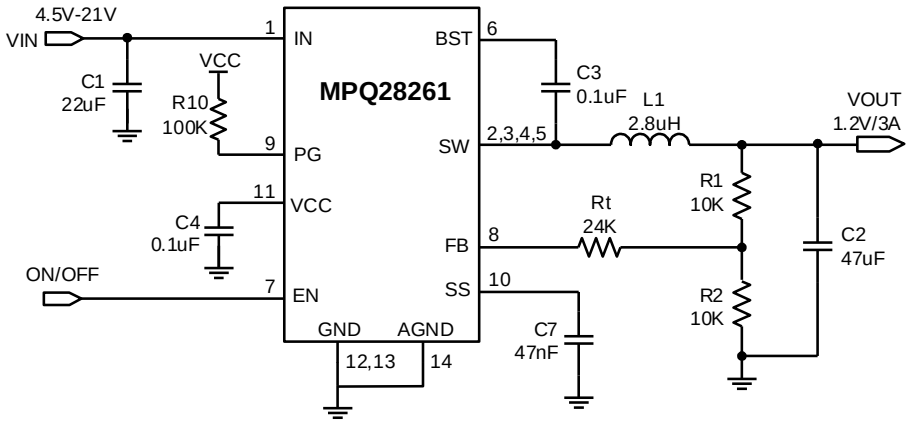
FEATURES

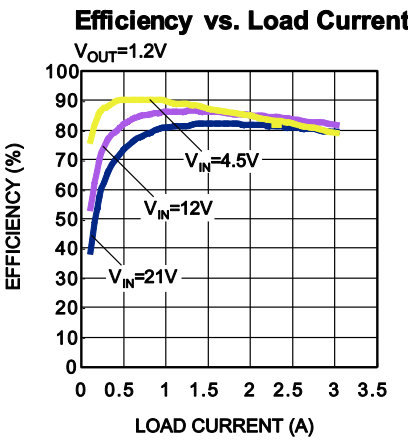
- Wide 4.5V-to-21V Operating Input Range
- 3A Maximum Continuous Output Current
- Integrated 120mΩ High-Side and 20mΩ Low-Side Power MOSFETs
- 1% Reference Voltage Accuracy
- Up to 85% Efficiency (for Drops of 12V to 1.2V)
- Fixed 500kHz Switching Frequency
- External Soft-Start
- PG Output
- OCP and Thermal Shutdown
- Output Adjustable from 0.603V to 18V
- Available in a 3mm x 4mm 14-pin QFN Package.

APPLICATIONS

- DSL Modems
- Cable Modems
- Set-Top Boxes
- Telecom

TYPICAL APPLICATION



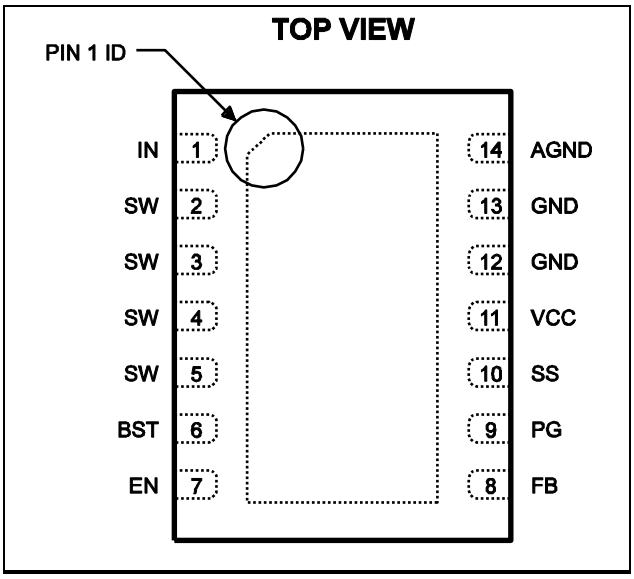


ORDERING INFORMATION

Part Number*	Package	Top Marking	Operation Junction Temperature (T_J)
MPQ28261DL	QFN14 (3x4mm)	28261	-40°C to +125°C

* For Tape & Reel, add suffix –Z (e.g. MPQ28261DL–Z);
For RoHS, compliant packaging, add suffix –LF (e.g. MPQ28261DL–LF–Z).

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (1)

V_{IN} ..... -0.3V to +23V
V_{SW} .....-0.3V(-5V for <10ns) to (V_{IN} +0.3V)
V_{BST} .....V_{SW} + 6V
Enable Current I_{EN}(2).....0.2mA
All Other Pins..... -0.3V to +6V
Continuous Power Dissipation (T_A = 25°C) (3)
.....2.6W
Junction Temperature.....150°C
Lead Temperature .....260°C
Storage Temperature..... -65°C to +150°C

Recommended Operating Conditions (4)

Supply Voltage V_{IN} ..... 4.5V to 21V
Output Voltage V_{OUT}..... 0.603V to 18V
Maximum Junction Temp. (T_J) ..... 125°C

Thermal Resistance (5) θ_{JA} θ_{JC}

QFN14 (3x4mm) ..... 48 ..... 11... °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) Refer to the section “Configuring the EN Control”.
3) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) The device is not guaranteed to function outside of its operating conditions.
5) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_J = -40°C to +125°C, unless otherwise noted. Typical value is tested at T_J = +25°C.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Supply Current						
Supply Current (Shutdown)	I_{IN}	V_{EN} = 0V			1	μA
Supply Current (Quiescent, Not Switching)	I_q	V_{EN} = 2V, V_{FB} = 1V	0.45	0.7	0.9	mA
MOSFET						
HS Switch On Resistance[6]	HS_{RDS-ON}			120		mΩ
LS Switch On Resistance[6]	LS_{RDS-ON}			20		mΩ
Switch Leakage	SW_{LKG}	V_{EN} = 0V, V_{SW} = 0V or 12V		0.1	1	μA
Current Limit						
Current Limit	I_{LIMIT}	D=40%	4.2	5.2		A
Timer						
Oscillator Frequency	f_{SW}	V_{FB}=550mV , T_J= +25°C	425	500	575	kHz
		V_{FB}=550mV , T_J= -40°C to +125°C	400		575	kHz
Minimum On Time[6]	t_{ON-MIN}			60		ns
Maximum Duty Cycle	D_{MAX}	V_{FB} = 550mV	89	92	95	%
Reference And Soft Start						
Feedback Voltage	V_{FB}	T_J= +25°C	597	603	609	mV
		T_J= -40°C to +125°C	594		612	mV
Feedback Current	I_{FB}	V_{FB} = 650mV		10	50	nA
Soft-Start Current	I_{SS}	V_{SS}=0	9	12	15	μA
Enable and UVLO						
EN Rising Threshold	V_{EN_RISING}		1.1	1.3	1.4	V
EN Threshold Hysteresis	$V_{EN\ HYS}$			0.4		V
EN Input Current	I_{EN}	V_{EN}=2V		2		μA
		V_{EN}=0V		0.1		μA
V_{IN} Under-Voltage Lockout Threshold Rising	$INUV_{Vth}$		3.8	4.0	4.2	V
V_{IN} Under-Voltage Lockout Threshold Hysteresis	$INUV_{HYS}$			880		mV
Power Good						
Power-Good Rising Threshold	PG_{Vth-Hi}			0.9		V_{FB}
Power-Good Falling Threshold	PG_{Vth-Lo}			0.8		V_{FB}
Power-Good Delay[6]	PG_{Td}	Start Up		0.25		t_{SS}
Power-Good Leakage Current	$I_{PG\ LEAK}$	V_{PG} = 3.3V			200	nA

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_J = -40°C to +125°C, unless otherwise noted. Typical value is tested at T_J = +25°C.

Parameters	Symbol	Condition	Min	Typ	Max	Units
VCC Regulator						
VCC Regulator	V_{CC}			5.1		V
VCC Load Regulation	V_{CC_REG}	I_{CC}=5mA		5		%
Thermal Protection						
Thermal Shutdown[6]	T_{SD}			150		°C
Thermal Shutdown Hysteresis[6]	$T_{SD\ HYS}$			25		°C

Notes:

6) Guaranteed by design

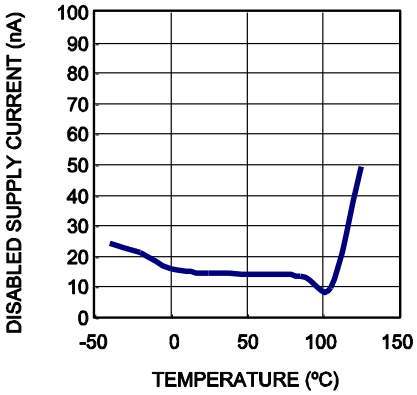
PIN FUNCTIONS

QFN14 (3x4mm) Pin #	Name	Description
1	IN	Supply Voltage. Supplies power for the internal MOSFET and regulator. The MPQ28261 operates from a 4.5V-to-21V input rail. Requires a low-ESR and low-inductance capacitor (C1) to decouple the input rail. Place the input capacitor close to this pin and connect it with wide PCB traces and multiple vias.
2,3,4,5	SW	Switch Output. Connect to the inductor and bootstrap capacitor. The internal high-side MOSFET drives these pins up to the V_{IN} voltage during the PWM duty-cycle on-time. The inductor current drives the SW pins negative during the off-time. The on-resistance of the low-side switch and the internal Schottky diode fixes the negative voltage. Connect using wide PCB traces and multiple vias.
6	BST	Bootstrap. Use a capacitor connected between SW and BST pins to form a floating supply across the high-side switch driver.
7	EN	Enable. Connected internally to a 1MΩ pull-down resistor. EN=1 to enable the MPQ28261. Pull EN low to disable the part.
8	FB	Feedback. Connect to the tap of an external resistor divider from the output to GND to set the output voltage. The frequency fold-back comparator lowers the oscillator frequency when the FB voltage is below 100mV to prevent current-limit runaway during a short circuit fault condition. Place the resistor divider as close to FB pin as possible. Avoid vias on the FB traces.
9	PG	Power-Good Output. Active high. Pin output goes to open drain of an internal switch. Power-good low-to-high threshold is 90% of regulation value. There is delay from FB ≥ 90% to PG high during start up, which is about 1/4 of SS time. Power-good high-to-low threshold is 80% of regulation value.
10	SS	Soft-Start. Connect an external capacitor to program the soft-start time of the switch-mode regulator. The soft-start pin connects to an internal reference source and to the non-inverting input of an error amplifier. When the soft-start period begins, an internal 10μA current source begins charging the capacitor. The soft-start voltage continues to rise until the voltage exceeds the reference voltage of 0.6V.
11	VCC	Bias Supply. Typical level of around 5.1V. Decouple with a 0.1μF-up-to-0.22μF capacitor. Provides most of the power to the device's internal circuits. Powered by V_{IN}, and operates in the full V_{IN} range. When V_{IN} exceeds 5.1V, VCC operates at maximum output. When V_{IN} falls below 5.1V, VCC decreases.
12,13, Exposed Pad	GND	System Ground. Reference ground for the regulated output voltage. Requires special care for PCB layout. Connect exposed pad to GND plane for optimal thermal performance.
14	AGND	Signal Ground. AGND is not internally connected to System Ground—connect to System Ground on PCB.

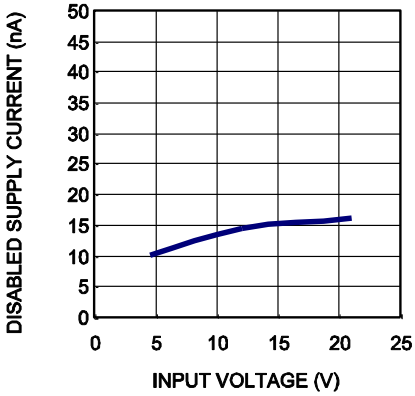
TYPICAL PERFORMANCE CHARACTERISTICS

Performance curves are tested on the evaluation board of the Design Example section.
V_{IN} = 12V, V_{OUT} = 1.2V, L = 2.8µH, T_A = 25°C, unless otherwise noted.

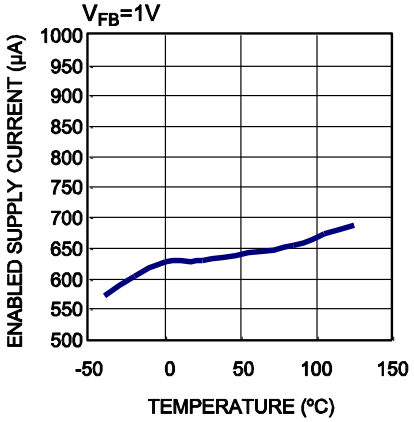
Disabled Supply Current vs .Temperature
V_{EN}=0V



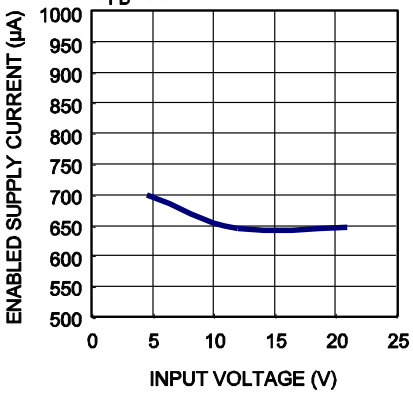
Disabled Supply Current vs .Input Voltage
V_{EN}=0V



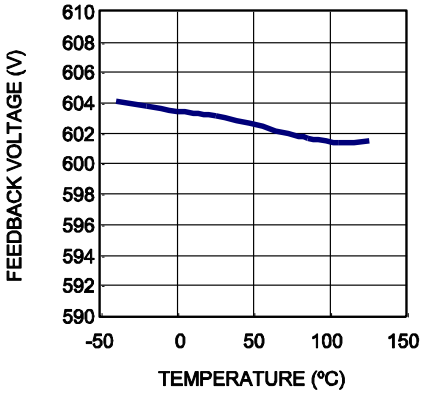
Enabled Supply Current vs.Temperature
V_{FB}=1V



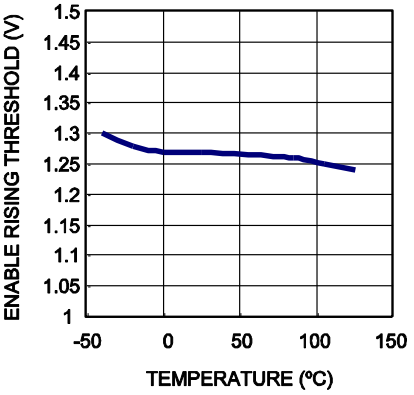
Enable Supply Current vs. Input Voltage
V_{FB}=1V



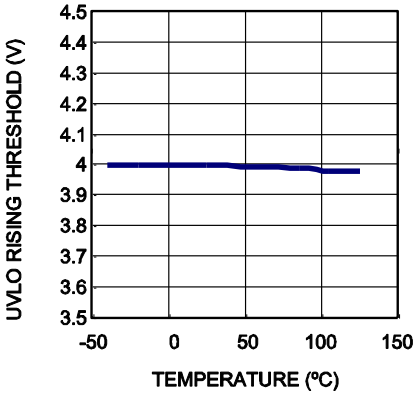
Feedback Voltage vs .Temperature



EN Rising Threshold vs .Temperature



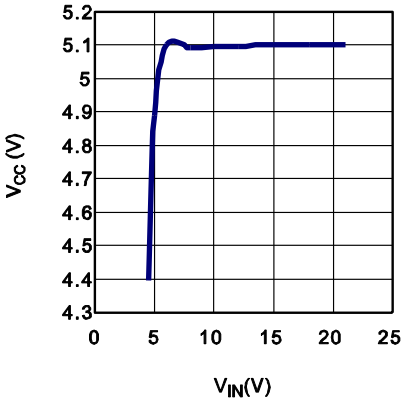
UVLO Rising Threshold vs .Temperature



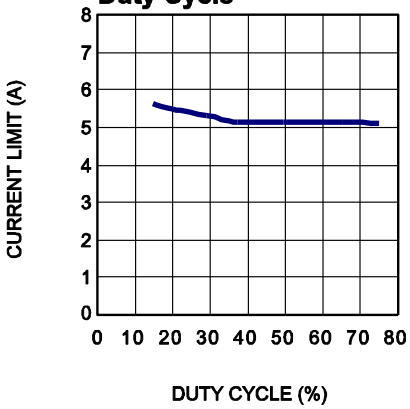
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance curves are tested on the evaluation board of the Design Example section.
V_{IN} = 12V, V_{OUT} = 1.2V, L = 2.8µH, T_A = 25°C, unless otherwise noted.

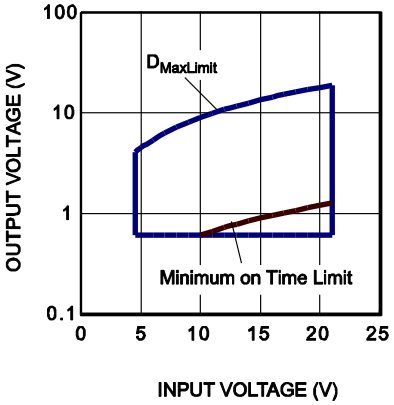
Vcc Regulator Line Regulation



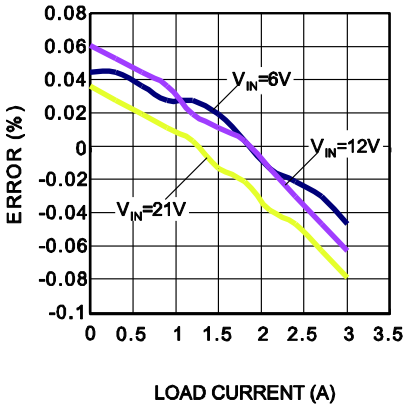
Current Limit vs. Duty Cycle



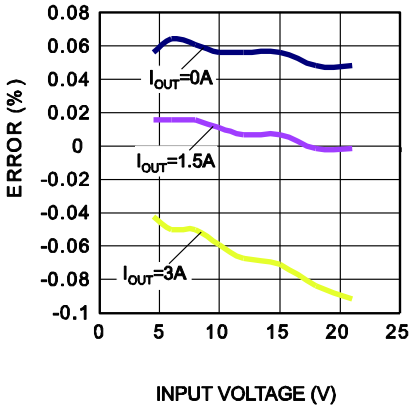
Operating Range



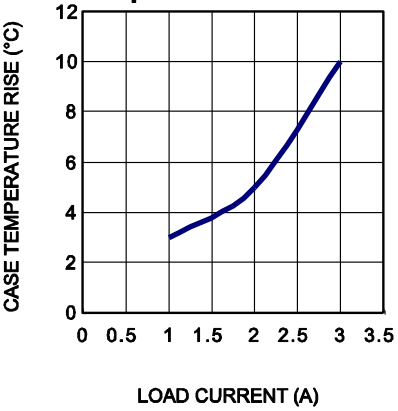
Load Regulation



Line Regulation



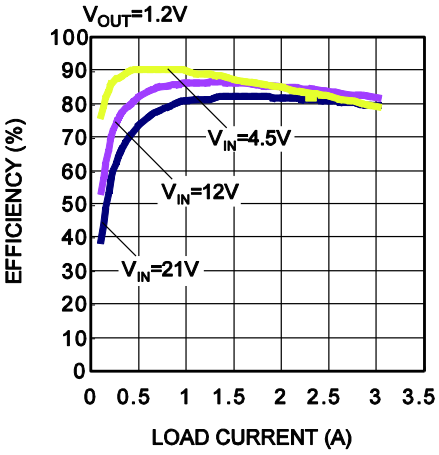
Case Temperature Rise vs. Output Current



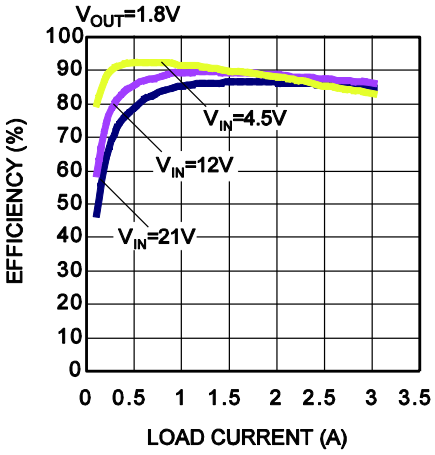
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance curves are tested on the evaluation board of the Design Example section.
V_{IN} = 12V, V_{OUT} = 1.2V, L = 2.8µH, T_A = 25°C, unless otherwise noted.

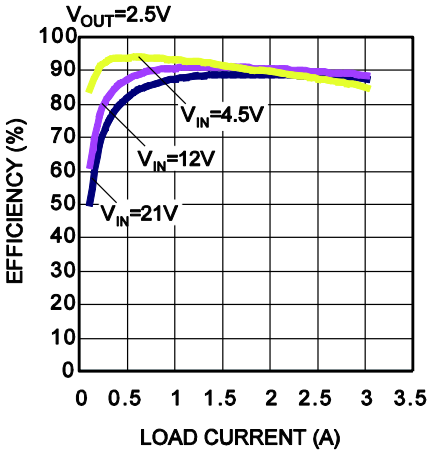
Efficiency



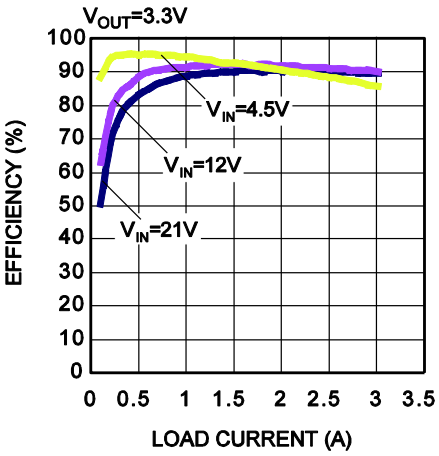
Efficiency



Efficiency



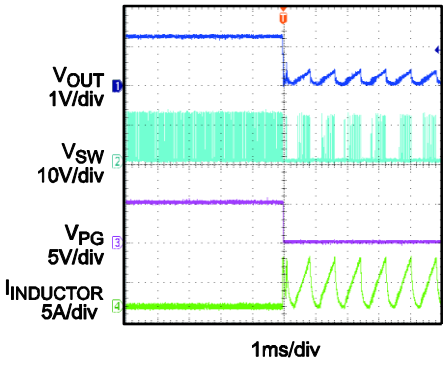
Efficiency



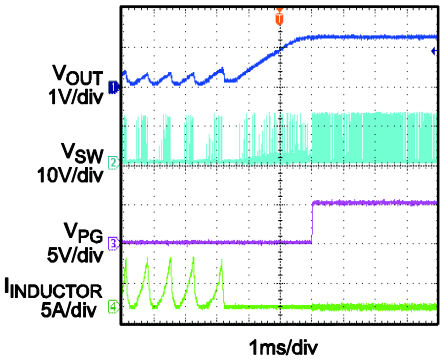
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance curves are tested on the evaluation board of the Design Example section.
V_{IN} = 12V, V_{OUT} = 1.2V, L = 2.8µH, T_A = 25°C, unless otherwise noted.

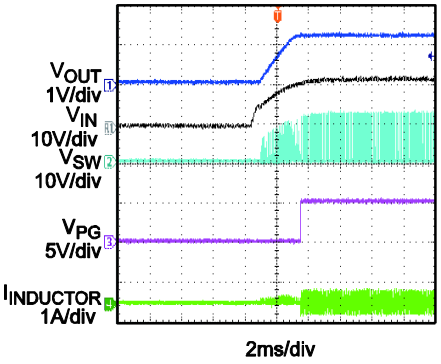
Short Entry



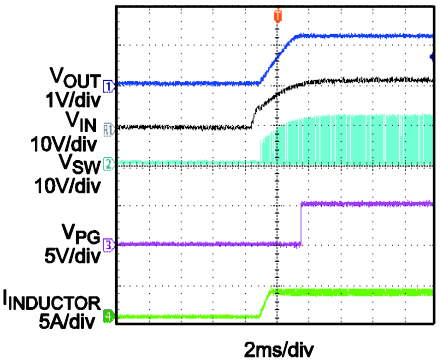
Short Recovery



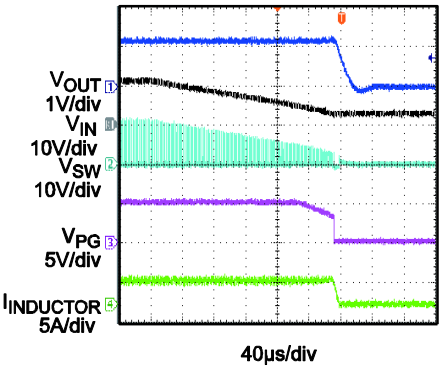
Power Up without Load



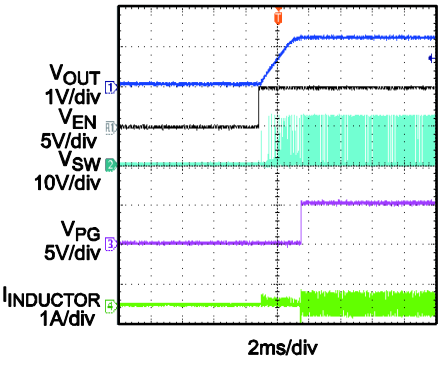
Power Up with 3A Load



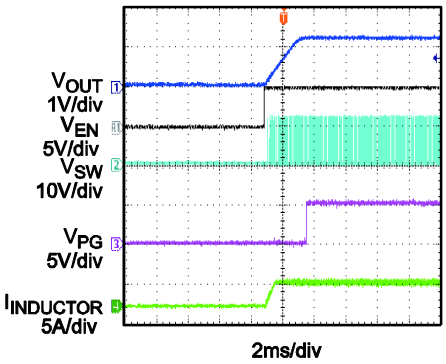
Power Off with 3A Load



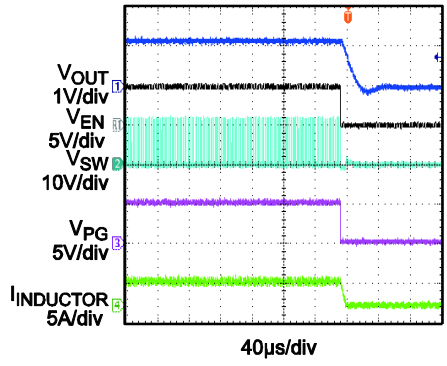
Enable Startup without Load



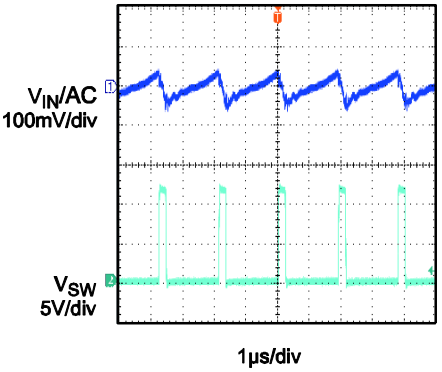
Enable Startup with 3A Load



Enable Shutdown with 3A Load



Input Ripple Voltage
I_{OUT}=3A

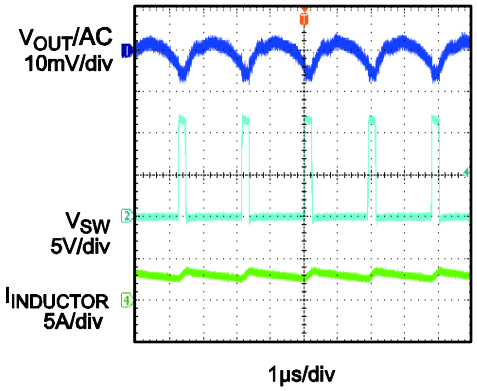


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance curves are tested on the evaluation board of the Design Example section.
V_{IN} = 12V, V_{OUT} = 1.2V, L = 2.8µH, T_A = 25°C, unless otherwise noted.

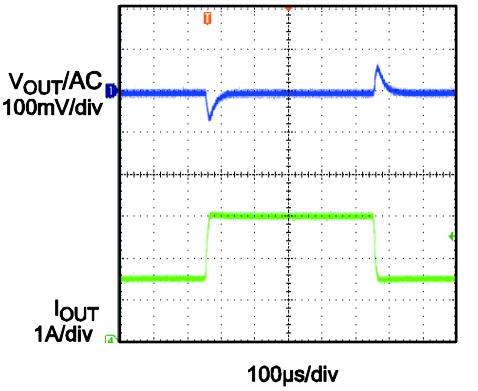
Output Ripple Voltage

I_{OUT}=3A



Load Transient Response

I_{OUT}=1.5A-3A



FUNCTIONAL BLOCK DIAGRAM

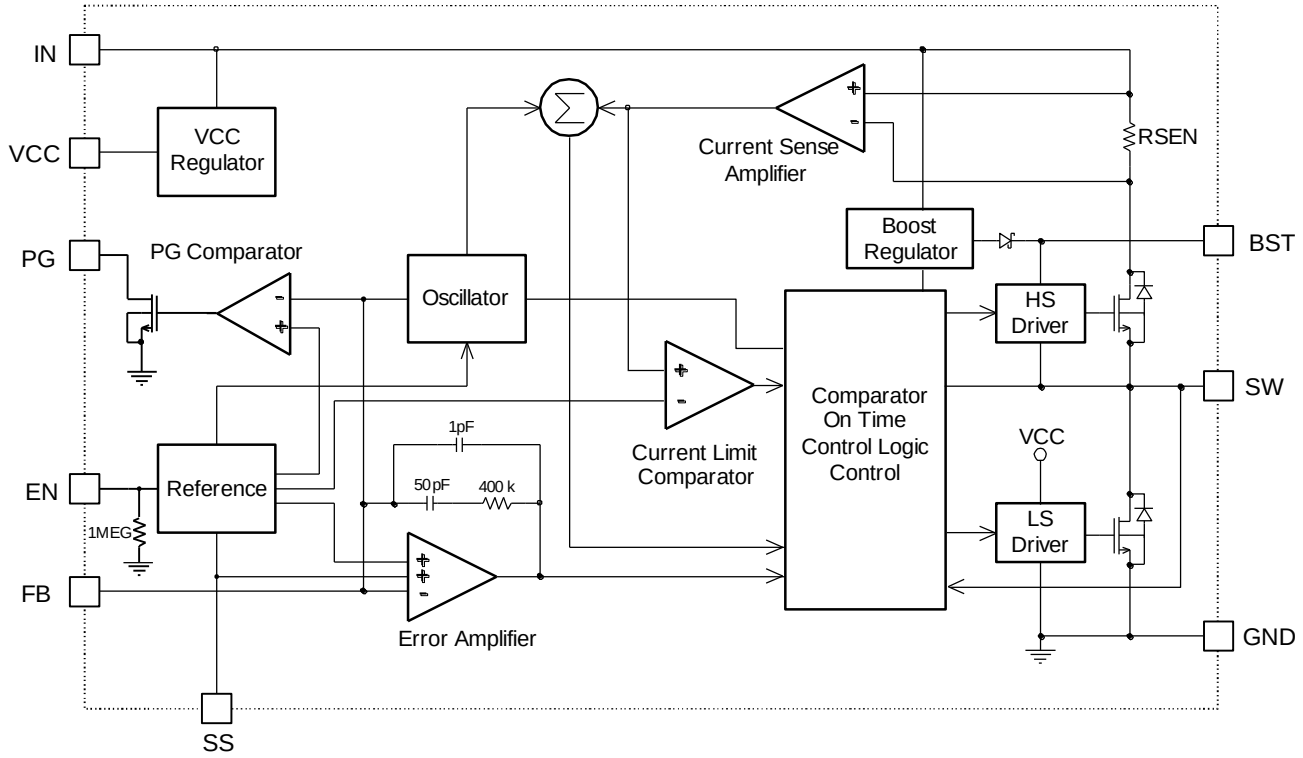


Figure 1: Functional Block Diagram

OPERATION

The MPQ28261 is a high-frequency, synchronous, rectified, step-down, switch mode converter with built-in internal power MOSFETs. It offers a very compact solution to output a 3A continuous output current over a wide input supply range, with excellent load and line regulation.

The MPQ28261 operates in a fixed-frequency peak-current–control mode to regulate the output voltage. Around the start of a PWM cycle, the integrated high-side power MOSFET (HS-FET) turns on and remains on until its current reaches the value set by the COMP voltage. When the power switch turns off, it remains off until the next clock cycle starts. If the current in the HS-FET does not reach the COMP set value for 90% of one PWM period, the HS-FET will turn off.

Error Amplifier

The error amplifier compares V_{FB} against the internal 0.6V reference (V_{REF}) and outputs a current proportional to the difference. The output current both charges and discharges the internal compensation network to form the COMP voltage, which controls the power MOSFET current. The optimized internal compensation network minimizes the external component counts and simplifies the control loop design.

Internal Regulator

The 5V regulator powers most of the internal circuitry. This regulator takes the V_{IN} input and operates in the full V_{IN} range When V_{IN} exceeds 5.1V, the regulator outputs at its maximum level; when V_{IN} falls below 5.1V, the output decreases. The regulator requires a 0.1µF ceramic capacitor for decoupling purposes.

Configuring the Enable Control

The MPQ28261 has a dedicated Enable control pin (EN): pulling this pin high or low enables or disables the IC. Tie EN to V_{IN} through a resistor for automatic start up. Choose the values of the pull-up resistor (R_{UP} from the IN pin to the EN pin) and the pull-down resistor (R_{DOWN} from the EN pin to GND) to determine the automatic start-up voltage:

$$V_{IN-START} = 1.4 \times \frac{(R_{UP} + R_{DOWN})}{R_{DOWN}} (V)$$

For example, for R_{UP}=100kΩ and R_{DOWN}=51kΩ, the $V_{IN-START}$ is set at 4.15V.

To reduce noise, add a 10nF ceramic capacitor from EN to GND.

An internal zener diode on the EN pin clamps the EN pin voltage to prevent run away. The maximum pull up current assuming the worst case 6V for the internal zener clamp should be less than 0.2mA.

Therefore, when driving EN with an external logic signal, use an EN voltage less than 6V. When connecting EN to IN through a pull-up resistor or a resistive voltage divider, select a resistance that ensures a maximum pull-up current less than 0.2mA.

If using a resistive voltage divider and V_{IN} exceeds 6V, then the minimum resistance for the pull-up resistor R_{UP} should meet:

$$\frac{V_{IN} - 6V}{R_{UP}} - \frac{6V}{R_{DOWN}} \leq 0.2mA$$

With only R_{UP} (the pull-down resistor, R_{DOWN}, is not connected), then the VCC UVLO threshold determines $V_{IN-START,}$ so the minimum resistor value is:

$$R_{UP} \geq \frac{V_{IN} - 6V}{0.2mA} (\Omega)$$

Under-Voltage Lockout

Under-voltage lockout (UVLO) protects the chip from operating at insufficient supply voltages. The UVLO comparator monitors the output voltage of the internal regulator, VCC. The UVLO rising threshold is about 4.0V while its falling threshold is 3.2V.

Power Good Indicator

MPQ28261 uses the open drain of an NMOS for the Power Good (PG) indicator. When V_{FB} rises above 90% of the reference voltage, PG pin is pulled up to VCC by an external resistor

after a delay. The PG delay time is about 1/4 of SS time. If V_{FB} falls below 80% of the reference voltage, PG pin is pulled down to ground by an internal MOSFET.

External Soft-Start

Connecting a capacitor from the soft-start (SS) pin to ground adjusts the SS time. During SS initiation, an internal 12μA current source charges the external capacitor. The SS pin connects internally to the non-inverting input of the error amplifier. The SS continues to charge until the voltage on the SS capacitor exceeds the 0.6V reference voltage. Then the reference voltage functions as the non-inverting input of the error amplifier. The following equation estimates the SS time:

$$t_{SS}(ms) = \frac{0.6V \times C_{SS}(nF)}{12\mu A}$$

Table 1 lists SS times with different external capacitor values. If the output capacitor is large, use a large SS capacitor to ensure proper device start-up.

Table 1: Soft Start Time vs. Capacitor Value

t_{SS} (ms)	C_{SS} (nF)
0.5	10
1.65	33
2.35	47
3.4	68
5	100

If the output of the MPQ28261 is pre-biased to a certain voltage during startup, the IC will disable switching on both the HS-FET and LS-FET until the voltage on the internal SS capacitor exceeds the sensed output V_{FB}, as Figure 2 shows.

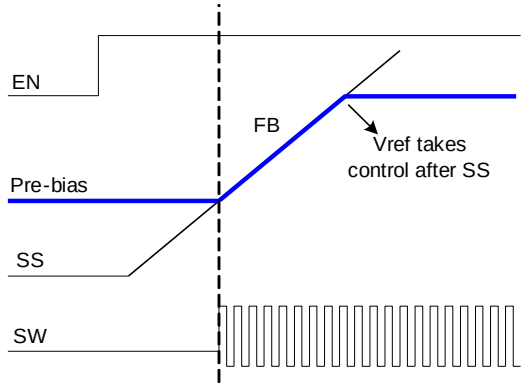


Figure 2: Pre-Biased Soft-Start

Over-Current Protection

The MPQ28261 has hiccup over-current limit protection for when the inductor current peak value exceeds the set current limit threshold: hiccup occurs when the output voltage drops below 70% of the reference voltage and the inductor current exceeds the current limit. This is especially useful to ensure system safety under fault conditions. The hiccup function is enabled during SS duration.

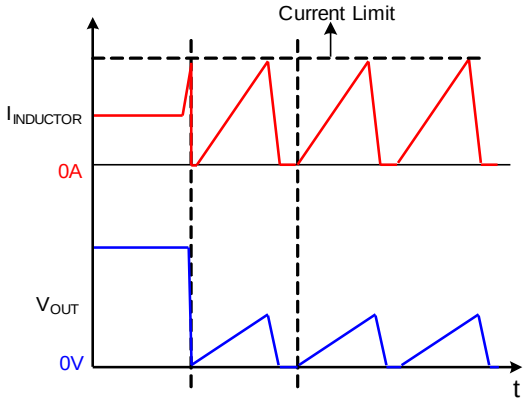


Figure 3: Over-Current Behavior in Hiccup

Figure 3 shows the hiccup function. After the hiccup occurs, the SS pin voltage goes low and MPQ28261 begins SS shortly after. During the SS period, if the inductor current hits current limit and the output voltage is less than 70% of the reference, the SS voltage will go low.

Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures.

When the silicon die temperature exceeds 150°C, the whole chip shuts down: The HS-FET and LS-FET turn off, and the SS pin voltage goes low. When the temperature drops below the lower threshold—typically 140°C—the chip restarts with an SS.

Floating Driver and Bootstrap Charging

The floating power MOSFET driver has several features to ensure stability and functionality, such as its own UVLO protection with a rising threshold of 2.2V and a hysteresis of 150mV. An external bootstrap capacitor—regulated internally by V_{IN} through D1, M1, C4, L1 and C2 (see Figure 4)—powers this driver. U1 regulates M1 to maintain a 5V BST voltage across C4 whenever (V_{IN}-V_{SW}) > 5V.

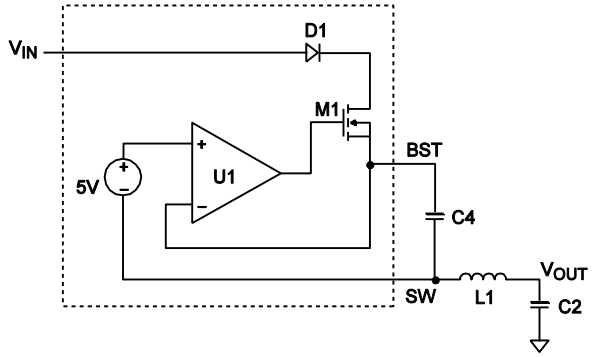


Figure 4: Internal Bootstrap Charging Circuit

Startup and Shutdown

When V_{IN} and EN exceed their respective thresholds, the chip starts. The reference block starts first, generating stable reference voltages and currents, and then the internal regulator is enabled. The regulator provides a stable power supply for the rest of the device.

Three events can shut down the chip: EN low, V_{IN} low, and thermal shutdown. In shutdown, the signaling path shuts down first to avoid triggering any faults. Then the COMP voltage and the internal supply rail are pulled down. The floating driver is not subject to this shutdown command.

APPLICATION INFORMATION

COMPONENT SELECTION

Output Voltage Selection

The external resistor divider sets the output voltage (see Typical Application circuits on pages 1 and 17). The feedback resistor R1 also sets the bandwidth of the feedback loop in conjunction with the internal compensation capacitor. Choose R1 with a value of ~10kΩ. Use the following equation to then estimate R2:

$$R2 = \frac{R1}{\frac{V_{OUT}}{0.6V} - 1}$$

Use a T-type network for low values V_{OUT}, as shown in Figure 5.

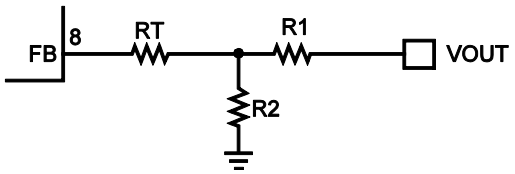


Figure 5: T-Type Network

Table 2 lists the recommended T-type resistors value for common output voltages.

Table 2: Resistor Selection for Common

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	Rt (kΩ)
1.0	10(1%)	15(1%)	24 (1%)
1.2	10(1%)	10(1%)	24 (1%)
1.8	10(1%)	4.99(1%)	24 (1%)
2.5	10(1%)	3.16(1%)	24 (1%)
3.3	10(1%)	2.20(1%)	24 (1%)
5	10(1%)	1.36(1%)	24 (1%)

Inductor Selection

For most applications, chose an inductor value between 1µH and 10µH with a DC current rating that is at least 25% percent higher than the maximum load current. Select an inductor with a DC resistance less than 15mΩ for best efficiency. Use the following equation to estimate the inductance value for most designs:

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}}$$

Where ΔI_L is the inductor ripple current.

Choose the inductor current to equal ~30% of the maximum load current. Estimate the maximum inductor peak current as:

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2}$$

A larger value inductor provides a higher maximum load current, and reduces the output voltage ripple. If the load is lower than the maximum load current, then a lower-value inductor will suffice and the chip then operates with higher ripple current; this allows for the use of a either a physically smaller inductor, or one with a lower DCR that can result in higher efficiency. If the inductance differs from the conditions described above, then the maximum load current will depend on the input voltage.

Choose an inductor value that allows for maximum output current near the switch current limit. Table 3 lists some of the recommended inductors.

Table 3: Recommended Inductor

Part Number	Manufacturer	Inductance (µH)	DCR (mΩ)	Current Rating (A)
HC8LP-1R2	Cooper	1.2	7.5	12.4
D104C-919AS-1R8N	TOKO	1.8	7.6	10.4
7443552280	Wurth	2.8	10.5	11
FDA1055-3R3M	TOKO	3.3	7.3	11.7
7447709004	Wurth	4.7	11	13

Selecting the Input Capacitor

The MPQ28261 requires an input capacitor (C1) to supply the AC current to the step-down converter while maintaining the DC input voltage, because the input current to the step-down converter is discontinuous. Use capacitors with low equivalent series resistance (ESR)—such as ceramic capacitors with X5R or X7R dielectrics with low ESR and small temperature coefficients. For most applications, use a 22µF capacitor.

Since C1 absorbs the input switching current, it must withstand significant ripple current. The RMS current in the input capacitor can be estimated by:

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

The worse case condition occurs at $V_{IN} = 2V_{OUT}$, where:

$$I_{C1} = \frac{I_{LOAD}}{2}$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum or ceramic. Include a small ceramic capacitor with a value of ~0.1µF as close to the IC as possible when using electrolytic or tantalum capacitors. Use sufficiently-large ceramic capacitors that can provide sufficient charge to prevent excessive voltage ripple. The capacitor-induced input voltage ripple can be estimated by:

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_S \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Selecting the Output Capacitor

The output capacitor (C2) maintains the DC output voltage. Use ceramic, tantalum, or low-ESR electrolytic capacitors to minimize the output voltage. The output voltage ripple can be estimated as:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_S \times C2}\right)$$

Where L1 is the inductor value and R_{ESR} is the ESR value of the output capacitor.

For ceramic capacitors, the capacitor dominates the impedance at the switching frequency, and subsequently dominates the output voltage ripple. For simplicity, the output voltage ripple can be estimated as:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_S^2 \times L1 \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. Subsequently, the output ripple can be approximated as:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR}$$

The characteristics of the output capacitor also affect the system regulation stability. The MPQ28261 can be optimized for a wide range of capacitances and ESR values.

The maximum capacitance is 1100µF. (Tested on Chroma 63030, CCH mode, 3A load current, soft start capacitor is 100nF, V_{OUT}=5V).

External Bootstrap Diode

An external bootstrap diode may enhance the efficiency of the regulator under the following applicable conditions:

- V_{OUT} is 5V or 3.3V; and
- Duty cycle is high: $D = \frac{V_{OUT}}{V_{IN}} > 65\%$

In these cases, an external BST diode is recommended from the VCC pin to BST pin, as shown in Figure 6.

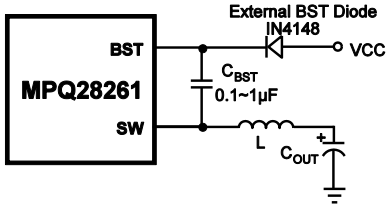


Figure 6: Add Optional External Bootstrap Diode to Enhance Efficiency

The recommended external BST diode is IN4148 where the BST capacitor value is between 0.1 and 1µF.

TYPICAL APPLICATIONS

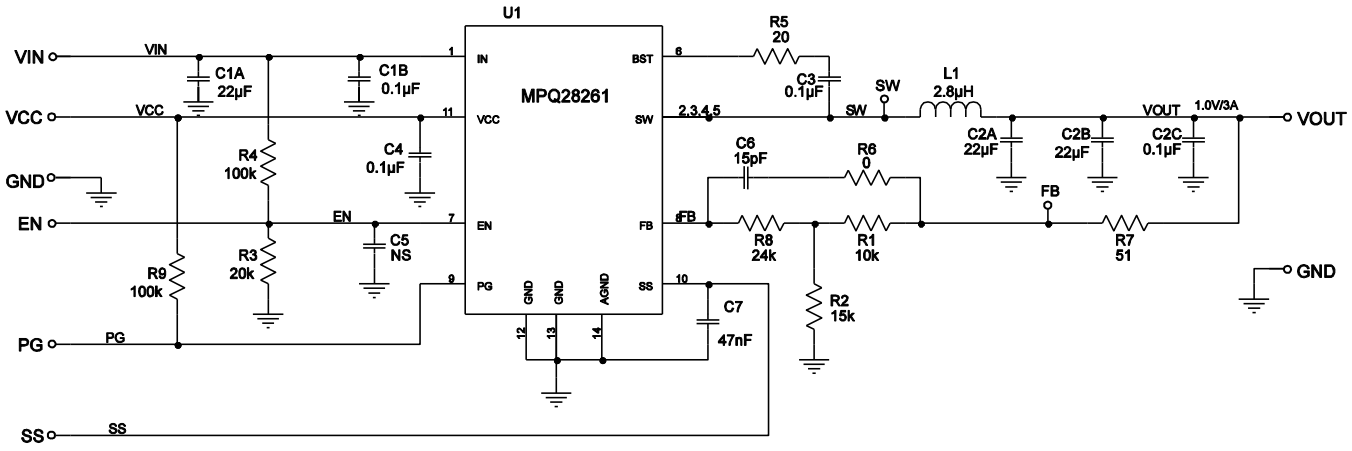


Figure 7: V_{OUT} = 1V

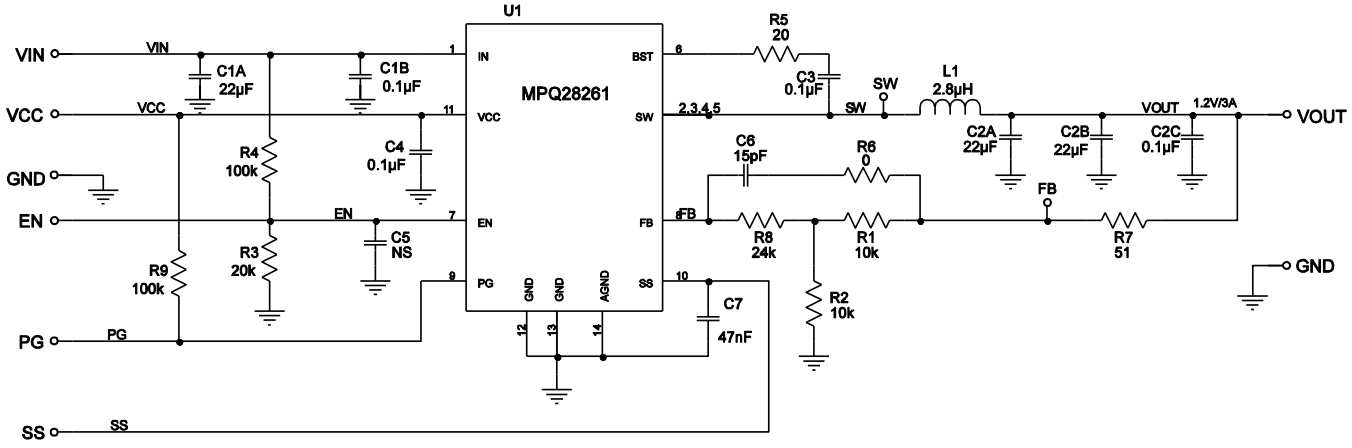


Figure 8: V_{OUT} = 1.2V

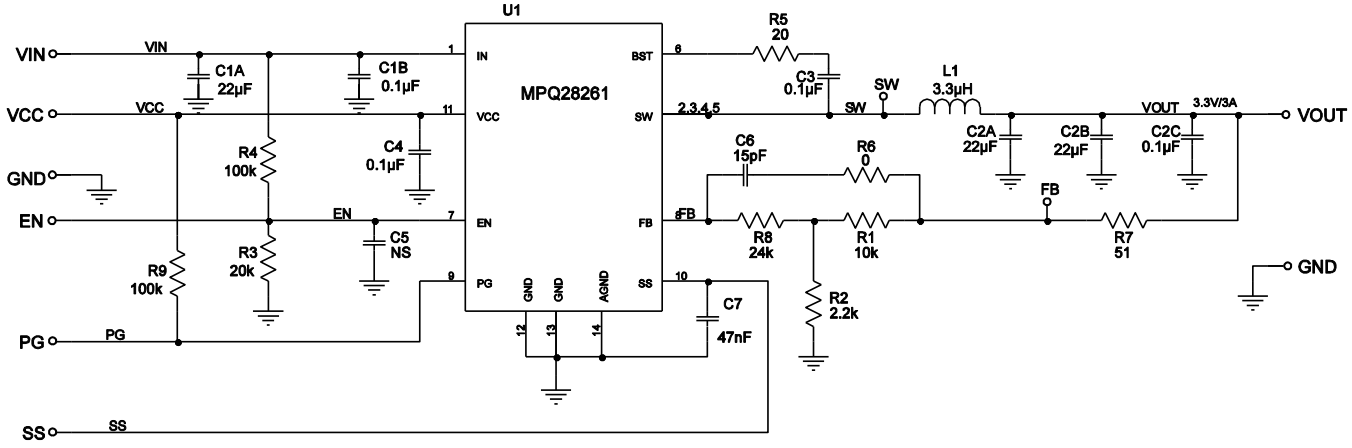


Figure 9: V_{OUT} = 3.3V

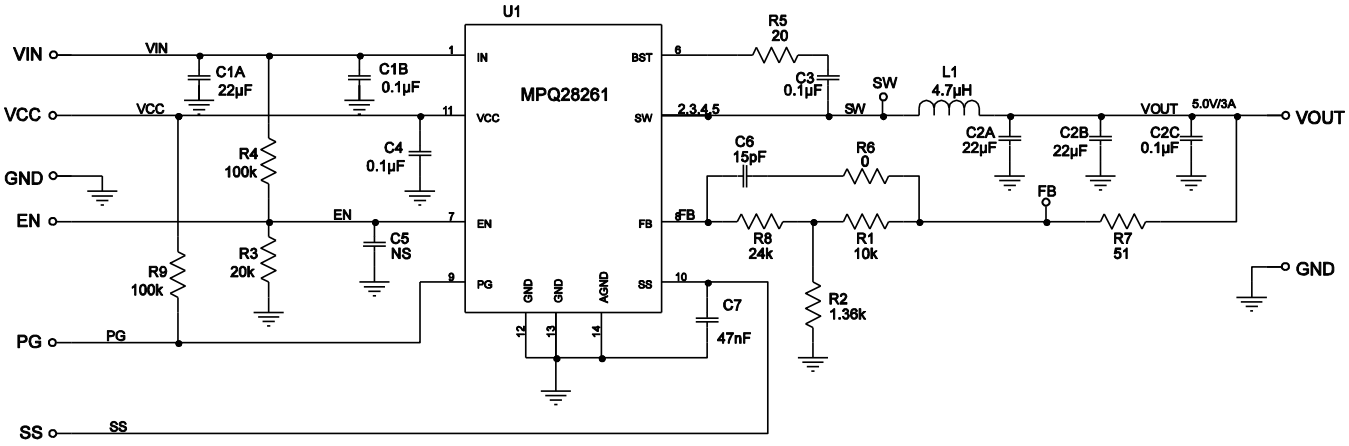
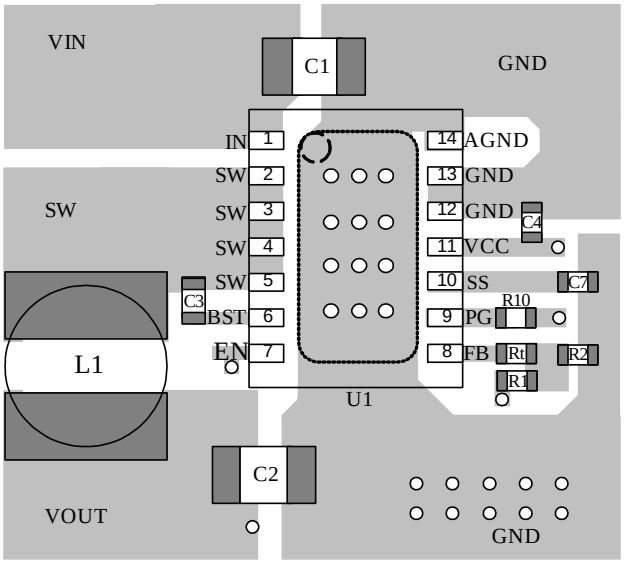


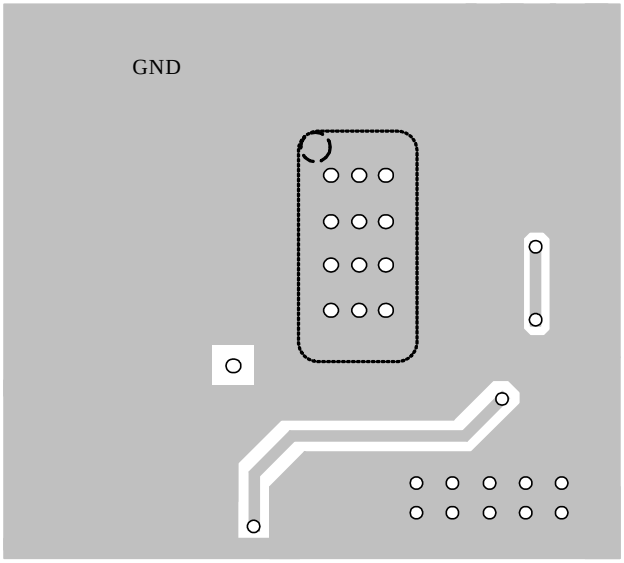
Figure 10: V_{OUT} = 5V

Layout Recommendation

1) Lay the large switching current paths (GND, IN, and SW) very close to the device using short, wide, and direct traces. Minimize the loop length and area formed by these components. These components, including the inductor and output capacitor, should be placed on the same side of the circuit board, with their connections on that layer. Place a localized unbroken ground plane below these components.
2) Place input capacitors as close as possible to the IN and GND pins with wide PCB traces to avoid excess inductance and to prevent large spikes. Add thermal vias to the bottom side to improve thermal performance.
3) Place the decoupling capacitor as close as possible to the VCC and GND pins. Avoid routing the VCC trace near the noisy SW-to-BST trace.
4) Place the inductor as close as possible to the SW pin. Keep the switching node SW short and away from the sensitive nodes such as the feedback network.
5) Place external feedback resistors next to the FB pin. Make sure that there is no via on the FB trace and keep the FB trace short. Route the FB trace away from the noisy SW and BST node.
6) Keep the BST voltage path (BST, C3, and SW) as short as possible. Keep the BST trace should away from sensitive nodes.



Top Layer

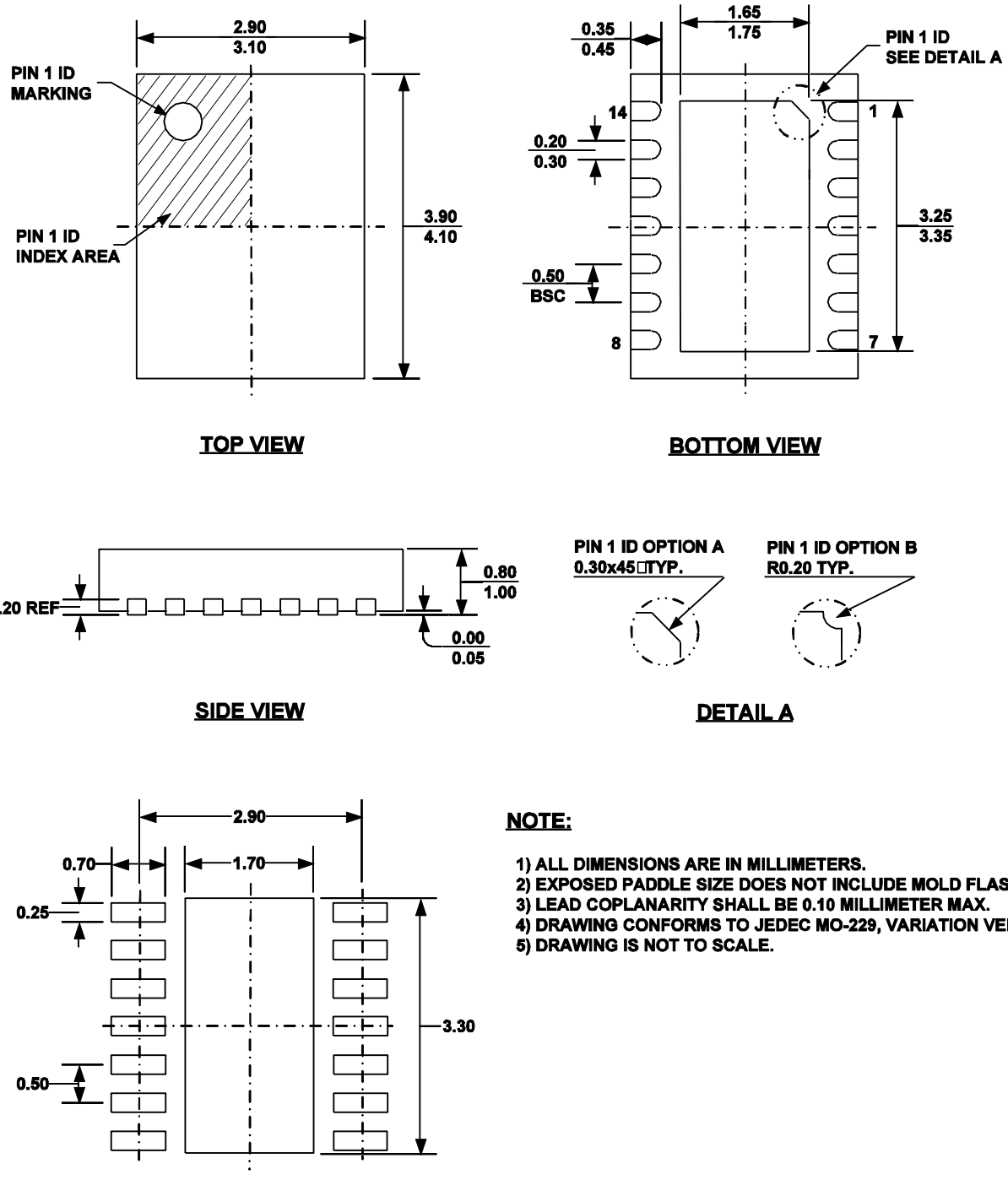


Bottom Layer

Figure 11: PCB Layout

PACKAGE INFORMATION

QFN14 (3mmx4mm)



NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX.
4) DRAWING CONFORMS TO JEDEC MO-229, VARIATION VEED-5.
5) DRAWING IS NOT TO SCALE.