DESCRIPTION

The MPQ2420 is a step-down switching regulator with integrated high- and low-side, high-voltage power MOSFETs. It provides a highly efficient output of up to 0.3A. The integrated watchdog adds additional security redundancy to the system.

The wide 4.5V to 75V input range accommodates a variety of step-down applications in an automotive environment. A 5μA shutdown mode quiescent current in a full temperature range is ideal for battery-powered applications. It allows for high-power conversion efficiency over a wide load range by scaling down the switching frequency under a light-load condition to reduce switching and gate driver losses. The start-up switching frequency and short circuit can also be scaled down to prevent inductor current runaway.

Full protection features include under-voltage lockout (UVLO) and thermal shutdown. Thermal shutdown provides reliable, fault-tolerant operation.

The MPQ2420 is available in a TSSOP-16 EP package.

FEATURES

- 20μA Quiescent Current for Buck Only
- Wide 4.5V to 75V Operating Input Range (80V ABS MAX)
- 1.2Ω/0.45Ω Internal Power MOSFETs
- Programmable Soft Start
- FB Tolerance: 1% at Room Temperature, 2% at Full Temperature
- Adjustable Output Voltage
- Integrated Window Watchdog
- Power-On Reset during Power-Up
- Under-Voltage Lockout and Thermal Shutdown
- Programmable Short Window Mode or Long Window Mode
- Low Shutdown Mode Current of 5μA
- TSSOP-16 EP Package
- Available in AEC-Q100 Grade 1

APPLICATIONS

- Automotive Systems
- Industrial Power Systems
- Distributed Power Systems
- Battery-Powered Systems

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ORDERING INFORMATION

<table>
<thead>
<tr>
<th>Part Number*</th>
<th>Package</th>
<th>Top Marking</th>
</tr>
</thead>
<tbody>
<tr>
<td>MPQ2420GF</td>
<td>TSSOP-16 EP</td>
<td></td>
</tr>
<tr>
<td>MPQ2420GF-AEC1</td>
<td></td>
<td>See Below</td>
</tr>
</tbody>
</table>

* For Tape & Reel, add suffix –Z (e.g. MPQ2420GF–Z)

TOP MARKING

MPSYWW
MP2420
LLLLLL

MPS: MPS prefix
YY: Year code
WW: Week code
MP2420: Part code of MPQ2420GF
LLLLLL: Lot number

PACKAGE REFERENCE

TSSOP-16 EP
ABSOLUTE MAXIMUM RATINGS

Supply voltage ($V_{IN}$) ............... -0.3V to +80V
Switch voltage ($V_{SW}$) ............ -0.3V to $V_{IN}$ + 1V
BST to SW............................... -0.3 to +6.0V
All other pins.......................... -0.3V to +6.0V
EN sink current......................... 150µA

Continuous power dissipation ($T_A = +25^\circ$C) 

TSSOP-16 EP.............................. 2.7W
Junction temperature...................... 150°C
Lead temperature........................ 260°C
Storage temperature...................... -65°C to +150°C

Recommended Operating Conditions

Supply voltage ($V_{IN}$) ............... 4.5V to 75V
Output voltage ($V_{OUT}$) .............. 1V to 0.9×$V_{IN}$
Operating junction temp. ($T_J$) ...... -40°C to 125°C

Thermal Resistance

TSSOP-16 EP.............................. 45°...10°C/W

NOTES:
1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature $T_J$ (MAX), the junction-to-ambient thermal resistance $\theta_{JA}$, and the ambient temperature $T_A$. The maximum allowable continuous power dissipation at any ambient temperature is calculated by $P_D$ (MAX) = ($T_J$ (MAX) - $T_A$)/$\theta_{JA}$. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.
## ELECTRICAL CHARACTERISTICS

$V_{IN} = 24\text{V}, \ V_{EN} = 2\text{V}, \ V_{CC} = 5\text{V}, \ T_J = -40^\circ\text{C} \text{ to } +125^\circ\text{C}, \text{ unless otherwise noted.}$

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>DC/DC Converter</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Supply quiescent current</td>
<td>No load, $V_{FB} = 1.2\text{V}$</td>
<td>20</td>
<td>30</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>Shutdown supply current</td>
<td>$V_{EN} &lt; 0.3\text{V}$</td>
<td>2.2</td>
<td>5</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>$V_{IN}$ UVLO rising threshold</td>
<td>$V_{IN} = 4.5\text{V} \text{ to } 75\text{V}, \ T_J = 25^\circ\text{C}$</td>
<td>0.99</td>
<td>1.0</td>
<td>1.01</td>
<td>V</td>
</tr>
<tr>
<td>$V_{IN}$ UVLO falling threshold</td>
<td>$V_{IN} = 4.5\text{V} \text{ to } 75\text{V}$</td>
<td>0.98</td>
<td></td>
<td>1.02</td>
<td>V</td>
</tr>
<tr>
<td>$V_{IN}$ UVLO hysteresis</td>
<td>$V_{EN} = 2.4\text{V}, \ V_{SW} = 75\text{V}$</td>
<td>0.275</td>
<td>0.45</td>
<td>0.625</td>
<td>Ω</td>
</tr>
<tr>
<td>Feedback voltage</td>
<td>$V_{REF} = 5\text{V}, \ T_J = 25^\circ\text{C}$</td>
<td>0.2</td>
<td></td>
<td>1.035</td>
<td>V</td>
</tr>
<tr>
<td>Feedback current</td>
<td>$V_{FB} = 1.2\text{V}$</td>
<td>-50</td>
<td>2</td>
<td>50</td>
<td>nA</td>
</tr>
<tr>
<td>$V_{REF}$ voltage</td>
<td>$V_{IN} = 4.5\text{V} \text{ to } 75\text{V}, \ I_{REF} = 100\mu\text{A}$</td>
<td>0.965</td>
<td>1</td>
<td>1.035</td>
<td>V</td>
</tr>
<tr>
<td>Upper switch-on resistance</td>
<td>$V_{BST} - V_{SW} = 5\text{V}, \ T_J = 25^\circ\text{C}$</td>
<td>0.9</td>
<td>1.2</td>
<td>1.5</td>
<td>Ω</td>
</tr>
<tr>
<td>Lower switch-on resistance</td>
<td>$V_{BST} - V_{SW} = 5\text{V}$</td>
<td>0.7</td>
<td></td>
<td>2.5</td>
<td>Ω</td>
</tr>
<tr>
<td>Lower switch leakage</td>
<td>$V_{EN} = 0\text{V}, \ V_{SW} = 75\text{V}$</td>
<td>1</td>
<td></td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>Peak current limit</td>
<td></td>
<td>630</td>
<td>720</td>
<td>810</td>
<td>mA</td>
</tr>
<tr>
<td>Minimum switch-on time(5)</td>
<td></td>
<td>120</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Enable rising threshold</td>
<td></td>
<td>1.25</td>
<td>1.55</td>
<td>1.85</td>
<td>V</td>
</tr>
<tr>
<td>Enable falling threshold</td>
<td></td>
<td>1.152</td>
<td>1.2</td>
<td>1.248</td>
<td>V</td>
</tr>
<tr>
<td>Enable threshold hysteresis</td>
<td></td>
<td>0.35</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Enable current</td>
<td>$V_{EN} = 2.4\text{V}$</td>
<td>0.8</td>
<td></td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>Soft-start current</td>
<td></td>
<td>4</td>
<td>5.5</td>
<td>7</td>
<td>µA</td>
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<tr>
<td>POK upper trip threshold</td>
<td>$I_{SINK} = 1\text{mA}$</td>
<td>86</td>
<td>90</td>
<td>94</td>
<td>%</td>
</tr>
<tr>
<td>POK lower trip threshold</td>
<td></td>
<td>81</td>
<td>85</td>
<td>89</td>
<td>%</td>
</tr>
<tr>
<td>POK threshold hysteresis</td>
<td></td>
<td>5</td>
<td></td>
<td></td>
<td>%</td>
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<tr>
<td>POK deglitch timer</td>
<td></td>
<td>40</td>
<td></td>
<td></td>
<td>µs</td>
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<tr>
<td>POK output voltage low</td>
<td></td>
<td>0.4</td>
<td></td>
<td></td>
<td>V</td>
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<tr>
<td>FB OVP rising threshold</td>
<td>$I_{SINK} = 1\text{mA}$</td>
<td>1.05</td>
<td>1.1</td>
<td></td>
<td>V</td>
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<tr>
<td>FB OVP hysteresis</td>
<td></td>
<td>50</td>
<td></td>
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<td>mV</td>
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<tr>
<td>Thermal shutdown(5)</td>
<td></td>
<td>175</td>
<td></td>
<td></td>
<td>°C</td>
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<tr>
<td>Thermal shutdown hysteresis(5)</td>
<td></td>
<td>20</td>
<td></td>
<td></td>
<td>°C</td>
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</tbody>
</table>

**NOTE:**

5) Derived from bench characterization. Not tested in production.
# ELECTRICAL CHARACTERISTICS (continued)

$V_{\text{IN}} = 24\text{V}$, $V_{\text{EN}} = 2\text{V}$, $V_{\text{CC}} = 5\text{V}$, $T_J = -40^\circ\text{C}$ to $+125^\circ\text{C}$, unless otherwise noted.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
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<tr>
<td><strong>Watchdog Power Supply</strong></td>
<td></td>
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<tr>
<td>Timer voltage</td>
<td>$R_{\text{TIMER}} = 51\text{k}$</td>
<td></td>
<td>0.3</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Quiescent current</td>
<td>$R_{\text{TIMER}} = 100\text{k}$</td>
<td>16</td>
<td>32</td>
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<td></td>
<td>µA</td>
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<tr>
<td></td>
<td>$R_{\text{TIMER}} = 51\text{k}$</td>
<td>19</td>
<td></td>
<td></td>
<td></td>
<td>µA</td>
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<tr>
<td>Power-on reset threshold</td>
<td>$V_{\text{POR-HIGH}}$ (WDO goes high with rising $V_{\text{CC}}$)</td>
<td>4.4</td>
<td>4.6</td>
<td>4.8</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>$V_{\text{POR-LOW}}$ (WDO goes low with falling $V_{\text{CC}}$)</td>
<td>4.3</td>
<td>4.5</td>
<td>4.7</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td><strong>Watchdog Timing</strong></td>
<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Single period</td>
<td>$T$</td>
<td>$R_{\text{TIMER}} = 51\text{k}$</td>
<td>-10%</td>
<td>880</td>
<td>+10%</td>
<td></td>
</tr>
<tr>
<td>Power-on delay$^6$</td>
<td>$t_0$</td>
<td>$R_{\text{TIMER}} = 51\text{k}$</td>
<td></td>
<td>10</td>
<td></td>
<td></td>
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<tr>
<td>Sync signal monitoring time$^6$</td>
<td>$t_1$</td>
<td>$R_{\text{TIMER}} = 51\text{k}$</td>
<td></td>
<td>450</td>
<td></td>
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<tr>
<td>Watchdog window close time (short mode)$^6$</td>
<td>$t_2$</td>
<td>$R_{\text{TIMER}} = 51\text{k}$, mode = low</td>
<td></td>
<td>15</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Watchdog window open time (short mode)$^6$</td>
<td>$t_3$</td>
<td>$R_{\text{TIMER}} = 51\text{k}$, mode = low</td>
<td></td>
<td>10</td>
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<tr>
<td>Watchdog window close time (long mode)$^6$</td>
<td>$t_4$</td>
<td>$R_{\text{TIMER}} = 51\text{k}$, mode = high</td>
<td></td>
<td>1500</td>
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<tr>
<td>Watchdog window open time (long mode)$^6$</td>
<td>$t_5$</td>
<td>$R_{\text{TIMER}} = 51\text{k}$, mode = high</td>
<td></td>
<td>1000</td>
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<tr>
<td>WDO reset pulse width$^6$</td>
<td>$t_6$</td>
<td>$R_{\text{TIMER}} = 51\text{k}$</td>
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<td>4</td>
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<tr>
<td>WDI_OK pulse width</td>
<td></td>
<td></td>
<td>10</td>
<td></td>
<td>5000</td>
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<tr>
<td><strong>Watchdog Input and Output</strong></td>
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</tr>
<tr>
<td>WDI logic high</td>
<td></td>
<td></td>
<td>3.2</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>WDI logic low</td>
<td></td>
<td></td>
<td>0.8</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>MODE logic high</td>
<td></td>
<td></td>
<td>3.2</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>MODE logic low</td>
<td></td>
<td></td>
<td>0.8</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>MODE input current</td>
<td>MODE = $5\text{V}$</td>
<td></td>
<td>0.1</td>
<td></td>
<td>1</td>
<td></td>
</tr>
<tr>
<td></td>
<td>MODE = $0\text{V}$</td>
<td></td>
<td>5</td>
<td></td>
<td>8</td>
<td></td>
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<tr>
<td>/WD_DIS logic high</td>
<td></td>
<td></td>
<td>3.2</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>/WD_DIS logic low</td>
<td></td>
<td></td>
<td>0.8</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>/WD_DIS input current</td>
<td>WD_DIS = $5\text{V}$</td>
<td></td>
<td>0.1</td>
<td></td>
<td>1</td>
<td></td>
</tr>
<tr>
<td></td>
<td>WD_DIS = $0\text{V}$</td>
<td></td>
<td>5</td>
<td></td>
<td>8</td>
<td></td>
</tr>
<tr>
<td>WDO high</td>
<td>$V_{\text{CC}} = 5\text{V}$, $I_{\text{WDO}} = 1\text{mA}$</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$V_{\text{CC}} = 1\text{V}$, $I_{\text{WDO}} = 300\text{µA}$</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>WDO low</td>
<td>$V_{\text{CC}} = 5\text{V}$, $I_{\text{WDO}} = 1\text{mA}$</td>
<td></td>
<td>0.2</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$V_{\text{CC}} = 1\text{V}$, $I_{\text{WDO}} = 300\text{µA}$</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**NOTE:**

6) Guaranteed by design.
TYPICAL CHARACTERISTICS
DC/DC Converter
$V_{\text{IN}} = 12V$, unless otherwise noted.

- Feedback Voltage vs. Junction Temperature
- Quiescent Current vs. Junction Temperature
- Shutdown Current vs. Junction Temperature
- Current Limit vs. Junction Temperature
- Switch On Resistance vs. Junction Temperature
- EN Threshold vs. Junction Temperature
- $V_{\text{IN}}$ UVLO vs. Junction Temperature
- $V_{\text{REF}}$ vs. Junction Temperature
- $I_{\text{SS}}$ vs. Junction Temperature
TYPICAL CHARACTERISTICS (continued)

Watchdog

- **Quiescent Current vs. Junction Temperature**
  - $R_{\text{TIMER}}=51\,k\Omega$

- **Quiescent Current vs. Junction Temperature**
  - $R_{\text{TIMER}}=100\,k\Omega$

- **Single Period vs. Junction Temperature**
  - $R_{\text{TIMER}}=51\,k\Omega$

- **Single Period vs. $R_{\text{TIMER}}$**
  - $T_{\text{A}}=25^\circ C$
TYPICAL PERFORMANCE CHARACTERISTICS

DC/DC Converter

$V_{IN} = 12V$, $V_{OUT} = 3.3V$, $L = 33\mu H$, $C_{OUT} = 2\times22\mu F$, $T_A = 25^\circ C$, unless otherwise noted.
Typical Performance Characteristics (continued)

Vin = 12V, Vout = 3.3V, L = 33µH, Cout = 2x22µF, Ta = 25°C, unless otherwise noted.

- Start-Up through EN
  - Iout = 0A
  - EN 2V/div.
  - Vout 2V/div.
  - 500mA/div.
  - SW 5V/div.
  - 1ms/div.

- Start-Up through EN
  - Iout = 0.3A
  - EN 2V/div.
  - Vout 2V/div.
  - 500mA/div.
  - SW 5V/div.
  - 10V/div.
  - 1ms/div.

- Shutdown through EN
  - Iout = 0A
  - EN 2V/div.
  - Vout 2V/div.
  - 500mA/div.
  - SW 5V/div.
  - 1ms/div.
  - 5V/div.
  - 2mA/div.

- Shutdown through EN
  - Iout = 0.3A
  - EN 2V/div.
  - Vout 2V/div.
  - 500mA/div.
  - SW 5V/div.
  - 200µs/div.

- SCP Entry
  - Iout = 0A to Short Circuit
  - EN 2V/div.
  - Vout 2V/div.
  - 500mA/div.
  - SW 5V/div.
  - 400µs/div.

- SCP Entry
  - Iout = 0.3A to Short Circuit
  - EN 2V/div.
  - Vout 2V/div.
  - 500mA/div.
  - SW 5V/div.
  - 200µs/div.

- SCP Steady State
  - Short Circuit to Iout = 0A
  - EN 2V/div.
  - Vout 2V/div.
  - 500mA/div.
  - SW 5V/div.
  - 40µs/div.

- SCP Recovery
  - Short Circuit to Iout = 0.3A
  - EN 2V/div.
  - Vout 2V/div.
  - 500mA/div.
  - SW 5V/div.
  - 400µs/div.
## PIN FUNCTIONS

<table>
<thead>
<tr>
<th>Pin #</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Watchdog</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>WDO</td>
<td><strong>Watchdog output.</strong> WDO outputs the reset signal to MCU.</td>
</tr>
<tr>
<td>2</td>
<td>WDI</td>
<td><strong>Watchdog input.</strong> WDI receives the trigger signal from MCU.</td>
</tr>
<tr>
<td>3</td>
<td>MODE</td>
<td><strong>Mode switching.</strong> Pull MODE high to make the watchdog work in a long window mode. Pull MODE low to make the watchdog work in a short window mode. MODE has a weak internal pull-up.</td>
</tr>
<tr>
<td>4</td>
<td>GND</td>
<td><strong>Ground.</strong> Connect GND as close as possible to the output capacitor to avoid high-current switch paths.</td>
</tr>
<tr>
<td>14</td>
<td>VCC</td>
<td><strong>Power input.</strong></td>
</tr>
<tr>
<td>15</td>
<td>TIMER</td>
<td><strong>Watchdog timer.</strong> Set the time out with an external resistor.</td>
</tr>
<tr>
<td>16</td>
<td>/WD_DIS</td>
<td><strong>Watchdog disable.</strong> Pull /WD_DIS low to disable the watchdog. Pull /WD_DIS high to enable the watchdog. /WD_DIS has a weak internal pull-up.</td>
</tr>
<tr>
<td><strong>DC/DC</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>GND</td>
<td><strong>Ground.</strong> Same as GND in Watchdog.</td>
</tr>
<tr>
<td>5</td>
<td>IN</td>
<td><strong>Input supply.</strong> IN requires a decoupling capacitor connected to ground to reduce switching spikes.</td>
</tr>
<tr>
<td>6</td>
<td>EN</td>
<td><strong>Enable input.</strong> Pull EN below the low threshold to shut the chip down. Pull EN above the high threshold to enable the chip. Float EN to disable the chip.</td>
</tr>
<tr>
<td>7</td>
<td>VREF</td>
<td><strong>Reference voltage output.</strong></td>
</tr>
<tr>
<td>8</td>
<td>FB</td>
<td><strong>Feedback input to the error amplifier (QFN-10 3mmx3mm package only).</strong> Connect FB to the tap of an external resistive divider between the output and GND. FB sets the regulation voltage when compared to the internal 1V reference.</td>
</tr>
<tr>
<td>9</td>
<td>SS</td>
<td><strong>Soft-start control input.</strong> Connect a capacitor from SS to GND to set the soft-start period.</td>
</tr>
<tr>
<td>10</td>
<td>POK</td>
<td><strong>Open-drain power-good output.</strong> A high output indicates that $V_{OUT}$ is higher than 90% of the reference. POK is pulled down during shutdown.</td>
</tr>
<tr>
<td>11</td>
<td>BIAS</td>
<td><strong>Controller bias input.</strong> BIAS supplies current to the internal circuit when $V_{BIAS}$ &gt; 2.9V and provides a feedback input for the SOIC8E package, which has a fixed output only.</td>
</tr>
<tr>
<td>12</td>
<td>BST</td>
<td><strong>Bootstrap.</strong> BST provides a positive power supply for the internal floating high-side MOSFET driver. Connect a bypass capacitor between BST and SW.</td>
</tr>
<tr>
<td>13</td>
<td>SW</td>
<td><strong>Switch node.</strong></td>
</tr>
<tr>
<td></td>
<td>Exposed Pad</td>
<td><strong>Connect exposed pad to GND plane for optimal thermal performance.</strong></td>
</tr>
</tbody>
</table>
FUNCTIONAL BLOCK DIAGRAM

Figure 1: Functional Block Diagram
DC/DC OPERATION

The MPQ2420 is a 75V, 0.3A, synchronous, step-down, switching regulator with integrated high-side and low-side, high-voltage power MOSFETs (HS-FET and LS-FET, respectively). It provides a highly efficient 0.3A output and features a wide input voltage range, external soft-start control, and precision current limit. It has a very low operational quiescent current, making it suitable for battery-powered applications.

Control Scheme

The ILIM comparator, FB comparator, and zero current detector (ZCD) block control of the PWM (see Figure 2). If $V_{FB}$ is below the 1V reference and the inductor current drops to zero, the HS-FET turns on, and the ILIM comparator begins sensing the HS-FET current. When the HS-FET current reaches its limit, the HS-FET turns off, and the LS-FET and the ZCD block turn on. The ILIM comparator turns off to reduce the quiescent current. The LS-FET and the ZCD block turn off after the inductor current drops to zero. If $V_{FB}$ is below the 1V reference, the HS-FET turns on and begins another cycle. If $V_{FB}$ remains higher than the 1V reference, the HS-FET remains off until $V_{FB}$ drops below 1V.

![Figure 2: Control Scheme](image)

Internal Regulator and BIAS

The 2.6V internal regulator powers most of the internal circuitry. This regulator takes $V_{IN}$ and operates in the full $V_{IN}$ range. When $V_{IN}$ is greater than 3.0V, the output of the regulator is in full regulation. Lower values of $V_{IN}$ result in lower output voltages. When $V_{BIAS}$ > 2.9V, the BIAS supply overrides the input voltage and supplies power to the internal regulator. When $V_{BIAS}$ > 4.5V, BIAS powers the LS-FET driver. Using BIAS to power the internal regulators improves efficiency. It is recommended to connect BIAS to the regulated output voltage when it is in the 2.9V to 5.5V range. When the output voltage is out of this range, BIAS can be powered using an external supply of >2.9V to >4.5V.

Enable Control (EN)

The MPQ2420 has a dedicated enable control (EN). When $V_{IN}$ goes high, EN enables and disables the chip (high logic). Its falling threshold is a consistent 1.2V, and its rising threshold is about 350mV. When floating, EN is pulled down internally to GND to disable the chip.

When $EN = 0V$, the chip enters the lowest shutdown current mode. When EN is higher than zero, but lower than its rising threshold, the chip remains in shutdown mode with a slightly larger shutdown current.

A Zener diode is connected internally from EN to GND. The typical clamping voltage of the Zener diode is 6.5V. $V_{IN}$ can be connected to EN through a high ohm (Ω) resistor if the system does not have another logic input acting as an EN signal. The resistor must be designed to limit the EN sink current to less than 150μA. Since there is an internal 3M resistor from EN to GND, the external pull-up resistor should be smaller than $\frac{[V_{IN(MIN)} - 1.55V] \times 3M}{1.55V}$ to ensure that EN can turn on at the lowest operational $V_{IN}$. 

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Under-Voltage Lockout (UVLO)
Under-voltage lockout (UVLO) protects the chip from operating below the operational supply voltage range. The UVLO rising threshold is about 4.2V while its falling threshold is about 3.75V.

Soft Start (SS)
The MPQ2420 employs a soft-start (SS) mechanism to prevent the converter output voltage from overshooting during start-up. When the chip starts, the internal circuitry generates a constant current to charge an external soft-start capacitor. The SS voltage ramps up slowly from 0V at a slow pace set by the SS time. When \(V_{SS}\) is less than \(V_{REF}\), \(V_{SS}\) overrides \(V_{REF}\), and the FB comparator uses \(V_{SS}\) as the reference instead of \(V_{REF}\). When \(V_{SS}\) is higher than \(V_{REF}\), \(V_{REF}\) resumes control.

\(V_{SS}\) can be much smaller than \(V_{FB}\), but it can only barely exceed \(V_{FB}\). If \(V_{FB}\) drops, \(V_{SS}\) tracks \(V_{FB}\). This function prevents an output voltage overshoot during short-circuit recovery. When the short circuit is removed, a new SS process ramps up.

Thermal Shutdown
Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the silicon die reaches temperatures that exceed its upper threshold, the entire chip shuts down. When the temperature falls below its lower threshold, the chip is enabled again.

Floating Driver and Bootstrap Charging
An external bootstrap capacitor powers the floating HS-FET driver. This floating driver has its own UVLO protection. This UVLO’s rising threshold is about 2.4V with a hysteresis of about 300mV. During the UVLO, the SS voltage resets to zero. When the UVLO is disabled, the regulator follows the soft-start process.

The dedicated internal bootstrap regulator charges and regulates the bootstrap capacitor to about 5V. When the voltage difference between BST and SW falls below its working parameters, a PMOS pass transistor connected from \(V_{IN}\) to BST turns on to charge the bootstrap capacitor. The current path runs from \(V_{IN}\) to BST to SW. The external circuit must have enough voltage headroom to accommodate charging.

If \(V_{IN}\) is sufficiently higher than SW, the bootstrap capacitor charges. When the HS-FET is on, \(V_{IN}\) is about equal to SW, and the bootstrap capacitor cannot charge. The optimal charging period occurs when the LS-FET is on and \(V_{IN} - V_{SW}\) is at its largest. \(V_{SW}\) is equal to \(V_{OUT}\) when there is no current in the inductor. The difference between \(V_{IN}\) and \(V_{OUT}\) charges the bootstrap capacitor.

If the internal circuit does not have sufficient voltage and time to charge the bootstrap capacitor, extra external circuitry can be used to ensure that the bootstrap voltage operates in its normal region.

Start-Up and Shutdown
If both \(V_{IN}\) and \(V_{EN}\) are higher than their appropriate thresholds, the chip starts up. The reference block starts first, generating stable reference voltages and currents, and then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuitries.

If the internal supply rail is high, an internal timer keeps the power MOSFET off for about 50µs to clear any start-up glitches. When the soft-start block is enabled, the SS output is held low and ramps up slowly.

Three events can shut down the chip: \(V_{EN}\) low, \(V_{IN}\) low, and thermal shutdown. During the shutdown procedure, the signaling path is blocked first to avoid any fault triggering. The internal supply rail is then pulled down. The floating driver is not subject to this shutdown command, but its charging path is disabled.

Power OK (POK)
POK is an open-drain power good output. A high output indicates that \(V_{OUT}\) is higher than 90% of its nominal value. POK is pulled down in shutdown mode.

Reference Voltage Output (\(V_{REF}\))
\(V_{REF}\) has an output reference voltage of 1V. It has up to 500µA of source current capability.
WATCHDOG OPERATION

Supply Voltage
A supply voltage of $V_{CC} = 5V \pm 10\%$ is recommended for normal operation. WDO is pulled low when $V_{CC}$ rises to 1V or higher. When $V_{CC}$ rises to 4.65V, WDO remains at a low level for $t_0$ to reset the MCU.

Timer
Calculate Period $T$ ($\mu$s) with Equation (1):

$$T(\mu s) = 15.75 \times R_{\text{TIMER}} (k\Omega) + 73.5 \quad (1)$$

Calculate $R_{\text{TIMER}}$ ($k\Omega$) with Equation (2):

$$R_{\text{TIMER}} (k\Omega) = 0.063 \times T(\mu s) - 4.67 \quad (2)$$

For example, if $R_{\text{TIMER}}=51k\Omega$, then $T=0.88ms$.

Monitor MCU Synchronization Signal
When the watchdog is in a sync signal monitoring state, the watchdog IC receives a WDI_OK signal from the MCU within $t_0$, the timer resets and the watchdog enters normal operation ($WDI$ remains low for 10$\mu$s to 5ms). If the watchdog does not receive the WDI_OK signal from the MCU during $t_0$, it generates a reset signal and enters the sync signal monitoring state again.

Short Window Mode
When the MCU and watchdog are synchronized correctly and MODE is low, the watchdog operates in short window mode if WDI_OK is received in a window close state ($t_2$). The watchdog then outputs a reset signal and enters the sync signal monitoring state.

If WDI_OK is received in a window open state ($t_3$), the watchdog enters a window close state. The MCU is in normal operation in this situation.

If WDI_OK is not received in $t_2+t_3$, the watchdog outputs a reset signal and enters the sync signal monitoring state.

MODE is pulled high during the short window mode, and the watchdog enters a long window mode.

Long Window Mode
When the MCU and watchdog are synchronized correctly and MODE is high, the watchdog works in a long window mode if WDI_OK is received in a window close state ($t_4$). The watchdog then outputs a reset signal and enters the sync signal monitoring state.

If WDI_OK is received in a window open state ($t_5$), the watchdog enters a window close state. The MCU is in normal operation in this situation.

If WDI_OK is not received in $t_4+t_5$, the watchdog then outputs a reset signal and enters the sync signal monitoring state.

MODE is pulled low during a long window mode, and the watchdog then enters a short window mode.

Watchdog Disable
Pull /WD_DIS low to disable the watchdog. Pull /WD_DIS high to enable the watchdog. It has a weak internal pull-up so leaving /WD_DIS open enables the watchdog.

WDI Error
The WDI signal remaining at a low level for longer than the max WDI_OK pulse width is regarded as an error. When this error occurs, WDO is pulled down until WDI rises to a high level again.
TIMING DIAGRAM

Power-On Reset and No-Sync Signal

VCC = 1V  VCC = 90%

Synchronized by WDI and Triggered in Open Window (MODE=0, Short Window Mode)

Synchronized by WDI and No-Trigger Signal (MODE=0, Short Window Mode)
NOTE: When the WDI_OK rising edge approaches WDO when it is low, the $t_6$ timer resets. In the above situation, the WDO reset signal keeps a $t_6 + \text{WDI}_\text{OK}$ time.
NOTE: When the WDI_OK rising edge approaches WDO when it is low, the $t_6$ timer resets. In the above situation, the WDO reset signal keeps a $t_6 + WDI\_OK$ time.
STATE DIAGRAM

NOTE: The above state diagram does not show a WDI error situation.
APPLICATION INFORMATION

Selecting the Inductor
The $I_{\text{peak}}$ is fixed, and the inductor value can be determined with Equation (3):

$$L = \frac{V_{\text{OUT}}}{{V_{\text{IN}}} - V_{\text{OUT}}} \times \frac{{I_{\text{peak}}}}{f_s}$$

Where $f_s$ is the switching frequency at the maximum output current.

A larger inductor value results in a lower switching frequency and higher efficiency. However, the larger value inductor has a larger physical size, a higher series resistance, a lower saturation current, and/or a slow load transient dynamic performance. The inductor value has a lower limit, which is determined by the minimum on time. To keep the inductor functioning properly, choose an inductor value that is higher than $L_{\text{MIN}}$, which is derived from Equation (4):

$$L_{\text{MIN}} = \frac{V_{\text{IN(MAX)}}}{I_{\text{peak}}} \times t_{\text{ON(MIN)}}$$

Where $V_{\text{IN(MAX)}}$ is the maximum value of the input voltage, and $t_{\text{ON(MIN)}}$ is the 115ns minimum switch on time.

Switching Frequency
The switching frequency can be estimated with Equation (5):

$$f_s = 2 \times \frac{\log \left( \frac{V_{\text{OUT}}}{{V_{\text{IN}}} - V_{\text{OUT}}} \right)}{I_{\text{peak}}}$$

A larger inductor can produce a lower $f_s$. $f_s$ increases as $I_{\text{LO}}$ increases. When $I_{\text{LO}}$ increases to its maximum value $I_{\text{peak}}/2$, $f_s$ also reaches its highest value. The maximum $f_s$ value can be estimated with Equation (6):

$$f_{s(MAX)} = 2 \times \frac{\log \left( \frac{V_{\text{OUT}}}{{V_{\text{IN}}} - V_{\text{OUT}}} \right)}{I_{\text{peak}}}$$

Setting the Output Voltage
The output voltage is set using a resistive voltage divider from the output voltage to FB. To achieve the desired output voltage, select a resistor divider using Equation (7):

$$\frac{R1}{R2} = \frac{V_{\text{OUT}}}{{V_{\text{REF}}} - 1}$$

Where $V_{\text{REF}}$ is the FB reference voltage 1V.

The current flowing into the resistor divider increases the supply current, especially at no-load and light-load conditions. The $V_{\text{IN}}$ supply current caused by the feedback resistors can be calculated with Equation (8):

$$I_{\text{IN,FB}} = \frac{V_{\text{OUT}}}{{R1 + R2}} \times \frac{V_{\text{OUT}}}{{V_{\text{IN}}} - 1} \times \frac{1}{\eta}$$

Where $\eta$ is the efficiency of the regulator.

To reduce this current, resistors in the MΩ range are recommended. The recommended value of the feedback resistors are shown in Table 1.

Table 1: Resistor Selection for Common Output Voltages

<table>
<thead>
<tr>
<th>$V_{\text{OUT}}$ (V)</th>
<th>$R1$ (kΩ)</th>
<th>$R2$ (kΩ)</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.3</td>
<td>1200</td>
<td>523</td>
</tr>
<tr>
<td>5</td>
<td>1200</td>
<td>300</td>
</tr>
</tbody>
</table>

Under-Voltage Lockout Point Setting
The MPQ2420 has an internal fixed under-voltage lockout (UVLO) threshold. The rising threshold is about 4.2V while the falling threshold is about 3.75V. An external resistor divider between EN and $V_{\text{IN}}$ can be used to obtain a higher equivalent UVLO threshold (see Figure 3).

Figure 3: Adjustable UVLO Using EN

The UVLO threshold can be calculated with Equation (9) and Equation (10):

$$\text{UVLO}_{\text{TH,Rising}} = (1 + \frac{\text{R4}}{3\text{M}/\text{R5}}) \times \text{EN}_{\text{TH,Rising}}$$

$$\text{UVLO}_{\text{TH,Falling}} = (1 + \frac{\text{R4}}{3\text{M}/\text{R5}}) \times \text{EN}_{\text{TH,Falling}}$$
Soft-Start Capacitor
The soft-start time is the duration of an internal 5μA current source charging the SS capacitor from 0 to the FB reference voltage (1V). The SS capacitor value can be determined with Equation (11):

$$C_{ss} = 5 \times t_{ss} \, (\mu F)$$ (11)

Feed-Forward Capacitor
The HS-FET turns on when FB drops below the reference voltage, producing good load transient performance. However, this also causes the HS-FET to be sensitive to the FB voltage during turn-on. The HS-FET is easily affected by FB noise at turn-on, which can trigger a Fsw jitter. Fsw jitter occurs most often when the Vo ripple is very small. To improve jitter performance, it is recommended to use a small feed-forward capacitor of about 39pF between Vo and FB.
TYPICAL APPLICATION CIRCUITS

Figure 4: 3.3V Output Typical Application Circuit
PACKAGE INFORMATION

TSSOP-16 EP

NOTE:
1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING CONFORMS TO JEDEC MO-153, VARIATION ABT.
6) DRAWING IS NOT TO SCALE.

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