MPQ2325

24V, 3A, 500kHz, High-Efficiency, Synchronous, Step-Down Converter

The Future of Analog IC Technology

DESCRIPTION

The MPQ2325 is a high-frequency, synchronous, rectified, step-down, switch-mode converter with built-in, internal power MOSFETs. It offers a very compact solution that achieves 3A of continuous output current with excellent load and line regulation over a wide input supply range. The MPQ2325 uses synchronous mode operation for higher efficiency over the output current load range.

Current mode operation provides a fast transient response and eases loop stabilization.

Full protection features include over-current protection (OCP) and thermal shutdown.

The MPQ2325 requires a minimal number of readily available, standard, external components and is available in a space-saving, 8-pin, TSOT23 package.

FEATURES

- Wide 4.5V to 24V Operating Input Range
- 90mΩ/40mΩ Low $R_{DS(ON)}$ Internal Power MOSFETs
- Low Quiescent Current
- High-Efficiency Synchronous Mode Operation
- Fixed 500kHz Switching Frequency
- Frequency Sync from 200kHz to 2MHz External Clock
- Power-Save Mode at Light Load
- Internal Soft Start
- Power Good Indicator
- Over-Current Protection (OCP) and Hiccup
- Thermal Shutdown
- Output Adjustable from 0.8V
- Available in a TSOT23-8 Package

APPLICATIONS

- Notebook Systems and I/O Power
- Digital Set-Top Boxes
- Flat-Panel Televisions and Monitors

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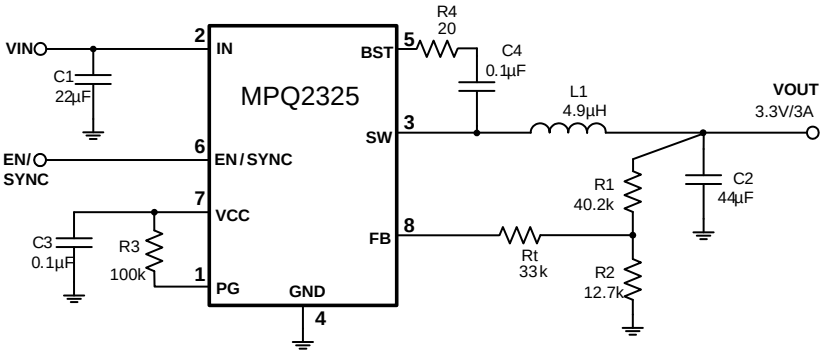
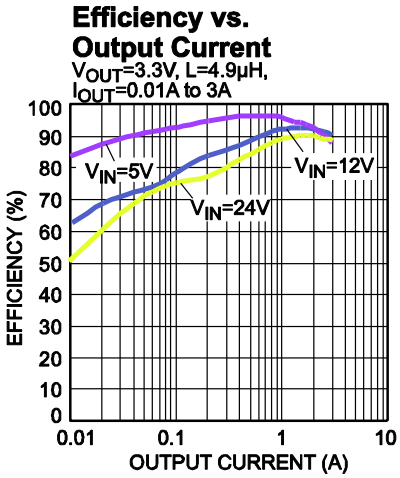
TYPICAL APPLICATION





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ORDERING INFORMATION

Part Number*	Package	Top Marking
MPQ2325GJ	TSOT23-8	*See Below*

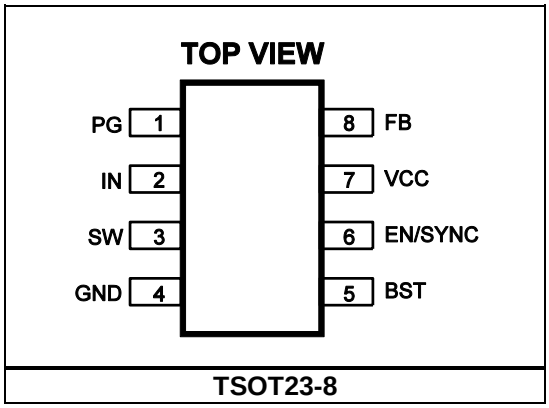
* For Tape & Reel, add suffix –Z (e.g. MPQ2325GJ–Z)

TOP MARKING

|AKEY

AKE: Product code of MPQ2325GJ
Y: Year code

PACKAGE REFERENCE



TSOT23-8

ABSOLUTE MAXIMUM RATINGS (1)

V_{IN} ..... -0.3V to +28V
V_{SW} .... -0.3V (-5V < 10ns) to +28V (30V < 10ns)
V_{BST} ..... +6V
All other pins ..... -0.3V to +6V
Continuous power dissipation (T_A = +25°C) (2) 1.25W
Junction temperature ..... 150°C
Lead temperature ..... 260°C
Storage temperature ..... -65°C to 150°C

Recommended Operating Conditions

Supply voltage (V_{IN}) ..... 4.5 to 24V
Output voltage (V_{OUT}) ..... 0.8V to V_{IN}*D_{MAX}
Operating junction temp (T_J). ... -40°C to +125°C

Thermal Resistance (3) θ_{JA} θ_{JC}

TSOT23-8 ..... 100 ..... 55 ... °C/W

NOTES:

1) The absolute maximum is rated under room temperature unless otherwise noted. Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the device to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_J = 25°C.

Parameter	Symbol	Condition		Min	Typ	Max	Units
Supply current (shutdown)	I_{IN}	V_{EN} = 0V	T_J = 25°C		5.5		µA
			T_J = -40°C to +125°C			20	
Supply current (quiescent)	I_q	V_{EN} = 2V, V_{FB} = 1V		130	180	240	µA
HS switch on resistance	HS_{RDS-ON}	V_{BST-SW} = 5V			90		mΩ
LS switch on resistance	LS_{RDS-ON}	V_{CC} = 5V			40		mΩ
Switch leakage	SW_{LKG}	V_{EN} = 0V, V_{SW} = 12V				1	µA
Current limit (5)	I_{LIMIT}	Duty cycle = 40%		4.5	6		A
Oscillator frequency	f_{SW}	V_{FB} = 750mV	T_J = 25°C	420	500	620	kHz
			T_J = -40°C to +125°C	380		620	
Foldback frequency	f_{FB}	V_{FB} = 200mV			0.5		f_{SW}
Maximum duty cycle	D_{MAX}	V_{FB} = 750mV		90	95		%
Minimum on time (5)	T_{ON_MIN}				60		ns
Sync frequency range	f_{SYNC}			0.2		2	MHz
Feedback voltage	V_{FB}	T_J = 25°C		779	791	803	mV
		T_J = -40°C to +125°C		775		807	
Feedback current	I_{FB}	V_{FB} = 820mV			10	50	nA
EN rising threshold	V_{EN_RISING}	T_J = 25°C		1.2	1.4	1.6	V
		T_J = -40°C to +125°C		1.1		1.7	
EN hysteresis	V_{EN_HYS}				150		mV
EN input current	I_{EN}	V_{EN} = 2V	T_J = 25°C	1.8	2.3	2.8	µA
			T_J = -40°C to +125°C	1.6		3	
		V_{EN} = 0	T_J = 25°C			50	nA
			T_J = -40°C to +125°C			100	
EN turn-off delay	EN_{Td-off}			6	10	14	µs
Power good rising threshold	PG_{VTH-Hi}				0.9		V_{FB}
Power good falling threshold	PG_{VTH-LO}				0.85		V_{FB}
Power good delay	PG_{Td}				40		µs
Power good sink current capability	V_{PG}	Sink 1mA				0.4	V
Power good leakage current	$I_{PG-LEAK}$					1	µA
VIN under-voltage lockout threshold rising	$INUV_{Vth}$	T_J = 25°C		3.7	3.9	4.1	V
		T_J = -40°C to +125°C		3.6		4.2	
VIN under-voltage lockout threshold hysteresis	$INUV_{HYS}$				650		mV
VCC regulator	V_{CC}	T_J = 25°C		4.65	4.9	5.15	V
		T_J = -40°C to +125°C		4.6		5.2	
VCC load regulation		I_{CC} = 5mA			1	3	%

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_J = 25°C.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Soft-start period	T_{SS}	T_J = 25°C	0.8	1.6	2.4	ms
		T_J = -40°C to +125°C	0.5		2.7	
Thermal shutdown(4)				150		°C
Thermal hysteresis(4)				20		°C

NOTES:

4) Derived from bench characterization.
5) Guaranteed by design.

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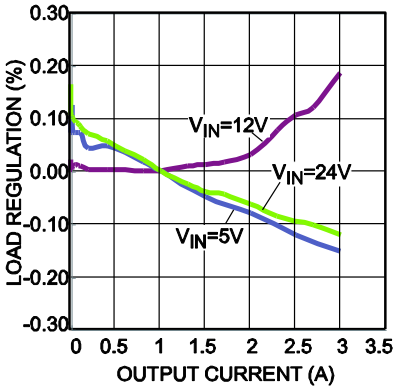
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.9µH, T_A = 25°C, unless otherwise noted.

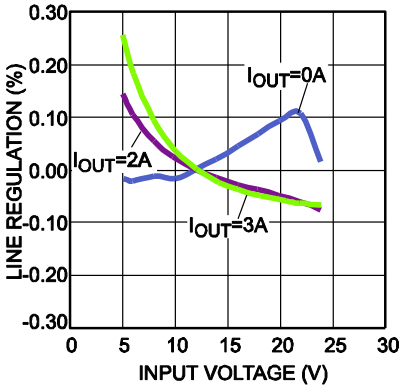
Load Regulation

V_{IN}=5V to 24V, I_{OUT}=0.1A to 3A

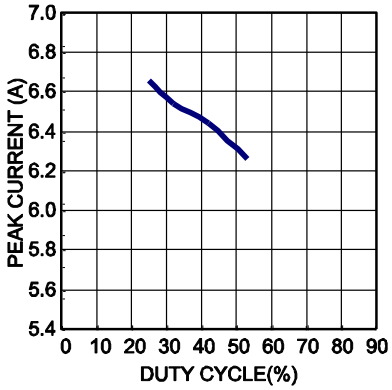


Line Regulation

V_{IN}=5V to 24V

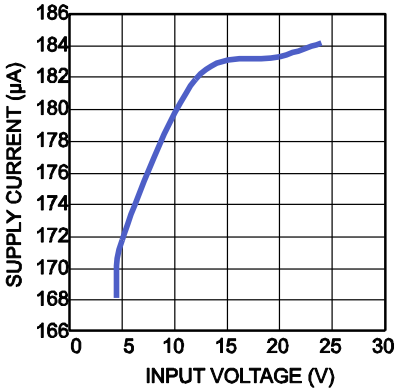


Peak Current vs. Duty Cycle



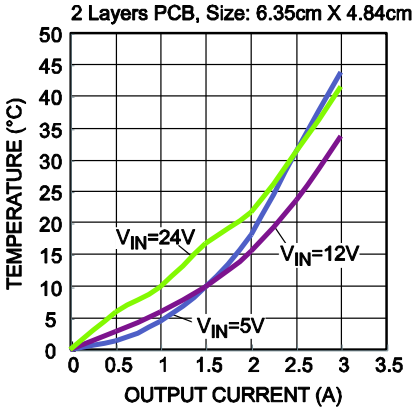
Enabled Supply Current vs. Input Voltage

V_{IN}=4.5V to 24V, EN=5V



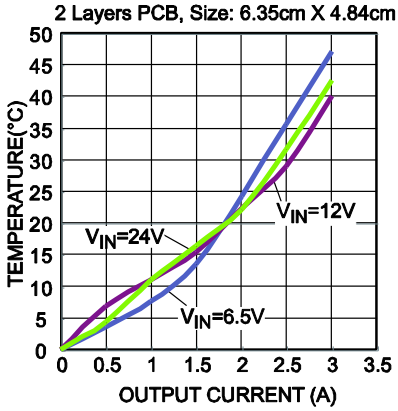
Case Temperature Rise vs. Output Current

V_{OUT}=3.3V, I_{OUT}=0 to 3A
2 Layers PCB, Size: 6.35cm X 4.84cm



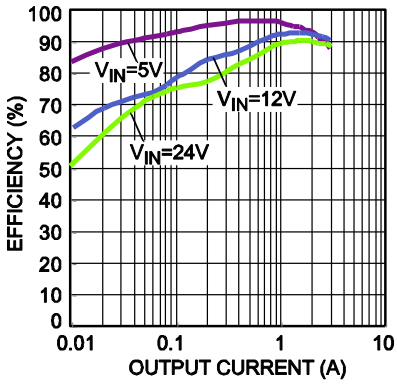
Case Temperature Rise vs. Output Current

V_{OUT}=5V, I_{OUT}=0 to 3A,
2 Layers PCB, Size: 6.35cm X 4.84cm



Efficiency vs. Output Current

I_{OUT}=0.01A to 3A



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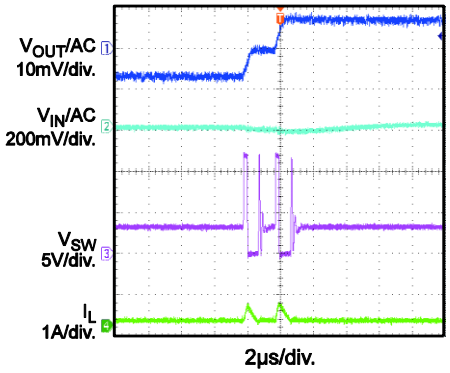
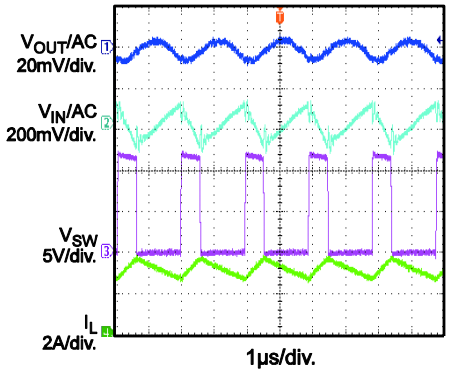
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.9µH, T_A = 25°C, unless otherwise noted.

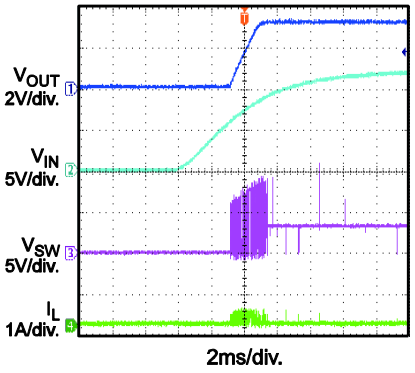
Input/Output Ripple
I_{OUT}= 0A



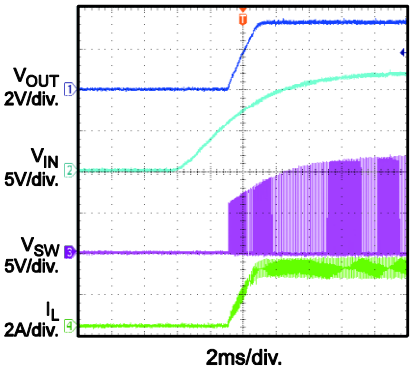
Input/Output Ripple
I_{OUT}= 3A



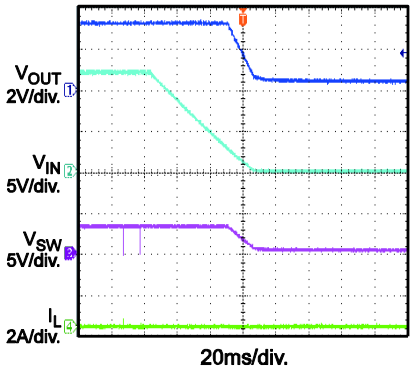
V_{IN} Start-Up
I_{OUT}= 0A



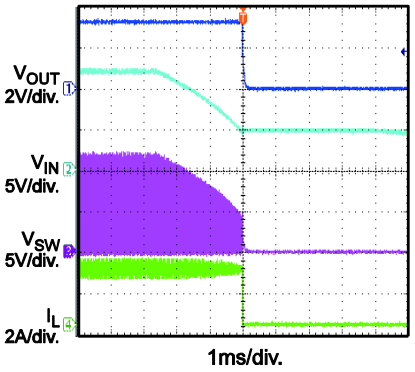
V_{IN} Start-Up
I_{OUT}= 3A



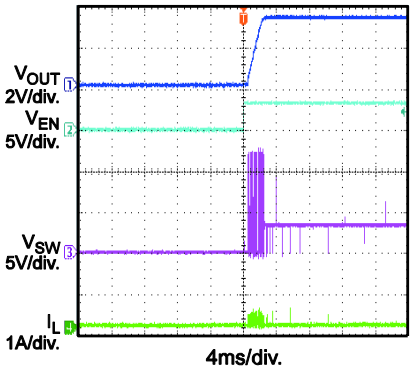
V_{IN} Shutdown
I_{OUT}= 0A



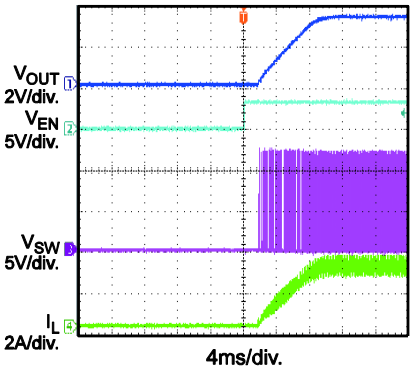
V_{IN} Shutdown
I_{OUT}= 3A



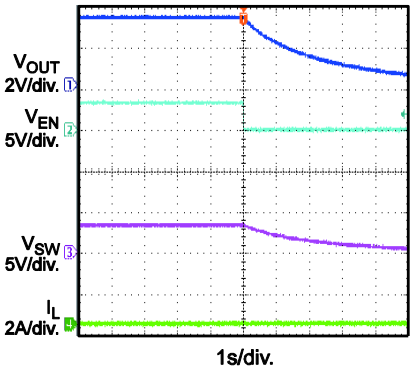
EN Start-Up
I_{OUT}= 0A



EN Start-Up
I_{OUT}= 3A



EN Shutdown
I_{OUT}= 0A



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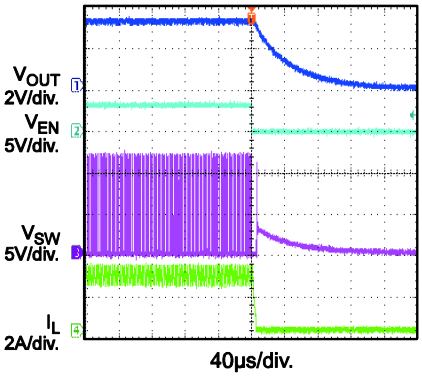
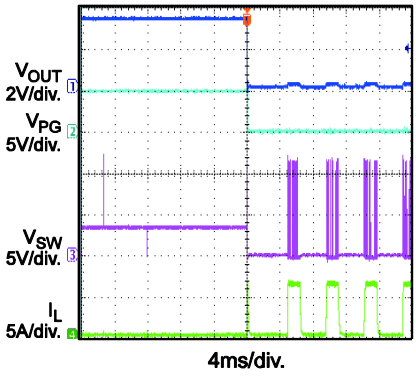
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.9µH, T_A = 25°C, unless otherwise noted.

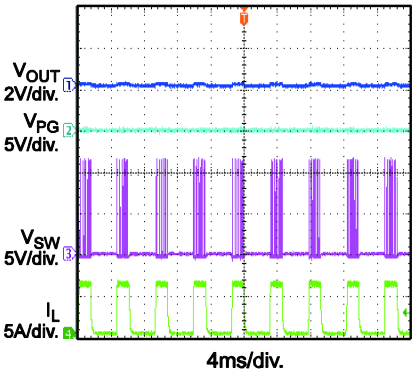
EN Shutdown
I_{OUT}= 3A



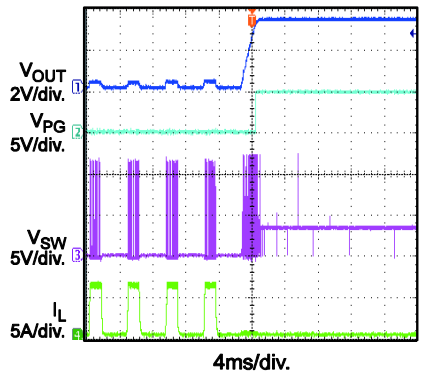
Short-Circuit Entry



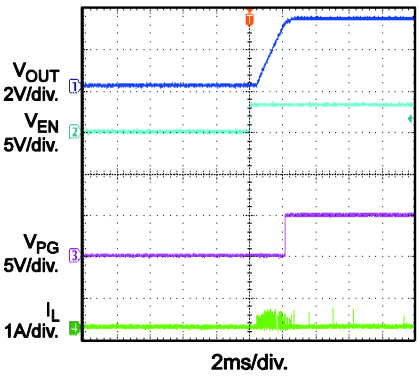
Short Circuit



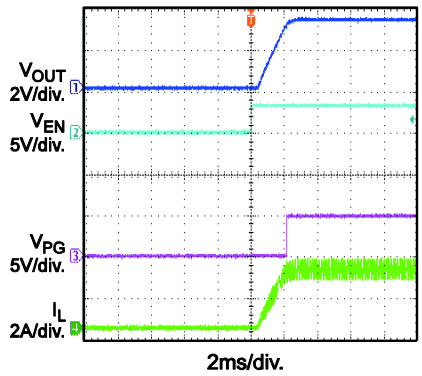
Short-Circuit Recovery



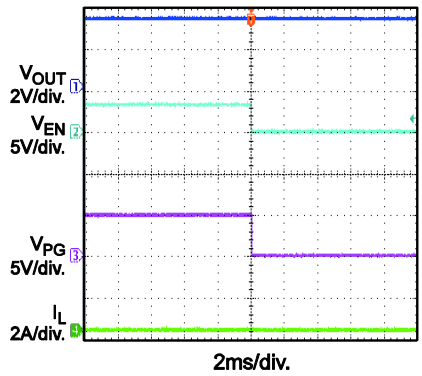
EN Start-Up (PG)
I_{OUT}= 0A



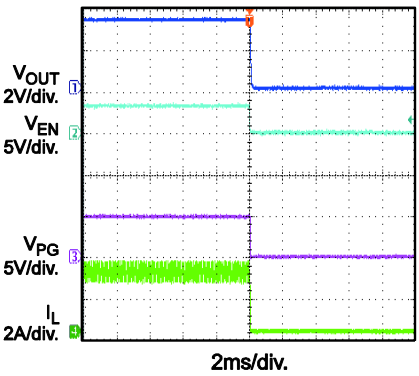
EN Start-Up (PG)
I_{OUT}= 3A



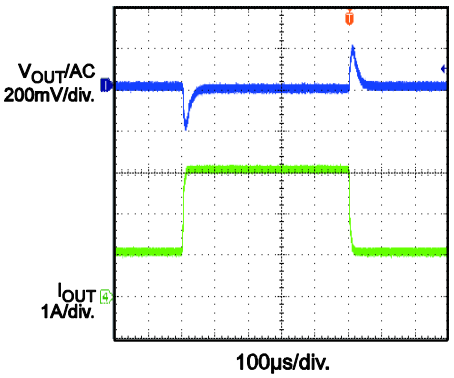
EN Shutdown(PG)
I_{OUT}= 0A



EN Shutdown(PG)
I_{OUT}= 3A



Load Transient Response
I_{OUT}= 1A to 3A



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PIN FUNCTIONS

Package Pin #	Name	Description
1	PG	**Power good output.** The output of PG is an open drain. PG is pulled up to VCC by an external resistor when the output voltage exceeds 90% of the normal voltage. There is a 40µs delay between the time when FB becomes greater than or equal to 90% and PG rises high.
2	IN	**Supply voltage.** IN supplies power for the internal MOSFET and regulator. The MPQ2325 operates from a +4.5V to +24V input rail. IN requires a low ESR and low inductance capacitor (C1) to decouple the input rail. Place the input capacitor very close to IN, and connect it with wide PCB traces and multiple vias.
3	SW	**Switch output.** Connect SW to the inductor and bootstrap capacitor. SW is driven up to VIN by the high-side switch during the PWM duty cycle on time. The inductor current drives SW negative during the off time. The on resistance of the low-side switch and the internal body diode fixes the negative voltage. Connect SW using wide PCB traces and multiple vias.
4	GND	**System ground.** GND is the reference ground of the regulated output voltage. GND requires special consideration during PCB layout. For best results, connect GND with copper traces and vias.
5	BST	**Bootstrap.** A capacitor and a 20Ω resistor connected between SW and BST are required to form a floating supply across the high-side switch driver.
6	EN/SYNC	**Enable/sync.** Set EN/SYNC = 1 to enable the MPQ2325. An external clock can be applied to EN/SYNC to change the switching frequency. For automatic start-up, connect EN/SYNC to V_{IN} with a 100kΩ resistor.
7	VCC	**Bias supply.** Decouple VCC with a 0.1µF - 0.22µF capacitor. The capacitance should not exceed 0.22µF.
8	FB	**Feedback.** An external resistor divider from the output to GND tapped to FB sets the output voltage. To prevent current limit runaway during a short-circuit fault condition, the frequency foldback comparator lowers the oscillator frequency when the FB voltage is below 400mV.

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BLOCK DIAGRAM

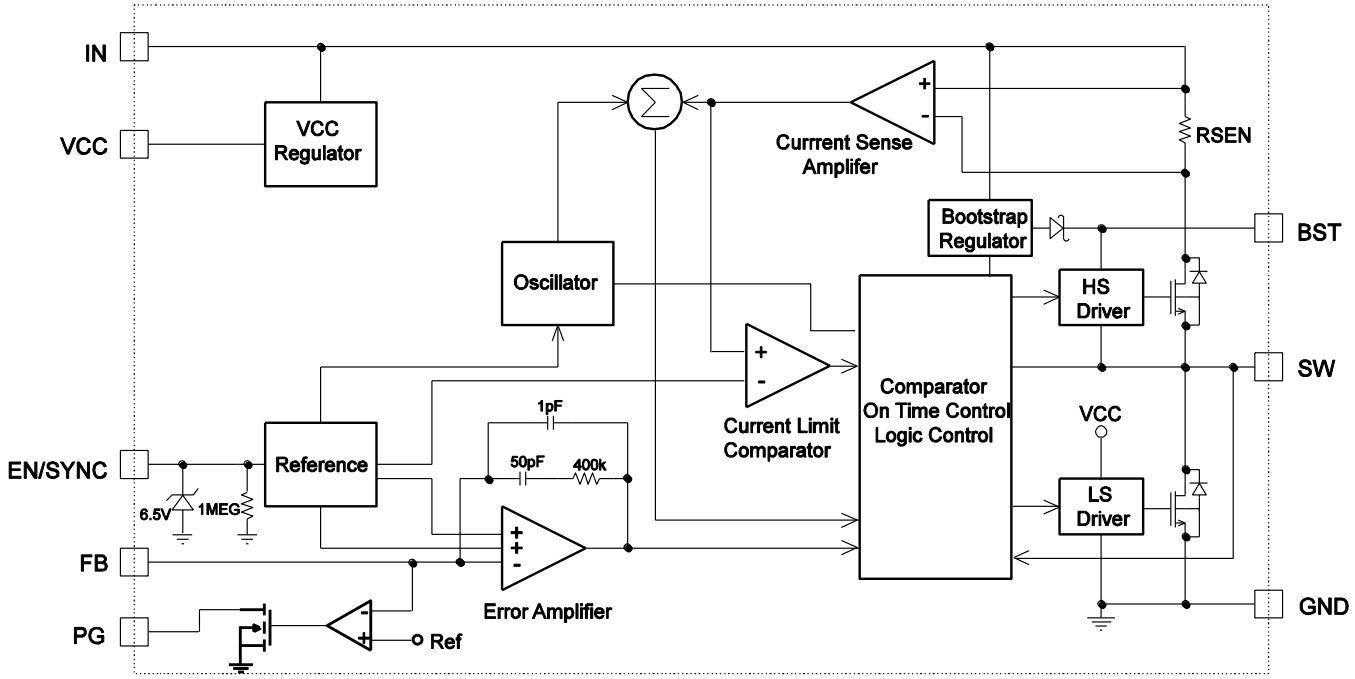

Figure 1: Functional Block Diagram

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OPERATION

The MPQ2325 is a high-frequency, synchronous, rectified, step-down, switch mode converter with built-in, internal power MOSFETs. The MPQ2325 offers a very compact solution that achieves 3A of continuous output current with excellent load and line regulation over a wide input supply range.

The MPQ2325 operates in a fixed-frequency, peak-current-control mode to regulate the output voltage. A PWM cycle is initiated by the internal clock. The integrated high-side power MOSFET is turned on and remains on until its current reaches the value set by the COMP voltage (V_{COMP}). When the power switch is off, it remains off until the next clock cycle starts. If the current in the power MOSFET does not reach the COMP-set current value within 95% of one PWM period, the power MOSFET is forced off.

Internal Regulator

Most of the internal circuitries are powered from the 5V internal regulator. This regulator takes the VIN input and operates in the full VIN range. When VIN is greater than 5.0V, the output of the regulator is in full regulation. When VIN is lower than 5.0V, the output decreases. A 0.1µF ceramic capacitor is required for decoupling.

Error Amplifier (EA)

The error amplifier compares the FB voltage with the internal 0.8V reference (REF) and outputs a COMP voltage, which is used to control the power MOSFET current. The optimized internal compensation network minimizes the external component count and simplifies the control loop design.

Power Save Mode for Light-Load Condition

The MPQ2325 uses advanced asynchronous modulation (AAM) power-save mode for light load (see Figure 2). Under heavy-load condition, V_{COMP} is higher than V_{AAM}. When the clock goes high, the high-side power MOSFET turns on and remains on until $V_{ILsense}$ reaches the value set by V_{COMP}. The internal clock resets whenever V_{COMP} is higher than V_{AAM}.

Under light-load condition, the value of V_{COMP} is low. When V_{COMP} is less than V_{AAM}, and V_{FB} is less than V_{REF}, V_{COMP} ramps up until it exceeds V_{AAM}. During this time, the internal clock is blocked, so the MPQ2325 skips some pulses for pulse-frequency modulation (PFM) mode and achieves a light-load power save.

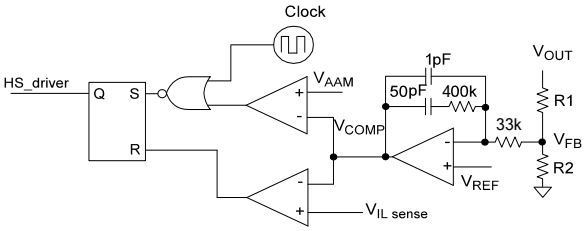

Figure 2: Simplified AAM Control Logic

For V_{IN} = 12V, V_{OUT} = 3.3V, and L = 4.9µH, the inductor peak current set internally is about 500mA at light load. The AAM voltage is varied with the duty cycle internally to keep the inductor peak current constant.

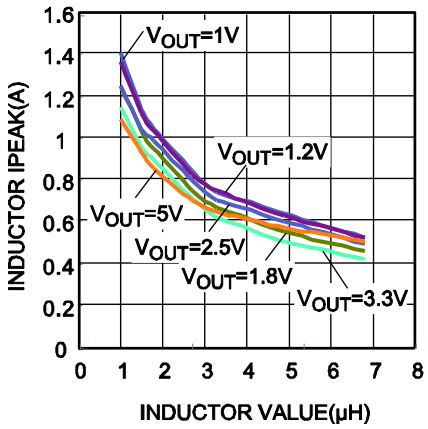

Figure 3: AAM Selection for Common Output Voltages (V_{IN} = 4.5V - 24V)

Enable/SYNC Control (EN/SYNC)

EN/SYNC is a digital control pin that turns the regulator on and off. Drive EN/SYNC high to turn on the regulator; drive EN/SYNC low to turn off the regulator. There is an internal 1MΩ resistor from EN/SYNC to GND, so EN/SYNC can be floated to shut down the chip. The EN/SYNC voltage is clamped at around 6.5V by an internal Zener diode. The pull-up resistor connecting V_{IN} and EN/SYNC should be large enough to limit the EN/SYNC input current below 100µA. Generally, a resistor around 100kΩ should be sufficient for all applications.

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The chip can be synchronized to the external clock range from 200kHz up to 2MHz through EN/SYNC about 2ms after the output voltage is set with the internal clock rising edge synchronized to the external clock rising edge. The EN/SYNC synchronized logic high voltage should be higher than 2V. The EN/SYNC synchronized logic low voltage should be lower than 400mV. The EN/SYNC logic high pulse width must be less than 1.6µs; otherwise, the internal clock may turn on the high-side MOSFET. The EN/SYNC logic low pulse width must be less than 6µs; otherwise, the MPQ2325 may enter EN/SYNC shutdown.

Power Good (PG) Indicator

The MPQ2325 has an open-drain pin for power good indication (PG). When FB is higher than 90% of the regulation voltage, PG is pulled up to VCC by an external resistor. If the FB voltage drops down to 85% of the regulation voltage, PG is pulled down to ground by an internal MOSFET.

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) is implemented to protect the MPQ2325 from operating at an insufficient supply voltage. The MPQ2325 UVLO comparator monitors the output voltage of the internal regulator (VCC). The UVLO rising threshold is about 3.9V, while its falling threshold is a consistent 3.25V.

Internal Soft Start (SS)

Soft start (SS) is implemented to prevent the converter output voltage from overshooting during start-up. When the chip starts up, the internal circuitry generates a soft-start voltage that ramps up from 0V. The soft-start period lasts until the voltage on the soft-start capacitor exceeds the reference voltage of 0.8V. At this point, the reference voltage takes over. The soft-start time is set to around 1.5ms internally.

Over-Current Protection (OCP) and Hiccup

The MPQ2325 uses a cycle-by-cycle over-current limit when the inductor current peak value exceeds the set current limit threshold. Meanwhile, the output voltage begins dropping until FB is below the under-voltage (UV) threshold, typically 50% below the reference. Once UV is triggered, the MPQ2325 enters hiccup mode to restart the part periodically. This protection mode is especially useful when the output is dead shorted to ground. The average short-circuit current is reduced greatly to alleviate thermal issues and protect the regulator. The MPQ2325 exits hiccup mode once the over-current condition is removed.

Thermal Shutdown

Thermal shutdown is implemented to prevent the chip from operating at exceedingly high temperatures. When the silicon die temperature is higher than 150°C, the entire chip shuts down. When the temperature is lower than its lower threshold (typically 130°C), the chip is enabled again.

Floating Driver and Bootstrap Charging

The floating power MOSFET driver is powered by an external bootstrap capacitor. This floating driver has its own UVLO protection. This UVLO's rising threshold is 2.2V with a hysteresis of 150mV. The bootstrap capacitor voltage is regulated internally by V_{IN} through D1, R5, C5, L1, and C2 (see Figure 4). If V_{IN} - V_{SW} is more than 5V, U1 regulates M1 to maintain a 5V BST voltage across C5.

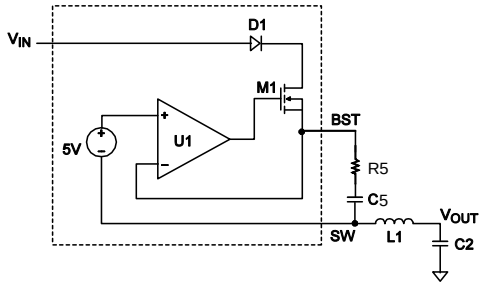

Figure 4: Internal Bootstrap Charging Circuit

Start-Up and Shutdown

If both V_{IN} and EN/SYNC are higher than their appropriate thresholds, the chip starts up. The reference block starts first, generating a stable reference voltage and current, and then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuitries.

Three events can shut down the chip: EN/SYNC low, V_{IN} low, and thermal shutdown. In the shutdown procedure, the signaling path is first blocked to avoid any fault triggering. V_{COMP} and the internal supply rail are then pulled down. The floating driver is not subject to this shutdown command.

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APPLICATION INFORMATION

Setting the Output Voltage

The external resistor divider is used to set the output voltage (see the Typical Application on page 1). The feedback resistor (R1) also sets the feedback loop bandwidth with the internal compensation capacitor. R2 can be calculated with Equation (1):

$$R2 = \frac{R1}{\frac{V_{OUT}}{0.8V} - 1} \quad (1)$$

The T-type network is highly recommended (see Figure 5).

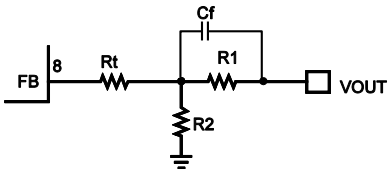

Figure 5: T-Type Network

Table 1 lists the recommended T-type resistors values for common output voltages.

Table 1: Resistor Selection for Common Output Voltages

V_{OUT} (V)	R1(kΩ)	R2(kΩ)	Rt (kΩ)	L (µH)	Cf (pF)
1	20.5	76.8	100	1.8	15
1.2	20.5	39.2	100	1.8	15
1.8	40.2	31.6	56	3.3	15
2.5	40.2	18.7	56	3.3	15
3.3	40.2	12.7	33	4.9	15
5	40.2	7.5	33	4.9	15

Selecting the Inductor

A 1µH to 22µH inductor with a DC current rating at least 25% higher than the maximum load current is recommended for most applications. For the highest efficiency, the inductor DC resistance should be less than 15mΩ. For most designs, the inductance value can be derived from Equation (2):

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}} \quad (2)$$

Where ΔI_L is the inductor ripple current.

Choose the inductor current to be approximately 30% of the maximum load current. The maximum inductor peak current can be calculated with Equation (3):

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2} \quad (3)$$

Under light-load conditions below 100mA, a larger inductance is recommended for improved efficiency.

Selecting the Input Capacitor

The input current to the step-down converter is discontinuous and therefore requires a capacitor to supply AC current to the step-down converter while maintaining the DC input voltage. Use low ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For most applications, a 22µF capacitor is sufficient.

Since the input capacitor (C1) absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated with Equation (4):

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (4)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, shown in Equation (5):

$$I_{C1} = \frac{I_{LOAD}}{2} \quad (5)$$

For simplification, choose the input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, a small, high-quality, ceramic capacitor (i.e.: 0.1µF) should be placed as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide a sufficient charge to prevent excessive voltage ripple at the input. The input voltage ripple caused by the capacitance can be estimated with Equation (6):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_S \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (6)$$

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Selecting the Output Capacitor

The output capacitor (C2) is required to maintain the DC output voltage. Ceramic, tantalum, or low ESR electrolytic capacitors are recommended. Low ESR capacitors are recommended to keep the output voltage ripple low. The output voltage ripple can be estimated with Equation (7):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_S \times C2}\right) \quad (7)$$

Where L_1 is the inductor value and RESR is the equivalent series resistance (ESR) value of the output capacitor.

In the case of ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is mainly caused by the capacitance. For simplification, the output voltage ripple can be estimated with Equation (8):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_S^2 \times L_1 \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (8)$$

In the case of tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated with Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (9)$$

The characteristics of the output capacitor also affect the stability of the regulation system. The MPQ2325 can be optimized for a wide range of capacitance and ESR values.

External Bootstrap Diode

An external bootstrap diode may enhance the efficiency of the regulator. The applicable conditions of the external BST diode are:

- V_{OUT} is 5V or 3.3V
- Duty cycle is high: D = $\frac{V_{OUT}}{V_{IN}}$ > 65%

In these cases, an external BST diode is recommended from VCC to BST (see Figure 6).

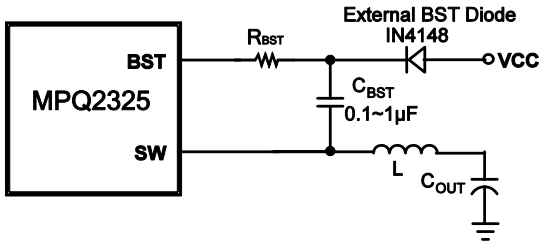

Figure 6: Optional External BST Diode Added

Bootstrap Diode to Enhance Efficiency

The recommended external BST diode is IN4148, and the recommended BST cap is 0.1μF - 1μF.

PCB Layout Guidelines [6]

Efficient PCB layout is critical for stable operation. For best results, refer to Figure 7 and follow the guidelines below.

1. Keep the connection of the input ground and GND as short and wide as possible.
2. Keep the connection of the input capacitor and IN as short and wide as possible.
3. Ensure that all feedback connections are short and direct.
4. Place the feedback resistors and compensation components as close to the chip as possible.
5. Route SW away from sensitive analog areas such as FB.

NOTE:

6) The recommended layout is based on Figure 8 in the Typical Application Circuit section on page 15.

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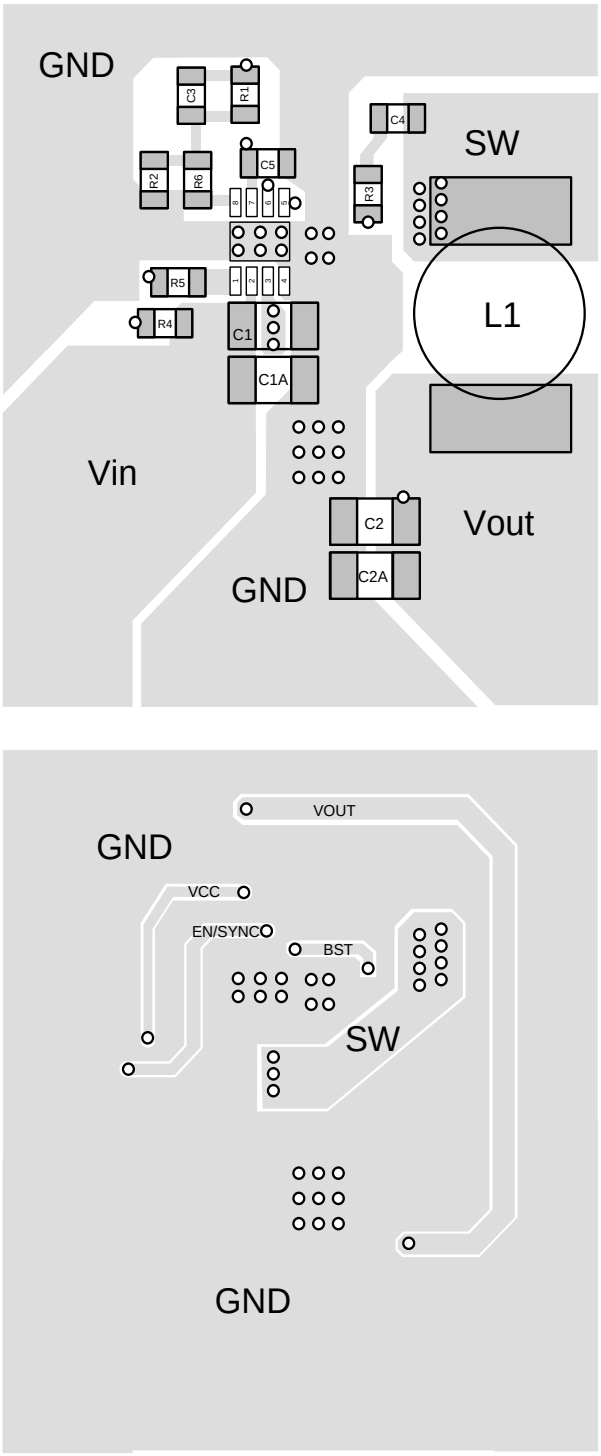

Figure 7: Sample Board Layout

Design Example

Table 2 is a design example following the application guidelines for the specifications below.

Table 2: Design Example

V_{IN}	19V
V_{OUT}	5V
I_O	3A

The detailed application schematics are shown in Figure 8 through Figure 13. The typical performance and circuit waveforms are shown in the Typical Performance Characteristics section. For more device applications, please refer to the related evaluation board datasheets.

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TYPICAL APPLICATION CIRCUITS

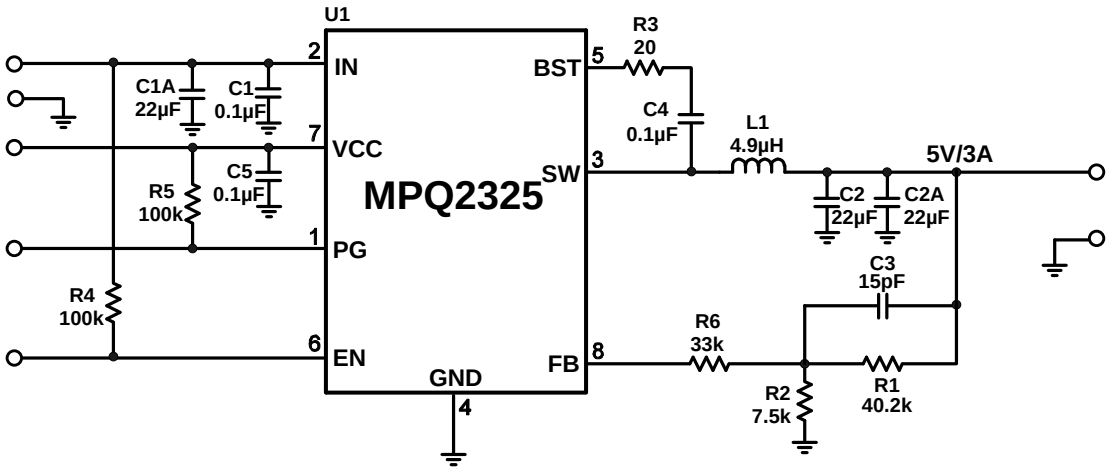

Figure 8: Vo = 5V, Io = 3A

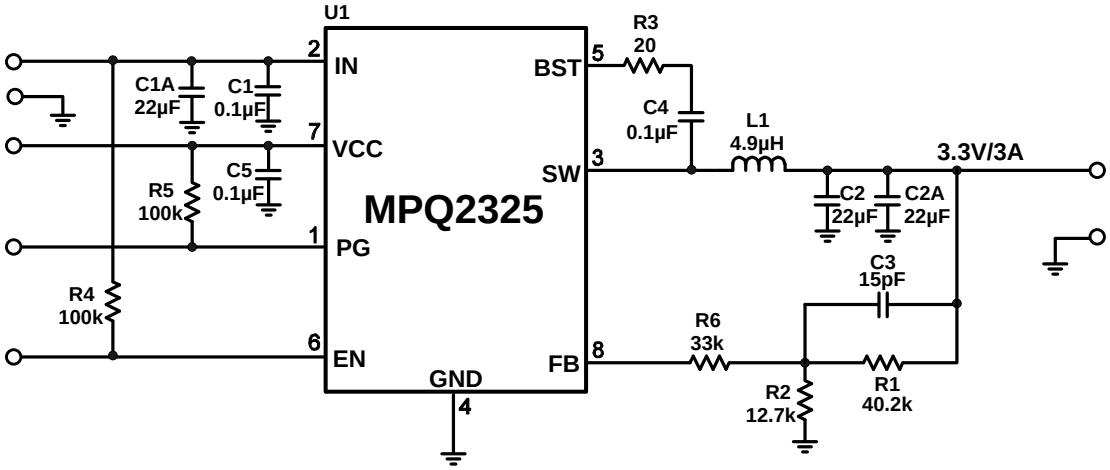

Figure 9: Vo = 3.3V, Io = 3A

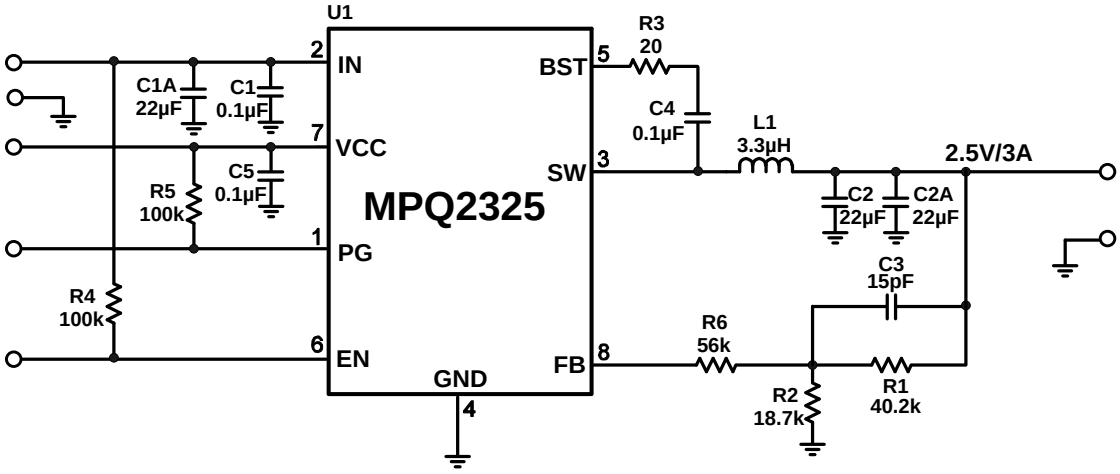

Figure 10: Vo = 2.5V, Io = 3A

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TYPICAL APPLICATION CIRCUITS *(continued)*

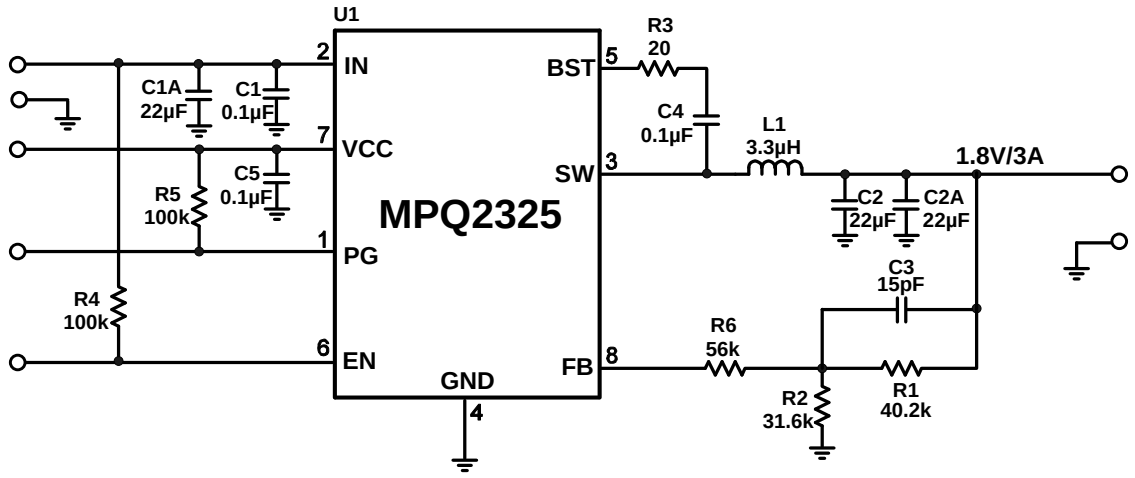

Figure 11: Vo = 1.8V, Io = 3A

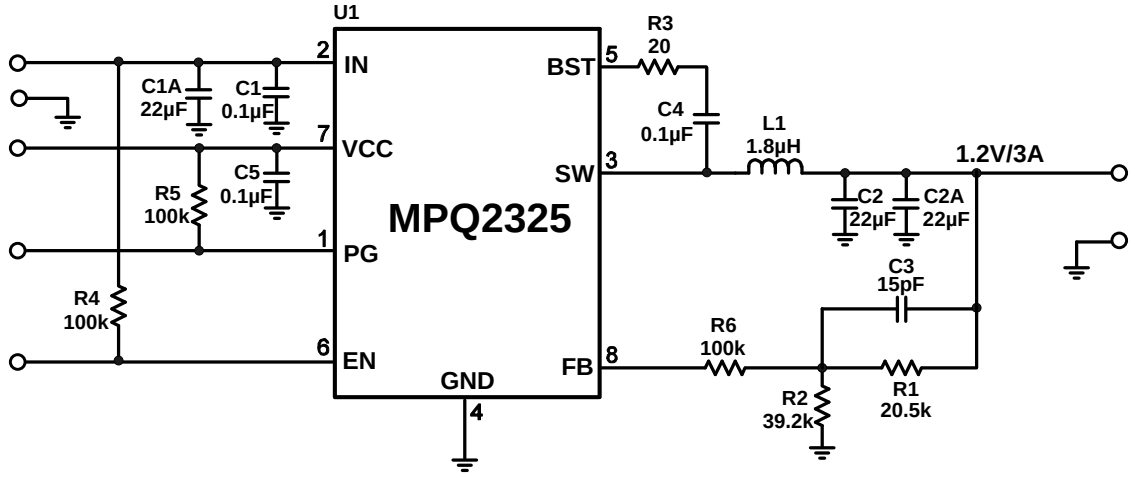

Figure 12: Vo = 1.2V, Io = 3A

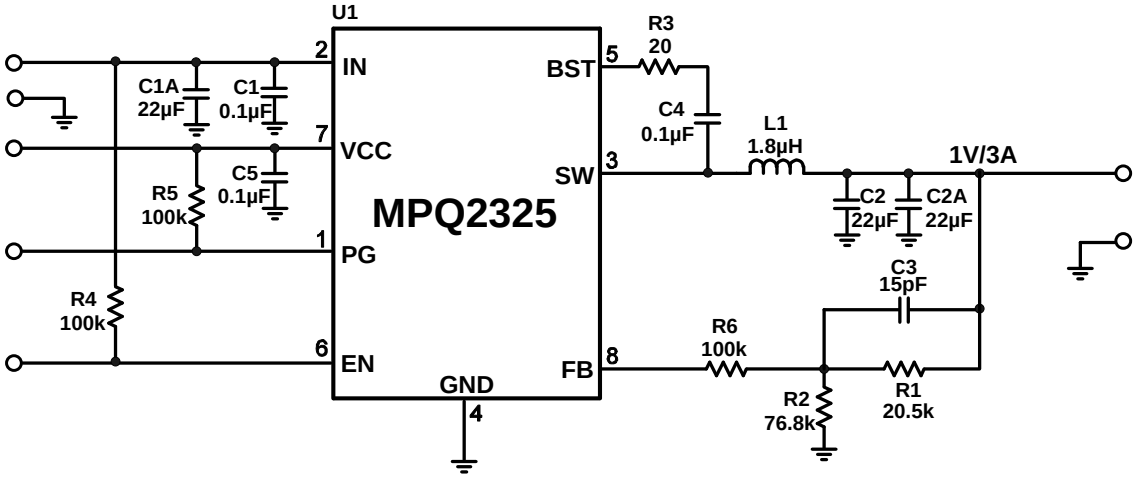

Figure 13: Vo = 1V, Io = 3A

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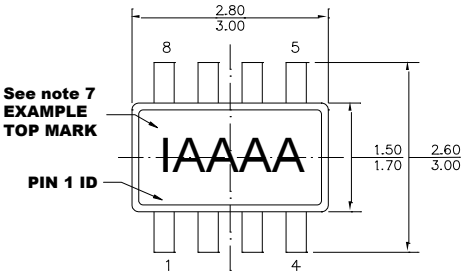
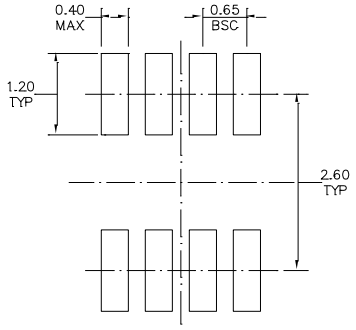
PACKAGE INFORMATION

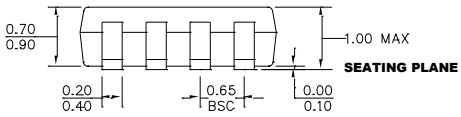
TSOT23-8



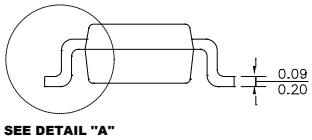
TOP VIEW



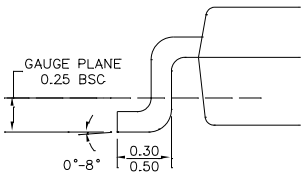
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) JEDEC REFERENCE IS MO-193, VARIATION BA.
6) DRAWING IS NOT TO SCALE.
7) PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT, (SEE EXAMPLE TOP MARK)

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