MPQ2287

6V, 14A, Configurable, High-Frequency, Synchronous Buck Converter, with ZDP™, AEC-Q100 Qualified

DESCRIPTION

The MPQ2287 is a configurable, high-frequency, synchronous buck regulator with integrated internal high-side and low-side power MOSFETs (HS-FET and LS-FET, respectively). The MPQ2287 operates from a 2.7V to 6V input voltage (V_{IN}) range and provides up to 14A of highly efficient output current (I_{OUT}) with fixed-frequency, zero-delay PWM (ZDP™) control for optimal transient response.

The configurable 2MHz to 4MHz switching frequency (f_{SW}) during forced continuous conduction mode (FCCM) greatly reduces the external inductance and capacitance. Internal feedback and compensation minimize the external component count and improves accuracy.

Full protection features include short-circuit protection (SCP), over-current protection (OCP), input over-voltage protection (OVP), output OVP, and thermal shutdown. These protections provide reliable, fault-tolerant operation.

The PMBus interface features packet error checking (PEC), and integrated multi-page one-time programmable (OTP) memory allows for a high degree of configurability.

The MPQ2287 is available in a QFN-18 (3mmx4mm) package with wettable flanks. It is available in AEC-Q100 Grade 1.

FEATURES

- Designed for Automotive Point-of-Load (PoL) Applications
  - 2.7V to 6V Input Voltage (V_{IN})
  - 14A of Continuous Output Current (I_{OUT})
  - 1.0% Output Regulation Accuracy
  - Differential Output Voltage (V_{OUT}) Sense
  - Internal 6mΩ High-Side MOSFET (HS-FET) and 4mΩ Low-Side MOSFET (LS-FET)
  - Configurable 2MHz to 4MHz Switching Frequency (f_{SW})

FEATURES *(continued)*

  - Available in AEC-Q100 Grade 1
- Optimized for EMC/EMI
  - Synchronization Input/Output
  - Frequency Spread Spectrum (FSS)
- Flexible Application with PMBus Interface
  - PMBus Interface with Cyclic Redundancy Check (CRC)
  - Converter On/Off
  - V_{OUT} Setting Range from 0.20625V to 3.6V
  - Faults Detection
  - Factory-Configurable Multi-Page One-Time Programmable (OTP) Memory
- Protections
  - Peak and Valley Current Limit
  - Over-Current Protection (OCP)
  - Short-Circuit Protection (SCP)
  - Output Over-Voltage Protection (OVP)
  - Input OVP
  - Thermal Warning
  - Thermal Shutdown
- Additional Features
  - Soft Start and Soft Shutdown
  - Power Good
  - Available in a QFN-18 (3mmx4mm) Package with Wettable Flanks
- Functional Safety System Design Capable
  - MPSafe ™ Compatible – Functional Safety Supporting Document Available

MPSafe™
FuSa Compatible

APPLICATIONS

- Advanced Driver-Assistance Systems (ADAS)
- Infotainment
- System-On-Chip (SoC) System Cores
- DDR Memory

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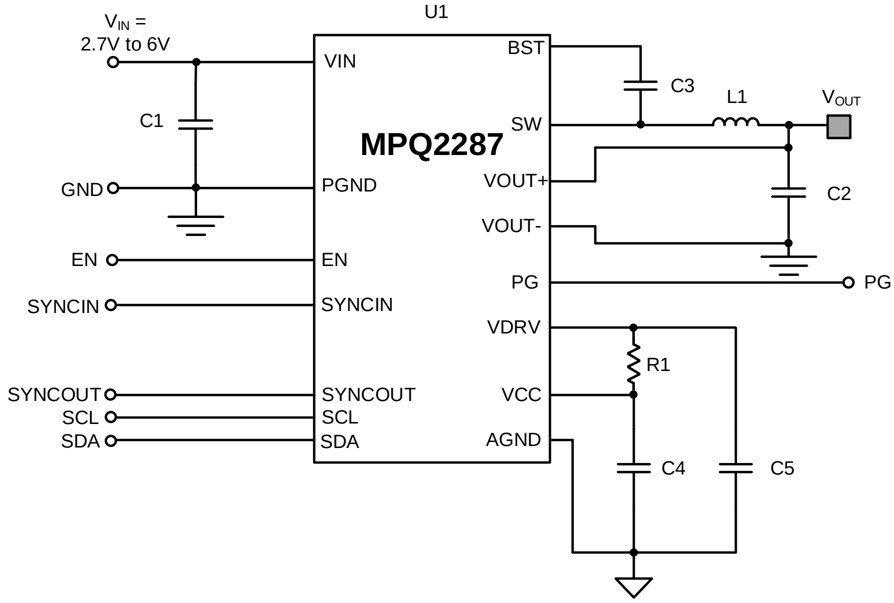
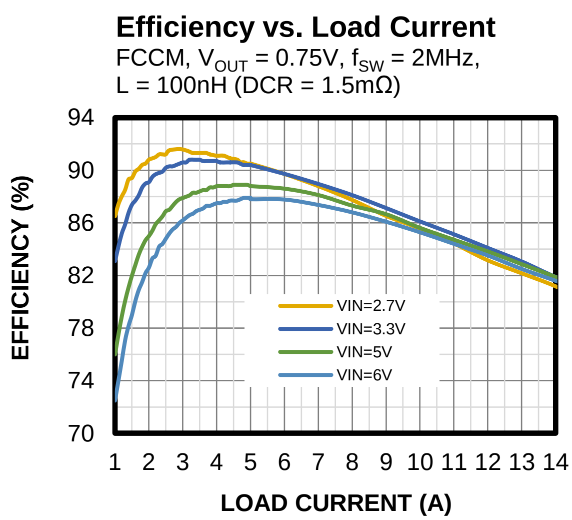
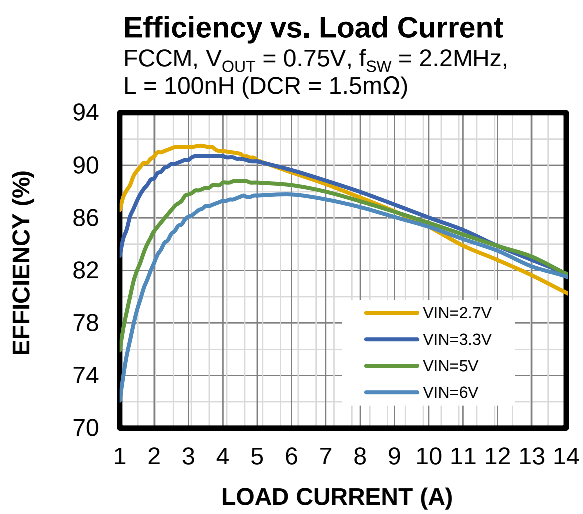
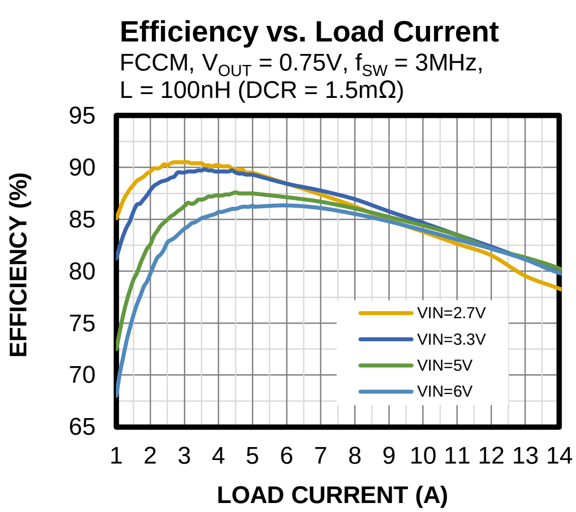
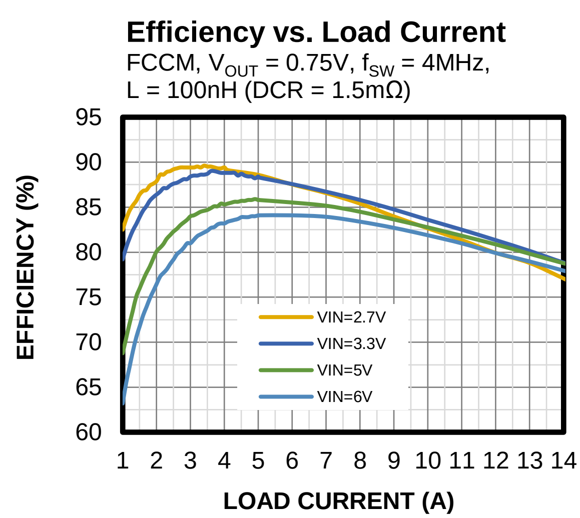
TYPICAL APPLICATION











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ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating***
MPQ2287GLE-xxxx-AEC1 **, ****	QFN-18 (3mmx4mm)	*See Below*	1

* For Tape & Reel, add suffix -Z (e.g. MPQ2287GLE-xxxx-AEC1-Z).

** "xxxx" is the configuration code identifier for the register settings stored in the OTP register. The first value must be a numerical value (0–9), while the last three values can be a hexadecimal value between 0 and F. The default code is "0000". Contact an MPS FAE to create this unique number.

*** Moisture Sensitivity Level Rating

**** Wettable flank

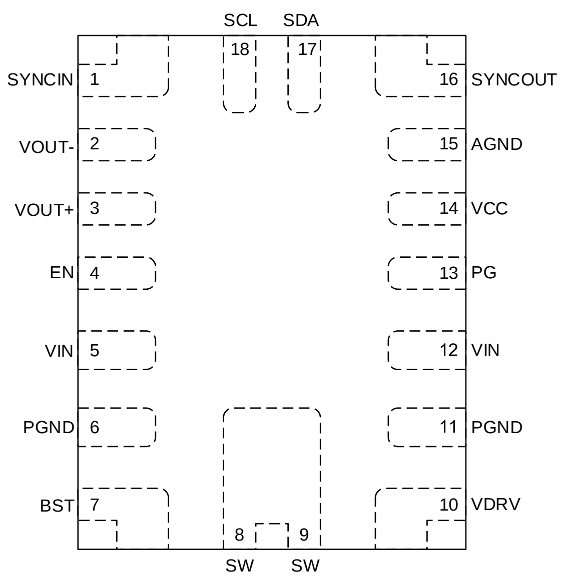
TOP MARKING

<u>MPYW</u>
2287
LLL
E

MP: MPS prefix
Y: Year code
W: Week code
2287: Part number
LLL: Lot number
E: Wettable Flank

PACKAGE REFERENCE

TOP VIEW



QFN-18 (3mmx4mm)

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PIN FUNCTIONS

Pin #	Name	Description
1	SYNCIN	**SYNC input.** Apply a clock signal to the SYNCN pin to synchronize the internal oscillator frequency to the external clock. Use an external clock to enter forced continuous conduction mode (FCCM). The MPQ2287 can also be set to FCCM via the PMBus interface. Connect SYNCIN to GND through a resistor if it is not used.
2	VOUT-	**Output negative differential sense.** Connect VOUT- to the negative side of the output capacitor.
3	VOUT+	**Output positive differential sense.** Connect VOUT+ to the positive side of the output capacitor.
4	EN	**Enable.** Pull the EN pin below the specified threshold (1.1V) to shut down the chip. Pull EN above the specified threshold (1.2V) to enable the chip. There is an internal 200kΩ pull-down resistor. This pin can be floated if it is not used.
5, 12	VIN	**Input supply.** The VIN pins are connected internally. VIN supplies power to the internal low-dropout (LDO) regulator, control circuitry, and the power switch connected to SW. It is recommended to connect a decoupling capacitor from VIN to ground, and placed close to VIN to minimize switching spikes.
6, 11	PGND	**Power ground.** The PGND pins are connected internally.
7	BST	**Bootstrap supply.** The BST pin is the positive power supply for the high-side MOSFET (HS-FET) driver connected to SW. Connect a 0.22µF bypass capacitor between the BST and SW pins.
8, 9	SW	**Switch node**. SW is the output of the internal power switch. Connect SW to the power inductor.
10	VDRV	**Internal LDO decoupling pin and supply input for internal power circuits.** Connect a 4.7µF capacitor from VDRV to PGND. Connect a 2.2Ω resistor between VCC and VDRV.
13	PG	**Power good indicator.** The PG pin is an open-drain output. Connect PG to VCC using an external resistor. PG asserts if the output is not within regulation, or if an error has occurred. This pin can be configured via the PMBus interface. Connect PG to AGND directly or through a resistor if it is not used. See the Power Good (PG) Indicator section on page 32 for the detailed description of the PG state.
14	VCC	**Supply input for internal analog and digital circuits**. Connect a 2.2µF capacitor from VCC to AGND. Connect a 2.2Ω resistor between VCC and VDRV.
15	AGND	**Analog ground.**
16	SYNCOUT	**SYNC output.** SYNCOUT outputs a 0° or 180° out-of-phase clock to the other devices. This pin can be floated if it is not used.
17	SDA	**PMBus interface serial data.** The SDA pin is an open-drain port and cannot be floated. Use an external pull-up resistor to connect this pin to the supply rail of the PMBus interface. Connect this pin to GND if it is not used.
18	SCL	**PMBus interface serial clock.** The SCL pin is an open-drain port and cannot be floated. Use an external pull-up resistor to connect this pin to the supply rail of the PMBus interface. Connect this pin to GND if it is not used.

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ABSOLUTE MAXIMUM RATINGS [1]

V_{IN}, V_{SW} ....-0.3V to +8.5V
V_{BST} .... -0.3V to 4V + V_{SW}
All other pins ....-0.3V to +4V
Continuous power dissipation (T_A = 25°C) [2] [6]
QFN-18 (3mmx4mm) 4.59W
Junction temperature (T_J) ....150°C
Lead temperature ....260°C

ESD Ratings

Human body model (HBM) ....Class 2 [3]
Charged-device model (CDM) ....Class 2b [4]

Recommended Operating Conditions

Input voltage (V_{IN}) ....2.7V to 6V
Output voltage (V_{OUT})..............0.20625V to 3.6V
Operating junction temp (T_J).... -40°C to +150°C

Thermal Resistance θ_{JA} θ_{JC}

QFN-18 (3mmx4mm)
JESD51-7……………………44.67....4.2…°C/W [5]
EVQ2287-L-00A…………..27.22………..°C/W [6]

Ψ_{JT}
JESD51-7….......................................1.3... °C/W [5]
EVQ2287-L-00A..............................2.86... °C/W [6]

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) Per AEC-Q100-002.
4) Per AEC-Q100-011.
5) Measured on a JESD51-7, 4-layer PCB. The values given in this table are only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application. The value of θ_{JC} shows the thermal resistance from junction-to-case bottom, and the Ψ_{JT} value shows the characterization parameter from the junction-to-case top.
6) Measured on an MPS standard EVB, 8.3cmx8.3cm, 2oz copper thickness, 4-layer PCB. The value of Ψ_{JT} shows the characterization parameter from the junction-to-case top.

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ELECTRICAL CHARACTERISTICS

Typical values are V_{IN} = 5V, V_{EN} = 2V, T_J = 25°C, all voltages with respect to ground, unless otherwise noted. Minimum and maximum values are at V_{IN} = 5V, V_{EN} = 2V, T_J = -40°C to +150°C, all voltages with respect to ground, guaranteed by characterization, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Supply Voltage						
Input voltage (V_{IN}) under-voltage lockout (UVLO) rising threshold	V_{IN_UVLO}		2.4		2.7	V
V_{IN} UVLO hysteresis	$V_{IN\_UVLO\_HYS}$			150		mV
VIN quiescent current	I_{Q_ON}	Buck on, no switching			7	mA
VIN shutdown current	I_{Q_OFF}	Buck off, enable low			20	µA
VDRV Regulator						
VDRV regulation voltage	V_{VDRV}	C = 2.2µF, I_{VCC} = 20mA, V_{IN} = 5V	3.1	3.3	3.5	V
VDRV current limit	I_{VDRV}	VDRV = 2.7V, V_{IN} = 5V		100		mA
		VDRV = 0V, V_{IN} = 5V		100		mA
Oscillator						
Switching frequency range (9)	f_{SW}		2		4	MHz
Switching frequency accuracy	f_{SW_ACC}		-10		+10	%
Minimum on time	t_{ON_MIN}	V_{IN} = 5V, V_{OUTP} = 2 x VOUT_SCALE		26	45	ns
Minimum off time	t_{OFF_MIN}			100		ns
Minimum frequency	f_{SW_MIN}	Ultrasonic mode enabled	40		50	kHz
Spread spectrum modulation frequency spread	f_{SS_SPREAD}			-7.5		%
				+6.5		%
Spread spectrum modulation frequency rate	f_{SS_RATE}			9		kHz
Dynamic Output Voltage (V_{OUT})						
VOUT output range (9) (10)	V_{OUT}		0.20625		3.6	V
V_{OUT} accuracy	V_{OUT_ACC}	V_{OUT} ≥ 0.5V x VOUT_SCALE, as a percentage of V_{OUT}, I_{OUT} = 0A	-1		+1	%
		VOUT_SCALE = 1, V_{OUT} < 0.5V, I_{OUT} = 0A	-5		+5	mV
		VOUT_SCALE = 2, V_{OUT} < 1V, I_{OUT} = 0A	-10		+10	mV
V_{OUT} start-up slew rate range (9)	$V_{OUTSLEW\_ST}$		1.25		10	mV/µs
V_{OUT} start-up slew rate accuracy	$V_{OUTSLEW\_ST\_ACC}$		-15		+15	%
V_{OUT} shutdown slew rate range (9)	$V_{OUTSLEW\_SD}$		1.25		10	mV/µs
V_{OUT} shutdown slew rate accuracy	$V_{OUTSLEW\_SD\_ACC}$		-15		+15	%

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ELECTRICAL CHARACTERISTICS *(continued)*

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Parameter	Symbol	Condition	Min	Typ	Max	Units
V_{OUT} dynamic slew rate range (9)	$V_{OUTSLEW}$		2.5		20	mV/µs
V_{OUT} dynamic slew rate accuracy	$V_{OUTSLEW\_ACC}$		-15		+15	%
Power Stage						
High-side (HS) switch on resistance	R_{DS_HS}			6	12	mΩ
Low-side (LS) switch on resistance	R_{DS_LS}			4	8	mΩ
HS switch leakage current	I_{ILEAK_HS}	V_{DS} = 6V			200	µA
LS switch leakage current	I_{ILEAK_LS}	V_{DS} = 6V			200	µA
Peak current limit (9)	I_{LIM_HS}	ILIM_SCALE = 100%	20.5	25	32	A
Valley current limit (9)	I_{LIM_LS}	ILIM_SCALE = 100%	14	18	20.5	A
Reverse current limit	$I_{LIMIT\_REVERSE}$		7	10		A
High-side (HS) recovery threshold	$I_{RECOVERY\_HS}$	V_{IN} = 5V		-3		A
Feedback leakage	R_{FB1}	VOUT_SCALE = 1	20			kΩ
	R_{FB2}	VOUT_SCALE = 2	20			kΩ
Output discharge	R_{DIS}			120		Ω
Bootstrap Supply						
Bootstrap UVLO rising threshold	V_{BST_UVLO}				2.5	V
Bootstrap UVLO Hysteresis	$V_{BST\_UVLO\_HYS}$		0.2			V
Thermal Protection						
Thermal warning rising threshold (7)	T_{TW}		125	140	155	°C
Thermal warning hysteresis	T_{TW_HYS}			20		°C
Thermal shutdown rising threshold (7)	T_{TSD}		155	170	185	°C
Thermal shutdown hysteresis	T_{TSD_HYS}			20		°C
Output Voltage Protection						
V_{OUT} over-voltage (OV) rising threshold	V_{OUT_OV}		113	116	119	%
V_{OUT} OV hysteresis	$V_{OUT\_OV\_HYS}$			7		%
V_{OUT} under-voltage (UV) falling threshold	V_{OUT_UV}		70	75	80	%
V_{OUT} UV hysteresis	$V_{OUT\_UV\_HYS}$			7		%
Hiccup time range (9)	t_{HICK}		2		8	ms

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ELECTRICAL CHARACTERISTICS *(continued)*

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Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Over-Voltage Protection (OVP)						
V_{IN} OV rising threshold	V_{IN_OV}		6.5	6.7	6.85	V
V_{IN} OV hysteresis	$V_{IN\_OV\_HYS}$			0.7		V
V_{IN} OV delay time	t_{VIN_OV}			7		µs
Enable (EN)						
EN logic on rising threshold	V_{EN_LOG}		0.25	0.65	1	V
EN rising threshold	V_{EN}		1.1	1.2	1.3	V
EN voltage hysteresis	V_{EN_HYS}			100		mV
EN leakage	I_{EN}	V_{EN} = 3.3V			10	µA
Power Good (PG)						
PG OV rising threshold (8) (9)	PG_{OV_TH}	PG_OV_TH = 0	103%	104%	105%	V_{OUT}
		PG_OV_TH = 1	105%	106%	107%	V_{OUT}
PG OV threshold hysteresis	PG_{OV_HYS}			0.8%		V_{OUT}
PG UV falling threshold (8) (9)	PG_{UV_TH}	PG_UV_TH = 0	95%	96%	97%	V_{OUT}
		PG_UV_TH = 1	93%	94%	95%	V_{OUT}
PG UV threshold hysteresis	PG_{UV_HYS}			0.8%		V_{OUT}
PG sink capability	I_{PG}	I_{PG} = 1mA			300	mV
PG delay range (9)	t_{PG_DELAY}		0		10	ms
PG rising deglitch	$t_{PG\_R\_DEGLITCH}$			20		µs
PG falling deglitch	$t_{PG\_F\_DEGLITCH}$			20		µs
SCL/SDA input logic low	V_{IL}		0		0.4	V
SCL/SDA input logic high	V_{IH}		1.2			V
SCL/SDA output logic low	V_{OL}	I_{LOAD} = 3mA			0.4	V
SCL clock frequency (7)	f_{SCL}				1000	kHz
SCL high time (7)	t_{HIGH}		0.26			µs
SCL low time (7)	t_{LOW}		0.5			µs
Data set-up time (7)	t_{SU_DAT}		50			ns
Data hold time (7)	t_{HD_DAT}		0			µs
Set-up time for repeated start (7)	t_{SU_STA}		0.26			µs
Hold time for start (7)	t_{HD_STA}		0.26			µs
Bus free time between a start and a stop command (7)	t_{BUF}		0.5			µs
Set-up time for stop command (7)	t_{SU_STO}		0.26			µs
Rising time of SCL/SDA (7)	t_R				120	ns
Falling time of SCL/SDA (7)	t_F	V_{DD} supplies the PMBus interface	20 x (V_{DD} / 5.5V)		120	ns

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ELECTRICAL CHARACTERISTICS *(continued)*

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Parameter	Symbol	Condition	Min	Typ	Max	Units
Pulse width of suppressed spike (7)	t_{SP}				50	ns
Capacitance bus for each bus line (7)	C_B				550	pF

Notes:

7) Derived from bench characterization. Not tested in production.
8) The power good threshold is based on the nominal output voltage.
9) Use the write register to set the EC parameters. See the Register Map section starting on page 39 for the detailed description.
10) Set VOUT_SCALE to 1 when V_{OUT} is between 0.20625V and 1.8V. If V_{OUT} is between 1.8V and 3.6V, set VOUT_SCALE to 2.

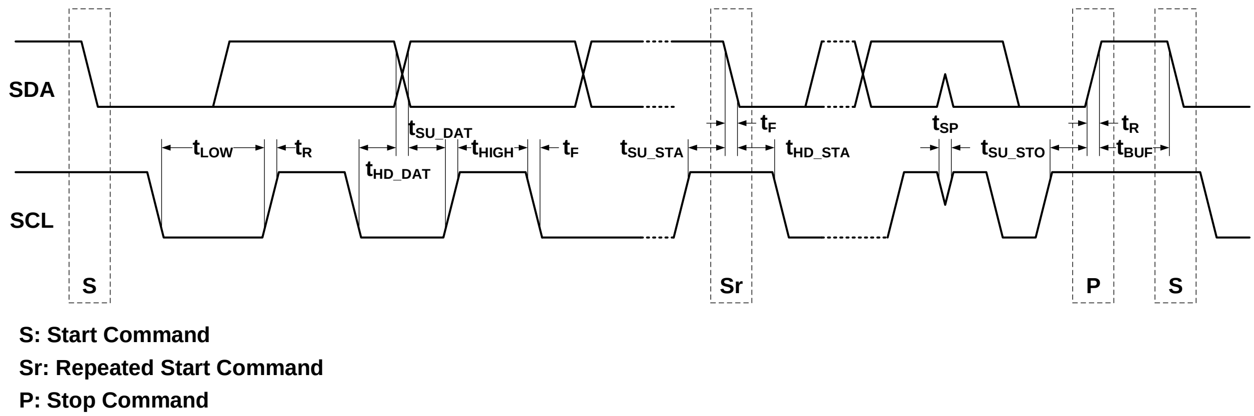

Figure 1: Digital Interface Compatible Timing Diagram

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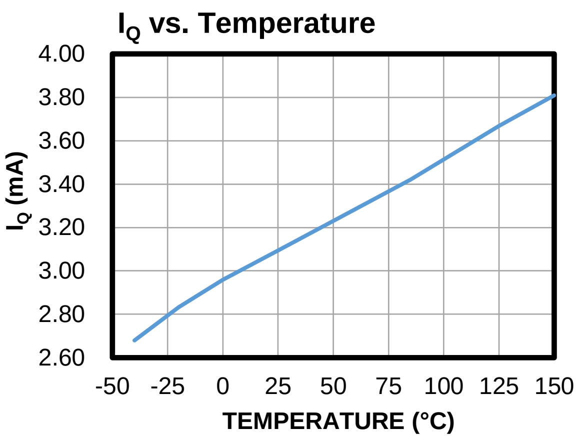
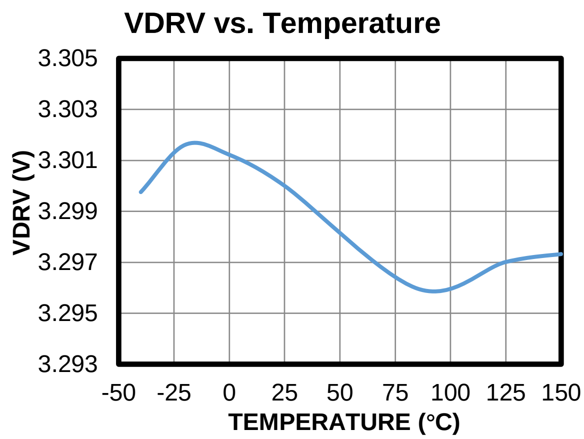
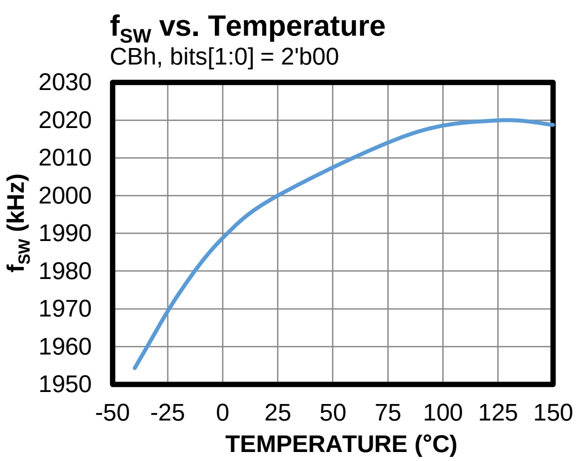
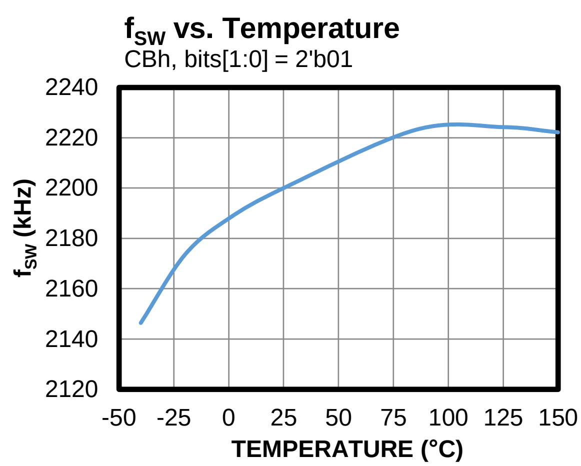
TYPICAL CHARACTERISTICS

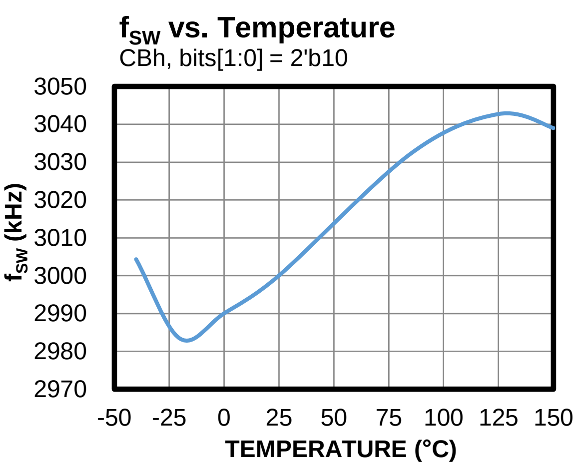
V_{IN} = 5V, T_J = -40°C to +150°C, unless otherwise noted.

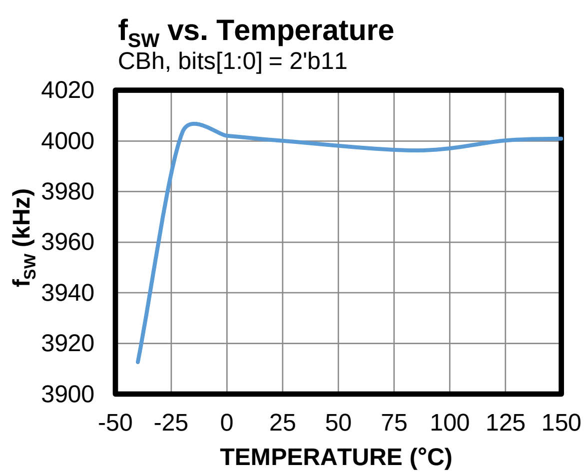












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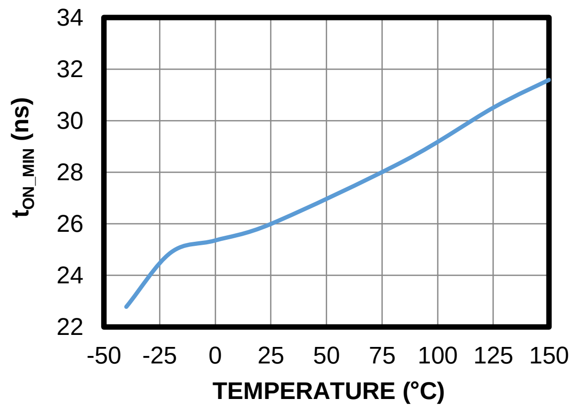
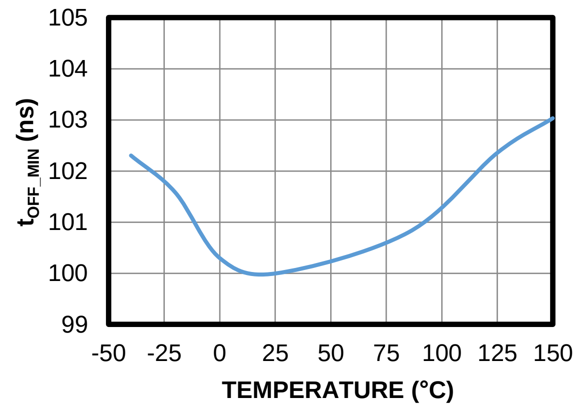
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, T_J = -40°C to +150°C, unless otherwise noted.

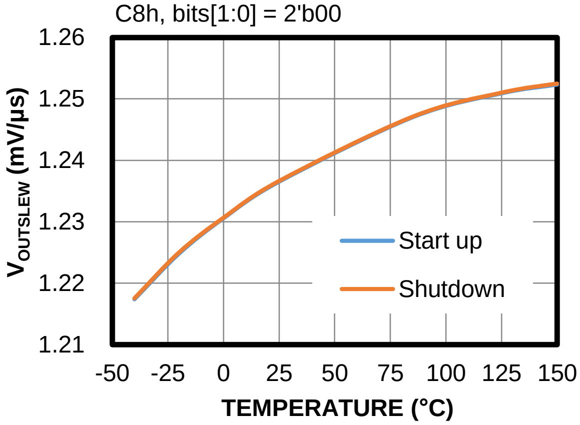
t_{ON_MIN} vs. Temperature



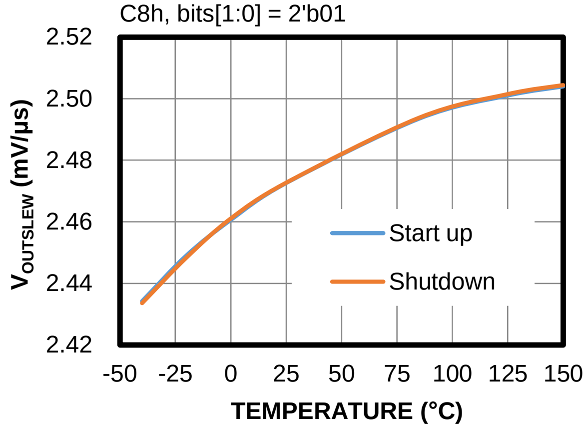
t_{OFF_MIN} vs. Temperature



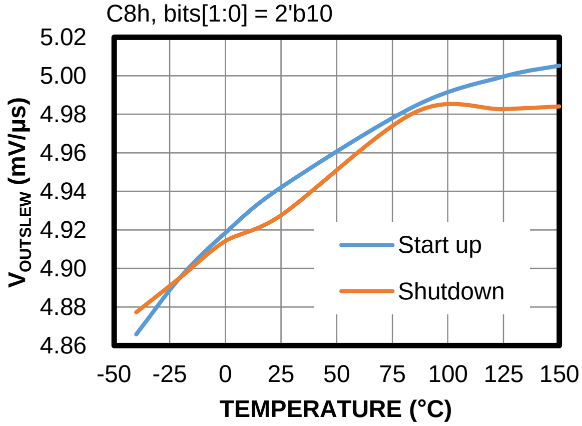
V_{OUT} Slew Rate vs. Temperature
29h, bit[0] = 1'b0,
C6h, bits[1:0] = 2'b00,
C8h, bits[1:0] = 2'b00



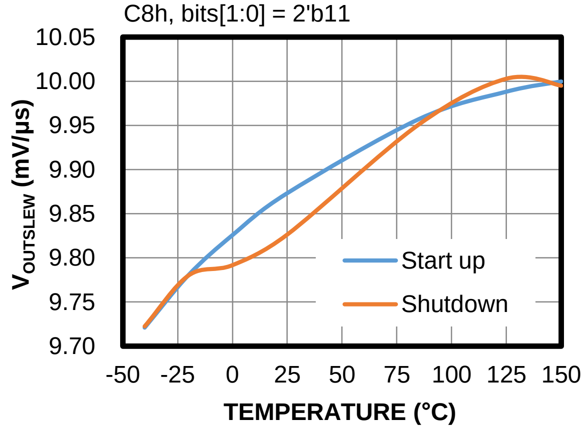
V_{OUT} Slew Rate vs. Temperature
29h, bit[0] = 1'b0,
C6h, bits[1:0] = 2'b01,
C8h, bits[1:0] = 2'b01



V_{OUT} Slew Rate vs. Temperature
29h, bit[0] = 1'b0,
C6h, bits[1:0] = 2'b10,
C8h, bits[1:0] = 2'b10



V_{OUT} Slew Rate vs. Temperature
29h, bit[0] = 1'b0,
C6h, bits[1:0] = 2'b11,
C8h, bits[1:0] = 2'b11



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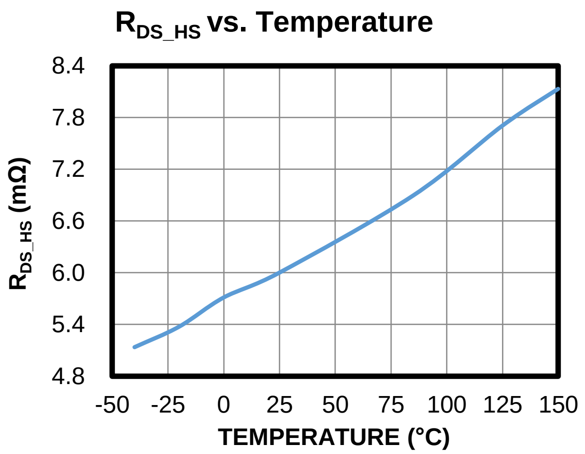
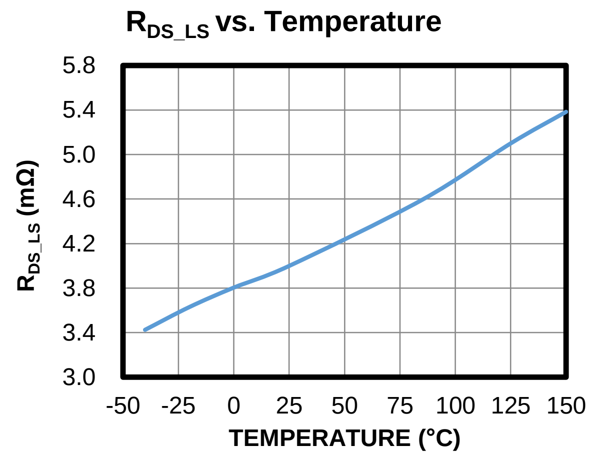
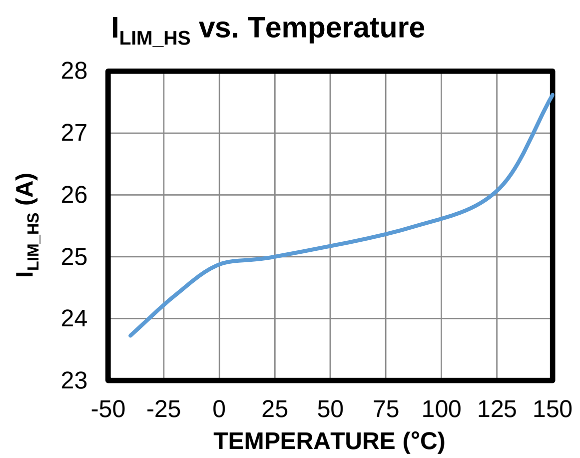
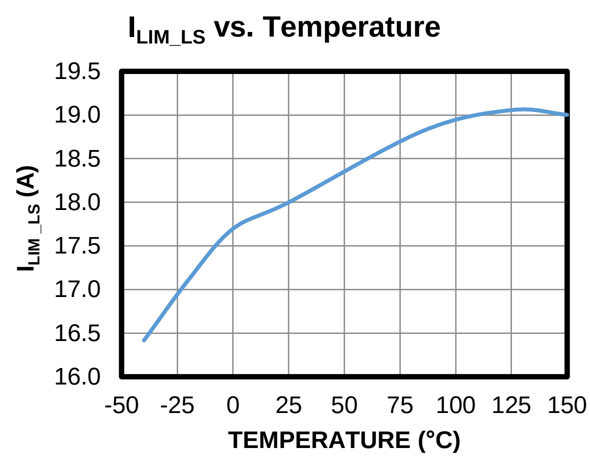
TYPICAL CHARACTERISTICS *(continued)*

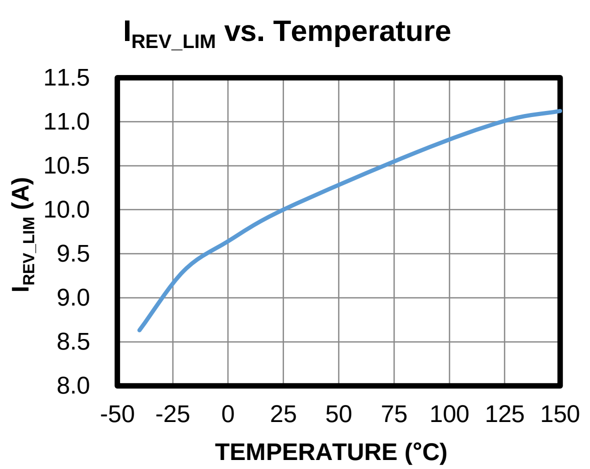
V_{IN} = 5V, T_J = -40°C to +150°C, unless otherwise noted.

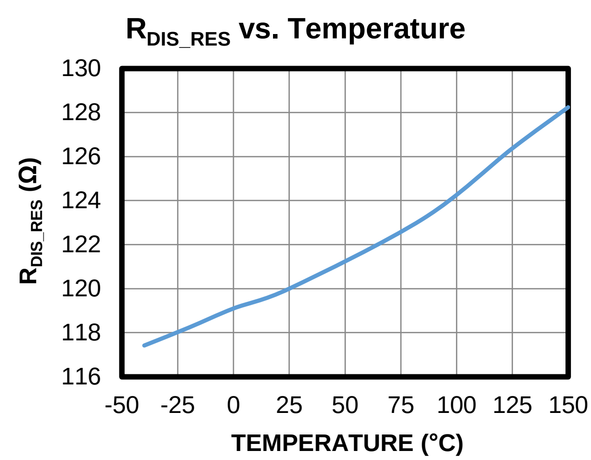












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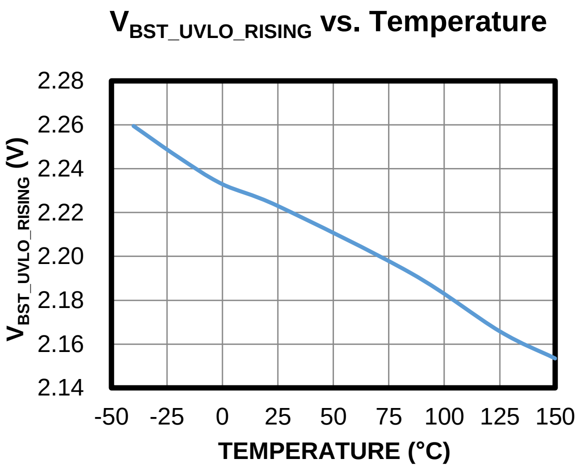
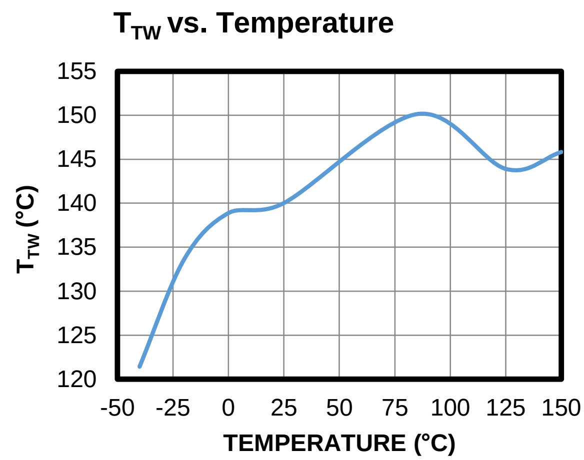
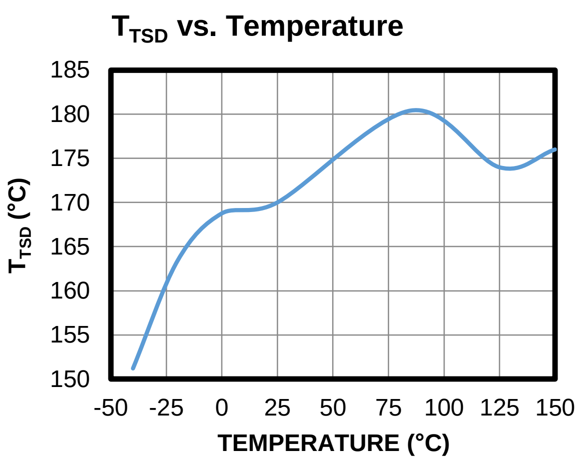
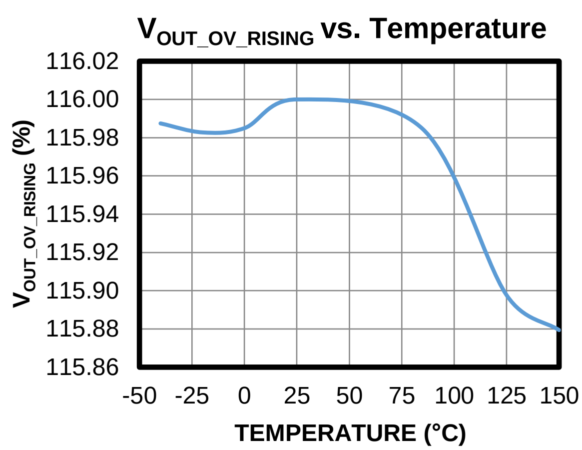
TYPICAL CHARACTERISTICS *(continued)*

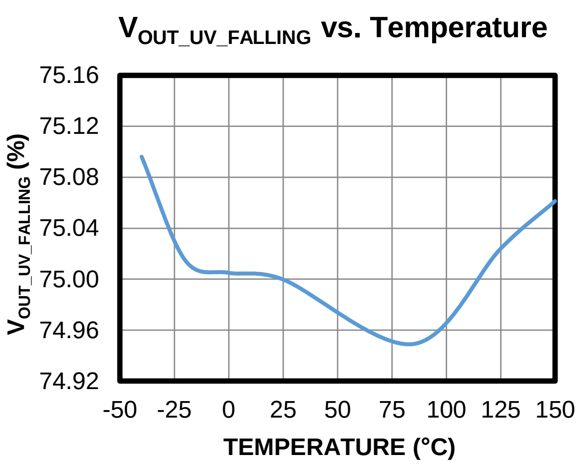
V_{IN} = 5V, T_J = -40°C to +150°C, unless otherwise noted.

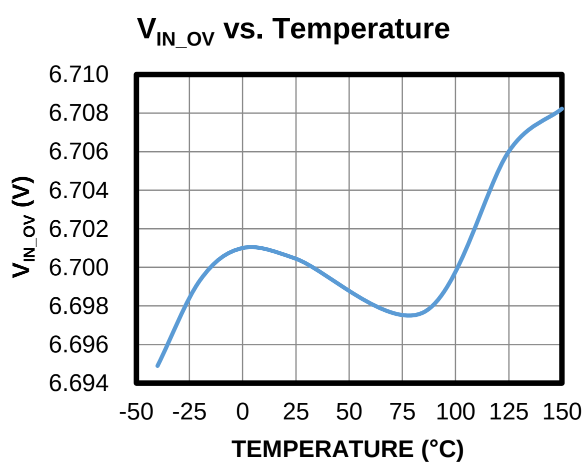












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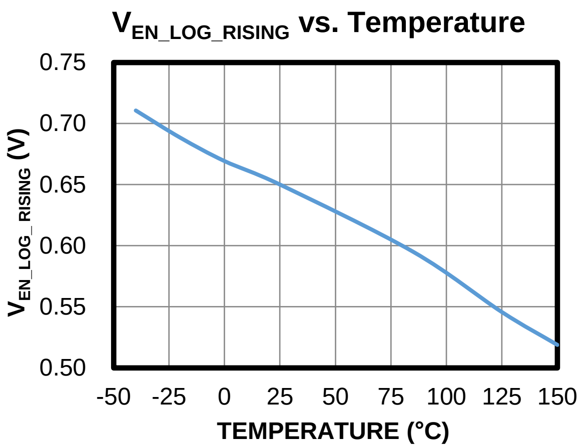
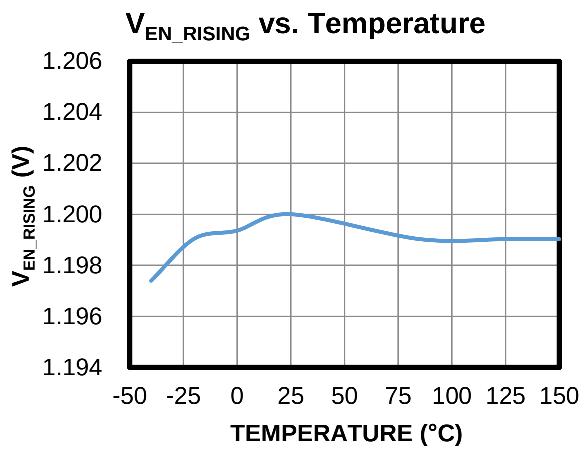
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, T_J = -40°C to +150°C, unless otherwise noted.





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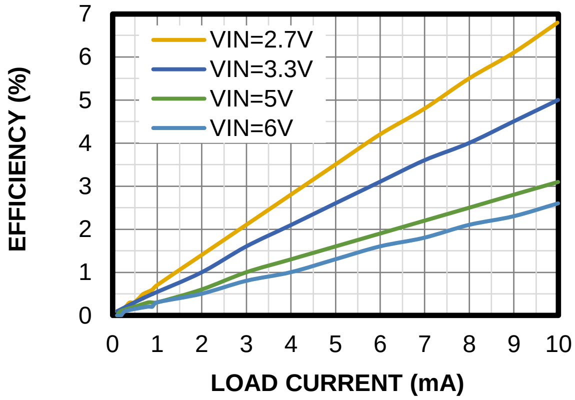
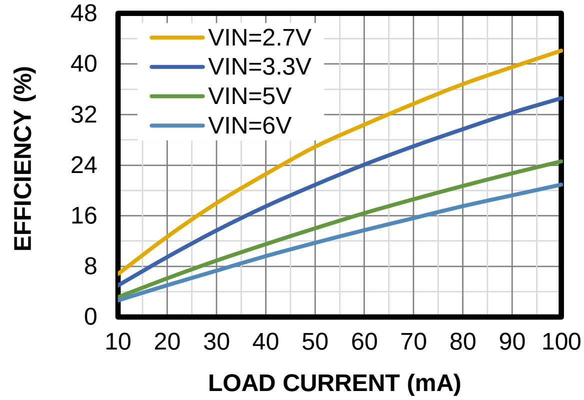
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 5V, V_{OUT} = 0.75V, L = 100nH, C_{OUT} = 4 x 47µF, f_{SW} = 3MHz, T_A = 25°C, unless otherwise noted.

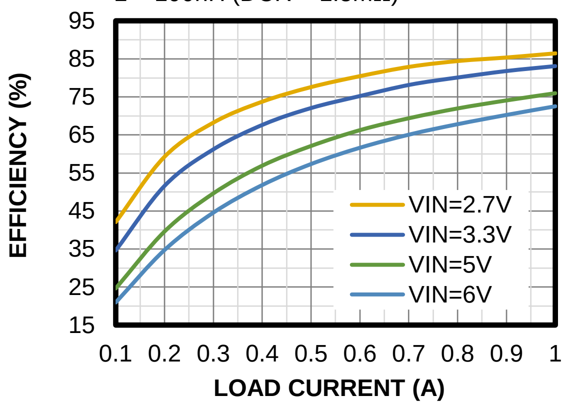
Efficiency vs. Load Current
FCCM, V_{OUT} = 0.75V, f_{SW} = 2MHz,
L = 100nH (DCR = 1.5mΩ)



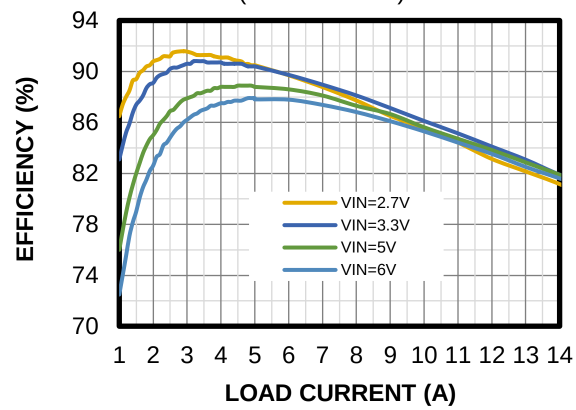
Efficiency vs. Load Current
FCCM, V_{OUT} = 0.75V, f_{SW} = 2MHz,
L = 100nH (DCR = 1.5mΩ)



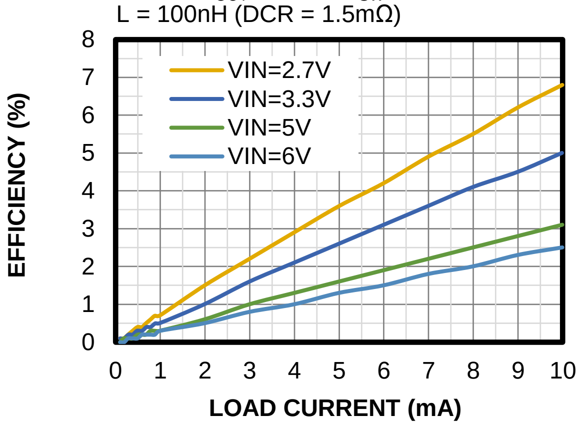
Efficiency vs. Load Current
FCCM, V_{OUT} = 0.75V, f_{SW} = 2MHz,
L = 100nH (DCR = 1.5mΩ)



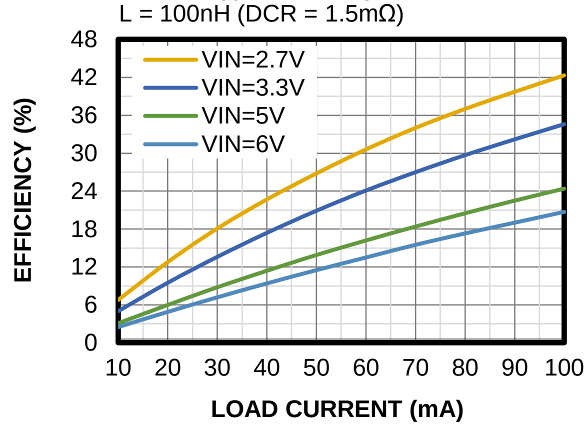
Efficiency vs. Load Current
FCCM, V_{OUT} = 0.75V, f_{SW} = 2MHz,
L = 100nH (DCR = 1.5mΩ)



Efficiency vs. Load Current
FCCM, V_{OUT} = 0.75V, f_{SW} = 2.2MHz,
L = 100nH (DCR = 1.5mΩ)



Efficiency vs. Load Current
FCCM, V_{OUT} = 0.75V, f_{SW} = 2.2MHz,
L = 100nH (DCR = 1.5mΩ)



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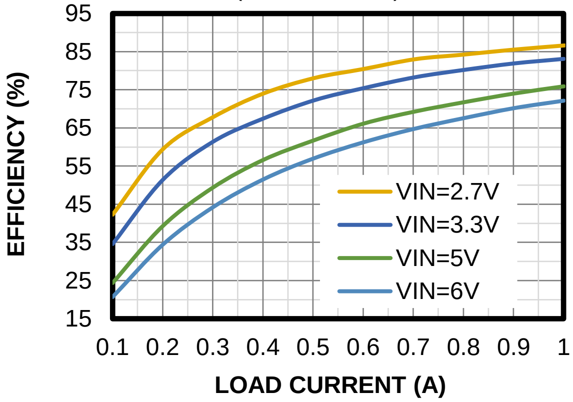
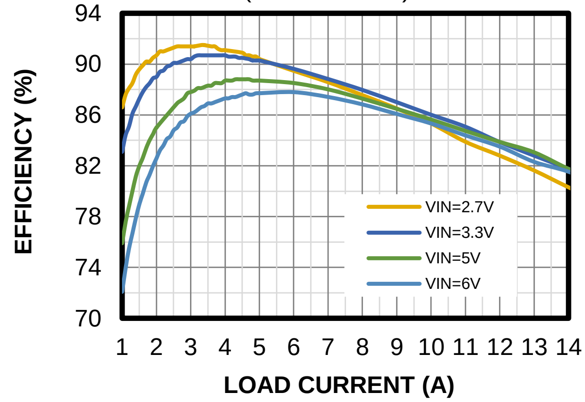
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 0.75V, L = 100nH, C_{OUT} = 4 x 47µF, f_{SW} = 3MHz, T_A = 25°C, unless otherwise noted.

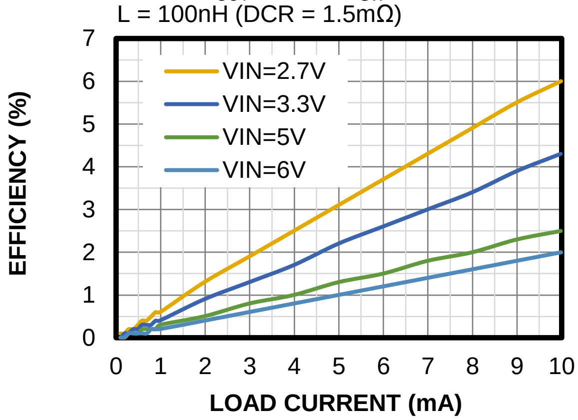
Efficiency vs. Load Current
FCCM, V_{OUT} = 0.75V, f_{SW} = 2.2MHz,
L = 100nH (DCR = 1.5mΩ)



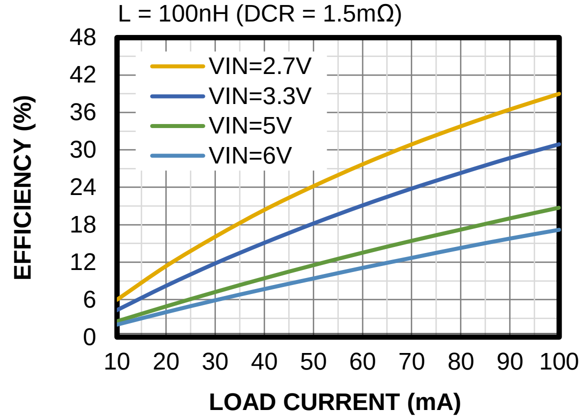
Efficiency vs. Load Current
FCCM, V_{OUT} = 0.75V, f_{SW} = 2.2MHz,
L = 100nH (DCR = 1.5mΩ)



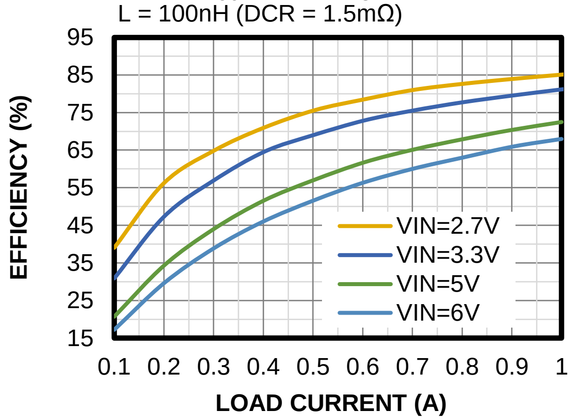
Efficiency vs. Load Current
FCCM, V_{OUT} = 0.75V, f_{SW} = 3MHz,
L = 100nH (DCR = 1.5mΩ)



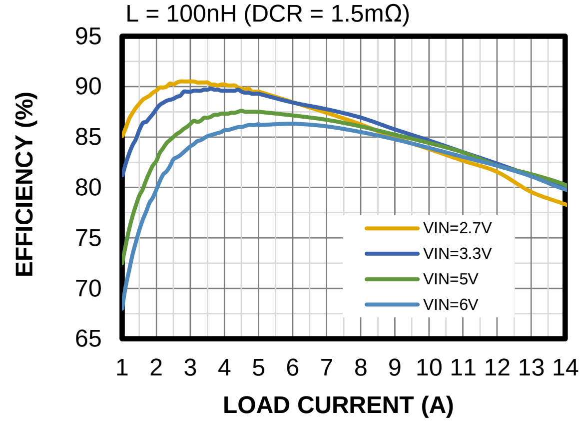
Efficiency vs. Load Current
FCCM, V_{OUT} = 0.75V, f_{SW} = 3MHz,
L = 100nH (DCR = 1.5mΩ)



Efficiency vs. Load Current
FCCM, V_{OUT} = 0.75V, f_{SW} = 3MHz,
L = 100nH (DCR = 1.5mΩ)



Efficiency vs. Load Current
FCCM, V_{OUT} = 0.75V, f_{SW} = 3MHz,
L = 100nH (DCR = 1.5mΩ)



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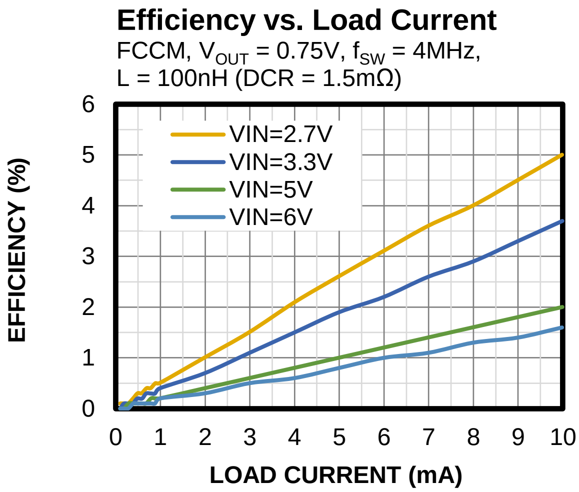
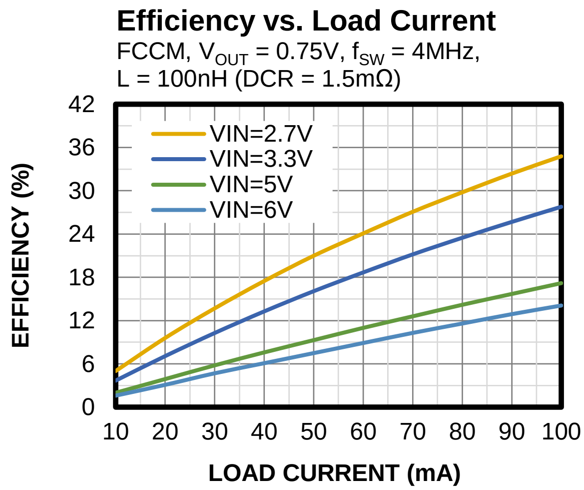
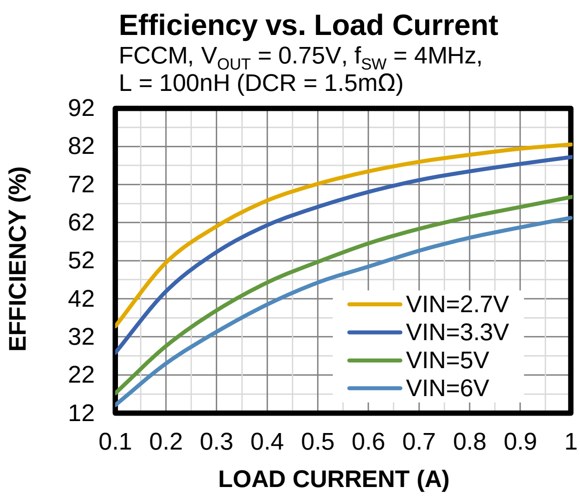
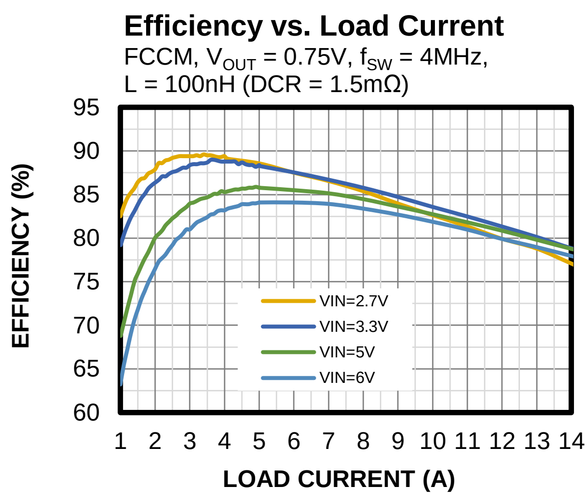
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

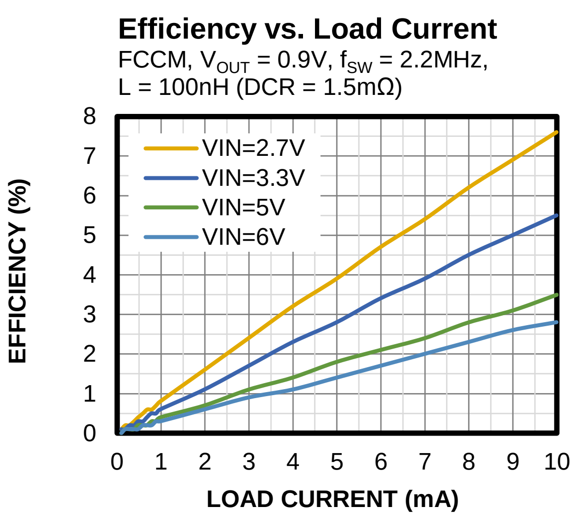
V_{IN} = 5V, V_{OUT} = 0.75V, L = 100nH, C_{OUT} = 4 x 47µF, f_{SW} = 3MHz, T_A = 25°C, unless otherwise noted.

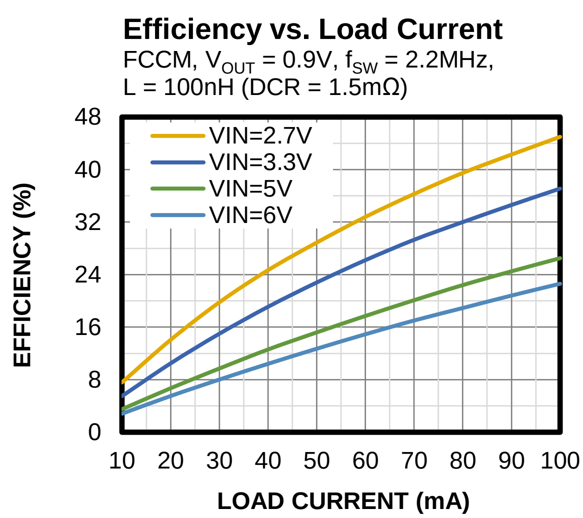












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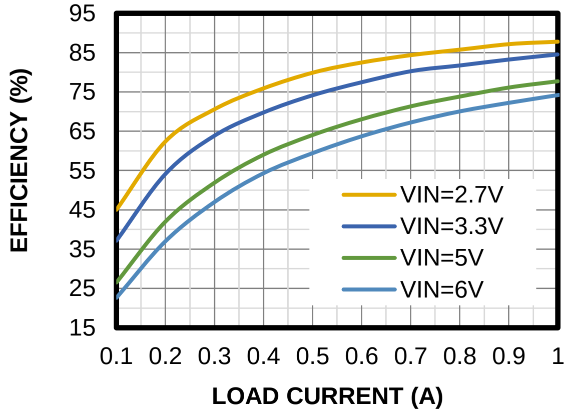
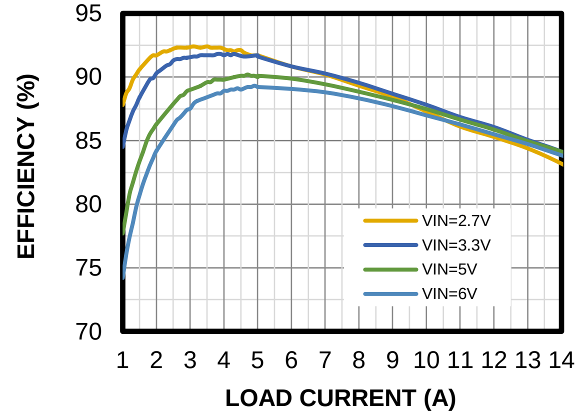
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 0.75V, L = 100nH, C_{OUT} = 4 x 47µF, f_{SW} = 3MHz, T_A = 25°C, unless otherwise noted.

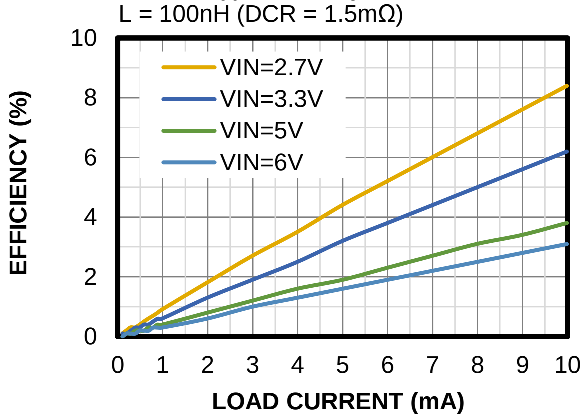
Efficiency vs. Load Current
FCCM, V_{OUT} = 0.9V, f_{SW} = 2.2MHz,
L = 100nH (DCR = 1.5mΩ)



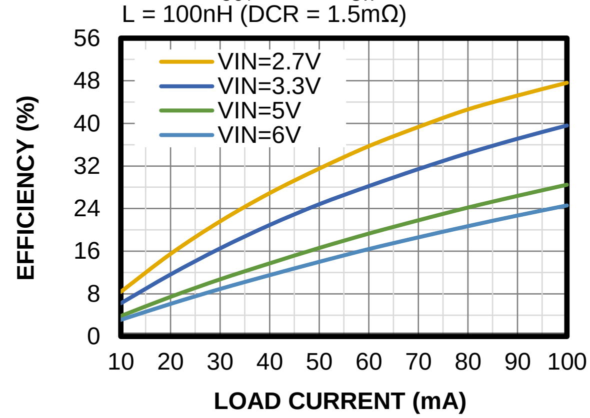
Efficiency vs. Load Current
FCCM, V_{OUT} = 0.9V, f_{SW} = 2.2MHz,
L = 100nH (DCR = 1.5mΩ)



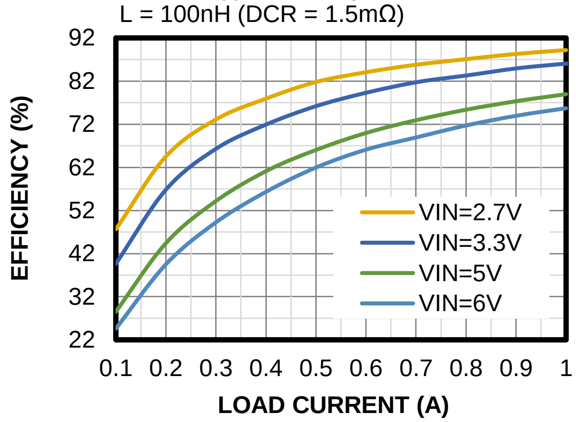
Efficiency vs. Load Current
FCCM, V_{OUT} = 1.1V, f_{SW} = 2.2MHz,
L = 100nH (DCR = 1.5mΩ)



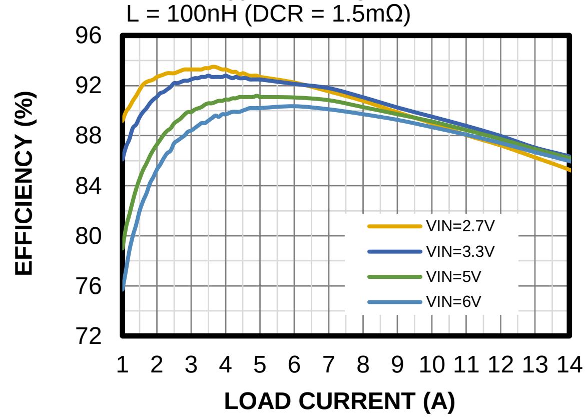
Efficiency vs. Load Current
FCCM, V_{OUT} = 1.1V, f_{SW} = 2.2MHz,
L = 100nH (DCR = 1.5mΩ)



Efficiency vs. Load Current
FCCM, V_{OUT} = 1.1V, f_{SW} = 2.2MHz,
L = 100nH (DCR = 1.5mΩ)



Efficiency vs. Load Current
FCCM, V_{OUT} = 1.1V, f_{SW} = 2.2MHz,
L = 100nH (DCR = 1.5mΩ)



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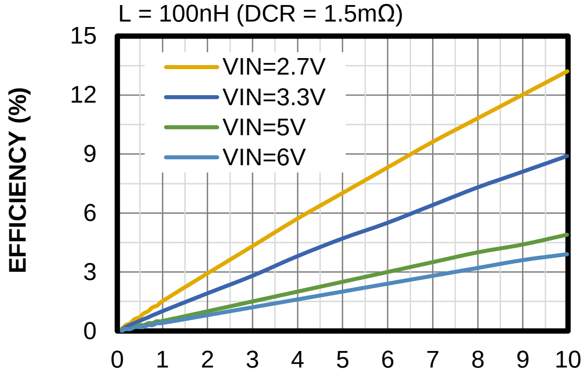
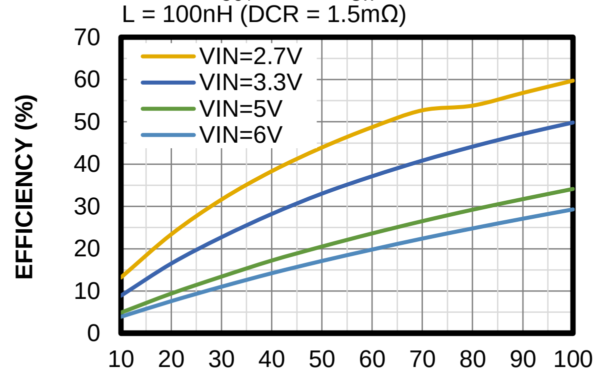
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 0.75V, L = 100nH, C_{OUT} = 4 x 47µF, f_{SW} = 3MHz, T_A = 25°C, unless otherwise noted.

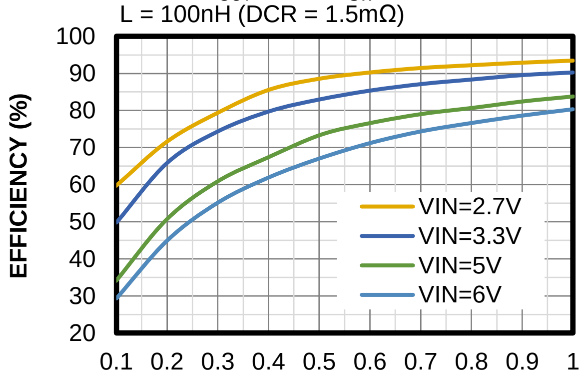
Efficiency vs. Load Current
FCCM, V_{OUT} = 1.8V, f_{SW} = 2.2MHz,
L = 100nH (DCR = 1.5mΩ)



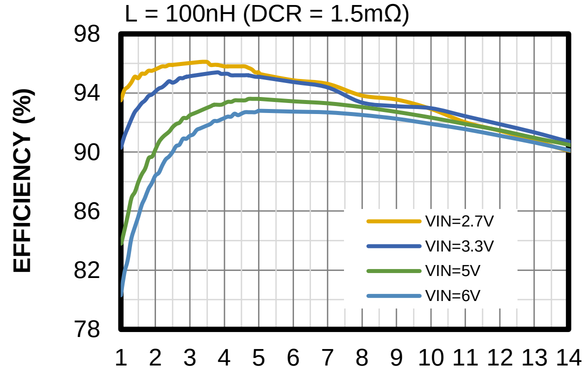
Efficiency vs. Load Current
FCCM, V_{OUT} = 1.8V, f_{SW} = 2.2MHz,
L = 100nH (DCR = 1.5mΩ)



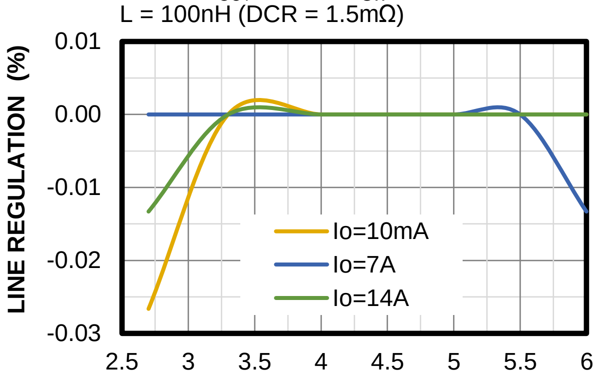
Efficiency vs. Load Current
FCCM, V_{OUT} = 1.8V, f_{SW} = 2.2MHz,
L = 100nH (DCR = 1.5mΩ)



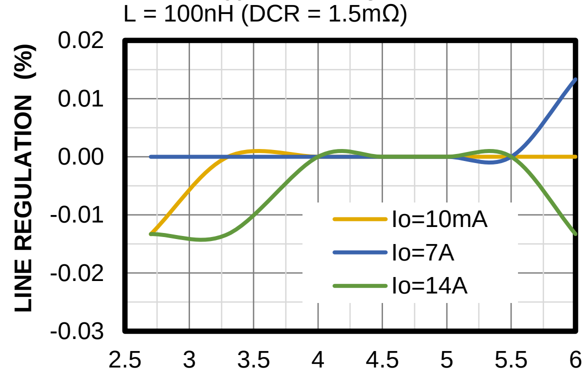
Efficiency vs. Load Current
FCCM, V_{OUT} = 1.8V, f_{SW} = 2.2MHz,
L = 100nH (DCR = 1.5mΩ)



Line Regulation
FCCM, V_{OUT} = 0.75V, f_{SW} = 2MHz,
L = 100nH (DCR = 1.5mΩ)



Line Regulation
FCCM, V_{OUT} = 0.75V, f_{SW} = 2.2MHz,
L = 100nH (DCR = 1.5mΩ)



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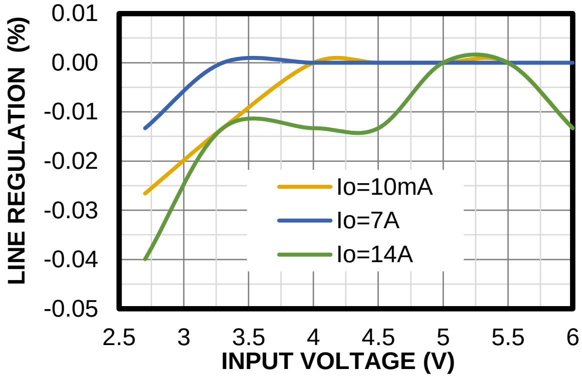
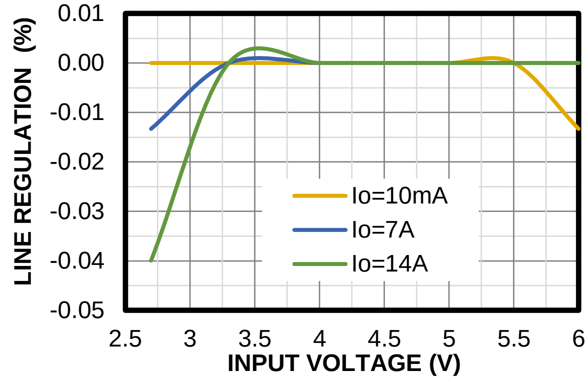
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 0.75V, L = 100nH, C_{OUT} = 4 x 47µF, f_{SW} = 3MHz, T_A = 25°C, unless otherwise noted.

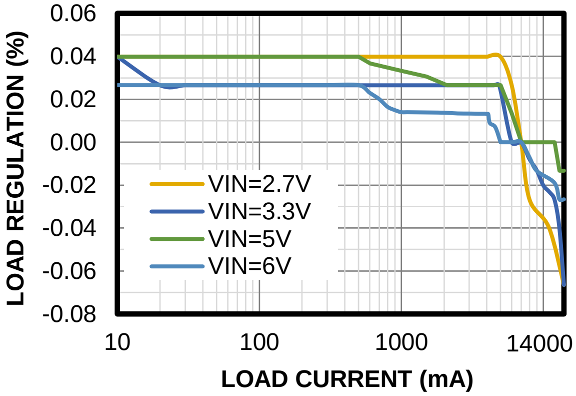
Line Regulation
FCCM, V_{OUT} = 0.75V, f_{SW} = 3MHz,
L = 100nH (DCR = 1.5mΩ)



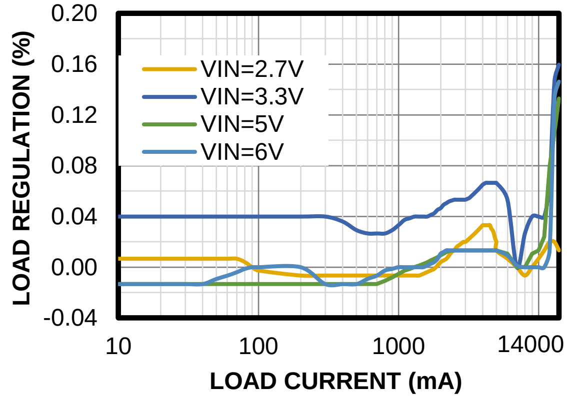
Line Regulation
FCCM, V_{OUT} = 0.75V, f_{SW} = 4MHz,
L = 100nH (DCR = 1.5mΩ)



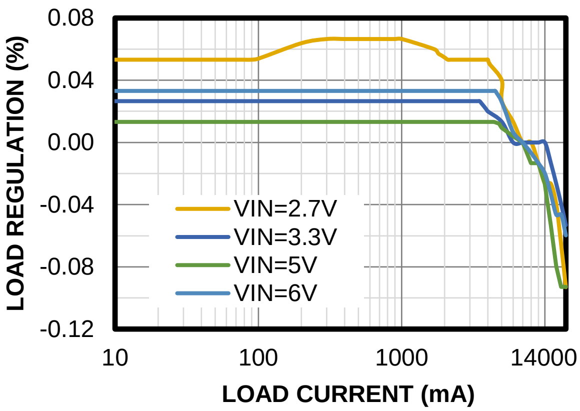
Load Regulation
FCCM, V_{OUT} = 0.75V, f_{SW} = 2MHz,
L = 100nH (DCR = 1.5mΩ)



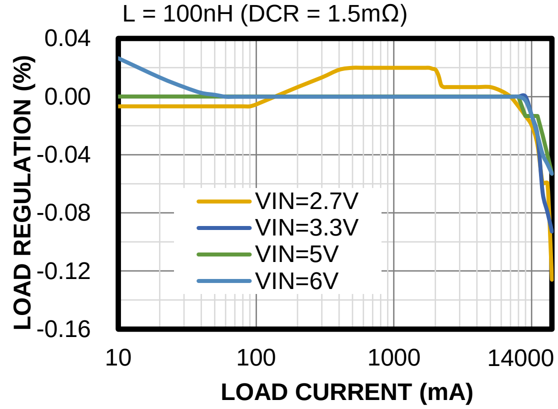
Load Regulation
FCCM, V_{OUT} = 0.75V, f_{SW} = 2.2MHz,
L = 100nH (DCR = 1.5mΩ)



Load Regulation
FCCM, V_{OUT} = 0.75V, f_{SW} = 3MHz,
L = 100nH (DCR = 1.5mΩ)



Load Regulation
FCCM, V_{OUT} = 0.75V, f_{SW} = 4MHz,
L = 100nH (DCR = 1.5mΩ)



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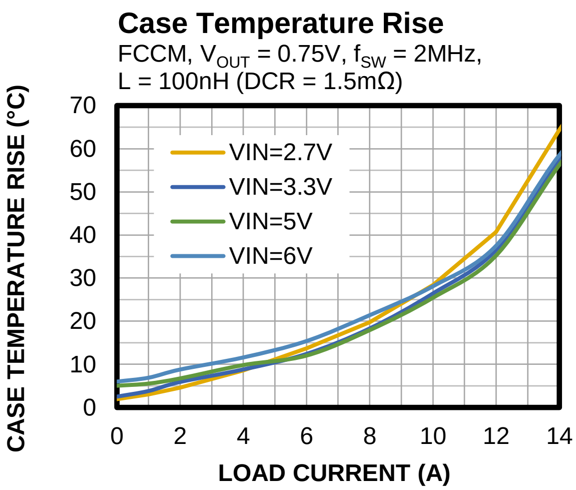
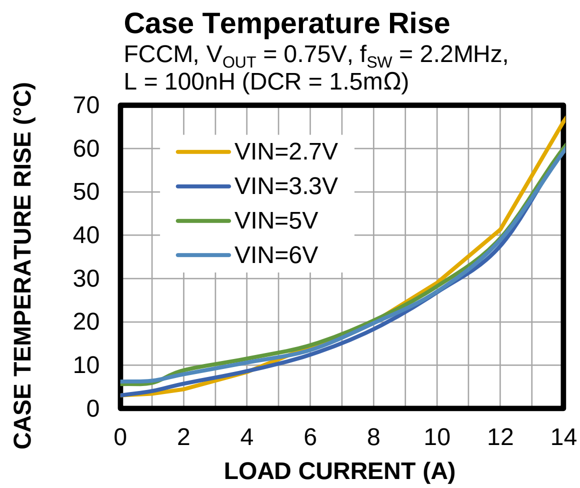
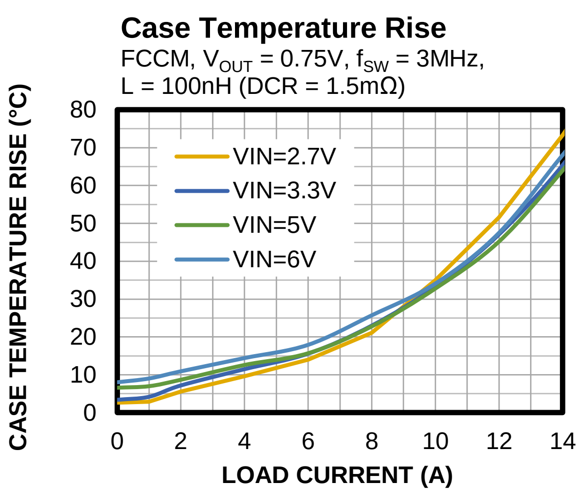
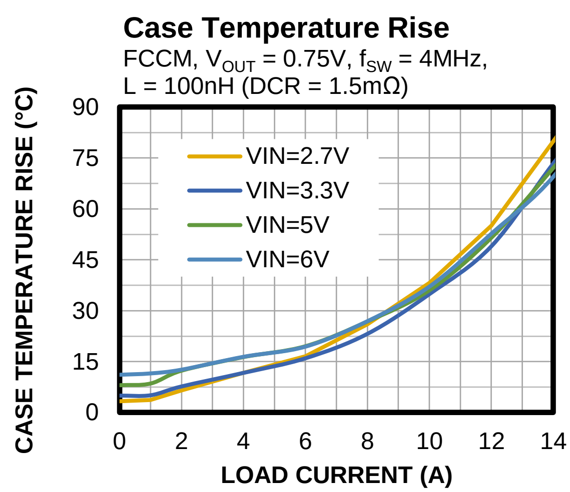
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 0.75V, L = 100nH, C_{OUT} = 4 x 47µF, f_{SW} = 3MHz, T_A = 25°C, unless otherwise noted.









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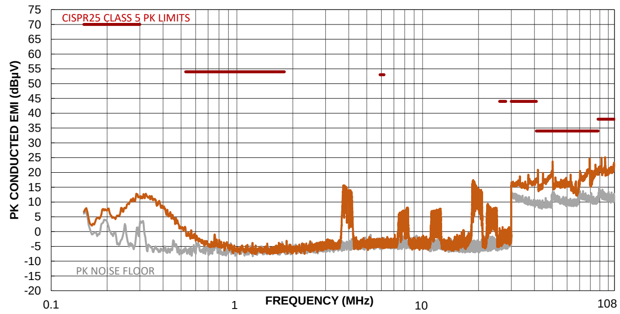
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 6V, V_{OUT} = 1.1V, L= 100nH [11], C_{OUT} = 4 x 47µF, f_{SW} = 4MHz, I_{OUT} = 14A, T_A = 25°C, unless otherwise noted. [12]

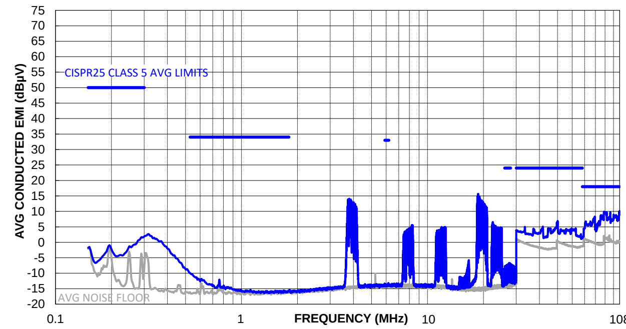
CISPR 25 Class 5 Peak Conducted Emissions

150kHz to 108MHz



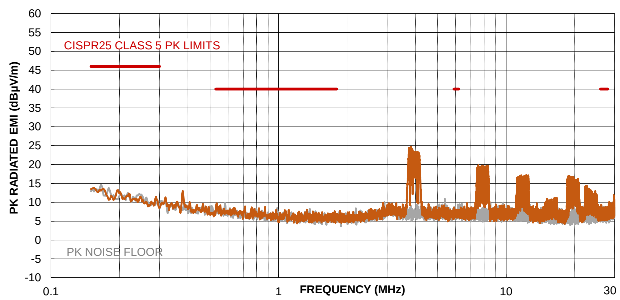
CISPR 25 Class 5 Average Conducted Emissions

150kHz to 108MHz



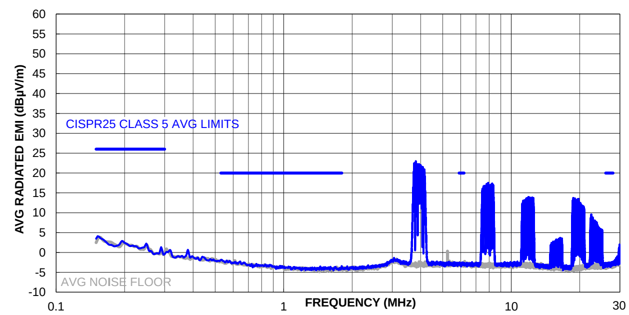
CISPR 25 Class 5 Peak Radiated Emissions

150kHz to 30MHz



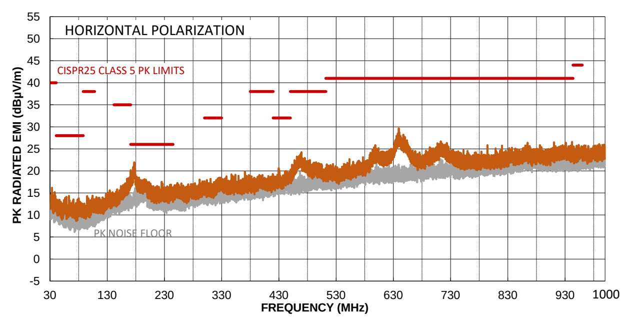
CISPR 25 Class 5 Average Radiated Emissions

150kHz to 30MHz



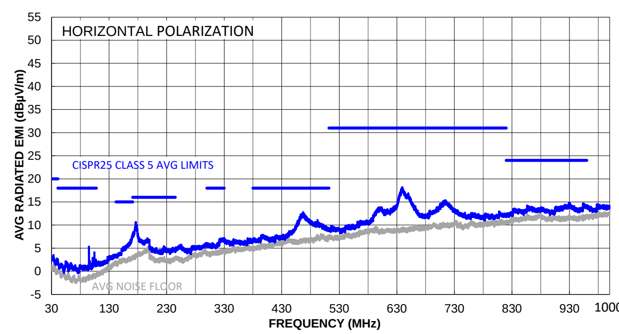
CISPR 25 Class 5 Peak Radiated Emissions

Horizontal, 30MHz to 1GHz



CISPR 25 Class 5 Average Radiated Emissions

Horizontal, 30MHz to 1GHz



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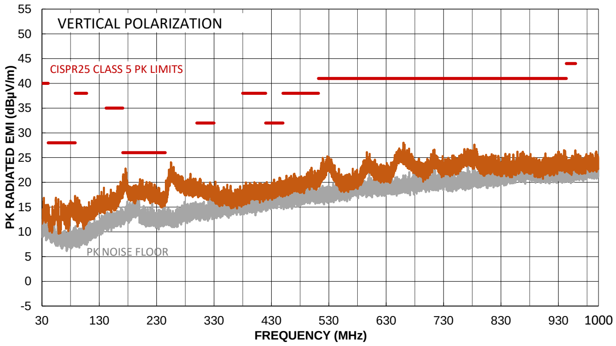
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 6V, V_{OUT} = 1.1V, L= 100nH (11), C_{OUT} = 4 x 47μF, f_{SW} = 4MHz, I_{OUT} = 14A, T_A = 25°C, unless otherwise noted. (12)

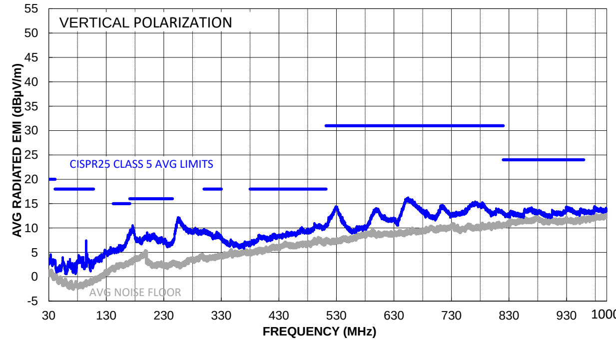
CISPR 25 Class 5 Peak Radiated Emissions

Vertical, 30MHz to 1GHz



CISPR 25 Class 5 Average Radiated Emissions

Vertical, 30MHz to 1GHz



Notes:

11) Inductor part number: HBED042T-R10MS-99; DCR = 1.3mΩ.
12) The EMC test results are based on the typical application circuit with EMI filters (see Figure 14 on page 58).

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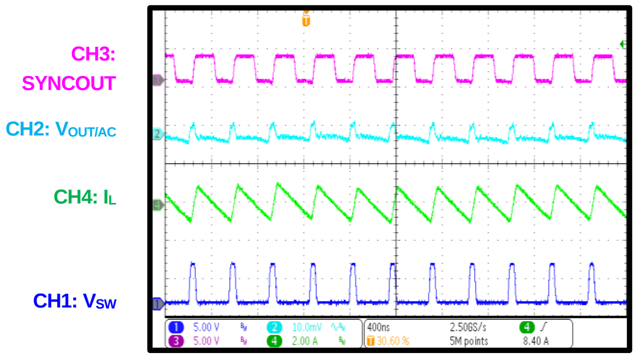
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 0.75V, L = 100nH, C_{OUT} = 4 x 47µF, f_{SW} = 3MHz, T_A = 25°C, unless otherwise noted.

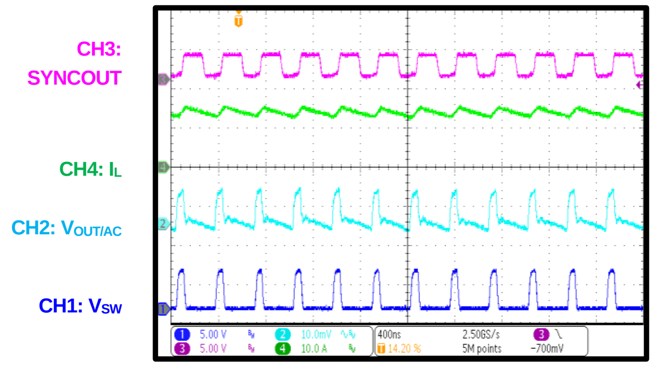
Steady State

I_{OUT} = 0A



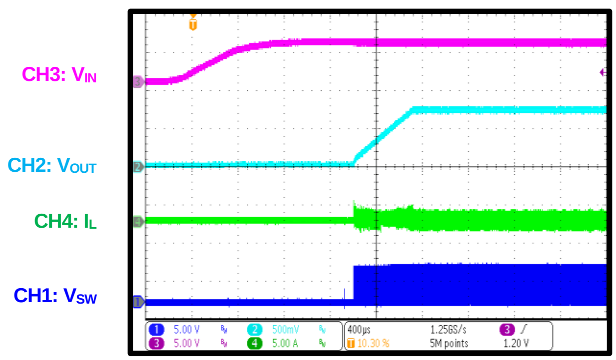
Steady State

I_{OUT} = 14A



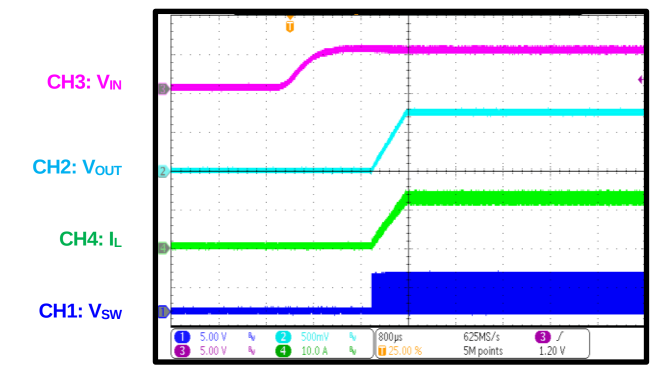
Start-Up through VIN

I_{OUT} = 0A



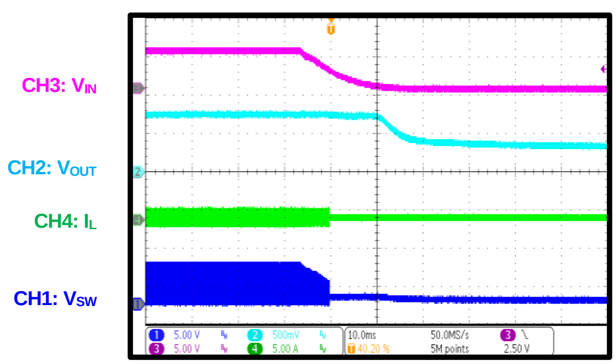
Start-Up through VIN

I_{OUT} = 14A



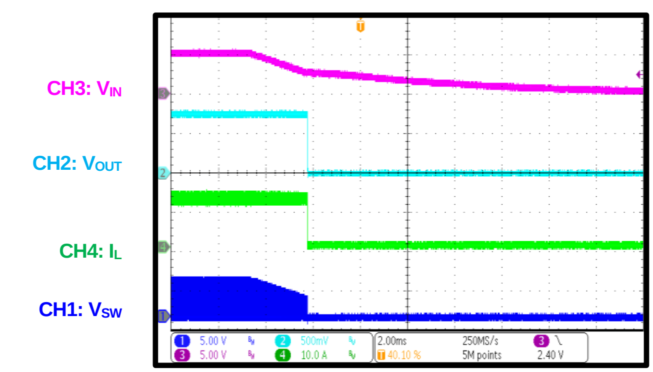
Shutdown through VIN

I_{OUT} = 0A



Shutdown through VIN

I_{OUT} = 14A



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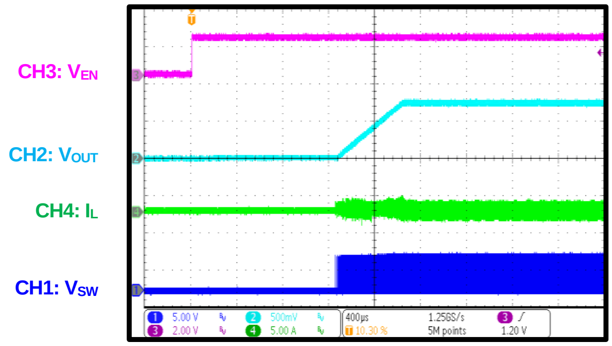
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 0.75V, L = 100nH, C_{OUT} = 4 x 47µF, f_{SW} = 3MHz, T_A = 25°C, unless otherwise noted.

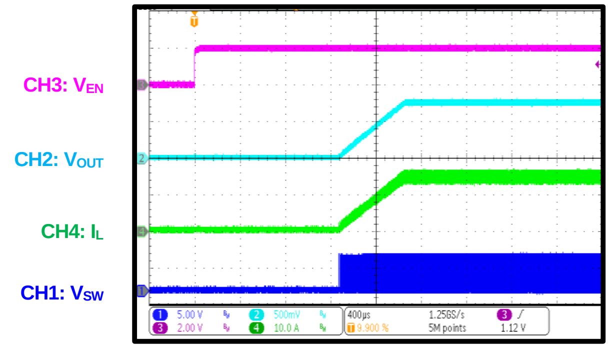
Start-Up through EN

I_{OUT} = 0A



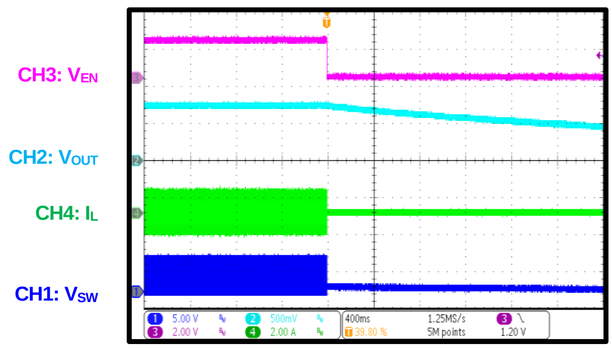
Start-Up through EN

I_{OUT} = 14A



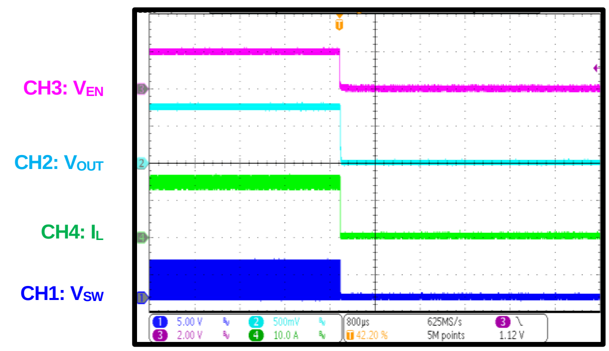
Shutdown through EN

I_{OUT} = 0A



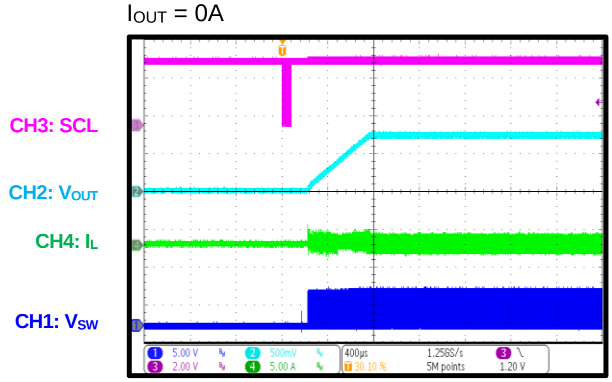
Shutdown through EN

I_{OUT} = 14A



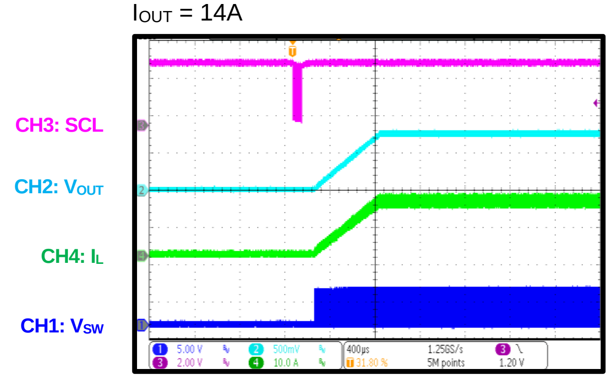
Start-Up via the PMBus Interface

I_{OUT} = 0A



Start-Up via the PMBus Interface

I_{OUT} = 14A



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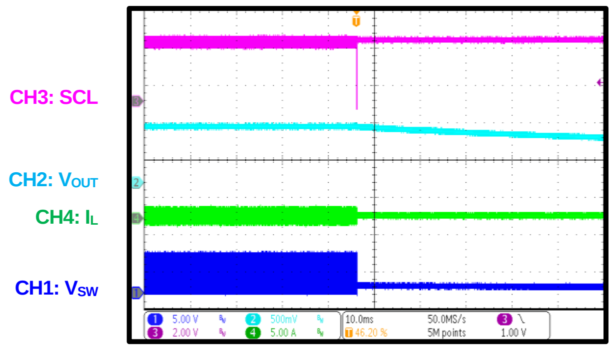
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 0.75V, L = 100nH, C_{OUT} = 4 x 47µF, f_{SW} = 3MHz, T_A = 25°C, unless otherwise noted.

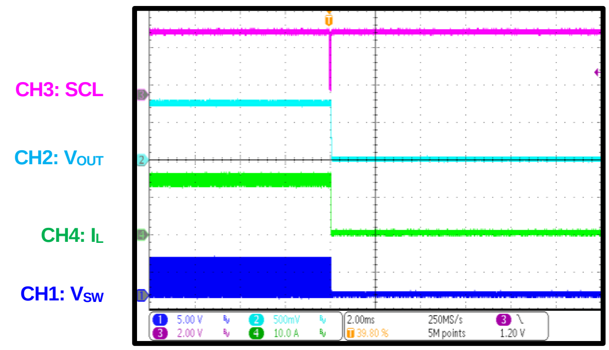
Shutdown via the PMBus Interface

I_{OUT} = 0A



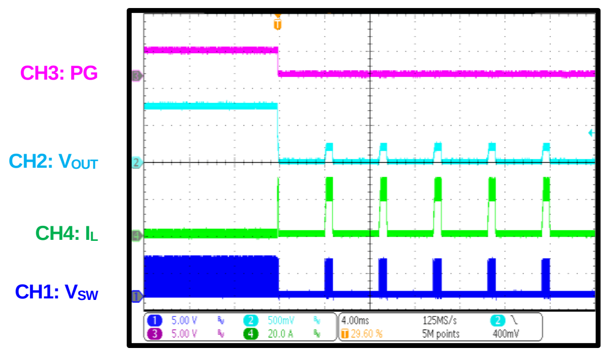
Shutdown via the PMBus Interface

I_{OUT} = 14A



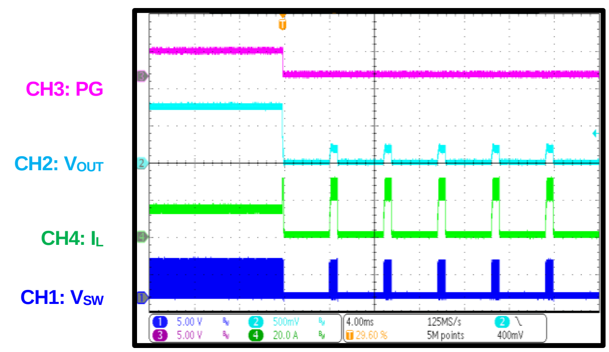
SCP Entry

I_{OUT} = 0A



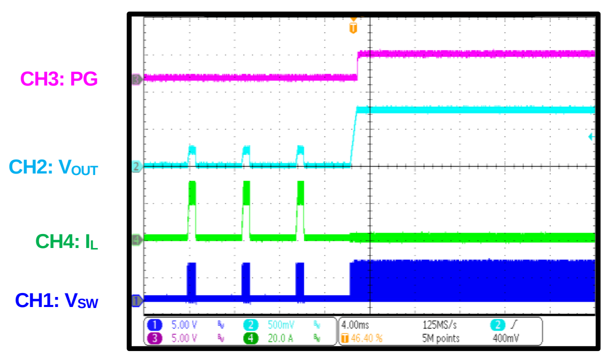
SCP Entry

I_{OUT} = 14A



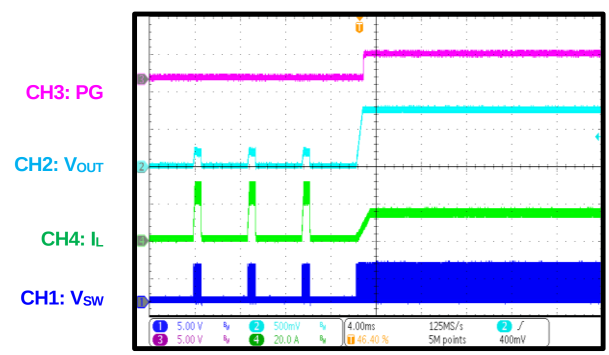
SCP Recovery

I_{OUT} = 0A



SCP Recovery

I_{OUT} = 14A



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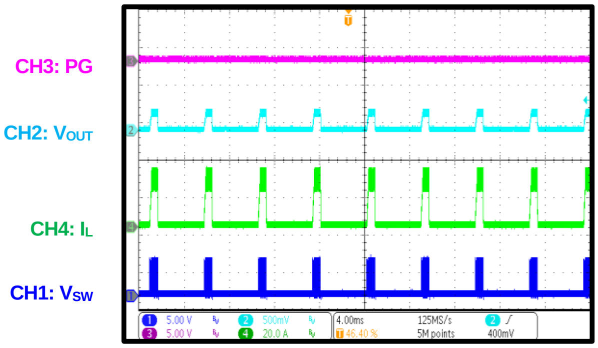
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 0.75V, L = 100nH, C_{OUT} = 4 x 47µF, f_{SW} = 3MHz, T_A = 25°C, unless otherwise noted.

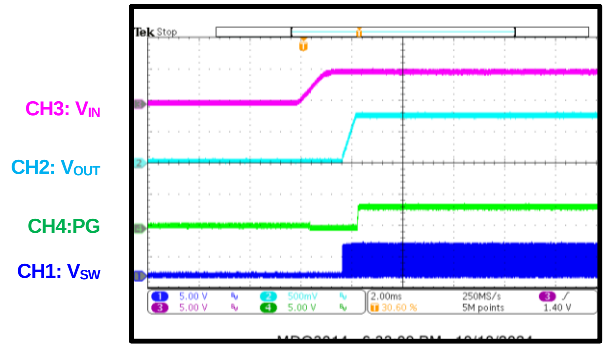
SCP Steady State

I_{OUT} = 0A



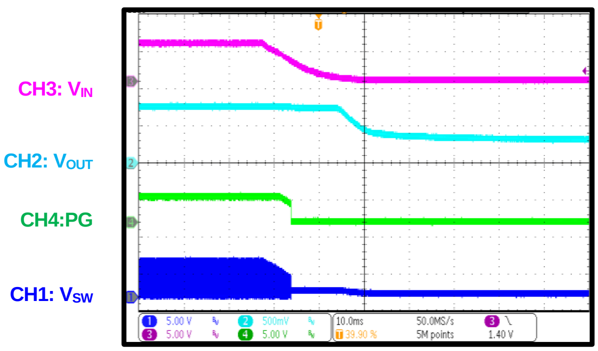
PG during Start-Up through VIN

I_{OUT} = 0A



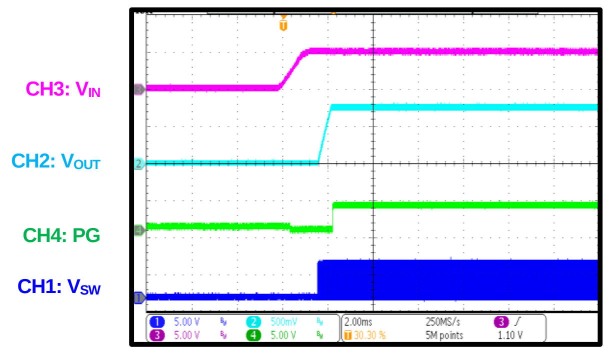
PG during Shutdown through VIN

I_{OUT} = 0A



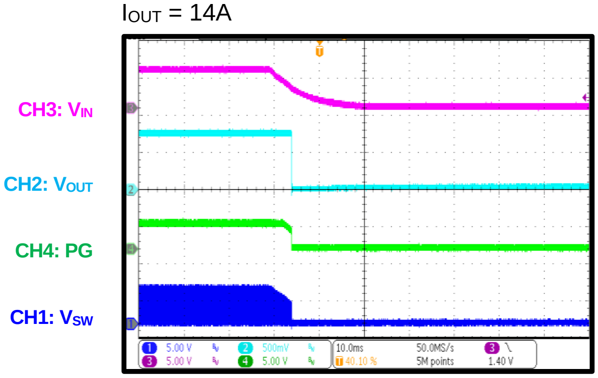
PG during Start-Up through VIN

I_{OUT} = 14A



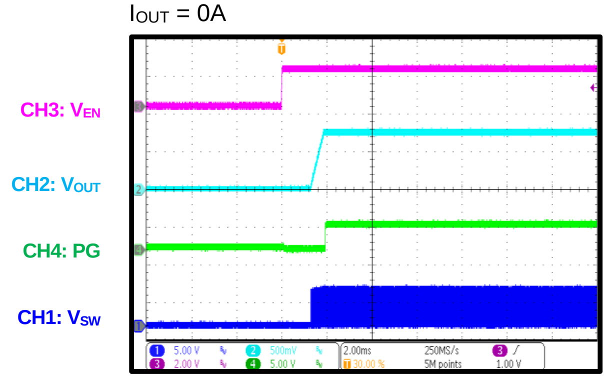
PG during Shutdown through VIN

I_{OUT} = 14A



PG during Start-Up through EN

I_{OUT} = 0A



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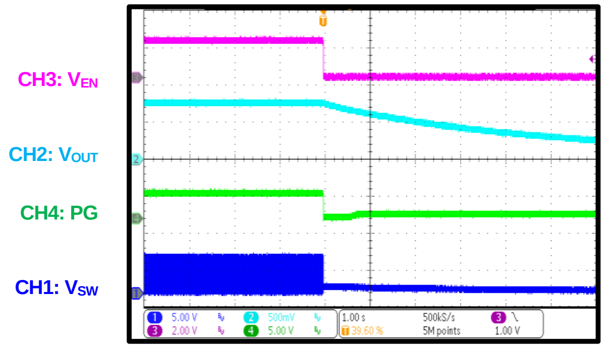
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 0.75V, L = 100nH, C_{OUT} = 4 x 47μF, f_{SW} = 3MHz, T_A = 25°C, unless otherwise noted.

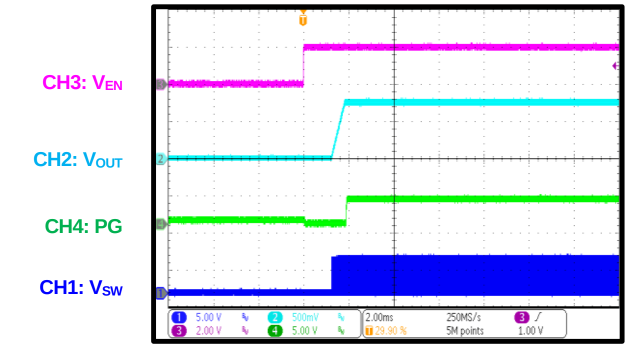
PG during Shutdown through EN

I_{OUT} = 0A



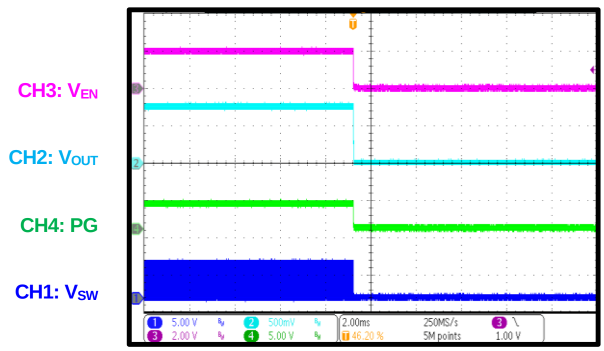
PG during Start-Up through EN

I_{OUT} = 14A



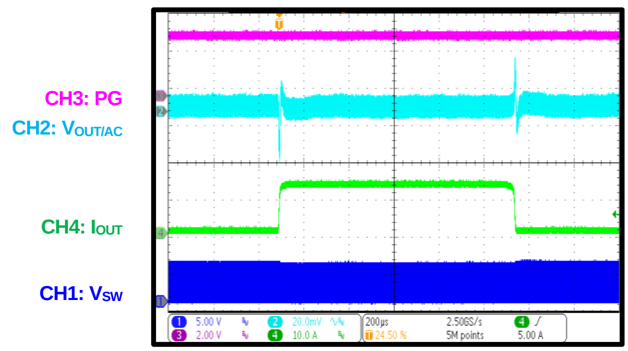
PG during Shutdown through EN

I_{OUT} = 14A



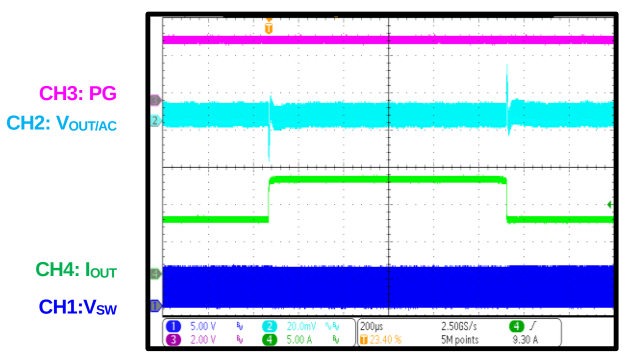
Load Transient Response

I_{OUT} = 0A to 14A,1.6A/μs



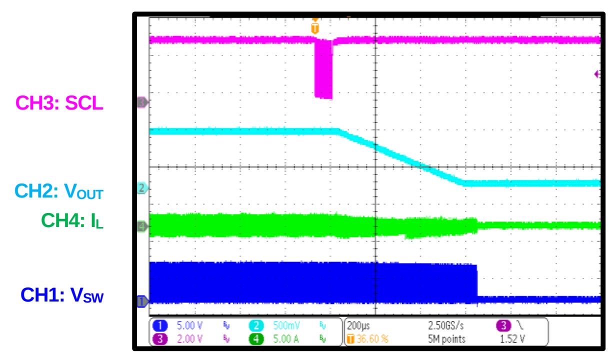
Load Transient Response

I_{OUT} = 7A to 14A,1.6A/μs



Soft Shutdown via the PMBus Interface

I_{OUT} = 0A



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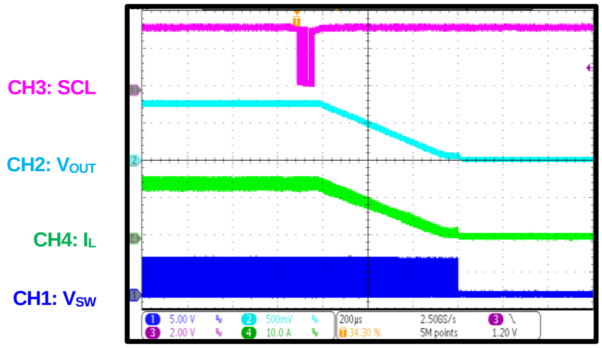
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 0.75V, L = 100nH, C_{OUT} = 4 x 47µF, f_{SW} = 3MHz, T_A = 25°C, unless otherwise noted.

Soft Shutdown via the PMBus Interface

I_{OUT} = 14A



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FUNCTIONAL BLOCK DIAGRAM

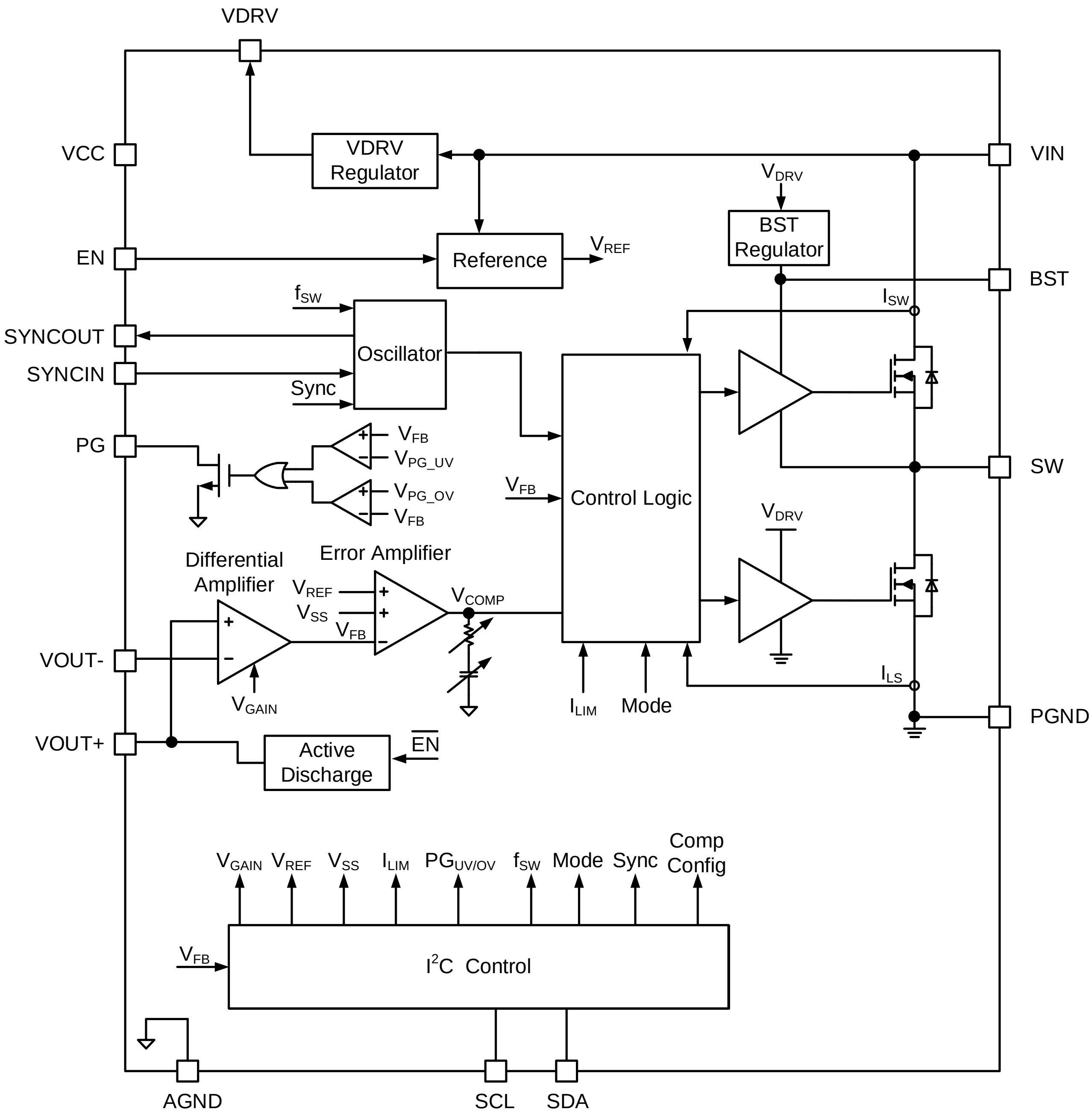

Figure 2: Functional Block Diagram

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OPERATION

The MPQ2287 is a high-efficiency, high-frequency, synchronous buck regulator with integrated internal high-side and low side-power MOSFETs (HS-FET and LS-FET, respectively). The device provides up to 14A of highly efficient output current (I_{OUT}) with fixed-frequency, zero-delay PWM (ZDP™) control.

The device features a configurable 2MHz to 4MHz switching frequency (f_{SW}), soft start, soft shutdown, and precision current limit. It also features a PMBus interface with packet error checking (PEC) and integrated multi-page one-time programmable (OTP) memory, which allows for a high degree of configurability.

Zero-Delay PWM (ZDP™) Control

Automotive applications generally require fixed-frequency operation to reduce EMI concerns, but traditional fixed control topologies have major limitations. Voltage mode control is difficult to compensate in automotive environments, while peak current mode struggles to keep up with stringent modern system-on-chip (SoC) transient requirements with excessive output capacitance. With these requirements in mind, the MPQ2287 implements fixed-frequency, zero-delay PWM (ZDP™) control.

ZDP™ control combines current information with hysteretic-style output voltage control in a clocked system. This provides a near optimal transient response while maintaining a high phase margin across a wide variety of operating conditions and external component values. In addition, it maintains superior EMI performance. The improved transient response decreases output capacitance requirements, which lowers system cost. Trailing edge modulation facilitates a narrow on time for high conversion ratio applications.

At the beginning of the pulse-width modulation (PWM) cycle, the HS-FET turns off and the LS-FET turns on immediately until the control signal reaches the COMP voltage. The HS-FET remains off for at least 80ns at the beginning of the cycle.

Light-Load Operation

Under light-load conditions, the MPQ2287 works in forced continuous conduction mode (FCCM). During FCCM, the MPQ2287 works with a fixed frequency across the no-load to full-load range. The advantages of FCCM are its constant frequency and lower output voltage ripple at light loads.

The MPQ2287 has a reverse current limit ($I_{LIMIT\_REVERSE}$) to prevent the negative current from dropping too low and damaging the components. Once the negative inductor current (I_L) reaches $I_{LIMIT\_REVERSE}$, the LS-FET turns off and the HS-FET turns on until I_L reaches the high-side recovery threshold ($I_{RECOVERY\_HS}$).

Internal Regulator VDRV and VCC

The internal 3.3V VDRV regulator powers the gate driver and BST supply. This regulator uses VIN as its input and operates across the full input voltage (V_{IN}) range. When V_{IN} exceeds 3.3V, VDRV is in full regulation. When V_{IN} is below 3.3V, the VDRV output degrades. Connect a 4.7µF capacitor from VDRV to PGND, and placed as close to the VDRV pin as possible, to decouple the supply.

Connect the VDRV supply to the VCC pin with a 2.2Ω resistor and decouple the VCC pin with a 2.2µF capacitor connected to AGND to provide the power supply to the rest of the MPQ2287.

Dynamic Voltage Scaling

The output voltage (V_{OUT}) can be adjusted via the PMBus interface during normal operation. When the voltage changes, the slope is determined by the PMBus interface's VOUT_SLEW register.

During the rising transition, the device maintains the previous mode. During the falling transition, the device automatically switches to FCCM.

Bootstrap Charging

The bootstrap capacitor is charged and regulated to about 3.3V by the dedicated internal bootstrap regulator. When the voltage between the BST and SW nodes is below its regulation value, a transistor connected from VDRV to BST turns on to charge the bootstrap capacitor.

When the HS-FET is on, BST exceeds VDRV, so the bootstrap capacitor cannot be charged. Under higher duty cycle conditions, the time available for bootstrap charging is shorter, so the bootstrap capacitor may not be sufficiently charged. In this scenario, the bootstrap refresh

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circuit turns off the HS-FET and turns on the LS-FET to ensure that the bootstrap capacitor is correctly charged.

Enable (EN) Control

EN is a digital control pin that turns the regulator on and off. Forcing the EN pin above the EN threshold turns on the device. The device turns off when the EN pin is driven below 1.1V.

SYNCIN

f_{SW} can be synchronized to the rising edge of an external clock signal applied at SYNCIN. The high amplitude of the SYNC clock should exceed 1.8V and have a low amplitude below 0.4V to drive the internal logic. The recommended external SYNC frequency is set to ±15% for the range between 2MHz and 4MHz.

The MPQ2287 operates in FCCM with a fixed frequency when there is a SYNC clock, regardless of I_{OUT}. A pulse longer than 200ns is recommended. Connect SYNCIN to GND through a resistor if it is not used.

SYNCOUT

The MPQ2287 can output the internal clock with a 0° or 180° phase shift. With this function, two devices can operate at the same frequency but 180° out of phase to reduce the total input current ripple. This allows a lower-value input bypass capacitor to be used.

Soft Start

The soft-start function is implemented to prevent V_{OUT} from overshooting during start-up. When the MPQ2287 starts up, the internal circuitry generates a soft-start voltage that ramps up from 0V. The soft-start period lasts until the voltage on the soft-start capacitor exceeds the reference voltage (V_{REF}). At this point, the error amplifier uses V_{REF} as the reference. There are four available soft-start slew rates, which can be configured via the OTP.

Soft Shutdown

Four shutdown slew rates are available to set the soft-shutdown time, which can be enabled via the OTP. The soft-shutdown function is implemented to discharge V_{OUT}. When the MPQ2287 starts to turn off, V_{REF} ramps down and V_{OUT} follows. This causes charge to transfer from the output to the input. The soft-shutdown slew rates can be configured via the OTP.

Minimum On Time and Minimum Off Time

When the device triggers the minimum on time (26ns), the MPQ2287's control loop automatically skips some pulses. The device does not reduce f_{SW} once the minimum off time (100ns) is triggered. This means that for applications with a low V_{IN} and a high V_{OUT}, V_{OUT} drops once the device reaches the minimum off time.

Output Discharge

An optional 120Ω discharge MOSFET is available, which can be configured via the OTP. When enabled, the discharge MOSFET turns on after the part is disabled. This MOSFET continues to operate as long as V_{IN} > 2.4V.

Pre-Biased Start-Up

If V_{OUT} exceeds 0V at start-up, both the HS-FET and LS-FET remain off until the soft-start ramp reaches V_{OUT}.

Power Good (PG) Indicator

The power good (PG) indicator is an open-drain output that indicates whether V_{OUT} is within the PG thresholds. PG can be connected to VCC through an external resistor (e.g. 100kΩ). When using the VCC pin as a pull-up voltage source, PG is at a low level when the part is disabled and EN = 0V. When using pull-up voltage sources other than VCC, an external circuit should be added to ensure that there is a low PG level when the part is disabled and EN = 0V (see Figure 3). The pin asserts (pulls low) if V_{OUT} is outside of the PG thresholds, the output is off, or if soft start/shutdown occurs. PG can also be configured to indicate thermal warning or PMBus interface communication failures via the OTP.

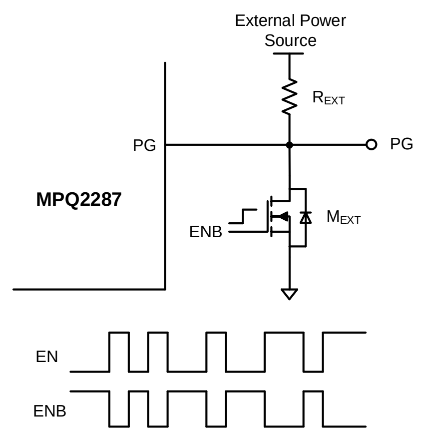

Figure 3: Recommended External Circuit for PG

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Table 1 shows the PG state based on different device input values if V_{IN} is present.

Table 1: PG State with V_{IN} Present

Circuit Configuration	EN	VCC	V_{OUT}	PG
PG pull-up to VCC	<0.65V	Off	-	Low
	0.65V ≤ V_{EN} < 1.2V	On	-	Low
	≥1.2V	On	Out of Range	Low
	≥1.2V	On	In Range	High
PG pull-up to ext. source	<0.65V	Off	-	High
	0.65V ≤ V_{EN} < 1.2V	On	-	Low
	≥1.2V	On	Out of Range	Low
	≥1.2V	On	In Range	High

Over-Current Protection (OCP)

The MPQ2287 implements cycle-by-cycle over-current protection (OCP) to limit I_{OUT}. The peak and valley current limits guarantee protection regardless of the duty cycle. It can be configured whether OCP causes a hiccup via the OTP.

When the inductor current (I_L) reaches the high-side peak current limit while the HS-FET is on, the HS-FET is forced off immediately to prevent the current from rising further. If the clock is received before I_L reaches current limit, the HS-FET also turns off due to the clock.

When the LS-FET is on, the next clock's rising edge is held until I_L drops below the low-side valley current limit. Then I_L can drop to a sufficiently low value when the HS-FET turns on again. This current limit scheme prevents current runaway if an overload or short-circuit event occurs. When OCP hiccup mode is enabled via the OTP, the output shuts off for the hiccup time after the valley current limit is triggered for a certain time (can be configured via the OTP), and restarts with a full soft-start period.

Short-Circuit Protection (SCP) and Under-Voltage Protection (UVP)

If V_{OUT} is below 75% of the configured output voltage, short-circuit protection (SCP) and output under-voltage protection (UVP) is triggered. The output shuts off for the hiccup time and restarts with a full soft-start period. It is possible to enable or disable output under-voltage protection via the OTP. If enabled, the output discharge function operates during the hiccup time.

Output Over-Voltage Protection (OVP)

If an output exceeds the output over-voltage protection (OVP) threshold, that output shuts off for the hiccup time, and then the normal soft-start process begins again. Enable output OVP via the OTP. If enabled, the output discharge function operates during the hiccup time.

Input Over-Voltage Protection (OVP)

If V_{IN} exceeds 6.7V, input OVP is triggered. The MPQ2287 starts operating once V_{IN} drops below the input OVP threshold (OVP rising threshold - OVP hysteresis).

Thermal Warning (TW)

If the die temperature exceeds the thermal warning threshold, the thermal warning register asserts. The power good function can be configured to indicate whether thermal warning has occurred via the PG_MAPPING register.

Thermal Shutdown (TSD)

If the die temperature exceeds the thermal shutdown threshold, the MPQ2287 disables switching and the PG pin asserts.

Multi-Page One-Time Programmable (OTP) Memory

The MPQ2287 features two user pages of OTP memory to store settings permanently.

For long-term reliability, a differential OTP cell is used instead of a single-ended cell. Data is stored on two floating gate avalanche injection metal oxide semiconductors (FAMOS), and output comparators are used for differential reading.

Only the MPQ2287-0000 code has OTP memory that can be written to twice; all other codes have OTP memory that can be written to once, or not at all. The OTP memory can be written to via the dedicated STORE_USER_ALL (15h) command.

Cyclic Redundancy Check (CRC)

The OTP memory is protected by a cyclic redundancy check (CRC). If the calculated CRC

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value does not match the recorded value during the power on process, the device does not start up.

Remote Output Voltage Sensing

The remote output voltage sensing function is implemented to compensate for the voltage drop in the copper between the MPQ2287, as well as the load caused by the large output current and the resistance in the transmission line.

Figure 4 shows the remote output voltage sensing circuit. Connect the VOUT+ and VOUT- pins close to the load with a Kelvin connection to accurately sense V_{OUT}. Ensure that there are enough capacitors to support the voltage at the load terminal.

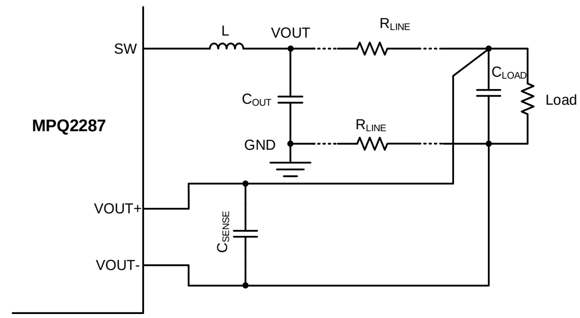

Figure 4: Remote Output Voltage Sensing Circuit

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PMBUS INTERFACE

PMBus Interface Description

The PMBus interface is an open-standard, power-management protocol that defines a means of communication with power conversion and other devices. The PMBus interface is a two-wire, bidirectional serial interface, consisting of a serial data line (SDA) and a serial clock line (SCL). The lines are externally pulled to a bus voltage when they are idle. Connecting to the line, a master device generates the SCL signal and device address, and arranges the communication sequence.

The MPQ2287 works as a slave-only device, which supports fast-mode plus (1Mbps) bidirectional data transfer, adding flexibility to the power supply solution. The output voltage, transition slew rate, and other converter parameters can be instantaneously controlled via the PMBus interface.

Data Validity

One clock pulse is generated for each data bit transferred. The data on the SDA line must be stable during the high period of the clock. The high or low state of the SDA line can only change when the clock signal on the SCL line is low (see Figure 5).

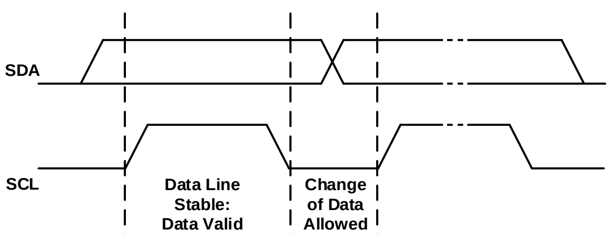

Figure 5: Bit Transfer on the PMBus Interface

Start and Stop Commands

The start and stop commands are signaled by the master device, which signifies the beginning and the end of the PMBus interface transfer. The start (S) command is defined as the SDA signal transitioning from high to low while the SCL line is high. The stop (P) command is defined as the SDA signal transitioning from low to high while the SCL is high (see Figure 6).

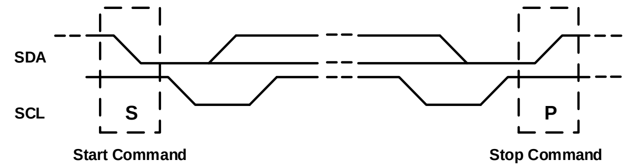

Figure 6: Start and Stop Command

Start and stop commands are always generated by the master. The bus is considered busy after the start command. The bus is considered free again after a certain time after the stop command. The bus stays busy if a repeated start (Sr) command is generated instead of a stop command. The start and repeated start commands are functionally identical.

Data Transfer

Every byte put on the SDA line must be 8 bits long. Each byte must be followed by an acknowledge (ACK) bit. The acknowledge-related clock pulse is generated by the master. The transmitter releases the SDA line (high) during the acknowledge clock pulse. The receiver must pull down the SDA line during the acknowledge clock pulse, so that it remains stable low during the high period of the clock pulse.

Figure 7 shows the data transfer format. After the start command, a slave address is sent. This address is 7 bits long followed by an 8th data direction bit (R/W). A 0 indicates a transmission (write), and a 1 indicates a request for data (read). Data transfer is always terminated by a stop command, which is generated by the master. However, if a master still wishes to communicate on the bus, it can generate a repeated start command and address another slave without first generating a stop command.

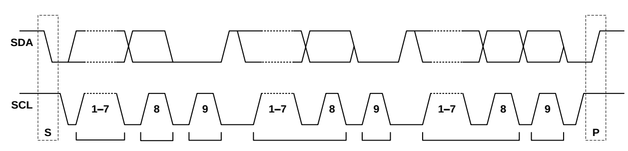

Figure 7: A Complete Data Transfer

Packet Error Checking (PEC)

The packet error checking (PEC) mechanism is employed to improve communication reliability and robustness. Whenever applicable, PEC is implemented by appending a packet error code after the data of each message transfer.

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The packet error code is a CRC-8 error-checking byte, calculated on all the message bytes, including addresses and read/write (R/W) bits. The code is appended to the message by the device that supplied the last data byte.

If an incorrect code is received, a communications fault is triggered. The power good flag asserts until the fault register is cleared.

PMBus Interface Communication Failure

A data transmission fault occurs when the data is not properly transferred between the devices. There are several data transmission faults, listed below:

- The host sends too little data
- The host reads too little data
- The host sends too many bytes
- The host reads too many bytes
- Improperly set read bit in the address byte
- Unsupported command code

The communication failure is recorded in the STATUS_CML register.

Write/Read Sequence

All PMBus interface commands are supported by the MPQ2287. There are five kinds of commands that can be implemented with or without PEC:

1) Send command only
2) Write byte
3) Write word
4) Read byte
5) Read word

If the master writes a command to a read-only register, the MPQ2287 performs the same action as it would if the host sent too many bytes. If the master sends a read command from a write-only register, the MPQ2287 performs the same action as it would if the host read too many bytes.

Figure 8 shows the write/read sequence without PEC. Figure 9 on page 37 shows the write/read sequence with PEC.

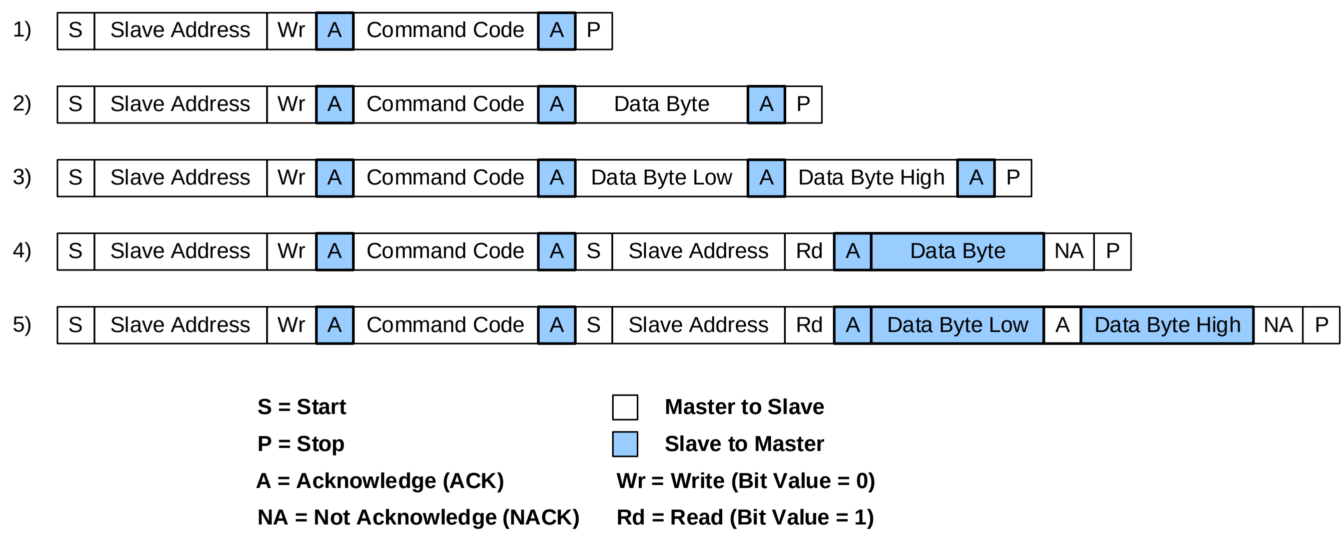

Figure 8: PMBus Interface Write/Read Sequence without PEC

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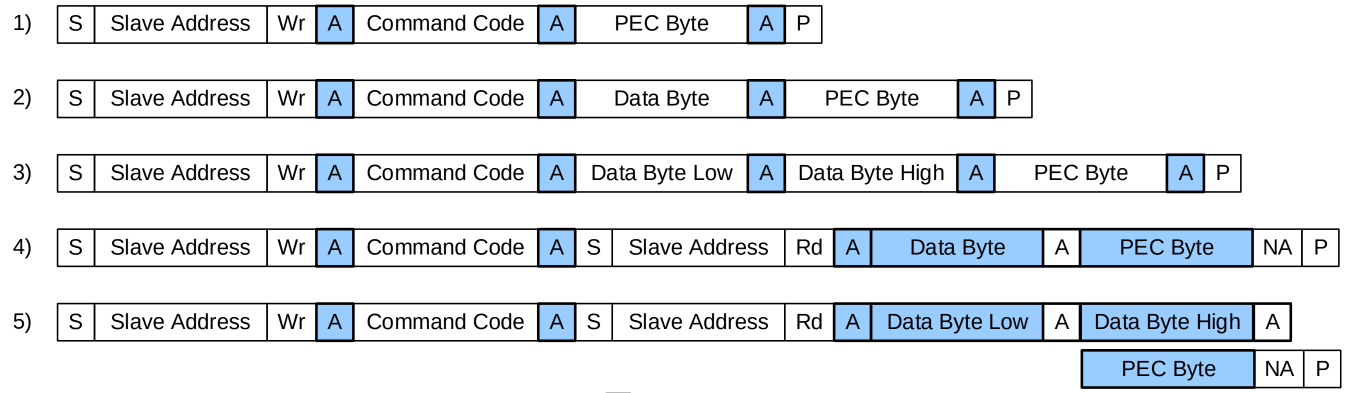

S = Start — **Master to Slave**
P = Stop — **Slave to Master**
A = Acknowledge (ACK) — **Wr = Write (Bit Value = 0)**
NA = Not Acknowledge (NACK) — **Rd = Read (Bit Value = 1)**

Figure 9: PMBus Interface Write/Read Sequence with PEC

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STATE MACHINE DESCRIPTION

The state machine describes the different states of operation. There are six states in the device: POWER OFF, RESTORE_OTP, START-UP, NORMAL, STORE_USER, and RESTORE_USER (see Figure 10).

Each state is described in greater detail below.

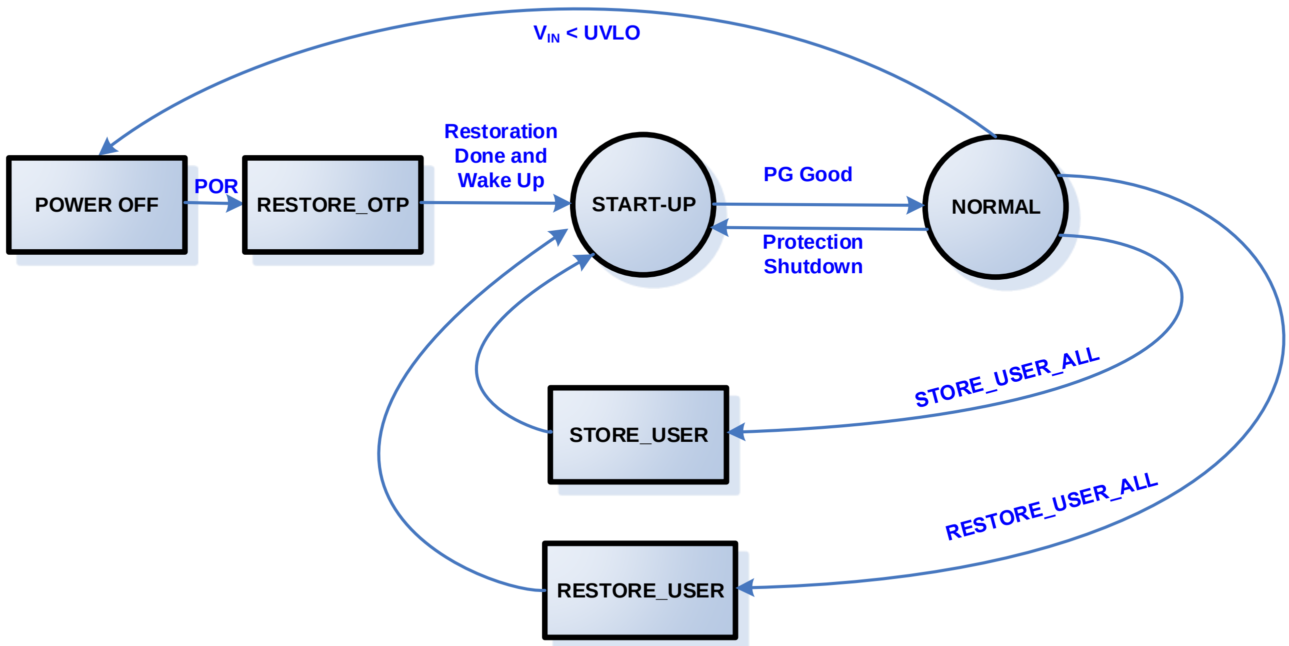

Figure 10: System State Machine

Power Off State (POWER OFF)

The MPQ2287 is in the power off state as long the power on reset (POR) is not released.

Restore the OTP State (RESTORE_OTP)

When V_{IN} exceeds its rising UVLO threshold, POR is released. The MPQ2287 restores the registers from the embedded OTP content data. Once restoration is complete, the MPQ2287 automatically enters the start-up state.

Start-Up State (START-UP)

Once restoring the OTP is complete and the wake-up signal is enabled, the device enters the start-up state. In the start-up state, all the other supplies are enabled and the output starts to ramp up.

Normal State (NORMAL)

The MPQ2287 enters the normal state as soon as the regulator's output voltage is power good. The normal state is the standard operating state for the MPQ2287, during which the output regulator is up and running.

Store User State (STORE_USER)

The store user state writes the present data from the registers to the internal OTP content. Then the MPQ2287 transitions to the start-up state and restarts. Only writing to the STORE_USER_ALL (15h) register from the normal state can force the device to enter the store user state. See the STORE_USER_ALL (15h) section on page 40 for more details.

Restore User State (RESTORE_USER)

The restore user state copies the entire contents of the OTP values to the matching locations in the registers. The values in the registers are overwritten by the value retrieved from the OTP. Any items in the OTP that do not have matching locations in the operating memory are ignored. Then the MPQ2287 transitions to the start-up state and restarts. Only writing to RESTORE_USER_ALL (16h) register from the normal state can force the device to enter the restore user state. See the RESTORE_USER_ALL (16h) section on 40 for more details.

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REGISTER MAP

Command Code	Command Name	Type	Bytes	OTP	Page 0
01h	OPERATION	R/W	1	Yes	✓
03h	CLEAR_FAULTS	W	0	No	✓
10h	WRITE_PROTECT	R/W	1	No	✓
15h	STORE_USER_ALL	W	0	No	✓
16h	RESTORE_USER_ALL	W	0	No	✓
19h	CAPABILITY	R	1	No	✓
20h	VOUT_MODE	R	1	No	✓
21h	VOUT_COMMAND	R/W	1	Yes	✓
24h	VOUT_MAX	R/W	1	Yes	✓
29h (13)	VOUT_SCALE	R/W	1	Yes	✓
2Bh	VOUT_MIN	R/W	1	Yes	✓
60h	TON_DELAY	R/W	1	Yes	✓
64h	TOFF_DELAY	R/W	1	Yes	✓
78h	STATUS_BYTE	R/W	1	No	✓
79h	STATUS_WORD	R/W	2	No	✓
7Ah	STATUS_VOUT	R/W	1	No	✓
7Bh	STATUS_IOUT	R/W	1	No	✓
7Ch	STATUS_INPUT	R/W	1	No	✓
7Dh	STATUS_TEMPERATURE	R/W	1	No	✓
7Eh	STATUS_CML	R/W	1	No	✓
9Bh	MFR_REVISION	R	1	No	✓
C4h	SECURE_LOCKOUT	R/W	1	No	✓
C5h	HICCUP_TIMER	R/W	1	Yes	✓
C6h	VOUT_STARTUP_SLEW	R/W	1	Yes	✓
C7h	VOUT_SHUTDOWN_SLEW	R/W	1	Yes	✓
C8h	VOUT_SLEW	R/W	1	Yes	✓
C9h	OUTPUT_DISCHARGE	R/W	1	Yes	✓
CAh	FREQUENCY_DITHER	R/W	1	Yes	✓
CBh	FREQUENCY_SET	R/W	1	Yes	✓
CCh	COMPENSATION_CONFIG	R/W	2	Yes	✓
CEh	PROTECTION_CONFIG	R/W	1	Yes	✓
CDh	PG_MAPPING	R/W	1	Yes	✓
CFh	PG_DELAY	R/W	1	Yes	✓
D0h	PG_CONFIG	R/W	1	Yes	✓
D1h	LIGHT_LOAD	R/W	1	Yes	✓
D2h	ILIM_SCALE	R/W	1	Yes	✓
D3h	ADDRESS	R/W	1	Yes	✓
D4h	CONFIGURATION_CODE	R	1	Yes	✓
D5h	MEMORY_CRC	R	2	Yes	✓
D6h	LATEST_PEC	R	1	No	✓
D8h	MFR_OTP_MEM_STATUS	R	1	No	✓
DBh	ADVANCED_CONFIG	W	1	No	✓
DCh	SUMMING_BLOCK_CONFIG	R/W	1	Yes	✓
DDh	MIN_ON_CONFIG	R/W	1	Yes	✓

Note:

13) This register value cannot be modified while the device is operating. Disable the output before modifying this register.

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REGISTER MAP (PAGE 0)

OPERATION (01h)

Format: Unsigned binary

The OPERATION command on Page 0 configures the converter output's on/off state, in conjunction with input from the EN pin.

Bits	Access	Bit Name	Default	Description
7	R/W	OPERATION	1'b1	1'b1: Output on (if enabled high) 1'b0: Output off
6:0	R	RESERVED	-	Unused. Writes are ignored and always read as 0.

CLEAR_FAULTS (03h)

The CLEAR_FAULTS command on Page 0 clears any fault bit in all status registers: STATUS_BYTE (78h), STATUS_WORD (79h), STATUS_VOUT (7Ah), STATUS_INPUT (7Ch), STATUS_TEMPERATURE (7Dh), and STATUS_CML (7Eh).

This command is write-only. There is no data byte for this command.

WRITE_PROTECT (10h)

Format: Unsigned binary

The WRITE_PROTECT command on Page 0 controls writing to the converter. The intent of this command is to provide protection against accident changes. It is not intended to provide protection against deliberate changes to the converter's configuration or operation. All the supported commands may have their parameters read, regardless of the WRITE_PROTECT settings.

Bits	Access	Bit Name	Default	Description
7:0	R/W	WRITE_PROTECT	8'b00000000	8'b10000000: Disable all writes except to the WRITE_PROTECT command 8'b01000000: Disable all writes except to the WRITE_PROTECT, OPERATION, and PAGE commands 8'b00100000: Disable all writes except to the WRITE_PROTECT, OPERATION, PAGE, and VOUT_COMMAND commands 8'b00000000: Enable writes to all commands Others: Invalid commands

STORE_USER_ALL (15h)

The STORE_USER_ALL command on Page 0 instructs the MPQ2287 to copy the contents of the operating memory to the matching locations in the OTP, except for the internal trim registers. This process begins when the MPQ2287 receives a STORE_USER_ALL command from the PMBus interface.

This command is write-only. There is no data byte for this command.

RESTORE_USER_ALL (16h)

The RESTORE_USER_ALL command on Page 0 instructs the MPQ2287 to copy the contents from the OTP and overwrite the matching locations in the operating memory, except for the trim registers. Any items in the OTP that do not have matching locations in the operating memory are ignored.

The RESTORE_USER_ALL command can be used while the MPQ2287 is operating. However, the MPQ2287 may be unresponsive during this operation with unpredictable, undesirable, or even catastrophic results.

This command is write-only. There is no data byte for this command.

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CAPABILITY (19h)

Format: Unsigned binary

The CAPABILITY command on Page 0 provides 1 byte to return key PMBus interface features that the MPQ2287 can support.

Bits	Access	Bit Name	Default	Description
7	R	PACKET_ERR_ CHECKING	1'b1	1'b1: Packet error checking (PEC) is supported Others: Invalid commands
6:5	R	MAX_BUS_SPEED	2'b10	2'b10: The maximum supported bus speed is 1MHz Others: Invalid commands
4	R	SMBALERT#	1'b0	1'b0: The device does not have a SMBALERT# pin and does not support the SMBus Alert Response protocol Others: Invalid commands
3	R	NUMERIC_FORMAT	1'b0	1'b0: Numeric data is in Linear11, ULinear16, Slinear16, or direct format Others: Invalid commands
2	R	AVSBUS_SUPPORT	1'b0	1'b0: AVSBus is not supported Others: Invalid commands
1:0	R	RESERVED	-	Reserved.

VOUT_MODE (20h)

Format: Unsigned binary

The VOUT_MODE command on Page 0 commands and reads the output voltage mode. The 3MSB determine the data format (only direct format is supported by the MPQ2287).

Bits	Access	Bit Name	Default	Description
7:0	R	VOUT_MODE	8'b010000 00	8'b01000000: Direct mode. The coefficients are m = 160, R = 0, and b = -33 Others: Invalid commands

VOUT_COMMAND (21h)

Format: Unsigned binary

The VOUT_COMMAND command on Page 0 sets V_{OUT}.

Bits	Access	Bit Name	Default	Description
7:0	R/W	VOUT_CMD	8'b011111 11	V_{OUT} can be calculated with the following equation: V_{OUT} = (VOUT_CMD x 6.25mV + 206.25mV) x VOUT_SL If VOUT_SL = 1, V_{OUT} can be set between 0.20625V and 1.8V. If VOUT_SL = 2, V_{OUT} can be set between 0.4125V and 3.6V.

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VOUT_MAX (24h)

Format: Unsigned binary

The VOUT_MAX command on Page 0 sets an upper limit on the V_{OUT} that the converter can command, regardless of any other commands or combinations. The intent of this command is to provide a safeguard against a user accidentally setting V_{OUT} to a possibly destructive level, rather than to be the primary output over-voltage protection (OVP).

Bits	Access	Bit Name	Default	Description
7:0	R/W	VOUT_MAX	8'b11111111	Sets the maximum V_{OUT}, which can be calculated with the following equation: V_{OUTMAX} = (VOUT_MAX x 6.25mV + 206.25mV) x VOUT_SL If VOUT_SL = 1, V_{OUT} can be set between 0.20625V and 1.8V. If VOUT_SL = 2, V_{OUT} can be set between 0.4125V and 3.6V. Attempting to write a higher value to VOUT_COMMAND causes VOUT_COMMAND to be set to VOUT_MAX, and asserts a VOUT_MAX_MIN warning.

VOUT_SCALE_LOOP (29h)

Format: Unsigned binary

The VOUT_SCALE_LOOP command on Page 0 sets the V_{OUT} scale.

Bits	Access	Bit Name	Default	Description
7:1	R/W	RESERVED	N/A	Reserved.
0	R/W	VOUT_SC_L	1'b0	Sets the V_{OUT} scale. Direct mode. The coefficients are m = 1, R = 0, and b = -1. 1'b0: VOUT_SL = 1 1'b1: VOUT_SL = 2

VOUT_MIN (2Bh)

Format: Unsigned binary

The VOUT_MIN command on Page 0 sets a lower limit on the V_{OUT} that the converter can command, regardless of any other commands or combinations. The intent of this command is to provide a safeguard against a user accidentally setting V_{OUT} to a possibly destructive level, rather than to be the primary output under-voltage protection (UVP).

Bits	Access	Bit Name	Default	Description
7:0	R/W	VOUT_MIN	8'b00000000	Sets the minimum V_{OUT}, which can be calculated with the following equation: V_{OUTMIN} = (VOUT_MIN x 6.25mV + 206.25mV) x VOUT_SL If VOUT_SL = 1, V_{OUT} can be set between 0.20625V and 1.8V. If VOUT_SL = 2, V_{OUT} can be set between 0.4125V and 3.6V. Attempting to write a lower value to VOUT_COMMAND causes VOUT_COMMAND to be set to VOUT_MIN, and asserts a VOUT_MAX_MIN warning.

TON_DELAY (60h)

Format: Unsigned binary

The TON_DELAY command on Page 0 sets the start-up delay time.

Bits	Access	Bit Name	Default	Description
7:5	R/W	RESERVED	-	Reserved.

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4:0	R/W	TON_DELAY	5’b00000	Sets the start-up delay time, calculated with the following equation: Start-Up Delay = TON_DELAY x 0.25ms The delay can range between 0ms and 7.75ms.

TOFF_DELAY (64h)

Format: Unsigned binary

The TOFF_DELAY command on Page 0 sets the shutdown delay time.

Bits	Access	Bit Name	Default	Description
7:5	R/W	RESERVED	-	Reserved.
4:0	R/W	TOFF_DELAY	5’b00000	Sets the shutdown delay time, calculated with the following equation: Shutdown Delay = TOFF_DELAY x 0.25ms The delay can range between 0ms and 7.75ms.

STATUS_BYTE (78h)

Format: Unsigned binary

The STATUS_BYTE command on Page 0 returns the value of a number of flags indicating the state of the MPQ2287. Send a CLEAR_FAULTS (03h) command to clear the fault flag bits after the fault is removed. See the CLEAR_FAULTS (03h) section on page 40 for more details.

Bits	Access	Bit Name	Default	Description
7	R/W	BUSY	1’b0	1’b0: No busy fault 1’b1: A fault was declared because the device was busy and unable to respond
6	R/W	OFF	1’b0	1’b0: The device is on 1’b1: The device is off
5	R/W	VOUT_OV_FAULT	1’b0	1’b0: No output over-voltage (OV) fault has occurred 1’b1: An output OV fault has occurred
4	R/W	IOUT_OC_HICCUP_FAULT	1’b0	1’b0: No output over-current (OC) hiccup fault has occurred 1’b1: An output OC hiccup fault has occurred
3	R/W	RESERVED	-	Reserved.
2	R/W	TEMPERATURE	1’b0	1’b0: No temperature fault or warning has occurred 1’b1: A temperature fault or warning has occurred
1	R/W	CML	1’b0	1’b0: No communications, memory, or logic fault has occurred 1’b1: A communications, memory, or logic fault has occurred
0	R/W	FAULT_OTHER	1’b0	1’b0: No other fault has occurred 1’b1: A fault not covered by bits[7:1] of this command has occurred

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STATUS_WORD (79h)

Format: Unsigned binary

The STATUS_WORD command on Page 0 returns 2 bytes of information with a summary of the device's fault/warning conditions. The higher byte gives more detailed information of the fault conditions. The lower byte is shared with the STATUS_BYTE (78h) register. Send a CLEAR_FAULTS (03h) command to clear the fault flag bits after the fault is removed. See the CLEAR_FAULTS (03h) section on page 40 for more details.

Bits	Access	Bit Name	Default	Description
15	R/W	VOUT_FAULT	1'b0	1'b0: No output voltage fault has occurred 1'b1: An output voltage fault has occurred
14	R/W	IOUT_FAULT	1'b0	1'b0: No output current fault has occurred 1'b1: An output current fault has occurred
13	R/W	VIN__FAULT	1'b0	1'b0: No input voltage fault has occurred 1'b1: An input voltage fault has occurred
12	R/W	MANUFAC_FAULT	1'b0	1'b0: No manufacturer-specific fault has occurred 1'b1: A manufacturer-specific fault has occurred
11	R/W	PGOOD	1'b0	1'b0: The power good (PG) pin is high 1'b1: The PG pin is low
10:8	R/W	RESERVED	-	Reserved.
Low Byte	R/W	STATUS_BYTE	8'b00000000	The same as STATUS_BYTE (78h) on page 42.

STATUS_VOUT (7Ah)

Format: Unsigned binary

The STATUS_VOUT command on Page 0 returns detailed fault information. Clear the fault flag bit by writing 1 to the relevant fault bit after this fault has been removed.

Bits	Access	Bit Name	Default	Description
7	R/W	VOUT_OV_FAULT	1'b0	1'b0: No output over-voltage (OV) fault has occurred 1'b1: An output OV fault has occurred
6:5	R/W	RESERVED	-	Reserved.
4	R/W	VOUT_UV_FAULT	1'b0	1'b0: No output under-voltage (UV) fault has occurred 1'b1: An output UV fault has occurred
3	R/W	VOUT_MAX_MIN_WARN	1'b0	1'b0: No attempt to set V_{OUT} beyond VOUT_MIN or VOUT_MAX has occurred 1'b1: An attempt to set V_{OUT} beyond VOUT_MIN or VOUT_MAX has occurred
2:0	R/W	RESERVED	-	Reserved.

STATUS_IOUT (7Bh)

Format: Unsigned binary

The STATUS_IOUT command on Page 0 returns detailed fault information. Clear the fault flag bit by writing 1 to the relevant fault bit after this fault has been removed.

Bits	Access	Bit Name	Default	Description
7	R/W	IOUT_OC_HICCUP_FAULT	1'b0	1'b0: No output over-current (OC) hiccup fault has occurred 1'b1: An output OC hiccup fault has occurred
6:0	R/W	RESERVED	-	Reserved.

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STATUS_INPUT (7Ch)

Format: Unsigned binary

The STATUS_INPUT command on Page 0 returns detailed fault information. Clear the fault flag bit by writing 1 to the relevant fault bit after this fault has been removed.

Bits	Access	Bit Name	Default	Description
7	R/W	VIN_OV_FAULT	1’b0	1’b0: No input over-voltage (OV) fault has occurred 1’b1: An input OV fault has occurred
6:0	R/W	RESERVED	-	Reserved.

STATUS_TEMPERATURE (7Dh)

Format: Unsigned binary

The STATUS_TEMPERATURE command on Page 0 returns detailed fault information. Clear the fault flag bit by writing 1 to the relevant fault bit after this fault has been removed.

Bits	Access	Bit Name	Default	Description
7	R/W	TEMP_OT_FAULT	1’b0	1’b0: No over-temperature (OT) fault has occurred 1’b1: An over temperature fault has occurred
6	R/W	TEMP_OT_ WARNING	1’b0	1’b0: No OT warning has occurred 1’b1: An OT warning has occurred
5:0	R/W	RESERVED	-	Reserved.

STATUS_CML (7Eh)

Format: Unsigned binary

The STATUS_CML command on Page 0 returns detailed fault information. Clear the fault flag bit by writing 1 to the relevant fault bit after this fault has been removed.

Bits	Access	Bit Name	Default	Description
7	R/W	INVALID_CMD	1’b0	1’b0: No invalid or unsupported command has been received 1’b1: An invalid or unsupported command has been received
6	R/W	INVALID_DATA	1’b0	1’b0: No invalid or unsupported data has been received 1’b1: Invalid or unsupported data has been received
5	R/W	PEC_ERROR	1’b0	1’b0: No PEC failure has occurred 1’b1: A PEC failure has occurred
4	R/W	MEMORY_FAULT	1’b0	1’b0: No CRC failure has occurred 1’b1: A CRC failure has occurred
3:0	R/W	RESERVED	-	Reserved.

SECURE_LOCKOUT (C4h)

Format: Unsigned binary

The SECURE_LOCKOUT command on Page 0 locks out access to most registers.

Bits	Access	Bit Name	Default	Description
7:0	R/W	SECURE_LOCKOUT	8’b000000 00	Write 01011010 to lockout write access to most registers. Registers 03h, 21h, 78h, 79h, 7Ah, 7Bh, 7Ch, 7Dh, and 7Eh can still be written. These bits can only be cleared by setting the enable (EN) signal to low. Other commands are invalid.

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HICCUP_TIMER (C5h)

Format: Unsigned binary

The HICCUP_TIMER command on Page 0 sets the hiccup timer.

Bits	Access	Bit Name	Default	Description
7:2	R/W	RESERVED	-	Reserved.
1:0	R/W	HICCUP_TIMER	2'b01	2'b00: 2ms 2'b01: 4ms 2'b10: 6ms 2'b11: 8ms

VOUT_STARTUP_SLEW (C6h)

Format: Unsigned binary

The VOUT_STARTUP_SLEW command on Page 0 sets the start-up slew rate.

Bits	Access	Bit Name	Default	Description
7:2	R/W	RESERVED	-	Reserved.
1:0	R/W	VOUT_STARTUP_ SLEW	2'b00	2'b00: VOUT_SL x 1.25mV/µs 2'b01: VOUT_SL x 2.5mV/µs 2'b10: VOUT_SL x 5mV/µs 2'b11: VOUT_SL x 10mV/µs

VOUT_ SHUTDOWN_SLEW (C7h)

Format: Unsigned binary

The VOUT_SHUTDOWN_SLEW command on Page 0 sets the shutdown slew rate.

Bits	Access	Bit Name	Default	Description
7:2	R/W	RESERVED	N/A	Reserved.
1:0	R/W	VOUT_SHUTDOWN_ SLEW	2'b00	2'b00: VOUT_SL x 1.25mV/µs 2'b01: VOUT_SL x 2.5mV/µs 2'b10: VOUT_SL x 5mV/µs 2'b11: VOUT_SL x 10mV/µs

VOUT_SLEW (C8h)

Format: Unsigned binary

The VOUT_SLEW command on Page 0 sets the V_{OUT} slew rate.

Bits	Access	Bit Name	Default	Description
7:2	R/W	RESERVED	-	Reserved.
1:0	R/W	VOUT_SLEW	2'b00	2'b00: VOUT_SL x 2.5mV/µs 2'b01: VOUT_SL x 5mV/µs 2'b10: VOUT_SL x 10mV/µs 2'b11: VOUT_SL x 20mV/µs

OUTPUT_DISCHARGE (C9h)

Format: Unsigned binary

The OUTPUT_DISCHARGE command on Page 0 configures the discharge mode during shutdown.

Bits	Access	Bit Name	Default	Description
7:2	R/W	RESERVED	-	Reserved.
1	R/W	SS_EN	1'b0	1'b0: Soft shutdown disabled 1'b1: Soft shutdown enabled

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0	R/W	DISCHARGE_EN	1'b0	1'b0: 120Ω output discharge disabled 1'b1: 120Ω output discharge enabled

FREQUENCY_DITHER (CAh)

Format: Unsigned binary

The FREQUENCY_DITHER command on Page 0 enables frequency spread spectrum (FSS).

Bits	Access	Bit Name	Default	Description
7:1	R/W	RESERVED	-	Reserved.
0	R/W	FREQUENCY_ DITHER	1'b1	Enables FSS. 1'b0: Disabled 1'b1: Enabled

FREQUENCY_SET (CBh)

Format: Unsigned binary

The FREQUENCY_SET command on Page 0 sets the SYNC output phase and the switching frequency (f_{SW}).

Bits	Access	Bit Name	Default	Description
7:3	R/W	RESERVED	-	Reserved.
2	R/W	SYNCO_PHASE	1'b1	Sets the SYNC output phase. 1'b0: 180° 1'b1: 0°
1:0	R/W	FREQUENCY_SET	2'b00	Sets f_{SW}. 2'b00: 2MHz 2'b01: 2.2MHz 2'b10: 3MHz 2'b11: 4MHz

COMPENSATION_CONFIG (CCh)

Format: Unsigned binary

The COMPENSATION_CONFIG command on Page 0 configures the compensation network parameters.

Bits	Access	Bit Name	Default	Description
15:10	R/W	RESERVED	-	Reserved.
9:7	R/W	CCOMP	3'b000	Sets C_{COMP}. 3'b000: 30pF 3'b001: 10pF 3'b010: 20pF 3'b011: 0pF 3'b100: 50pF 3'b110: 40pF Others: Invalid commands
6:4	R/W	CPOLE	3'b000	Sets C_{POLE}, calculated with the following equation: C_{POLE} = (COMPENSATION_CONFIG x 0.1pF + 20pF)

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3:0	R/W	RCOMP	4'b0000	Sets R_{COMP}. 4'b0000: 20Ω 4'b0001: 25kΩ 4'b0010: 50kΩ 4'b0011: 75kΩ 4'b0100: 100kΩ 4'b0101: 125kΩ 4'b0110: 150kΩ 4'b0111: 175kΩ 4'b1001: 225kΩ 4'b1010: 250kΩ 4'b1011: 275kΩ 4'b1100: 300kΩ 4'b1101: 325kΩ 4'b1110: 350kΩ 4'b1111: 400kΩ Others: Invalid commands

PROTECTION_CONFIG (CEh)

Format: Unsigned binary

The PROTECTION_CONFIG command on Page 0 enables certain functions.

Bits	Access	Bit Name	Default	Description
7:5	R/W	RESERVED	-	Reserved.
4	R/W	VIN_ OVP_EN	1'b1	1'b0: Disable input over-voltage protection (OVP) 1'b1: Enable input OVP
3:2	R/W	OCP_CONFIG	2'b11	Configures whether over-current protection (OCP) causes a hiccup. 2'b00: OCP does not directly cause a hiccup 2'b01: If the internal OCP signal lasts for 16µs due to an OC condition, a hiccup occurs 2'b10: If the internal OCP signal lasts for 32µs due to an OC condition, a hiccup occurs 2'b11: If the internal OCP signal lasts for 64µs due to an OC condition, a hiccup occurs
1	R/W	VOUT_OVP_EN	1'b0	1'b0: Disable output OVP 1'b1: Enable output OVP
0	R/W	VOUT_UVP_EN	1'b0	1'b0: Disable output under-voltage protection (UVP) 1'b1: Enable output UVP

PG_MAPPING (CDh)

Format: Unsigned binary

The PG_MAPPING command on Page 0 configures whether PG pulls low for certain PMBus interface and thermal warning errors.

Bits	Access	Bit Name	Default	Description
7:3	R/W	RESERVED	-	Reserved.
2	R/W	PM_CML_PG_ MAPPING	1'b0	Maps PG for PMBus interface communication failures. 1'b0: A PMBus interface communication failure causes PG to go low and register assertion 1'b1: A PMBus interface communication failure causes register assertion only

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1	R/W	PM_CRC_PGMAPPING	1’b0	Maps PG for a PMBus interface CRC failure. 1’b0: A PMBus interface CRC failure causes PG to go low and register assertion 1’b1: A PMBus interface CRC failure causes register assertion only
0	R/W	THERMAL_WARN_PGMAPPING	1’b0	Maps PG for a thermal warning. 1’b0: A thermal warning causes PG to go low and register assertion 1’b1: A thermal warning causes register assertion only

PG_DELAY (CFh)

Format: Unsigned binary

The PG _DELAY command on Page 0 sets the de-assertion delay for PG.

Bits	Access	Bit Name	Default	Description
7:2	R/W	RESERVED	-	Reserved.
1:0	R/W	PG_DELAY	2’b00	Sets the PG de-assertion delay. 2’b00: Immediate 2’b01: 2ms 2’b10: 5ms 2’b11: 10ms

PG_CONFIG (D0h)

Format: Unsigned binary

The PG_CONFIG command on Page 0 sets the power good (PG) threshold.

Bits	Access	Bit Name	Default	Description
7:1	R/W	RESERVED	-	Reserved.
0	R/W	PG_THRESHOLD	1’b1	Sets the PG threshold. 1’b0: ±4% of the set value 1’b1: ±6% of the set value

LIGHT_LOAD (D1h)

Format: Unsigned binary

The LIGHT_LOAD command on Page 0 sets the operation mode under light-load conditions.

Bits	Access	Bit Name	Default	Description
7:2	R/W	RESERVED	-	Reserved.
1	R/W	USM	1’b0	Sets the minimum frequency for ultrasonic mode. 1’b0: No minimum frequency 1’b1: 50kHz
0	R/W	FCCM	1’b0	Sets forced continuous conduction mode (FCCM). 1’b0: Reserved 1’b1: FCCM

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ILIM_SCALE (D2h)

Format: Unsigned binary

The ILIM_SCALE command on Page 0 sets the current limit scale. For the MPQ2287 at a 14A output current level, the current limit scale should be set to 150%. Other options do not guarantee that the current limit parameters conform to the Electrical Characteristics section starting on page 6.

Bits	Access	Bit Name	Default	Description
7:2	R/W	RESERVED	-	Reserved.
1:0	R/W	ILIM_SCALE	2’b00	Sets the current limit scale. 2’b00: 50% 2’b01: 75% 2’b10: 100% Other: Invalid commands

ADDRESS (D3h)

Format: Unsigned binary

The ADDRESS command on Page 0 sets the address for PMBus interface communication.

Bits	Access	Bit Name	Default	Description
7	R/W	RESERVED	-	Reserved.
6:0	R/W	ADDRESS	7’b0000011	Sets the 7-bit PMBus interface address.

CONFIG_CODE (D4h)

Format: Unsigned binary

The CONFIG_CODE command on Page 0 returns the configuration code.

Bits	Access	Bit Name	Default	Description
7:0	R	CONFIG_CODE	8’b00000000	Returns the configuration code.

MEMORY_CRC (D5h)

Format: Unsigned binary

The MEMORY_CRC command on Page 0 returns the OTP data.

Bits	Access	Bit Name	Default	Description
15:0	R	MEMORY_CRC	16’b0000000000000000	Returns the CRC for the OTP data.

LATEST_PEC (D6h)

Format: Unsigned binary

The LATEST_PEC command on Page 0 returns the latest calculated packet error code from the previous write transition.

Bits	Access	Bit Name	Default	Description
7:0	R	LATEST_PEC	8’b00000000	Stores the latest calculated packet error code from the previous write transition.

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MFR_OTP_MEM_STATUS (D8h)

Format: Unsigned binary

The MFR_OTP_MEM_STATUS command on Page 0 indicates whether certain OTP-related errors have occurred.

Bits	Access	Bit Name	Default	Description
7:3	R	RESERVED	-	Reserved.
2	R	STRUP_OTP_CRC_ERR	1’b0	0: No start-up load OTP CRC error has occurred 1: A start-up load OTP CRC error has occurred
1	R	STRUP_OTP_IND_ERR	1’b0	0: No start-up load OTP indicator error has occurred 1: A start-up load OTP indicator error has occurred
0	R	STORE_OTP_ERR	1’b0	0: No store OTP failure has occurred 1: A store OTP failure has occurred

ADVANCED_CONFIG (DBh)

Format: Unsigned binary

The ADVANCED_CONFIG command on Page 0 can enable advanced configuration read and write. The advanced configurations include the SUMMING_BLOCK_CONFIG (DCh) and MIN_ON_CONFIG (DDh) registers.

Bits	Access	Bit Name	Default	Description
7:0	R/W	ADVANCED	-	8’b11100001: Enable advanced configuration read and write Others: Disable advanced configuration read and write

SUMMING_BLOCK_CONFIG (DCh)

Format: Unsigned binary

The SUMMING_BLOCK_CONFIG command on Page 0 can sets loop performance parameters.

Bits	Access	Bit Name	Default	Description
7:6	R/W	RESERVED	-	Reserved.
5:3	R/W	CURRENT_SENSE_GAIN	3’b000	There are no units; this is a ratio compared to the nominal value of 1. 3’b000: 1 x ISENSE_GAIN_SCALE 3’b001: 0.75 x ISENSE_GAIN_SCALE 3’b010: 0.5 x ISENSE_GAIN_SCALE 3’b011: 0.25 x ISENSE_GAIN_SCALE 3’b100: 1.25 x ISENSE_GAIN_SCALE 3’b101: 1.5 x ISENSE_GAIN_SCALE 3’b110: 1.75 x ISENSE_GAIN_SCALE 3’b111: 2 x ISENSE_GAIN_SCALE
2:1	R/W	SLOPE_GM	2’b00	There are no units; this is a ratio compared to the nominal value of 1. 2’b00: 1 x SLOPE_GM_SCALE 2’b01: 0.5 x SLOPE_GM_SCALE 2’b10: 1.5 x SLOPE_GM_SCALE 2’b11: 2 x SLOPE_GM_SCALE
0	R/W	FB_GM	1’b0	1’b0: FB_GM divider = 1 1’b1: FB_GM divider = 2

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MIN_ON_CONFIG (DDh)

Format: Unsigned binary

The MIN_ON_CONFIG command on Page 0 sets the minimum on-time specifications and loop performance.

Bits	Access	Bit Name	Default	Description
7	R/W	ADAPTIVE_MIN_ON_FCCM	1'b0	Enables the adaptive minimum on time during FCCM. 1'b0: Enabled 1'b1: Disabled
6	R/W	ADAPTIVE_MIN_ON_SS	1'b0	Enables the adaptive minimum on time during soft start. 1'b0: Enabled 1'b1: Disabled
5	R/W	ISENSE_GAIN_SCALE	1'b0	Sets the scale for CURRENT_SENSE_GAIN. 1'b0: 1 1'b1: 2
4	R/W	SLOPE_GM_SCALE	1'b0	Sets the scale for SLOPE_GM. 1'b0: 1 1'b1: 2
3	R/W	RESERVED	-	Reserved
2:0	R/W	ADAPTIVE_MIN_ON	3'b000	Sets the minimum on time parameter. There are no units; this is a ratio compared to the nominal value of 1. The smaller the ratio, the greater the minimum on time. 3'b000: 1 3'b001: 0.8 3'b010: 0.6 3'b011: 0.4 3'b100: 1 3'b101: 1.2 3'b110: 1.4 3'b111: 1.6

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APPLICATION INFORMATION

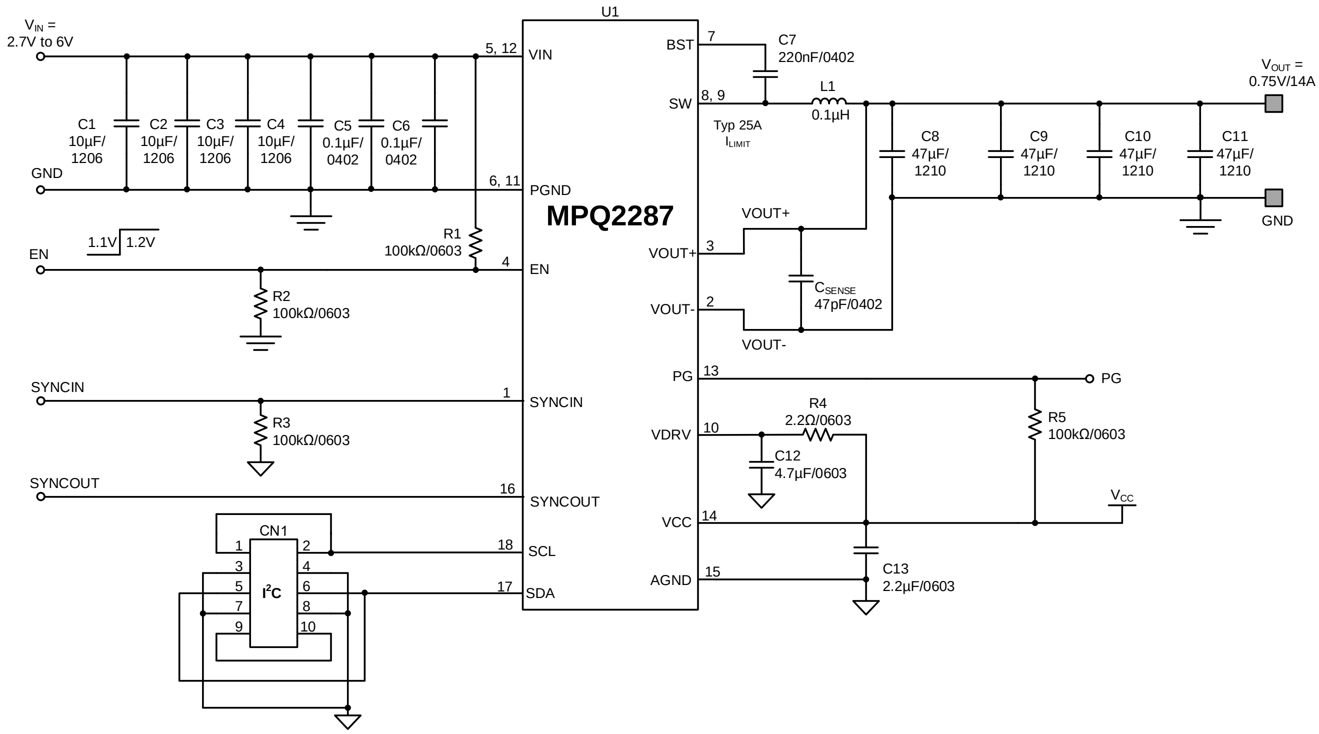

Figure 11: Typical Application Circuit (V_{OUT} = 0.75V, f_{SW} = 3MHz)

Table 2: Design Guide Index

Pin #	Pin Name	Component	Design Guide Index
1	SYNCIN	R3	External Sync Input (SYNCIN, Pin 1)
2	VOUT-	C_{SENSE}	Setting the Output Voltage (VOUT-, Pin 2; VOUT+, Pin 3)
3	VOUT+	C_{SENSE}	Setting the Output Voltage (VOUT-, Pin 2; VOUT+, Pin 3)
4	EN	R1, R2	Enable (EN, Pin 4)
5, 12	VIN	C1, C2, C3, C4, C5, C6	Selecting the Input Capacitor (VIN, Pins 5 and 12)
6, 11	PGND	-	GND Connection (PGND, Pin 6 and 11; AGND Pin 15)
15	AGND	-	GND Connection (PGND, Pin 6 and 11; AGND Pin 15)
7	BST	C7	Floating Driver and Bootstrap Charging (BST, Pin 7)
8, 9	SW	L1, C8, C9, C10, C11	Selecting the Inductor and Output Capacitor (SW, Pins 8 and 9)
10	VDRV	C12	Internal LDO Output (VDRV, Pin 10)
13	PG	R5	Power Good indicator (PG, Pin 13)
14	VCC	R4, C13	Supply Input for Internal Analog and Digital Circuits (VCC, Pin 14)
16	SYNCOUT	-	SYNC Output (SYNCOUT, Pin 16)
17	SDA	-	PMBus Interface (SDA, Pin 17; SCL, Pin 18)
18	SCL	-	PMBus Interface (SDA, Pin 17; SCL, Pin 18)

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External Sync Input (SYNCIN, Pin 1)

When the external clock signal is connected to the SYNCIN pin, the switching frequency can be synchronized to the rising edge. The high amplitude of the SYNC clock should exceed 1.8V, and its low amplitude should be below 0.4V to drive the internal logic. The recommended external SYNC frequency is ±15% the set frequency when the range is between 2MHz and 4MHz.

Setting the Output Voltage (VOUT-, Pin 2; VOUT+, Pin 3)

The OTP registers VOUT_COMMAND (21h) and VOUT_SCALE_LOOP (29h) set V_{OUT}.

Write to VOUT_COMMAND (21h), bits[7:0] (VOUT_CMD), and VOUT_SCALE_LOOP (29h), bit[0] (VOUT_SC_L). V_{OUT} can be calculated with Equation (1):

$$V_{OUT}\,(mV) = (VOUT\_CMD \times 6.25 + 206.25) \times VOUT\_SL \quad (1)$$

Set VOUT_SC_L to 0 when V_{OUT} is between 0.20625V and 1.8V. If V_{OUT} is between 1.8V and 3.6V, set VOUT_SC_L to 1. The output must be disabled via the PMBus interface when writing to VOUT_SC_L in VOUT_SCALE_LOOP (29h).

It is recommended to use another lower-value capacitor (e.g. 47pF) with a small package size (0402) to absorb high-frequency switching noise. Place the smaller capacitor as close to VOUT+ and VOUT- as possible.

Enable (EN, Pin 4)

EN is a digital control pin that turns the regulator on and off. When the EN pin's voltage exceeds 0.65V, the VDRV supply turns on. In this scenario, PMBus interface communication operates normally, and the host can read/write to the MPQ2287's registers normally. When the EN pin's voltage exceeds 1.2V, the MPQ2287 turns on.

Selecting the Input Capacitor (VIN, Pin 5 and 12)

The step-down converter has a discontinuous input current, and requires a capacitor to supply AC current to the converter while maintaining the DC input voltage. For the best performance, use low-ESR capacitors. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients.

It is recommended to use another lower-value capacitor (e.g. 0.1µF) with a small package size (0603) to absorb high-frequency switching noise. Place the lower-value capacitor as close to VIN and GND as possible.

Since the input capacitor (C_{IN}) absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in C_{IN} (I_{CIN}) can be estimated with Equation (2):

$$I_{CIN} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (2)$$

The worst-case condition occurs at V_{IN} = 2 x V_{OUT}, calculated with Equation (3):

$$I_{CIN} = \frac{I_{LOAD}}{2} \quad (3)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, add a small, high-quality ceramic capacitor (e.g. 0.1µF) as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide a sufficient charge to prevent excessive voltage ripple at the input. The input voltage ripple caused by the capacitance can be estimated with Equation (4):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (4)$$

GND Connection (PGND, Pin 6 and 11; AGND Pin 15)

See the PCB Layout Guidelines section on page 57 for more details.

Floating Driver and Bootstrap Charging (BST, Pin 7)

The BST capacitor (C7) is recommended to be 0.22µF.

The bootstrap capacitor is charged and regulated to about 3.3V by the dedicated internal bootstrap regulator. When the voltage between the BST and SW nodes is below its regulation value, a transistor connected from VDRV to BST turns on to charge the bootstrap capacitor.

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When the HS-FET is on, the BST voltage exceeds the VDRV voltage, so the bootstrap capacitor cannot be charged. At higher duty cycles, the time available for bootstrap charging is shorter, so the bootstrap capacitor may not be charged sufficiently. In this scenario, the bootstrap refresh circuit turns the HS-FET off and turns the LS-FET on to ensure that the bootstrap capacitor is correctly charged.

Selecting the Inductor and Output Capacitor (SW, Pin 8 and 9)

Selecting the Output Capacitor

The output voltage ripple can be calculated with Equation (5):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}}) \quad (5)$$

Where L is the inductor value and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

For ceramic capacitors, the capacitance dominates the impedance at the switching frequency and causes the majority of the output voltage ripple. For simplification, the output voltage ripple can be estimated with Equation (6):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}{}^2 \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (6)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be calculated with Equation (7):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (7)$$

The characteristics of the output capacitor also affect the stability of the regulation system. The MPQ2287 can be optimized for a wide range of capacitance and ESR values.

Selecting the Inductor

An inductor with a DC current rating at least 25% higher than the maximum load current is recommended for most applications. For higher efficiency, choose an inductor with a lower DC resistance. A larger-value inductor results in less ripple current and a lower output ripple voltage, but also has a larger physical size, higher series resistance, and lower saturation current. A good rule to determine the inductance is to allow the inductor ripple current to be approximately 30% of the maximum load current. The inductance can then be estimated with Equation (8):

$$L = \frac{V_{OUT}}{f_{SW} \times \Delta I_L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (8)$$

Where ΔI_L is the peak-to-peak inductor ripple current.

Choose the inductor ripple current to be approximately 30% of the maximum load current. The maximum inductor peak current can be calculated with Equation (9):

$$I_{LP} = I_{LOAD} + \frac{V_{OUT}}{2 \times f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (9)$$

Internal LDO Output (VDRV, Pin 10)

The VDRV capacitor's (C12) value is recommended to be about 4.7µF. The HS and LS drive circuits are powered by the internal VDRV regulator. This regulator uses VIN as its input and operates across the full V_{IN} range. When V_{IN} exceeds 3.3V, VDRV is in full regulation. When V_{IN} is below 3.3V, the VDRV output degrades.

Power Good (PG) Indicator (PG, Pin 13)

The PG pin is an open-drain output. If using PG, connect it to the VCC voltage via a pull-up resistor (R5, which is recommend to be about 100kΩ). PG asserts (pulls low) if the power is outside of the PG thresholds. The PG threshold can be configured by writing to PG_CONFIG (D0h), bit[0] (PG_THRESHOLD). The PG threshold is ±4% when PG_THRESHOLD is set to 0. The PG threshold is ±6% when PG_TRESHOLD is set to 1. See the Power Good (PG) Indicator section on page 32 for the detailed description of the PG state.

Supply Input for Internal Analog and Digital Circuits (VCC, Pin 14)

Connect the VDRV supply to the VCC pin with a 2.2Ω resistor, and decouple the VCC pin with a 2.2µF capacitor connected to AGND. The internal analog and digital circuits are powered by VCC, except for the HS and LS drive circuits.

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SYNC Output (SYNCOUT, Pin 16)

The pin can output the internal clock with a 0° or 180° phase shift. This phase shift can be configured via FREQUENCY_SET (CBh), bit[2] (SYNCO_PHASE).

PMBus Interface (SDA, Pin 17; SCL, Pin 18)

The MPQ2287 works as a slave-only device that supports fast-mode plus (1Mbps) bidirectional data transfer, adding flexibility to the power supply solution. See the PMBus Interface section on page 35 for more details.

The SCL and SDA lines are externally pulled to a bus voltage with resistor (e.g. 1.5kΩ).

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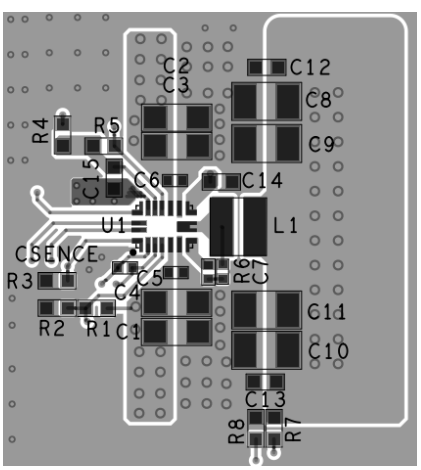
PCB Layout Guidelines [14]

Efficient PCB layout, especially for input capacitor placement, is critical for stable operation. A 4-layer layout is strongly recommended to improve thermal performance. For the best results, refer to Figure 12 and follow the guidelines below:

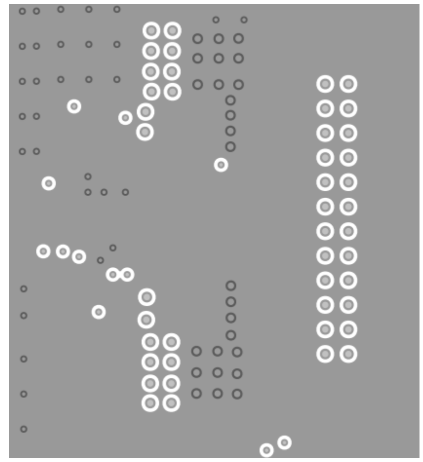
1. Place the symmetric input capacitors as close to VIN and GND as possible.
2. Use a large ground plane to connect to PGND directly.
3. Ensure that the high-current paths at GND and VIN have short, direct, and wide traces.
4. Place the ceramic input capacitor, especially the small package size (0603) input bypass capacitor, as close to VIN and PGND as possible to minimize high-frequency noise.
5. Keep the connection between the input capacitor and VIN as short and wide as possible.
6. Place the VCC capacitor as close to VCC and GND as possible.
7. Route SW away from sensitive analog areas, such as FB.
8. Ensure that the trace between FB and the output is as short as possible.
9. Use multiple vias to connect the power planes to the internal layers.

Notes:

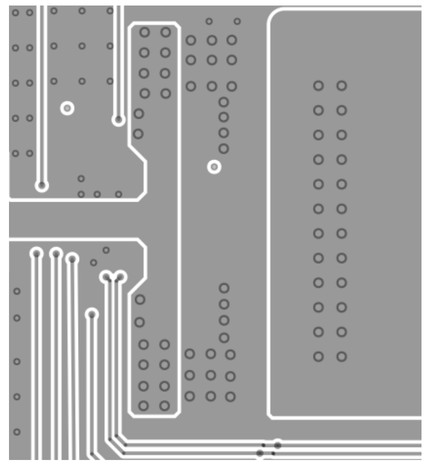
14) The recommended PCB layout is based on Figure 14 on page 58.



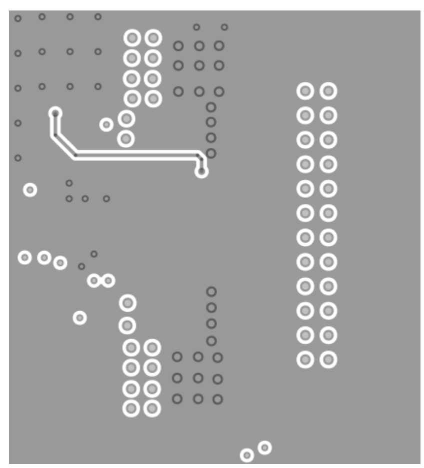
Top Layer



Mid-Layer 1



Mid-Layer 2



Bottom Layer

Figure 12: Recommended PCB Layout

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TYPICAL APPLICATION CIRCUITS

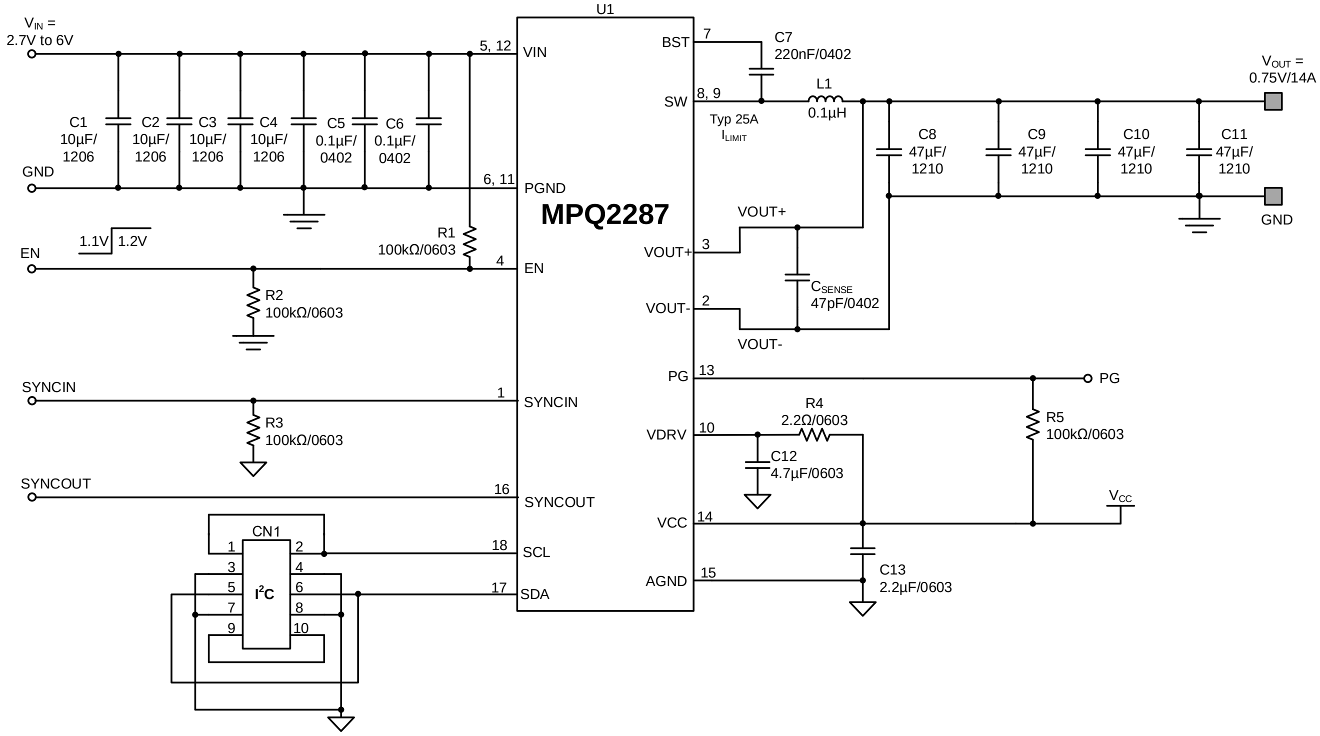

Figure 13: Typical Application Circuit (V_{OUT} = 0.75V, I_{OUT} = 14A, f_{SW} = 3MHz)

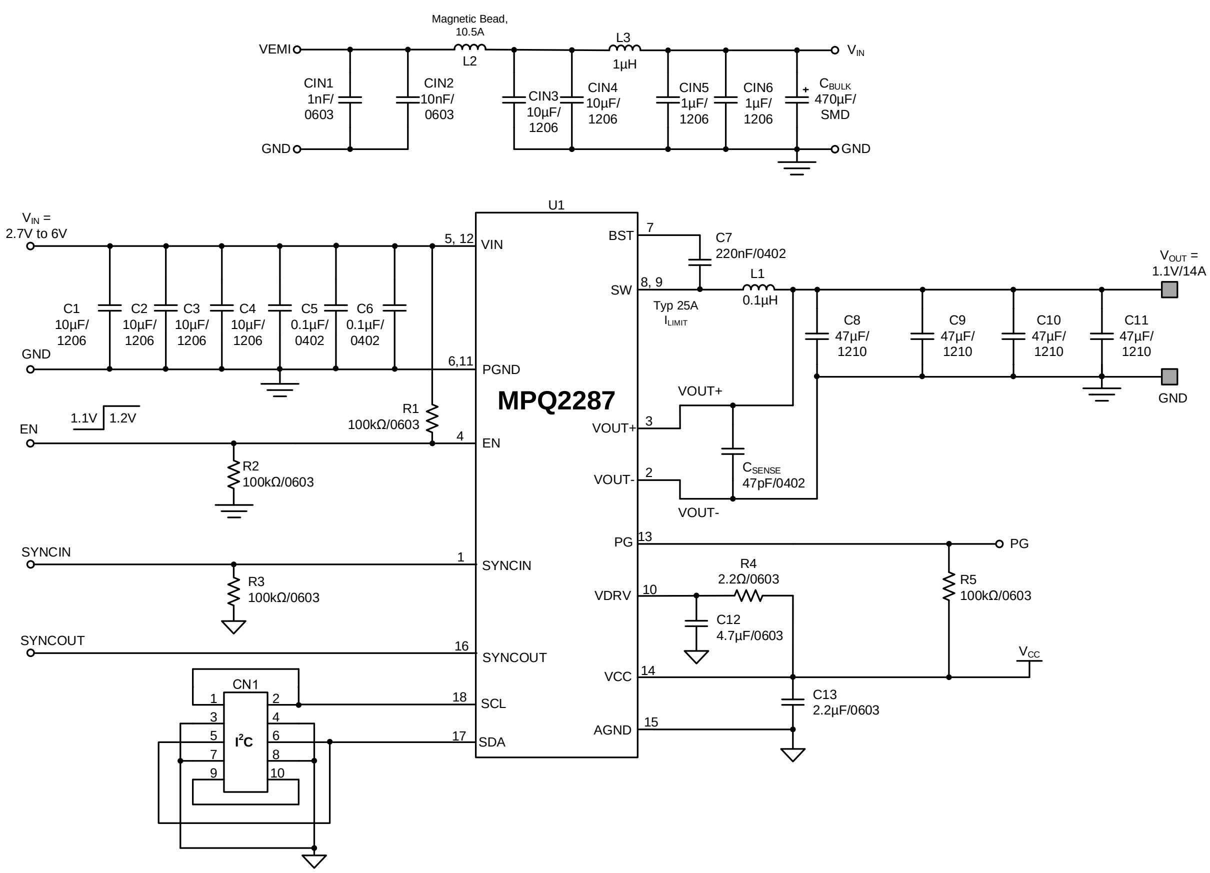

Figure 14: Typical Application Circuit (V_{OUT} = 1.1V, I_{OUT} = 14A, f_{SW} = 4MHz with EMI Filter)

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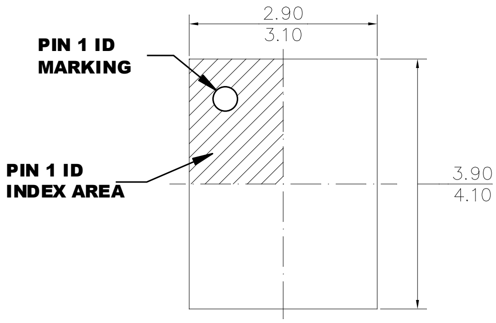
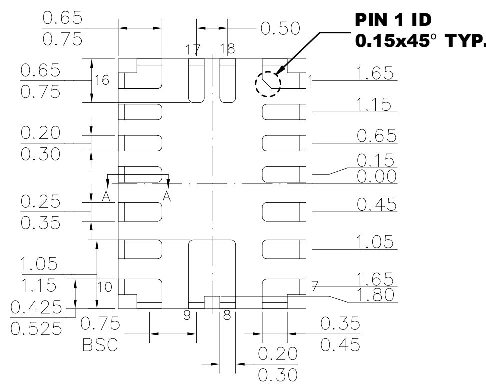
PACKAGE INFORMATION

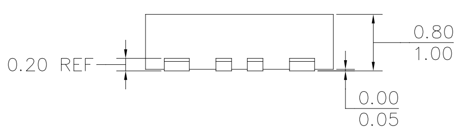
QFN-18 (3mmx4mm)
Wettable Flank



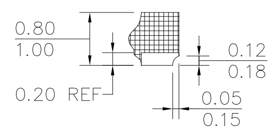
TOP VIEW



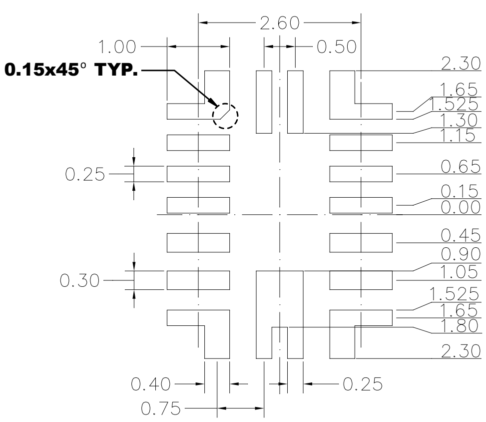
BOTTOM VIEW



SIDE VIEW



SECTION A-A



RECOMMENDED LAND PATTERN

NOTE:

1)THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

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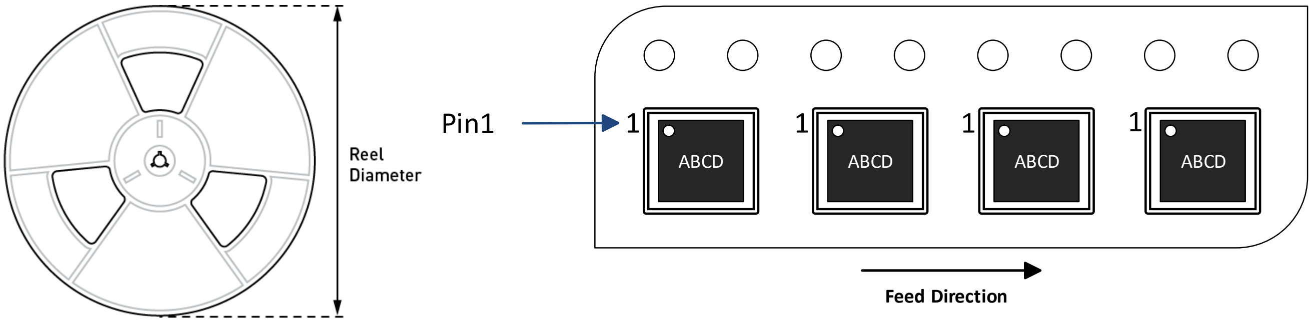
CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ2287GLE-xxxx-AEC1-Z	QFN-18 (3mmx4mm)	5000	N/A	N/A	13in	12mm	8mm

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REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	2/18/2025	Initial Release	-

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