MPQ2211

6V, 12A, 2.2MHz, Configurable Current Limit, Synchronous Step-Down Converter, AEC-Q100 Qualified

DESCRIPTION

The MPQ2211 is a fully integrated, high-frequency, synchronous buck converter. It offers a very compact solution to achieve up to 12A of output current (I_{OUT}) across a wide input voltage (V_{IN}) supply range with excellent load and line regulation. The MPQ2211 operates at high efficiency across the wide I_{OUT} load range.

The MPQ2211 adopts internally compensated constant-on-time (COT) control to provide fast transient response and facilitate loop stabilization. Pulse-skip mode (PSM) enables non-synchronous operation to optimize light-load efficiency.

The MPQ2211 has a fixed 2.2MHz frequency, which enables the MPQ2211's frequency to remain constant regardless of the input and output voltages.

The output voltage (V_{OUT}) start-up ramp is controlled by an internal 0.9ms timer, which can be lengthened by adding a capacitor on the SSTT pin. An open-drain power good (PG) signal indicates whether the output is within its nominal voltage range. The PG pin is clamped to about 0.7V with an external pull-up voltage when the input supply fails to power the MPQ2211.

Fully integrated protections include over-current protection (OCP), over-voltage protection (OVP), under-voltage protection (UVP), and over-temperature protection (OTP).

The MPQ2211 requires a minimal number of readily available, standard external components, and is available in an LGA-19 (3mmx3.5mm) package.

FEATURES

- Designed for Automotive Point-of-Load (PoL) Applications
  - Wide Operating Input Voltage (V_{IN}) Range from 3V
    - 3V to 3.6V with VCC Bias to VIN
    - 4V to 6V with Internal Bias
- Up to 12A Continuous Output Current (I_{OUT})

FEATURES *(continued)*

- Configurable Accurate Current Limit Level
- Constant-on-Time (COT) Control Provides an Excellent Transient Response
- Available in AEC-Q100 Grade 1
- Increases Battery Life
  - Pulse-Skip Mode (PSM) at Light Loads
  - 13.3mΩ and 3.8mΩ Internal Power MOSFET Switches
- Optimized for EMC/EMI
  - 2.2MHz Switching Frequency (f_{SW}) in Forced Continuous Conduction Mode (FCCM)
  - MeshConnect™ Flip-Chip Package
- Additional Features
  - Power Good (PG) Active-Clamped at Low Level during Power Failure
  - Output Voltage (V_{OUT}) Discharge
  - V_{OUT} Tracking
  - ±1% 0.5V Feedback (FB) Accuracy
  - Configurable Soft-Start Time from 0.9ms
  - Adjustable Output Up to 3.6V
  - Non-Latch Over-Current Protection (OCP), Under-Voltage Protection (UVP), Under-Voltage Lockout (UVLO), Thermal Shutdown, and Latch-Off for Over-Voltage Protection (OVP)
  - Available in an LGA-19 (3mmx3.5mm) Package
- Functional Safety System Design Capable
  - MPSafe™ Compatible – Functional Safety Supporting Document Available

MPSafe™ FuSa Compatible

APPLICATIONS

- Automotive ADAS
- Automotive Infotainment Systems
- System-on-Chip (SoC) System Cores
- DDR Memory

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TYPICAL APPLICATION

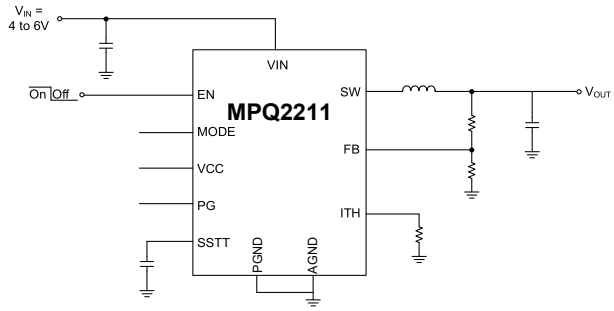


Figure 1: Typical Application (V_{IN} = 4V to 6V)

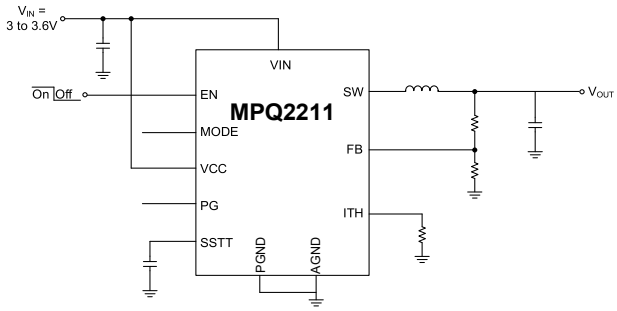
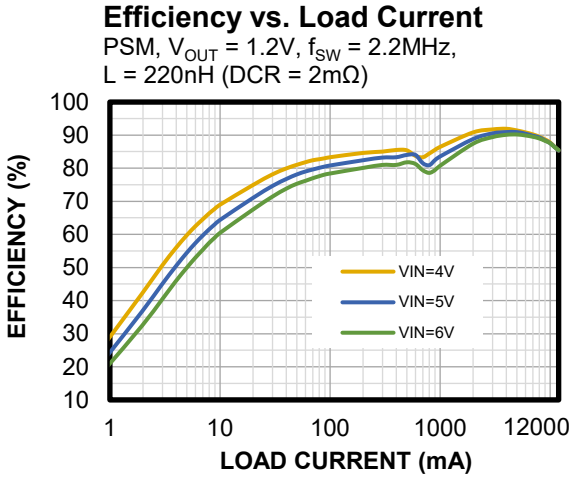
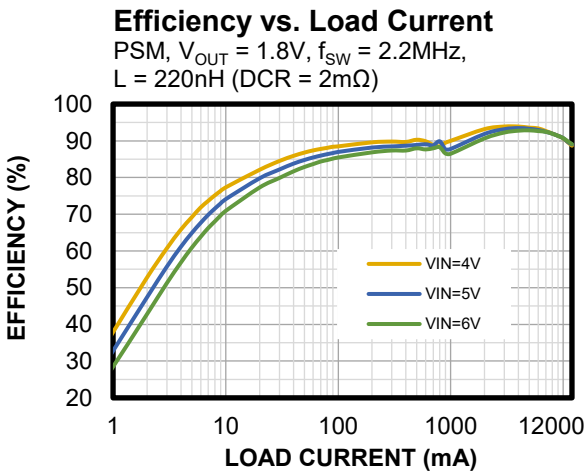
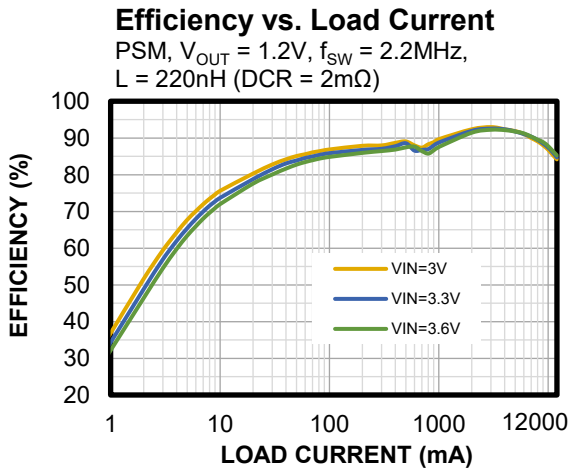
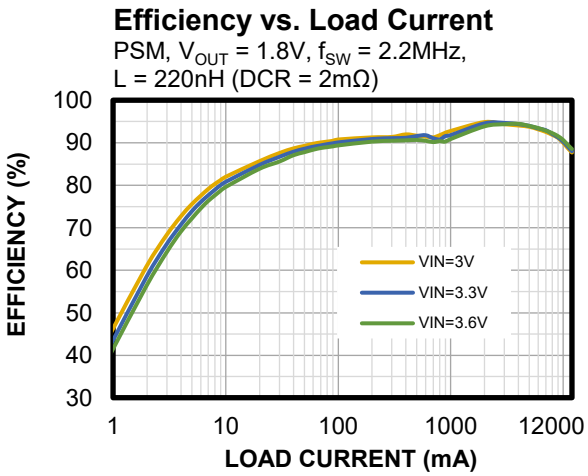


Figure 2: Typical Application (V_{IN} = 3V to 3.6V)









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ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating**
MPQ2211GLC-AEC1	LGA-19 (3mmx3.5mm)	*See Below*	3

* For Tape & Reel, add suffix -Z (e.g. MPQ2211GLC-AEC1-Z).

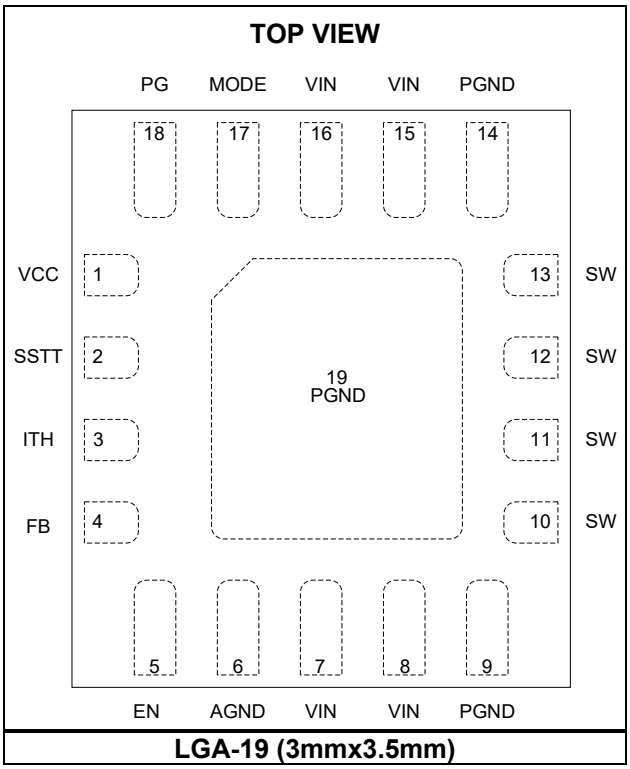
** Moisture Sensitivity Level Rating

TOP MARKING

MPYW
2211
LLL

MP: MPS prefix
Y: Year code
W: Week code
2211: Part number
LLL: Lot number

PACKAGE REFERENCE



LGA-19 (3mmx3.5mm)

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PIN FUNCTIONS

Pin	Name	Description
1	VCC	**Internal 3V LDO output.** The driver and control circuits are powered from this voltage. Float the VCC pin if it is not used. Do not apply external power to this pin. The VCC pin does not need an external capacitor. Connect the VCC pin to the VIN pin when the input voltage (V_{IN}) is below or equal to 3.6V.
2	SSTT	**Soft start and output voltage track.** Connect a capacitor from SSTT to GND to set the soft-start time. The minimum soft-start time is limited at 0.9ms. The feedback (FB) voltages follow the input signal when the SSTT pin is connected to an external voltage signal, and the soft-start setting is ignored. The SSTT capacitor is recommended to be at least 22nF. Do not float the SSTT pin.
3	ITH	**Current limit threshold.** Connect a resistor from the ITH pin to AGND to set the current limit trip point. Do not float the ITH pin.
4	FB	**Feedback.** An external resistor divider connected from the output to AGND (and tapped to FB) sets the output voltage. The feedback voltage is 0.5V. It is recommended to place the resistor divider as close to FB as possible. Avoid placing vias on the FB traces.
5	EN	**Enable.** EN is an input signal that turns the regulator on or off. Pulling this pin below the specified threshold (1V) shuts the chip down. Pulling it up above the specified threshold (1.22V) enables the chip. Connect EN to VIN through a pull-up resistor or a resistive voltage divider for automatic start-up. Do not float the EN pin.
6	AGND	**Analog ground.**
7, 8, 15, 16	VIN	**Input supply.** VIN supplies power to the internal MOSFET and regulator. An appropriate decoupling capacitance must be connected between VIN and PGND at each side of the IC to minimize switching spikes.
9, 14, 19	PGND	**Power ground.**
10, 11, 12, 13	SW	**Switch node.** SW is connected to the high-side MOSFET (HS-FET) source and the low-side MOSFET's (LS FET) drain. Connect the power inductor to this pin with a wide trace but limit its area to avoid EMI radiation.
17	MODE	**Operation mode selection.** Configured MODE to select forced continuous conduction mode ((CCM) or pulse-skip mode. Pull this pin to GND to enable FCCM. Float this pin to set pulse-skip mode. See Table 4 on page 36 for additional details.
18	PG	**Power good output.** PG is an open-drain signal. A pull-up resistor (connected to a DC voltage) is required to pull PG high if the output voltage (V_{OUT}) is within regulation. There is about a 1ms delay from when V_{OUT} exceeds 92.5% of the nominal voltage to when PG pulls high. The PG pin can be floated if it is not used.

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ABSOLUTE MAXIMUM RATINGS (1)

VIN, SW .....-0.3V to +18V
VCC, EN .....-0.3V to +4.5V
All other pins .....-0.3V to +4.3V
Junction temperature (T_J) .....150°C
Lead temperature .....260°C
Continuous power dissipation (T_A = 25°C) (2)
LGA-19 (3mmx3.5mm) …….. ..... 3.87W
Storage temperature ..... -65°C to +150°C

ESD Ratings

Human body model (HBM) .....Class 2 (3)
Charged-device model (CDM) ..... Class C2b (4)

Recommended Operating Conditions

Supply voltage (V_{IN}) .....4V to 6V
Supply voltage (V_{IN}, VCC biased to V_{IN})……
……..3V to 3.6V
Output voltage (V_{OUT}).....0.5V to 3.6V
EN voltage (V_{EN}) 2V
Operating junction temp (T_J).... -40°C to +150°C

Thermal Resistance	θ_{JA}	θ_{JC}	
LGA-19 (3mmx3.5mm)			
JESD51-7…….....	53.5....	9.5.	°C/W (5)
EVQ2211-LC-00A.…….....	32.3.....		°C/W (6)
		Ψ_{JT}	
JESD51-7 …..…..……..….....		16..	°C/W (5)
EVQ2211-LC-00A ....……..….....		2.4.	°C/W (6)

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) Per AEC-Q100-002.
4) Per AEC-Q100-011.
5) Measured on a JESD51-7, 4-layer PCB. The value of θ_{JA} given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application, the value of θ_{JC} shows the thermal resistance from junction-to-case bottom, and the value of Ψ_{JT} shows the characterization parameter from junction-to-case top.
6) Measured on an MPS standard EVB, 8.3cmx8.3cm, 2oz copper thickness, 4-layer PCB. The value of Ψ_{JT} shows the characterization parameter from the junction-to-case top.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 5V, V_{EN} = 2V, T_J = -40°C to +150°C, typical value is tested at T_J = 25°C, unless otherwise noted.

Parameters	Symbol	Conditions	Min	Typ	Max	Units
Supply Current						
Supply current (shutdown)	I_{SHDN}	V_{EN} = 0V		0	10	μA
Supply current (quiescent)	I_Q	V_{EN} = 2V, V_{FB} = 0.55V, FCCM		650	850	μA
MOSFET						
Switch leakage	SW_{LKG_HS}	V_{EN} = 0V, V_{SW} = 0V		0	10	μA
	SW_{LKG_LS}	V_{EN} = 0V, V_{SW} = 6V		0	30	
High-side MOSFET (HS-FET) on-state resistance	$R_{DS_ON_HS}$	V_{EN} = 2V		13.3	33	mΩ
Low-side MOSFET (LS-FET) on-state resistance	$R_{DS_ON_LS}$	V_{EN} = 2V		3.8	7	mΩ
Current Limit						
Current limit threshold	V_{OCP}		1.14	1.2	1.26	V
I_{ITH} to output current (I_{OUT}) ratio	G_{ITH}	I_{OUT} ≥ 2A	18	20	22	μA/A
Low-side negative current limit	I_{LIM_NEG}			-7.5	-9	A
OSM negative current limit	$I_{LIM_NEG_OSM}$	Output sinking mode		-5.5	-7	A
Negative current limit time-out (7)	t_{NCL}			200		ns
Zero-current detection (ZCD) current (7)	I_{ZCD}	PSM		0		mA
Switching Frequency (f_{SW})						
Switching frequency	f_{SW}	MODE = GND, I_{OUT} = 0A, V_{OUT} = 1V,	1900	2200	2500	kHz
Minimum on time	t_{ON_MIN}	V_{FB} = 500mV		20	50	ns
Minimum off time	t_{OFF_MIN}	V_{FB} = 500mV		100	180	ns
Over-Voltage Protection (OVP) and Under-Voltage Protection(UVP)						
OVP threshold	V_{OVP}		113%	116%	119%	V_{REF}
UVP threshold	V_{UVP}		77%	80%	83%	V_{REF}
Feedback Voltage (V_{FB}) and Soft-Start						
Feedback voltage	V_{FB}		495	500	505	mV
SSTT sourcing current	I_{SSTT_SOURCE}	V_{SSTT} = 0V	38	46	54	μA
SSTT sinking current	I_{SSTT_SINK}	V_{SSTT} = 1V	8	12	16	μA
Soft-start time	t_{SS}	C_{SSTT} = 22nF	0.65	0.9	1.15	ms
Error Amplifier (EA)						
Error amplifier offset	V_{OS}		-3	0	+3	mV
Feedback current	I_{FB}	V_{FB} = 500mV		50	100	nA
Enable (EN) and Under-Voltage Lockout (UVLO)						
Enable rising threshold	V_{EN_RISING}		1.17	1.22	1.27	V
Enable falling threshold	V_{EN_RISING}		0.96	1	1.04	V
Enable hysteresis	V_{EN_HYS}			200		mV
Enable input current	I_{EN}	V_{EN} = 2V		0	5	μA
Output discharge FET	R_{ON_DISCH}	V_{IN} = 4V, V_{EN} = 2V, I_{SW} = 5mA		80	150	Ω

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{EN} = 2V, T_J = -40°C to +150°C, typical value is tested at T_J = 25°C, unless otherwise noted.

Parameters	Symbol	Conditions	Min	Typ	Max	Units
Input Voltage (V_{IN}) UVLO						
V_{IN} UVLO threshold rising	V_{INUV_RISING}		2.65	2.8	2.95	V
V_{IN} UVLO threshold falling	$V_{INUV_FALLING}$		2.35	2.5	2.65	V
VCC Regulator						
VCC regulator	V_{CC}		2.91	3.00	3.09	V
VCC load regulation		I_{CC} = 25mA		0.3		%
Power Good (PG)						
Power good high threshold	$PG_{VTH_H_RISING}$	FB from low to high	89.5%	92.5%	95.5%	V_{REF}
Power good low threshold	$PG_{VTH_L_RISING}$	FB from low to high	113%	116%	119%	V_{REF}
	$PG_{VTH_L_FALLING}$	FB from high to low	77%	80%	83%	V_{REF}
Power good low to high delay	$t_{PG_R_DELAY}$	C_{SSTT} = 22nF	0.75	1	1.3	ms
Power good sink current capability	V_{PG}	I_{PG} = 10mA			0.5	V
Power good leakage current	I_{PG_LEAK}	V_{PG} = 3V			3	µA
Power good low-level output voltage	V_{OL_100}	V_{IN} = 0V, pull PG up to 3V through a 100kΩ resistor		650	800	mV
	V_{OL_10}	V_{IN} = 0V, pull PG up to 3V through a 10kΩ resistor		750	900	mV
Thermal Protection						
Thermal shutdown (7)	T_{SD}			168		°C
Thermal shutdown hysteresis (7)	T_{SD_HYS}			20		°C

Notes:

7) Guaranteed by design and characterization. Not tested in production.

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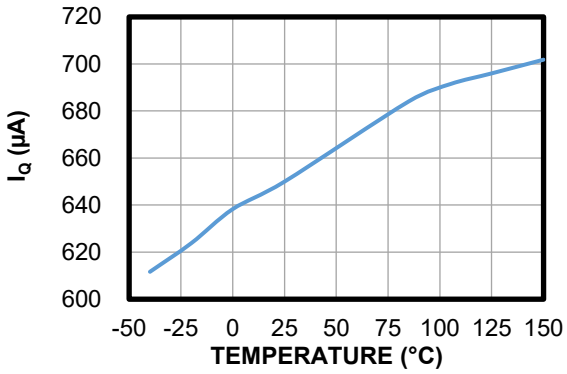
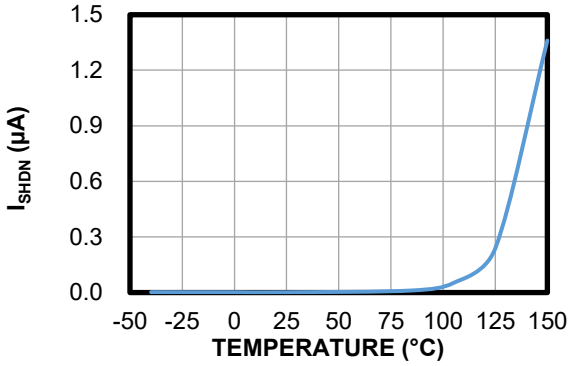
TYPICAL CHARACTERISTICS

V_{IN} = 5V, V_{OUT} = 1.2V, T_J = -40°C to 150°C, unless otherwise noted.

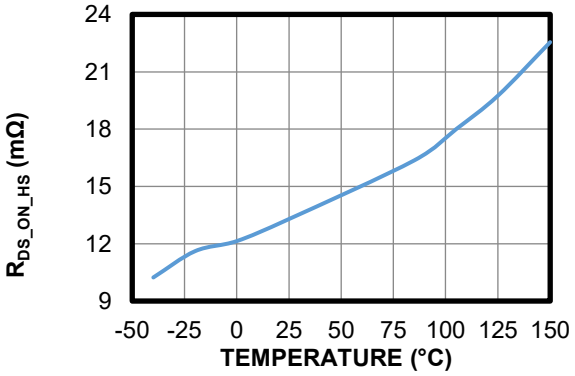
I_Q vs. Temperature



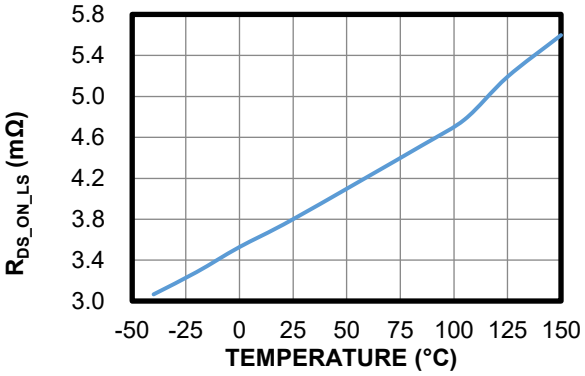
I_{SHDN} vs. Temperature



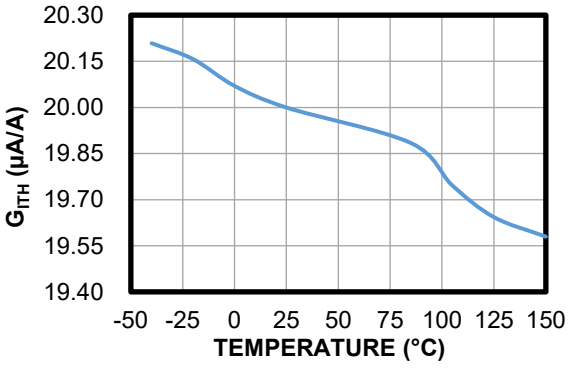
$R_{DS_ON_HS}$ vs. Temperature



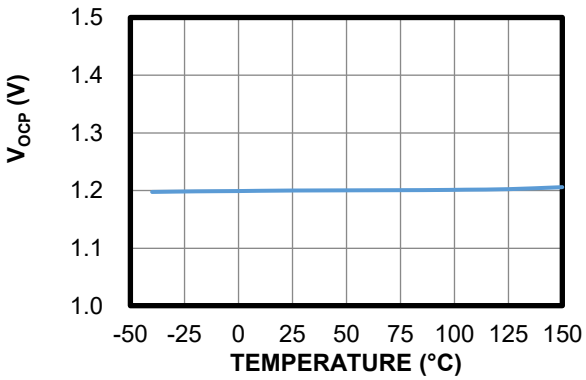
$R_{DS_ON_LS}$ vs. Temperature



G_{ITH} vs. Temperature



V_{OCP} vs. Temperature



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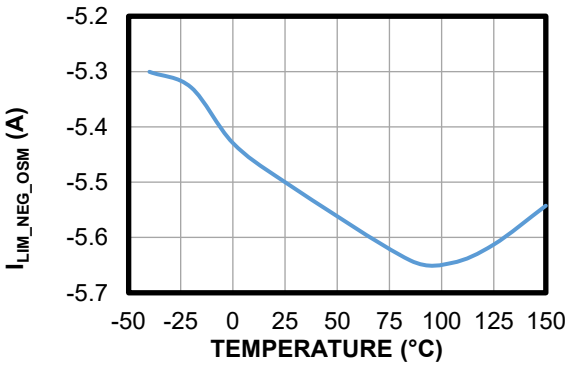
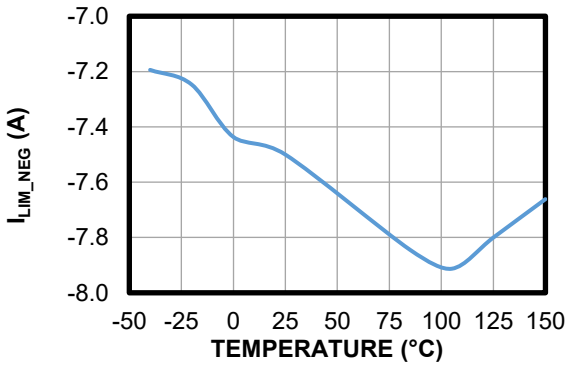
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 1.2V, T_J = -40°C to 150°C, unless otherwise noted.

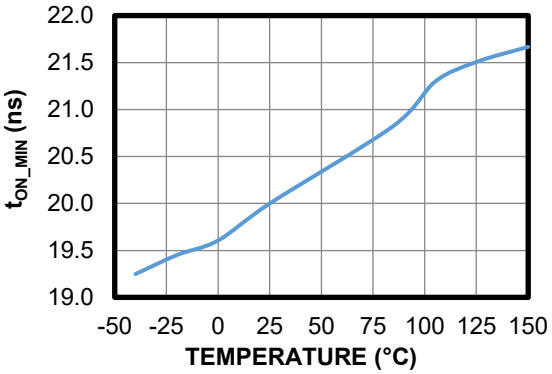
$I_{LIM_NEG_OSM}$ vs. Temperature



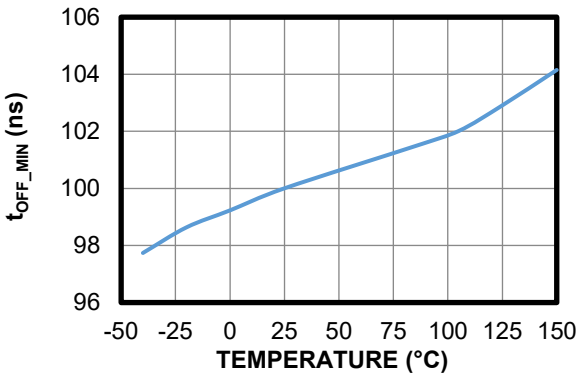
I_{LIM_NEG} vs. Temperature



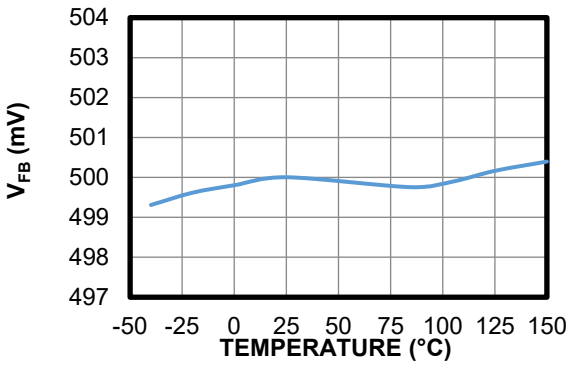
t_{ON_MIN} vs. Temperature



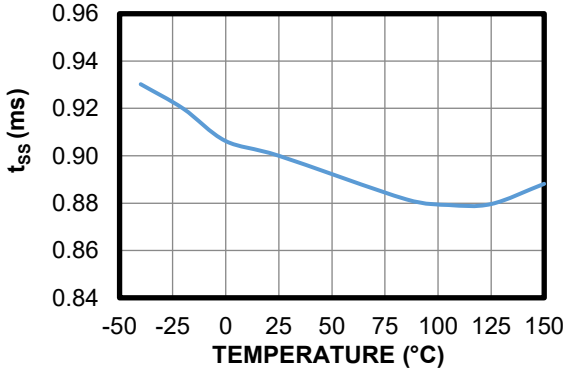
t_{OFF_MIN} vs. Temperature



V_{FB} vs. Temperature



t_{SS} vs. Temperature



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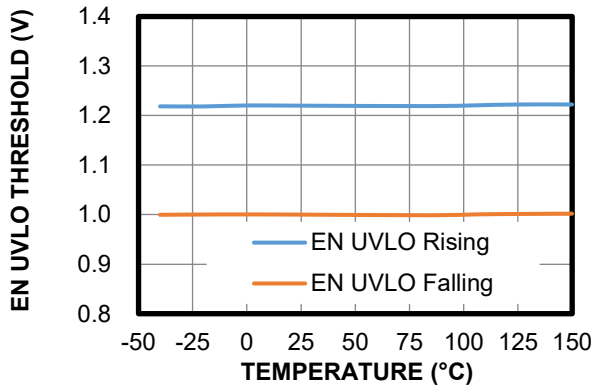
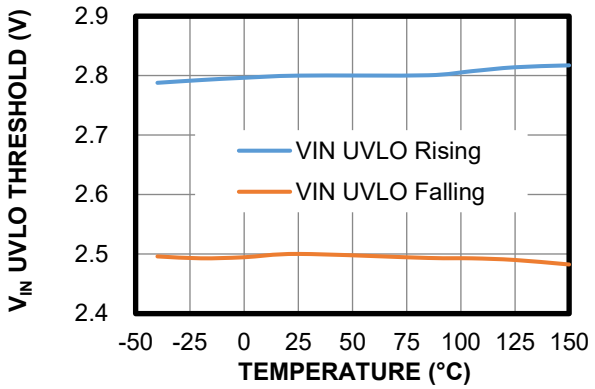
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 1.2V, T_J = -40°C to 150°C, unless otherwise noted.

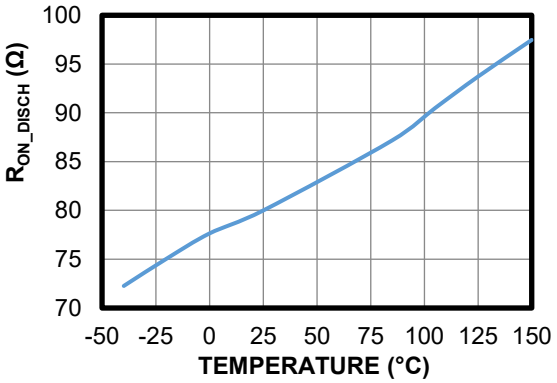
EN UVLO Threshold vs. Temperature



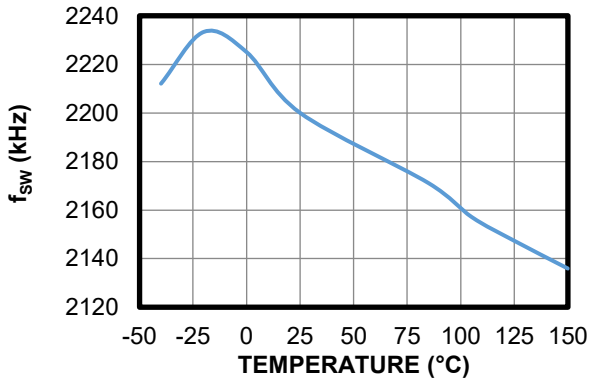
V_{IN} UVLO Threshold vs. Temperature



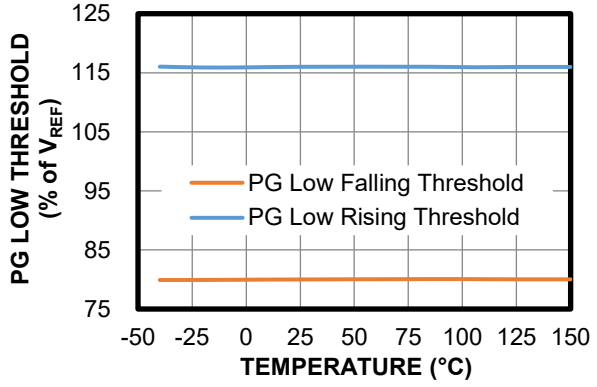
R_{ON_DISCH} vs. Temperature



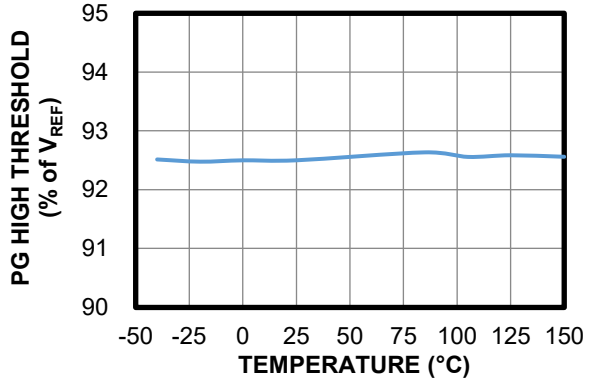
f_{SW} vs. Temperature



PG Low Threshold vs. Temperature



PG High Threshold vs. Temperature



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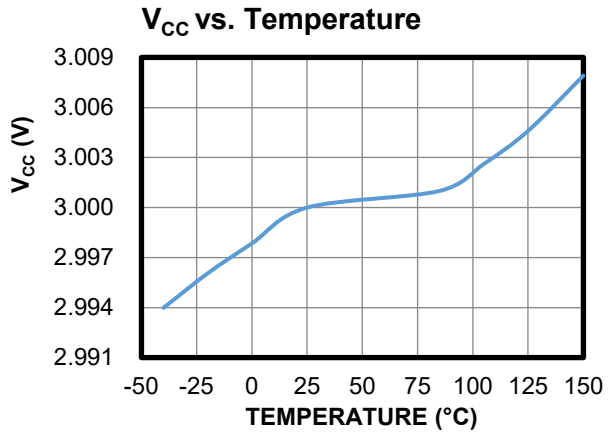
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 1.2V, T_J = -40°C to 150°C, unless otherwise noted.



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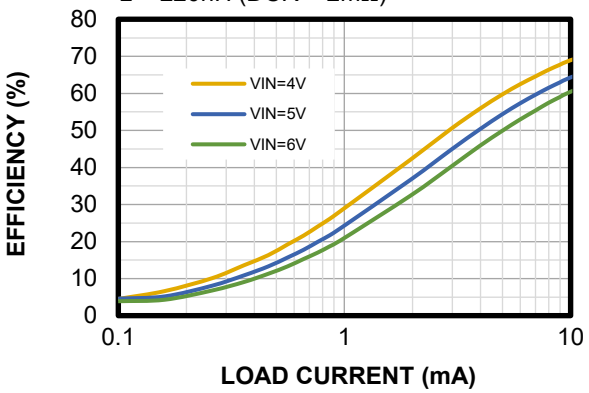
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 5V, V_{OUT} = 1.2V, L = 220nH, C_{OUT} = 4 x 47µF, f_{SW} = 2.2MHz, T_A = 25°C, unless otherwise noted.

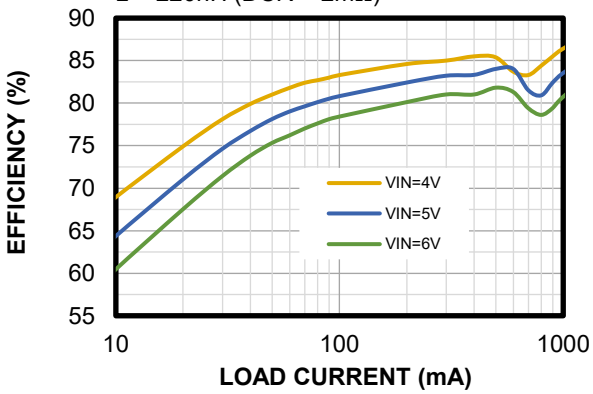
Efficiency vs. Load Current

PSM, V_{OUT} = 1.2V, f_{SW} = 2.2MHz, L = 220nH (DCR = 2mΩ)



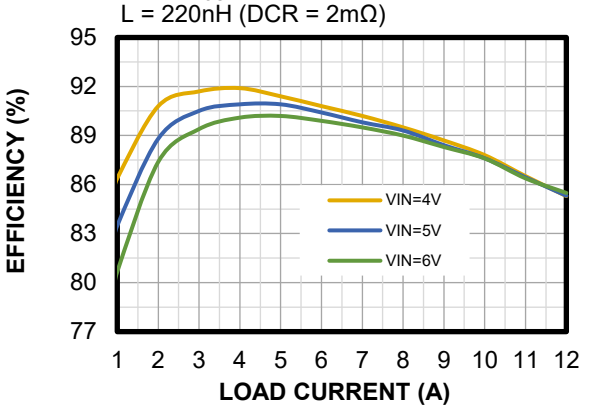
Efficiency vs. Load Current

PSM, V_{OUT} = 1.2V, f_{SW} = 2.2MHz, L = 220nH (DCR = 2mΩ)



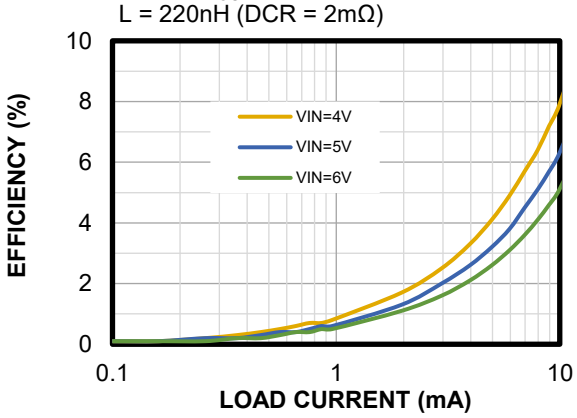
Efficiency vs. Load Current

PSM, V_{OUT} = 1.2V, f_{SW} = 2.2MHz, L = 220nH (DCR = 2mΩ)



Efficiency vs. Load Current

FCCM, V_{OUT} = 1.2V, f_{SW} = 2.2MHz, L = 220nH (DCR = 2mΩ)



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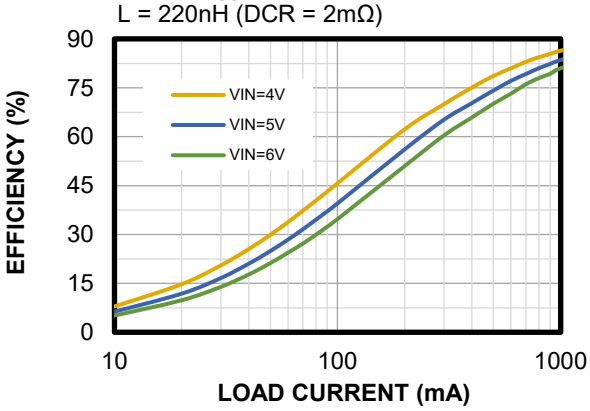

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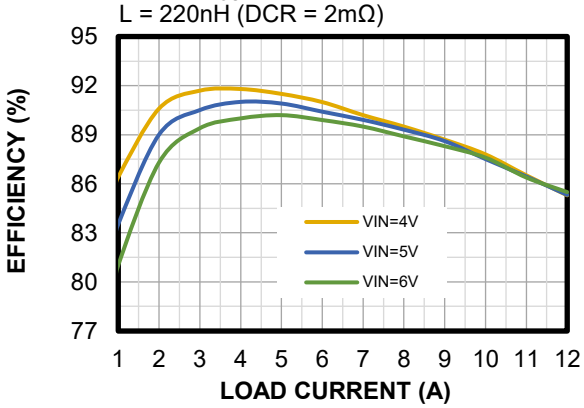

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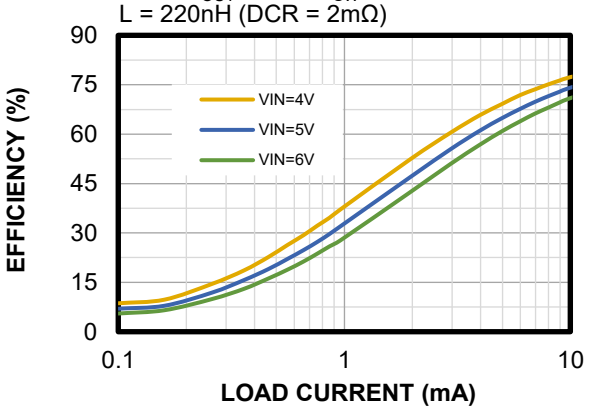
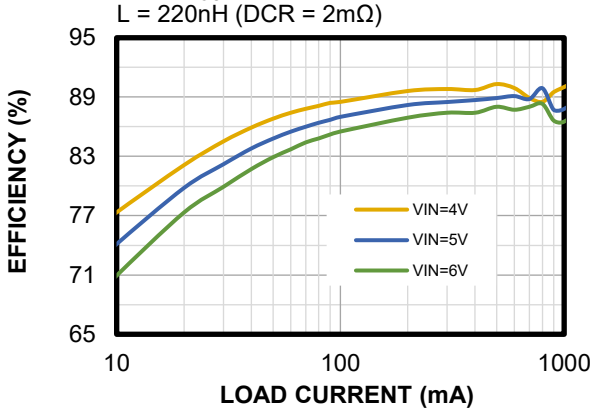
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 1.2V, L = 220nH, C_{OUT} = 4 x 47µF, f_{SW} = 2.2MHz, T_A = 25°C, unless otherwise noted.

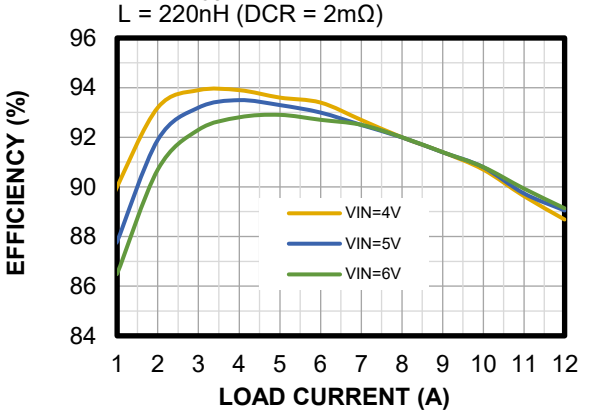
Efficiency vs. Load Current
PSM, V_{OUT} = 1.8V, f_{SW} = 2.2MHz,
L = 220nH (DCR = 2mΩ)



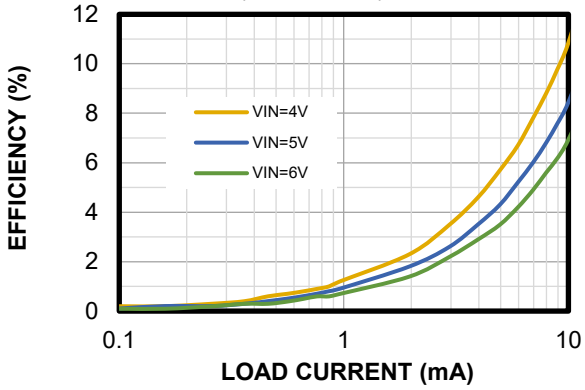
Efficiency vs. Load Current
PSM, V_{OUT} = 1.8V, f_{SW} = 2.2MHz,
L = 220nH (DCR = 2mΩ)



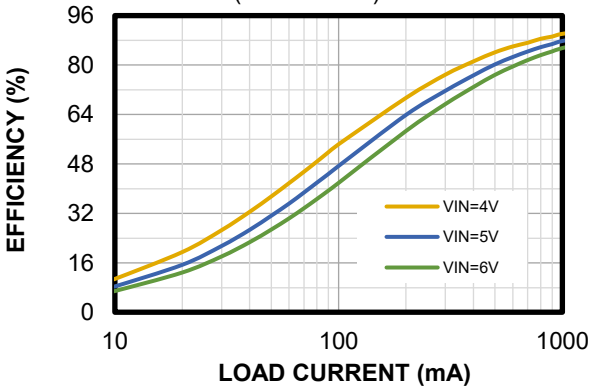
Efficiency vs. Load Current
PSM, V_{OUT} = 1.8V, f_{SW} = 2.2MHz,
L = 220nH (DCR = 2mΩ)



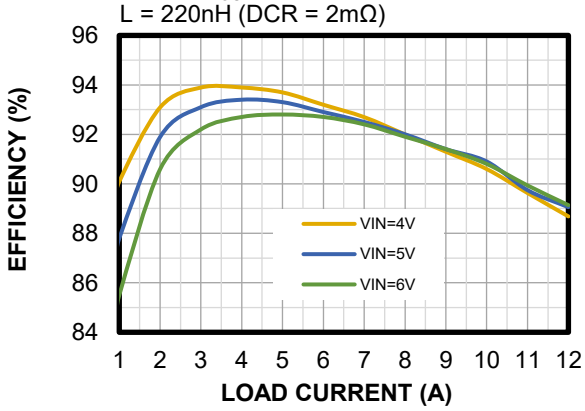
Efficiency vs. Load Current
FCCM, V_{OUT} = 1.8V, f_{SW} = 2.2MHz,
L = 220nH (DCR = 2mΩ)



Efficiency vs. Load Current
FCCM, V_{OUT} = 1.8V, f_{SW} = 2.2MHz,
L = 220nH (DCR = 2mΩ)



Efficiency vs. Load Current
FCCM, V_{OUT} = 1.8V, f_{SW} = 2.2MHz,
L = 220nH (DCR = 2mΩ)



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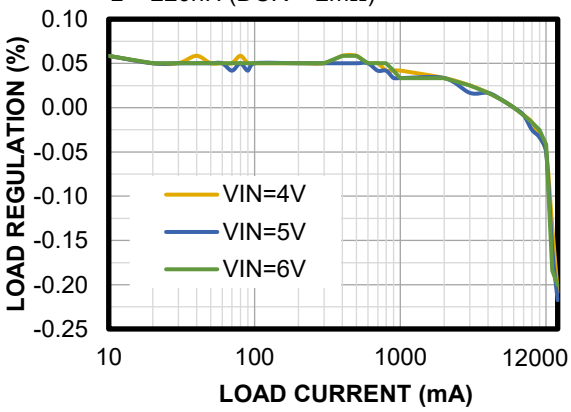
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 1.2V, L = 220nH, C_{OUT} = 4 x 47µF, f_{SW} = 2.2MHz, T_A = 25°C, unless otherwise noted.

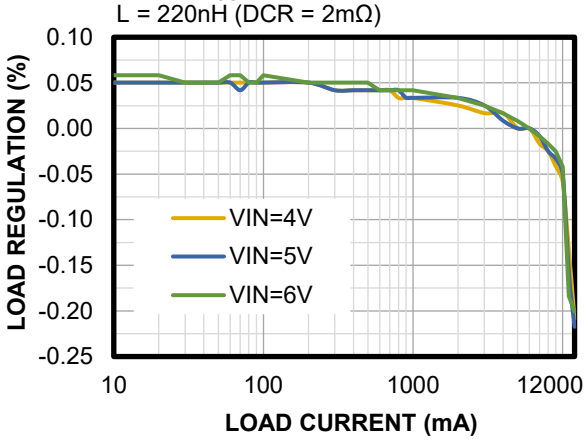
Load Regulation

PSM, V_{OUT} = 1.2V, f_{SW} = 2.2MHz,
L = 220nH (DCR = 2mΩ)



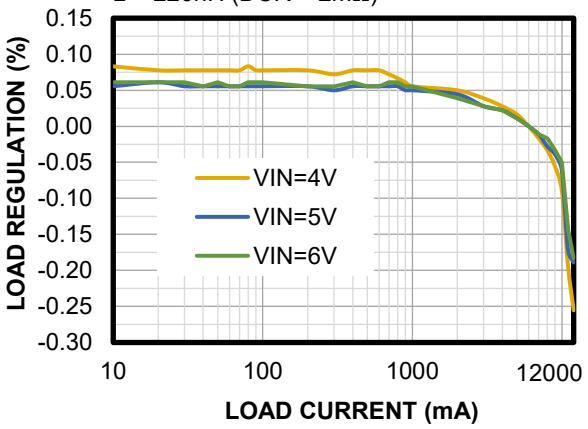
Load Regulation

FCCM, V_{OUT} = 1.2V, f_{SW} = 2.2MHz,
L = 220nH (DCR = 2mΩ)



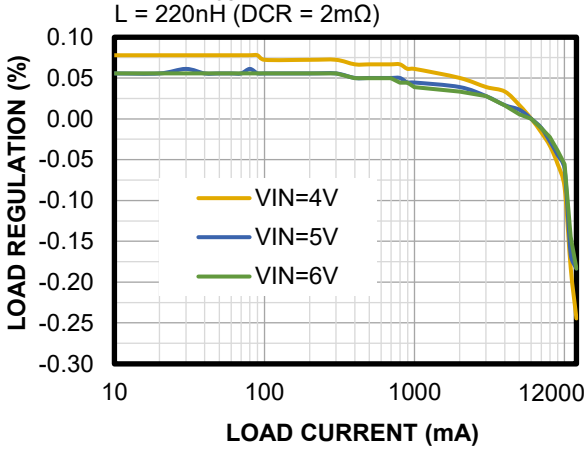
Load Regulation

PSM, V_{OUT} = 1.8V, f_{SW} = 2.2MHz,
L = 220nH (DCR = 2mΩ)



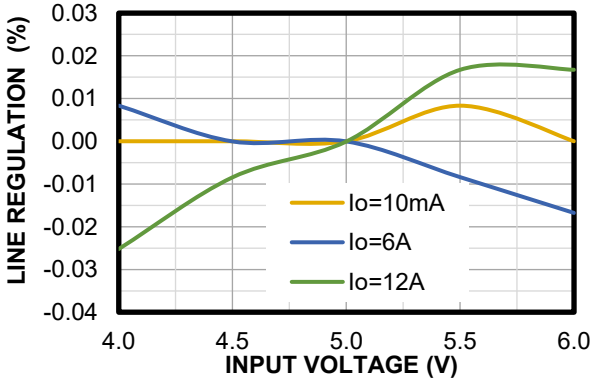
Load Regulation

FCCM, V_{OUT} = 1.8V, f_{SW} = 2.2MHz,
L = 220nH (DCR = 2mΩ)



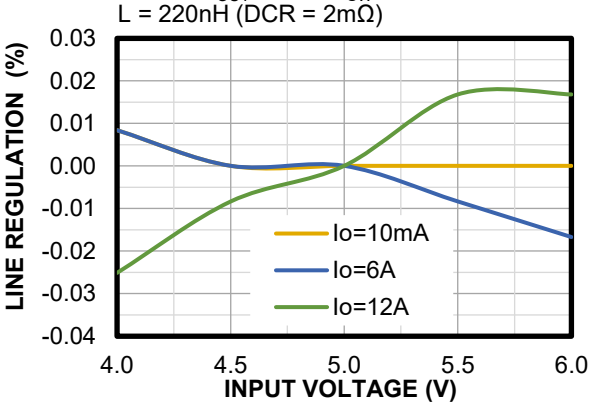
Line Regulation

PSM, V_{OUT} = 1.2V, f_{SW} = 2.2MHz,
L = 220nH (DCR = 2mΩ)



Line Regulation

FCCM, V_{OUT} = 1.2V, f_{SW} = 2.2MHz,
L = 220nH (DCR = 2mΩ)



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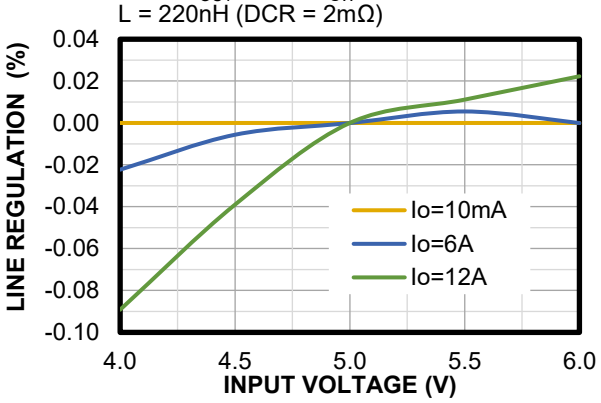
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 1.2V, L = 220nH, C_{OUT} = 4 x 47µF, f_{SW} = 2.2MHz, T_A = 25°C, unless otherwise noted.

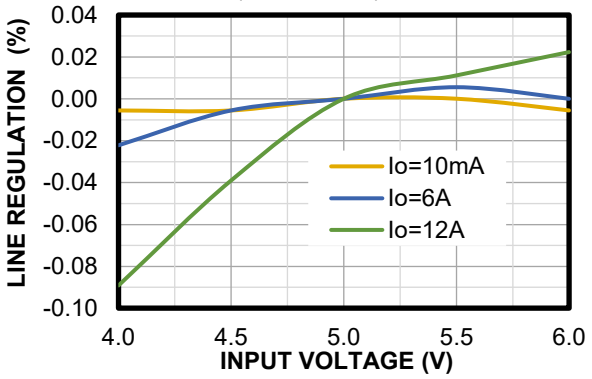
Line Regulation

PSM, V_{OUT} = 1.8V, f_{SW} = 2.2MHz,
L = 220nH (DCR = 2mΩ)



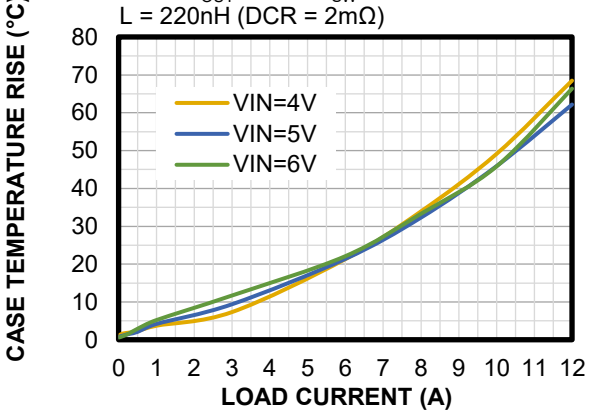
Line Regulation

FCCM, V_{OUT} = 1.8V, f_{SW} = 2.2MHz,
L = 220nH (DCR = 2mΩ)



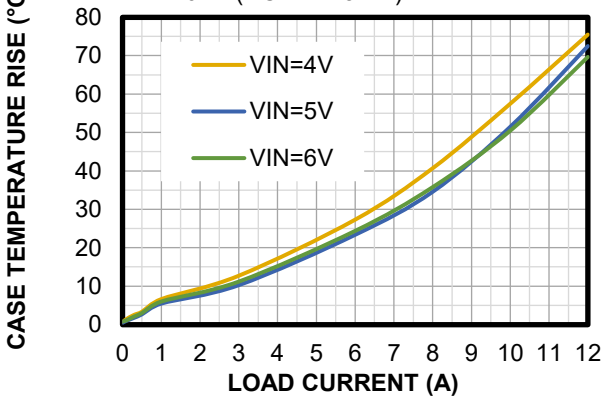
Case Temperature Rise

PSM, V_{OUT} = 1.2V, f_{SW} = 2.2MHz,
L = 220nH (DCR = 2mΩ)



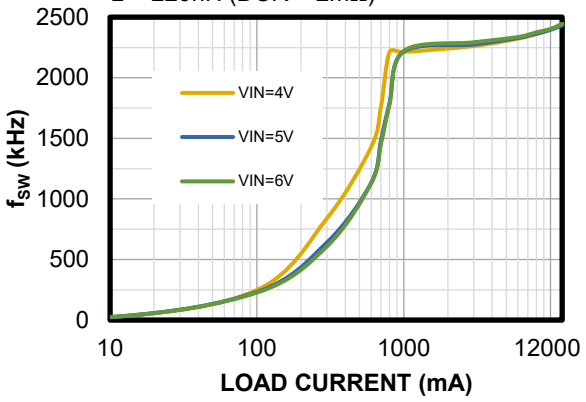
Case Temperature Rise

PSM, V_{OUT} = 1.8V, f_{SW} = 2.2MHz,
L = 220nH (DCR = 1.5mΩ)



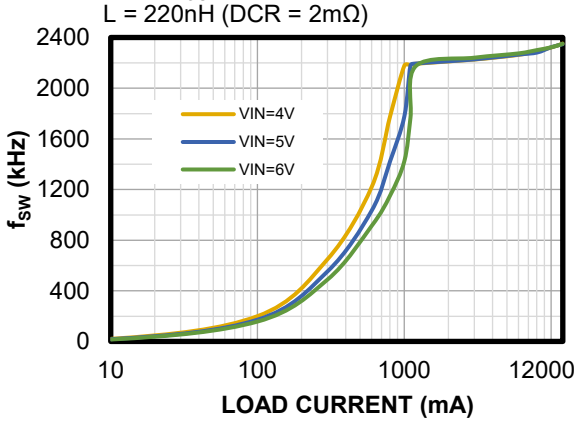
f_{SW} vs. Load Current

PSM, V_{OUT} = 1.2V, f_{SW} = 2.2MHz,
L = 220nH (DCR = 2mΩ)



f_{SW} vs. Load Current

PSM, V_{OUT} = 1.8V, f_{SW} = 2.2MHz,
L = 220nH (DCR = 2mΩ)



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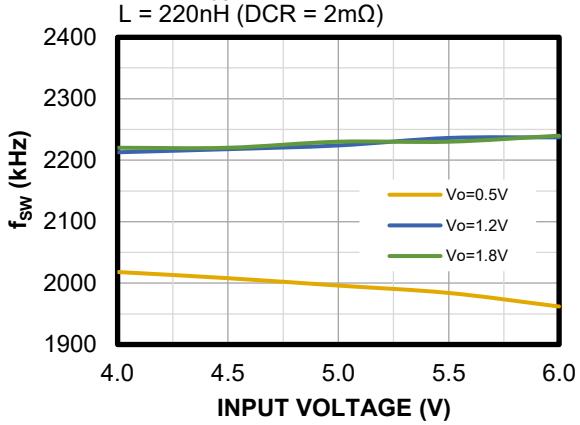
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 1.2V, L = 220nH, C_{OUT} = 4 x 47µF, f_{SW} = 2.2MHz, T_A = 25°C, unless otherwise noted.

f_{SW} vs. Input Voltage

FCCM, I_{OUT} = 0A, f_{SW} = 2.2MHz,
L = 220nH (DCR = 2mΩ)



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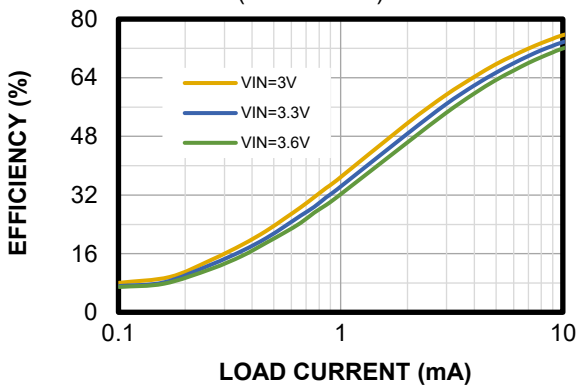
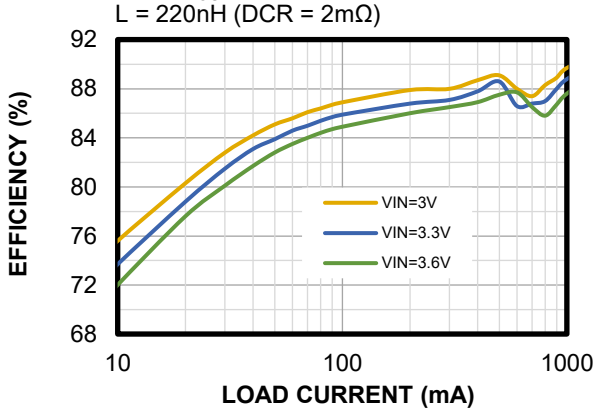
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.3V, V_{OUT} = 1.2V, L = 220nH, C_{OUT} = 4 x 47µF, f_{SW} = 2.2MHz, T_A = 25°C, unless otherwise noted.

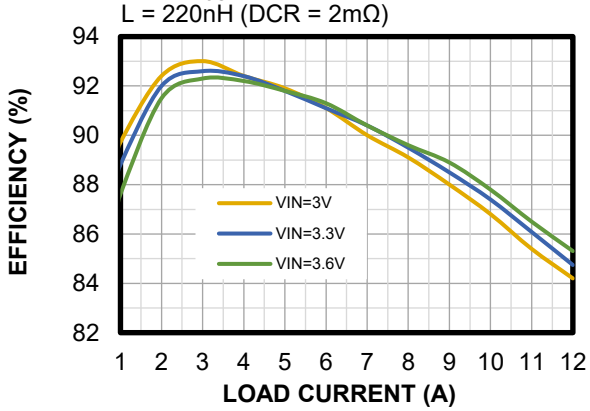
Efficiency vs. Load Current
PSM, V_{OUT} = 1.2V, f_{SW} = 2.2MHz,
L = 220nH (DCR = 2mΩ)



Efficiency vs. Load Current
PSM, V_{OUT} = 1.2V, f_{SW} = 2.2MHz,
L = 220nH (DCR = 2mΩ)



Efficiency vs. Load Current
PSM, V_{OUT} = 1.2V, f_{SW} = 2.2MHz,
L = 220nH (DCR = 2mΩ)



Efficiency vs. Load Current
FCCM, V_{OUT} = 1.2V, f_{SW} = 2.2MHz,
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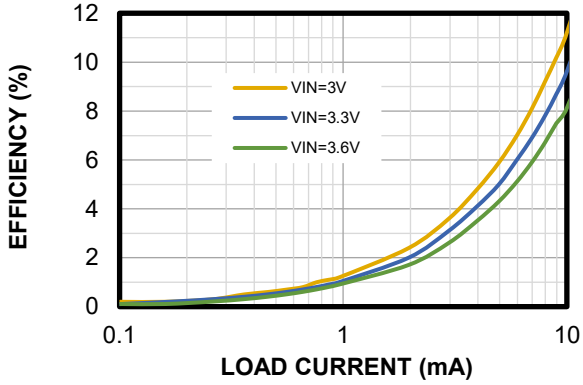
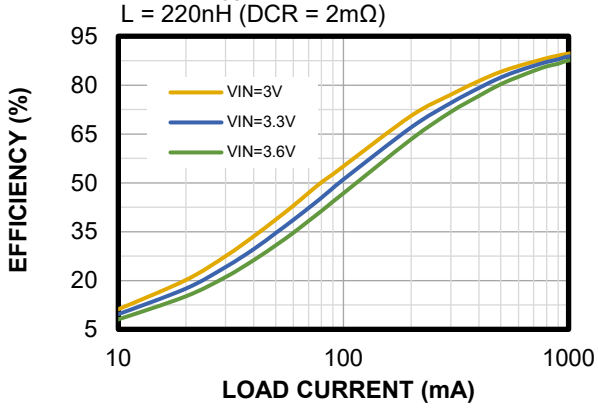
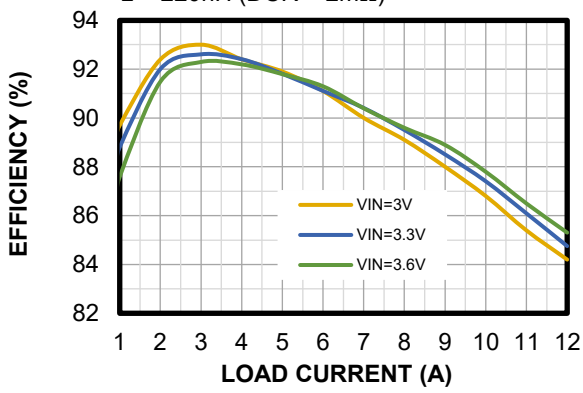


Efficiency vs. Load Current
FCCM, V_{OUT} = 1.2V, f_{SW} = 2.2MHz,
L = 220nH (DCR = 2mΩ)



Efficiency vs. Load Current
FCCM, V_{OUT} = 1.2V, f_{SW} = 2.2MHz,
L = 220nH (DCR = 2mΩ)



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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

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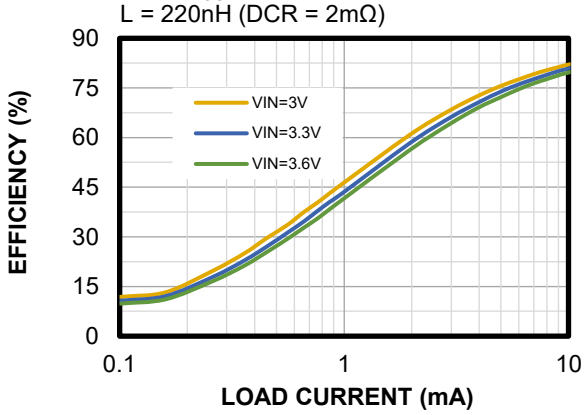
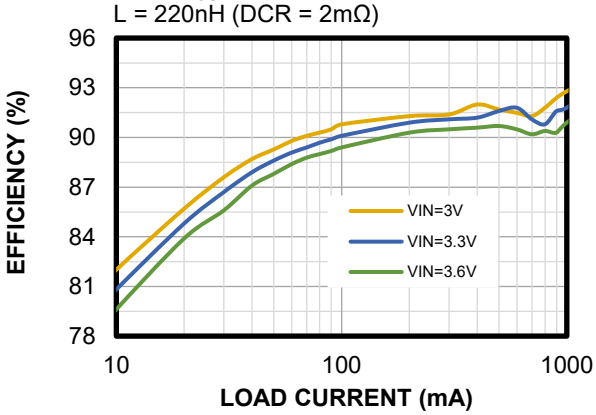
Efficiency vs. Load Current
PSM, V_{OUT} = 1.8V, f_{SW} = 2.2MHz,
L = 220nH (DCR = 2mΩ)



Efficiency vs. Load Current
PSM, V_{OUT} = 1.8V, f_{SW} = 2.2MHz,
L = 220nH (DCR = 2mΩ)



Efficiency vs. Load Current
PSM, V_{OUT} = 1.8V, f_{SW} = 2.2MHz,
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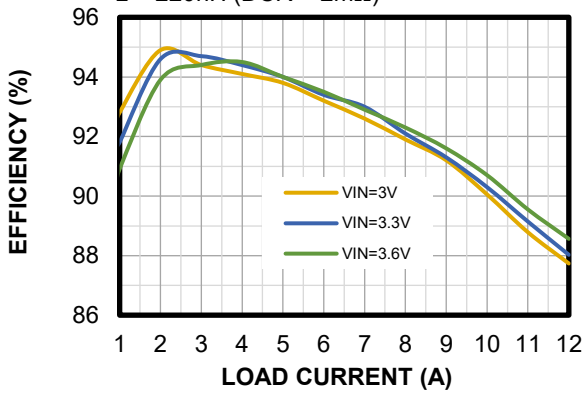
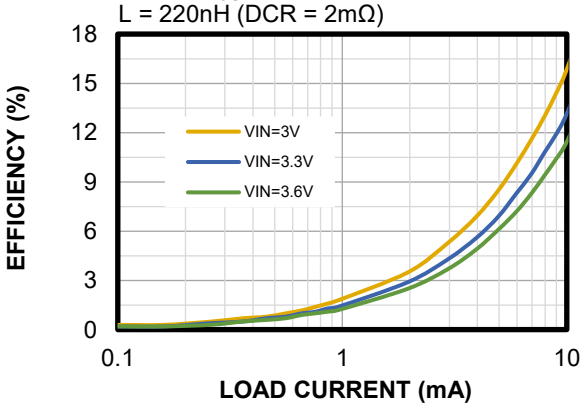
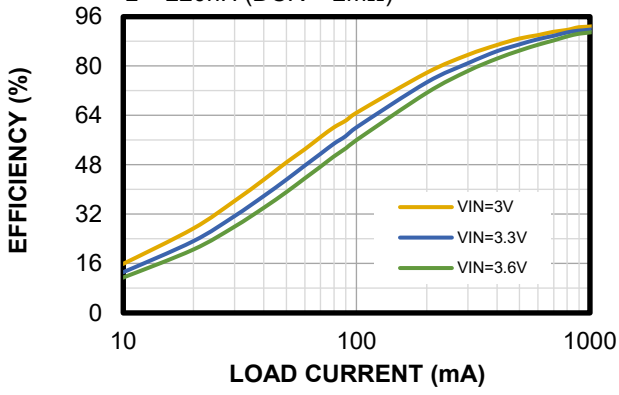


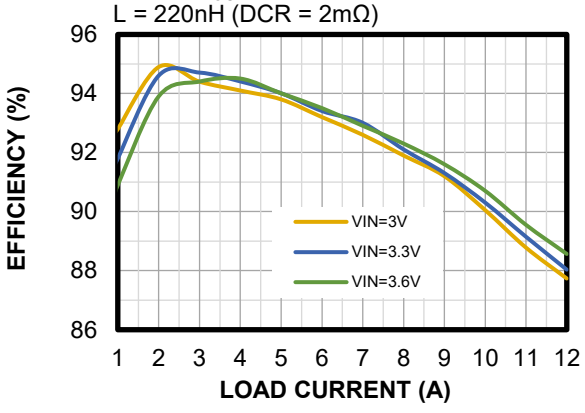
Efficiency vs. Load Current
FCCM, V_{OUT} = 1.8V, f_{SW} = 2.2MHz,
L = 220nH (DCR = 2mΩ)



Efficiency vs. Load Current
FCCM, V_{OUT} = 1.8V, f_{SW} = 2.2MHz,
L = 220nH (DCR = 2mΩ)



Efficiency vs. Load Current
FCCM, V_{OUT} = 1.8V, f_{SW} = 2.2MHz,
L = 220nH (DCR = 2mΩ)



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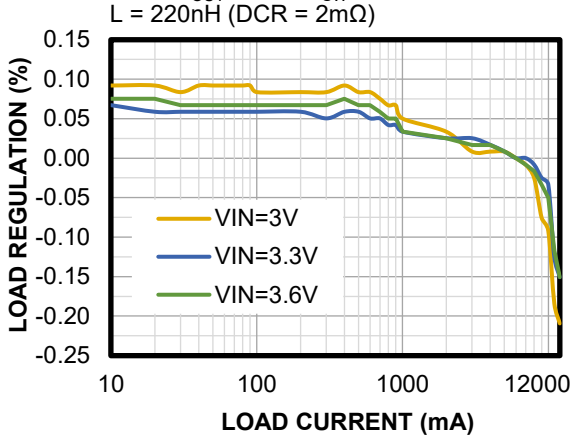
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.3V, V_{OUT} = 1.2V, L = 220nH, C_{OUT} = 4 x 47µF, f_{SW} = 2.2MHz, T_A = 25°C, unless otherwise noted.

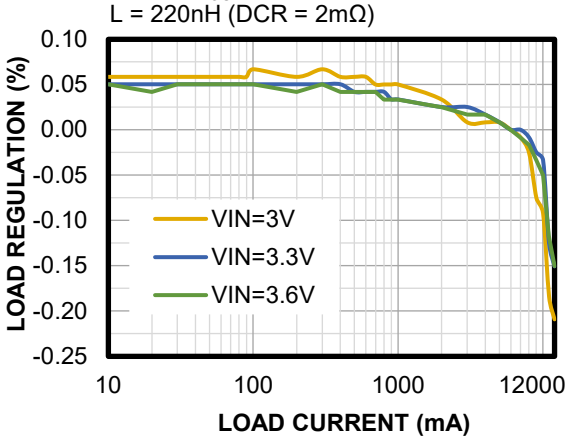
Load Regulation

PSM, V_{OUT} = 1.2V, f_{SW} = 2.2MHz,
L = 220nH (DCR = 2mΩ)



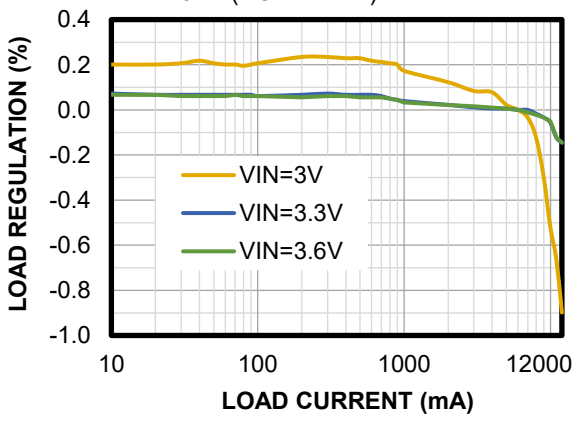
Load Regulation

FCCM, V_{OUT} = 1.2V, f_{SW} = 2.2MHz,
L = 220nH (DCR = 2mΩ)



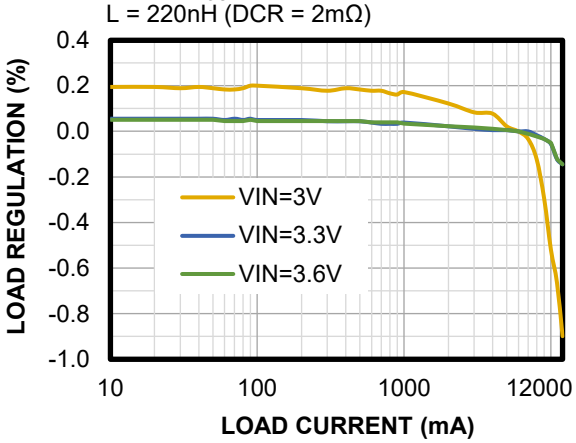
Load Regulation

PSM, V_{OUT} = 1.8V, f_{SW} = 2.2MHz,
L = 220nH (DCR = 2mΩ)



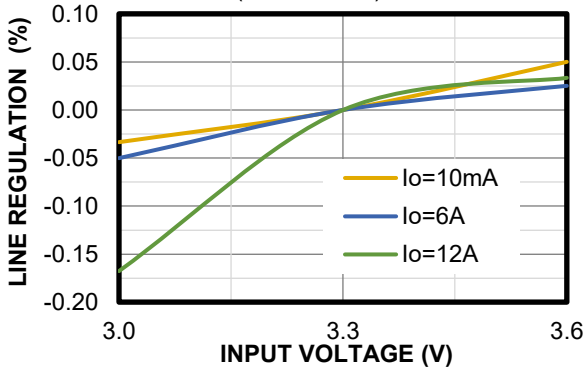
Load Regulation

FCCM, V_{OUT} = 1.8V, f_{SW} = 2.2MHz,
L = 220nH (DCR = 2mΩ)



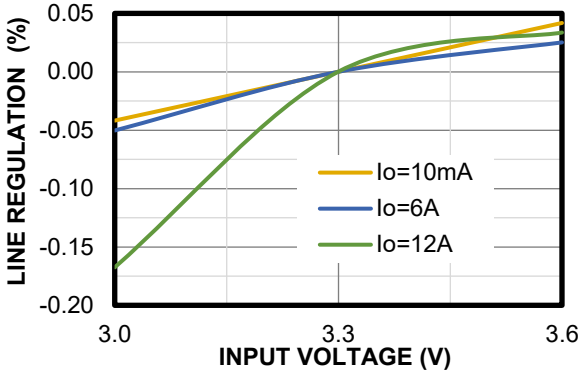
Line Regulation

PSM, V_{OUT} = 1.2V, f_{SW} = 2.2MHz,
L = 220nH (DCR = 2mΩ)



Line Regulation

FCCM, V_{OUT} = 1.2V, f_{SW} = 2.2MHz,
L = 220nH (DCR = 2mΩ)



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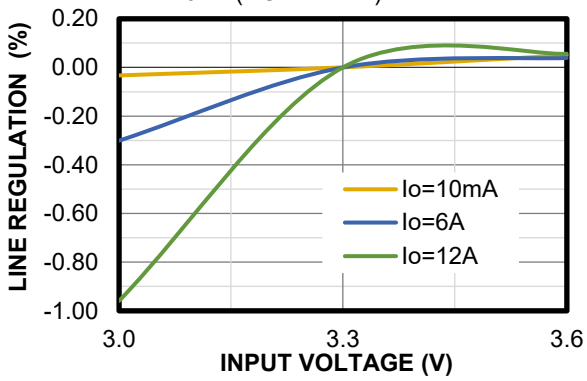
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.3V, V_{OUT} = 1.2V, L = 220nH, C_{OUT} = 4 x 47µF, f_{SW} = 2.2MHz, T_A = 25°C, unless otherwise noted.

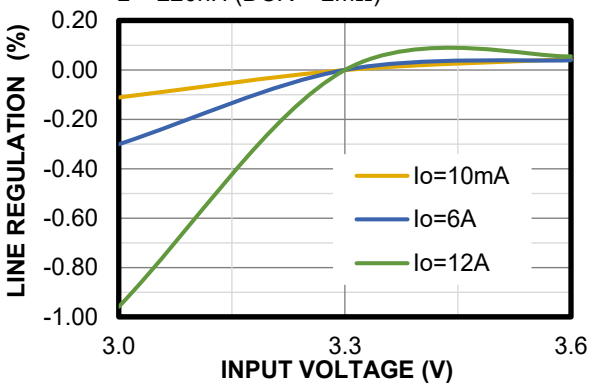
Line Regulation

PSM, V_{OUT} = 1.8V, f_{SW} = 2.2MHz,
L = 220nH (DCR = 2mΩ)



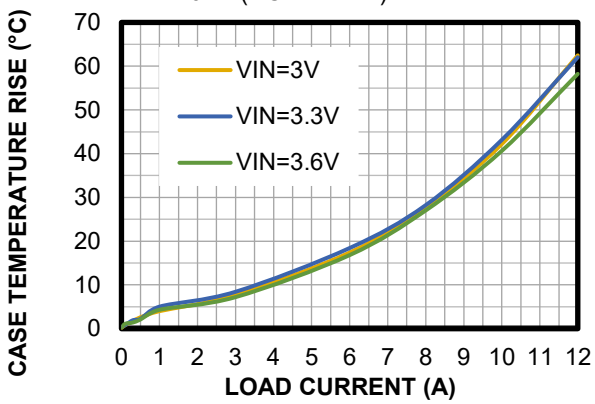
Line Regulation

FCCM, V_{OUT} = 1.8V, f_{SW} = 2.2MHz,
L = 220nH (DCR = 2mΩ)



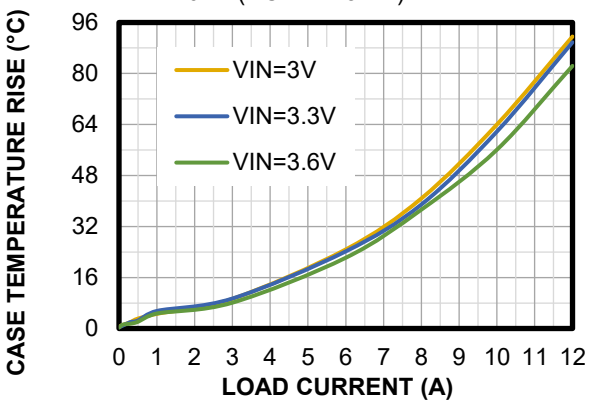
Case Temperature Rise

PSM, V_{OUT} = 1.2V, f_{SW} = 2.2MHz,
L = 220nH (DCR = 2mΩ)



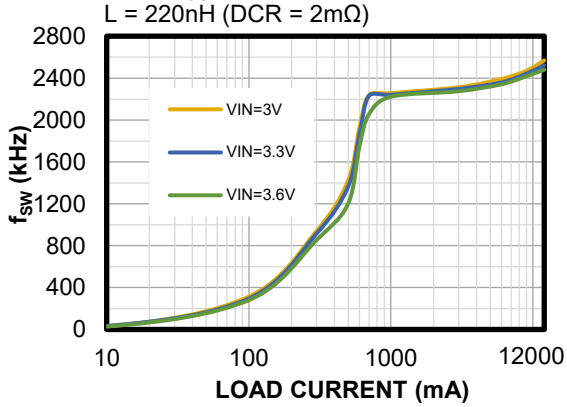
Case Temperature Rise

PSM, V_{OUT} = 1.8V, f_{SW} = 2.2MHz,
L = 220nH (DCR = 1.5mΩ)



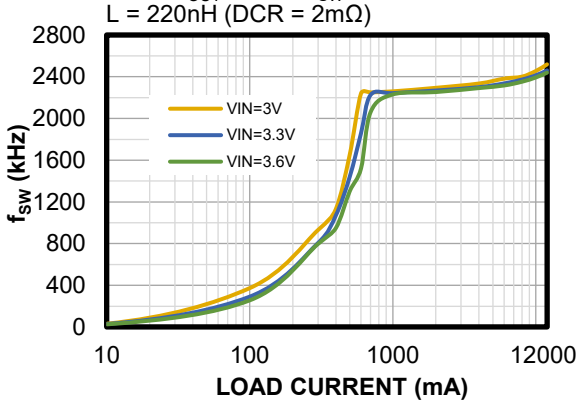
f_{SW} vs. Load Current

PSM, V_{OUT} = 1.2V, f_{SW} = 2.2MHz,
L = 220nH (DCR = 2mΩ)



f_{SW} vs. Load Current

PSM, V_{OUT} = 1.8V, f_{SW} = 2.2MHz,
L = 220nH (DCR = 2mΩ)



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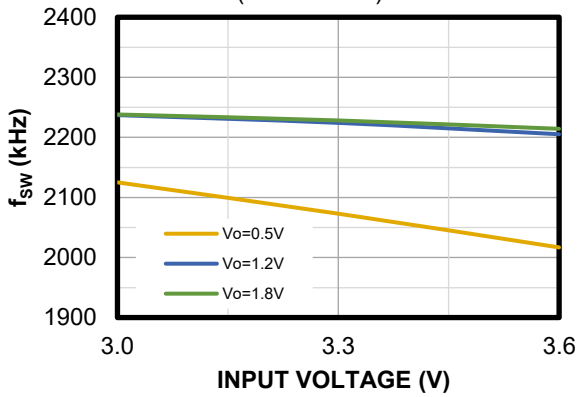
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.3V, V_{OUT} = 1.2V, L = 220nH, C_{OUT} = 4 x 47µF, f_{SW} = 2.2MHz, T_A = 25°C, unless otherwise noted.

f_{SW} vs. Input Voltage

FCCM, I_{OUT} = 0A, f_{SW} = 2.2MHz,
L = 220nH (DCR = 2mΩ)



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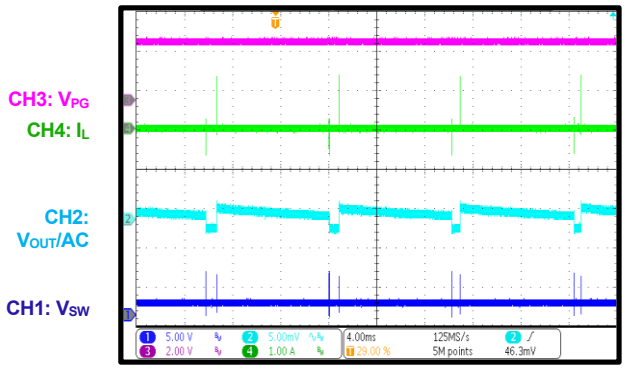
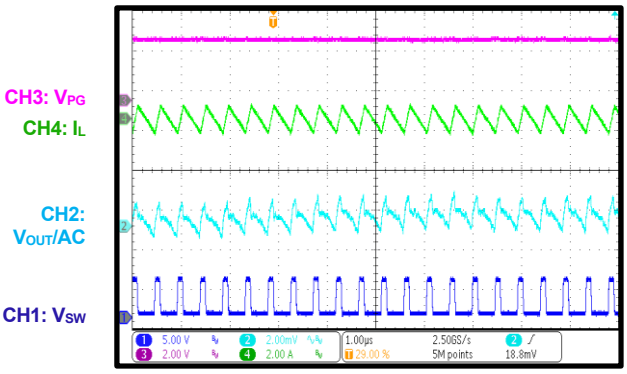
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 1.2V, L = 220nH, C_{OUT} = 4 x 47µF, f_{SW} = 2.2MHz, T_A = 25°C, unless otherwise noted.

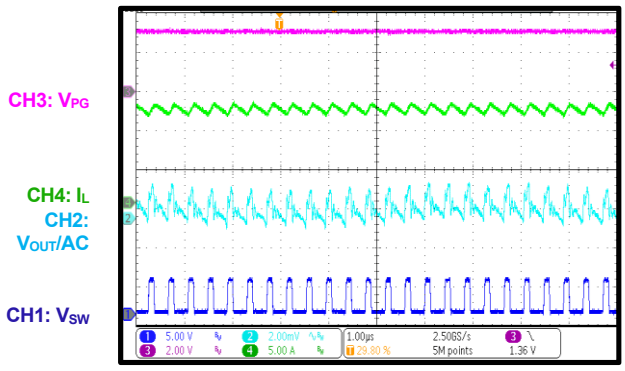
Steady State
I_{OUT} = 0A, PSM



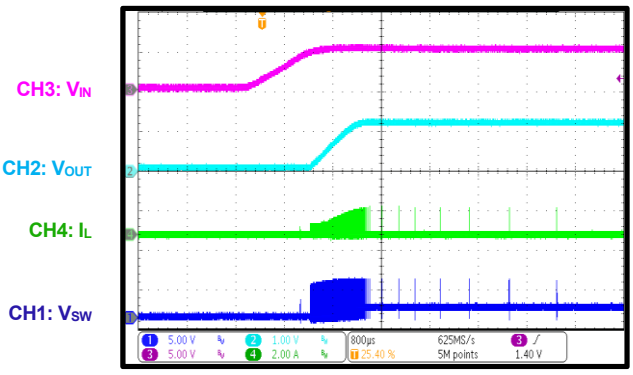
Steady State
I_{OUT} = 0A, FCCM



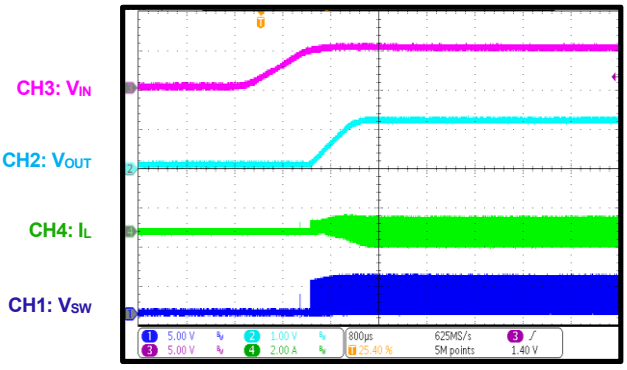
Steady State
I_{OUT} = 12A



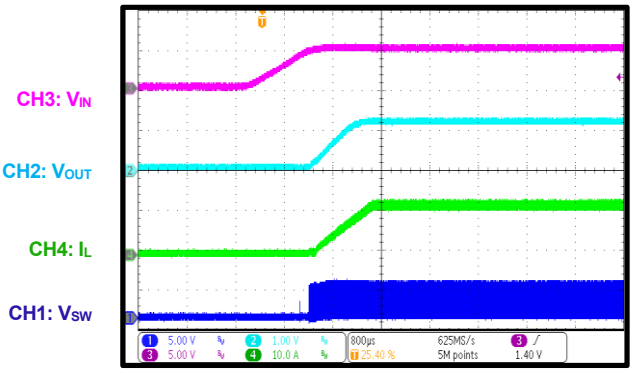
Start-Up through VIN
I_{OUT} = 0A, PSM



Start-Up through VIN
I_{OUT} = 0A, FCCM



Start-Up through VIN
I_{OUT} = 12A



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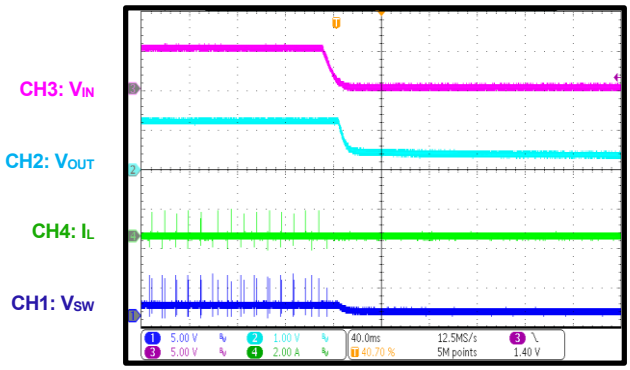
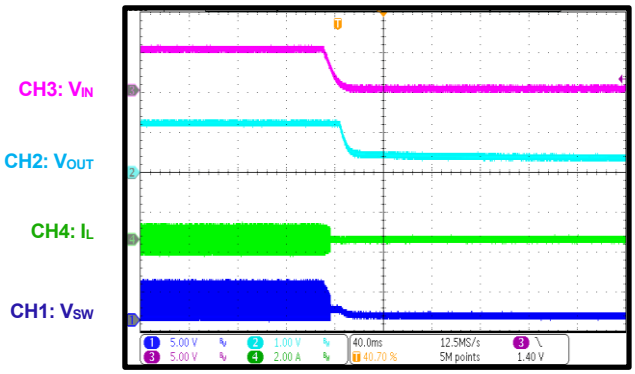
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 1.2V, L = 220nH, C_{OUT} = 4 x 47µF, f_{SW} = 2.2MHz, T_A = 25°C, unless otherwise noted.

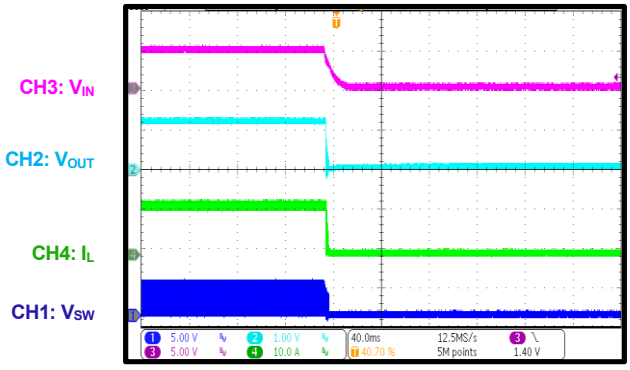
Shutdown through VIN
I_{OUT} = 0A, PSM



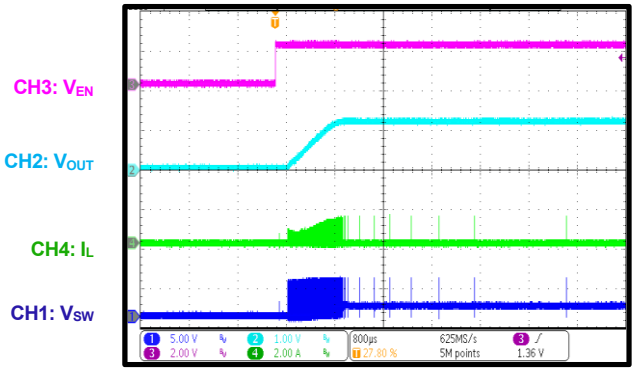
Shutdown through VIN
I_{OUT} = 0A, FCCM



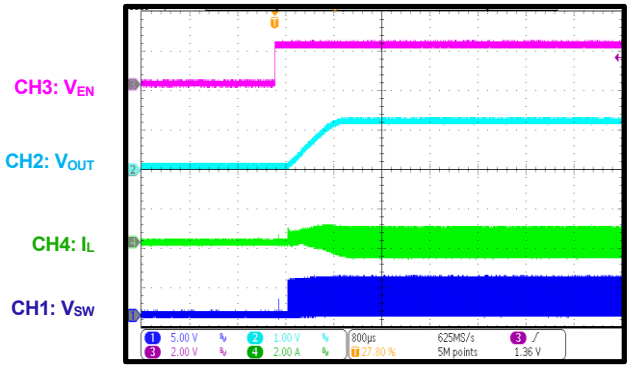
Shutdown through VIN
I_{OUT} = 12A



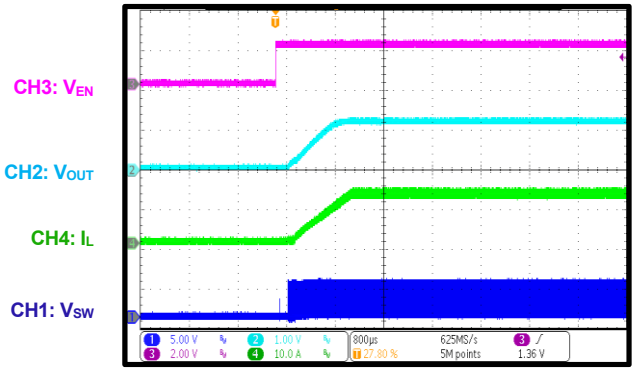
Start-Up through EN
I_{OUT} = 0A, PSM



Start-Up through EN
I_{OUT} = 0A, FCCM



Start-Up through EN
I_{OUT} = 12A



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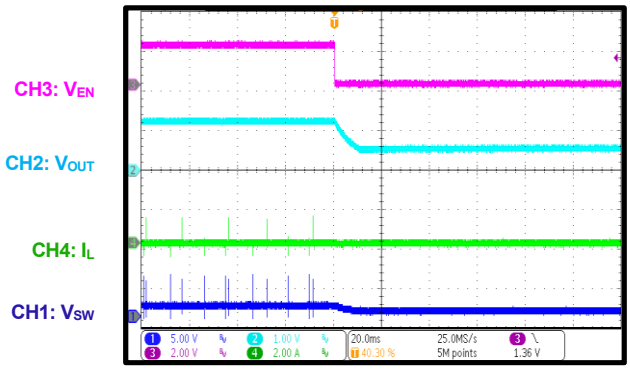
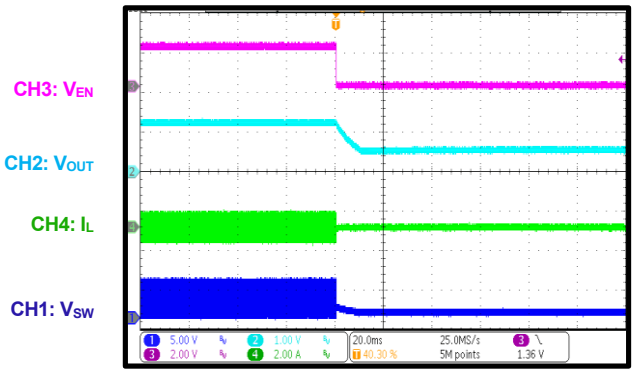
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 1.2V, L = 220nH, C_{OUT} = 4 x 47µF, f_{SW} = 2.2MHz, T_A = 25°C, unless otherwise noted.

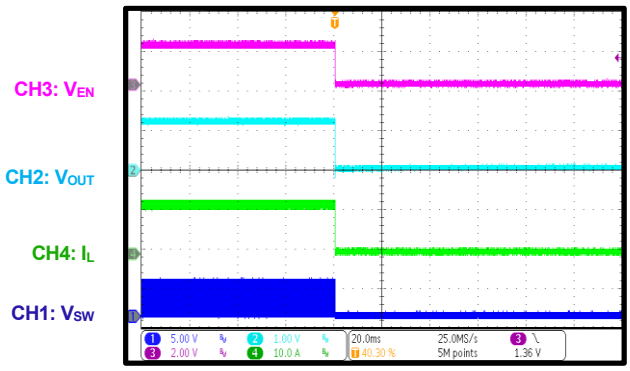
Shutdown through EN
I_{OUT} = 0A, PSM



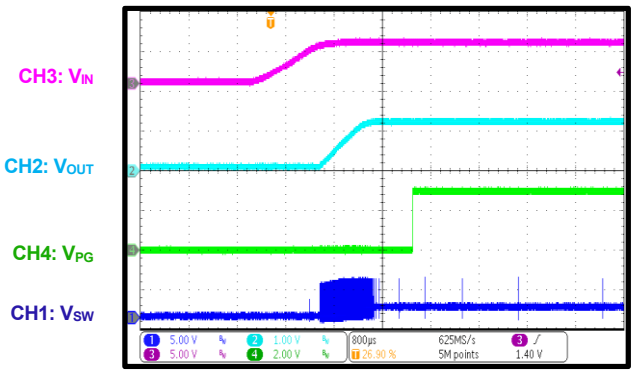
Shutdown through EN
I_{OUT} = 0A, FCCM



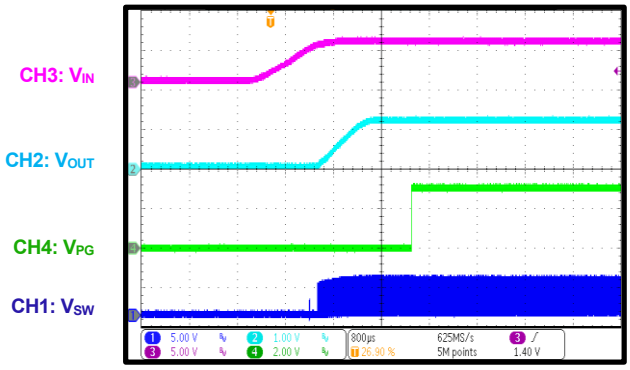
Shutdown through EN
I_{OUT} = 12A



PG in Start-Up through VIN
I_{OUT} = 0A, PSM



PG in Start-Up through VIN
I_{OUT} = 0A, FCCM



PG in Start-Up through VIN
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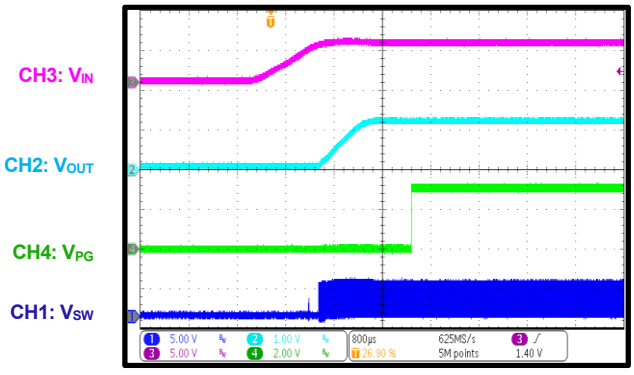

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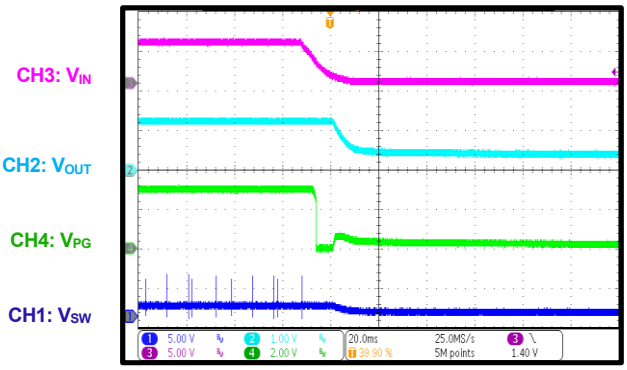
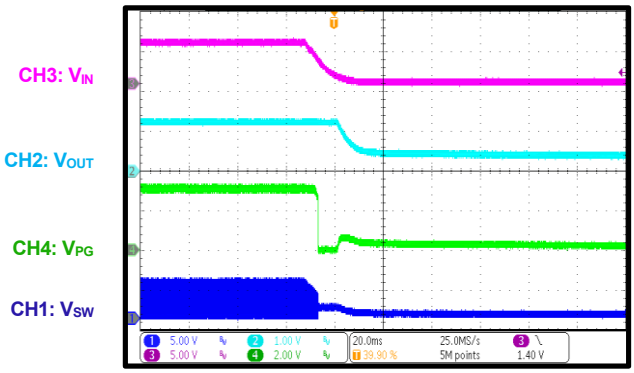
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 1.2V, L = 220nH, C_{OUT} = 4 x 47µF, f_{SW} = 2.2MHz, T_A = 25°C, unless otherwise noted.

PG in Shutdown through VIN
I_{OUT} = 0A, PSM



PG in Shutdown through VIN
I_{OUT} = 0A, FCCM



PG in Shutdown through VIN
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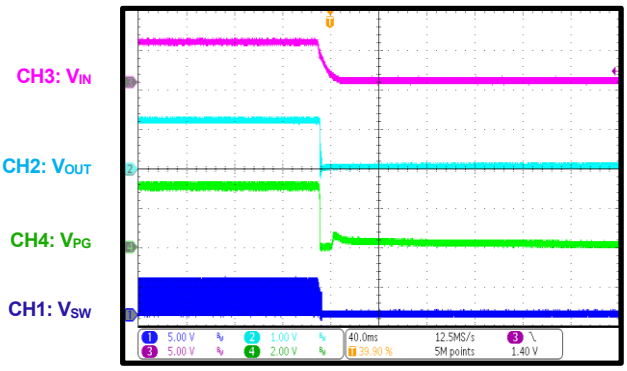

PG in Start-Up through EN
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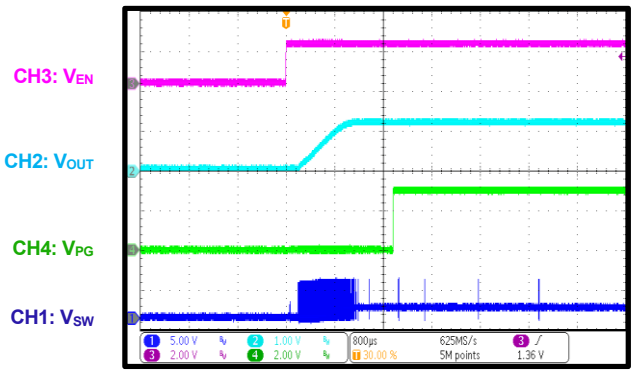
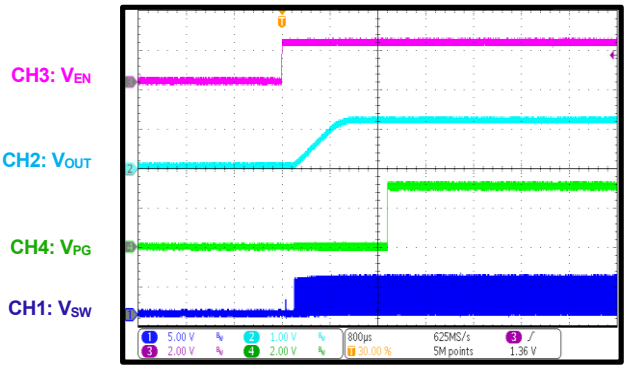
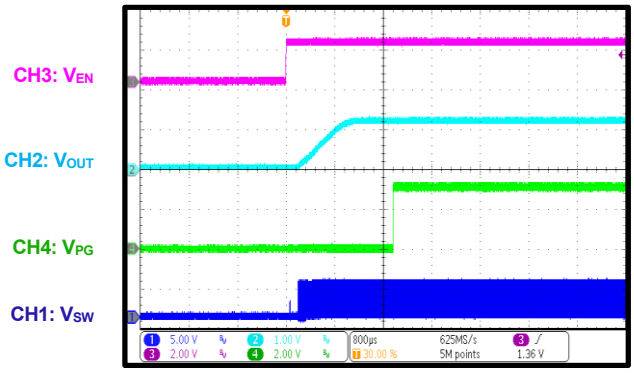


PG in Start-Up through EN
I_{OUT} = 0A, FCCM



PG in Start-Up through EN
I_{OUT} = 12A



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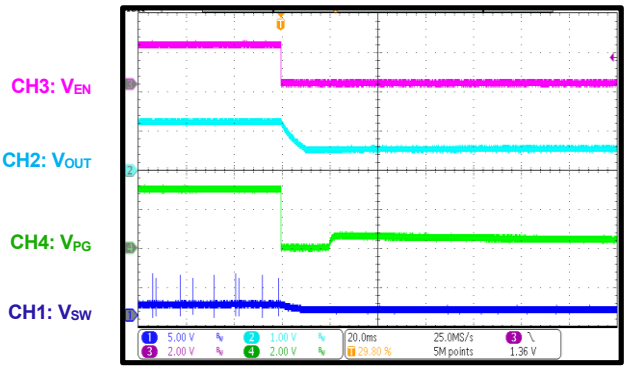
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 1.2V, L = 220nH, C_{OUT} = 4 x 47µF, f_{SW} = 2.2MHz, T_A = 25°C, unless otherwise noted.

PG In Shutdown through EN

I_{OUT} = 0A, PSM



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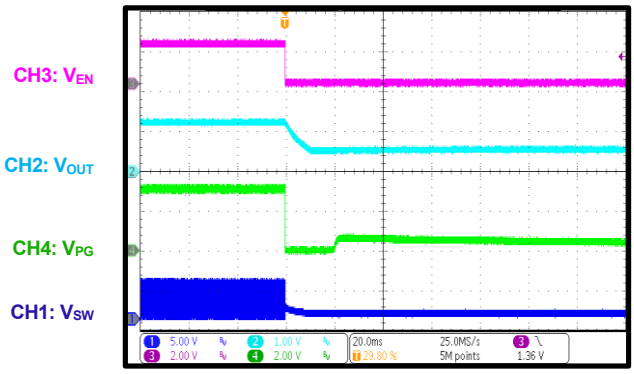
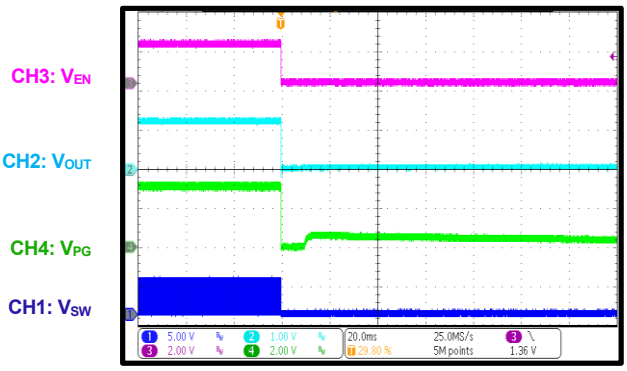
I_{OUT} = 0A, FCCM



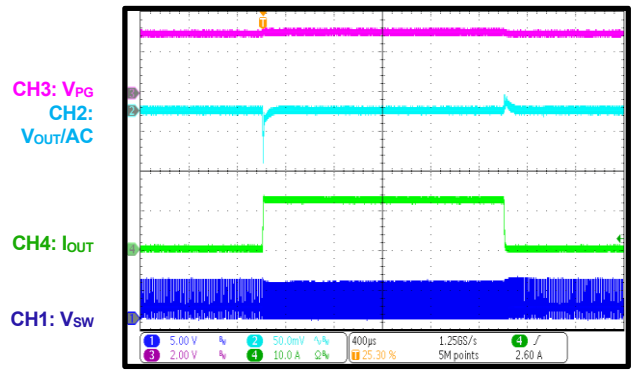
PG In Shutdown through EN

I_{OUT} = 12A



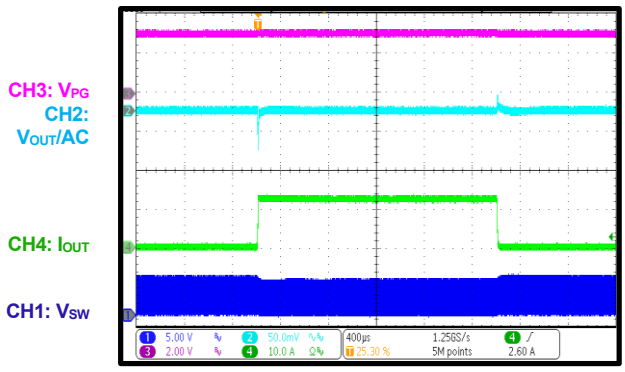
Load Transient Response

I_{OUT} = 0A to 12A, 1.6A/µs, PSM



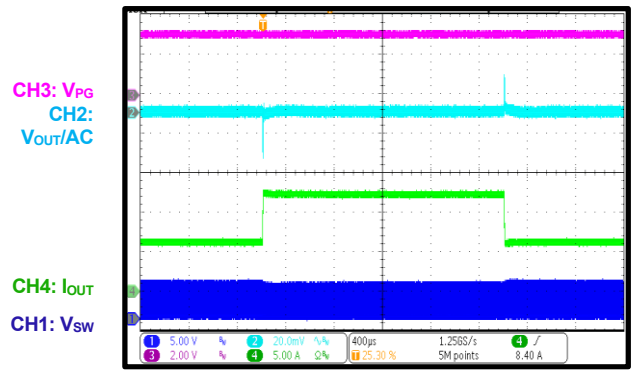
Load Transient Response

I_{OUT} = 0A to 12A, 1.6A/µs, FCCM



Load Transient Response

I_{OUT} = 6A to 12A, 1.6A/µs



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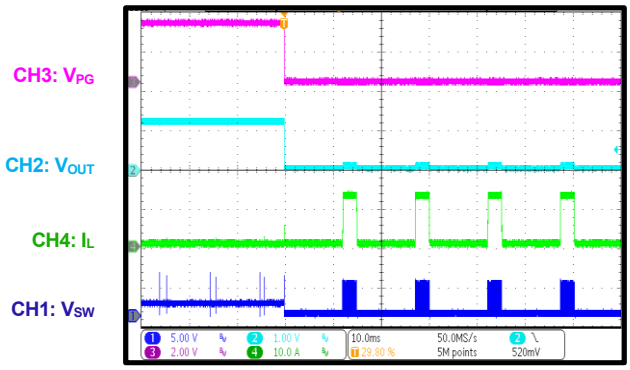
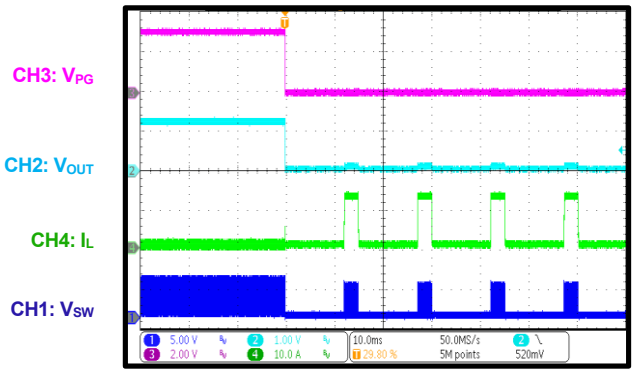
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 1.2V, L = 220nH, C_{OUT} = 4 x 47µF, f_{SW} = 2.2MHz, T_A = 25°C, unless otherwise noted.

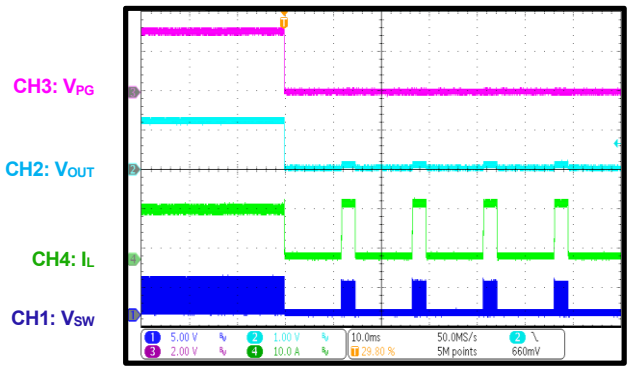
SCP Entry
I_{OUT} = 0A, PSM



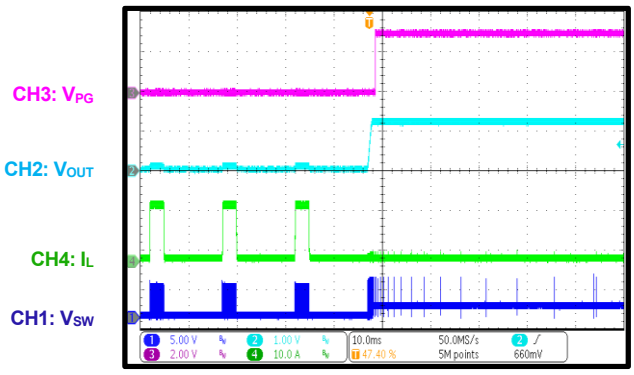
SCP Entry
I_{OUT} = 0A, FCCM



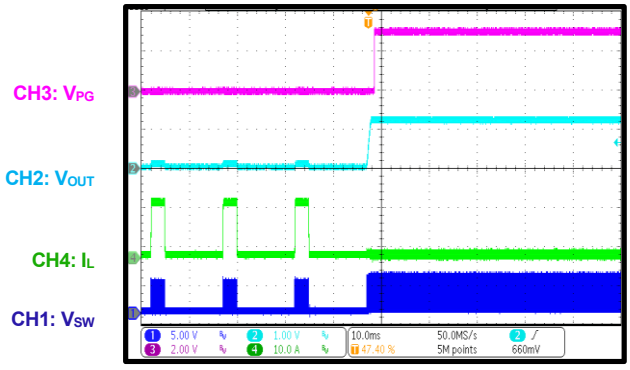
SCP Entry
I_{OUT} = 12A



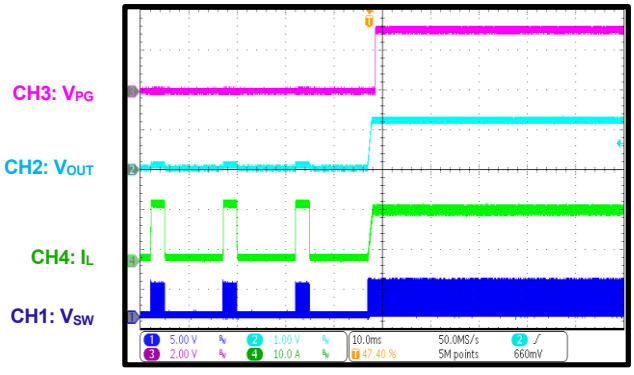
SCP Recovery
I_{OUT} = 0A, PSM



SCP Recovery
I_{OUT} = 0A, FCCM



SCP Recovery
I_{OUT} = 12A



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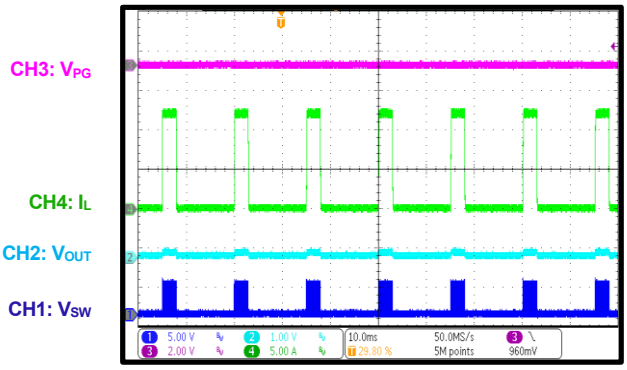
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 1.2V, L = 220nH, C_{OUT} = 4 x 47µF, f_{SW} = 2.2MHz, T_A = 25°C, unless otherwise noted.

SCP Steady State



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FUNCTIONAL BLOCK DIAGRAM

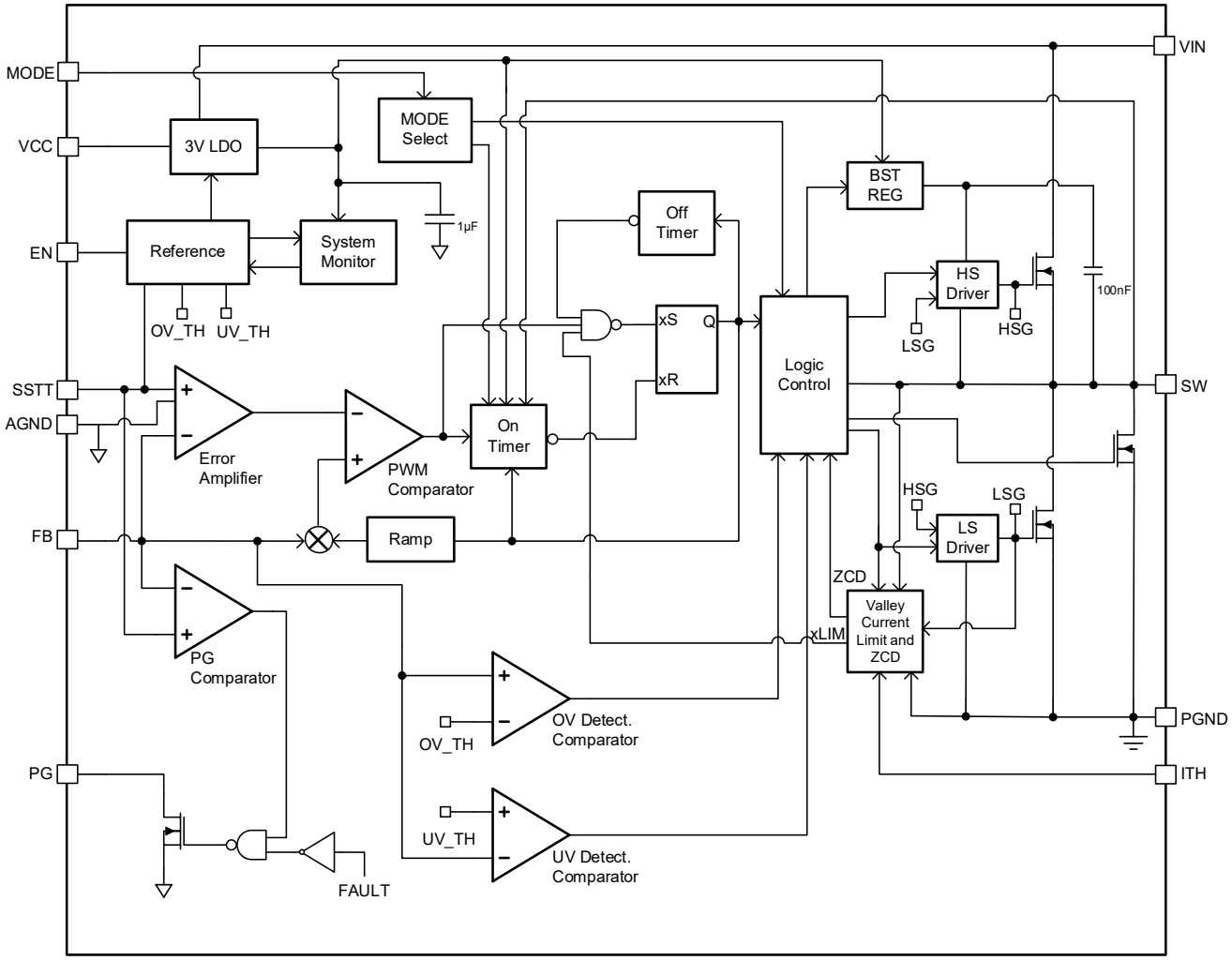

Figure 3: Functional Block Diagram

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OPERATION

Constant-On-Time (COT) Control

The MPQ2211 employs constant-on-time (COT) control to achieve fast load transient response. Figure 4 shows the details regarding the MPQ2211's control stage. The MPQ2211 provides up to 12A of continuous output current (I_{OUT}) from a 3V to 3.6V and 4V to 6V input voltage (V_{IN}) range. To support the 3V to 3.6V V_{IN} range, connect VCC to VIN. The output voltage (V_{OUT}) can be regulated to as low as 0.5V.

The operational amplifier (AMP) corrects any error voltage between the feedback voltage (V_{FB}) and internal reference voltage (V_{REF}, which is typically 0.5V). With the help of the AMP, the MPQ2211 can provide excellent load regulation across the entire load range, regardless of whether it operates in forced continuous conduction mode (FCCM) or pulse-skip mode (PSM).

The MPQ2211 has internal RAMP compensation to support a low-ESR MLCC output capacitor solution. The adaptive internal RAMP is optimized so that the MPQ2211 is stable across the entire operating V_{IN}/V_{OUT} range when the output L/C filter is properly designed.

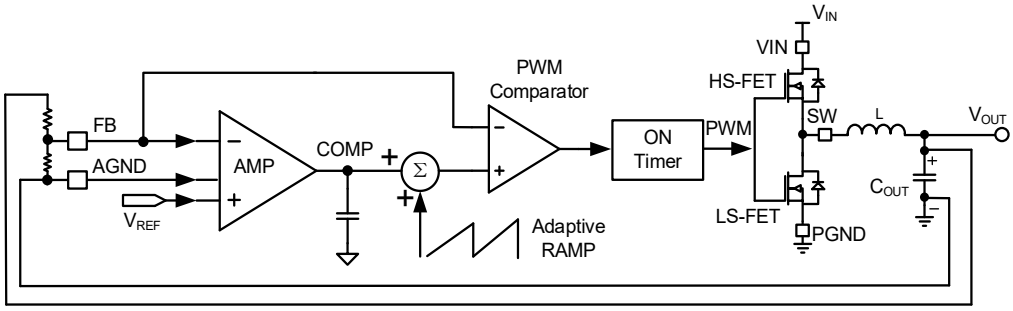

Figure 4: COT Control

Pulse-Width Modulation (PWM) Operation

Figure 5 shows how the pulse-width modulation (PWM) is generated.

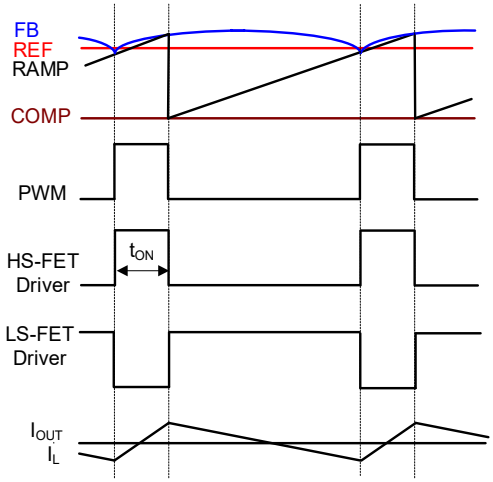

Figure 3: Heavy-Load Operation (PWM)

The AMP corrects any error between V_{FB} and V_{REF}, and generates a fairly smooth DC voltage (V_{COMP}). The internal RAMP is superimposed onto COMP. The superimposed COMP is compared to V_{FB}.

If V_{FB} drops below the superimposed V_{COMP}, the device turns on the integrated high-side MOSFET (HS-FET). The HS-FET stays on for a fixed turn-on time. The fixed on time is determined by V_{IN}, V_{OUT}, and the switching frequency (f_{SW}). After the on period elapses, the HS-FET turns off then turns on again when V_{FB} drops below the superimposed V_{COMP}. The MPQ2211 regulates V_{OUT} by repeating this operation.

The integrated low-side MOSFET (LS-FET) turns on when the HS-FET is in its off state to minimize conduction loss. A dead short occurs between VIN and PGND if both the HS-FET and the LS-FET turn on at the same time (shoot-through). To avoid shoot-through, a dead time (DT) is generated internally between the HS-FET off and the LS-FET on period, or the LS-FET off and the HS-FET on period.

Continuous Conduction Mode (CCM)

Continuous conduction mode (CCM) occurs when the output current (I_{OUT}) is high, and the inductor current (I_L) is always above zero amperes.

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The MPQ2211 can also be configured to operate in FCCM when I_{OUT} is low (see the MODE Selection (MODE, Pin 17) section on page 36 for more details). The MPQ2211 has a negative current limit to prevent the negative current from dropping too low and damaging the components. Once the negative inductor current reaches the negative current limit, the HS-FET immediately turns on and the LS-FET turns off.

In CCM, f_{SW} is fairly constant (pulse-width modulation (PWM) mode), which means that the output voltage ripple stays almost the same across the entire load range.

Pulse-Skip Operation

Under light-load conditions, the MPQ2211 can be configured to work in pulse-skip mode (PSM) to optimize efficiency. When the load decreases, I_L decreases as well. Once I_L reaches zero, the part transitions from CCM to PSM if the MPQ2211 is configured for this function (see the MODE Selection (MODE, Pin 17) section on page 36 for more details).

Figure 6 shows PSM under light-load conditions.

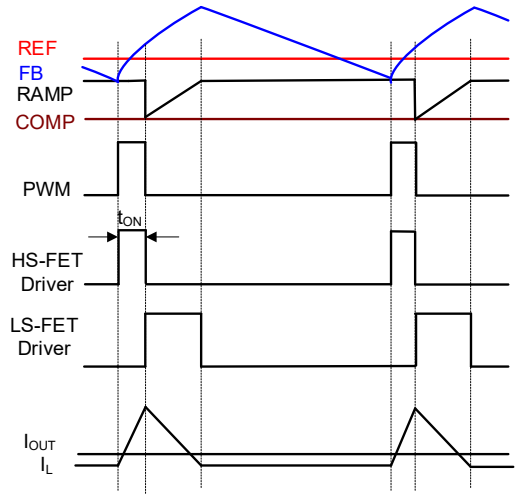

Figure 6: Pulse Skip at Light Loads

When V_{FB} drops below superimposed V_{COMP}, the HS-FET turns on for a fixed interval. When the HS-FET turns off, the LS-FET turns on until I_L reaches zero. In PSM, V_{FB} does not reach superimposed V_{COMP} when I_L approaches zero. The LS-FET driver turns into tri-state (Hi-Z) when I_L reaches zero. Under light-load conditions, the HS-FET does not turn on as frequently in PSM as it does in FCCM. As a result, the efficiency in PSM is greatly improved when compared to FCCM.

As I_{OUT} increases from the light-load condition, the time period during which the current modulator regulates becomes shorter, and the HS-FET turns on more frequently. f_{SW} increases accordingly. I_{OUT} reaches the critical level when the current modulator time is zero. The critical I_{OUT} level can be calculated with Equation (1):

$$I_{OUT} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times L \times f_{SW} \times V_{IN}} \quad (1)$$

Where f_{SW} is the switching frequency.

The part enters PWM mode once I_{OUT} exceeds the critical level. Afterward, f_{SW} stays fairly constant across the I_{OUT} range.

The MPQ2211 can be configured to operate in FCCM even under light-load conditions. See Table 4 on page 36 for the MODE configurations.

Pre-Biased Start-Up

The MPQ2211 has been designed for a monotonic start-up into pre-biased loads. If the output is pre-biased to a certain voltage during start-up, the IC disables switching for both the HS-FET and LS-FET until the voltage on the SSTT capacitor exceeds the sensed output voltage at FB.

Output Voltage (V_{OUT}) Discharge

When the MPQ2211 is disabled through EN, it enables output voltage discharge mode. This causes both the HS-FET and the LS-FET to latch off. A discharge FET connected between SW and PGND turns on to discharge the output voltage. The typical switch-on resistance of this FET is about 80Ω. Once V_{FB} drops below 200mV, the discharge FET turns off.

Output Over-Voltage Protection (OVP)

The MPQ2211 monitors the output voltage by connecting FB to the tap of the output voltage feedback resistor divider to detect an over-voltage condition. This provides latch-off over-voltage protection (OVP) mode.

If V_{FB} exceeds 116% of V_{REF}, the device enters latch-off OVP. The HS-FET latches off and PG latches low until power is cycled on VIN or EN. Meanwhile, the LS-FET remains on until it reaches the low-side negative current limit. Once

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the LS-FET reaches the -7.5A negative current limit, the LS-FET is momentarily turned off for 200ns and then turns on again.

The MPQ2211 maintains this operation to lower V_{OUT}. When V_{FB} drops below 50% of V_{REF}, the LS-FET turns off for PSM and keeps turning on for FCCM. If V_{FB} rises to exceed 116% of V_{REF}, the LS-FET turns on again with a low-side negative current limit until V_{FB} drops back below 50% of V_{REF}. The power must be cycled on EN or VIN to clear the OVP fault.

The OVP function is enabled after SSTT reaches 500mV.

Over-Temperature Protection (OTP)

The MPQ2211 has over-temperature protection (OTP). The IC monitors the internal junction temperature (T_J). If T_J exceeds the threshold (168°C, typically), the converter shuts off and discharges the SSTT capacitors. This is a non-latch protection. There is about a 20°C hysteresis. Once T_J drops to about 148°C, the MPQ2211 initiates a soft start.

The OTP function is effective once the MPQ2211 is enabled.

Over-Current Protection (OCP)

Over-current protection (OCP) with hiccup mode is active 3ms after the MPQ2211 is enabled. Once OCP hiccup mode is active, if the MPQ2211 detects an OC condition for 31 consecutive cycles, or if V_{FB} drops below the under-voltage protection (UVP) threshold, the device enters hiccup mode.

In hiccup mode, the MPQ2211 latches off the HS-FET immediately, then latches off the LS-FET after zero-current detection (ZCD) is detected. Meanwhile, the SSTT capacitor is also discharged. After about 11ms, the MPQ2211 tries to soft start automatically. If the OC condition still exists after the MPQ2211 has run for 3ms after soft start, the MPQ2211 repeats this operation cycle until the OC condition disappears, and the output voltage rises smoothly back to the regulation level.

Output Sinking Mode (OSM)

The MPQ2211 employs output sinking mode (OSM) to regulate V_{OUT} to the targeted value. If V_{FB} exceeds 104% of V_{REF} but is below the OVP threshold, the device triggers OSM. During OSM operation, the LS-FET remains on until it reaches the -5.5A negative current limit. Once the LS-FET reaches -5.5A, is turns off momentarily for 200ns then turns on again. The MPQ2211 maintains this operation until V_{FB} drops below 102% of V_{REF}. Afterward, the MPQ2211 exits OSM after 15 consecutive cycles of FCCM.

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APPLICATION INFORMATION

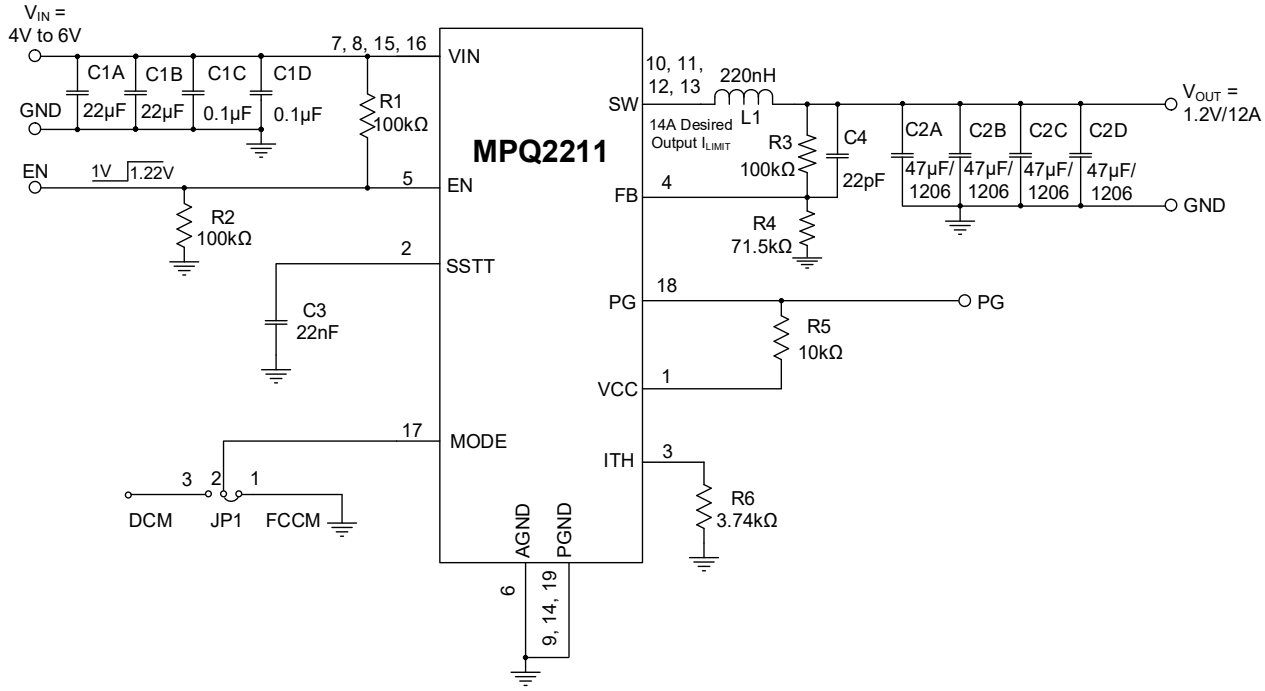

Figure 7: Typical Application Circuit (V_{OUT} = 1.2V, I_{OUT} = 12A, f_{SW} = 2.2MHz)

Table 1: Design Guide Index and Recommended Values

Pin Number	Pin Name	Component	Design Guide Index	Value
1	VCC		Internal 3V LDO Output (VCC, Pin 1)	-
2	SSTT	C3	Soft Start, Output Voltage Tracking and Reference (SSTT, Pin 2)	22nF
3	ITH	R6	Setting the Current Limit Threshold (ITH, Pin 3)	3.74kΩ
4	FB	R3, R4, C4	Feedback (FB, Pin 4)	100kΩ, 71.5kΩ, 22pF
5	EN	R1, R2	Enable (EN, Pin 5)	100kΩ, 100kΩ
6	AGND	-	GND Connection (PGND, Pins 9, 14, and 19; AGND, Pin 6)	-
7, 8, 15, 16	VIN	C1A, C1B, C1C, C1D	Selecting the Input Capacitor (VIN, Pins 7, 8, 15, and 16)	22µF, 22µF, 0.1µF, 0.1µF
9, 14, 19	PGND	-	GND Connection (PGND, Pins 9, 14, and 19; AGND, Pin 6)	-
10, 11, 12, 13	SW	L1, C2A, C2B,C2C, C2D	Selecting the Inductor and Output Capacitor (SW, Pins 10, 11, 12, and 13)	220nH, 47µF, 47µF, 47µF, 47µF
17	MODE		MODE Selection (MODE, Pin 17)	-
18	PG	R5	Power Good indicator (PG, Pin 18)	10kΩ

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Internal 3V LDO Output (VCC, Pin 1)

There is internal VCC capacitor, so there is no need to add an external capacitor. The internal driver and control circuits are powered by the internal, 3V low-dropout (LDO) regulator. This regulator uses VIN as its input and operates across the full V_{IN} range. This pin can be connected to PG through a pull-up resistor to act as the voltage source for the PG function. Connect VCC to VIN directly when V_{IN} below 3.6V. Float the VCC pin if it is not used.

Soft Start, Output Voltage Tracking and Reference (SSTT, Pin 2)

Soft Start (SS)

The minimum soft-start time (t_{SS}) is limited at 0.9ms. It can be increased by adding a soft-start capacitor (C_{SSTT}) between SSTT and AGND. If C_{SSTT} exceeds 68nF, t_{SS} is determined by C_{SSTT}.

C_{SSTT} can be estimated with Equation (2):

$$C_{SSTT}(nF) = \frac{t_{SS}(ms) \times 36(\mu A)}{0.5(V)} \quad (2)$$

Where C_{SSTT} is the external SSTT capacitor, which is recommended to be at least 22nF.

Output Voltage (V_{OUT}) Tracking and Reference

The MPQ2211 provides an analog input pin (SSTT) to track another power supply or accept an external reference. When an external voltage signal is connected to SSTT, the external voltage acts as a reference for the MPQ2211's V_{OUT}. V_{FB} follows this external voltage signal exactly, and the soft-start settings are ignored. The SSTT input signal can be between 0.3V and 1.4V. During the initial start-up, SSTT must reach at least 500mV first to ensure proper operation. Afterward, the SSTT voltage can be any value between 0.3V and 1.4V.

Setting the Current Limit Threshold (ITH, Pin 3)

Current-Limit Threshold

The MPQ2211 features an on-die current sense and a configurable, positive current limit threshold.

The current limit is active when the MPQ2211 is enabled. During the LS-FET on state, the SW current (inductor current) is sensed and mirrored to ITH with the ratio of G_{ITH}. By using a resistor (R_{ITH}) from ITH to AGND, the ITH voltage (V_{ITH}) is proportional to the SW current cycle-by-cycle. The HS-FET is only allowed to turn on when V_{ITH} is below the internal OCP voltage threshold (V_{OCP}) (during the LS-FET on state) to limit the SW valley current cycle-by-cycle.

Calculate the current-limit threshold from R_{ITH} with Equation (3):

$$R_{ITH}(\Omega) = \frac{V_{OCP}}{G_{ITH} \times \left(I_{LIM} - \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \times \frac{1}{2 \times L \times f_{SW}} \right) + 47(\mu A)} \quad (3)$$

Where V_{OCP} =1.2V, G_{ITH} = 20μA/A, and I_{LIM} = the target output current limit.

Table 2 lists the target output current limit for different output load currents.

Table 2: Target Current Limit for Output Load Current

I_{OUT} (A)	I_{LIM} (A)
8	10
10	12
12	14

Feedback (FB, Pin 4)

The feedback voltage is typically 0.5V, and its output can be adjusted from 0.5V to 3.6V. The external resistor divider connected to FB sets the output voltage (see Figure 8). Limit V_{OUT} to 60% of V_{IN} to prevent triggering the minimum off time condition, which can cause V_{OUT} to drop.

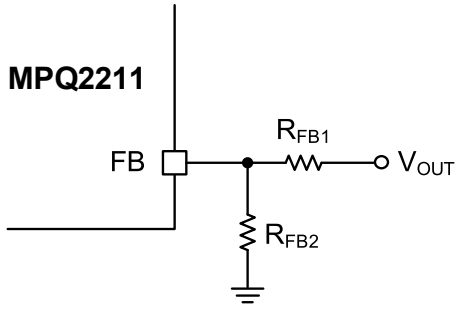

Figure 8: Feedback Divider Network of Adjustable Output version

Estimate R_{FB2} with Equation (4):

$$R_{FB2} = \frac{0.5(V)}{V_{OUT} - 0.5(V)} \times R_{FB1} \quad (4)$$

Table 3 on page 35 lists the recommended resistors value for common output voltages.

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Table 3: Resistor Values for Common Output Voltages

V_{OUT} (V)	R_{FB1} (kΩ)	R_{FB2} (kΩ)
0.8	60.4 (1%)	100 (1%)
1.0	100 (1%)	100 (1%)
1.2	100 (1%)	71.5 (1%)
1.8	100 (1%)	38.3 (1%)
2.5	75 (1%)	18.7 (1%)
3.3	100 (1%)	17.8 (1%)

To optimize the load transient response, a feed-forward capacitor (C_{FF}) is recommended to be placed in parallel with R_{FB1}. R_{FB1} and C_{FF} add an extra zero to the system, which improves the loop response. R_{FB1} and C_{FF} are selected so that the zero (f_Z) formed by R_{FB1} and C_{FF} is between 40kHz and 160kHz. f_Z can be calculated with Equation (5):

$$f_Z = \frac{1}{2\pi \times R_{FB1} \times C_{FF}} \quad (5)$$

Enable (EN, Pin 5)

The MPQ2211 turns on when EN exceeds its rising threshold (1.22V, typically), and it turns off when EN drops below its falling threshold (1V, typically). The EN pin cannot be left floating for proper operation. EN can be driven by an analog or digital control logic signal to enable/disable the MPQ2211. The maximum current going to EN is 50μA.

The MPQ2211 provides accurate EN thresholds, so a resistor divider connected from VIN to PGND can be used to configure the input voltage at which the MPQ2211 is enabled (see Figure 9).

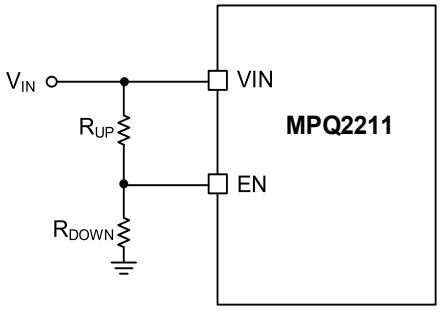

Figure 9: EN Control Divider Network

This is highly recommended for applications where there is no dedicated EN control logic signal, as it prevents potential UVLO bouncing during start-up and shutdown. The resistor divider values can be estimated with Equation (6):

$$V_{IN_START}(V) = V_{EN} \times \frac{R_{UP} + R_{DOWN}}{R_{DOWN}} \quad (6)$$

R_{UP} and R_{DOWN} should be selected such that the EN voltage (V_{EN}, typically 1.22V) does not exceed 3.6V when V_{IN} reaches its maximum value.

GND Connection (PGND, Pin 9, 14 and 19; AGND, Pin 6)

See the PCB Layout Guidelines section on page 38 for more details.

Selecting the Input Capacitor (VIN, Pins 7, 8, 15, and 16)

The step-down converter has a discontinuous input current, and requires a capacitor to supply the AC current to the converter while maintaining the DC input voltage. Use ceramic capacitors for the best performance. It is strongly recommended to use another, lower-value capacitor (e.g. 0.1μF) with a small package size (0402) to absorb high-frequency switching noise. Place the smaller capacitor as close to VIN and GND as possible.

The capacitance can vary significantly with temperature. Use capacitors with X5R and X7R ceramic dielectrics because they are fairly stable across a wide temperature range and they offer very low ESR.

The capacitors must have a ripple current rating that exceeds the converter's maximum input ripple current. Calculate the input ripple current with Equation (7):

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (7)$$

The worst-case condition occurs at $V_{IN} = 2 \times V_{OUT}$, estimated with Equation (8):

$$I_{CIN} = \frac{I_{OUT}}{2} \quad (8)$$

For simplification, choose an input capacitor with an RMS current rating that exceeds half the maximum load current. The input capacitance determines the converter input voltage ripple. If there is an input voltage ripple requirement in the

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system, select an input capacitor that meets the specification.

Estimate the input voltage ripple with Equation (9):

$$\Delta V_{IN} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (9)$$

The worst-case condition occurs at V_{IN} = 2 x V_{OUT}, calculated with Equation (10):

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{f_{SW} \times C_{IN}} \quad (10)$$

Selecting the Inductor and Output Capacitor (SW, Pins 10, 11, 12, and 13)

Selecting the Output Capacitor

The output capacitor maintains the DC output voltage. Estimate the output voltage ripple with Equation (11):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}}) \quad (11)$$

Where L is the inductance and R_{ESR} is the output capacitor's equivalent series resistance (ESR).

For ceramic capacitors, the capacitance dominates the impedance at the switching frequency and causes the majority of the output voltage ripple. For simplification, calculate the output voltage ripple with Equation (12):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^2 \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (12)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be estimated with Equation (13):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (13)$$

Selecting the Inductor

The inductor supplies constant current to the output load while being driven by the switching input voltage. A larger-value inductor results in less ripple current and lower output ripple voltage but has a larger physical size, a higher series resistance, and/or a lower saturation current. Generally, select an inductor value that allows the inductor peak-to-peak ripple current to be 30% to 40% of the maximum switch current limit. Design for a peak inductor current that is below the maximum switch current limit. Calculate the inductance with Equation (14):

$$L = \frac{V_{OUT}}{f_{SW} \times \Delta I_L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (14)$$

Where ΔI_L is the peak-to-peak inductor ripple current.

Choose an inductor that will not saturate under the maximum inductor peak current. The peak inductor current can be calculated with Equation (15):

$$I_{LP} = I_{OUT} + \frac{V_{OUT}}{2 \times f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (15)$$

MODE Selection (MODE, Pin 17)

The MPQ2211 provides both FCCM and PSM under light-load conditions. Selecting the operation mode under light-load conditions is accomplished by connected the MODE pin to GND, or by floating MODE or connected it to VCC (see Table 4). The mode can be changed within a certain time (110us, typically) after the device is enabled. The mode cannot be changed during operation unless the device re-powers on VIN or re-enables EN.

Table 4: MODE Selection

MODE	Light-Load Mode	Switching Frequency
Float (or VCC)	PSM	2200kHz
GND	FCCM	2200kHz

Power Good indicator (PG, Pin 18)

The MPQ2211 has a power good (PG) output. PG is the open drain of a MOSFET. Connect PG to VCC or another external voltage source (below 3.6V) through a pull-up resistor (10kΩ, typically). After applying the input voltage, the MOSFET turns on, so PG is pulled to GND before SSTT is ready. After V_{FB} reaches 92.5% of V_{REF}, PG is pulled high after a 1ms delay.

When V_{FB} drops to 80% of V_{REF} or exceeds 116% of the nominal V_{REF}, PG latches low. PG can only be pulled high again after a new soft start.

If the input supply fails to power the MPQ2211, PG is clamped low even though PG is tied to an external DC source through a pull-up resistor. Figure 10 on page 37 shows the relationship

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between the PG voltage (V_{PG}) and the pull-up current (I_{PG}).

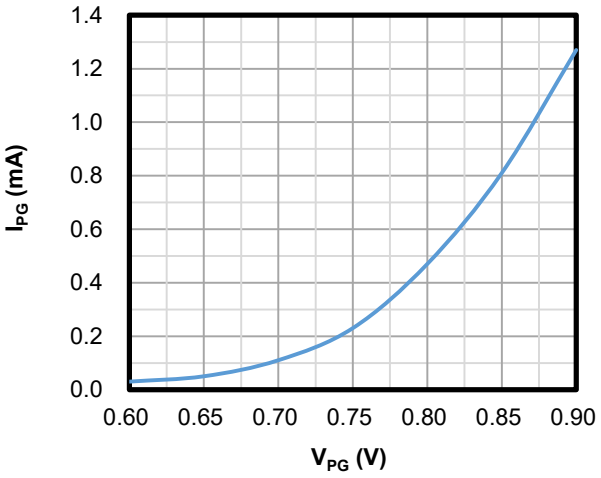

Figure 10: PG Clamped Voltage vs. Pull-Up Current

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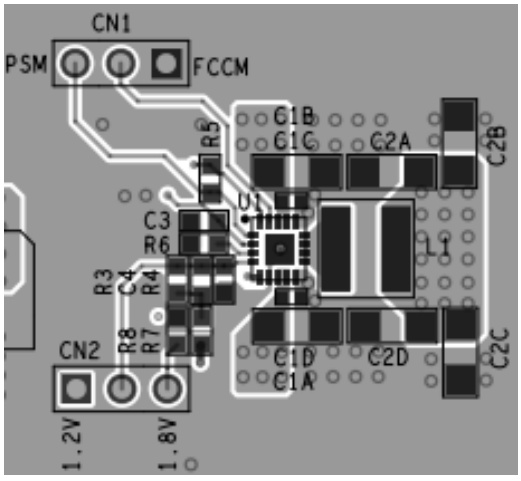
PCB Layout Guidelines [8]

Efficient PCB layout, especially for input capacitor placement, is critical for stable operation. A 4-layer layout is strongly recommended to improve thermal performance. For the best results, refer to Figure 9 and follow the guidelines below:

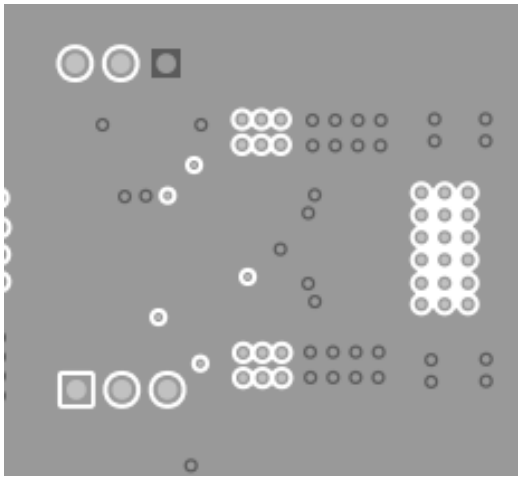
1. Place symmetric input capacitors as close to VIN and GND as possible.
2. Use a large ground plane to connect directly to PGND.
3. Add vias near PGND if the bottom layer is a ground plane.
4. Ensure that the high-current paths at GND and VIN have short, direct, and wide traces. Place the ceramic input capacitor, especially the small package size (0402) input bypass capacitor, as close to VIN and PGND as possible to minimize high-frequency noise.
5. Keep the connection between the input capacitor and VIN as short and wide as possible.
6. Use multiple vias to connect the power planes to the internal layers.

Notes:

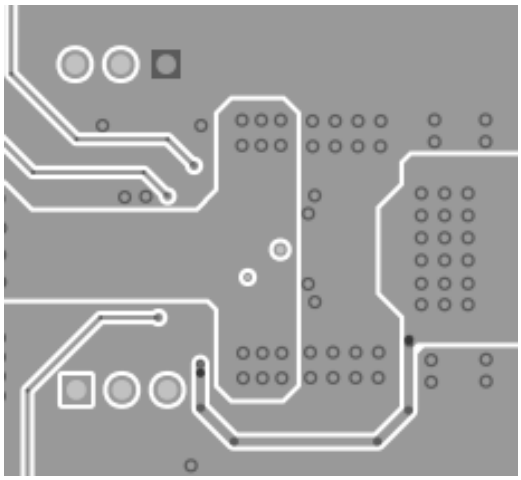
8) The recommended PCB layout is based on Figure 12 on page 39.



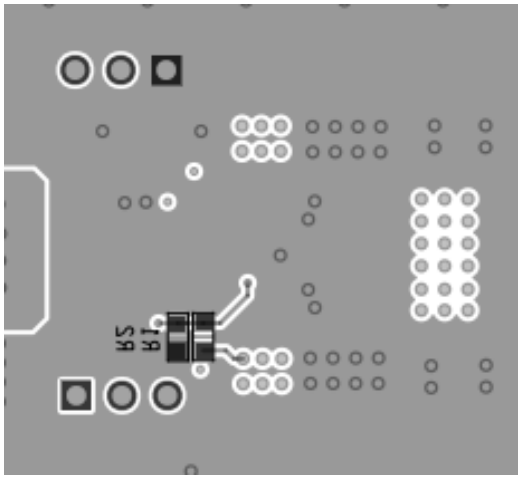
Top Layer



Mid-Layer 1



Mid-Layer 2



Bottom Layer

Figure 11: Recommended PCB Layer

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TYPICAL APPLICATION CIRCUIT

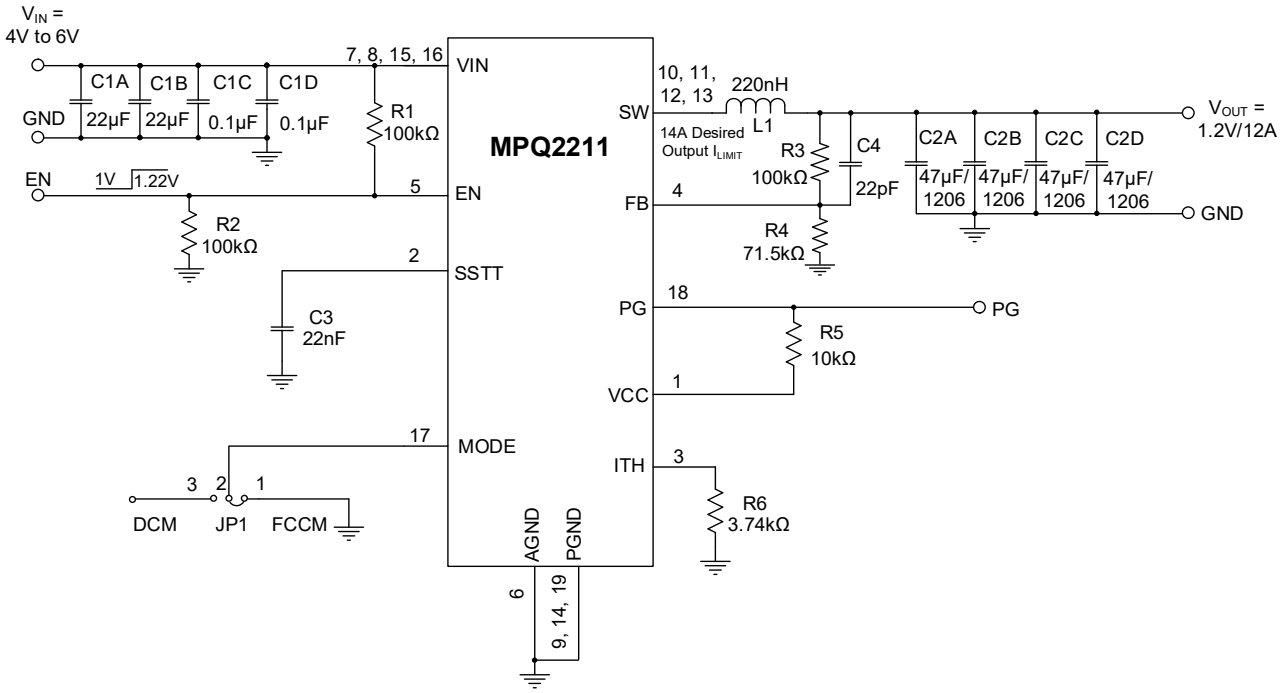

Figure 12: Typical Application Circuit (V_{IN} = 4V to 6V, V_{OUT} = 1.2V, I_{OUT} = 12A, f_{SW} = 2.2MHz)

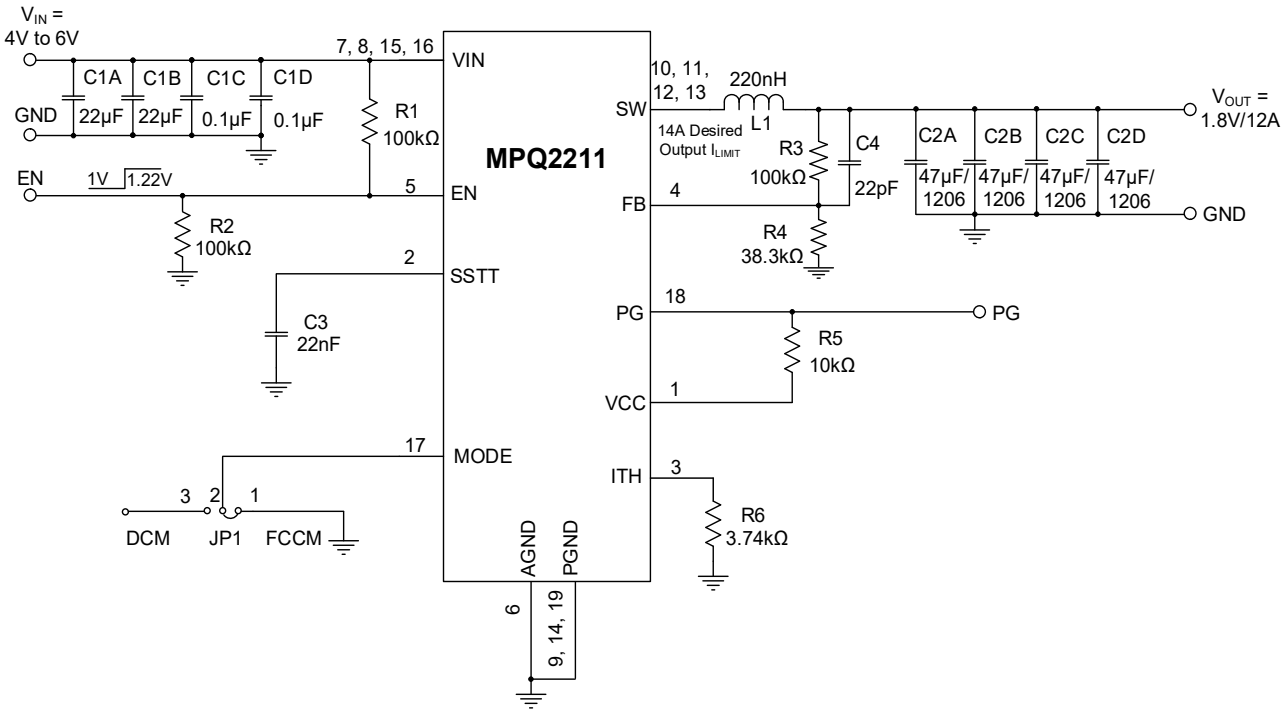

Figure 13: Typical Application Circuit (V_{IN} = 4V to 6V, V_{OUT} = 1.8V, I_{OUT} = 12A, f_{SW} = 2.2MHz)

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TYPICAL APPLICATION CIRCUITS *(continued)*

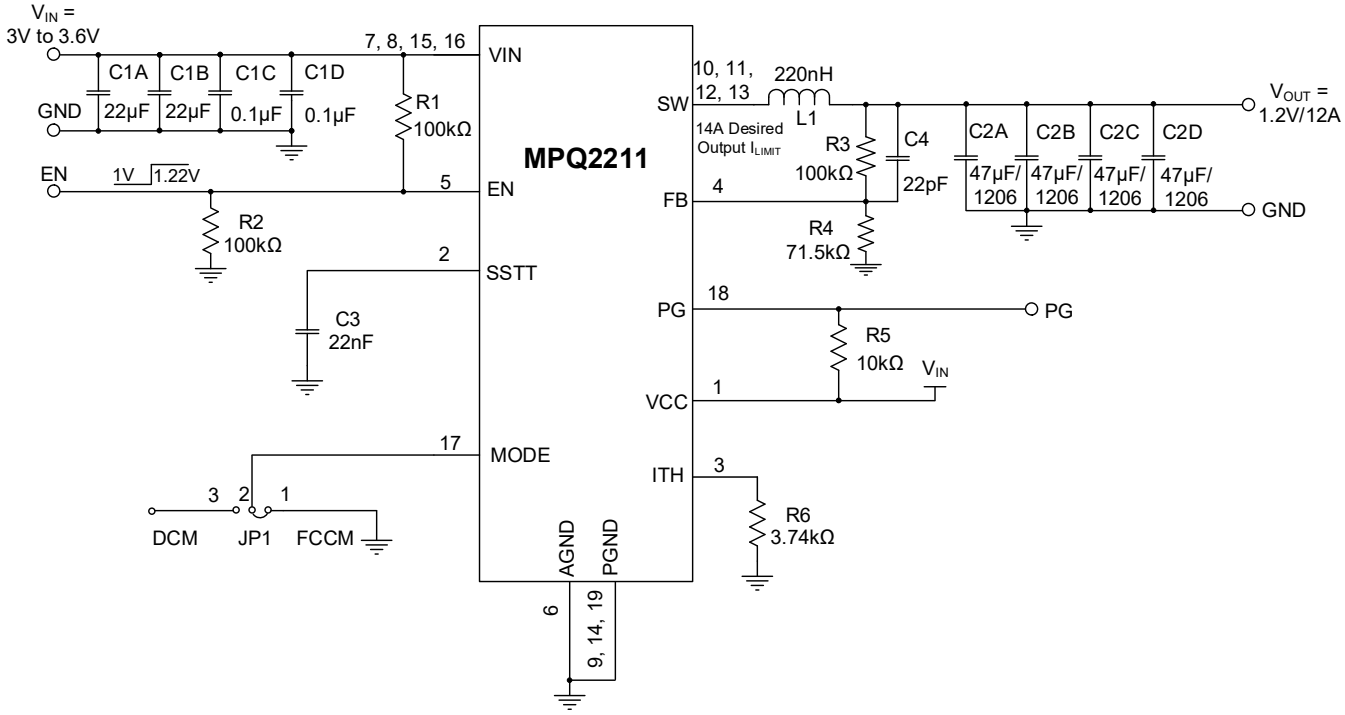

Figure 14: Typical Application Circuit (V_{IN} = 3V to 3.6V, V_{OUT} = 1.2V, I_{OUT} = 12A, f_{SW} = 2.2MHz)

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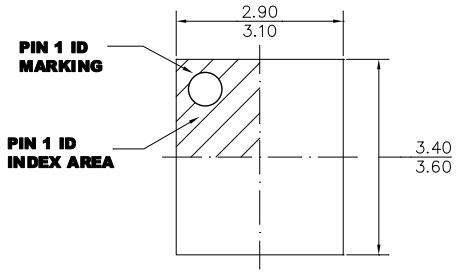
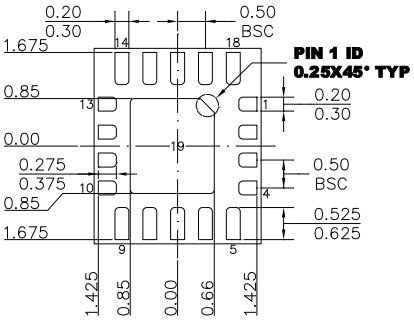
PACKAGE INFORMATION

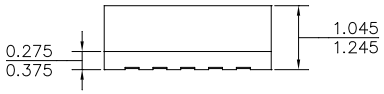
LGA-19 (3mmx3.5mm)



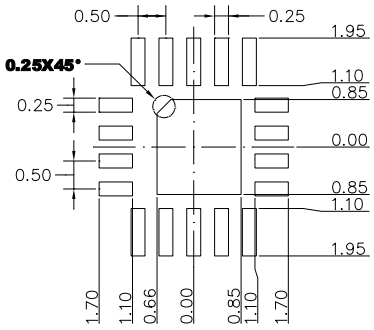
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-303.
4) DRAWING IS NOT TO SCALE.

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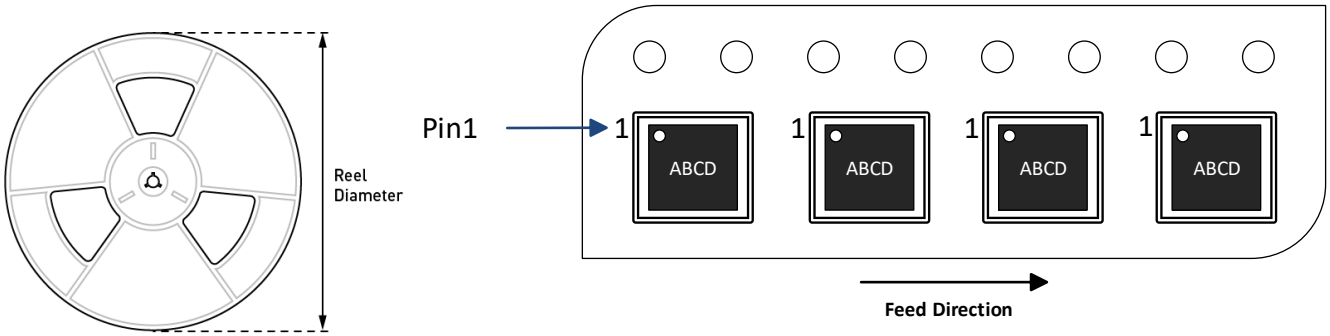
CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ2211GLC-AEC1-Z	LGA-19 (3mmx3.5mm)	2500	N/A	N/A	13in	12mm	8mm

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REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	10/23/2025	Initial Release	-

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