MPQ2180

6A, 2.7V to 6V, High-Efficiency, Synchronous Step-Down Converter with I²C Interface, AEC-Q100 Qualified

DESCRIPTION

The MPQ2180 is a highly integrated, high-frequency, synchronous step-down converter with an I²C control interface. The MPQ2180 can support up to 6A of load current across an input voltage (V_{IN}) supply range from 2.7V to 6V, with excellent load and line regulation.

Constant-frequency hysteretic mode provides an extremely fast transient response without loop compensation to achieve high efficiency under light-load conditions.

The output voltage (V_{OUT}) can be controlled on-the-fly through a 3.4Mbps I²C serial interface. The voltage range can be adjusted from 0.6V to 1.235V in 5mV steps. The V_{OUT} slew rate, switching frequency (f_{SW}), and power-save mode can be configured via the I²C interface.

Full protection features include internal soft start, over-current protection (OCP), and thermal shutdown.

The MPQ2180 requires a minimal number of readily available, standard external components, and is available in a compact QFN-14 (2.5mmx3mm) package.

MPQ2180 FAMILY VERSIONS

Part Number	Default V_{OUT}	Default Frequency	Default Mode
MPQ2180-8	0.8V	1.25MHz	FCCM
MPQ2180-10	1V	1.25MHz	FCCM

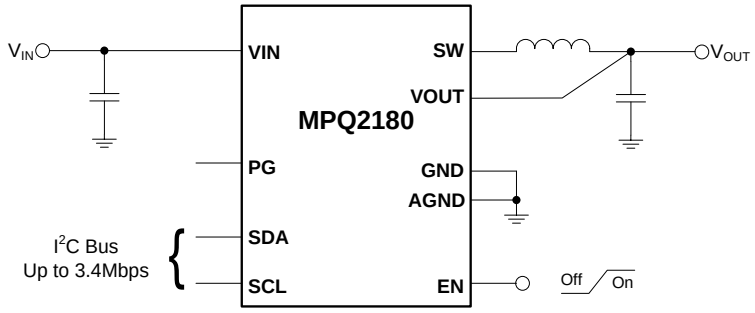
FEATURES

- Flexible with I²C Interface:
  - I²C-Configurable Output Voltage (V_{OUT}) Range from 0.6V to 1.235V in 5mV Steps
  - Adjustable Switching Frequency (f_{SW}) from 0.85MHz to 2.2MHz
  - I²C-Compatible Interface up to 3.4Mbps
  - Power-Save Mode Selectable via I²C
- Designed for Heavy Loads:
  - Up to 6A Load Current
  - Internal 40mΩ High-Side and 22mΩ Low-Side Power MOSFETs
- Additional Features:
  - 2.7V to 6V Input Voltage (V_{IN}) Range
  - Internal 165µs Soft Start
  - Power Good (PG) Indicator
  - Current Overload and Thermal Shutdown Protection
  - Available in a QFN-14 (2.5mmx3mm) Package
  - Available in a Wettable Flank Package
  - Available in AEC-Q100 Grade 1

APPLICATIONS

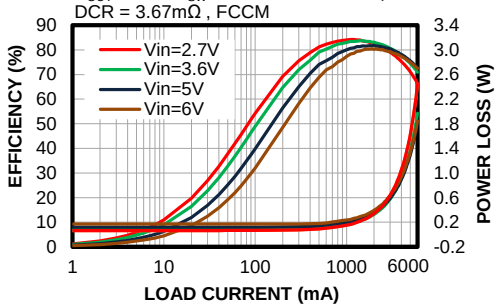
- Automotive Infotainment Systems
- Automotive Telematics Systems
- Advanced Driver Assistance Systems (ADAS)
- Automotive Applications
- Processor Core Supplies

TYPICAL APPLICATION



Efficiency vs. Load Current vs. Power Loss

V_{OUT} = 0.8V, f_{SW} = 1.25MHz, L = 0.47µH, DCR = 3.67mΩ , FCCM

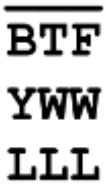


ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating**
MPQ2180GQBE-8-AEC1***	QFN-14 (2.5mmx3mm)	*See Below*	1
MPQ2180GQBE-10-AEC1***	QFN-14 (2.5mmx3mm)	*See Below*	1

*For Tape & Reel, add suffix -Z (e.g. MPQ2180GQBE-8-AEC1-Z).
** Moisture Sensitivity Level Rating
***Wettable Flank

TOP MARKING (MPQ2180GQBE-8-AEC1)

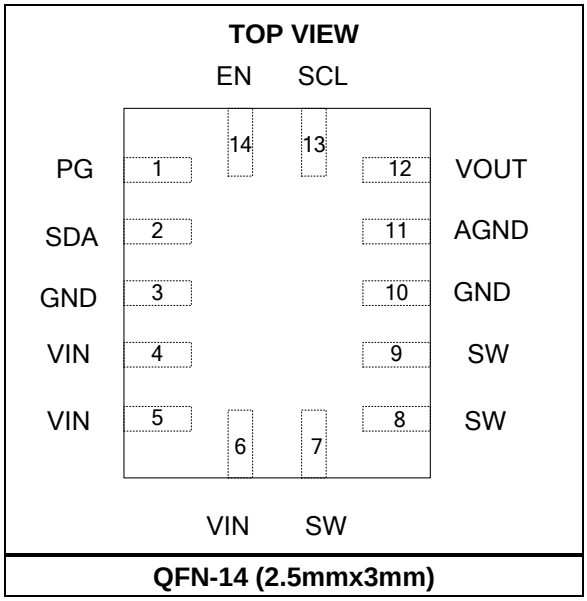


BTF: Product code of MPQ2180GQBE-8-AEC1
Y: Year code
WW: Week code
LLL: Lot number

TOP MARKING (MPQ2180GQBE-10-AEC1)

BTG: Product code of MPQ2180GQBE-10-AEC1
Y: Year code
WW: Week code
LLL: Lot number

PACKAGE REFERENCE



QFN-14 (2.5mmx3mm)

PIN FUNCTIONS

Pin #	Name	Description
1	PG	**Power good output.** The output of the PG pin is an open drain that goes low if the output voltage (V_{OUT}) exceeds 110% of nominal voltage or drops below 85% of the nominal voltage. Connect PG to a ≤6V voltage source with a resistor (e.g. 100kΩ). The PG pin can be floated if it is not used.
2	SDA	**I²C serial data.** The SDA pin can be floated if it is not used.
3, 10	GND	**Power ground.** The GND pin should be electrically connected to the system's power ground plane with the shortest and lowest impedance connection possible.
4, 5, 6	VIN	**Input supply voltage.** In addition to placing a large bulk input capacitor at the VIN pin for a stable power source, connect a bypass capacitor from VIN to GND to reduce noise. The bypass capacitor should be placed as close to the chip as possible.
7, 8, 9	SW	**Switch node.** The SW pin is the output from the high-side switch. SW should be connected to one side of the external power inductor.
11	AGND	**Analog ground.** The AGND pin is the ground for the internal logic and signal control blocks.
12	VOUT	**Output voltage sense.** Connect the VOUT pin directly to the MPQ2180's output. Note that the device's output voltage cannot be set by using an external resistor divider and connecting VOUT to the tap of divider.
13	SCL	**I²C serial clock.** The SCL pin can be floated if it is not used.
14	EN	**On and off control.** Pull the EN pin below 0.4V to shut the chip down. Pull EN above 1.8V to enable the chip. Floating EN shuts the chip down, since an internal 1MΩ resistor is connected from EN to ground.

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}) .....-0.3V to +7V
V_{SW}.....-0.3V (-5V for <10ns) to
…….+6.5V (+8V for <10ns or +10V for <3ns)
All other pins .....-0.3V to +6.5V
Junction temperature .....150°C
Lead temperature .....260°C
Continuous power dissipation (T_A = 25°C) (2) (7)
QFN-14 (2.5mmx3mm)..... 3.78W
Storage temperature..... -65°C to +150°C

ESD Ratings

Human body mode (HBM) .....Class 2 (3)
Charged device mode (CDM) ..... Class C2b (4)

Recommended Operating Conditions

Supply voltage (V_{IN}) .....2.7V to 6V
Output voltage (V_{OUT}).....0.6V to 1.235V
Operating junction temp (T_J)……...
……-40°C to +125°C (5)

Thermal Resistance θ_{JA} θ_{JC}

QFN-14 (2.5mmx3mm)		
JESD51-7 (6)	60	13 °C/W
EVQ2180-QB-00A (7)	33	3 °C/W

Notes:

1) Absolute maximum ratings are rated under room temperature unless otherwise noted.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can produce an excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) Per AEC-Q100-002.
4) Per AEC-Q100-011.
5) Operating junction temperatures above 125°C may be supported; contact MPS for details.
6) Measured on JESD51-7, 4-layer PCB. The values given in this table are only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.
7) Measured on EVQ2180-QB-00A, 4-layer PCB, 2oz copper thickness, 6.35cmx6.35cm.

ELECTRICAL CHARACTERISTICS

V_{IN} = 5V, T_J= -40°C to +125°C, typical values refer to T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input voltage range	V_{IN}		2.7		6	V
Quiescent current	I_Q	EN = 1.8V, no switching, PFM		300		µA
		EN = 1.8V, no switching, PWM		780		µA
Shutdown current	I_S	EN = GND, T_J = 25°C			1	µA
Internal reference voltage	V_{REF}	T_J = 25°C	0.585	0.600	0.615	V
		T_J = -40°C to +125°C	0.579	0.600	0.621	V
Output voltage	V_{TYP}	MPQ2180-8, T_J = 25°C V_{IN} = 2.7V to 5.5V	0.784	0.800	0.816	V
		MPQ2180-8, V_{IN} = 2.7V to 5.5V, T_J = -40°C to +125°C	0.776	0.800	0.824	V
		MPQ2180-10, T_J = 25°C, V_{IN}=2.7V to 5.5V	0.98	1.00	1.02	V
		MPQ2180-10, V_{IN} = 2.7V to 5.5V, T_J = -40°C to +125°C	0.97	1.00	1.03	V
Lowest output voltage	V_{LOW}	T_J = 25°C, V_{IN} = 2.7V to 5.5V	0.585	0.600	0.615	V
		T_J = -40°C to +125°C, V_{IN} = 2.7V to 5.5V	0.579	0.600	0.621	V
Highest output voltage	V_{HIGH}	T_J = 25°C, V_{IN} = 2.7V to 5.5V	1.198	1.235	1.272	V
		T_J = -40°C to +125°C, V_{IN} = 2.7V to 5.5V	1.192	1.235	1.278	V
Output voltage step	V_{STEP}			5		mV
High-side switch on resistance	R_{HS_ON}			40	80	mΩ
Low-side switch on resistance	R_{LS_ON}			22	45	mΩ
UVLO rising threshold	V_{UVLOR}			2.55	2.8	V
UVLO hysteretic	V_{UVLOHY}			150		mV
Switching frequency	f_{SW}		0.85		2.2	MHz
Frequency variation					25%	f_{SW}
Minimum on time[8]	t_{MINON}			60		ns
High-side switch leakage	I_{SW_H}	V_{EN} = 0V, V_{IN} = 5V, V_{SW} = 0V, T_J = 25°C			1	µA
Low-side switch leakage	I_{SW_L}	V_{EN} = 0V, V_{IN} = 5V, V_{SW} = 5V, T_J = 25°C			10	µA
EN input current	I_{EN}			4		µA
EN logic low voltage	V_{ENH}				0.4	V
EN logic high voltage	V_{ENL}		1.8			V

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, T_J= -40°C to +125°C, typical values refer to T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Power good UV rising threshold	PG_{VTH-HI}	Good		90%		V_{OUT}
Power good UV falling threshold	PG_{VTH-LO}	Fault		85%		V_{OUT}
Power good OV rising threshold	PG_{VTH-HI}	Fault		110%		V_{OUT}
Power good OV falling threshold	PG_{VTH-LO}	Good		105%		V_{OUT}
Power good pull-down voltage	V_{PGL}	I_{SINK} = 1mA			0.4	V
Power good deglitch time	t_{PGD}			50		µs
Power good leakage	I_{PGD}				1	µA
High-side switch peak current limit (source)	I_{PEAK}		9	12.7		A
Low-side switch valley current limit (8)	I_{VALLEY}			7.5		A
Low-side switch current limit (sink)		PFM mode		0		A
		PWM mode (8)		-5		A
Soft-start time	t_{SS-ON}	V_{OUT} rises from 10% to 90%		165		µs
Discharge resistor				500		Ω
Thermal shutdown (8)				170		°C
DAC resolution (8)				7		bits

Note:

8) Not tested in production. Guaranteed by design and characterization.

I/O LEVEL CHARACTERISTICS

V_{IN} = 5V, T_J= -40°C to +125°C, typical values refer to T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	HS Mode		LS Mode		Units
			Min	Max	Min	Max	
Low-level input voltage	V_{IL}		-0.5	0.3 x V_{CC}	-0.5	0.3 x Vcc	V
High-level input voltage	V_{IH}		0.7 x V_{CC}	V_{CC} + 0.5	0.7 x V_{CC}	V_{CC} + 0.5	V
Hysteresis of Schmitt trigger inputs	V_{HYS}	V_{CC} > 2V	0.05 x V_{CC}		0.05 x V_{CC}		V
		V_{CC} < 2V	0.1 x V_{CC}		0.1 x V_{CC}		
Low-level output voltage (open drain) at 3mA sink current	V_{OL}	V_{CC} > 2V	0	0.4	0	0.4	V
		V_{CC} < 2V	0	0.2 x V_{CC}	0	0.2 x V_{CC}	
Low-level output current	I_{OL}			3		3	mA
Transfer gate on resistance for currents between SDA and SCAH, or SCL and SCLH	R_{ONL}	V_{OL} level, I_{OL} = 3mA		50		50	Ω
Transfer gate on resistance between SDA and SCAH, or SCL and SCLH	R_{ONH}	Both signals (SDA and SDAH, or SCL and SCLH) at V_{CC} level	50		50		kΩ
Pull-up current of the SCLH current source	I_{CS}	SCLH output levels between 0.3 x V_{CC} and 0.7 x V_{CC}	2	6	2	6	mA
Rising time of the SCLH or SCL signal	t_{RCL}	Output rising time (current source enabled) with an external pull-up current source of 3mA					
		Capacitive load from 10pF to 100pF	10	40			ns
		Capacitive load of 400pF	20	80			ns
Falling time of the SCLH or SCL signal	t_{FCL}	Output falling time (current source enabled) with an external pull-up current source of 3mA					
		Capacitive load from 10pF to 100pF	10	40			ns
		Capacitive load of 400pF	20	80	20	250	ns
Rising time of the SDAH signal	t_{RDA}	Capacitive load from 10pF to 100pF	10	80			ns
		Capacitive load of 400pF	20	160	20	250	ns
Falling time of the SDAH signal	t_{FDA}	Capacitive load from 10pF to 100pF	10	80			ns
		Capacitive load of 400pF	20	160	20	250	ns

I²C PORT SIGNAL CHARACTERISTICS

V_{IN} = 5V, T_J= -40°C to +125°C, typical values refer to T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	C_B = 100pF		C_B = 400pF		Units
			Min	Max	Min	Max	
Pulse width of spikes that must be suppressed by the input filter	t_{SP}		0	10	0	50	ns
Input current for each I/O pin	I_I	Input voltage between 0.1 x V_{CC} and 0.9 x V_{CC}		10	-10	+10	µA
Capacitance for each I/O pin	C_I			10		10	pF
SCLH and SCL clock frequency	f_{SCHL}		0	3.4	0	0.4	MHz
Set-up time for a repeated start condition	t_{SU_STA}		160		600		ns
Hold time for a repeated start condition	t_{HD_STA}		160		600		ns
Low period of the SCL clock	t_{LOW}		160		1300		ns
High period of the SCL clock	t_{HIGH}		60		600		ns
Data set-up time	t_{SU_DAT}		10		100		ns
Data hold time	t_{HD_DAT}		0	70	0		ns
Rising time of SCLH signal	t_{RCL}		10	40	20 x 0.1 x C_B	300	ns
Rising time of SCLH signal after a repeated start condition and after an acknowledge bit	t_{FCL1}		10	80	20 x 0.1 x C_B	300	ns
Falling time of SCLH signal	t_{FCL}		10	40	20 x 0.1 x C_B	300	ns
Rising time of SDAH signal	t_{RDA}		10	80	20 x 0.1 x C_B	300	ns
Falling time of SDAH signal	t_{FDA}		10	80	20 x 0.1 x C_B	300	ns
Set-up time for a stop condition	t_{SU_STO}		160		600		ns
Bus free time between a stop and start condition	t_{BUF}		160		1300		ns
Data valid time	t_{VD_DAT}			16		90	ns
Data valid acknowledge time	t_{VD_ACK}			160		900	ns
Capacitive load for each bus line	C_B	SDAH and SCLH line		100		400	pF
		SDAH+SDA line and SCLH+SCL line		400		400	pF
Noise margin at the low level (9)	V_{NL}	For each connected device		0.1 x V_{CC}	0.1 x V_{CC}		V
Noise margin at the high level (9)	V_{NH}	For each connected device		0.2 x V_{CC}	0.2 x V_{CC}		V

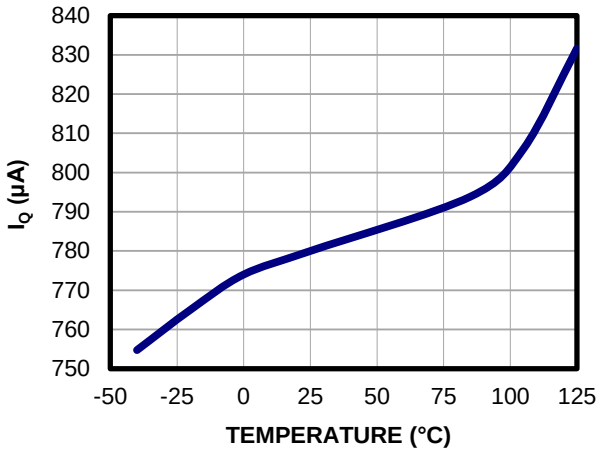
Note:

9) V_{CC} is the I²C bus voltage, which is between 1.5V and 3.3V.

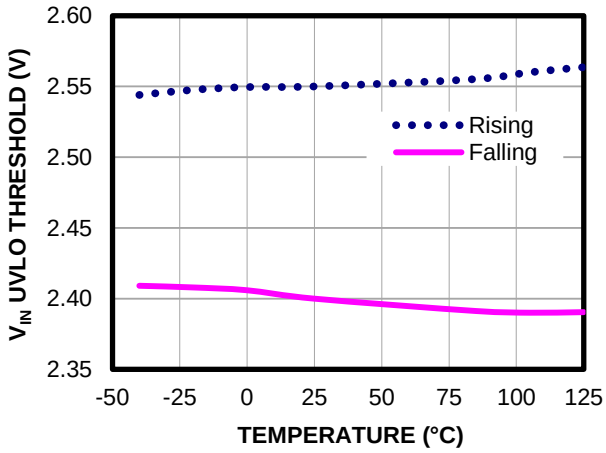
TYPICAL CHARACTERISTICS

V_{IN} = 5V, T_J = -40°C to +125°C, unless otherwise noted.

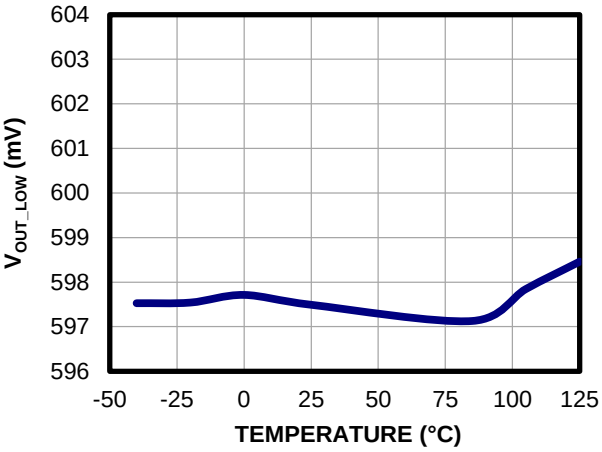
Quiescent Current vs. Temperature
PWM



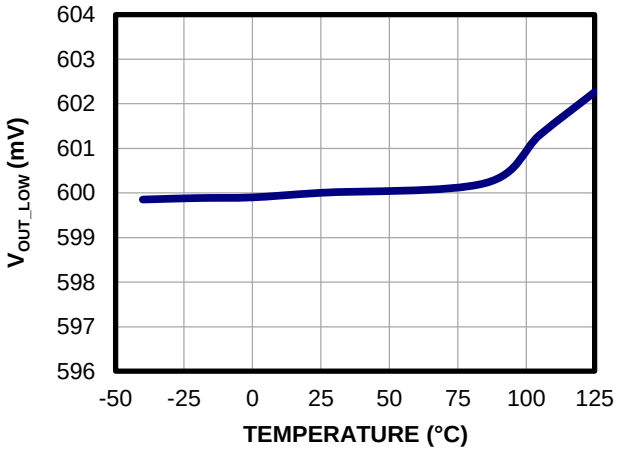
V_{IN} UVLO Threshold vs. Temperature



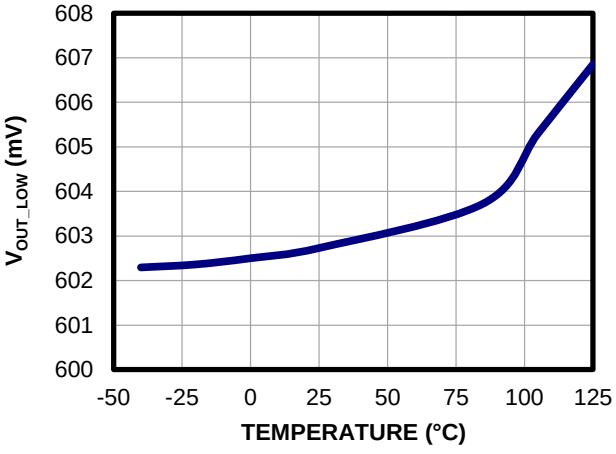
V_{OUT_LOW} vs. Temperature
V_{IN} = 2.7V



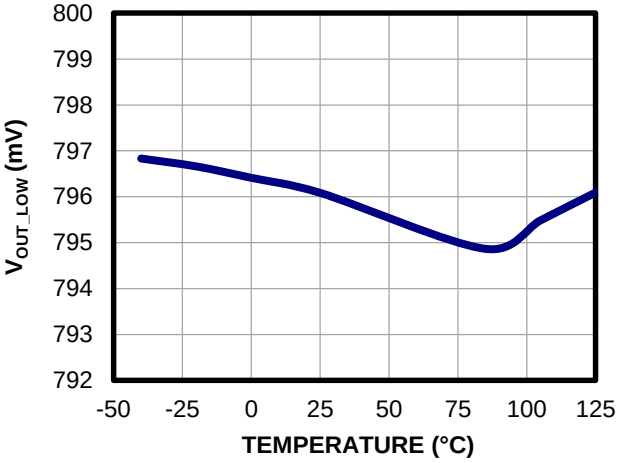
V_{OUT_LOW} vs. Temperature
V_{IN} = 5V



V_{OUT_LOW} vs. Temperature
V_{IN} = 6V



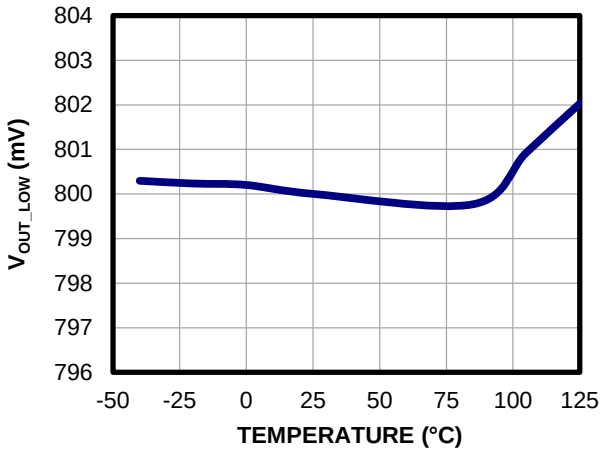
V_{OUT_LOW} vs. Temperature
V_{IN} = 2.7V,V_{OUT} = 0.8V (default)



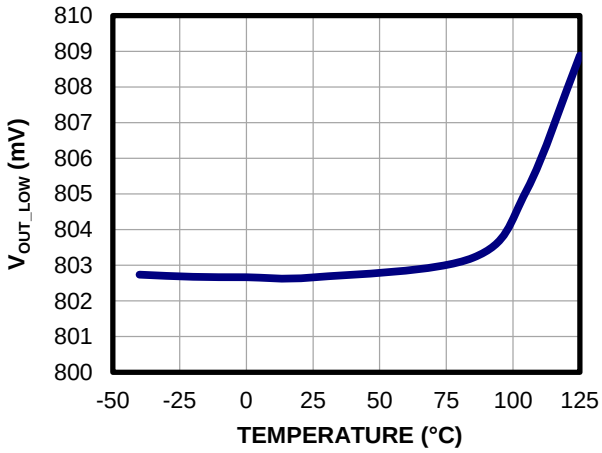
TYPICAL CHARACTERISTICS

V_{IN} = 5V, T_J = -40°C to +125°C, unless otherwise noted.

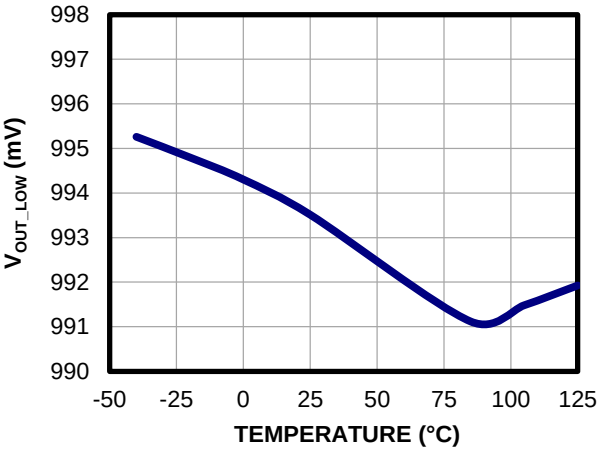
V_{OUT_LOW} vs. Temperature
V_{IN} = 5V,V_{OUT} = 0.8V (default)



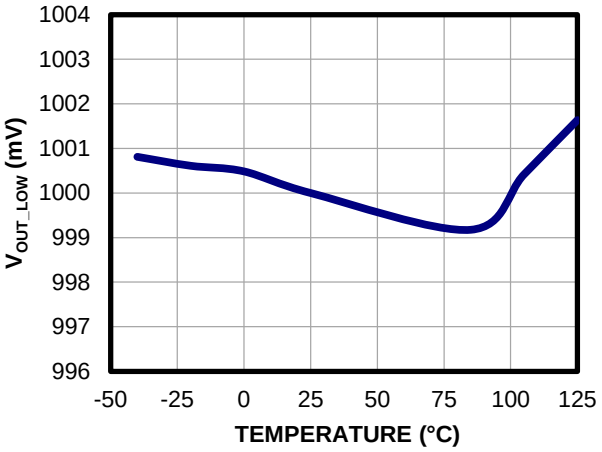
V_{OUT_LOW} vs. Temperature
V_{IN} = 6V,V_{OUT} = 0.8V (default)



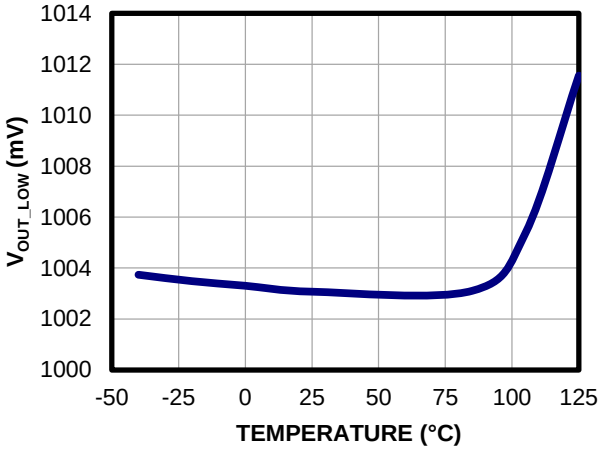
V_{OUT_LOW} vs. Temperature
V_{IN} = 2.7V,V_{OUT} = 1V (default)



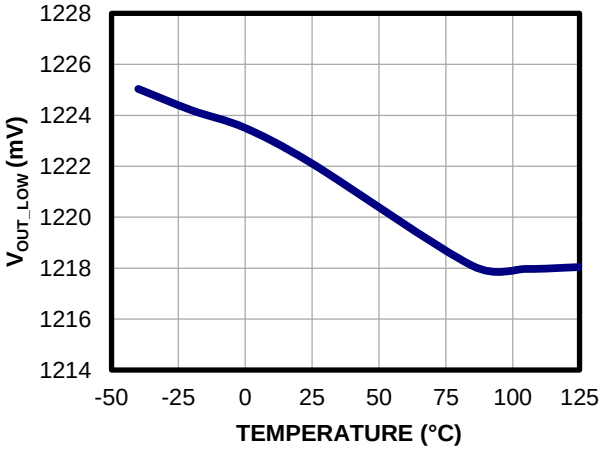
V_{OUT_LOW} vs. Temperature
V_{IN} = 5V,V_{OUT} = 1V (default)



V_{OUT_LOW} vs. Temperature
V_{IN} = 6V,V_{OUT} = 1V



V_{OUT_LOW} vs. Temperature
V_{IN} = 2.7V

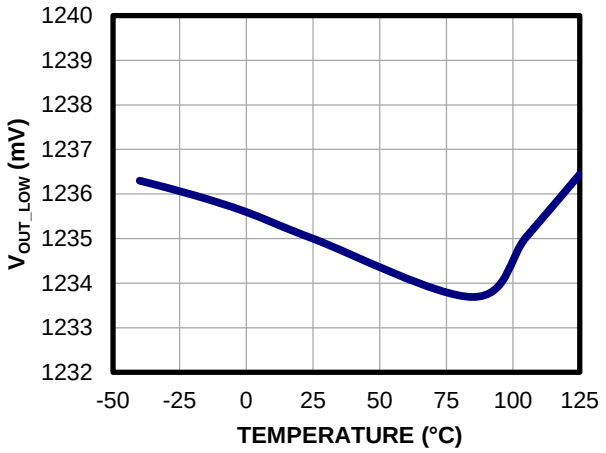


TYPICAL CHARACTERISTICS

V_{IN} = 5V, T_J = -40°C to +125°C, unless otherwise noted.

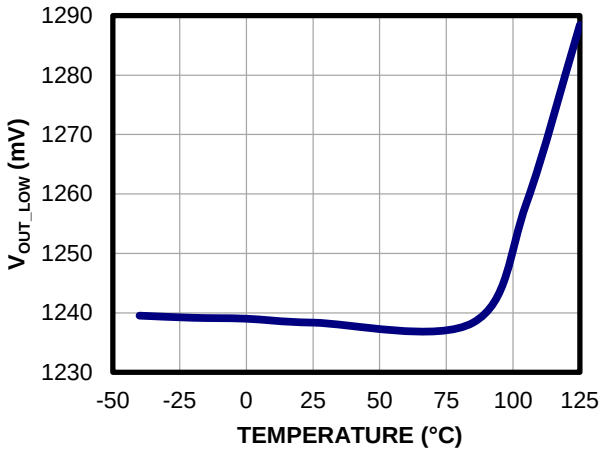
V_{OUT_LOW} vs. Temperature

V_{IN} = 5V

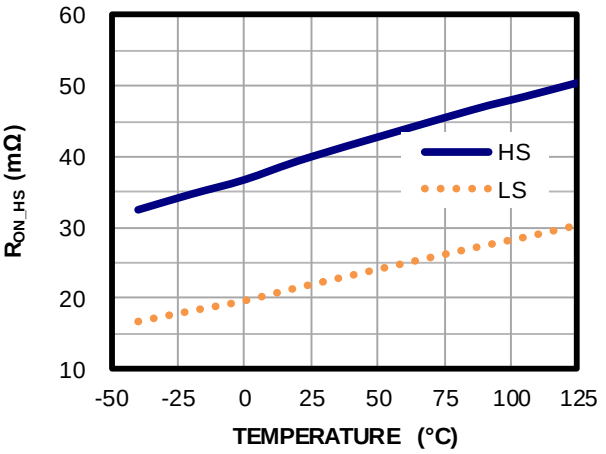


V_{OUT_LOW} vs. Temperature

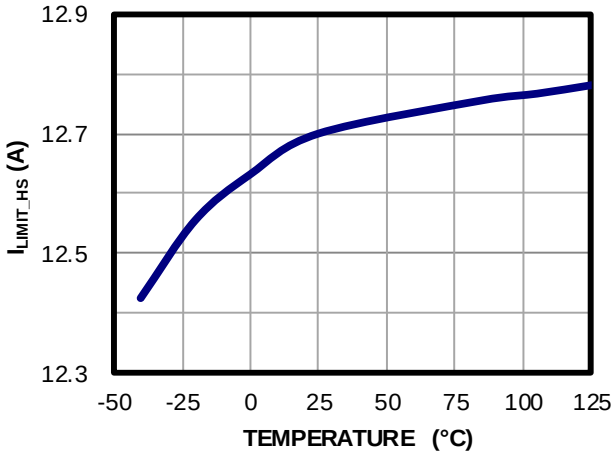
V_{IN} = 6V



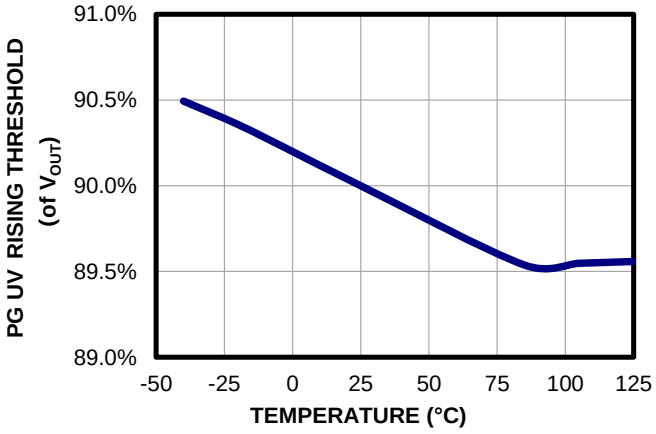
High-Side Switch On Resistance vs. Temperature



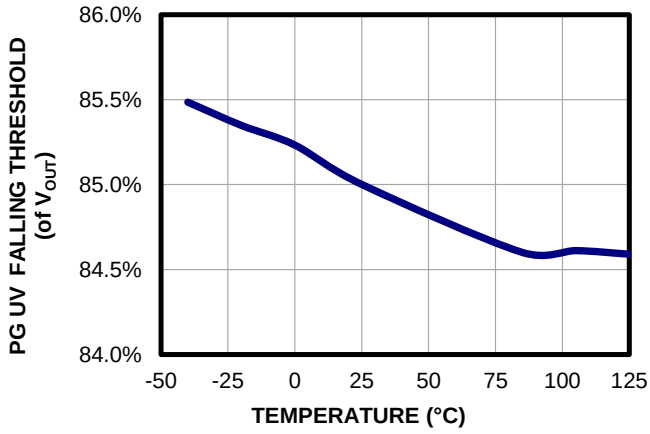
High-Side Current Limit vs. Temperature



PG Under-Voltage Rising Threshold vs. Temperature



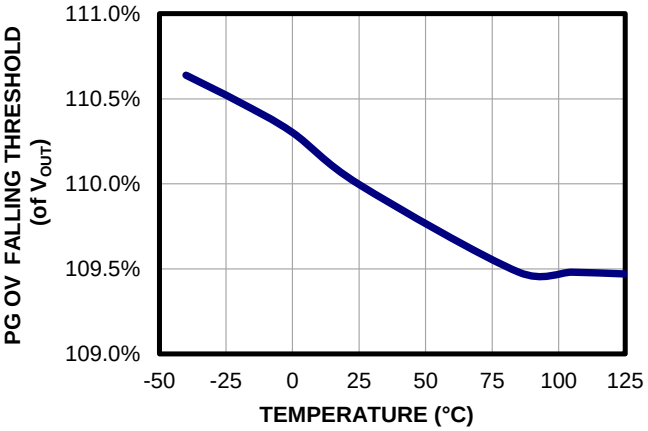
PG Under-Voltage Falling Threshold vs. Temperature



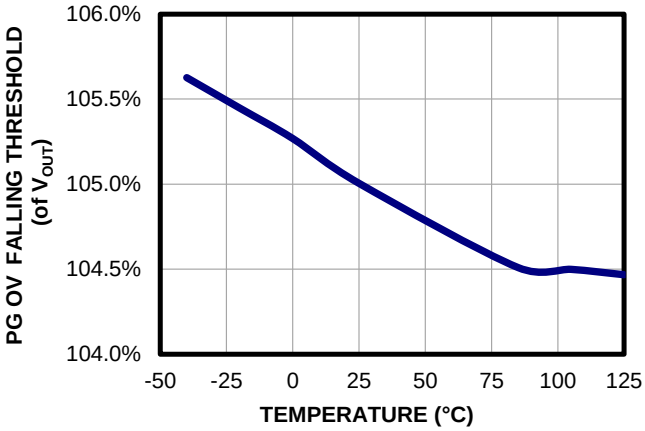
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, T_J = -40°C to +125°C, unless otherwise noted.

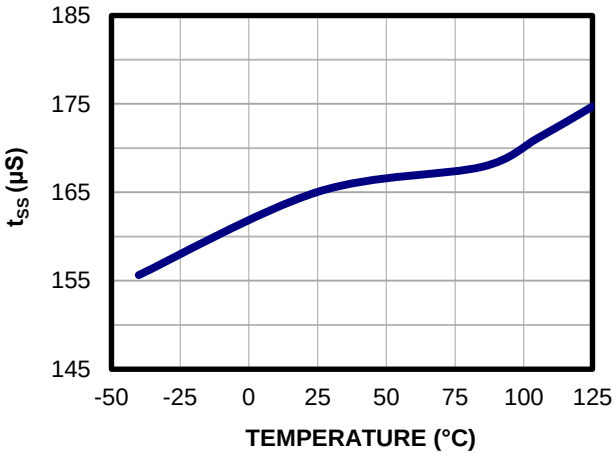
PG Over-Voltage Rising Threshold vs. Temperature



PG Over-Voltage Falling Threshold vs. Temperature



Soft-Start Time vs. Temperature

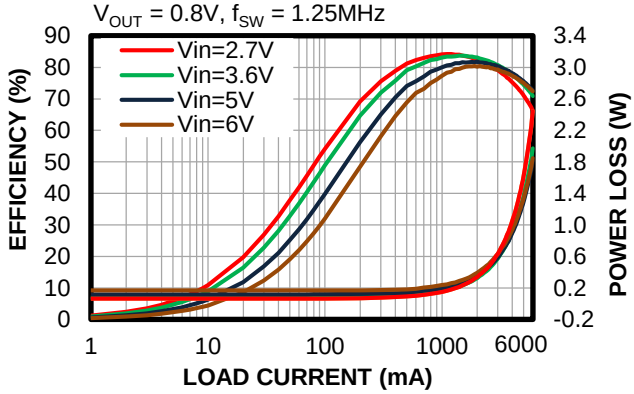


TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 5V, V_{OUT} = 0.8V, L = 0.47µH (DCR = 3.67mΩ), C_{OUT} = 3 x 47µF, FCCM, T_A = 25°C, unless otherwise noted.

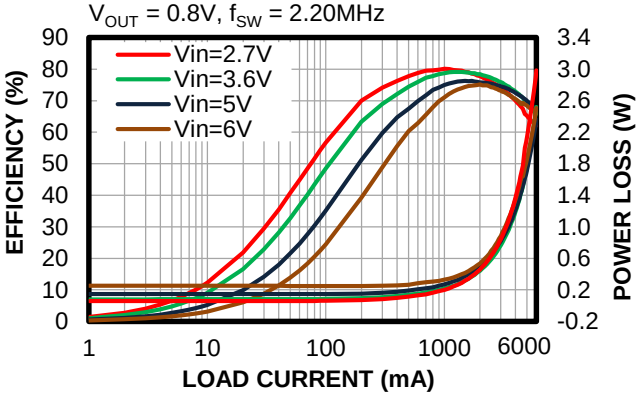
Efficiency vs. Load Current vs. Power Loss

V_{OUT} = 0.8V, f_{SW} = 1.25MHz



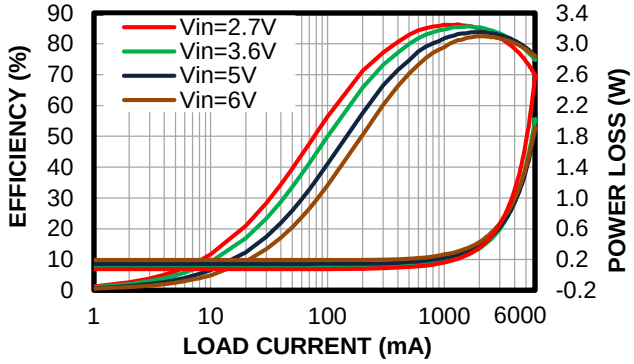
Efficiency vs. Load Current vs. Power Loss

V_{OUT} = 0.8V, f_{SW} = 2.20MHz



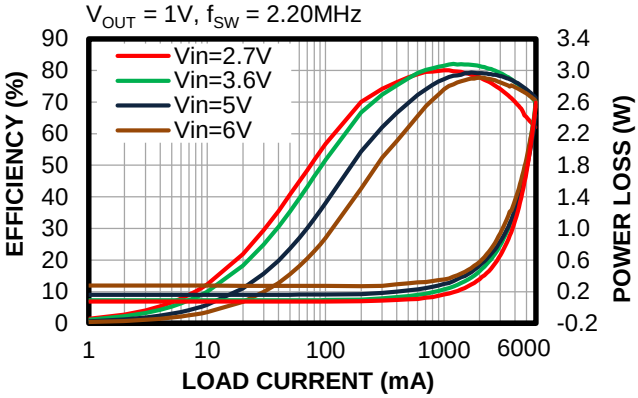
Efficiency vs. Load Current vs. Power Loss

V_{OUT} = 1V, f_{SW} = 1.25MHz



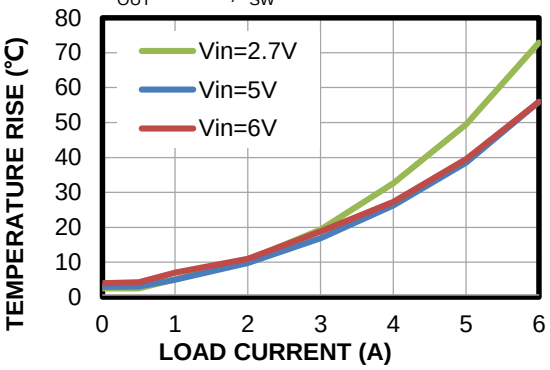
Efficiency vs. Load Current vs. Power Loss

V_{OUT} = 1V, f_{SW} = 2.20MHz



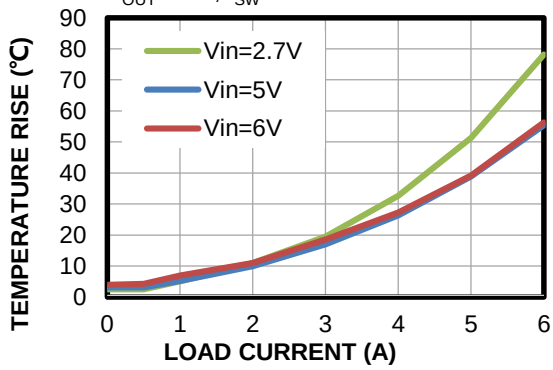
Case Temperature Rise

V_{OUT} = 0.8V, f_{SW} = 1.25MHz



Case Temperature Rise

V_{OUT} = 1V, f_{SW} = 1.25MHz

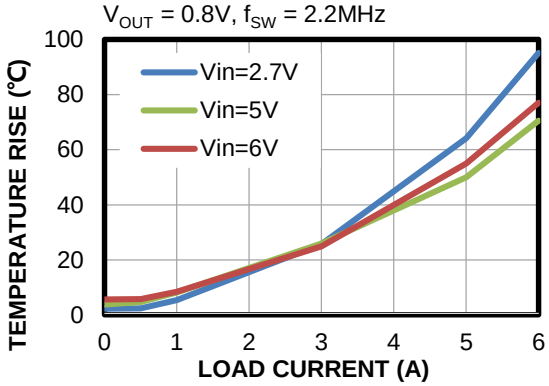


TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 5V, V_{OUT} = 0.8V, L = 0.47µH (DCR = 3.67mΩ), C_{OUT} = 3 x 47µF, FCCM, T_A = 25°C, unless otherwise noted.

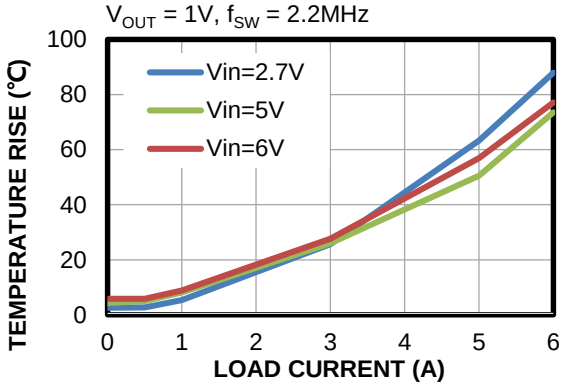
Case Temperature Rise

V_{OUT} = 0.8V, f_{SW} = 2.2MHz



Case Temperature Rise

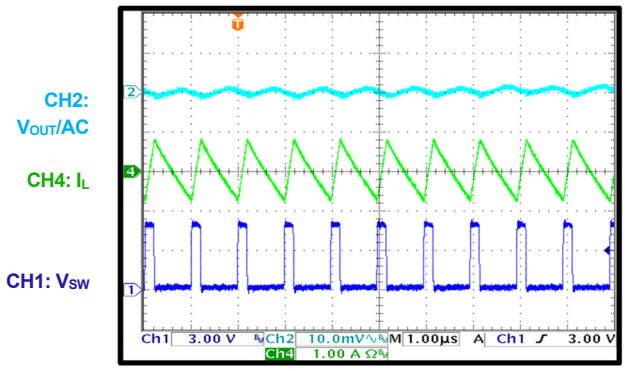
V_{OUT} = 1V, f_{SW} = 2.2MHz



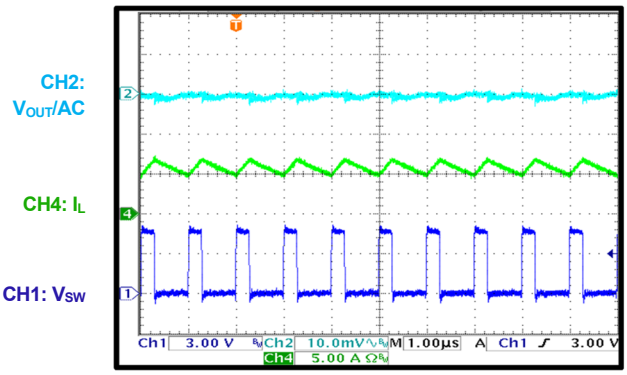
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 0.8V, L = 0.47µH, C_{OUT} = 3 x 47µF, FCCM, T_A = 25°C, unless otherwise noted.

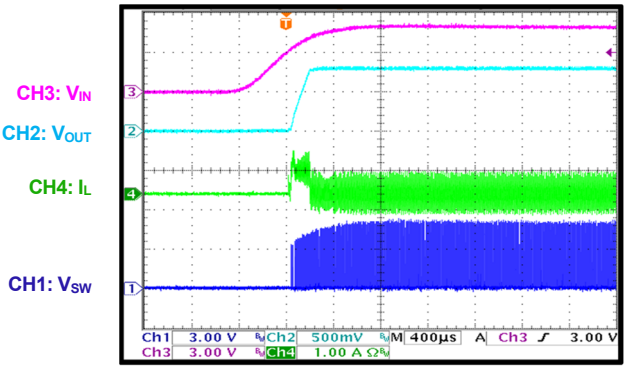
Output Voltage Ripple
I_{OUT} = 0A



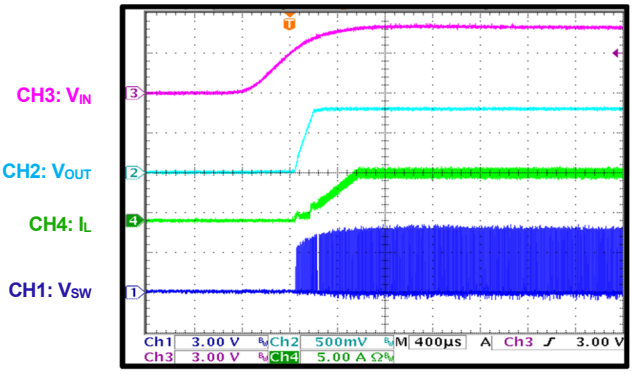
Output Voltage Ripple
I_{OUT} = 6A



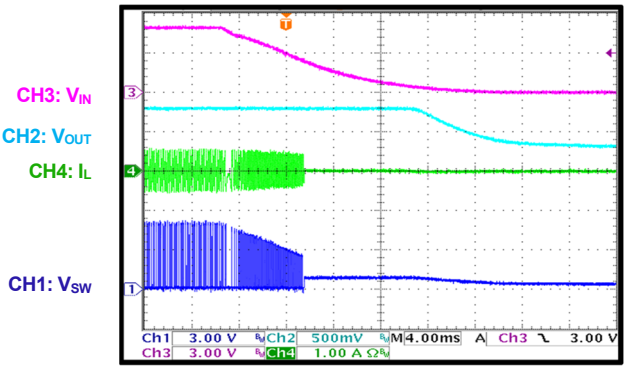
Start-Up through VIN
I_{OUT} = 0A



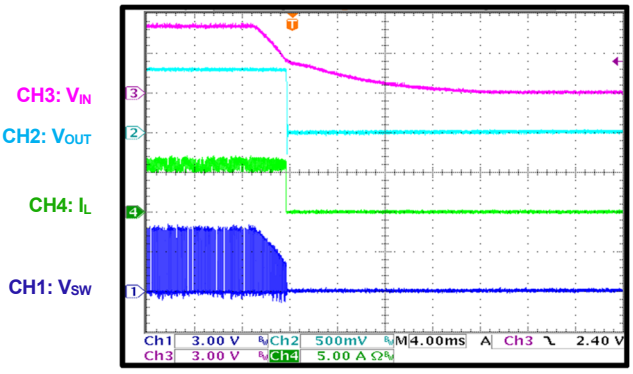
Start-Up through VIN
I_{OUT} = 6A



Shutdown through VIN
I_{OUT} = 0A



Shutdown through VIN
I_{OUT} = 6A

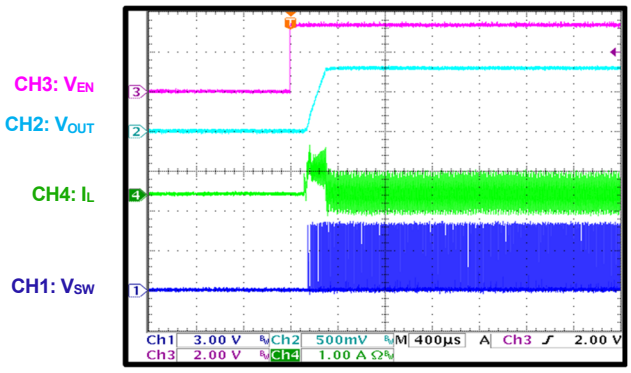


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 0.8V, L = 0.47µH, C_{OUT} = 3 x 47µF, FCCM, T_A = 25°C, unless otherwise noted.

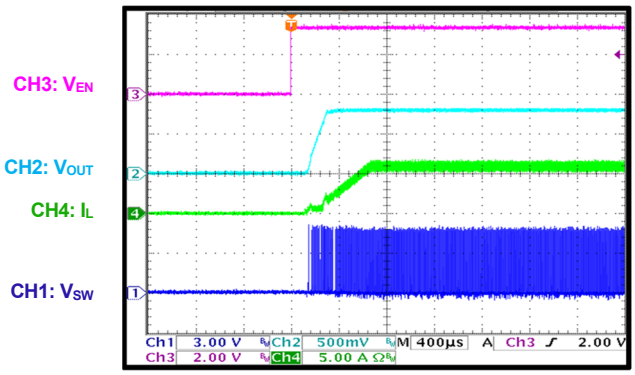
Start-Up through EN

I_{OUT} = 0A



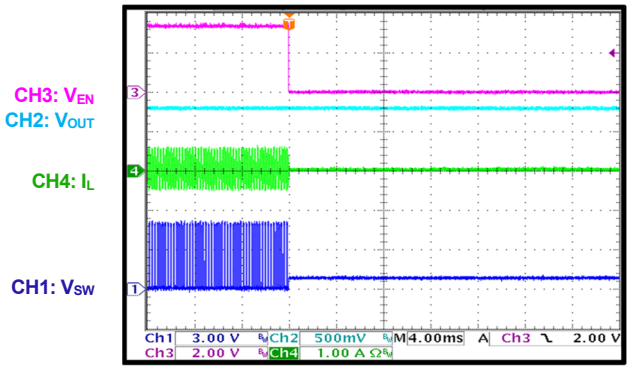
Start-Up through EN

I_{OUT} = 6A



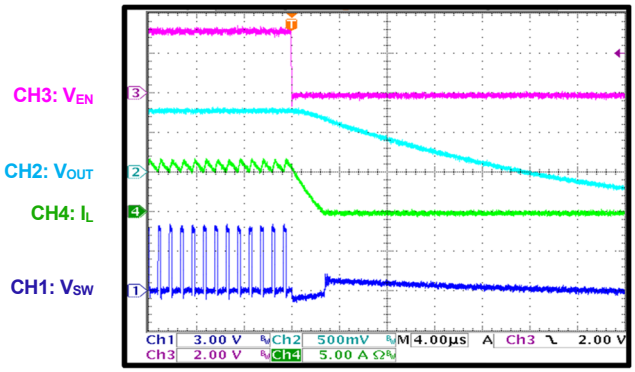
Shutdown through EN

I_{OUT} = 0A



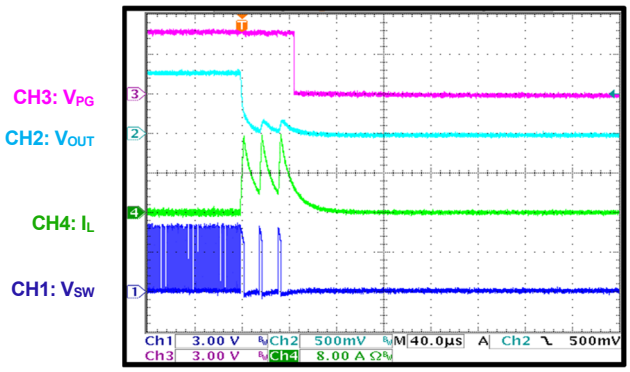
Shutdown through EN

I_{OUT} = 6A



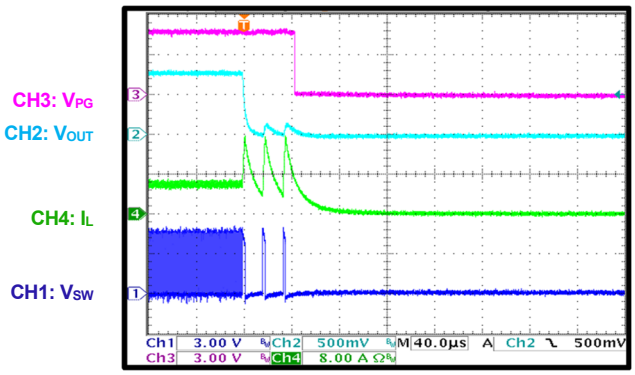
SCP Entry

I_{OUT} = 0A short to GND



SCP Entry

I_{OUT} = 6A short to GND

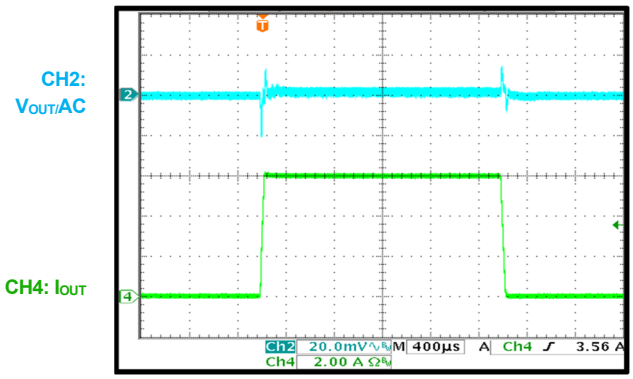


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 0.8V, L = 0.47µH, C_{OUT} = 3 x 47µF, FCCM, T_A = 25°C, unless otherwise noted.

Load Transient Response

I_O = 0A to 6A, 0.1A/µs



FUNCTIONAL BLOCK DIAGRAM

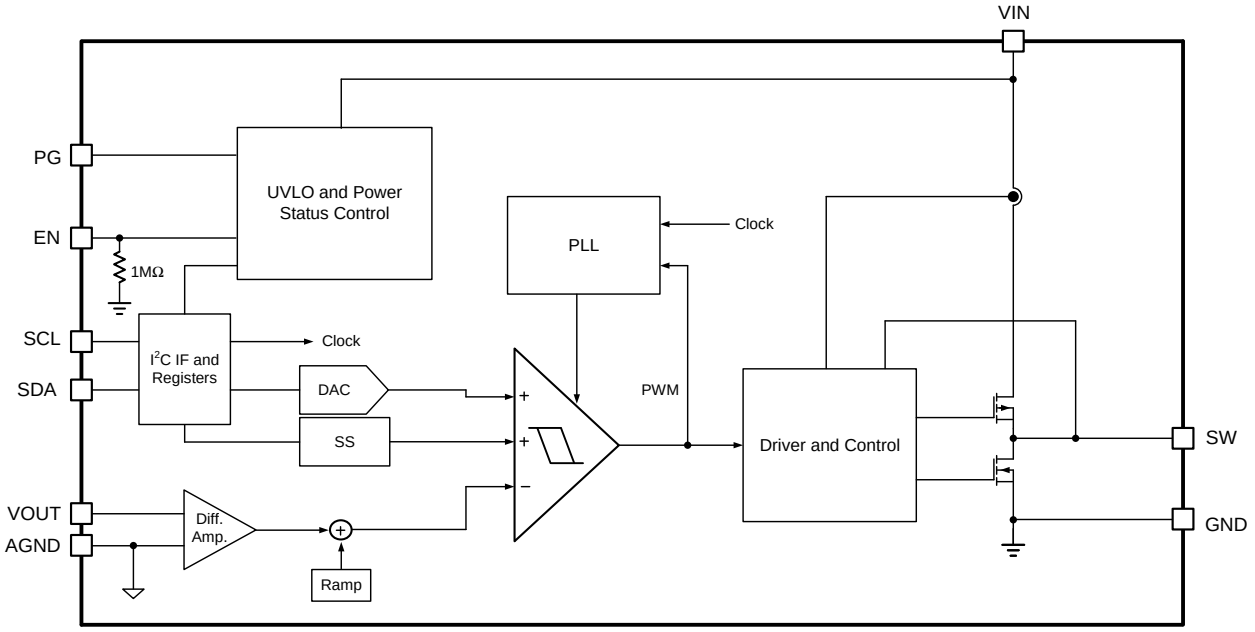


Figure 1: Functional Block Diagram

OPERATION

The MPQ2180 is a low-voltage, 6A, synchronous step-down converter with an I²C interface. The MPQ2180 applies MPS's patented constant-frequency hysteretic control to utilize fast transient response during hysteretic control and keep the switching frequency (f_{SW}) constant. No compensation is required, which simplifies the design procedure.

The MPQ2180 integrates an I²C-compatible interface that allows transfers up to 3.4Mbps. This communication interface can be used for dynamic voltage scaling with voltage steps down to 5mV, and an output voltage (V_{OUT}) ranging between 0.6V and 1.235V. The voltage transition slew rate can also be configured.

Light-Load Operation

Under light-load conditions, the MPQ2180 has selectable forced continuous conduction mode (FCCM) and automatic pulse-frequency modulation (PFM) mode via the I²C. In FCCM, MPQ2180 switching operates with a fixed frequency, regardless of the output load current. In PFM, the MPQ2180 uses a proprietary control scheme to save power and improve efficiency. The MPQ2180 turns off the low-side MOSFET (LS-FET) when the inductor current (I_L) begins reversing. The MPQ2180 then works in discontinuous conduction mode (DCM).

Enable (EN)

When the input voltage (V_{IN}) exceeds the under-voltage lockout (UVLO) threshold (typically 2.55V), the MPQ2180 can be enabled by pulling EN above 1.8V. Pull EN below 0.4V to disable the MPQ2180. The IC can also be disabled by floating EN. There is an internal 1MΩ resistor connected from EN to ground.

Soft Start (SS)

The MPQ2180 has built-in soft start (SS) that ramps up V_{OUT} at a controlled slew rate to prevent inrush current and V_{OUT} overshoot at start-up. The soft-start time (t_{SS}) is about 165µs.

Power Good (PG) Indictor

The MPQ2180 has an open-drain output for power good (PG) indication. Connect the PG pin to VIN or another voltage source through a resistor (e.g. 100kΩ). When V_{OUT} is within 90% to 110% of the regulation voltage, PG is pulled high by the external resistor.

Current Limit

Generally, the MPQ2180 has a 12.7A current limit for the high-side MOSFET (HS-FET). When the HS-FET reaches the current limit, the MPQ2180 extends the minimum off time until the current drops to 7.5A. Then the HS-FET turns on for the next switching cycle. This prevents I_L from becoming exceedingly high and damaging the components.

If the peak current limit is continuously reached several times (typically 3 to 5 times), the MPQ2180 shuts down. A new start-up cycle is required to turn on the MPQ2180 again.

Thermal Protection

The MPQ2180 employs thermal shutdown by monitoring the IC's internal junction temperature. The MPQ2180 shuts down if the junction temperature exceeds the thermal shutdown threshold (typically 170°C). After thermal shutdown, a new start-up cycle is required to turn on the MPQ2180 again.

Start-Up and Shutdown

If both V_{IN} and EN exceed their appropriate thresholds, the chip starts. The reference block starts first, generating a stable reference voltage and currents, then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuitries. When the internal supply rail is up, the internal circuits begin working. When the soft-start block is enabled, V_{OUT} starts to ramp up slowly and smoothly to its set target within 165µs.

The following events shut down the chip: EN going low, V_{IN} falling below its UVLO threshold, thermal shutdown, and writing the I²C register REG01, bit D[7] to 0. During the shutdown procedure, the signaling path is blocked first to avoid any fault triggering.

I²C INTERFACE

The MPQ2180 can communicate with the core and the I²C for smart design. MPS provides a GUI and evaluation kit to configure the MPQ2180 during development. To make

configurations in application, contact an MPS FAE.

I²C Address

The MPQ2180 has an internal I²C slave address, which is 0x60 (see Table 1). Contact an MPS FAE if a different address is required.

When the master sends the address as an 8-bit value, the 7-bit address should be followed by a 0 to indicate a write, or a 1 to indicate a read. For example, 0xC0 is a write operation, while 0xC1 is a read operation.

Table 1: I²C Slave Address

Hex	A7	A6	A5	A4	A3	A2	A1	A0
W 0xC0 R 0xC1	1	1	0	0	0	0	0	R/W
Address	0x60							

I²C Enable

The MPQ2180's EN pin can force the converter to start up or shut down. The EN command (REG01 VSEL, bit D[7]) in the I²C can also control the converter. If bit D[7] = 0, the converter is off. If bit D[7] = 1, the converter is on. Both the external EN and internal I²C EN can control the converter. The converter works only when both EN signals are high.

Output Voltage Selection

The output voltage (V_{OUT}) can be configured via the I²C. V_{OUT} cannot be changed with a traditional resistor divider because the internal circuit of the VOUT pin effects the voltage feedback loop.

The default V_{OUT} is 0.8V for the MPQ2180-8 and 1V for the MPQ2180-10, but this value can be set between 0.6V and 1.235V, with 5mV steps, via the I²C. To change V_{OUT}, set the GO bit (REG03 SYSCNTLREG2, bit [D5]) to 1. This allows V_{OUT} to be set to a value besides the default. Then set the OUTPUT_REFENCE bits (REG01 VSEL, bits D[6:0]). Table 3 on page 23 shows the possible values for V_{OUT}.

Switching Frequency

The default switching frequency (f_{SW}) is 1.25MHz, but this value can be changed based on the application. By setting the SWITCHING_FREQUENCY bits (REG02 SYSCNTLREG1, bits D[7:5]), f_{SW} can be configured to be 0.85MHz, 1.11MHz, 1.25MHz, 1.67MHz, 2MHz, or 2.2MHz.

Power Good (PG) Configuration

The MPQ2180 can be set to use the PG_LOHI function. This function can be set by the PG_LOHI bit (REG02 SYSCNTLREG1, bit D[2]). The default value is 1, where PG senses both a positive and negative excursion of V_{OUT} from the reference. If this bit is set to 0, PG only senses a negative voltage excursion of V_{OUT} from the reference.

Input Over-Voltage Protection (OVP)

The MPQ2180 has an option to enable V_{IN} over-voltage protection (OVP). This function can be set by the VIN_OVP bit (REG02 SYSCNTLREG1, bit D[1]). The default value is 0, which enables V_{IN} OVP. When V_{IN} exceeds 6.3V, the converter is disabled. After V_{IN} falls to 6.2V, the converter restarts. If VIN_OVP is set to 1, V_{IN} OVP is disabled. In this scenario, the converter continues operating, even if V_{IN} exceeds its safe range.

Forced Continuous Conduction Mode (FCCM)

The MPQ2180 has automatic pulse-frequency modulation (PFM) mode and forced continuous conduction mode (FCCM). This function can be written in the MODE bit (REG02 SYSCNTLREG1, bit D[0]). The default value is 1, where FCCM is selected.

Output Voltage Discharge

The MPQ2180 has a V_{OUT} discharge function. Writing the OUT-DIS bit (REG03 SYSCNTLREG2, bit D[4]) can change the output discharge mode. The default value is 0, which means V_{OUT} is discharged by its load when EN is low. Set this bit to 1 to enable V_{OUT} to be discharged by the internal pull-down resistance.

Output Voltage Transition Slew Rate

When V_{OUT} switches from low to high or from high to low, there may be different transition slew rates. There are two possible values to select through the SLEW_RATE bit (REG03 SYSCNTLREG2, bit D[2]). The slew rate should be set based on the application. The internal reference follows the set slew rate, but the V_{OUT} slew rate does not always follow the internal reference. Considering the output capacitor and

inductor, the actual V_{OUT} slew rate should be a slower than the set slew rate.

Fault Indicator and Diagnostics

The MPQ2180 provides diagnostics for different fault conditions. For example, the PG pin is pulled high during normal operation, and any fault or warning pulls PG low to indicate a fault status (see Table 2).

The MPQ2180 also has dedicated register bits that serve as fault flags and device status indicators for system diagnostics.

Table 2: Operation Status

Condition	PG	Regulation	Latch-Off	Status Bit
V_{IN} over-voltage	Low	Off	No	OVP
V_{IN} under-voltage	Low	Off	-	UVLO
Thermal shutdown	Low	Off	Yes	-
Short circuit protection	Low	Off	Yes	ILIM
Output under-voltage	Low	Off	Yes	VOUV
Output over-voltage (>108% of target output)	Low	On	No	VOOV

Table 3: Output Voltage Chart

D[6:0]	V_{OUT}	D[6:0]	V_{OUT}	D[6:0]	V_{OUT}	D[6:0]	V_{OUT}
000 0000	0.600	010 0000	0.760	100 0000	0.920	110 0000	1.080
000 0001	0.605	010 0001	0.765	100 0001	0.925	110 0001	1.085
000 0010	0.610	010 0010	0.770	100 0010	0.930	110 0010	1.090
000 0011	0.615	010 0011	0.775	100 0011	0.935	110 0011	1.095
000 0100	0.620	010 0100	0.780	100 0100	0.940	110 0100	1.100
000 0101	0.625	010 0101	0.785	100 0101	0.945	110 0101	1.105
000 0110	0.630	010 0110	0.790	100 0110	0.950	110 0110	1.110
000 0111	0.635	010 0111	0.795	100 0111	0.955	110 0111	1.115
000 1000	0.640	010 1000	0.800	100 1000	0.960	110 1000	1.120
000 1001	0.645	010 1001	0.805	100 1001	0.965	110 1001	1.125
000 1010	0.650	010 1010	0.810	100 1010	0.970	110 1010	1.130
000 1011	0.655	010 1011	0.815	100 1011	0.975	110 1011	1.135
000 1100	0.660	010 1100	0.820	100 1100	0.980	110 1100	1.140
000 1101	0.665	010 1101	0.825	100 1101	0.985	110 1101	1.145
000 1110	0.670	010 1110	0.830	100 1110	0.990	110 1110	1.150
000 1111	0.675	010 1111	0.835	100 1111	0.995	110 1111	1.155
001 0000	0.680	011 0000	0.840	101 0000	1.000	111 0000	1.160
001 0001	0.685	011 0001	0.845	101 0001	1.005	111 0001	1.165
001 0010	0.690	011 0010	0.850	101 0010	1.010	111 0010	1.170
001 0011	0.695	011 0011	0.855	101 0011	1.015	111 0011	1.175
001 0100	0.700	011 0100	0.860	101 0100	1.020	111 0100	1.180
001 0101	0.705	011 0101	0.865	101 0101	1.025	111 0101	1.185
001 0110	0.710	011 0110	0.870	101 0110	1.030	111 0110	1.190
001 0111	0.715	011 0111	0.875	101 0111	1.035	111 0111	1.195
001 1000	0.720	011 1000	0.880	101 1000	1.040	111 1000	1.200
001 1001	0.725	011 1001	0.885	101 1001	1.045	111 1001	1.205
001 1010	0.730	011 1010	0.890	101 1010	1.050	111 1010	1.210
001 1011	0.735	011 1011	0.895	101 1011	1.055	111 1011	1.215
001 1100	0.740	011 1100	0.900	101 1100	1.060	111 1100	1.220
001 1101	0.745	011 1101	0.905	101 1101	1.065	111 1101	1.225
001 1110	0.750	011 1110	0.910	101 1110	1.070	111 1110	1.230
001 1111	0.755	011 1111	0.915	101 1111	1.075	111 1111	1.235

REGISTERS MAP AND DESCRIPTION

REGISTER MAP

Add	Name	R/W	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
00	STATUS	R	ILIM	UVLO	OVP	VOOV	VOUV	PGOOD	RESERVED	EN_STAT
01	VSEL	R/W	EN	OUTPUT_REFERENCE						
02	SYSCNTLREG1	R/W	SWITCHING_FREQUENCY			TRANSIENT_RESPONSE		PGLOHI	VINOVP	MODE
03 (10)	SYSCNTLREG2	R/W	RESERVED		GO	OUT-DIS	RESERVED	SLEW_RATE	RESERVED	RESERVED
04	ID1	R	VENDOR_ID				DIE_ID			
05	ID2	R	RESERVED				DIE_REV			

Note:

10) The burst write cannot be on REG03.

DEFAULT REGISTER VALUES (MPQ2180-8)

Add	Name	R/W	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
00	STATUS	R	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
01	VSEL	R/W	1	0	1	0	1	0	0	0
02	SYSCNTLREG1	R/W	1	0	0	0	1	1	0	1
03	SYSCNTLREG2	R/W	0	0	0	0	0	0	0	1
04	ID1	R	0	0	0	0	0	0	0	1
05	ID2	R	0	0	0	1	0	0	0	1

DEFAULT REGISTER VALUES (MPQ2180-10)

Add	Name	R/W	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
00	STATUS	R	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
01	VSEL	R/W	1	1	0	1	0	0	0	0
02	SYSCNTLREG1	R/W	1	0	0	0	1	1	0	1
03	SYSCNTLREG2	R/W	0	0	0	0	0	0	0	1
04	ID1	R	0	0	0	0	0	0	0	1
05	ID2	R	0	0	0	1	0	0	0	1

REGISTER DESCRIPTION

REG00: Status

Bits	Bit Name	Description
D[7]	ILIM	When this bit is high, the IC has reached its current limit.
D[6]	UVLO	When this bit is high, V_{IN} is below the under-voltage lockout (UVLO) threshold.
D[5]	OVP	When this bit is high, V_{IN} exceeds the over-voltage protection (OVP) threshold.
D[4]	VOOV	When this bit is high, V_{OUT} exceeds 110% of the regulation voltage.
D[3]	VOUV	When this bit is high, V_{OUT} is below 90% of the regulation voltage.
D[2]	PGOOD	When this bit is high, V_{OUT} is in regulation; otherwise, V_{OUT} is out of regulation.
D[1]	RESERVED	Reserved.
D[0]	EN_STAT	When this bit is high, Smart_MPS is enabled; when the bit is low, Smart_MPS is disabled.

REG01: VSEL

Bits	Bit Name	Description
D[7]	EN	Enables the converter. 0: The converter is off 1: The EN bit takes control, and the part turns on when the EN pin is also high

D[6:0]	OUTPUT_ REFERENCE	Sets the output voltage (V_{OUT}) between 0.6V and 1.235V (see Table 3 on page 23).

REG02: SYSCNTLREG1

Bits	Bit Name	Description
D[7:5]	SWITCHING_ FREQUENCY	Sets the switching frequency (f_{SW}). The default value is 100. 000: 2.2MHz 001: 2MHz 010: 1.67MHz 011: Not used 100: 1.25MHz 101: 1.11MHz 110: 0.85MHz 111: Not used
D[4:3]	TRANSIENT_ RESPONSE	Sets the transient response speed. The default value is 01. 00: Ultra-fast response speed 01: Fast response speed 10: Normal response speed 11: Slow response speed
D[2]	PG_LOHI	0: PG only senses a negative voltage excursion of V_{OUT} from the reference 1: PG senses the positive and negative voltage excursion of V_{OUT} from the reference
D[1]	VIN_OVP	0: Enables V_{IN} over-voltage protection (OVP) (default). The converter turns off when V_{IN} reaches V_{IN_MAX} 1: Disables V_{IN} OVP
D[0]	MODE	0: Enables PFM mode 1: Disables PFM mode (default)

REG03: SYSCNTLREG2

Bits	Bit Name	Description
D[7:6]	RESERVED	Reserved.
D[5]	GO	Write to this bit to start a V_{OUT} transition, regardless of its initial value.
D[4]	OUTPUT_ DISCHARGE	0: Disables V_{OUT} discharge. V_{OUT} must be discharged by the load 1: Enables V_{OUT} discharge. V_{OUT} is discharged by the internal pull-down resistance
D[3]	RESERVED	Reserved.
D[2]	SLEW_RATE	0: The slew rate is 32mV/μs 1: The slew rate is 8mV/μs
D[1:0]	RESERVED	Reserved.

REG04: ID1

Bits	Bit Name	Description
D[7:4]	VENDOR_ID	Returns the vendor ID.
D[3:0]	DIE_ID	Returns the IC type.

REG05: ID2

Bits	Bit Name	Description
D[7:4]	RESERVED	Reserved.
D[3:0]	DIE_REV	Returns the die revision.

APPLICATION INFORMATION

Selecting the Inductor

An inductor must supply a constant current to the output load while being driven by the switching input voltage. A larger-value inductor results in less ripple current and a lower output voltage ripple. However, larger-value inductors are physically larger, have a higher series resistance, and a lower saturation current.

A good rule to determine the inductance is to allow the inductor's peak-to-peak ripple current to be approximately 30% of the maximum switch current limit. Ensure that the peak inductor current is below the maximum switch current limit. The inductance value can be calculated with Equation (1):

$$L1=\frac{V_{OUT}}{f_{SW}\times\Delta I_L}\times(1-\frac{V_{OUT}}{V_{IN}}) \quad (1)$$

Where V_{OUT} is the output voltage, V_{IN} is the input voltage, f_{SW} is the switching frequency, and ΔI_L is the peak-to-peak inductor ripple current.

Choose an inductor that does not saturate under the maximum inductor peak current. The peak inductor current can be estimated with Equation (2):

$$I_{LP}=I_{LOAD}+\frac{V_{OUT}}{2\times f_{SW}\times L1}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right) \quad (2)$$

Where I_{LOAD} is the load current.

Selecting the Input Capacitor

The step-down converter's input current is discontinuous, and a capacitor is required to supply the AC current to the converter while maintaining the DC input voltage. Use low-ESR capacitors for the best performance. Ceramic capacitors are recommended, but tantalum or low-ESR electrolytic capacitors are sufficient.

For simplification, choose an input capacitor with a RMS current rating greater than half of the maximum load current. The input capacitor (C_{IN}) can be electrolytic, tantalum, or ceramic.

When using electrolytic or tantalum capacitors, a small, high-quality ceramic capacitor (i.e. 0.1μF) should be placed as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide sufficient charge in order to prevent an excessive input voltage ripple The input voltage ripple caused by capacitance can be calculated with Equation (3):

$$\Delta V_{IN}=\frac{I_{LOAD}}{f_{SW}\times C_{IN}}\times\frac{V_{OUT}}{V_{IN}}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right) \quad (3)$$

Selecting the Output Capacitor

An output capacitor (C_{OUT}) is required to maintain the DC output voltage. Ceramic, tantalum, or low-ESR electrolytic capacitors are recommended. Low-ESR capacitors keep the output voltage ripple low. The output voltage ripple can be estimated with Equation (4):

$$\Delta V_{OUT}=\frac{V_{OUT}}{f_{SW}\times L}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right)\times\left(R_{ESR}+\frac{1}{8\times f_{SW}\times C_{OUT}}\right) \quad (4)$$

Where L is the inductor value, and R_{ESR} is the equivalent series resistance (ESR) value of C_{OUT}

When using ceramic capacitors, the capacitance dominates the impedance at the switching frequency and causes the majority of the output voltage ripple. For simplification, the output voltage ripple can be calculated with Equation (5):

$$\Delta V_{OUT}=\frac{V_{OUT}}{8\times f_{SW}^{2}\times L\times C_{OUT}}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right) \quad (5)$$

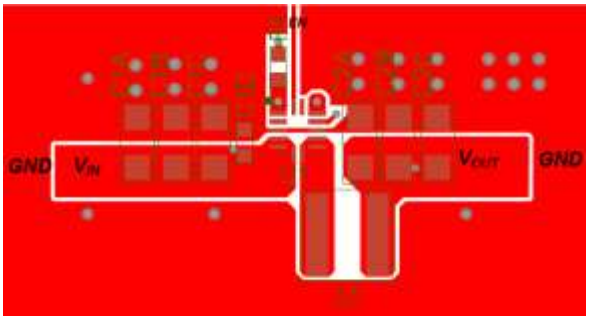
When using tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be estimated with Equation (6):

$$\Delta V_{OUT}=\frac{V_{OUT}}{f_{SW}\times L}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right)\times R_{ESR} \quad (6)$$

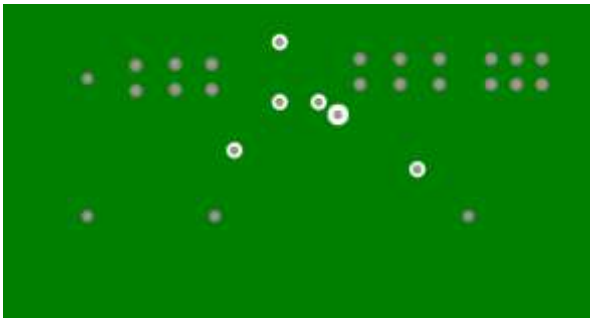
PCB Layout Guidelines (11)

Efficient PCB layout is critical for stable operation. For the best results, refer to Figure 2 and follow the guidelines below:

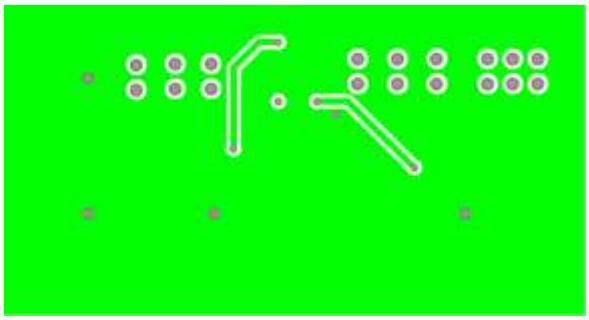
1. Keep the switching current path short.
2. Minimize the loop area formed by the input capacitor, high-side MOSFET, and low-side MOSFET.
3. Place the input capacitor as close to VIN as possible.
4. Ensure that all feedback connections are short and direct.
5. Make the trace between VOUT and the output capacitor as short as possible.
6. Route SW away from sensitive analog areas, such as the output.
7. Connect IN, SW, and GND to large copper areas to cool the chip, and improve thermal performance and long-term reliability.



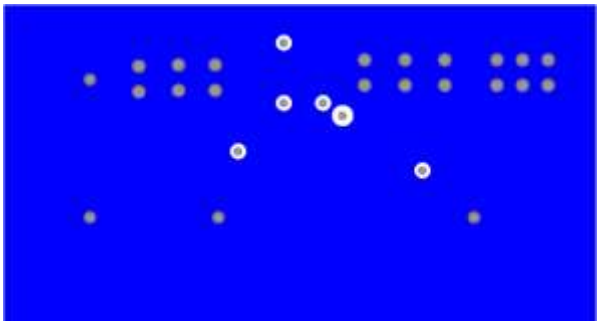
Top Layer



Mid-Layer 1



Mid-Layer 2



Bottom Layer

Figure 2: Recommended PCB Layout

Note:

11) The recommended PCB layout is based on Figure 3 on page 28.

TYPICAL APPLICATION CIRCUIT

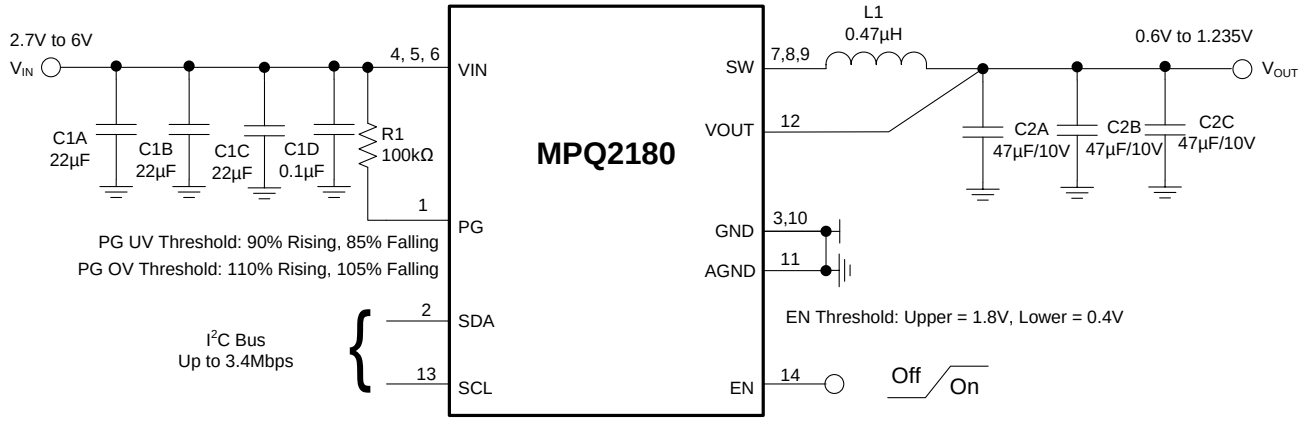
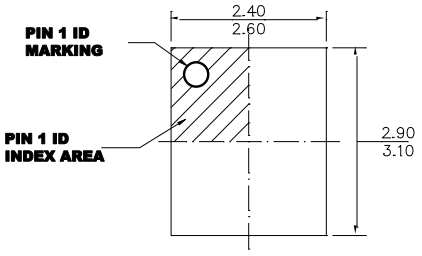


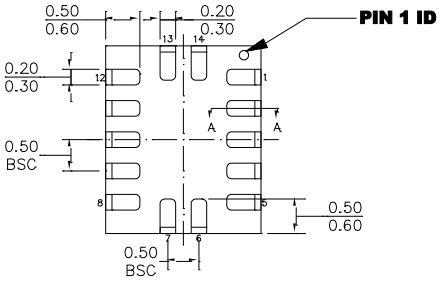
Figure 3: Typical Application Circuit (f_{SW} = 1.25MHz, V_{OUT} = 0.8V or 1.0V, FCCM)

PACKAGE INFORMATION

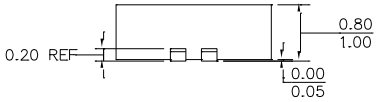
QFN-14 (2.5mmx3mm)
Wettable Flank



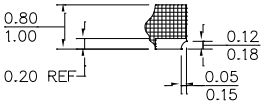
TOP VIEW



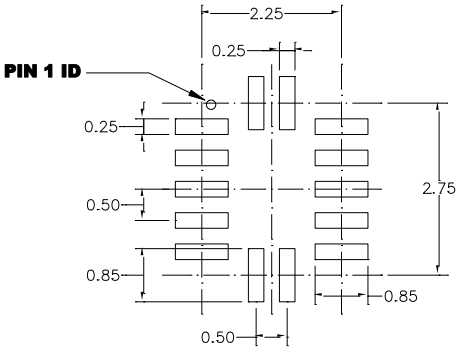
BOTTOM VIEW



SIDE VIEW



SECTION A-A

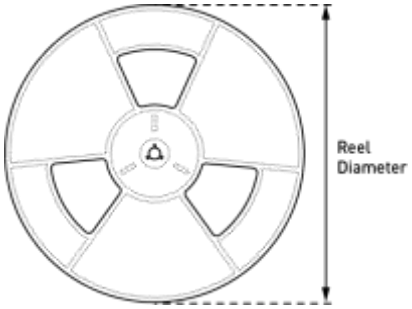


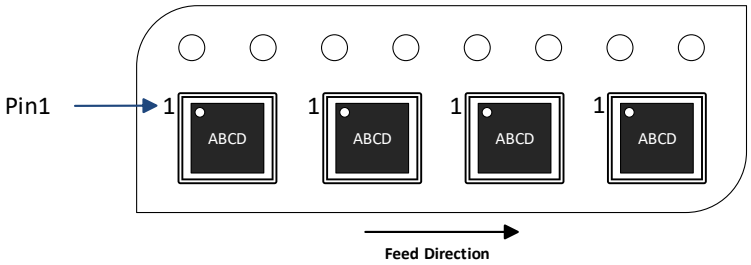
RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-220.
4) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION





Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ2180GQBE-8-AEC1-Z	QFN-14 (2.5mmx3mm)	5000	N/A	N/A	13in	12mm	8mm
MPQ2180GQBE-10-AEC1-Z							

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	3/7/2022	Initial Release	-